IEEE Transactions on Industrial Electronics, pp. 1–1, 2022

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2022.3170614, IEEE Transactions on Industrial Electronics

Shoot-Through Protection for an IGCT-Based ZVS Resonant DC Transformer

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***Abstract*—IGCTs have successfully demonstrated to be well-suited devices for an application in medium-voltage dc transformers based on LLC resonant converter topology. This application enables unusually high switching frequencies in kHz range thanks to the zero-voltage switching while maintaining the high conversion efficiency. Moreover, the clamp circuit that is an inseparable part of every hard-switched IGCT-based converter can be completely omitted – further lowering the converter complexity and cost. Nevertheless, without the clamp circuit, the effect of shoot-through becomes fatal, considering that the IGCTs have a defined mode of failure in short-circuit and the desaturation effect, is practically non-existent. To prevent the shoot-through, this letter proposes a simple, yet effective, protection method based on anode-voltage measurement that can be implemented locally on the IGCT gate unit. The validity of the solution is demonstrated using a custom IGCT gate unit in a medium-voltage resonant test setup.**

I. INTRODUCTION

THE LLC resonant converter operated in open loop near resonant frequency has been proposed as a solution for emerging dc transformer (DCT) applications several times in the literature [1]–[4]. This solution is preferable as it naturally provides a stiff voltage ratio with very good load rejection, galvanic isolation via a medium-voltage transformer (MFT), and high conversion efficiency due to zero-voltage switching (ZVS) specific for this converter topology. An example of a unidirectional DCT topology is depicted in Fig. 1.

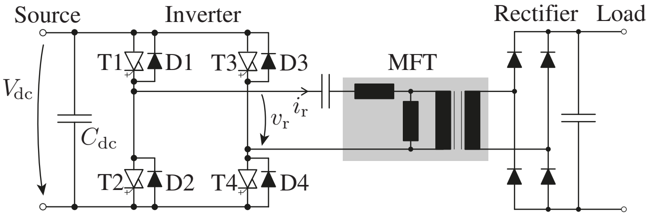

Fig. 1: Example of a unidirectional DCT based on LLC resonant topology utilizing H-bridge inverting stage with IGCTs.

To further maximize the conversion efficiency for medium-voltage applications, [5], [6] propose to utilize the integrated gate-commutated thyristors (IGCTs) in the inverting stage of the DCT. The IGCTs are advantageous as they provide lowest-in-class conduction losses and a high degree of reliability. Moreover, due to their press-pack packaging, they have very good thermal capabilities and a failure mode reliably defined as a short-circuit. Furthermore, the particular application in the resonant DCT enables an operation of this device at unusually high switching frequencies in a range of up to several kHz without significantly compromising the efficiency. Additionally, the resonant operation guarantees low $\mathrm{d}i/\mathrm{d}t$ of the switched current during turn ON, which in turn enables a possibility to omit the clamping circuitry that is otherwise required in all hard-switched applications.

While omitting the clamping circuitry reduces the cost and the complexity of the converter, it renders the converter to be significantly more sensitive to shoot-through. Typically, a shoot-through can occur when the switch turns ON, while the complementary switch has failed (IGCTs fail exclusively into short-circuit) or simply the turn-OFF delay was increased, e.g., due to increased junction temperature. Unlike IGBTs, IGCTs are thyristor-based switches and thus, they do not desaturate as signficantly with increasing current. Hence, IGCT-based converters usually rely on the clamping circuitry to limit the rate of the rise of the current during the failure, providing sufficient time to recognize the failure. In literature, many methods on measuring the devices' currents for the protection reasons can be found: based on external sensors [7], Rogowski coil integrated in gate unit [8], [9] or measurement of the ON-state voltage drop of the IGCT [10]. However, if the clamping circuit is omitted for soft-switching applications with IGCTs, the device's current rises too fast in a case of shoot-through, not providing sufficient time to recognize the necessity to turn OFF the device. Hence, another protection method has to be proposed, which is the subject of this letter.

The proposed protection method for an IGCT-based resonant DCT (patent pending) utilizes the (non-isolated) anode-voltage measurement to recognize whether the conditions to turn ON the IGCT are safe. Hence, the risk of a shoot-through is effectively eliminated, despite the absence of the clamping circuitry. Moreover, unlike the generic protection method from [9] that utilizes anode-voltage measurement as well, the method proposed here provides an option to implement the method locally on the gate unit without a necessity for additional communication channels with the central controller. This is expected to make the proposed method faster, more reliable, and cheaper. Hence, a reliable operation of the DCT without the clamping circuit is enabled.

The principle of the proposed protection method is explained in Section II and its practical implementation is

The results presented in this paper are a part of the EMPOWER project that has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (Grant agreement No. 818706).

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2022.3170614, IEEE Transactions on Industrial Electronics

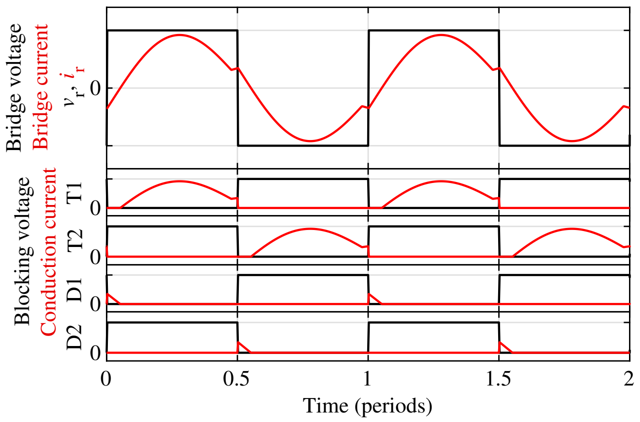

Fig. 2: Characteristic waveforms of the DCT: voltages and currents of the resonant tank and the switches of the first leg of the inverter.

presented in Section III. The method is validated on a medium-voltage test setup in Section IV. The conclusions are drawn in Section V.

II. PRINCIPLE OF THE PROPOSED PROTECTION METHOD

The principle of the protection method can be explained while observing typical waveforms in Fig. 2 of the example DCT from Fig. 1. The DCT is operated in an open loop at 50 % duty cycle and a switching frequency below the resonant frequency, which is the typical operation in constant-voltage-ratio DCT applications. When the parameters of the resonant tank are selected properly, such operation guarantees a good load-rejection properties and a ZVS turn ON for the switches while maintaining a constant low turn-off currents [1].

As Fig. 2 shows, the H-bridge generates rectangular voltage waveform v_r that is applied to the resonant tank consisting of two inductors (often integrated in a compact MFT) and the resonant capacitor. The resonant tank responds with a current i_r that is a superposition of a sinusoidal resonant current responsible for power transfer and an almost triangular “magnetizing” current that is independent of the converter loading. This “magnetizing” component of the current ensures that the current is positive during the IGCT turn off and thus, enables the ZVS turn ON for the topology.

Observing the voltages and currents of the switches T1 and T2 of the first H-bridge leg with corresponding diodes D1 and D2 in Fig. 2, the principle of ZVS can be highlighted: Each time when the switch (T1 or T2) turns OFF, the diode of the complementary switch (D2 or D1) starts conducting the bridge current i_r. Hence, when the complementary switch (T2 or T1) is turned ON after a short deadtime, the blocking voltage is already near zero as enforced by the conducting diode (this occurrence is described as ZVS). Not only does the ZVS eliminate the turn-ON losses of the switches and reverse-recovery losses of the diodes, the information that it provides can be exploited to assume the conduction state of the complementary switch.

The proposed protection method is to observe the conduction state of the antiparallel diode (D1 or D2) of a switch (T1 or T2) to determine whether the complementary switch (T2 or T1) has turned OFF successfully, signifying safe conditions for the next turn ON. This principle can be utilized because the ZVS property of the converter ensures that the antiparallel diode starts naturally conducting after the complementary switch is fully in the blocking mode. As a consequence, the switch is turned ON (after the corresponding dead time) only if its antiparallel diode is conducting. If the antiparallel diode is not conducting when the turn ON command is issued, an error state is activated, as this signifies that the complementary switch has possibly failed and the conditions for shoot-through are very likely.

The advantage of this method is that it can be executed locally on the gate unit of each IGCT, since all necessary information, i.e., conduction state of the antiparallel diode of the IGCT and the turn ON command, are available locally. Hence, the unsafe condition can be effectively recognized within the gate unit without any necessity for additional communication channels with the central controller. Not only does this decrease the reaction time (which is practically immediate) but it also reduces cost and reliability as the costly and mechanically sensitive fibre optic channels can be omitted.

The easiest way to recognize the conduction state of the antiparallel diode is by measuring the voltage drop over it (a certain threshold can be utilized to define the diode as conducting). This is especially effective because this voltage equals the anode-to-cathode voltage of the switch that is often measured by the gate unit to capture overvoltages [11] – leading to only small-impact required hardware changes on the gate unit. Moreover, this measurement can also be applied to reverse-conducting IGCTs (RC-IGCTs) that integrate the antiparallel diode in a single package.

Finally, it should be mentioned that the method is limited to the operating region where ZVS applies. Hence, if the duty-cycle reduction is used during a soft-start [12] or overload conditions [13], the converter parameters have to be selected in a manner to guarantee the ZVS also under these transient conditions or the method has to be temporarily disabled. At the same time, it should also be mentioned that the proposed principles can also be theoretically utilized in other topologies that provide ZVS turn ON.

Furthermore, the method does not provide any protection for a short-circuit directly at the MFT terminals. Nonetheless, such occurrence is relatively unlikely (and thus, tolerable), since the connection between the MFT and the inverter output can be done within the same cabinet.

III. IMPLEMENTATION OF THE PROTECTION METHOD

The method, that was described in the last section, can be implemented according to logic in Fig. 3 in an FPGA, which is an integral part of the most of the modern gate units.

As Fig. 3 shows, the logic waits until it obtains the turn ON command for the IGCT from the central controller. After, the logic checks if this is the first pulse that has been applied after turning ON the converter – as after restart of the converter,

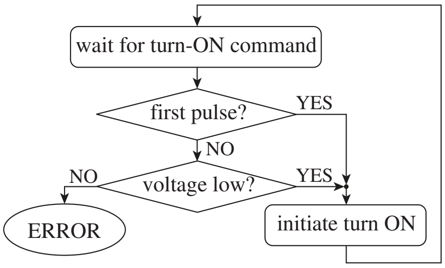

Fig. 3: Principle of the method.

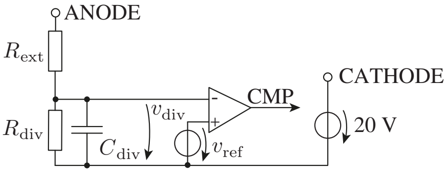

Fig. 4: Anode voltage measurement.

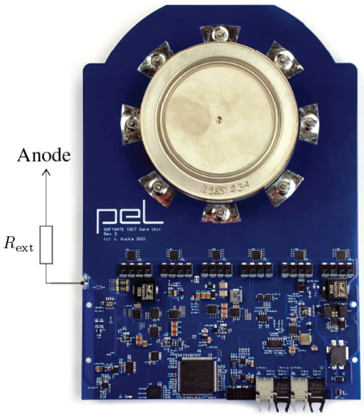

Fig. 5: *SOFTGATE* gate unit designed for soft-switching application with the Faston connection to the external 5 MΩ resistor R_{ext}.

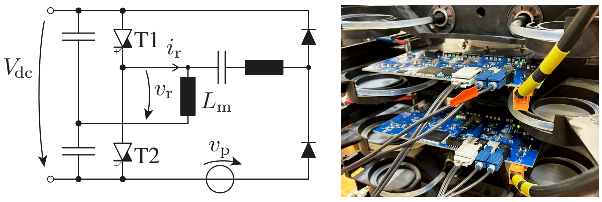

Fig. 6: Experimental test setup with reverse-conducting IGCTs (left: scheme; right: photo).

TABLE I: Parameters

Resonant frequency	1.6 kHz
Switching frequency	1.44 kHz
DC-link voltage	2 kV
Turn-off current	110 A
Peak resonant current	600 A
Deadtime	10 µs

the ZVS does not apply for the first pulse. If this is not the case and the measured voltage over the antiparallel diode is recognized as high, the error state is activated and the IGCT is kept in the turn-OFF state. Otherwise, the IGCT is turned ON by the typical turn-ON current pulse into the IGCT's gate.

In the example implementation, the voltage measurement, used for determining the antiparallel diode's conduction state, is realized using a voltage divider and a comparator, comparing to a constant threshold value [see Fig. 4], similarly as described in [11] for overvoltage detection. While the voltage divider can also be shared by the overvoltage detection circuit that is a part of many gate units, the comparator is dedicated for the proposed protection method and has to be implemented additionally. The 20 V offset to the cathode voltage visible in Fig. 4 is due to how the logic ground was selected on the unit. The comparator can be supplied from the available logic buses on the gate unit (in this example: 3.3 V).

The parameters of the circuit were selected as $R_{\mathrm{ext}} = 5\ \mathrm{M\Omega}$, $R_{\mathrm{div}} = 3.84\ \mathrm{k\Omega}$, and $C_{\mathrm{div}} = 100\ \mathrm{pF}$ to achieve a 770 mV/kV gain of the divider with a 414 kHz low-pass filtering. The gain was selected to obtain a reasonable voltage range without clipping at 3.3 V logic and the bandwidth is sufficiently high to track the rising and falling edges of the anode-to-cathode voltage which have typical rise and fall times of several microseconds.

The voltage of the divider v_{div} is compared to a constant value of 150 mV that represents a measured-voltage threshold of approx. 200 V below which the antiparallel diode is assumed as conducting. The voltage-detection signal "CMP" from comparator is connected directly to the FPGA (where the signal is further filtered by a 100 ns digital filter to remove the EMI), comprising the information whether the antiparallel diode's voltage is "low" or "high". Generally, the threshold value should be selected as low as possible to ensure that the diode is truly conducting. At the same time, however, the value should be sufficiently high to make the protection method more robust for the EMI. The 150 mV (200 V) threshold proved to be sufficient for the example design. However, this value should be understood as an example rather than an optimized general rule.

In Fig. 5, a picture of the developed gate unit for soft-switching IGCT applications *SOFTGATE* [14] is shown together with the connection point for the external medium-voltage 5 MΩ resistor.

IV. EXPERIMENTAL VALIDATION

To experimentally validate the application of the proposed method, a medium-voltage test setup from [6] was utilized. While the test setup does not directly process power, it enforces the same conditions on the IGCTs as the typical LLC resonant converter in DCT applications. The test setup is depicted in Fig. 6. The magnitude of the "magnetizing" current is adjusted by the inductance value L_{m}. The magnitude of the resonant pulse is adjusted by the voltage of the high-current direct voltage source v_{p}. The selected parameters of the setup are summarized in Table I.

To test the protection function, the test setup is operated in a typical open-loop operation until it reaches the rated power. After, the failure of IGCT T2 is emulated by forcing this IGCT to remain in the ON state.

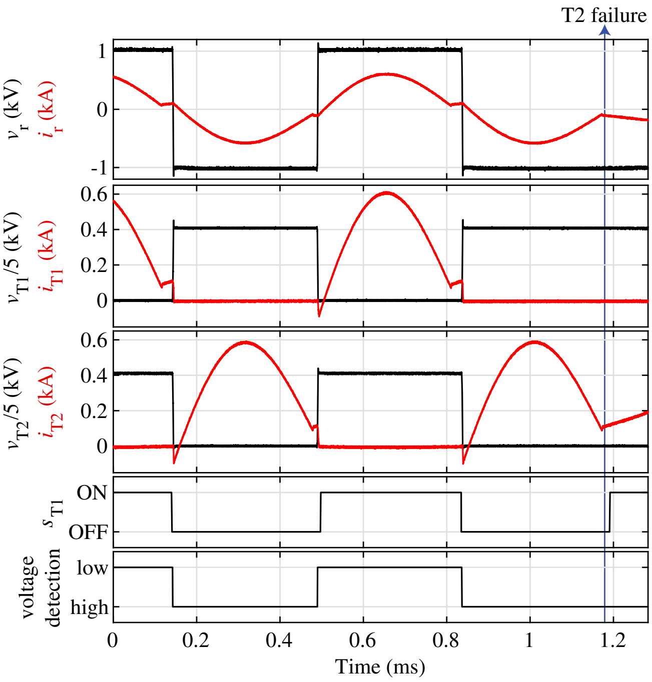

Fig. 7: Experimental validation of the protection function: the failure of switch IGCT T2 is emulated by keeping it turned ON after the point in time marked as “T2 failure”.

The measured waveforms are plotted in Fig. 7, showing the voltage and current waveforms in the resonant tank v_r, i_r, of the IGCTs T1 v_{T1}, i_{T1} and T2 v_{T2}, i_{T2}, the switching signal for IGCT T1 s_{T1}, generated by the central controller, and the state of the voltage-detection comparator on the gate unit of IGCT T1 “voltage detection signal” (signal “CMP” in Fig. 4).

As the results in Fig. 7 show, in the typical operation, the intrinsic antiparallel diode of the RC-IGCT T1 starts conducting after the turn OFF of the complementary IGCT T2. As the diode starts conducting, the IGCT blocking voltage v_{T1} drives the voltage detection to state “low”. When the switching signal initiates the turn ON command after the dead time by flipping to state “ON”, the voltage detection detects that the antiparallel diode is conducting and the protection method decides that it is safe to turn ON IGCT T1.

However, when the failure in IGCT T2 occurs, the intrinsic diode in T2 does not start conducting and thus, when the turn-ON command arrives, the protection method recognizes that it is unsafe to turn ON IGCT T1. As a consequence, the error state in the gate unit is assigned and the IGCT T1 remains in the blocking state.

Because of the failure in IGCT T2, its current keeps rising but with a $\mathrm{d}i/\mathrm{d}t$ limited by the resonant tank, which provides enough time for the central controller to take some action or for a fuse to activate.

V. CONCLUSIONS

This paper has proposed a simple, yet effective, shoot-through protection method (patent pending) that can be utilized in ZVS IGCT applications, such as an LLC-converter-based resonant DCT. The method can be implemented completely on the gate unit, effectively cutting the requirements for additional communication channels towards the central controller. The proposed protection was validated experimentally on a medium-voltage test setup, which demonstrated its applicability in the target applications. Finally, the proposed method enables the option to omit the clamping circuit, as the fatal shoot-through failure is effectively eliminated. As a consequence, the total footprint and cost of the converter are expected to be reduced.

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