

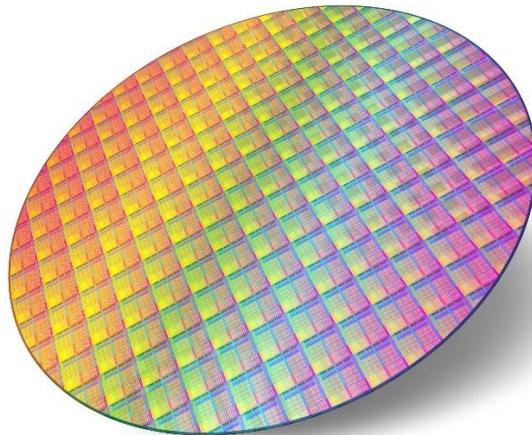


ECOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

ANEMS Laboratory

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*Characterization of thin film stress for MEMS planarization*



Presented to:

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## **Abstract**

The synthesis and stress characterization of metal thin-films deposited on silicon wafers were performed on this project. Two different deposition techniques were employed: magnetron sputtering and Atomic Layer Deposition (ALD). Moreover, different tests were executed varying deposition conditions, such as temperature and deposition equipment. On the other hand, the metal thin-film's thickness was also varied. The previous experiments provided us with an in-depth understanding of how the stress of a certain metal thin-film deposited on another different metal can be affected by such mentioned conditions. For our study, the stresses of fourteen metal thin-films were computed, this involves Aluminum Nitride (AlN), Platinum (Pt), Alumina ( $\text{Al}_2\text{O}_3$ ) and double-component based thin-films such as AlN/Pt and Ti/Pt.

**Key words:** Magnetron Sputtering, Atomic Layer Deposition (ALD), stress, curvature.

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## **1. Introduction**

Thin films and multilayers are widely used in technology, and their mechanical performance under severe environmental conditions often dictates design. Examples include electronic packages, coatings for thermal, chemical or abrasion protection, among others. [1]

Stress is a physical magnitude that expresses the internal forces that neighboring particles of a continuous material exert on each other. In thin films and multilayers the stress have three primary origins: intrinsic, thermal and mechanical. Intrinsic and thermal stresses are often referred to as residual stresses [1, 2].

Intrinsic stresses arise during the deposition process, which include sputtering, spraying, painting, spin coating, vapor deposition, and electro-deposition. These processes are used to create films and multilayers from metals, ceramics, polymers and intermetallic. Depending on the process, the deposition temperature can be "low" or "high" or room temperature. Intrinsic stresses are distinct from thermal stresses in that they are the stresses present at the deposition temperature [2]. The mechanisms which generate intrinsic stresses are not well characterized quantitatively. They include grain growth, defect annihilation, phase transition, and evaporation of a solvent [1].

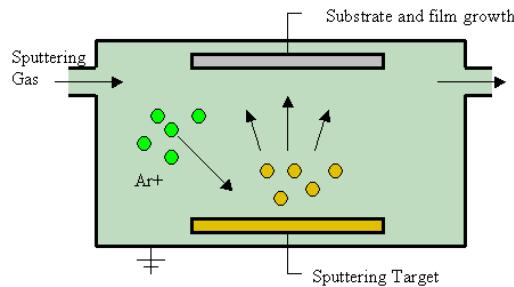
The presence of stress in thin films constitutes a major concern in many technological applications, as excessive residual stress levels can dramatically affect the performance, reliability, and durability of material components and devices. Worst scenarios lead to film cracking for layers subjected to tensile stress or peeling off, buckling or blistering in case of compressive stress. Residual stress distribution can significantly impact the adhesion and the fracture toughness of thin films and the resonance frequency of Micro- and Nanoelectromechanical devices (MEMS and NEMS).

Alternately, stress can have beneficial influence on the physical properties of thin layers such as conductivity, dielectric permittivity, piezoelectricity, magnetic anisotropy and or enhancement in charge carrier mobility in silicon-based semiconductor technology. Therefore, there is a significant motivation to understand the origin of stress in thin films as it can directly affect the design, processing, and lifetime of advanced materials and

components [3]. In this project, the stresses of different deposited materials are studied in order to optimize the deposition process to obtain flat and smoother thin-film surfaces.

## Sputtering

Sputtering is a PVD (Physical Vapor Deposition) class of thin film deposition technology. The material to be coated, the sputtering “target”, is bombarded with plasma ions and the removed particles enter into the gas phase. In other words, atoms are ejected from a target and they have a wide energy distribution of tens of eV. The vapor then condenses on the surface of a “substrate” such as a silicon wafer, adheres to it firmly and forms a thin layer. The process occurs in a vacuum chamber (figure 1). The sputtering gas is often an inert gas such as Argon. This process enables uniform applications of diverse substances (metals, alloys, oxides and nitrides) on a wide variety of substances; from semiconductor wafers to architectural glass [4].



**Figure 1. Schematic of standard sputtering deposition.[5]**

## Atomic Layer Deposition

Atomic layer deposition (ALD) is a vapor phase technique capable of producing thin films of a variety of materials. Based on sequential, self-limiting reactions, ALD offers exceptional conformality on high-aspect ratio structures, thickness control at the Angstrom level, and tunable film composition [6].

Figure 2 illustrates the steps of ALD. It consists of sequential alternating pulses of gaseous chemical precursors that react with the substrate. These individual gas-surface reactions are called ‘half-reactions’ and appropriately make up only part of the materials synthesis. During each half-reaction, the precursor is pulsed into a chamber under vacuum (<1 Torr) for a designated amount of time to allow the precursor to fully react with the substrate surface

through a self-limiting process that leaves no more than one monolayer at the surface. Subsequently, the chamber is purged with an inert carrier gas (typically N<sub>2</sub> or Ar) to remove any unreacted precursor or reaction by-products. This is then followed by the counter-reactant precursor pulse and purge, creating up to one layer of the desired material. This process is then cycled until the appropriate film thickness is achieved. Typically, ALD processes are conducted at modest temperatures (<350 °C). The temperature range where the growth is saturated depends on the specific ALD process and is referred to as the ‘ALD temperature window’. Temperatures outside of the window generally result in poor growth rates and non-ALD type deposition due to effects such as slow reaction kinetics or precursor condensation (at low temperature) and thermal decomposition or rapid desorption of the precursor (at high temperature). In order to benefit from the many advantages of ALD, it is desirable to operate within the designated ALD window for each deposition process [6].

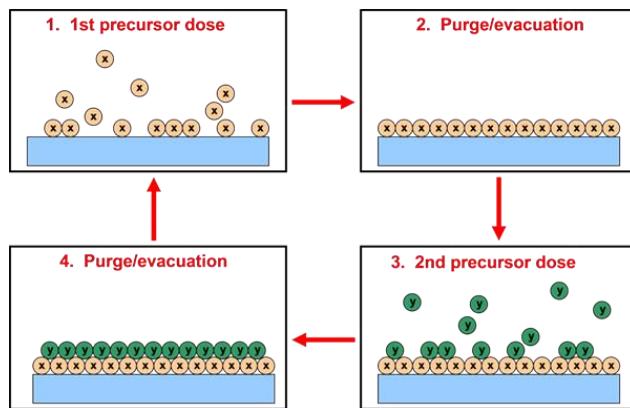


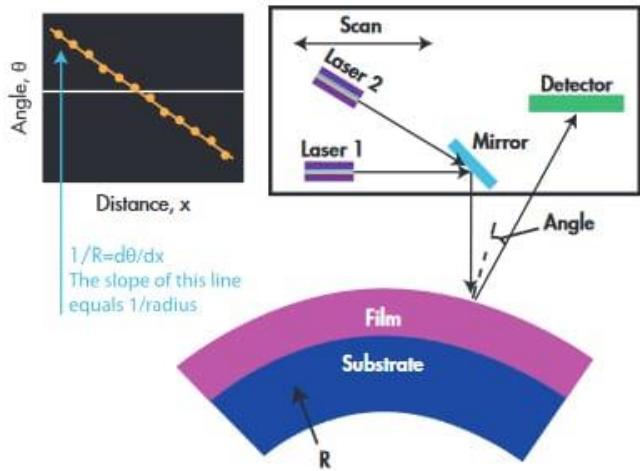
Figure 2. Schematic of Atomic Layer Deposition Process [7]

### Optical profilometry for stress measurement

In order to compute the stress of a thin film, an optical profilometer employs a laser scanner to measure the changes in the radius of curvature of the substrate caused by the deposition of a thin film on the wafer (Figure 3). This is accomplished by first measuring the wafer curvature before the film is deposited and then re-measuring the curvature after the film is deposited [8]. The standard relation which infers film stress from substrate curvature changes is known as the Stoney formula (equation 1). This relation describes a plate system composed of a stress-bearing thin film of uniform thickness  $t$ , deposited on a relatively thick substrate of uniform thickness  $h$ :

$$\sigma = \frac{Eh^2}{6Rt(1-\nu)} \quad Eq. 1$$

Where  $E$  is the Young's modulus of the wafer material,  $R$  is the wafer radius of curvature, and  $\nu$  is the Poisson's ratio [9].



**Figure 3. Optical Profilometer for thin film curvature and stress characterization [10]**

## 2. Methods

All the thin film depositions and stress characterizations for this project were performed within the facilities of the Center for MicroNanotechnologies (CMi) at EPFL. For the thin film deposition through sputtering, two different tools were employed: [Pfeiffer SPIDER600](#) and [Alliance concept DP650](#). Besides sputtering, the ALD machine that was used is [BENEQ TF200](#), and for stress and curvature characterization we used the Toho Technology FLX 2320-S.

In this project, six silicon wafers (a-f) were used to deposit multilayers as described in table 1 and illustrated in figure 4. Table 1 indicates the thin-film's material, thickness and deposition temperature. Moreover, when it comes to depositions, the color of the table entry indicates the equipment employed: Purple is assigned for the *Alliance concept DP650*, dark green for *Pfeiffer SPIDER600* and pink for the *BENEQ TF200*.

As it can be observed, between the films depositions, stress measurements were performed (step: 1, 3, 6 and 8). For every wafer, 3 measurements were obtained by rotating the wafer in

3 different orientations: 0°, 45°, 90° degrees. The purpose of this practice is obtaining a precise measurement of the stress and observe repetition in the numerical value for verification.

**Table 1. Processes and measurements performed in different silicon wafers for this project**

	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8
a)	<i>C</i>	AlN/Pt 15nm/25nm 25°C	<i>S</i>	AlN 500nm <i>300 °C</i>		<i>S</i>		<i>S</i>
b)		AlN/Pt 15nm/25nm 25°C		AlN 500nm <i>300 °C</i>	Pt 200nm <i>300°C</i>		<i>T</i>	
c)	<i>V</i>	Ti/Pt 15nm/25nm 25°C	<i>R</i>	AlN 500nm <i>300 °C</i>		<i>R</i>		<i>R</i>
d)		Ti/Pt 15nm/25nm 25°C		AlN 500nm <i>300 °C</i>	Pt 200nm <i>300°C</i>		<i>E</i>	
e)	<i>U</i>	Ti/Pt 15nm/25nm 25°C	<i>S</i>	AlN 500nm <i>300 °C</i>	Pt 200nm 25°C	<i>S</i>	<i>Al<sub>3</sub>O<sub>2</sub></i> 30nm 200°C	<i>S</i>
f)		Ti/Pt 15nm/25nm 25°C		AlN 500nm <i>300 °C</i>	Pt 200nm 25°C		<i>Al<sub>3</sub>O<sub>2</sub></i> 50nm 200°C	

Figure 4 illustrates the arrangement and process flow for every wafer described in table 1, the numbers in red in such figure indicate the thin-film's stresses of interest for this project. These numbers are between the layers of study, which means that we are analyzing the stress of the layer above the number over the one that is below. In the cases of the numbers 3, 8 and 11 (labeled with \*) we are considering the system AlN/Pt (500nm/200nm) as one layer. Observe that in the previous cases, the layers are deposited over different thin films: AlN/Pt in 3 and Ti/Pt for 8 and 11. The deposition temperature is also different. For this reason, it is important to understand how stress varies with this parameters.

### Pfeiffer SPIDER600

The thickness of the thin film is time-dependent and the deposition rate varies depending of the material. In order to obtain the 15 nm of AlN and the 25 nm of Pt at room temperature (step 2, wafers a and b), we employed a recipe with 18s of AlN deposition and 14s for the Pt

deposited on top. The flow of argon during the deposition was 10 sccm in the case of AlN and 5 sccm for the Pt. The sputtering power was 1500W for the AlN and 500W for the Pt.

For the depositions of step 4, in order to obtain 500 nm of AlN at 300°C, the deposition time was 10 minutes with a flow of argon of 10 sccm and a sputtering power of 1500W.

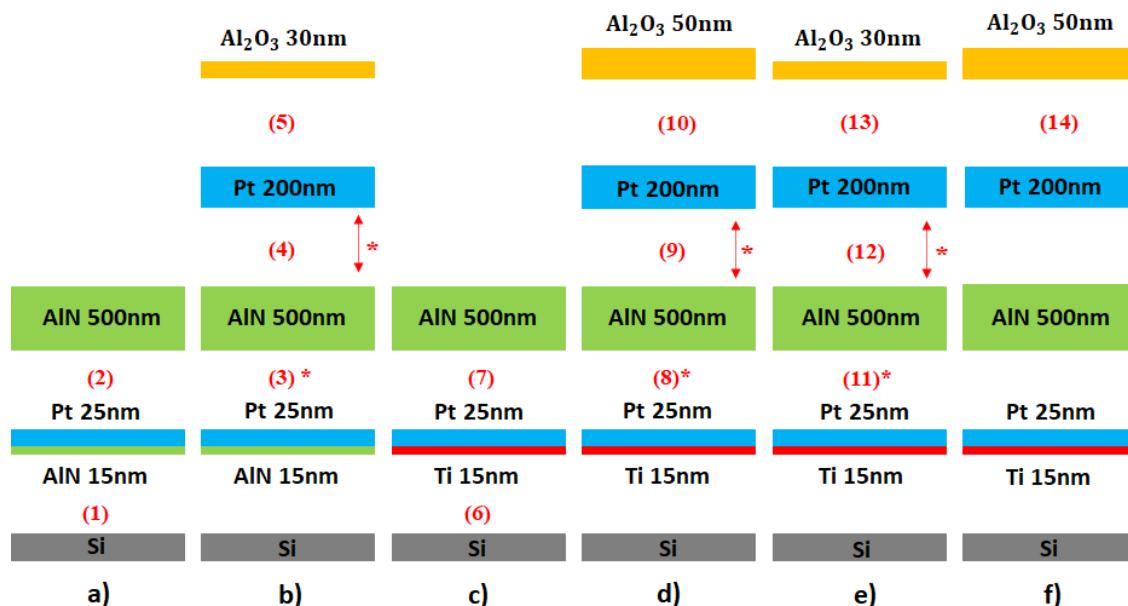
On the other hand, for step 5 (wafers b, d, e and f), that corresponds to a 200 nm Pt top-layer, a deposition time of 48s was employed. The sputtering power was 1000W at room temperature (wafers e and f) and 1500W at 300°C (wafers b and d), the argon flow was 15 sccm at room temperature and 10 sccm at 300°C.

## DP650

In the case of the wafers c-f (see table 1), the recipe employed to deposit the system of layers Ti/Pt at room temperature in step 2, we employed the following parameters: 48s to deposit 15nm of titanium and 37s to deposit 25 nm of Pt.

### Atomic layer deposition (ALD)

The last material to be deposited on the wafers (b, d, e and f) is alumina  $Al_3O_2$ , this material has a deposition rate of 1.15 (Å/cycle). In order to deposit the alumina layers at 200°C, 435 cycles were needed to achieve a 50 nm thickness and 260 cycles for 30nm.



**Figure 4. Overview of the depositions performed in every wafer and the stresses measured.**

### 3. Results and discussions

The stresses obtained for the different thin films are described in table 2. Since the system AlN/Pt (500nm/200nm) was deposited as a whole (without unloading the wafer from the sputtering machine), an analytical calculation was performed to compute the stress of Pt over AlN (see supplementary material)

**Table 2. Summary of key stresses obtained in each wafer**

Number	Wafer	Bottom layer description	Top layer description	Stress (MPa)
1	A	<b>Si</b> (wafer)	<b>AlN/Pt</b> (15nm, 25°C/25nm, 25°C)	-212.28
2	A	<b>AlN/Pt</b> (15nm, 25°C/25nm, 25°C)	<b>AlN</b> (500nm, 300°C)	-29.45
3*	B	<b>AlN/Pt</b> (15nm, 25°C/25nm, 25°C)	<b>AlN/Pt</b> (500nm, 300°C/200nm, 300°C)	-47.28
4	B	<b>AlN</b> (500nm, 300°C)	<b>Pt</b> (200nm, 300°C)	165
5	B	<b>Pt</b> (200nm, 300°C)	<b>Al<sub>3</sub>O<sub>2</sub></b> (30nm, 200°C)	21.63
6	C	<b>Si</b> (wafer)	<b>Ti/Pt</b> (15nm, 25°C/25nm, 25°C)	-84.67
7	C	<b>Ti/Pt</b> (15nm, 25°C/25nm, 25°C)	<b>AlN</b> (500nm, 300°C)	-81.56
8*	D	<b>Pt/Ti</b> (15nm, 25°C/25nm, 25°C)	<b>AlN/Pt</b> (500nm, 300°C/200nm, 300°C)	-56.87
9	D	<b>AlN</b> (500nm, 300°C)	<b>Pt</b> (200nm, 300°C)	-199
10	D	<b>Pt</b> (200nm, 300°C)	<b>Al<sub>3</sub>O<sub>2</sub></b> (50nm, 200°C)	23.81
11*	E	<b>Ti/Pt</b> (15nm, 25°C/25nm, 25°C)	<b>AlN/Pt</b> (500nm, 300°C/200nm, 25°C)	-27.36
12	E	<b>AlN</b> (500nm, 300°C)	<b>Pt</b> (200nm, 25°C)	-95
13	E	<b>Pt</b> (200nm, 25°C)	<b>Al<sub>3</sub>O<sub>2</sub></b> (30nm, 200°C)	3.04
14	F	<b>Pt</b> (200nm, 25°C)	<b>Al<sub>3</sub>O<sub>2</sub></b> (50nm, 200°C)	32.25

From the data obtained, we can make some comparations between the thin-films' stresses according to their synthesis parameters. As a first instance, the stress generated by the layer AlN/Pt over Si (-212.18 MPa) has a lower value than that generated by Ti/Pt over Si (-84.67 MPa). Both thin films have the same thickness, however, the fact of changing the AlN for Ti, creates an stress over the wafer that is closer to be zero.

Another interesting result is the stress produced by the 500 nm AlN film over two different materials. This layer produces an stress of -29.45 MPa when deposited over AlN/Pt and -81.56 MPa when it is deposited over Ti/Pt, this result is mostly in the same range.

In the case of the layer of platinum of 200nm deposited over the 500nm AlN layer, we obtained two different stresses. This result is probably generated by the difference of temperature of the top layer (platinum) during the deposition. The stress (9), which corresponds to a temperature of 300°C has a value of -199 MPa over the AlN, whereas the stress (12) produced by Pt deposited at room temperature has a value closer to zero, it is -95MPa, which is also half the stress of the previously mentioned.

In order to have a better appreciation of the results, observe figure 5. The stresses in color red represent the stress produced by the final top layer for each wafer. As we can see, the wafer e, has an stress of 3.04 MPa generated by the 30nm Alumina layer over the platinum. This wafer has the lowest stress, since it is closest to be zero. For the other wafers, the stress produced by the alumina is almost in the same range: 21.63 MPa for b, 23.81 MPa for e and 32.25 MPa for f.



**Figure 5. Overview of the stress obtained.**

## **Conclusion**

The results of this project demonstrate that the stress produced by certain metal thin-film can be affected by the deposition conditions.

In general, the system AlN/Pt causes a greater negative stress when deposited on silicon than the system Ti/Pt, when deposited on the same material.

Temperature of deposition might cause a variation in the stress produced by metal thin-films as well. This was observed when depositing Pt at two different temperatures over AlN. Increasing the deposition temperature from 25°C to 300°C resulted in a duplication of the negative stress, -95 MPa and 195 MPa respectively.

On the other hand, it was observed that the thickness of the deposited film will affect the stress as well. For instance, the alumina top layer produced an stress of 3.04 MPa when its thickness was 30 nm, and increased to 32.23 MPa when its thickness was 50 nm. This observation was extracted from wafer e and f respectively, where the layer systems have the same deposition parameters except for the last deposited layer that corresponds to the alumina.

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