Fabrication of new generation particle detectors

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1 Abstract

This project presents a microfabrication method for new generation particle detectors. This microsystem is supposed to detect ionizing radiation such as alpha particles, beta particles, and gamma rays. This project aims to miniaturized the otherwise well known Geiger counter instrument used for detecting and measuring ionization radiation. This report will identify each step of the fabrication, from the silicon wafer to the finalised microsystem, while explaining the potential problems inside the cleanroom and what needs to be avoided in order to get a desired final product. The whole microfabrication process was carried out inside the CMi at EPFL throughout the semester.

2 Introduction

A Geiger counter (Geiger-Muller tube) is a device used for the detection and measurement of all types of radiation: alpha, beta and gamma radiation. It consists of a pair of electrodes surrounded by a gas (typically Helium or Argon), with the electrodes having a high voltage across them. When ionizing radiation such as an alpha, beta or gamma particle enters the tube, it can ionize some of the gas molecules inside. Due to these ionized atoms, an electron is knocked out of the atom, and the remaining atom is positively charged [1]. The high voltage in the tube produces an electric field inside the tube.
The electrons that were knocked out of the atom are attracted to the positive electrode, and the positively charged ions are attracted to the negative electrode. This produces a pulse of current in the wires connecting the electrodes, and this pulse is counted. After the pulse is counted, the charged ions become neutralized, and the Geiger counter is ready to record another pulse.

The goal of this project is to create a micrometer version of the Geiger counter. The microfabrication process is still in the research and development phase but we were able to create the desired product at the end of the semester's internship.

3 Project identification

3.1 Goal of the project

The goal of the project lays within two main points :

- Create the desired microsystem.
- Analyze which problems we experienced and find ways to resolve them.

In order to achieve our desired goal, we first created a process flow that could explain step by step the fabrication method. This process would be carried out inside the CMi facility throughout the semester. Each steps can be found at the annex, at the end of the report.
After almost each fabrication steps, either SEM or optical microscope images were taken in order to get more accurate information.
The desired final structure can be found in figure 1.

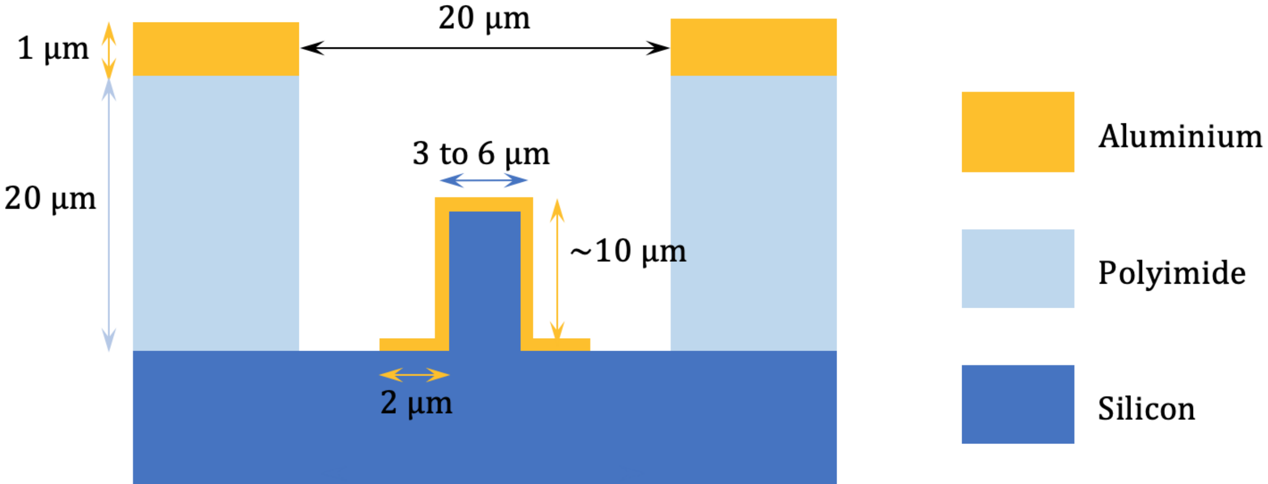


Figure 1: Final structure showing silicon pillars covered in Aluminium around a thick Polyimide layer

In this project, 4 different silicon pillar sizes were tested, ranging from 3 to 6 micrometers (3, 4, 5 and 6 μm). The purpose of the size dissimilarity was to see any noticeable difference at the end of the fabrication process between the structure of the pillars. A thin Aluminium layer (about 600 nm) needed to cover all of the silicon pillars, and a 20 μm Polyimide layer was coated all around them. Finally, a 1 μm Aluminium layer needed to be sputtered on top of the Polyimide layer.

3.2 Process flow and photolithography masks

The process flow in itself has approximately 20 steps, but some machines were used several times during the process. Indeed, three different photolithography steps were necessary in this process and each of them involved the same machines.
Three masks were designed on a software programm called K-layout. Chips of 4 arrays of 20x20 silicon pillars were designed (figure 2), with each array having its own pillar diameter size ranging from 3 to 6 micrometers. These four quadrants were seperated by a cross, and this greatly helped to identify each array under optical microscope. 49 of these chips were microfabricated on one single 4inch HiRes Si wafer. Additional masks images can be found in the annex as well.

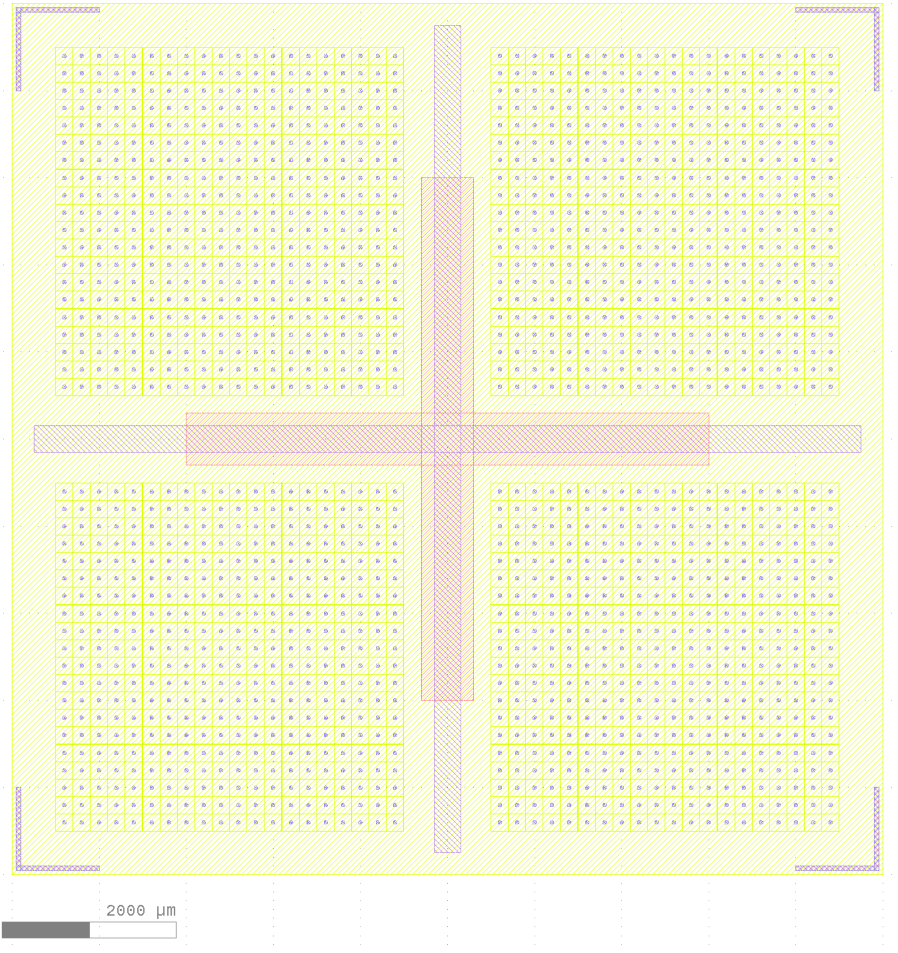


Figure 2: 4 arrays of different pillar size separated by a cross, visualisation on K-Layout (top left: 3 μm, top right : 4 μm, bottom left : 5 μm, bottom right : 6 μm)

4 Microfabrication steps

We used 2 HiRes Silicon wafers for the semester project. In case one of the wafer would break or be unusable, we could always count on the second wafer to continue our research.

4.1 Step 1 - 1st Photoresist coating

This is the first microfabrication step. This photoresist coating purpose was to create the silicon pillars. The resist used was AZ ECI 3007, we coated a thickness of 1 μm, which is thick enough as the selectivity to mask ratio between silicon and the photoresist is about 75:1. The machine used was the ACS200 Gen3, which has all the necessary tools to process the wafers.

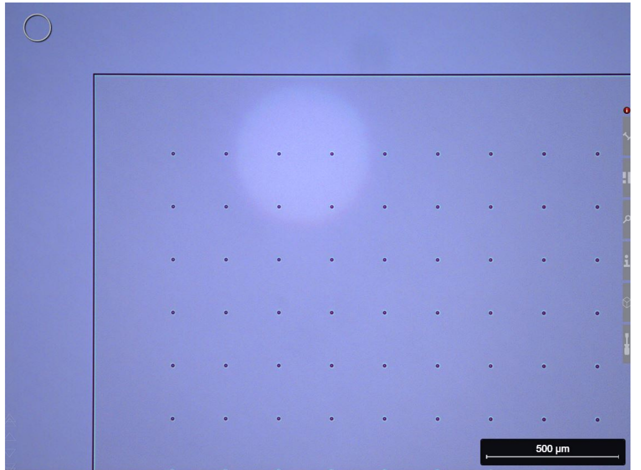
4.2 Step 2 - 1st Exposure

In order to get the desired size for the silicon pillars, exposure was needed. Initially, the exposure was supposed to be done on the MLA150, a new generation mask-less aligner. This system allows researchers to quickly print a design, without the need to order or produce a mask, by exposing

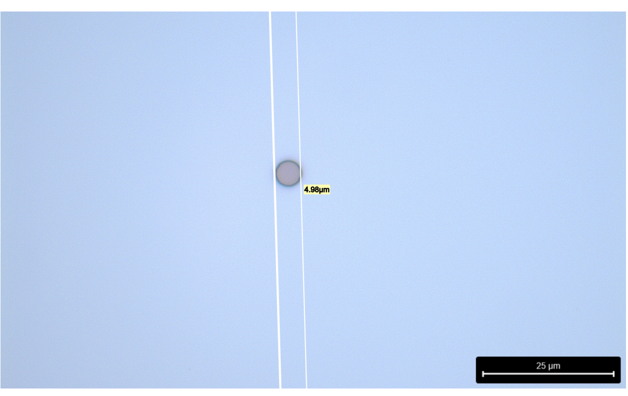
the photoresist with a UV laser focussed and scanned over the wafer. However, this process can be rather long, and in our case most of the resist needed to be exposed, so we opted out for the use of a photo-lithography mask. Since the process flow required three different lithography processes, we fabricated all of the masks at the beginning of the project. The Suss MA6Gen3 was the machine used for the exposure. The parallelism between the wafer and the mask is achieved with the help of an automated Wedge Error Correction. The resolution is limited by light diffraction through the mask opening, and can reach a minimum of about 800 nm, which is enough in our case because the smallest structure size is 3 μm.

4.3 Step 3 - 1st Development

The development was done on the same machine used for coating, which is the ACS200. This step is mandatory in order to get rid of the photoresist left. Moreover, once the wafer is developed, a rinsing bath should be done to be sure any left over resist is gone. Optical images were taken (see figure 3) and it showed that no critical issues occured during the first 3 steps. There was however some tiny (less than 1 μm in size) resist residues in unwanted places. We could have placed the wafer right after development inside the Tepla (resist etcher) to remove the residues by applying a low power etching process for 5-10 seconds.



(a) Raws and columns of circular photoresists for the future formation of the silicon pillars



(b) Zoom in on a 5um diameter photoresist structure

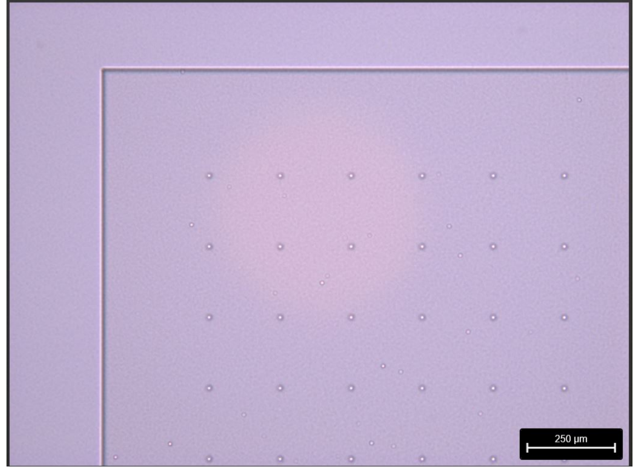
Figure 3: Optical microscope images taken after development revealing the circular photoresist structures.

4.4 Step 4 - Silicon etching

This was the process that consists in etching the silicon parts that were not covered by the resist in order to reveal the formation of silicon pillars. The desired height of the pillars were between 5 to 10 micrometers. We used the AMS 200 etcher which is an optimized Deep Reactive Ion Etching (DRIE) system for Silicon (Si) and Silicon on Insulator (SOI) wafers. The recipe was SOI-accurate++ and the etching time was 1 minute and 20 seconds. After visualisation using the optical microscope, the average height of the pillars ranged from around 6 up to 7.5 micrometers,

which was in our desired spectrum.

An important point here is that even though the silicon pillars were well fabricated (figure 4), silicon under-etching occured. Even though DRIE is an anisotropic process, optical images showed that the silicon pillars had a diameter slightly under the desired values. Indeed, all silicon pillars saw a decrease of around 500 nanometers in diameter from their desired size, i.e for an initial resist circle of 4 μm, the resulted pillar after etching was around 3.5 μm.
If your aim is to create a pillar of a certain size, make sure the diameter of the resist circle is slightly larger (around 0.5 μm more) if you plan to use DRIE.



(a) Formation of silicon pillars after silicon etching using the AMS200

(b) Close up of a 6 μm silicon pillar

Figure 4: Optical microscope images after silicon etching and resist stripping revealing the circular pillars.

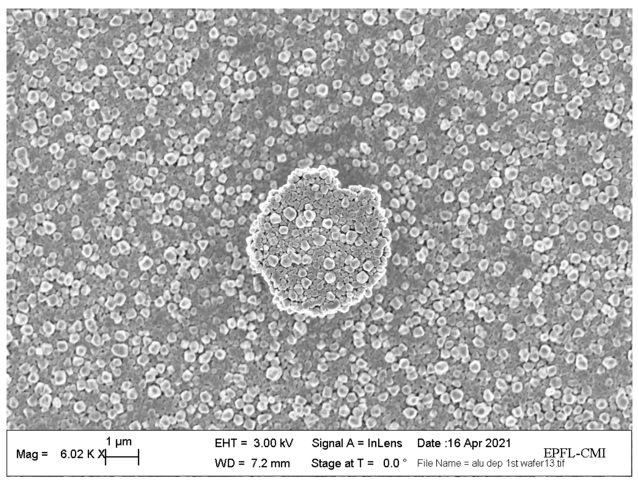
4.5 Step 5 - 1st resist stripping

The resist stripping is done on the Tepla GiGAbatch. The resist thickness was 1 micrometer, so we used the "resist strip low power" recipe for 5 minutes. This process etches between 100 nm to 500 nm per minute. In our case, the resist on our wafers was fully etched after 5 minutes.

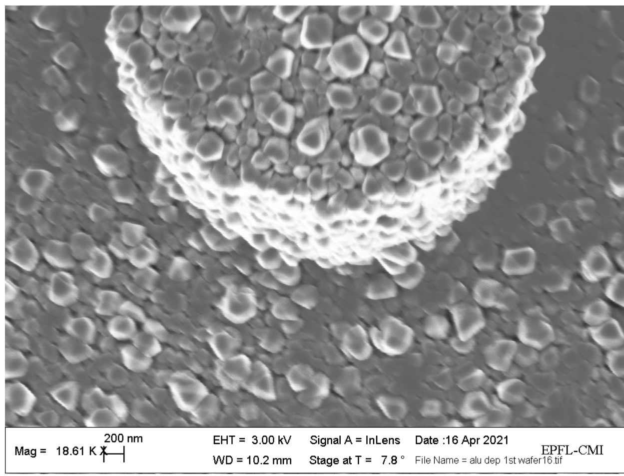
4.6 Step 6 - Sputtering of Titanium/Aluminium

This fabrication step is one of the most decisive one. The goal was to sputter aluminium around the whole silicon pillars (the top surface as well as the lateral surface). We sputtered first a 20 nm thick titanium layer first in order to have a more adhesive surface for aluminium. The difficulty was to have a good aluminium coverage on the Si pillars because sputtering is mostly unidirectional (vertical), which means that lateral surfaces might not get enough coverage. The desired aluminium layer thickness was between 500 nm to 1 μm. We opted for a thickness of around 600 nm to see if the coverage was already enough, if not another aluminium sputtering would have been done.

Several SEM images (see figure 5) were captured after the sputtering process to see if the aluminium layer did cover all the surfaces of the silicon pillars. We also tilted the wafer to see if aluminium covered the lateral surfaces of the pillars. After review, the aluminium coverage was close to 100% so we didn't need to sputter a second aluminium layer.



(a) 3 μm diameter silicon pillar covered by aluminium



(b) Vertical surface of a silicon pillar covered by aluminium

Figure 5: SEM images taken after Aluminium sputtering covering the silicon pillars)

4.7 Step 7 to 9 - 2nd Photoresist coating, exposure and development

The second photolithograpy steps were needed in order to etch most of the aluminium part. The place where aluminium was important was on the silicon pillars as well as the base of the pillars. The second mask was designed in order to also keep 2 μm of aluminium around the base of all the pillars. The photoresist used was the AZ 10XT-60 with a thickness of 20 μm. The rather thick layer of resist was needed in order to sufficiently cover the silicon pillars. Indeed, if the resist layer was too thin, the top part of the silicon pillars would have been exposed to the outside air instead of being covered by the resist, which would have been critical for the next steps in this process flow.

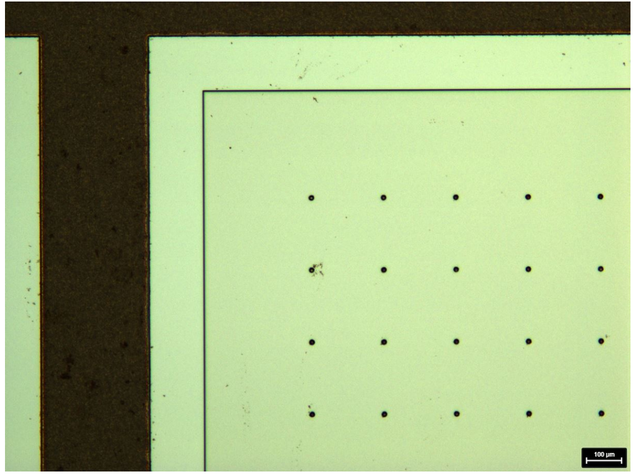
The 2nd exposure was also done on the Suss MA6Gen3 mask aligner. A manual alignment was first done with the help of an optical microscope as well as an automated process.

The development was once again done on the ACS200. Additionnaly, the newly developped wafer received right after a rinsing bath. Optical microscope images were taken after drying to see if the development was successful.
After analyzing the images, it seemed that the aluminium was already mostly etched during the development phase. Indeed, most NaOH-, KOH-, or TMAH-based developers attack Aluminium at a rate of approximately 50-100 nm/min, sensitive processes require an Al-compatible developer with very low Al attack [2]. In our case, the developer was not Al-compatible, thus most of the aluminium layer was already etched right after the development.

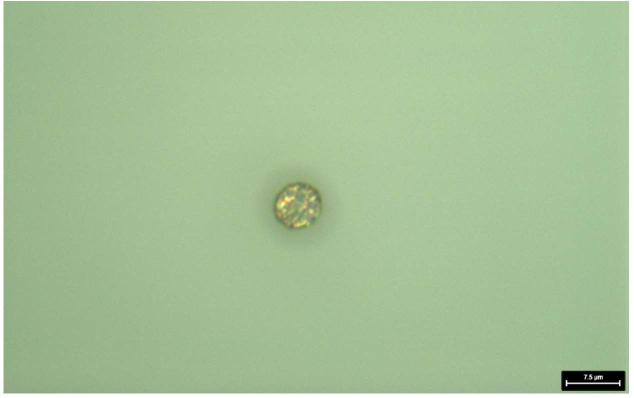
4.8 Step 10 - Aluminium and titanium wet etching

Wet etching was performed to remove all the left-over aliminium and the thin titanium adhesion layer. It is always recommended to perform a low power resist etching process in order to get rid of resist residuals in unwanted areas. Using the baths of the plade metal, we first wet etched the aluminium using the ANP bath, which has its own heating system. This bath etches aluminium at an average rate of 300nm/minutes. With the initial Al layer being around 600 nm, we let the wafer stay in the bath for approximately 2 minutes, knowing that the aluminium was already mostly etched. We didn't see any thin aluminium film separating itself from the wafer, meaning that probably most of the Aluminium was already gone.
For the titanium bath we used diluted HF at room temperature, in our case the 20 nm titanium layer was etched after approximately 20 seconds. The chemical reaction was visible and the change in the colour's wafer inside the bath was also slightly noticeable.

After reviewing microscope images, we could see that there was no Aluminium left at the base of the silicon pillars (figure 6b). The most plausible reason is that the Aluminium next to the pillar was both etched under the resist layer during the 2nd development (due to the developer not being Al-compatible) as well as during the wet ANP etching bath. Two options can resolve this problem, either use a developer that is Al-compatible or increase the resist diameter in order to have a wider aluminium layer at the base of the pillar.



(a) Post wet etching process with resist still on the wafer



(b) Silicon pillar covered in aluminium after resist stripping

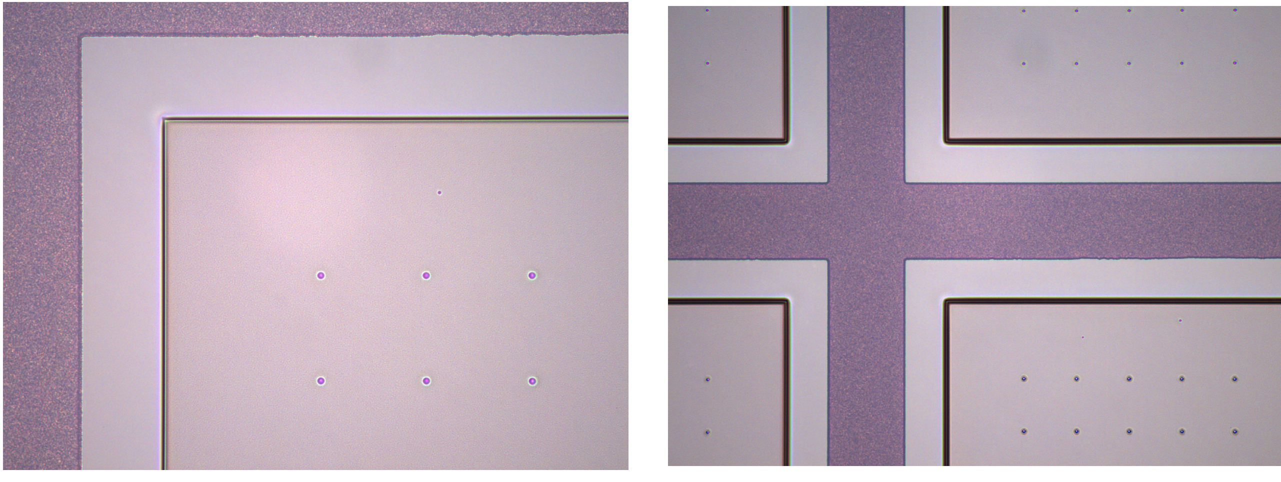
Figure 6: Optical microscope images after 2nd wet etching revealing the Aluminium covered pillars

4.9 Step 11 - 2nd resist stripping

Resist stripping was done inside the Tepla GiGAbatch. Because the thickness of the resist was 20 micrometers, the recipe was put on high power with a time of 30 minutes. Optical microscope images revealed that all of the photoresists was gone after the stripping process.

4.10 Step 12 - Polyimide deposition

The polyimide deposition was a critical step in order to obtain the final prototype. We aimed for a thickness of 20 micrometers using the PI 2611. The first process, called silanization, was performed on the wafer using manual coating. VM652 was the adhesion promoter used for this silanization step.
To have a 20 μm thick polyimide layer, we did 2 successive depositions, each with a thickness of 1 μm. The machine used for the PI coating was the Sawatec LSM200. After each coating, two soft bakes were performed, one at 65 Celsius degrees and one at 105, each for a period of 3 minutes. The last step was the oven curing, where we kept the wafer inside the Heraeus T6060 (a multipurpose oven) during approximately 4 hours.



(a) Microscope image after 20 μm thick polyimide deposition

(b) Microscope image after 20 μm thick polyimide deposition showing the 4 quadrants

Figure 7: Optical microscope images after polyimide deposition revealing the Aluminium covered pillars

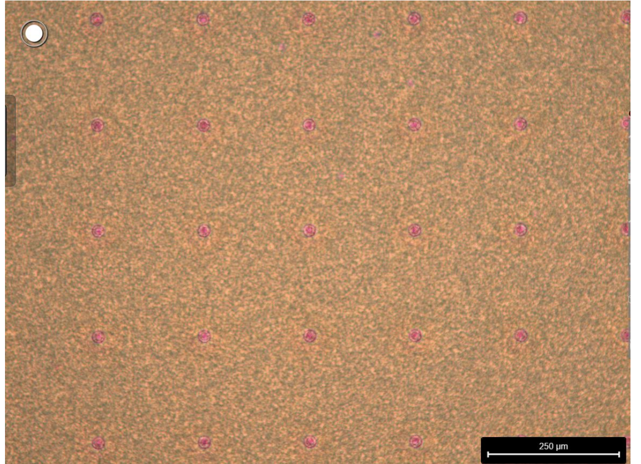
4.11 Step 13 - 2nd Aluminium and titanium deposition

The second metal deposition was closely similar from the first. However, a 3rd photolithography step was necessary after the sputtering, so the alignment markers still needed to be visible after sputtering. This is why before doing the sputtering kapton tape was placed on top of the polyimide layer where the alignment markers were located (both left and right of the wafer).
After the kapton tape placement, a 20 nm titanium adhesion layer was sputtered on top of the polyimide layer. Then an Aluminium layer of an average thickness of 1.1 μm was sputtered on top of the titanium. Once the sputtering process was done, the kapton tapes were removed and the alignement markers were still visible under the polyimide layer.

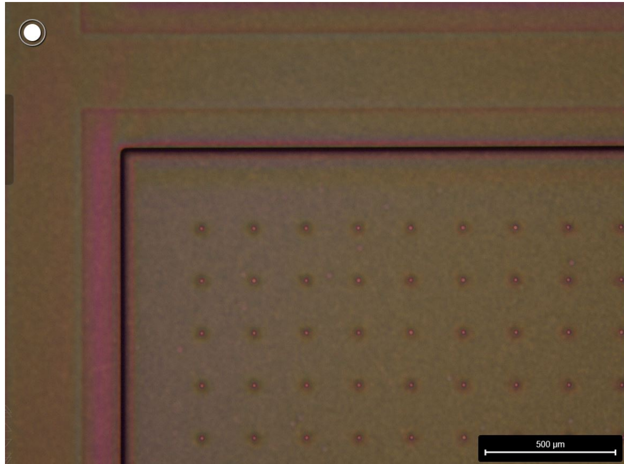
4.12 Step 14 to 16 - 3rd coating, exposure and development

A 3rd lithography step was introduced in order to get rid of both the aluminium and the polyimide layers around the silicon pillars. The goal was to etch everything around the aluminium covered

pillars in order to let them exposed to the outside air. A 20 μm diameter surface were exposed on top of all the silicon structures.
The photoresist used was the same as the first one, which was the AZ ECI 3007, and the same thickness was applied (1 micrometer). The machine used for coating, exposing and developing were the same used in steps 1,2 and 3.



(a) Exposed aluminium (in pink) around the silicon pillars



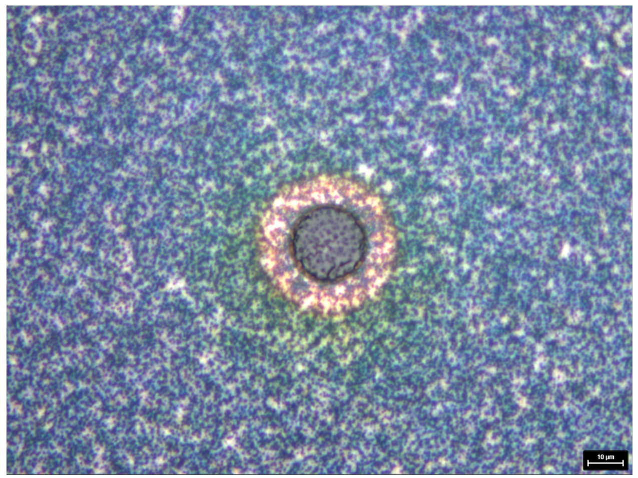
(b) Wafer covered in photoresist exposing the aluminium layer next to the silicon pillars

Figure 8: Optical microscope images after resist development revealing the aluminium layer as well as the exposed resist

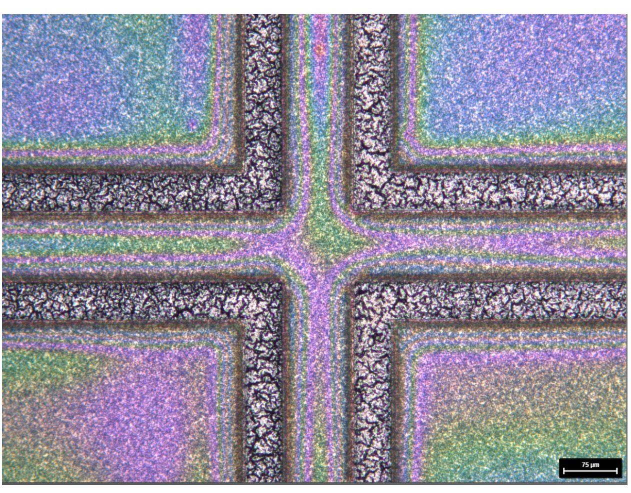
4.13 Step 17 - Aluminium and Titanium wet etching

Once again, wet etching was performed to remove the unwanted aluminium and titanium on the polyimide layer. During the 3rd development, most of the aluminium seemed to have stayed on the wafer, unlike the 2nd development. This might be explained because this development was rather quick in contrary to the 2nd one which took at least 6 minutes, meaning that less etching occured. Indeed, only 1 μm of resist needed to be developed for the former, unlike 20 μm for the latter.
With an aliminium thickness of around 1.1 μm, Aluminium wet etching was performed during 4 minutes inside the ANP bath. With an average rate of 300nm/minute, we thought that 4 minutes was enough to etch all the undesired aluminium.

However, optical microscope images were taken after this first bath and it seemed that some Al residues were still on surfaces that were supposed to be fully cleaned (figure 9). This is why the wafers were placed another 2 minutes inside the ANP bath in order to make sure all unwanted Al residues would be removed. Then the titanium etching was also performed using the HF bath to remove the adhesion layer. Optical images were also taken after the second bath and the Aluminium seemed to be fully etched (figure 10) exposing a clearly visible polyimide layer.

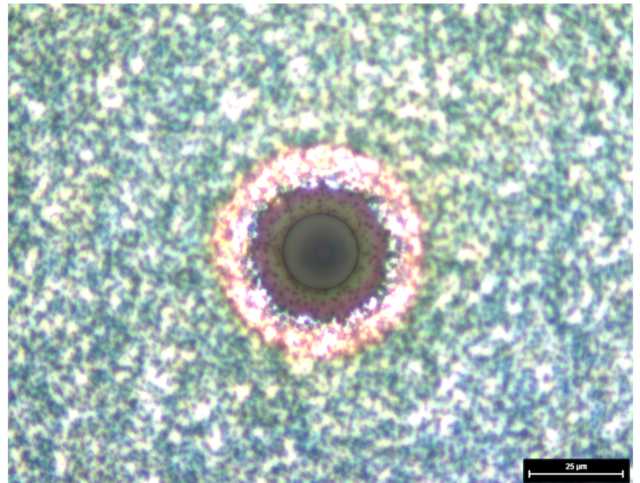


(a) Thin layer of aluminium (in grey) in the 20 μm diameter exposed area

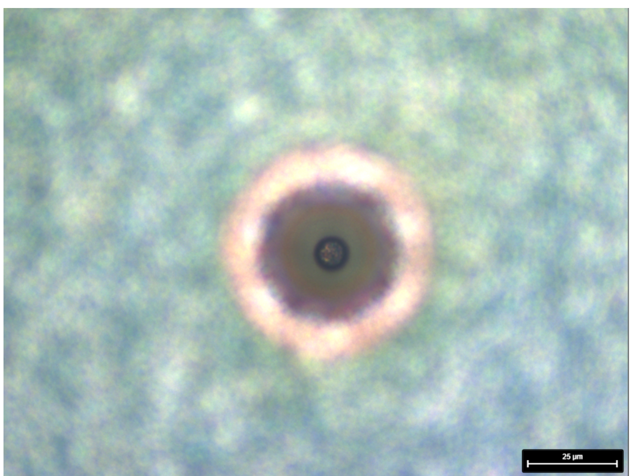


(b) Aluminium residues (in grey) on the dicing marks

Figure 9: Optical microscope images after 1st wet Aluminium etching revealing Al in unwanted areas



(a) Exposed polyimide (in brown) on top of the silicon pillar



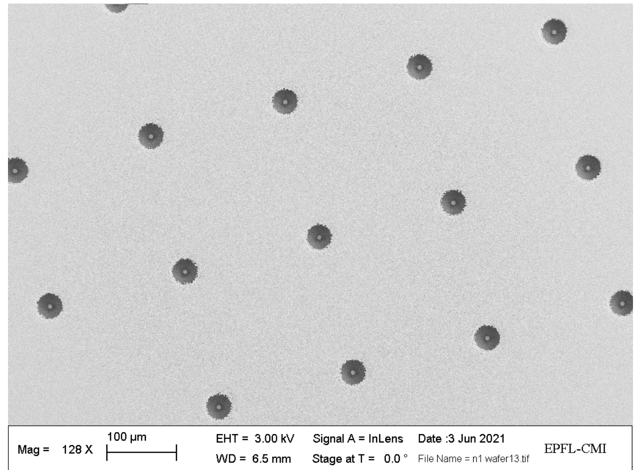
(b) Aluminium covered pillar visible underneath the polyimide layer

Figure 10: Optical microscope images after 2nd wet Aluminium etching revealing the polyimide and the pillar underneath

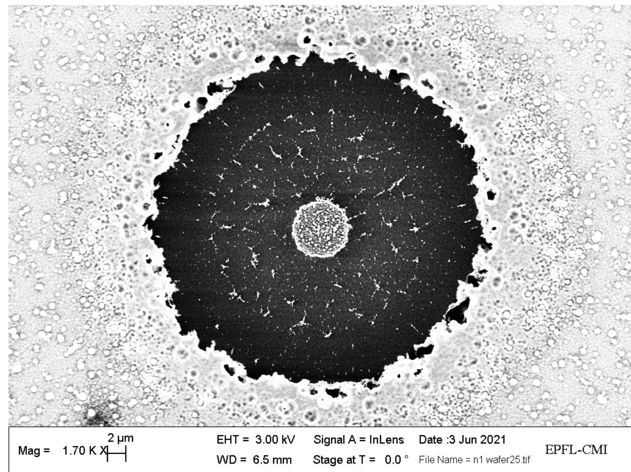
4.14 Step 18 - Polyimide etching

The final step inside the process flow was the polyimide etching. We used the STS Multiplex ICP machine to etch the 20 μm thick polyimide layer around the silicon pillars. The recipe was called parylin and the aluminium layer served as a mask. Indeed, the 1 μm resist layer was quickly etched, revealing the aluminium layer which resists very well against 02 plasma etching. The process was almost 30 minutes long and both SEM (figure 11) and optical images were taken to see the end

results. The final product was really close to the desired structure, which is highly encouraging for a first process.



(a) Rows and columns of Aluminium covered pillars



(b) Close up of an Aluminium covered pillar (in the center) and the silicon (in black) at the base

Figure 11: SEM images of the finalized microsystem revealing the Al covered pillars and the Al coating on top of the polyimide layer

5 Further improvements

This semester project showed that it is possible to create a first version of the miniaturized geiger counter. The silicon pillars, ranging from a diameter of 3 μm to 6 μm, were all nicely structured and all covered with Aluminium. Potential next steps could be to either reduce even more the diameter size as well as creating taller pillar structures (more than 10 μm), and see if the coverage can still be close to 100%.

Moreover, no testing of this microsystem was done as time was limited. Further testing should be done to see if any promising results can be found. As of today, the process flow seemed to be rather time efficient and no new ideas can be proposed.

6 Conclusion

This project showed a straightforward microfabrication process to create a novel particle detector. A step by step fabrication method was proposed. All the potential issues that happened during the fabrication inside the cleanroom were explained and ways to resolve them were given. Further testing should now be performed in order to see if this miniaturized system shows promising results.

References

[1] "Introduction to geiger counters," *https://www.cpp.edu/ pbsiegel/bio431/texnotes/chapter4.pdf*, 2011.

[2] www.microchemicals.eu, "Aluminium etching mechanism," *https://www.microchemicals.com /technical$_i$nformation/aluminium$_e$tching.pdf*, 2013.

7 Annex

Fabrication of new generation particle detectors

Description

Fabrication of new generation of particles detectors

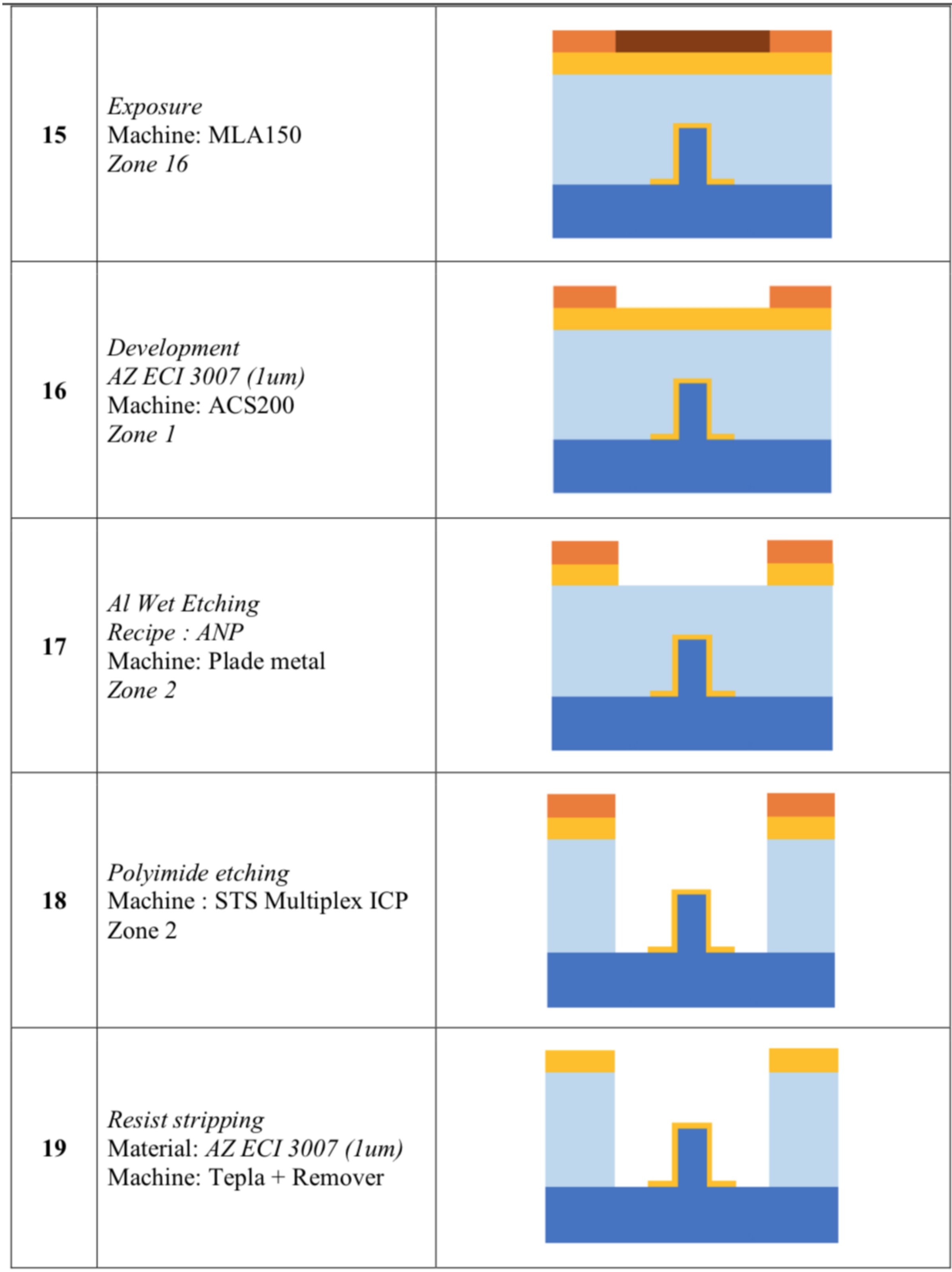
Technologies used			
Mask fabrication, sputtering, evaporation, positive resist , SU-8, Wet etching, SEM			
Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**3um**	First Mask	Silicon etching
2	**8um**	1 um	Al structuration
3	**30um**	5 um	Al structuration
Substrate Type			
HR silicon, Ø100mm, 525um thick			

Process outline

Step	Process description	Cross-section after process
01	*Photoresist coating* *AZ ECI 3007 (1um)* Machine: ACS200 *Zone 1*	Si
02	*Exposure* Machine: MLA150 *Zone 16*	Si
03	*Development* *AZ ECI 3007 (1um)* Machine: ACS200 *Zone 1*	Si

04	*Silicon etching* *Depth : 5-10 um* *Recipe :* SOI_accurate Machine: AMS200 *Zone 2*	Si
05	*Resist stripping* Material: *AZ ECI 3007 (1um)* Machine: Tepla + Remover	Si
06	*Sputtering of Ti/Al* *Thickness : 20nm for Ti (adhesion layer)* *0.5-1 um for Al* Machine: DP 650 *Zone 11*	
07	*Photoresist coating* *AZ 10XT-60 (20um)* Machine: EVG150 *Zone 6*	
08	*Exposure* Machine: Süss MA6 *Zone 16*	
09	*Development* *AZ 10XT-60 (20um)* Machine: EVG150 *Zone 6*	

10	*Al Wet Etching* *Recipe : ANP* Machine: Plade metal *Zone 2*	
11	*Resist stripping* Material: *AZ 10XT-60 (20um)* Machine: Tepla + Remover	
12	*Polyimide deposition* *Thickness : 20-25 um* Machine: Sawatec LSM200	
13	*Al deposition* *Thickness : 1-2 um* Machine: EVA 760 *Zone 11*	
14	*Photoresist coating* *AZ ECI 3007 (1um)* Machine: ACS200 *Zone 1*	



15	*Exposure* Machine: MLA150 *Zone 16*	
16	*Development* *AZ ECI 3007 (1um)* Machine: ACS200 *Zone 1*	
17	*Al Wet Etching* *Recipe : ANP* Machine: Plade metal *Zone 2*	
18	*Polyimide etching* Machine : STS Multiplex ICP Zone 2	
19	*Resist stripping* Material: *AZ ECI 3007 (1um)* Machine: Tepla + Remover	

Figure 12: Process flow of the particle detector

Figure 13: Design of the whole wafer with the 3 different masks used during the process flow

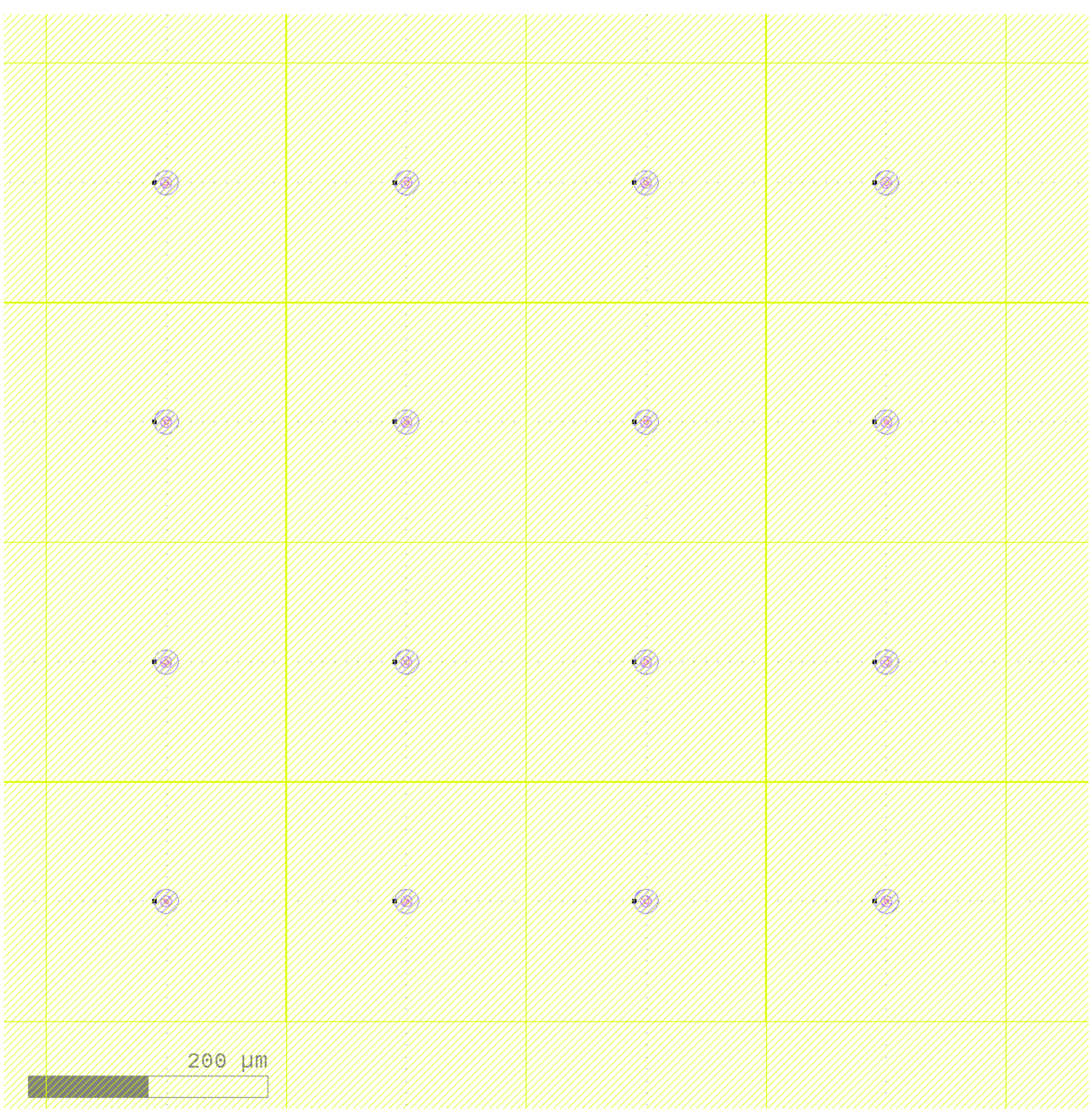


Figure 14: Close up of one of the arrays of the masks