Master Semester Project at Advanced NEMS lab

Optimization of the fabrication of buried electrodes for NEMS resonators

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Contents

1 Introduction **1**

2 Background **2**
2.1 AZ 1512 resist on LOR . . . 2
2.2 AZ ECI 3007 resist . . . 2

3 Methods **3**
3.1 Photolithography . . . 4
3.1.1 Coating . . . 4
3.2 Exposure . . . 4
3.3 Development . . . 4
3.4 Etching . . . 4
3.5 Metal deposition and lift-off . . . 4
3.6 Scanning Electron Microscope (SEM) . . . 4

4 Results **5**
4.1 Fabrication with recommended parameters . . . 5
4.2 Fabrication with different etch angles . . . 6
4.3 Fabrication to verify the hypothesis of reflow . . . 7

5 Discussion **10**
5.1 Fabrication with recommended parameters . . . 10
5.1.1 AZ 1512 on LOR . . . 10
5.1.2 AZ ECI 3007 . . . 11
5.2 Fabrication with different etch angles . . . 11
5.3 Fabrication to verify the hypothesis of reflow . . . 12

6 Conclusion **13**

A Appendix **14**
A.1 Original process flow . . . 14
A.2 Mask layout . . . 15

List of Figures

1 Process steps using LOR and a positive photoresist such as AZ 1512 [9] . . . 2
2 Process flow to assess the feasibility of fabricating buried lateral electrodes for NEMS resonators. . . . 3
3 SEM images of the cross section of three steps done on a AZ1512 resist wafer: after IBE a) and b), after LAB600 c) and d), and after lift-off e) and f). . . . 5
4 SEM images of the cross section of an AZ ECI 3007 wafer, after IBE. . . . 6
5 SEM image of cross section of AZ ECI chips after lift off step, with different etch angles. Metal deposition was done with EVA760. . . . 7
6 SEM image of cross section of AZ1512 chips after lift off step, with different etch angles. Metal deposition was done with EVA760. . . . 8
7 SEM image of cross section of chips after etching of SiO2 on IBE: $-30°$ for AZ1512 resist chips and $-10°$ for AZ ECI chips. . . . 8
8 1. Schematic of the two redeposition mechanisms: (i) direct or line-of-sight redeposition and (ii) indirect redeposition after interaction with the gas phase. [7] . . . 10
9 Single layer lift-off process (left) and bilayer lift-off process (right) [5] . . . 11
10 Cross-section of resist structures at increasing bake temperatures (AZ ECI 3000) [6] . . . 11

1 Introduction

The aim of this project is to optimize the fabrication of buried lateral electrodes, with a piezolectric material sandwiched between two metal electrodes. Lateral electrodes have the advantage of allowing the applied electric field to be and to remain completely horizontal. The fabrication is difficult to achieve since fencing and redeposition must be avoided, whilst total lateral coverage must be accomplished. In fact, fencing and redeposition between the metal and the piezoelectric material would lead to nonfunctional electrodes. Moreover, partial lateral coverage would not allow to have an ohmic contact between the metal and the piezoelectric material, therefore would not allow the application of an electric field.

We will tackle these challenges by optimizing each step of the process flow to fabricate lateral electrodes with maximum electrode coverage to the sidewall, and by minimizing redeposition and fencing. To minimize fencing and redeposition, and optimal etch angle is to be found. To maximize sidewall coverage, an optimal metal deposition method is to be found. Finally, two resists will be compared in order to select the one yielding the best results.

A possible application of these lateral electrodes is to make thickness mode resonators that are small enough to be inserted inside of cells. This allows the resonators to be used as RFID tags to identify and track the movement of individual cells. Lithium niobate has been proven to be biocompatible and cytocompatible with certain cells, which allows lithium niobate to be used in biological applications [3], such as using lithium niobate to make biocompatible RFID tags. In fact, lithium niobate is a piezoelectric material, which allows it to be used as a material for RFID tags. The piezoelectric material is driven into vibration modes when an RF signal is applied to the electrodes surrounding the lithium niobate. Different resonance frequencies can be obtained by varying the width of the lithium niobate component. Therefore, RFID tags at different resonance frequencies can be obtained, which will then be used for identifying cells, as unique ID.

The challenge of this project is to optimize the process flow in order to obtain an improved and feasible microstructure. This means having a reproducible result, avoiding classical problems of microfabrication such as fencing and redeposition after etching. Finally, optimal sidewall coverage has to be achieved.

2 Background

2.1 AZ 1512 resist on LOR

LOR is a resist that is often used as a sacrificial layer. It is very well suited for lift-off processes and is used in combination with positive photoresists. LOR resist is designed for high resolution, easy process tuning and line width control. This is a huge help for projects such as this one, where lines with variable and precise widths are to be made. An advantage of LOR 5A is its stability: wafers can be prepared in advance. LOR 5A was used in this project, corresponding to the LOR A series, having relatively low dissolution rates. The adhesion of LOR resist does not require the presence of an HMDS primer. However, for adhesion on SiO2, thermal dehydration is strongly recommended. This is done by the EVG 150 before spincoating of the resists. Figure 1 shows the profile obtained when using LOR with a positive photoresist, such as AZ 1512 [8],[9].

AZ 1512 is a positive photoresist: the part of the resist exposed to the light will be dissolved. The AZ 1500 series of resists has many recommended applications, and in particular for this project: resist thickness ranging from 1.0-2.0 µm. In fact, we use a thickness of AZ 1512 of 1.5 µm. Wall angles of up to 20 ° are achievable for small exposure energies. [1]

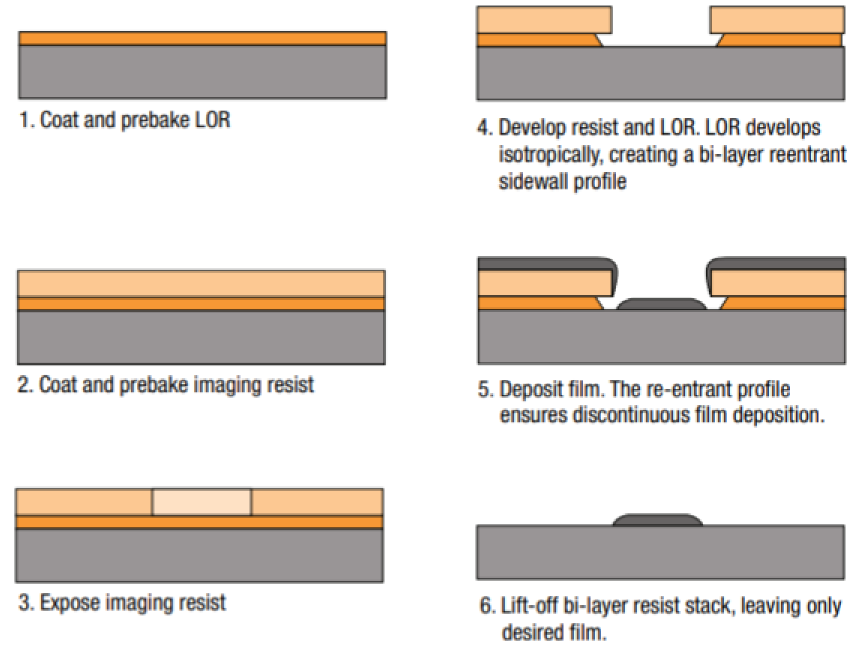


Figure 1: Process steps using LOR and a positive photoresist such as AZ 1512 [9]

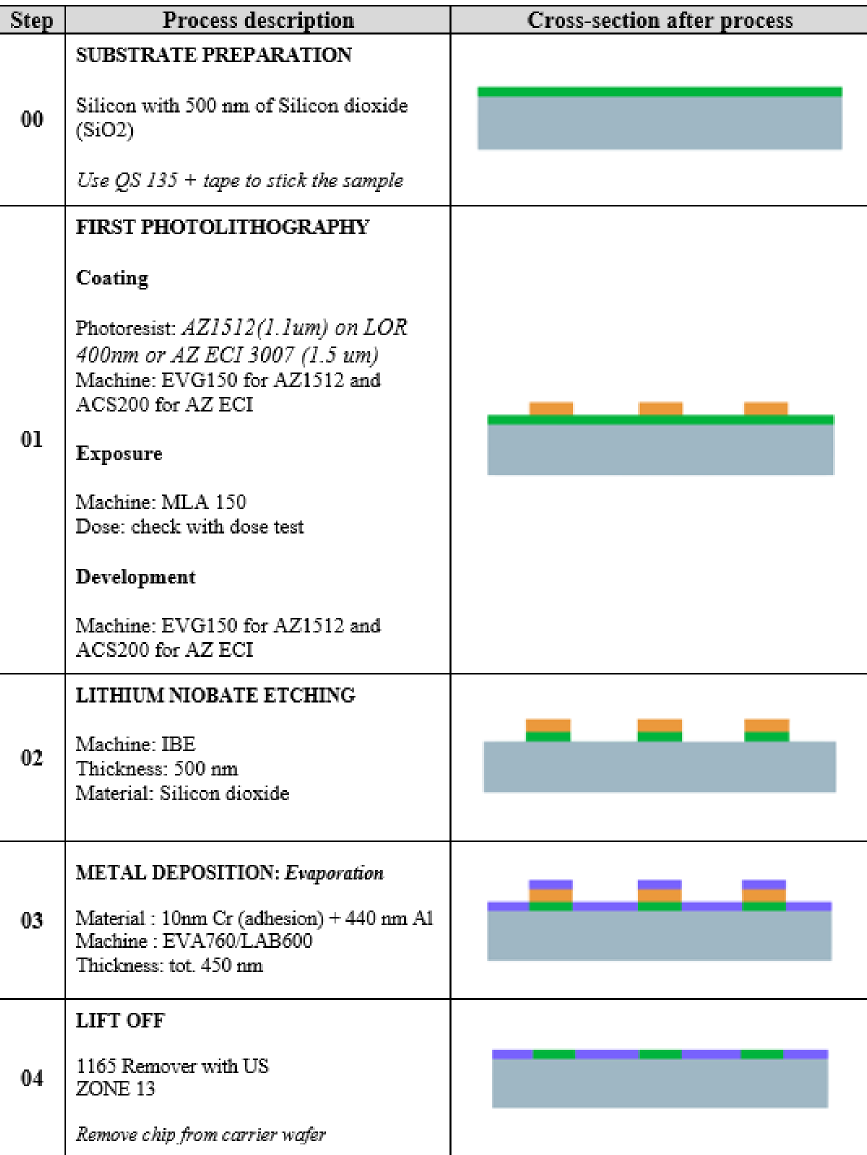
2.2 AZ ECI 3007 resist

AZ ECI 3007 is also a positive photoresist. However, it is not used with LOR. It is thermally stable, therefore is suitable for processes carried out at high temperatures. Moreover, the AZ ECI family of resists is suitable for fabrication of steep resist sidewalls, high resolution, as well as dry etching. The high resolution allows to achieve lines down to 1 µm [2].

3 Methods

In order to optimize and asses the feasibility of the process flow, another material than lithium niobate was used. This is due to the fact that lithium niobate is a very expensive material, therefore optimizing the process flow with this material would be very onerous. Hence, silicon wafers with 500 nm of silicon dioxide were used. The 500 nm of silicon dioxide replace the 300 nm of lithium niobate.

Two photoresists are of interest, and are to be optimized. This leads to two sets of parameters to be optimized. The project is to complete and optimize the five steps of the process flow shown in figure 2. As it can be seen, the steps 01, 02 and 03 are the ones subject to optimization. The original process flow, using lithium niobate, can be seen in appendix A.1.



Step	Process description	Cross-section after process
00	**SUBSTRATE PREPARATION** Silicon with 500 nm of Silicon dioxide (SiO2) *Use QS 135 + tape to stick the sample*	
01	**FIRST PHOTOLITHOGRAPHY** **Coating** Photoresist: *AZ1512(1.1um) on LOR 400nm or AZ ECI 3007 (1.5 um)* Machine: EVG150 for AZ1512 and ACS200 for AZ ECI **Exposure** Machine: MLA 150 Dose: check with dose test **Development** Machine: EVG150 for AZ1512 and ACS200 for AZ ECI	
02	**LITHIUM NIOBATE ETCHING** Machine: IBE Thickness: 500 nm Material: Silicon dioxide	
03	**METAL DEPOSITION:** ***Evaporation*** Material : 10nm Cr (adhesion) + 440 nm Al Machine : EVA760/LAB600 Thickness: tot. 450 nm	
04	**LIFT OFF** 1165 Remover with US ZONE 13 *Remove chip from carrier wafer*	

Figure 2: Process flow to assess the feasibility of fabricating buried lateral electrodes for NEMS resonators.

3.1 Photolithography

3.1.1 Coating

Since two photoresists had to be studied, two batches of wafers were done: one with each photoresist. The first batch was spin-coated with a 1.5 μm layer of AZ ECI 3007 using the Süss Microtec ACS200 Gen3. The second batch was spin-coated with a 1.1 μm layer of AZ1512 on 400 nm of LOR 5A, using the EVG 150.

3.2 Exposure

The wafers were exposed with the Heidelberg MLA150 Maskless Aligner. The mask layout can be found in appendix A.2. The initial parameters that were used, the ones suggested, were a dose of 65 mJ/cm^2 with defocus -2 for AZ 1512 resist and a dose of 185 mJ/cm^2 with defocus -1 for AZ ECI 3007 resist. However, the results obtained with these parameters were not optimal. Therefore, a dose test was performed and it was determined that a dose of 40 mJ/cm^2 with defocus -2 yields the best results for AZ1512 resist, and that a dose of 200 mJ/cm^2 with defocus -1 yields the best results for AZ ECI 3007 resist. Therefore, these parameters were used for the exposures of the wafers throughout the rest of the project.

3.3 Development

The development was done with the Süss Microtec ACS200 Gen3 for AZ ECI 3007 resist and with EVG 150 for AZ 1512 resist.

3.4 Etching

Silicon dioxide etching was done using Veeco Nexus IBE350. The etching rate for Si02 is of 37 nm/min. Therefore, in order to etch 500 nm, the process time was set to 14 min. However, the etch angle had to be optimized in order to obtain the best result. The angles $\vartheta = 0°, -10°, -20°, -30°$ were tested. The process was done four times, each time with two chips: one per resist. Therefore, eight chips were obtained and to be analysed. When processing chips, they were glued onto a carrier wafer with Quickstick for the etching step. In order to do so, the chips had to be heated to a temperature of 135 °C, the melting point of Quickstick wax.

3.5 Metal deposition and lift-off

Metal deposition was done using LAB600 or EVA760. An adhesion layer of 10 nm of Cr was used, for the 440 nm of Al to adhere better to the surface and for the lift-off to be facilitated. Lift-off was performed in photosensitive resist stripping remover 1165.

3.6 Scanning Electron Microscope (SEM)

Imaging of the chips to be analysed was done with the Zeiss LEO 1550 and Zeiss MERLIN scanning electron microscopes (SEM). The chips were diced into smaller chips by cleaving. The cross section of the chips was then analysed with the SEM. SEM imaging provides information on the microstructure and quality of the structures. Moreover, the SEM images were used to measure the thickness of the layers.

4 Results

4.1 Fabrication with recommended parameters

(a) after IBE ($-10°$)

(b) after IBE ($-10°$)

(c) after LAB600

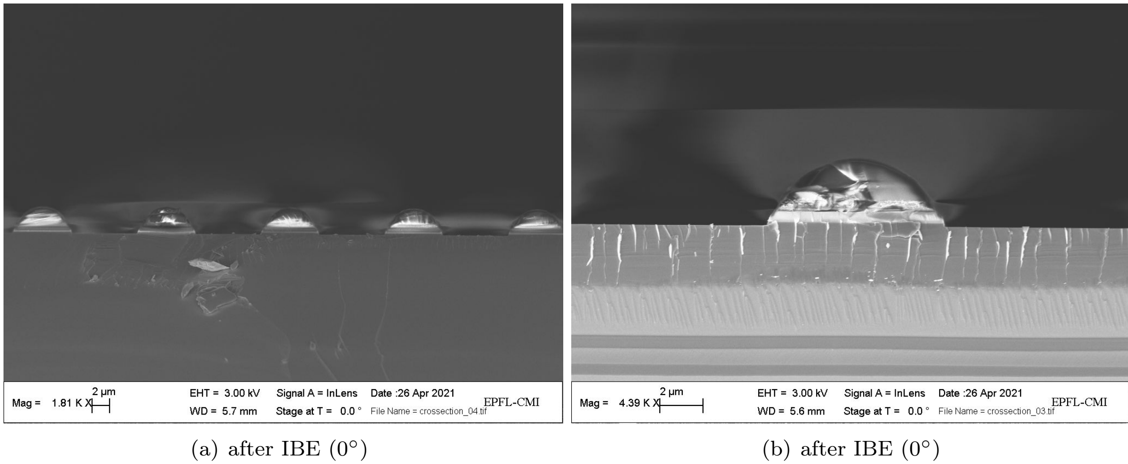
(d) after LAB600

(e) after lift-off

(f) after lift-off

Figure 3: SEM images of the cross section of three steps done on a AZ1512 resist wafer: after IBE a) and b), after LAB600 c) and d), and after lift-off e) and f).

The process flow was done once to completion with AZ 1512 resist and the recommended MLA dose and defocus, as well as the recommended etch angle for IBE. The different steps can be seen on figure 3. The process up to LAB600 was done on a wafer, therefore no QuickStick was used for placement of the chips on dummy wafers for IBE. Moreover, it can be seen that the lift-off has functioned. However, fencing can be observed due to the re-deposition of SiO2 after etching. The fencing can be seen between the LOR and the AZ 1512 on figure 3(a) and on the SiO2 sidewall on figure 3(f). Finally, it can be seen on figure 3(f) that there is no sidewall coverage. In fact, there is a gap between the metal and the SiO2. This would not allow to apply the electric field to the resonator.



(a) after IBE (0°) (b) after IBE (0°)

Figure 4: SEM images of the cross section of an AZ ECI 3007 wafer, after IBE.

The SEM imaging in figure 4 was performed after IBE, step 02 of the process flow shown in figure 2 with AZ ECI 3007 resist. The fabrication was performed with the recommended MLA dose and defocus, as well as the recommended etch angle for IBE. It can be seen on figure 4 that the profile obtained is less vertical than the one obtained with AZ 1512. However, no re-deposition or fencing can be observed.

4.2 Fabrication with different etch angles

A selection of SEM images of the cross sections of chips with AZ ECI 3007 with the different IBE etch angles can be seen in figure 5. These images were taken after the lift-off step, step 4 of the process flow shown in figure 2. Sidewall non uniformity can be seen on figures 5(a), 5(e) and 5(f). Moreover, in images 5(b), 5(d) and 5(f) can been seen dome like structures, with a failed lift-off. The shape of the structures is most likely due to resist reflow due to the 135 °C heat that was applied on the chip for the QuickStick glue.

A selection of SEM images of the cross sections of chips with AZ 1512 with the different IBE etch angles can be seen in figure 6. These images were taken after the lift-off step, step 4 of the process flow shown in figure 2. Similarly to the images of the AZ ECI 3007 chips, we can see dome like structures 6(d). This is also most likely due to resist reflow. Sidewall non uniformity can be observed on the silicon dioxide on figure 6(c), which might be due to the etch angle used.

Finally, it can be seen that sidewall coverage was achieved for both resists. This varies from the results obtained when using LAB600 for metal deposition, where sidewall coverage was not accomplished. Therefore, EVA760 yields better sidewall coverage than LAB600.

(a) AZECI resist at $-10°$, no defect

(b) AZECI resist at $-10°$, with defect

(c) AZECI resist at $-20°$, no defect

(d) AZECI resist at $-20°$, with defect

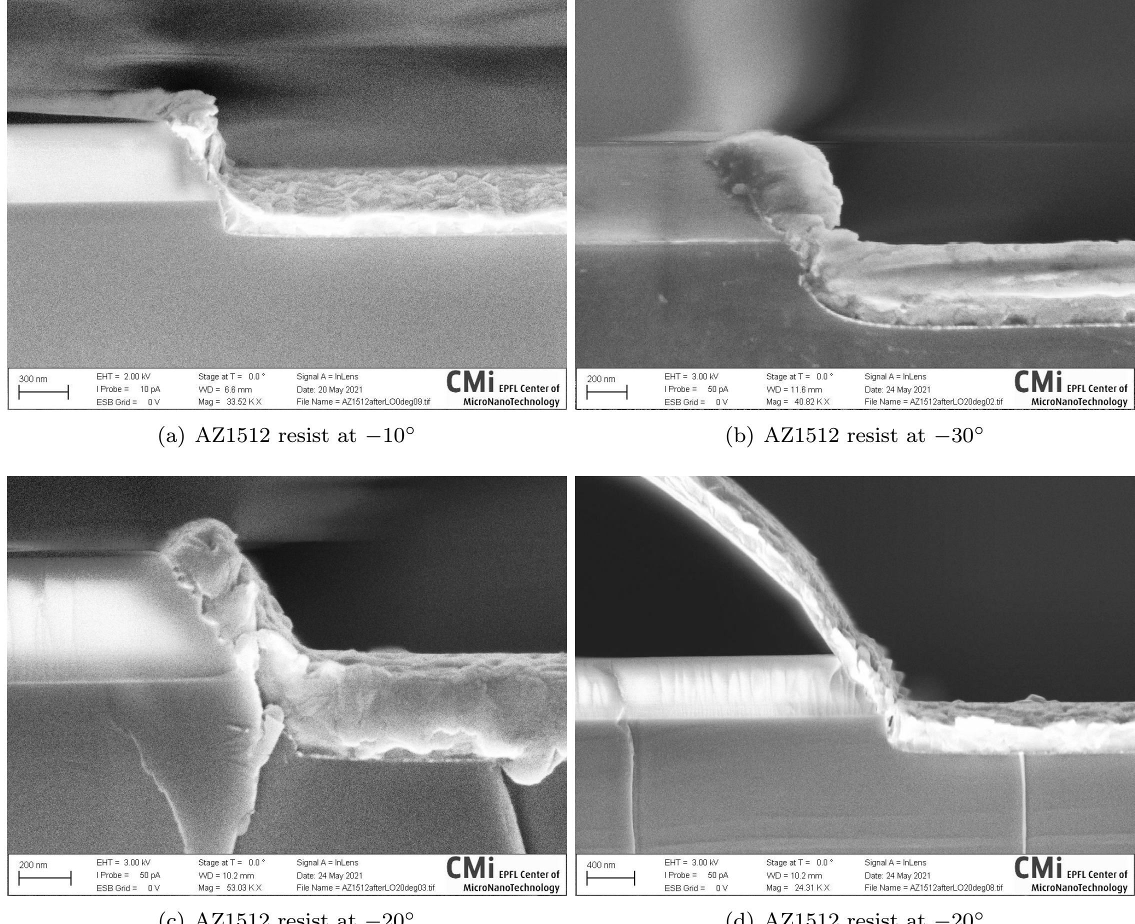
(e) AZECI resist at $-30°$, no defect

(f) AZECI resist at $-30°$, with defect

Figure 5: SEM image of cross section of AZ ECI chips after lift off step, with different etch angles. Metal deposition was done with EVA760.

4.3 Fabrication to verify the hypothesis of reflow

In order to verify the hypothesis of the heat used during QuickStick causing the problem of the dome like structures, the process was done a final time, up to step 2 of the process flow shown in figure 2.



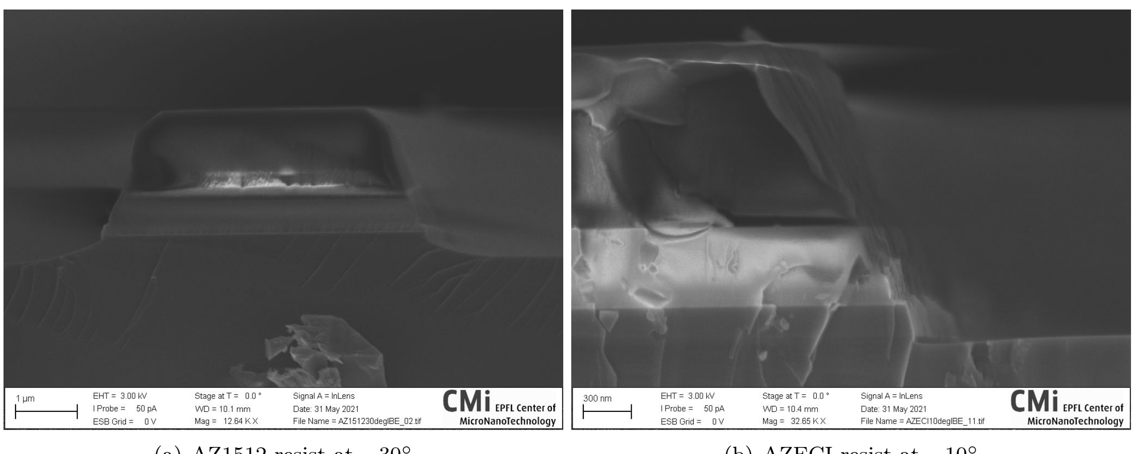
(a) AZ1512 resist at −10°

(b) AZ1512 resist at −30°

(c) AZ1512 resist at −20°

(d) AZ1512 resist at −20°

Figure 6: SEM image of cross section of AZ1512 chips after lift off step, with different etch angles. Metal deposition was done with EVA760.



(a) AZ1512 resist at −30°

(b) AZECI resist at −10°

Figure 7: SEM image of cross section of chips after etching of SiO2 on IBE: −30° for AZ1512 resist chips and −10° for AZ ECI chips.

The process was done with a full wafer, meaning that no chips had to be stuck on carrier wafers with QuickStick. Two different angles were used: $-30°$ for AZ 1512 as the angle $-10°$ was already used for the first fabrication, shown in figure 3(b). The angle $-10°$ was used for the AZ ECI 3007 resist, as this angle was never used on a full wafer. As it can be seen in figure 7, no reflow was observed. However, there is sidewall non uniformity with both resists.

5 Discussion

5.1 Fabrication with recommended parameters

5.1.1 AZ 1512 on LOR

The expected resist profile is obtained, the metal deposition is uniform and the lift off was accomplished. However, certain abnormalities can be seen.

Figures 5(a) and 5(b) reveal overetching of SiO2: the silicon of the wafer has also been slightly etched away. The etch time was time was set to 15 min and should therefore be slightly reduced. Moreover, it appears that additional material has accumulated on the LOR layer. This is due to re-deposition of some etched SiO2. This can also be seen, in a less flagrant way, on the silicon oxide layers. This also seems to be re-deposition of SiO2. Re-deposition is known to happen in substrate regions that are not directly exposed to the ions: the removed material fails to be completely ejected into the gas phase, and redeposits on the substrate being etched. The sputtered material either immediately redeposits on the sidewalls, or can be ejected and then redeposit. The two possibilities are shown in figure 8. Sidewalls of photoresist can be affected by this re-deposition, and this is what happens here, with SiO2 being redeposited on the sidewalls of the LOR. To reduce this effect, tilting the sidewalls of the photoresist is advised, exposing them to ions, therefore minimizing the re-deposition of material. Another possibility to reduce this effect is to change the etch angle.

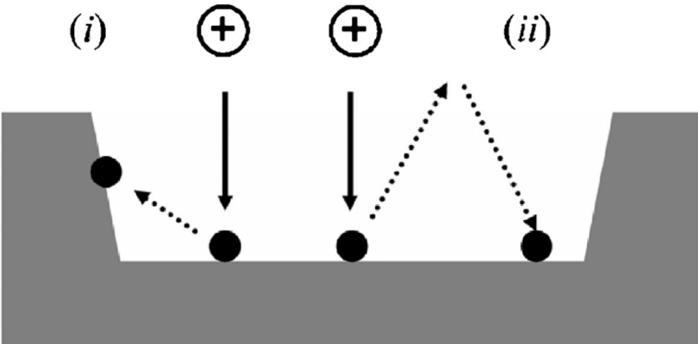


Figure 8: 1. Schematic of the two redeposition mechanisms: (i) direct or line-of-sight redeposition and (ii) indirect redeposition after interaction with the gas phase. [7]

Re-deposition can lead to a phenomenon called fencing, where fence-like structure remain on the edge of a structure after photoresist stripping. This will be observable after the lift-off step.

Figures 5(c) and 5(d) show a uniform deposition of metal.

As it can be seen on figures 5(e) and 5(f), the lift-off was achieved. The photoresist was entirely removed, as well as the SiO2 that had redeposited on the LOR. Therefore, fencing was avoided. This is most likely due to the fact that a bilayer process was used, with LOR and AZ 1512. The process of using a bilayer is shown in figure 9. However, the SiO2 that has re-deposited on the SiO2 layer is still present, and has not been removed.

The obtained result is close to the expectation, as seen on figure 2. However, there is an unwanted gap between the metal and the SiO2 lines. It results in a lack of sidewall coverage. This gap will prevent an ohmic contact with the piezoresistive material and will not allow to apply an electric field. The gap could be due to a non optimal etching angle, and the etching angle will therefore be optimized. The exposure dose might also have a role in this, and will also be optimized.

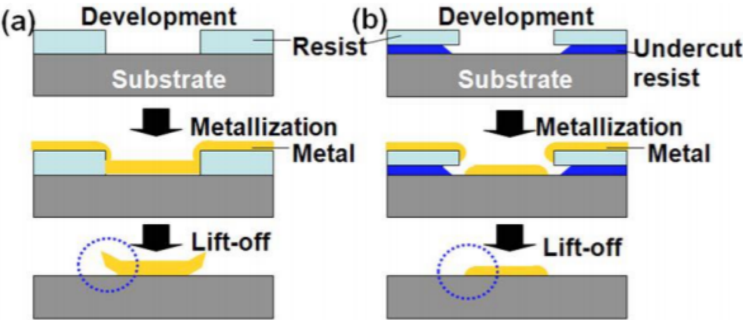


Figure 9: Single layer lift-off process (left) and bilayer lift-off process (right) [5]

5.1.2 AZ ECI 3007

The results shown in figure 4 reveal a very different shape of resist than with AZ 1512. In fact, the profile of AZ ECI 3007 has a dome like shape and a less vertical sidewall. The slopes of the AZ ECI 3007 profile might have an advantage to minimize the re-deposition of SiO2 from etching. However, the process was not done to completion since it had already been deduced that optimization had to be performed.

5.2 Fabrication with different etch angles

After having optimized MLA dose and defocus parameters with a dose test per resist, the etch angle was to optimize. Figures 5 and 6 show the results, and have a common defect of fabrication. In fact, the resist has taken a dome shape in most of the cases, for each angle, and clean lift-off was not achieved. This is most likely due to a phenomenon called reflow of photoresist. Reflow is a phenomenon in which, in most cases, the resist structure aims to minimise its contact with the air by maximising its contact with the substrate [6]. Another explanation for this phenomenon is the surface tension of the liquid resist that pulls the resist up in a convex shape, on top of the substrate [4]. Furthermore, reflow can only take place on resists that do not crosslink, therefore can happen on positive photoresists, which is the case for AZ ECI 3007 and AZ 1512.

The reflow temperature varies from substrate to substrate. In this experiment, the chips were placed on a hotplate at a temperature of 135 °C for the QuickStick glue to melt. The minimal temperature for reflow of AZ 1512 is approximately 100 °C, and the minimal temperature for AZ ECI 3007 is 100 °C [6]. Therefore, these temperatures were reached and even exceeded while processing the chips. The hypothesis of reflow having lead to the shape of the obtained lines is therefore plausible.

Figure 10 shows the evolution of the cross-sections of AZ ECI 3000 resist with increasing temperatures. AZ ECI 3000 is in the same series of resists as AZ ECI 3007, and have similar properties. Having heated the AZ ECI 3007 resist at 135 °C lead to a similar profile as seen in figure 10, at 125 °C.

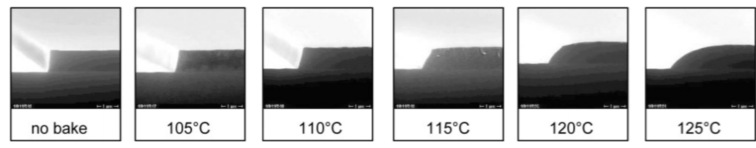


Figure 10: Cross-section of resist structures at increasing bake temperatures (AZ ECI 3000) [6]

Another pointer to the hypothesis of reflow being the cause of these dome shaped resists is the fact that when processing an entire wafer, and never bringing it to a heat of 135 °C, these dome shapes

never appeared. These results can be seen on figure 3.

Finally, EVA760 yields a conformal deposition on the sidewall whereas LAB600 does not. This is due to the fact that the working distance in the LAB600 is 1010 mm and that the working distance in the EVA760 is 450 mm. The larger distance in LAB600 allows a better directionality for the deposition. However, this better directionality leads to less deposition under the AZ 1512, therefore less deposition on the SiO2 and on the LOR. This can be seen on figures 1 and 3(d). The lack of metal on the SiO2 leads to less sidewall coverage. Since the working distance in EVA760 is smaller than the one in LAB600, the achieved directionality is lesser. This is an advantage for sidewall coverage, since more of the surface under the resist is reached. Hence, EVA760 gives uniform sidewall coverage whereas LAB600 does not.

5.3 Fabrication to verify the hypothesis of reflow

As it can be seen on figure 7, no reflow was observed, and the resists have the expected profiles. Since full wafers were processed here, no QuickStick was used for IBE and the structures were not brought to a temperature of 135 °C. This allows to confirm that reflow was at the origin of the dome shaped structures observed in figures 5 and 7. Therefore, when fabricating these devices, QuickStick glue should not be used and the substrates should not be brought to high temperatures. Fabricating the substrate on full wafers until the end of step 2 shown in the process flow on figure 2 allows the wafer to be cut into chips for deposition and lift-off, since QuickStick glue is not needed for these steps. However, chips should not be used for IBE.

We can observe that the AZ 1512 resist has a more vertical sidewall than the AZ ECI 3007 resist. This observation allows to give a preference to AZ 1512 resist, since even with a -30° etching angle, it has better verticality than AZ ECI 3007 with a -10 ° etching angle.

Sidewall non uniformity in the shape of steps can be observed on the SiO2 and on the Si. The origin of these steps is uncertain, but might be the etch angle. In fact, when etching, the substrate is rotated to promote homogeneity. However, homogeneity is not achieved here. It is possible that these steps are due to redeposition of SiO2. However, sidewall non uniformity is not seen on figure 3, using the same resist. Therefore, the steps might be due to the fact that an angle of 30° is not suitable for AZ 1512 resist.

6 Conclusion

After having tried different parameters and different techniques for the fabrication of the devices, we are able to conclude that:

- AZ 1512 on LOR yields better sidewall verticality than AZ ECI 3007 resist
- The substrates should not be brought to a temperature greater than 100 °C during processing, after development
- EVA760 yields a conformal deposition on the sidewall whereas LAB600 fails to do so
- AZ 1512 on LOR yields a cleaner lift-off than AZ ECI 3007

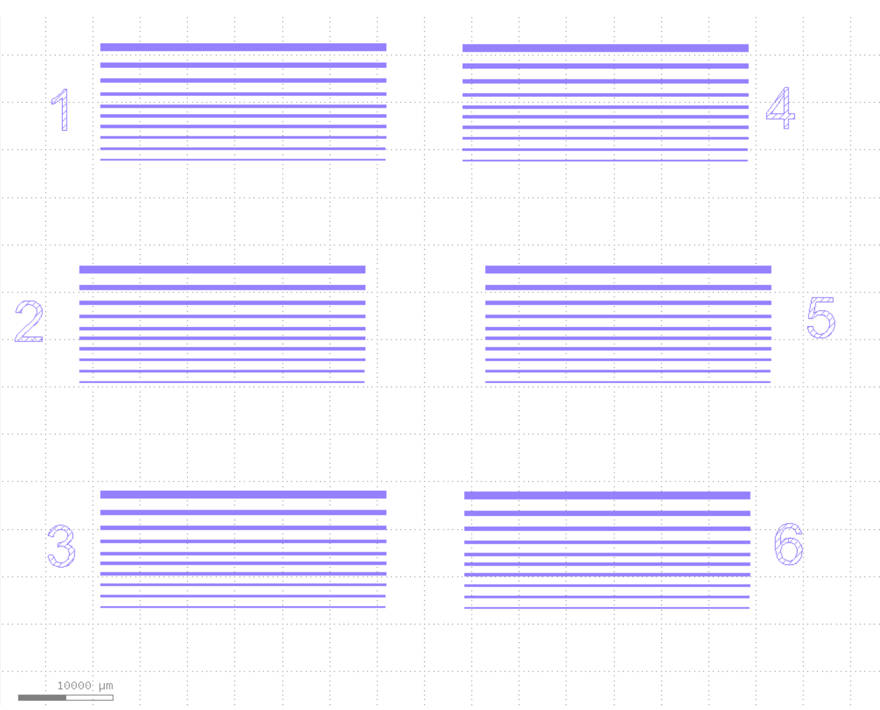
However, an optimal etch angle has not been found and could greatly improve the final result. Furthermore, the silicon oxide was slightly overetched, leading to etching of silicon. Therefore, the etch time should also be optimized.

A Appendix

A.1 Original process flow

Step	Process description	Cross-section after process
00	**SUBSTRATE PREPARATION** Silicon with 300 nm of Lithium Niobate (LN) *Use QS 135 + tape to stick the sample*	
01	**FIRST PHOTOLITHOGRAPHY** **Coating** Photoresist: *AZ1512(1.1um) on LOR 400nm* Machine: EVG150 **Exposure** Machine: MLA 150 Dose: check with dose test **Development** Machine: EVG150	
02	**LITHIUM NIOBATE ETCHING** Machine: IBE Thickness: 300 nm Material: Lithium Niobate	
03	**METAL DEPOSITION: *Evaporation*** Material : 5nm Cr (adhesion) + 295 nm Al Machine : EVA760/LAB600 Thickness: tot. 300 nm	
04	**LIFT OFF** 1165 Remover with US ZONE 13 *Remove chip from carrier wafer*	

A.2 Mask layout



References

[1] AZ 1500 SERIES POSITIVE PHOTORESISTS. Hoechst. URL: https://www.lsu.edu/camd/files/AZSeries.pdf.

[2] Basics of Microstructuring. MicroChemicals. URL: https://micro-chemicals.com/technical_information/lift_off_photoresist.pdf.

[3] N.C. Carville. Biocompatible Lithium Niobate for Sensing and Microfluidics Applications. URL: http://isaf-iwatmd-pfm2017.gatech.edu/abstracts/Session%20II/Devices/245%20-%20ORAL%20-%20Rodriguez,%20Brian.pdf.

[4] Encyclopedia of Microfluidics and Nanofluidics. Springer, Boston, MA. URL: https://link.springer.com/referenceworkentry/10.1007%5C%2F978-0-387-48998-8_1224 (visited on 2008).

[5] R. Gao and L. Zhang. Micromachined Microsensors for Manufacturing. IEEE Instrumentation and Measurement Magazin. 2004.

[6] HARDBAKE, REFLOW AND DUV HARDENING. Springer, Boston, MA. URL: https://www.microchemicals.com/technical_information/photoresist_hardbake_reflow_uv_hardening.pdf.

[7] Influence of redeposition on the plasma etching dynamics. American Institute of Physics. 2007. URL: https://aip.scitation.org/doi/full/10.1063/1.2719015?casa_token=ixeEqeajUv4AAAAA%5C%3AKEGSxGTbrQRYXRu_hRtMysj1J4pmxYl-8lDsx_K79vKN3BhaUGQn-1_HZg1yI0La0Ku12ITVFm1o.

[8] LOR and PMGI Resists. MicroCHEM. URL: http://apps.mnc.umn.edu/pub/photoresists/lor_pds.pdf.

[9] LOR Lift-off resists. MicroCHEM. URL: https://amolf.nl/wp-content/uploads/2016/09/datasheets_LOR_datasheet.pdf.