ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

MICROENGINEERING SEMESTER PROJECT I

Advanced NEMS group

Fabrication of piezoelectric electrodes

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1 Introduction

1.1 Objective

The objective of this semester project is to investigate different fabrication processes and materials used for the fabrication of piezoelectric electrodes. More in detail, to investigate if the use of test wafers and high resistivity wafers play a role on the quality of the contacts for the microelectrodes and the difference in quality of the deposition of the bottom electrode between two different sputtering equipments, namely SPIDER and the DP650.

1.2 The devices

The devices we aim at fabricating are piezoelectric resonators. Those devices have the following characteristics: They are a suspended beam (cantilever or clamped - clamped beam) made of a supporter material and several other layers on top that forms the piezoelectric device. The piezoelectric device is composed of a sandwiched piezoelectric material between two metallic layers. Those two metal conductive layers above and below the piezoelectric material are the electrodes. Applying a voltage between those two layers generates an electric field across the piezoelectric material. Tanks to the piezoelectric effect the piezoelectric material deforms when it is exposed to an electric field. This serves as a means to generate movement/vibration. In figure 1 a cross section of a model finished device is shown (dimension not in scale, only one explanatory model).

1.3 Materials

We work on two different starting substrates; on p doped wafers (test wafers) and on high resistivity wafers (HR wafers). Both with 700nm low-stress silicone nitride already present on the surface. The piezoelectric device layers (metals, piezoelectric material, metals) resides on top of it. The SiN (silicone nitride, light blue in figure 1) functions as a supportive structure and together with the piezoelectric device forms the beam resonator. The piezoelectric material chosen is AlN (aluminum nitride, 200nm, green in figure 1). The bottom contact is made of two materials, firstly an adhesion layer of Ti[1] (titanium, 15nm, yellow in figure 1) and Pt (platinum, 25nm, blue in figure 1). The Ti serves as an adhesion layer between the SiN and Pt. Pt is in contact with AlN. The top contact is made of Pt (25 nm).

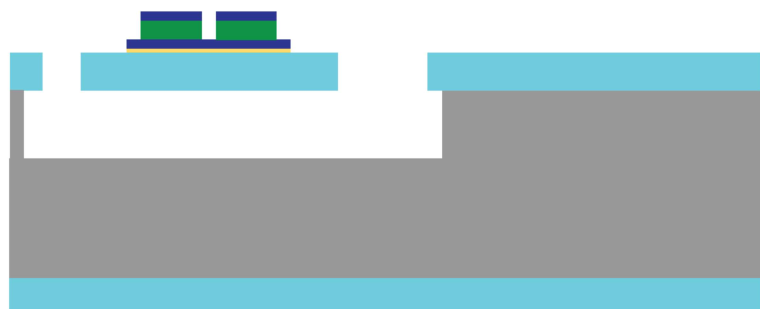

Figure 1: Cross section of one possible device. In blue the Pt, in yellow the Ti, in gray the Si, in light blue the SiN and in green the AlN. The dimension are not in scale and the image serves just to give an idea of the shape.

[1]Titanium is deposited using the sputtering machine DP650, however in the SPIDER instead of Ti AlN is used. As we will see further the best result is obtained with the sputtering machine DP650.

1.4 Fabrication in brief

What follows is a summary of the fabrication processes. More details are given further. We begin with the wafers with already present a layer of SiN. In the first lithography we fabricate a PR mask specifically made for lift-off. This mask reduces the amount of material deposited on the PR sidewalls. We deposit by sputtering the bottom contact electrode layers. Afterwards we do the lift off. That is the removal of the PR layer together with the on-top sputtered materials; leaving the patterned electrodes. Afterwards the piezoelectric layer is deposited by sputtering on the whole wafer (a PR mask is not used). Afterwards (in the same machine) the top contact is also deposited. Afterwards a PR protective mask is fabricated for the next step. The unwanted piezoelectric material and top contact layer is removed by anisotropic dry etching in a chlorine/argon ICP (Inductively Coupled Plasma) etcher. After O2 plasma strip of the PR another PR mask is fabricated. This time it is used to protect the fabricated structures during the following step; the release. The release is done in two steps. Firstly by anisotropic Bosh etching (SF6 and C4F8 chemistry) of SiN and Si. This machines vertical trenches. Afterwards we proceed with isotropic Si etching. With this last etching step the Si under the beam is etched away leaving the beam suspended.

2 Fabrication

2.1 First lithography – S1 to S4

In the first lithography a PR mask is fabricated. This mask is used to fabricate the bottom contact electrodes using sputter deposition and consequently lift off.

More in detail, in the first lithography we deposit two PR layers. The first (in contact with the wafer) is LOR 5A and the one on top of it is AZ1512. Two resists are used because the PR will be used as a mask for the sputter deposition of the bottom contact electrode. LOR 5A is used to obtain an empty region under AZ1512 to prevent the sputtered material to deposit on the sidewalls of the resist, as we can see in figure 2.

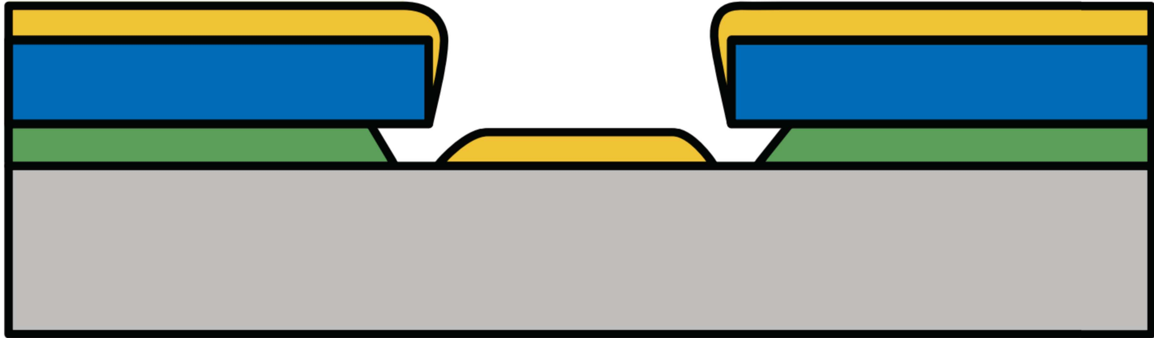

Figure 2: Image taken from the LOR 5A datasheet that shows how the LOR 5A (green) together with the top resist (blue, in our case AZ1512) forms a strong undercut to facilitate lift-off. In yellow is the sputtered material.

The material deposition on the sidewalls is an unwanted phenomenon that would occur more prominently if we only used one resist. It is an unwanted phenomenon because if it would happen to cover the whole PR sidewall than the PR remover would not be able to reach and remove the PR. However even if the wall would be partially covered it would still be detrimental. This because after the lift off we won't have only a flat layer of the sputtered structures but also on the edges of them there would be vertical deposition (where the wall was). Those vertical structures are called fences. In our case they could be extremely detrimental to the piezoelectric resonator because if tall enough they could make contact with the top electrode creating a short circuit. This would render the device unusable.

The first photolithography mask has the pattern of the bottom contact electrodes. Exposure was done in UV on the MA6 Gen3 mask aligner using a dose of 50mJ/cm2 (UV I-line used, contact exposure). To obtain a better bigger cavity under the AZ1512 PR the development step was done two times. After the development a short 10s low power oxygen plasma was used to descum the wafer (remove residues).

2.2 Sputter deposition of the bottom contact electrode – S5

For this step we used two different machines to compare the quality of the deposition of the bottom contact electrode. The two machines compared are the SPIDER and the DP650. With "quality of the deposition" in this case is meant which machine will deposit the bottom contact electrode with the less amount and size of fencing. The machine that achieves the less fencing is thus considered the machine best suited for the deposition of the bottom contact electrode. In each machine two wafers are used; a

test wafer and an high resistivity wafer. In SPIDER an adhesion layer of 15nm of AlN is deposited and afterwards 25nm Pt are deposited. In DP650 15nm Ti are deposited as adhesion layer and afterwards also 25nm Pt. Both SPIDER and DP650 are sputtering machines. One big difference is the adhesion layer; that in SPIDER is obtained by reactive sputtering (AlN) whereas in DP650 is just Ti.

2.3 Lift-off and inspection – S6 to S7

2.3.1 Method

The lift-off has been done in the wet bench for the 4 wafers. No sonication was used. The two wafers, that had been processed in the SPIDER for the deposition of the bottom contact electrode, had considerable worse lift-off than the ones processed in DP650. Some of the metallic film did not detach from the wafer, forming small spots varying from a few millimeters to hundreds of micrometers (rough eye estimation). Using a jet of PR remover to remove some of the remaining metallic film attached to the SPIDER's wafers proved to not be sufficient and the use of q-tips was necessary. This problematic was considerably less prominent on the DP650 processed wafers. In figure 3 and figure 5, one can still see that there are still some spots where the lift-off didn't occur. Both are wafers processed in SPIDER.

2.3.2 Strong fencing in SPIDER's wafers

The majority of devices processed in the SPIDER for the deposition for the bottom contact electrode present strong fencing in each device. The fences appear on the images as dark lines along the edges of the deposited electrode. Especially remarkable is the device shown in figure 4 presenting long and thick fencing along the contact for the beam. In figure 6 is shown one of the best devices I could find on the test wafer processed in SPIDER. Even this one showed some fencing.

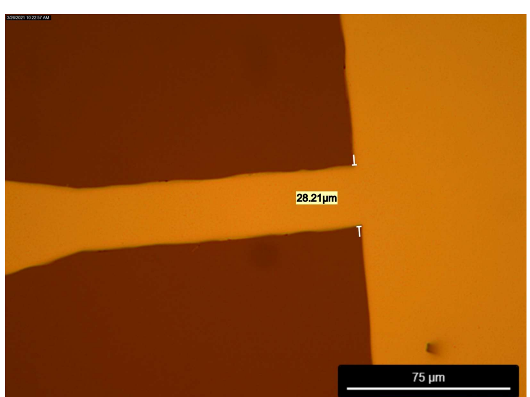

Figure 3: Remarkably non straight edges on HR wafer processed in SPIDER.

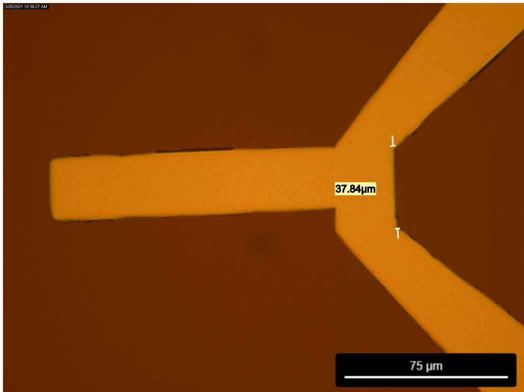

Figure 4: On the HR SPIDER's processed wafer it's easy to spot the big fences (black edges).

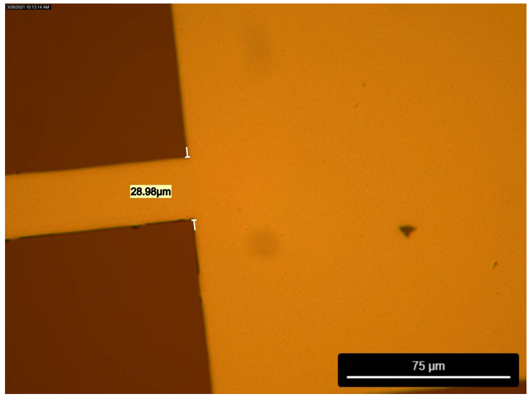

Figure 5: Also on this test wafer, also processed in SPIDER, it's easy to spot the big fences.

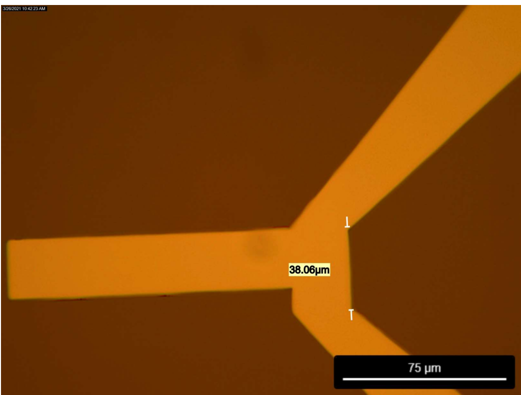

Figure 6: The best structure I could find on SPIDER's test wafer also has some fencing.

2.3.3 DP650's wafers

Wafers processed on DP650 for the bottom contact electrode appear a lot cleaner and do not have thick fences. On the HR wafer shown in figure 7 and figure 8 two examples of the fencing are shown. The fences on the DP650 HR processed wafer are thinner than the ones present on the ones processed in the SPIDER and are loosely attached. The two devices shown in figure 7 and figure 8 are among the worst I could find on the HR wafer processed in DP650. More representative of the general situation on the DP650's wafers are figure 9 and figure 10.

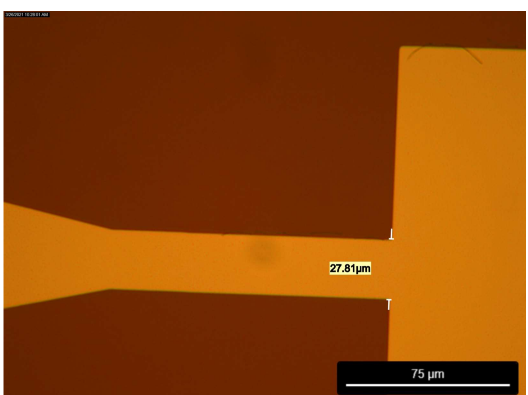

Figure 7: The HR wafer processed in DP650 presents straight edges, however presents some fencing half detached on some devices.

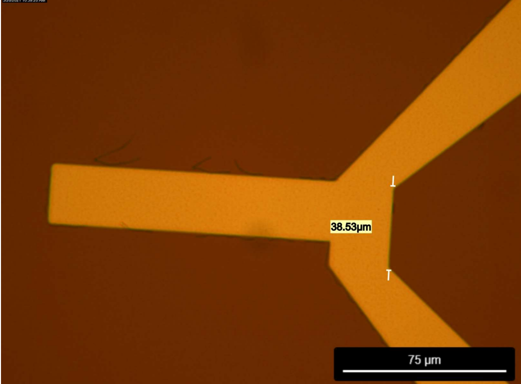

Figure 8: Another device on the DP650's HR wafer presenting some heavy fencing half detached on some devices.

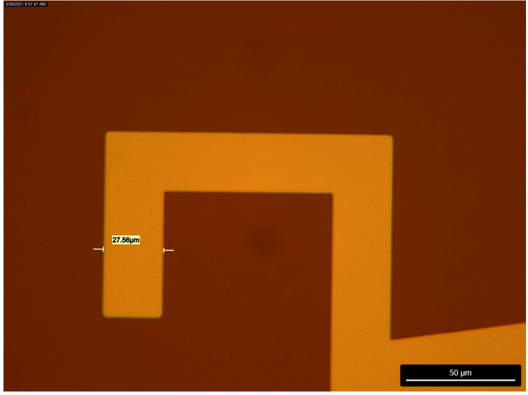

Figure 9: On the test wafer processed in DP650 all devices inspected did not present fencing of any sort.

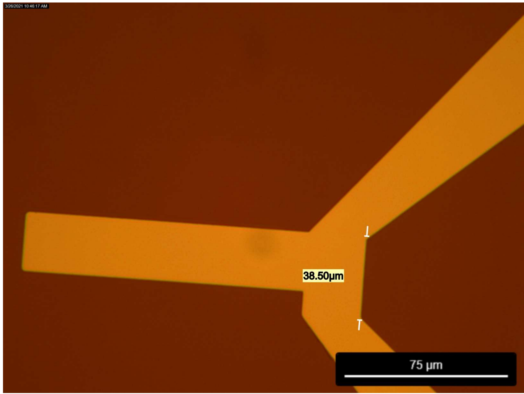

Figure 10: Another image of the test wafer processed in DP650 showing a clean device.

2.4 Sputter deposition of active piezoelectric layer and top contact electrodes – S8

In this step the active piezoelectric layer was deposited together with the top contact electrodes layer. The cleaner wafers (DP650 wafers, one test and one HR) were used to continue the fabrication. The wafers from the other machine (SPIDER) were not used further. From this point forward we will refer to the DP650's wafers only as test and HR wafers for brevity.

The piezoelectric layer is used as a mean of activation of the resonators, applying a voltage across the top and bottom electrode generates an electric field across the piezoelectric material that will deform accordingly to the piezoelectric effect. This to occur needs that the bottom and top electrode are not connected. Fences of the bottom contact are thus detrimental to the functioning of the device. This is why the wafers from the SPIDER were not used.

On the test and HR wafer were deposited 200nm of AlN (piezoelectric material) and 25nm Pt as the top contact electrode; both by sputtering (reactive sputtering for AlN). The unwanted materials deposited will be removed this time by anisotropic directional dry etching instead of lift off. To do this in the next step a PR mask was fabricated to protect the regions we wanted to keep.

2.5 Second lithography – S9 to S11

After the deposition of the piezoelectric layer and the top contact the not needed materials needed to be removed. This was done using dry etching (see step 12 further for details). The second lithography served to fabricate the protective mask for the etching. AZ ECI 3007 was used as photoresist with a thickness of 1.5µm. The automatic coater ACS200 was used for the deposition and development of the PR. The alignment with the second photolithography mask and UV exposure was done manually on the MA6 Gen3 mask aligner using a dose of 180mJ/cm2 (UV I-line used, contact exposure).

2.5.1 Misalignment of HR wafer

During the second lithography, the alignment on the HR wafer was not good enough. The PR structure was visibly out of boundaries, as one can clearly see on figure 11. The resist was stripped and the lithography repeated with better accuracy. The new good alignment can be seen in figure 20. The alignment of the test wafer was good enough. On figure 12 it's quite difficult to see. However in figure

14, after the anisotropic dry etching of the top electrode and piezoelectric layer (details further), one can see, even though the alignment is not perfect, that the top contact is inside its boundaries.

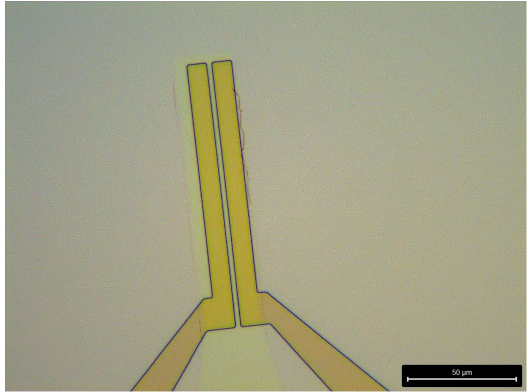

Figure 11: Bad alignment on the HR wafer. We can see that one of the future contacts is not even on the structure underneath.

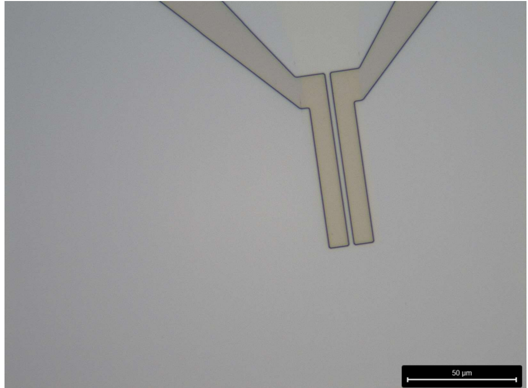

Figure 12: On the test wafer, the alignment is much better than on the HR one. The future contacts are inside of the structure.

2.6 Anisotropic dry etching of Pt and AlN – S12 to S13

The removal of the excess Pt and AlN is done in an anisotropic chlorine/argon chemistry ICP (Inductively Coupled Plasma) etcher; namely STS. In this machine the ions present in the gas impinge on the substrate. The ions are attracted by a voltage bias applied to the substrate. Those ions by impinging on the substrate knock off the atoms from the substrate; etching it. Thanks to the bias voltage the etching is directional.

Here we can see that immediately after the etching the surface of the wafer is full of redeposited materials. This appears as black dots scattered everywhere on the wafer, as one can see in figure 13 and figure 14. Those will disappear after KOH etching of the remaining AlN.

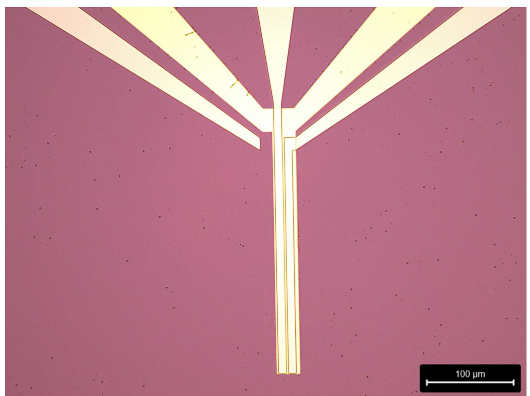

Figure 13: Test wafer after etching Pt and AlN. We can see some strips and dots.

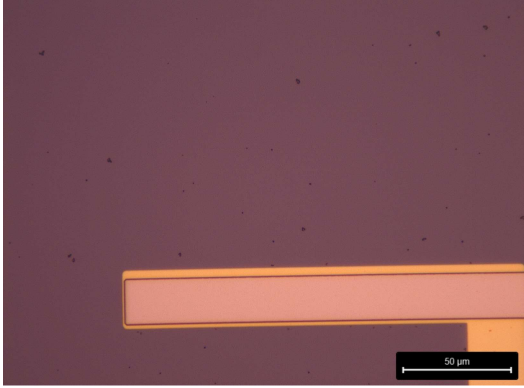

Figure 14: Closeup on the test wafer after etching Pt and AlN.

To detect the end of the etching, end-point detection was used in conjunction with an estimation of the time needed to etch. The end-point detection consists of using a laser and detect the reflected intensity. This was proven tricky to use. It was difficult to determine the end of the etching of AlN. After the etching of Pt the reflection intensity graph over time did not look at all similar to the one predicted for a transparent material deposited on a reflective one. This was most probably due to the

presence of SiN (another transparent material) underneath AlN. Knowing this, the responsible route was to stop the etching at the predicted time and leave some AlN; this to prevent etching the bottom contact also made of Pt. The remaining AlN was measured with Filmetrics F54. On figure 15 and figure 16, the measurements of the thickness of the remaining AlN are shown.

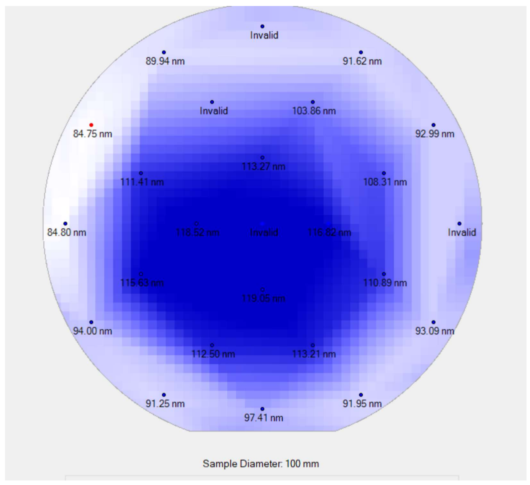

Figure 15: Thickness of remaining AlN on the test wafer after the etching step.

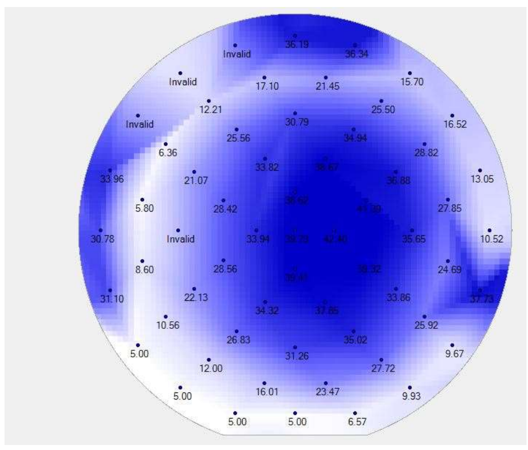

Figure 16: Thickness of remaining AlN on the HR wafer after the etching step. Units in nm.

2.7 Inspection after anisotropic dry etching and wet etching of AlN – S14

To remove the remaining AlN, the process used was wet etching in 40% KOH solution until visual indication of the end of the reaction (change of color to homogeneous color). This was followed by washing the wafers in DI water three times followed by neutralization in 37% HCl solution for around 2 hours and again three washes in DI water. The neutralization with HCl, an acid, is done to neutralize all residual KOH remaining on the wafer (the acid compensate for the basis). The remaining KOH on the wafer is undesirable since it could damage the structure. In all the steps, cleanroom DI water was used.

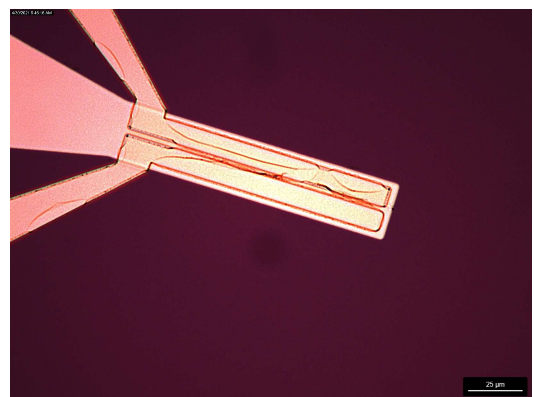

Figure 17: HR wafer after KOH. We can see the remaining PR.

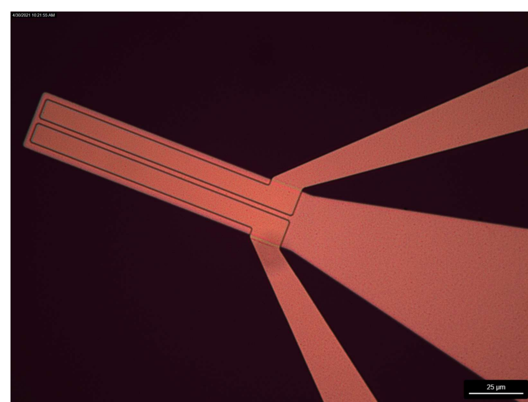

Figure 18: After the O2 plasma strip of the PR the HR wafer has a clean aspect.

In figure 17 and figure 19, we can still see that most of the PR is still present. After PR strip in a O2 plasma stripper, we can see in figure 18 and figure 20 that both wafers are clean and present no problems.

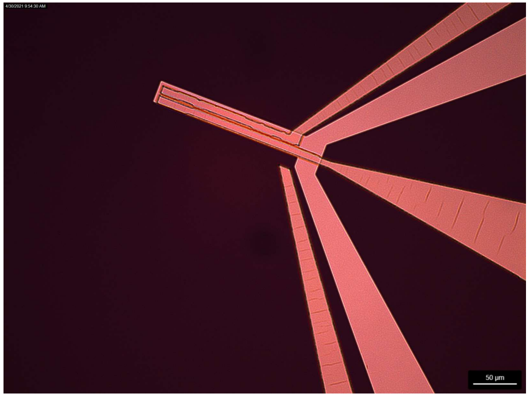

Figure 19: Test wafer after KOH. We can see the remaining PR.

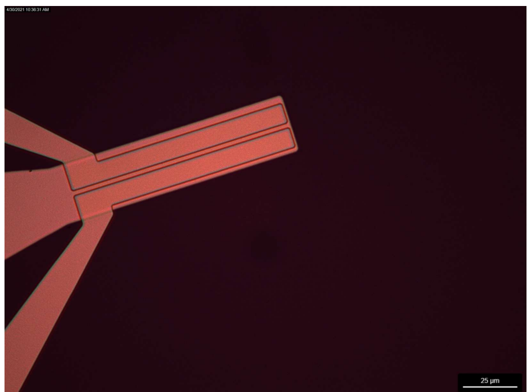

Figure 20: After the strip on the O2 plasma stripper, the test wafer has a clean aspect.

2.8 Photolithography and misalignment – S15 to S17

In the third and last lithography a layer of 5µm of AZ ECI 3027 was deposited. The exposure dose was 430 mJ/cm2 and done in contact. This mask serves as a protective mask for the following steps; the release of the structures.

2.8.1 Misalignment

As it is quite obvious from figure 21 and figure 22, I aligned the mask to the wrong alignment mark. The test and HR wafers were subsequently stripped and correctly aligned.

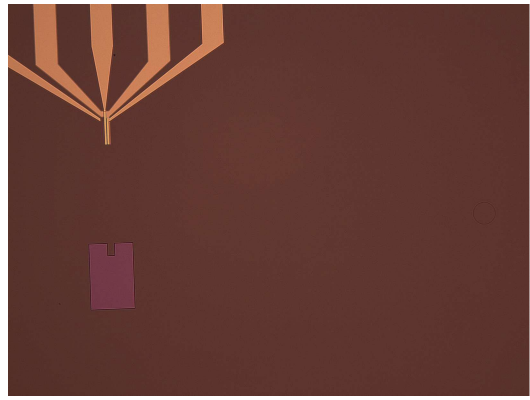

Figure 21: Misalignment caused by aligning to the wrong alignment mark.

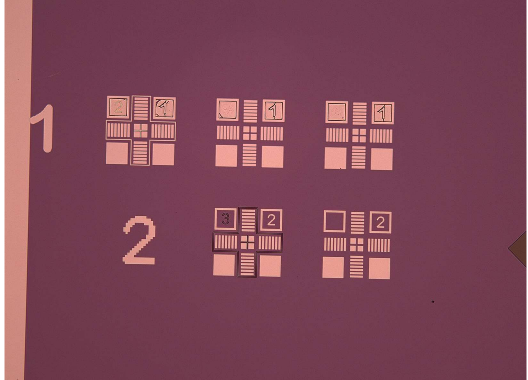

Figure 22: The wrong alignment mark I used to align, first alignment mark on row 2.

2.8.2 Correct alignment and measurements

After the correct alignment some pictures and measures of the PR were taken, as one can see in figures 23, 24, 25 and 26.

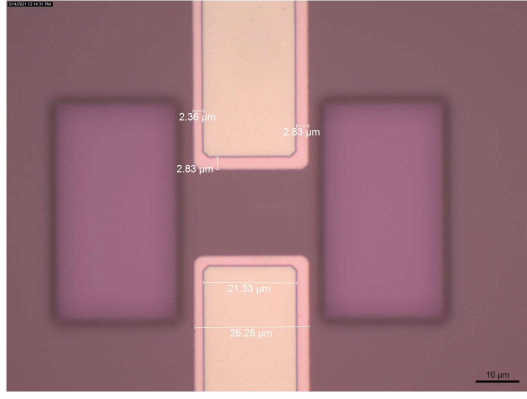

Figure 23: Measures of some dimensions of the device A1L1 on the HR wafer.

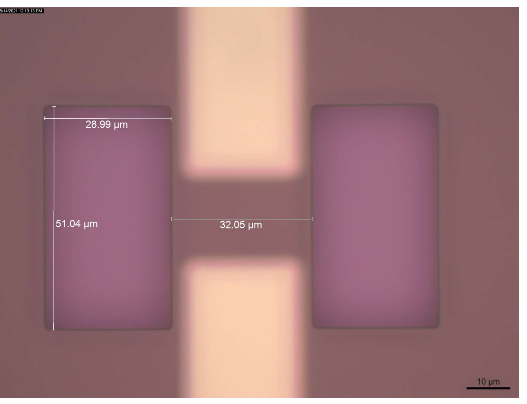

Figure 24: Measures of some dimensions of the PR on device A1L1 on the HR wafer.

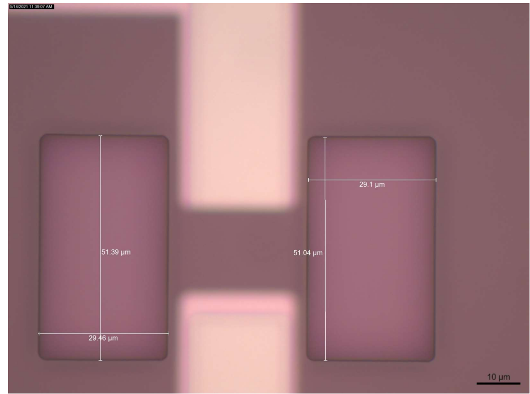

Figure 25: Measures of some dimensions of the PR on device A1L1 on the test wafer.

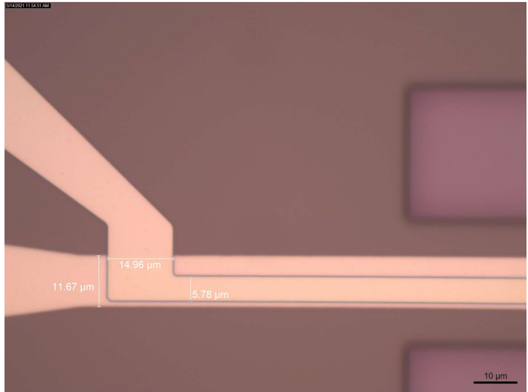

Figure 26: Measures of some dimensions of the device D2L6 on the test wafer.

2.9 Release

2.9.1 Anisotropic dry etching – S18

First of all we do an anisotropic dry etching. This aims to etch deep trenches that will allow the isotropic etching of Si for the release step to occur in a more contained and directed manner. The anisotropic dry etching is done using the Bosh process using SF6 and C4F8 chemistry. With this we etch the SiN first, stop the machine once finished (end point detection), run a clean cycle and afterwards proceed to the anisotropic dry etching of Si creating approximately 20µm depth trances. After the Bosch etching of SiN and Si, we have a straight cavity.

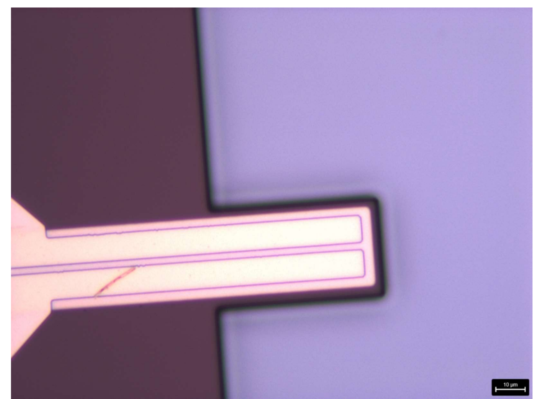

Figure 27: HR wafer after isotropic etching. The device was damaged before the process.

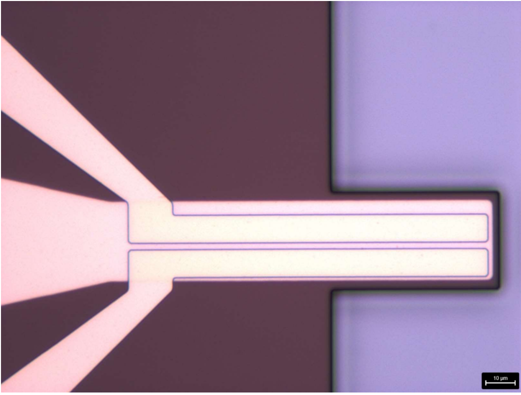

Figure 28: Test wafer after anisotropic etching.

2.9.2 Isotropic etching – S19

The release of the resonators is done by isotropic etching of Si. Some structures (the one with a small aperture for etching) will have smaller cavities underneath than the ones with bigger apertures. This is due to the mass loading effect. The smaller the aperture the less reactive gas can enter and exit freely, slowing the etch rate.

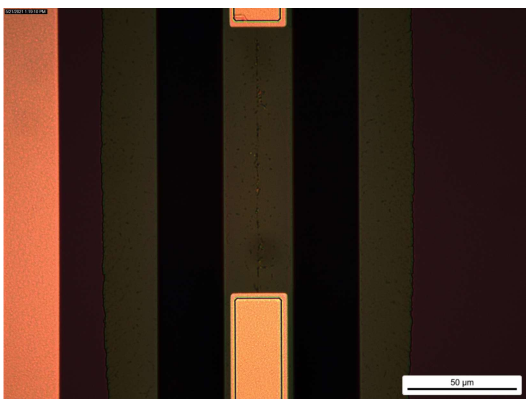

Figure 29: Device C3L4 on the HR wafer. We can see that, under the SiN, there are some residues even though the device is released.

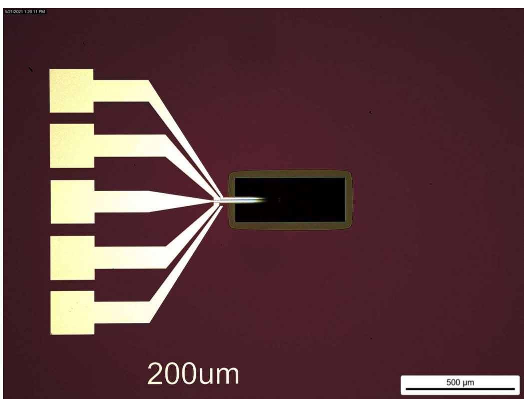

Figure 30: Device C3L4 on the HR wafer. We can see that the cantilever bends downwards: this means it is released.

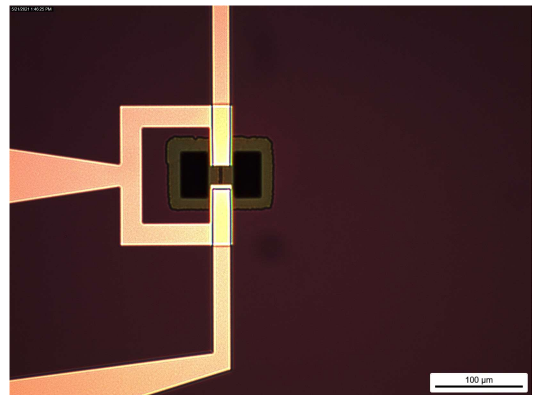

Figure 31: Device A1L1 on the test wafer. This device could not be released completely due to the mass loading effect (small aperture, 50um).

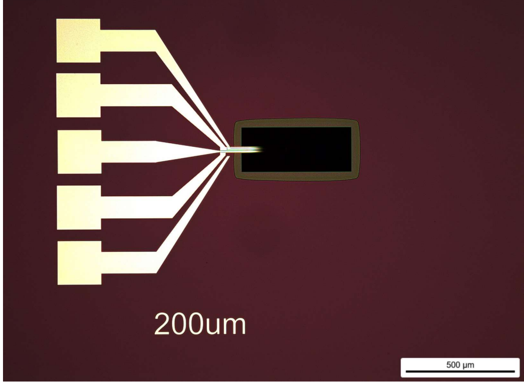

Figure 32: Device C3L4 on the test wafer. We can see that the cantilever is released thanks to its bending.

2.9.3 PR Strip – S20

After inspection the PR mask was removed using an O2 plasma stripper.

3 Results

3.1 Resistance measurement between the top to bottom electrodes

In figure 33, the final results are presented. In blue the measurements of the devices on the test wafer before the release, and in red after the release. In beige, the measurements of the devices on the HR wafer before the release, and in gray after the release. In total, the same 70 top to bottom contacts were measured on each wafer before and after the release.

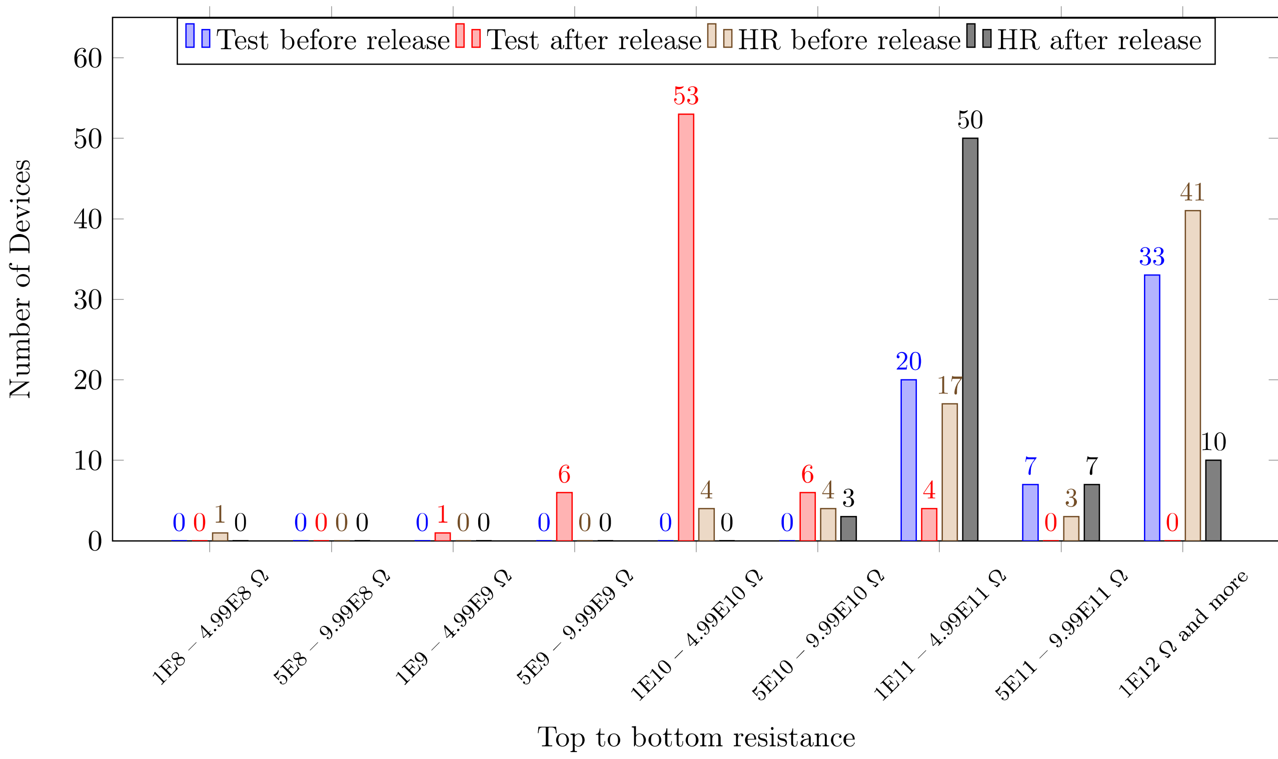

Figure 33: Number of devices on each wafer in a given resistance range, before and after release. We clearly see that the release reduced quite drastically the resistance for the HR wafer's devices.

We can see that, prior to the release, the HR wafer is marginally better than the test one. However, the difference is not significative. The majority of measurements for the HR wafer fall on the TΩ and above interval and almost half of the devices on the test wafer also fall in this interval.

However after the release, we can see that the majority of the device's resistances of the HR wafer fall in the interval of 100 GΩ to 500 GΩ and the majority for the test wafer fall in the interval of 10 GΩ to 50 GΩ. The resistance of the majority of the devices on the test wafer have their resistance one order of magnitude less than the one on the HR one. This significative difference indicates that the high resistivity wafer yielded better contact resistance in general, compared to the test wafer.

4 Appendix

4.1 Abbreviations used

HR is used for high resistivity.

PR is used for photoresist.

The elemental symbols are used for their corresponding elements.

SiN is used for silicone nitride.

AlN is used for aluminum nitride.

4.2 References

CMi website.

Figure 2: Taken from the LOR 5A datasheet; "LOR and PMGI Resists for Bi-layer Lift-off Processing"

4.3 History of the wafers

Table 1: Table with the history of the wafers. "S" stays for "step". If followed by "E" it means it is an extra step that was not on the process flow. If followed by "B" it stands for "bis", because that step had to be repeated.

Wafer	Step	Name	Materials	Machine	Recipe	Comment
HR21, T11, HR20, T04	S1	Photolithography: Coating	0.4μm LOR 5A, 1.1μm AZ1512	Z6 – EVG150	C4-LOR-u4-1512-1u1-EC	AZ1512 on LOR 5A
HR21, T11, HR20, T04	S2	Photolithography: Exposure		Z1 – MA6 Gen3	dku.firstexposure	Dose: 50mJ/cm2
HR21, T11, HR20, T04	S3	Photolithography: Development		Z6 – EVG150	D4-HB-1512-1u1-PVD	Double development
HR21, T11, HR20, T04	S4	O2 Plasma Descum		Z2 – Tepla	10s low power	Let chamber cool down before descum
HR21, T11	S5	Sputter deposition	15nm Ti, 25nm Pt	Z11 – DP650	RTU-Ti-Pt (Ti 37.3s, Pt 48,4s)	Using average deposition rates of 0.67 nm/s Pt and 0.31nm/s Ti
HR20, T04	S5	Sputter deposition	15 nm AlN, 25 nm Pt	Z4 – SPIDER600	AlN-1 (19s), Pt-D-1 (14s, 500W, Ar 5sccm)	
HR21, T11, HR20, T04	S6	Lift-off	PR + Ti + Pt	Z13 – Arias Solvent Wet Bench	Left in immersion in 1165 remover until lift off, washed with IPA and than DI water	Sonication not used, manual intervention for attached clumps necessary

HR21, T11, HR20, T04	S7	Inspection		Optical microscopes		
HR21, T11	S8	Sputter deposition	200nm AlN, 25nm Pt	Z4 – SPIDER600	AlN-T-1(4min), Pt-D-1(14s)	
HR21, T11	S9	Photolithography: Coating	1.5μm AZ ECI 3007	Z1 – ACS200	C4-D-3007-1u5-EC	
HR21, T11	S10	Photolithography: Exposure		Z1 – MA6 Gen3	dku.secondexposure	Dose: 180mJ/cm2
HR21, T11	S11	Photolithography: Development		Z1 – ACS200	D4-PEB-3007-1u5	
HR21, T11	S11E1	Inspection		Microscope		HR21 misaligned
HR21	S11E2	O2 Plasma PR strip	AZ ECI	Z2 – Tepla	3min, 1min, 3min, 1min high power	Stripped until clean
HR21	S9B	Photolithography: Coating	1.5μm AZ ECI 3007	Z1 – ACS200	C4-D-3007-1u5-EC	
HR21	S10B	Photolithography: Exposure		Z1 – MA6 Gen3	dku.secondexposure	Dose: 180mJ/cm2
HR21	S11B	Photolithography: Development		Z1 – ACS200	D4-PEB-3007-1u5	
HR21, T11	S12	Anisotropic dry etching	depth: 25nm Pt, 200nm AlN	Z2 – STS	Aln.set (1min 30s)	Color change due to thinning of AlN, not removed totally.
HR21, T11	S12E1	AlN thickness measurement		Z3 – Filmetrics F54		Measurment of remaining AlN
HR21, T11	S12E2	AlN wet etching	AlN	Chemistry bench in MED 0 2322 LAB	Immersion in 40% KOH solution until visual observation of change of colour followed by neutralization in HCl and finished by DI water wash	KOH etching and HCl neutralization
HR21, T11	S12E3	Two points resistance measurement		Measuring probe station in MED 0 2322 LAB		70 devices measured and compared on each wafer
HR21, T11	S13	O2 Plasma PR strip	AZ ECI	Z2 – Tepla	2min high power	
HR21, T11	S14	Inspection		Microscope		
HR21, T11	S15	Photolitography: Coating	AZ ECI 3027	Z1 – RiteTrack	C4-N-3027-5u-EC	5μm thickness
HR21, T11	S16	Photolithography: Exposure		Z1 – MA6 Gen3	dku.thirdexposure	430 mJ/cm2
HR21, T11	S17	Photolithography: Development		Z1 – RiteTrack	D4-PEB-3027-5u-B	
HR21, T11	S17E1	Inspection		Microscope		Both wafers misaligned, aligned to wrong alignment mark.
HR21, T11	S17E2	O2 Plasma PR strip	AZ ECI	Z2 – Tepla	5min high power	Stripped until clean

HR21, T11	S15B	Photolitography: coating	AZ ECI 3027	Z1 – RiteTrack	C4-N-3027-5u-EC	5µm thickness
HR21, T11	S16B	Photolithography: Exposure		Z1 – MA6 Gen3	dku.thirdexposure	430 mJ/cm2
HR21, T11	S17B	Photolithography: Development		Z1 – RiteTrack	D4-PEB-3027-5u-B	
HR21, T11	S17E1B	Inspection		Microscope		Took images for measurement
HR21, T11	S18	Anisotropic dry etching	ls-SiNx/Si	Z2 – AMS200	SIO2–PR1:1 (T11/HR21) 2m31s/2m40s SiN etch, 1m30s/ 1m30s Bosch etching	500nm ls-SiNx and 20µm Si. Process alted when SiN is etched. Run O2 plasma to clean machine (dummy used). Insert back wafer for Si etching.
HR21, T11	S19	Isotropic dry etching	Si	Z2 – AMS200	(T11/HR21) 3m/3m Si-Release, 2m/1m Si-Release	Lateral etching to release structures, checked after 3 minutes
HR21, T11	S20	O2 Plasma PR strip	AZ ECI	Z2 – Tepla	1min, 1min, 2min, 2min, 2min, 2min high power	Stripped until finished
HR21, T11	S21	Inspection		microscope		
HR21, T11	S21E1	Two points resistance measurement		Measuring probe station in MED 0 2322 LAB		The same 70 devices measured in step S12E3 and compared on each wafer

4.4 Process flow

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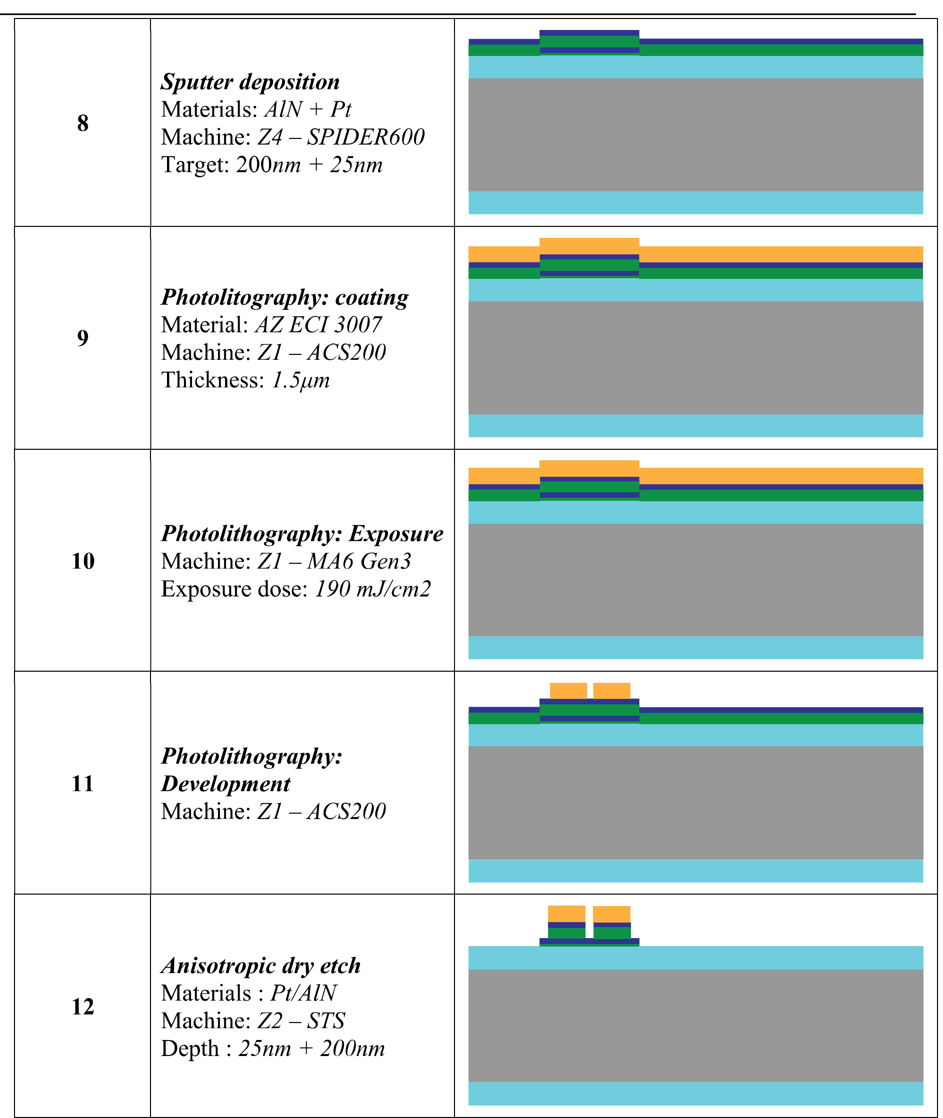
OPTIMIZATION OF PZE ELECTRODES FOR SUSPENDED MICROCHANNEL RESONATORS

Technologies used			
Photolithography, Sputtering, Lift-off, Dry etching, Wet etching, PR strip			
Photolitho masks			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**5 um**	First Mask	
2	**5 um**	1 um	
3	**5 um**	1 um	
Substrate Type			
Silicon <100>, Ø100mm, 525 um thick, Single-side polished Layer: 500nm low-stress silicon nitride			

Process outline

Step	Process description	Cross-section after process
0	State of the wafer at the beginning of the process	
1	***Photolitography: coating*** Material: *AZ1512 on LOR 5A* Machine: *Z6 – EVG150* Thickness: *0.4µm LOR, 1.1µm, AZ1512*	

2	***Photolithography: Exposure*** Machine: *Z1 – MA6 Gen3* Exposure dose: *50mJ/cm*^{2}	
3	***Photolithography: Development*** Machine: *Z6 – EVG150*	
4	***O2 Plasma Descum*** *Machine: Tepla Z2* *10s low power*	
5	***Sputter deposition*** Materials: *Ti + Pt* Machine: *Z11 – DP650* Target: *15nm + 25nm*	
6	***Lift-off*** Materials : *PR + Ti + Pt* Machine: *Z1 – Photolitho bench*	
7	***Inspection*** Machines: *Z1 – Microscope, Z1 – Zeiss LEO*	



8	***Sputter deposition*** Materials: *AlN + Pt* Machine: *Z4 – SPIDER600* Target: 200*nm + 25nm*	
9	***Photolitography: coating*** Material: *AZ ECI 3007* Machine: *Z1 – ACS200* Thickness: *1.5µm*	
10	***Photolithography: Exposure*** Machine: *Z1 – MA6 Gen3* Exposure dose: *190 mJ/cm2*	
11	***Photolithography: Development*** Machine: *Z1 – ACS200*	
12	***Anisotropic dry etch*** Materials : *Pt/AlN* Machine: *Z2 – STS* Depth : *25nm + 200nm*	

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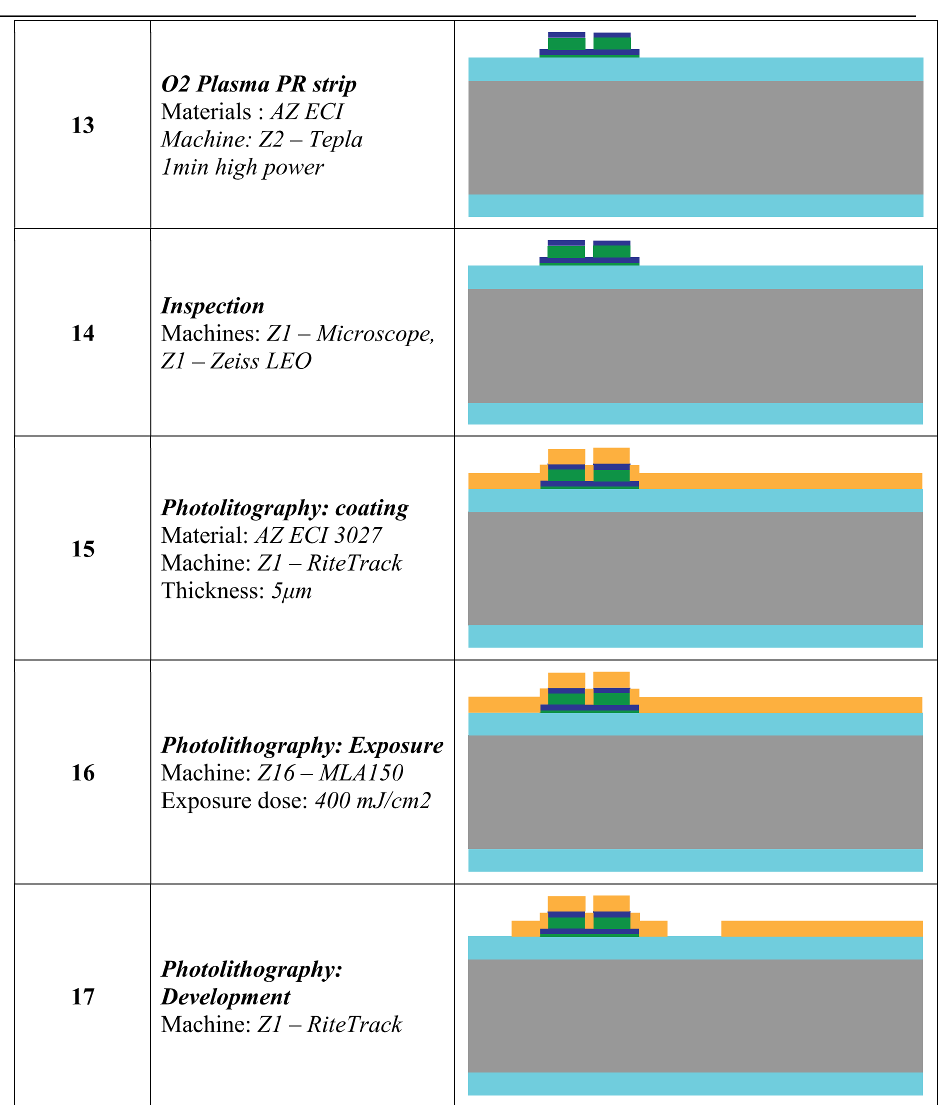

13	***O2 Plasma PR strip*** Materials : *AZ ECI* *Machine: Z2 – Tepla* *1min high power*	
14	***Inspection*** Machines: *Z1 – Microscope, Z1 – Zeiss LEO*	
15	***Photolitography: coating*** Material: *AZ ECI 3027* Machine: *Z1 – RiteTrack* Thickness: *5µm*	
16	***Photolithography: Exposure*** Machine: *Z16 – MLA150* Exposure dose: *400 mJ/cm2*	
17	***Photolithography: Development*** Machine: *Z1 – RiteTrack*	

18	***Anisotropic dry etching*** Materials : *ls-SiNx/Si* Machine: *Z2 – AMS200* Depth : *500nm + 20µm* Program for SiN etch: *SIO2_PR1:1* *Notes: Process alted when SiN is etched. Run O2 plasma to clean machine (dummy used). Insert back wafer for Si etch.*	
19	***Isotropic dry etching*** Materials : *Si* Machine: *Z2 – AMS200* Lateral depth : *20µm*	
20	***O2 Plasma PR strip*** *Machine: Z2 – Tepla* Materials : *AZ ECI* *1min high power*	
21	***Inspection*** Machines: *Z1 – Microscope, Z1 – Zeiss LEO*	