EPFL

Semester Project at ANEMS Lab

Development of an encapsulation solution for suspended microchannel resonators

---

Student:

Sarah Cuesta (275368)

Supervisor:

Damien Maillard

Professor:

Guillermo Villanueva

June, 2021

Contents

1 Introduction **2**

2 Encapsulation Solution Ideas **3**

3 Process Flow Preparation **4**
3.1 Initial state of the substrate 4
3.2 Photolithography 4
3.3 Etching 5
3.4 Bonding via a Parylene-C layer 5

4 Mask Design **7**

5 Fabrication in Cleanroom **8**
5.1 Choice of photoresist for photolithography 8
5.1.1 AZ 40XT 8
5.1.2 AZ 10XT-60 8
5.2 Etching 10
5.2.1 Dry etching of SiO_2 and SiN_x 10
5.2.2 DRIE of Si 10
5.3 Bonding 11
5.3.1 Parylene Deposition 11

6 Conclusion **12**

7 References **13**

1 Introduction

Microelectromechanical systems (MEMS) are devices that integrate electrical and mechanical functions at the nanoscale. MEMS provide unique advantages such as high sensitivity, small size, and low power consumption. In recent years, resonators have shown great potential as sensors. The working principle of a resonant sensor is illustrated in Figure 1. An event is measurable by inducing a change in the resonant frequency. The studied resonator is a beam cantilever in flexural mode, as illustrated in Figure 2. More precisely, we will be working with silicon nitride beams, actuated by electrodes on top. We intend to apply this project later to SMRs from the fabrication process from the article [2]. Such type of resonator offers great advantages as sensor due to its low mass for higher sensitivity.

The resonator's performance in terms of frequency stability is highly related to their Quality factor (Q) describing how underdamped a resonator is. This factor is approximately defined as the ratio of the initial energy stored in the resonator to the energy lost. The energy lost directly affects the sensitivity in a transducer, thus the goal is to minimise it. As previously stated, most of the energy lost from this type of resonator comes from the friction with air, so ideally the resonator should be in vacuum. The goal of this project is to create a reliable process flow for the fabrication of a vacuum encapsulation for the resonator. This process shall be done in few steps and with standard processes from cleanroom. This encapsulation provides a wafer-level packaging for the sensor, which has multiple industrial benefits such as increasing yield and reliability and decreasing cost.

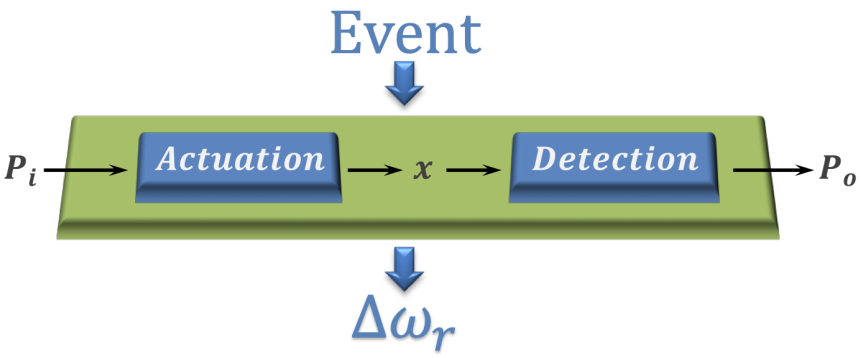

Figure 1: Resonant sensor, illustration from Advanced MEMS course at EPFL

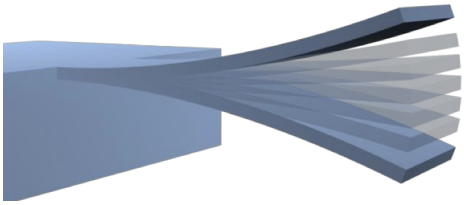

Figure 2: Cantilever beam resonator with the first flexural mode

2 Encapsulation Solution Ideas

The first step in developing a solution is to do research on the current processes for the fabrication of vacuum encapsulations directly on chip using standard microfabrication techniques. One possible approach was making a vacuum-encapsulated microchamber as in the article: [3]. However, this wasn't suited to our cantilever device nor to the standard processes at CMi. The best way to encapsulate the resonators directly in a wafer is to bond another wafer with cavities aligned to the resonators cavities, thus forming an encapsulation. The idea is illustrated in Figures 3 and 4. The design of the wafer that we want to bond to is shown in Figure 5. The wafer contains electrode pads to actuate the resonators and make measurements, the cantilevers are in the center of a released cavity corresponding to the encapsulation.

Figure 3: Front Chip design

Figure 4: Lateral Chip design

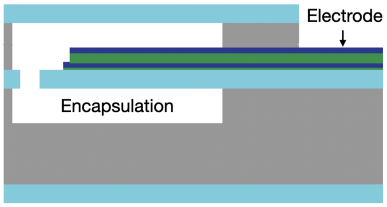

Figure 5: Lateral Encapsulation design

The type of bonding that has the longest long-term stability is the anodic bonding. However this process involves a minimum voltage of 400V, that would generate an electric current that could make the devices electrically shorted. This would make the devices useless for piezo-electric measurements. For our application the process must be compatible for bonding a wafer with micropatterned features and containing electrodes. This is why we would rather use an adhesive bonding via an intermediate polymer layer. A wafer bonding technique used in CMi in this cases is via a Parylene-C layer. For this technique, we will apply a known process as described in a paper from EPFL, to make sure that it works. This technique was seen in the article [1].

Regarding the membrane, it will be made of low-stress SiN_x, for strength, deposited onto a SiO_2 layer. The reason why we have SiO_2 is that when we do the Bosch process, this SiO_2 acts as a stop layer. If we had SiN_x only, we would damage it during the etching process. This combination has proven an improvement in the mechanical properties of the membrane.

3 Process Flow Preparation

Once that the solution to implement has been studied and chosen, the next step is to prepare the process flow.

3.1 Initial state of the substrate

Step 0: The state of the wafer at the beginning of the process

- Silicon $< 100 >$
- Ø100 mm
- 525 μm thick
- Single-side polished
- Coating layer on both sides: 200nm silicon dioxide inside, 700nm low-stress silicon nitride outside

Step 1: Aluminium coating on the backside

This step is essential to protect the membranes during the process of etching Silicon. It will be done by evaporation on the EVA 760 machine, to coat several wafers at the same time. The thickness of the deposition will be of $2\mu m$.

3.2 Photolithography

Only one photolithography is needed to pattern at the same time the cavities for encapsulation and the areas to be released for the electrodes. Since we will be etching through the whole Silicon of $525\mu m$ of thickness, the photoresist recommended by CMi is AZ 40-XT. According to the estimation ratios on the CMi webpage on the etching rate of photoresist over the etching rate of each of the processes, approximatively $7\mu m$ of photoresist will be etched. This is why the photoresist selected is $AZ40-XT$ with a thickness of $20\mu m$. This was the first choice, but later during the fabrication process there will be some modifications explained in the section 5.1.
The minimal thickness is computed: $SiO_2 + SiN_x = 900nm$ with 4,2:1 selectivity to PR and $Si = 525\mu m$ with 75:1 selectivity to PR, gives: $\frac{0.9}{4.2} + \frac{525}{75} = 7.215\mu m$

Step 2: HDMS pre-treatment

The HMDS surface treatment is highly recommended to promote adhesion of the photoresist to Silicon surfaces. This process consists of drying the wafer first and then deposing a monolayer of the HMDS priming agent that will make the surface more hydrophobic, ensuring a good adhesion of the photoresist. The dehydratation of the wafer surface is achieved by rising the temperature of the wafer and reducing the pressure. While this process may not totally eliminate all of the water molecules on the surface of the wafer, particularly the chemically bound water, it does remove a large percentage and it prepares the wafer for the next step.

Step 3: Photoresist Coating

The coating of the $AZ40XT$ will be done at the $ACS200$ machine.

Step 4: Exposure

The exposure of the design will be done at $MLA150$. The design for this exposure is in the next Section 4.

Step 5: Development

The development will be done again on $EVG150$. After the development the wafer is cleaned in a DI water bath.

Step 6: Hardbake

A hardbake will be performed after development in order to increase the thermal, chemical, and physical stability of developed resist structures for subsequent processes. The hardbake is done at 85°C on an oven and left overnight.

3.3 Etching

Step 7: Deep Reactive Ion Etching of Si

The Bosch process is used to etch structures with high AR. In our design the smaller structures are of the order of $200\mu m$, and the thickness to etch is $500\mu m$. Thus, the AR is 5, this means the etch is vertical in this structures. However the AR is not too large so we can choose a fast process to etch $500\mu m$. This could take a long time if the time if the passivation time (time delivering the passivating gas C_4F_8) is long in comparison to the etching time (time delivering the etching gas SF_6) in the cycle. This is why we choose the recipe $SOIaccurate4+$, which has the higher time delivering SF_6. This process is adapted to bulk Si wafers and optimized to avoid notching while giving a low Aspect Ratio Dependent Etching (ARDE) to have similar etch rates all over the wafer.

Step 8: Photoresist Stripping

After all the etching has been done, the photoresist is stripped with O_2 plasma on the Tepla GIGAbatch. The plasma also activates the surface for the next step, so ideally it shall be done just before the next step.

Step 9: Removal of Al layer

The Aluminium layer on the backside that was used to protect the membranes during the DRIE process can be removed at this point. This is done on the Plade Metal bench with the chemical: ANP (H3PO4 85% + CH 3COOH 100% + HNO3 70% at ratios 83:5.5:5.5).

3.4 Bonding via a Parylene-C layer

The following bonding technique comes from the article previuously mentioned [1]. The steps of the technique are illustrated in Figure 6. The illustration is extracted from the same article.

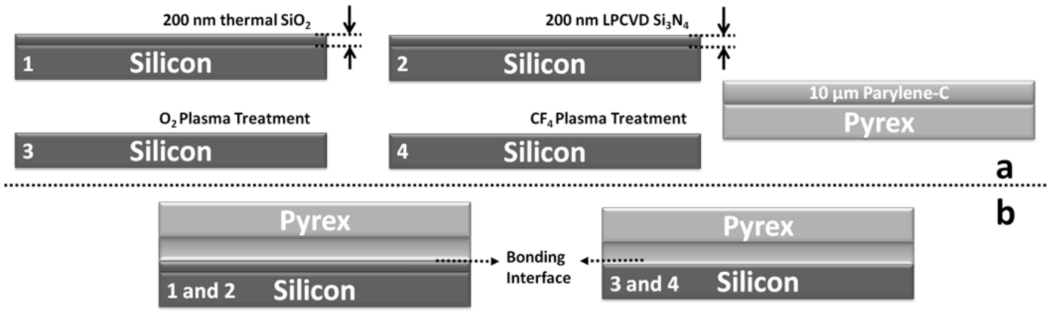

Figure 6: Illustration of the bonding process. (a) The process uses a Pyrex wafer covered with a $10\mu m$ thick parylene-C layer. 4 different silicon substrates have been prepared (b) All of the bonding with parylene-C was performed at **280 °C under vacuum during 40 minutes** while applying 1000 mbar pressure. Prior to bonding, Pyrex wafers were **plasma-treated during 15 s at 200 W** under 400 sccm O2 flow for surface activation of the parylene-C layer.

Step 10: Parylene coating

The coating of a $10\mu m$ layer of Parylene-C is done on the frontside of the wafer.

Step 11: O_2 Plasma-treatment

This step activates the Parylene by introducing chemical functionalities at the surface to enhance the bonding later. The wafer will be O_2 plasma-treated at 200 W during 15 seconds for surface activation using a $Tepla300$ plasma system under 400 sccm O_2 flow.

Step 12: Alignment of both wafers

The wafer is aligned to the wafer from a parallel process, containing the cantilevers released and the electrodes. This is done with the marks from both pattern on the $BA6$ machine.

Step 13: Bonding of wafers

Finally, the wafer will be bonded to the other one. It will be bonded on Suss $SB6$ vacuum bonder at 280°C during 40 minutes under vacuum with a tool pressure of 1000 mbar. The selection of the temperature is done to be close to stress-free bonding temperature at the bonding interface. Here, since we are bonding silicon with silicon we can choose the lower temperature possible to minimize deformations and stress.

4 Mask Design

As stated in the process flow, one single mask is needed for the whole process. The exposition of one single layer allows to pattern at the same time the encapsulation areas and the areas for the electrode pads. Since we will etch through the whole Si layer, only a thin membrane of SiO_2 and SiN_x will be left on the exposed areas. The idea is to make the encapsulation surface small enough to resist the stress from the differential pressure in vacuum. So the surface shall be as small as possible to make a stronger membrane while having at least with $100\mu m$ tolerance for alignment on both directions. Whereas the membranes above the electrode pads will be broken and shall be big enough to allow connections. The design of the layer to expose is done over the mask set design of the wafer that we want to bond to (shown in Figure 7 and in Figure 8). The layer of interest is in the pink in Figure 9 and in Figure 10. Only this layer will be exposed during photolithography. Alignment marks are added on top of the marks of the other design on the four sides of the wafer to allow alignment before bonding. In addition, multiple test membranes with different sizes and shapes are included to test their strength.

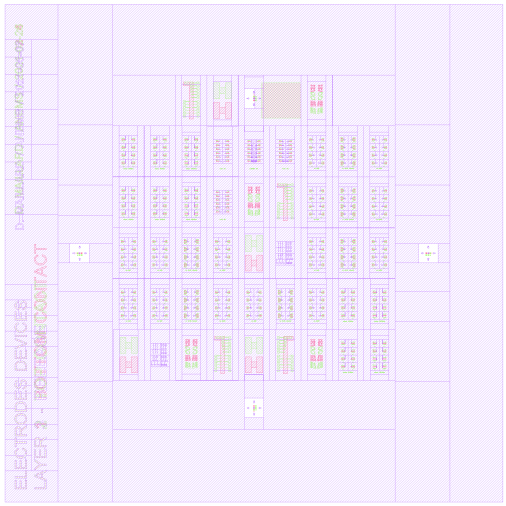

Figure 7: Mask design for electrodes and cantilever release from the parallel process

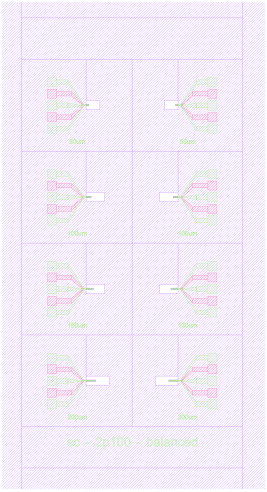

Figure 8: Chip design from mask in Figure 5

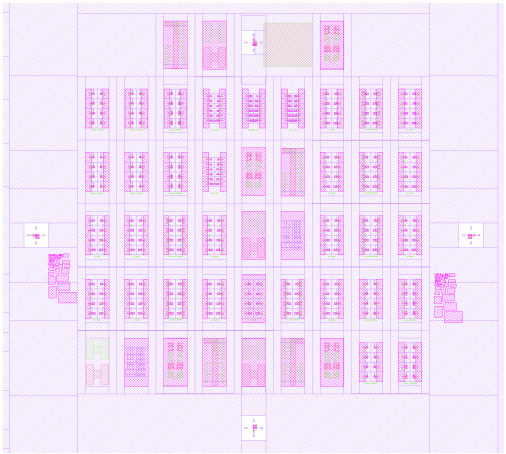

Figure 9: Mask design for encapsulation in pink layer

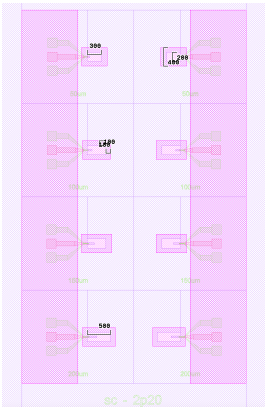

Figure 10: Encapsulation design from mask in Figure 7

5 Fabrication in Cleanroom

5.1 Choice of photoresist for photolithography

5.1.1 AZ 40XT

The first choice of potoresist was the AZ 40XT which is recommended for dry etching (depth up to 500+ μm), since we will be etching 525 μm. However, the resulting etch using this photoresist was chemically incompatible with the SPTS etching process, as seen in the resulting pictures in Figure 11 and Figure 12.

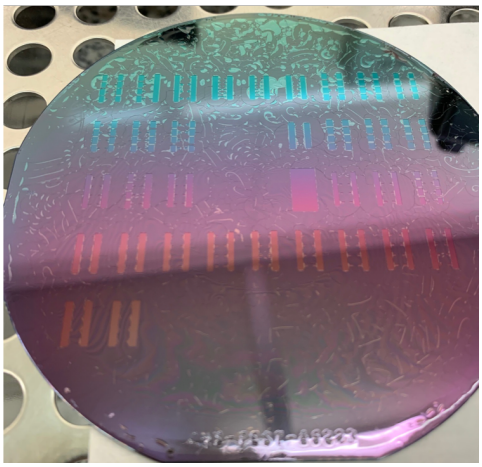

Figure 11: After 30" on SPTS APS with AZ 40XT

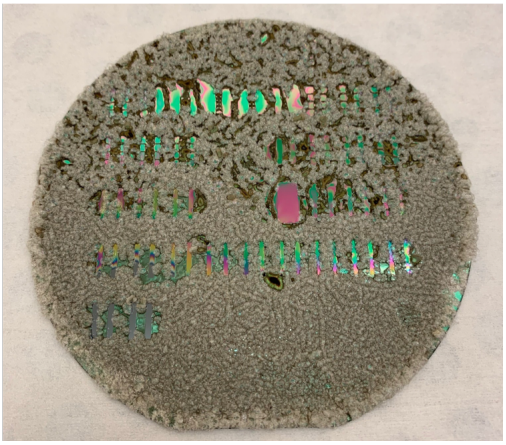

Figure 12: After 5' on SPTS APS with AZ 40XT

5.1.2 AZ 10XT-60

After this issue, the next photoresist used was AZ 10XT-60 which is the next one recommended for deep dry etching (depth < 200 μm). This photoresist was overstressed after the etching process at STPS, as seen in Figure 13. The issue could have been a layer too thick of photoresist or a hardbake at too hot temperature causing stress.

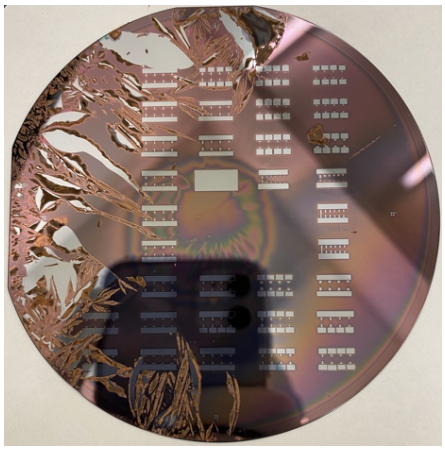

Figure 13: After 5' on SPTS APS with AZ 10XT-60 10μm

At this point the idea was to avoid the step of etching on SPTS and to make the substrate thinner to be able to use thinner potoresists, which could have been a problem earlier. In order to achieve this, a grinding is done on one side of the wafer to strip the SiO_2 and SiN_x layers and to reduce the overall thickness from 525 μm to 300 μm. The grinding on this side of the wafer will also be beneficial later for the adhesion of the polymer. The wafer states before and after the grinding process are illustrated in Figure 14.

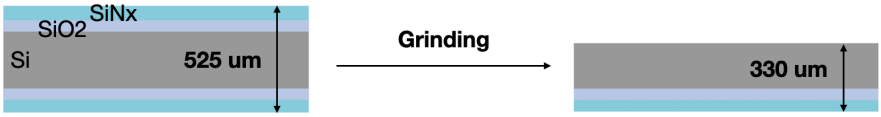

Figure 14: Wafer state before and after grinding

After the grinding, we are using the AZ 10XT-60, which showed better results, with a thinner layer of $5\mu m$ and decreasing the temperature of hardbake by 10°C. This time the next process is on AMS 200 (dry etching) instead of SPTS, since there is no more Si_2 nor SiN_x on this side of the wafer. In this way, the chances that it works properly are maximized because this photoresist is specially recommended for DRIE. The cavities from the photolithography are perfectly etched with sharp borders and the SiO_2 layer is attained. However, the photoresist has been consumed at the end of the process and the wafer's surface isn't flat anymore, as seen in Figure 15. This will be problematic for the bonding later. (An approximate difference of $80\mu m$ was measured under the microscope). This is why, for the next fabrication we will rather use a photoresist slightly thicker, such as $8\mu m$.

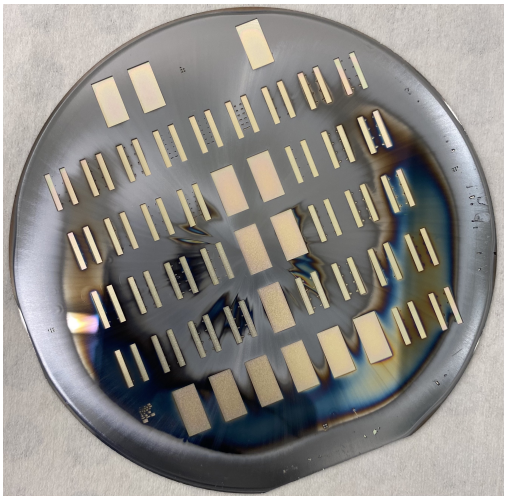

Figure 15: After 1h on AMS with AZ 10XT-60 $5\mu m$)

Figure 16: Same wafer, after PR strip and Al removal

Another successful result from this wafer is seen in Figure 16, after removing the Al layer on the backside, all the membranes have resisted the process and are seen in perfect state. This means that the membranes for encapsulation are strong because their surface is much smaller than the electrode pads which have all resisted.

The same process is done on another grinded wafer, but with a $8\mu m$ thickness for the photoresist layer. This time, the membrane seems to have more stress, since some of the bigger ones have broken. But the important result is that the ones needed for encapsulation are still present. This time the photoresist hasn't been consumed during the process, so the surface is as flat as at the beginning of the process. This is why, for the next fabrication processes we will use the same photoresist thickness. Finally, we have found a photoresist that works, the AZ 10XT-60, and its ideal thickness for the process, which is $8\mu m$. This wafer will be used for the next bonding step, shown in Figure 17.

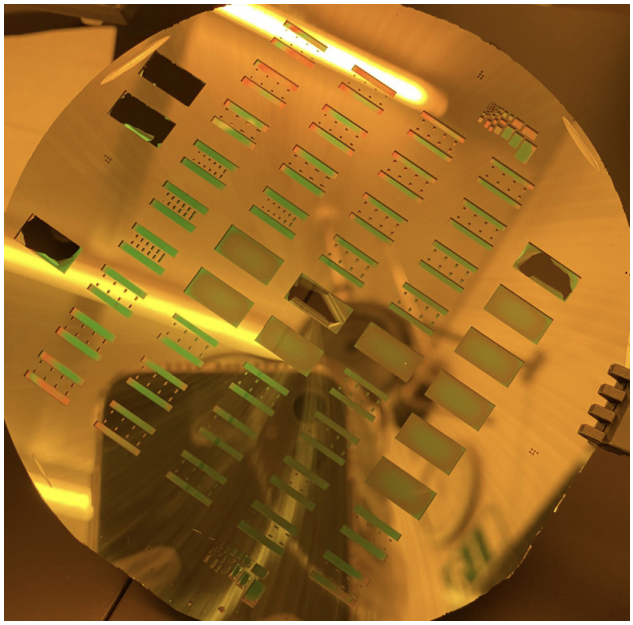

Figure 17: Wafer after etching and Al removal with AZ 10XT-60 ($8\mu m$)

5.2 Etching

5.2.1 Dry etching of SiO_2 and SiN_x

The process was incompatible with both of the photoresists used. This is why, finally, both layers where removed by grinding to simplify the process.

5.2.2 DRIE of Si

The etching of $330\mu m$ of Si is done with pulsed process (Bosch process) and pulsed LF wafer biasing, on the Alcatel AMS 200 machine. According to the etching rates of the process (3-4,5 $\mu m/min$), this process could take under the fastest mode (highest ratio etching/passivation in the pulsations): $\frac{330(\mu m)}{4.5(\mu m/min)} = 1h13min$. This value could vary depending on the design and other unpredictable parameters, this is why we should take out the wafer before to measure the etching rate. For this process the computed value ended up being almost exact to the total etching time spent: $1h20min$.

After the etching through the whole Si layer, we check under the microscope that the SiO_2 layer is reached. The SiO_2 layer is easily recognizable under microscope as seen in Figure 18. The Si borders appear sharp in Figure 19.

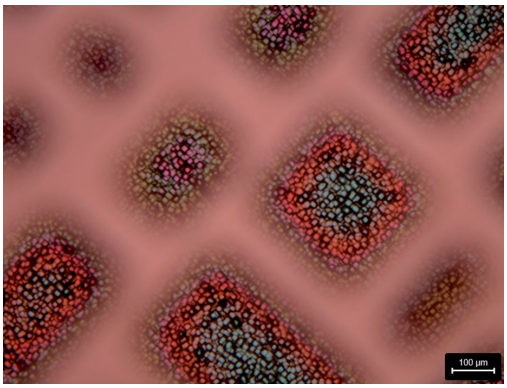

Figure 18: SiO_2 test membranes

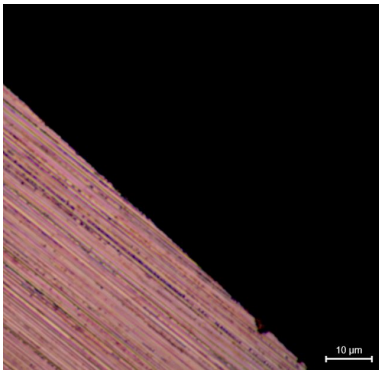

Figure 19: Same wafer, after PR strip and Al removal

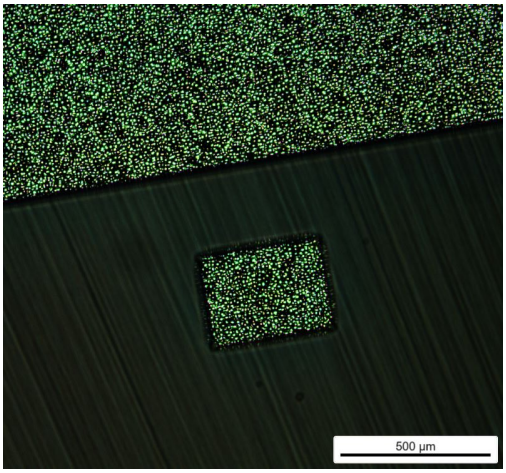

Figure 20: Encapsulation region

5.3 Bonding

5.3.1 Parylene Deposition

The wafer is coated with a Parylene layer of 10 μm on both sides. However, only one side should be coated for the process in the bonding machine. This is why, we removed one side under O2 plasma by covering the other side with a test wafer. While doing this, the wafer heated up and bonded to the test wafer. After this, we tried to remove the adhesion by leaving the wafers on a remover bath. For the next fabrication process, the Parylene deposition will be done only on one side by covering the other one with a dummy Si wafer to avoid this problem.

6 Conclusion

The goal of this project was to develop a reliable process flow for the encapsulation of resonators. An idea was envisioned with an initial proposal of process flow stated in section 3. In this part I was able to apply the knowledge from the courses in Microfabrication Technologies, which helped in finding the most suitable processes for the application. The initial envisioned process was standardized and seemed relatively simple at the beginning. However, the fabrication in cleanroom wasn't as straight-forward as I first thought. Because later during the fabrication process multiple complications were encountered (notably in the photoresist choice and in the dry etching step) as explained in section 5. Finally, each challenge encountered was overcome. An appropriate photoresist was found and the grinding solution further simplified the process. As a consequence the process flow has been modified and its updated version is in appendix.

In spite of the progress, the final goal wasn't reached due to the time constraint. This is because the beginning of the project was too slow because I had to learn to use all the machines. An achievement of the project is that what has been done in months can now be done in few days, thanks to the solutions encountered. Some remaining challenges are left to finish the last bonding steps. To avoid bonding to the dummy wafer, the wafer will be covered with a dummy wafer during the parylene deposition to cover only one side. The resulting state of the wafer from the final process flow was as expected: flat surface, resistant membrane, sharp borders and visible alignment marks. And since the final problem was that it bonded to another wafer unexpectedly, we can be optimistic about this process for the bonding in vacuum. If this bonding is successful, the next step will be the characterization of the vacuum encapsulations. The pressure inside the cavity should be measured in the long-term, to check the stability of the vacuum inside.

Overall, this project was a great opportunity to become more familiar with the fabrication in cleanroom.

7 References

Articles

[1] A.T. Ciftlik and M.A.M. Gijs. "Low Temperature Pyrex/Silicon wafer bonding via a single intermediate parylene layer". In: (2011). URL: https://infoscience.epfl.ch/record/163759?ln=en.

[2] A. De Pastina, D. Maillard, and L.G. Villanueva. "Fabrication of suspended microchannel resonators with integrated piezoelectric transduction". In: *Microelectronic Engineering* 192 (2018), pp. 83–87. ISSN: 0167-9317. DOI: https://doi.org/10.1016/j.mee.2018.02.011. URL: https://www.sciencedirect.com/science/article/pii/S0167931718300704.

[3] Steven J. Randolph et al. "A microfabrication process for a vacuum-encapsulated microchamber". In: *Microelectronic Engineering* 77.3 (2005), pp. 412–419. ISSN: 0167-9317. DOI: https://doi.org/10.1016/j.mee.2005.02.003. URL: https://www.sciencedirect.com/science/article/pii/S0167931705000298.

Lab : Advanced NEMS Laboratory
Operator Name : **CUESTA ERCORECA Sarah**
Supervisor Name : VILLANUEVA Luis Guillermo
Date of comitee :

Téléphone :
Office : -
E-mail : sarah.cuestaercoreca@epfl.ch

CMi EPFL Center of MicroNanoTechnology

PARYLENE-ASSISTED WAFER-BONDING FOR SUSPENDED MICROCHANNEL RESONATORS VACUUM ENCAPSULATION

Technologies used
Photolithography, Dry etching, Deep Reacting Ion Etching, PR strip, Bonding

Substrate Type
Silicon <100>, Ø100mm, 330 um thick, Single-side polished Layer: 200nm silicon dioxide, 700nm low-stress silicon nitride on one side

Ebeam litho data - Photolitho masks - Laser direct write data

Mask #	Critical Dimension	Critical Alignment
1	**10um**	2um

Process outline

Step	Process description	Cross-section after process
0	State of the wafer at the beginning of the process	
1	***Aluminium coating*** Machine: *EVA 760* Thickness: *2 µm*	
2	***Photolitography: coating*** Material: *AZ 10XT-60* Machine: *EVG 150* Thickness: *8 µm*	

Téléphone :
Office : -
E-mail : sarah.cuestaercoreca@epfl.ch

3	***Photolithography: Exposure*** Machine: *MLA 150*	
4	***Photolithography: Development*** Machine: *EVG 150*	
5	***Bake PR:*** Temperature : *85°C* Time: *overnight*	
6	***DRIE*** Machine: *AMS200* Process name : *SOI_accurate 4+* Temperature : *30°C*	
7	***PR strip*** Machine : *Tepla 300*	

Téléphone :
Office : -
E-mail : sarah.cuestaercoreca@epfl.ch

8	***Removal of Al layer*** Machine: Plade Metal Temperature: *35°C* Time: *10 min*	
9	***Parylene coating*** Material: *parylene-C* Machine: *Comelec C-30-S* Thickness: *10µm* *On one side covering the other one with a Si dummy wafer*	
10	***O2 plasma-treatment*** Power : *200 W* Time : *15s* Machine : *Tepla 300*	
11	***Bonding of the wafer to another one from a parallel process*** Machine: *Süss SB (+ BA6 for alignement)* Temperature : *280 C* Time : *40 min* Pressure : *vacuum with a tool pressure of 1000 mbar*