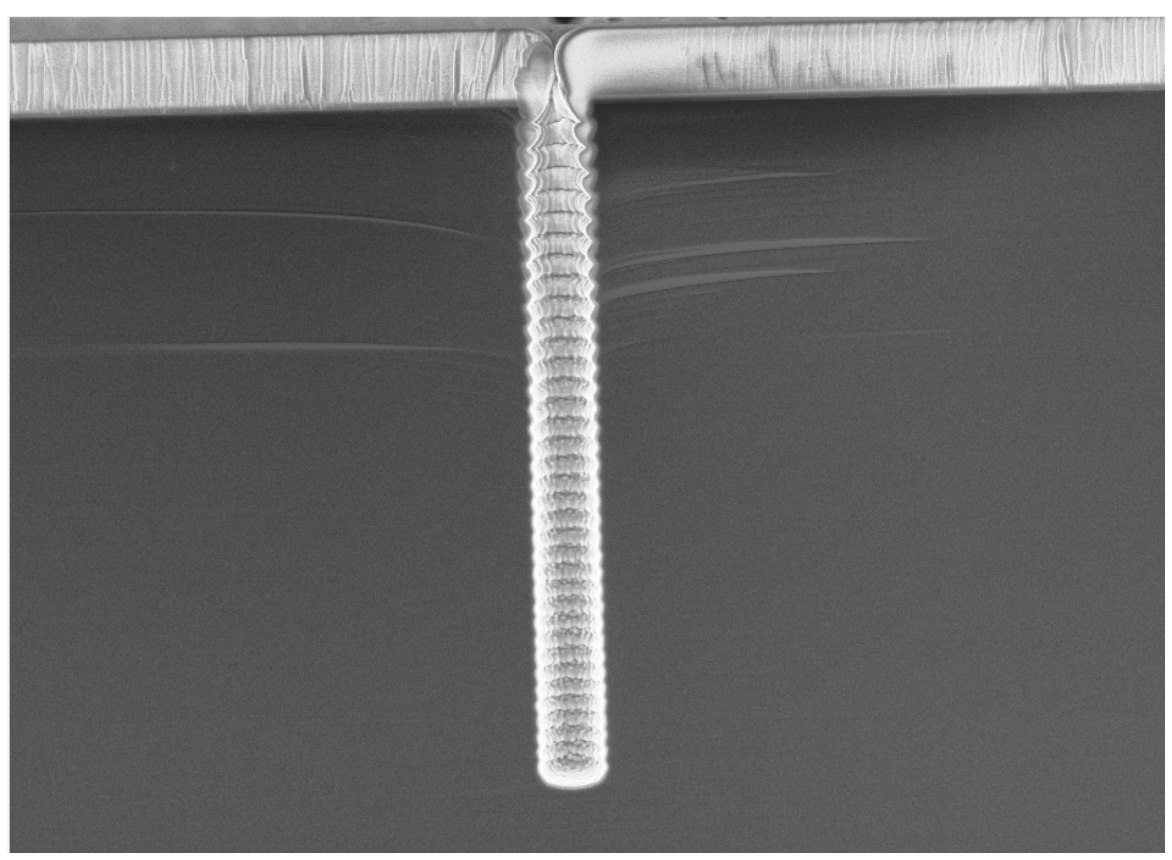
Silicon Oxide Walls

Author: Calamandrei Hugo



Supervisor: Seniz Küçük
Professor: Guillermo Villanueva

July 1, 2021

Contents

1 Introduction **2**

2 Machines used **2**
- 2.1 EVG 150 . . . 2
- 2.2 VPG 200 . . . 3
- 2.3 AMS 200 . . . 3
- 2.4 SPTS APS . . . 4

3 Preparation of the Wafers **5**

4 Deposition techniques **6**
- 4.1 LTO . . . 6
- 4.2 c-C4F8 plasma polymerization . . . 6
- 4.3 PECVD . . . 7
- 4.4 Parylene . . . 7

5 Results **7**
- 5.1 Surface roughness . . . 7
- 5.2 Obtained thickness before final etching . . . 8
- 5.3 Cross-section before final etching . . . 8
  - 5.3.1 LTO . . . 9
  - 5.3.2 $c - C_4F_8$ . . . 10
  - 5.3.3 PECVD . . . 11
  - 5.3.4 Parylene . . . 11
- 5.4 After final etching . . . 12
  - 5.4.1 LTO . . . 12
  - 5.4.2 $c - C_4F_8$ . . . 13
  - 5.4.3 PECVD . . . 13
  - 5.4.4 Parylene . . . 14

6 Conclusion **14**

A Microscope's photos before final etching **16**

B Process Flow **17**

1 Introduction

Nowadays almost all the mobile networks use the 4G and will eventually soon use the 5G. To use this technology, devices need lots of band filters. This is why the Advanced NEMS laboratory of the EPFL is developing a new kind of MEMS resonant device at 5GHz called "Lithium niobate bulk acoustic resonator"[1] [2] [3].

The goal of this project is to compare several techniques to create thin walls by several deposition methods into silicon layer in order to allow chain production of those resonators. Therefore four methods will be compared:

1. Low temperature oxidation (LTO)
2. $c - C_4F_8$ oxidation with AMS200
3. Plasma-enhanced chemical vapor deposition (PECVD)
4. Parylene deposition.

2 Machines used

In this section, the machines used during the project will be presented. Note that the machines used during the steps made by S. Küçük, by the CMi staff or the physics department will not be presented here. Those steps are made by other persons due to a lack of time to receive all the trainings needed to use these machines.

2.1 EVG 150

The EVG 150 is used to coat and to develop the wafers, and is available in the zone 6 of the CMi clean room under yellow light since it is in the photolithography zone. It is a modular cluster tool and it is equipped with 2 loading/unloading cassettes, one wafer centering station, one coater bowl, one developer bowl, a stack of 3 hotplates and a robot arm to feed all those individual processing stations. This EVG150 can be used to process standard silicon wafers or transparent substrates from 100mm to 150mm. For this project, standard silicon wafers of 100mm are used.

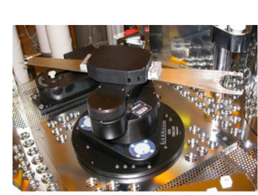
Figure 1: EVG 150 [5]

There are several recipes stored in the library for each photoresist:

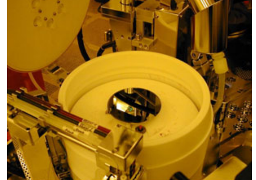
- Std = Silicon wafers without HMDS pre-treatment
- No_Dehydratation = Silicon wafers treated with HMDS in a Yes Oven
- Glass only = Skip wafer centering
- Quartz = wafer with low thermal conductivity

There are also two resins already fed in the machine :

1. Cybor 1 = AZ 1512 HS: general purpose resist. Thickness range from 1.1 to 2.0μm
2. Cybor 2 = AZ 10XT-60 thick resist. Thickness range 5.0 to 14μm (single coat)



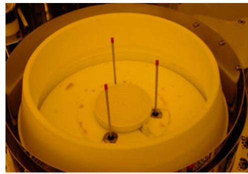
(a) EVG150 robot arm



(b) EVG150 coater bowl with dispense arm

(c) EVG 150 cold plate

(d) EVG 150 hot plates



(e) EVG 150 developer bowl

Figure 2: EVG 150 specific modules [5]

2.2 VPG 200

The VPG 200 (Volume Pattern Generator) used in the CMI clean room is developed by Heidelberg Instruments GmbH in Germany. It is a laser pattern generator used to create masks to use with mask aligners or to make direct exposure to writing on the resist. Three different lenses (4mm, 10mm and 20mm) are available in order to offer different specifications for writing speeds and magnification. The resolution can reach a minimum of 600nm, limited by the photoresist, the wavelength and the resolving power of the optics (NA, depth of focus).

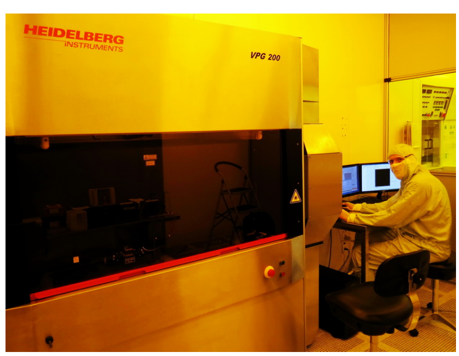


Figure 3: VPG 200 [6]

There are two different user levels of access on this machine, the Basic level used for this project offers wizardry like script editor which requires only two parameters:

1. The Laser Intensity (% of maximum available laser power): Controls the exposure dose. The dose is calibrated for standard mask sensitivity. Conversion factor to exposure dose are available for each optic.

2. Defocus: defines where the focus is done. If set to zero, focus is done at the top of the resist, a positive defocus will shift the focus downwards inside the resist.

A file conversion must be done before use. During this conversion, it is very important to be careful if a mirroring is needed or not. The figure 4 below shows an example of this mirroring : for the present the mirroring is not necessary since the direct writing method is used instead of a mask method.

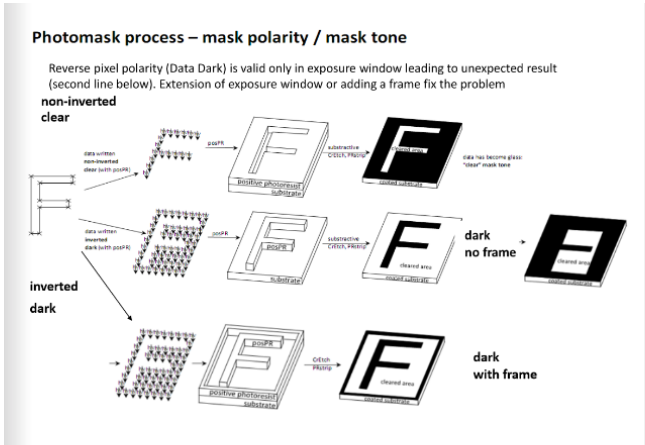


Figure 4: VPG 200 mirroring example [6]

2.3 AMS 200

Figure 5: AMS 200 [7]

The AMS 200 machine available in the CMi clean room is an Adixen AMS200 etcher. It is an optimized Deep Reactive Ion Etching (DRIE) system for Silicon (Si) and Silicon on Insulator (SOI) wafers. The machine used has the following special hardware arrangements to make that possible:

- A high density plasma source : Inductive Coupled Plasma (ICP)
- A temperature controlled process chamber
- An Electrostatic Clamping Chuck (ESC) controlled in temperature for wafer cooling
- Two possible wafer voltage biasings : RF (13.56MHz) for dielectric etching and pulsed Low Frequency (LF) for Si etching
- A powerful gas process pumping arrangement (Adixen 1600l/s Turbo pump + Adixen ADP122 rough pump).

There are three main families of process used in this machine.

1. Si etching with pulsed process (Bosch process) and pulsed LF wafer biasing,
2. Si etching with none pulsed process (continuous process)
3. Dielectric etch with RF wafer biasing

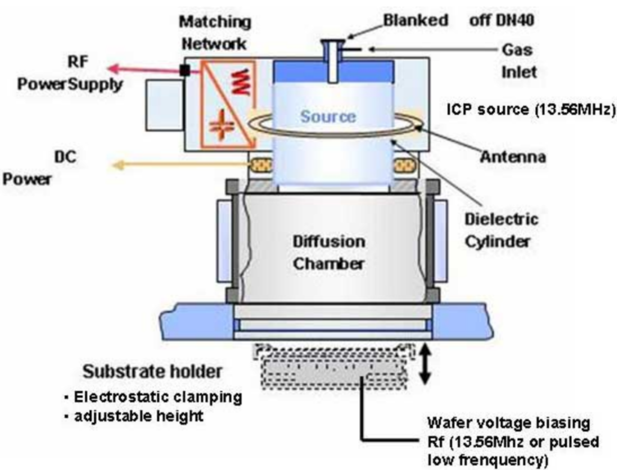


Figure 6: AMS Processing chamber [7]

2.4 SPTS APS

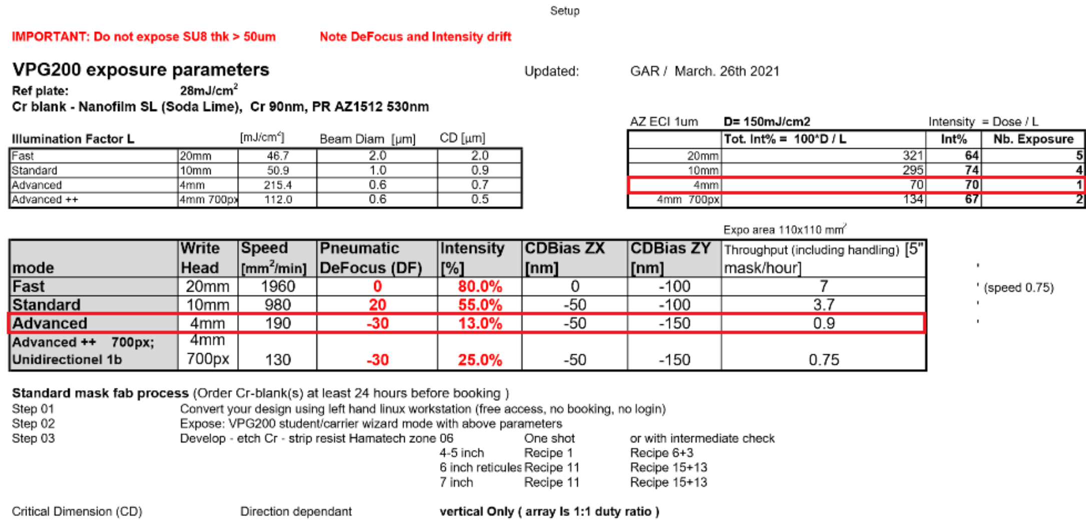
The SPTS avanced plasma system (APS) module is optimized for etching dielectrics (e.g. SiO_2, Si_xN_y, SiC, Al_2O_3, glass types...). Those materials are usually difficult to etch with conventional etching methods. To pass trough some difficulties, it uses ICP-based high density plasma source.
There are the following features on this machine:

- High density plasma source
- Wafer voltage biasing independent from the ICP
- Electrostatic clamping => no EBR required
- Powerful gas process pumping arrangement
- Loadlock/chamber transfers for single wafer processing
- Control software offering fully automated processes
- End-point detection system (optical spectroscopy)

Figure 7: SPTS [8]

3 Preparation of the Wafers

Before making the deposition with the different methods, the four wafers have to be prepared as shown in the process flow in appendix. The wafers used for this project, as said before, are standard silicon wafers of 100mm diameter.
Since the thickness needed is as thick as possible, the coating was made with an AZ1512 resin and a thickness of 1.1 μm with the EVG 150. Before that, a 25 minute dehydration in a 70°C oven is needed. The recipe used for the coating is "*C4_1512_1.1_EC*". It is already in option in the EVG 150 in zone 6 of the CMI clean room.



Setup

IMPORTANT: Do not expose SU8 thk > 50um   Note DeFocus and Intensity drift

VPG200 exposure parameters   Updated: GAR / March. 26th 2021

Ref plate: 28mJ/cm²
Cr blank - Nanofilm SL (Soda Lime), Cr 90nm, PR AZ1512 530nm

Illumination Factor L		[mJ/cm²]	Beam Diam [µm]	CD [µm]
Fast	20mm	46.7	2.0	2.0
Standard	10mm	50.9	1.0	0.9
Advanced	4mm	215.4	0.6	0.7
Advanced ++	4mm 700px	112.0	0.6	0.5

AZ ECI 1um   D= 150mJ/cm2   Intensity = Dose / L

	Tot. Int% = 100*D / L	Int%	Nb. Exposure
20mm	321	64	5
10mm	295	74	4
4mm	70	70	1
4mm 700px	134	67	2

Expo area 110x110 mm²

mode	Write Head	Speed [mm²/min]	Pneumatic DeFocus (DF)	Intensity [%]	CDBias ZX [nm]	CDBias ZY [nm]	Throughput (including handling) [5" mask/hour]
Fast	20mm	1960	0	80.0%	0	-100	7
Standard	10mm	980	20	55.0%	-50	-100	3.7
Advanced	4mm	190	-30	13.0%	-50	-150	0.9
Advanced ++ 700px; Unidirectionel 1b	4mm 700px	130	-30	25.0%	-50	-150	0.75

' (speed 0.75)

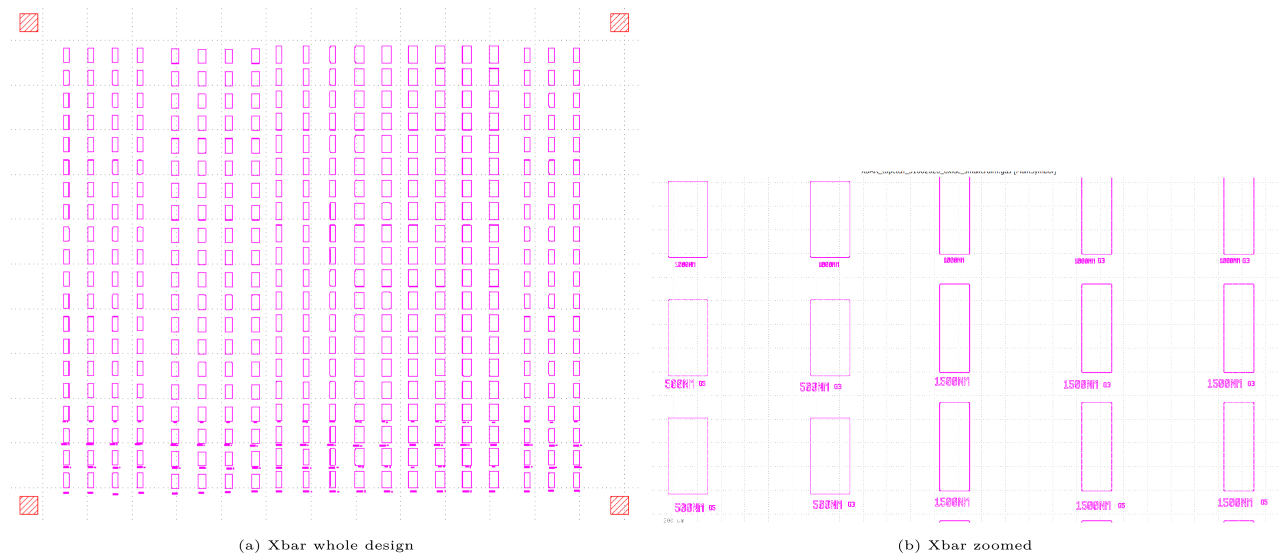
Standard mask fab process (Order Cr-blank(s) at least 24 hours before booking)
Step 01 Convert your design using left hand linux workstation (free access, no booking, no login)
Step 02 Expose: VPG200 student/carrier wizard mode with above parameters
Step 03 Develop - etch Cr - strip resist Hamatech zone 06

	One shot	or with intermediate check
4-5 inch	Recipe 1	Recipe 6+3
6 inch reticules	Recipe 11	Recipe 15+13
7 inch	Recipe 11	Recipe 15+13

Critical Dimension (CD)   Direction dependant   **vertical Only (array Is 1:1 duty ratio)**

Figure 8: VPG 200 Exposure dose [6]

The second step is the laser writing on the photoresist. This one is done with the VPG200. Since the smallest design is about 0.5 μm, the 4mm head writing was use. The writing was made with a 80% power of the laser, 15% more than recommended. Like shown in the figure 8 the recommended power for a 4mm lens is at 70%, the pneumatic DeFocus was set to -30DF and the speed at 190 mm^2/min , the design for the writing is shown in the figure 9. The four red square on the figure 9a are here to have a visual on the wafer without microscope but for the final results they were not engraved. On the figure 9b, it can be seen that some of rectangles of the design are labeled as a function of their thickness, so 500, 1000 and 1500 nm, the final desired results are 1500, 2000 and 2500 nm but since the laser, during the writing step, generally burn more than desired this choice was made during the design creation by S. Küçük. In the AMS 200 machine, it is possible to put many times a design, this was done for this project, where the Xbar design was written 16 × on each wafers (4 × 4).



(a) Xbar whole design   (b) Xbar zoomed

Figure 9: Xbar design

The development is done again with the EVG 150 with the following recipe "*D4_HB_1512_1u1_PVD*", again

this recipe is available in the EVG 150 and afterward a cleaning on a wet bench is necessary, 5 minutes in two benches with different ultrasound frequencies.
The final step is the plasma etching to engrave on the silicon. This is done with the AMS200 and the recipe used is "*SOI_accurate++*". Afterwards, the residual photoresist is remove with the UFT Remover Wet bench, with 5 minutes in each removal liquid and finally 5 minutes in both water baths to rinse it.
Now the four wafers are ready for the oxidation step, this step will be done with four different methods. The first method is the Low temperature oxidation or LTO, this is done by the CMi staff. The second deposition is made with $c - C_4F_8$ and done with the AMS200 with the method explain in [4]. The third method is the PECVD done by the Physics department clean room. And finally, the last method is done with Parylene polymer, again done by the CMi staff. These four methods will be explain in the following sections. Since the final etching is different for the four method, it will be explain in the corresponding section.

4 Deposition techniques

4.1 LTO

The Low temperature oxidation is a method of deposition of SiO_2, it is a reaction occurring at low temperature between a solid and a gas, usually between oxygen and a metal, here with silicium. First an RCA cleaning is done by the CMI staff before they made the LTO deposition in the tube 3-1 of Centrotherm furnaces presented in figure 10, it is a Low Pressure Chemical Vapor Deposition (LPCVD), the thickness asked was of 2μm, since the available thickness are between 50Å and 3μm, this is in the range. They made a deposition of SiO_2 by using silane (SiH_4) and O_2 at 425°C. The final etching is made with the SPTS APS, with 2μm to etch. Since the final etching is done after the measurements of the cross-section, meaning the original wafer with LTO has been broken in the aim to have photos with SEM of the cross-section, a piece of the wafer is glued on a new wafer in purpose to make the final etching. The recipe used is $SiO_2_PR_2:1$, this recipe is done at 10°C for a duration of 5 minutes.

Figure 10: 3-1 tube for the LTO deposition [9]

4.2 c-C4F8 plasma polymerization

The plasma polymerization of the octafluorocyclobutane ($c - C_4F_8$) is shown in the PDM of L. Frehner [4]. In his project, L. Frehner uses the C_4F_8 as a protection for the sidewall during the etching of a trench, by doing a deep reactive ion etching process (DRIE), shown in figure 11. Here, since the trenches are already done, the C_4F_8 is only used to make a deposition in those trenches to create the desired "walls". This deposition is made with the AMS 200 and the recipe used is the 8761 C called P1 in the PDM, the parameters use for this recipe are presented in the table 1 below. The recipe used is already present on the AMS, it is called "*LF_passivation2*".

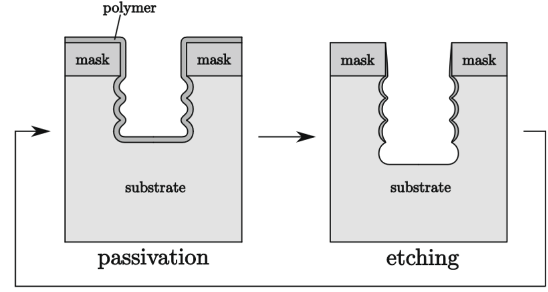


Figure 11: Scheme of the Deep Reactive Ion Etching. [4]

Table 1: AMS parameters of the recipe P1

Parameters	Units	Recipe P1
Source Power	[W]	2000
Pressure	[mbar]	0.1
Chuck bias RF	[W]	20
C_4F_8 Flow	[scm]	100
CH_4	[scm]	60
Substrate temperature	[°C]	20
Time	[min]	2.5

Seeing the Figures 20 and 22 presented in section 5.3.2, in the AMS wafer, the deposition is peeled off of the wafer during breaking to pass through the SEM, so the final etching was not been done during this project. But

in his PDM, L. Frehener recommends an Argon milling method done with the AMS200 to etch the $c - C_4F_8$. In the rest of this report, this wafer will sometimes be referred as AMS wafer.

4.3 PECVD

The Plasma-enhanced chemical vapor deposition (PECVD) is made by a lab in the physics department, with the Oxford plasmalab system 100. PECVD is a chemical vapor deposition method using plasma to deposit a thin film from a gas state to a solid state on a substrate. The Figure 12 shows an example of a PECVD deposition. The PECVD deposition thickness done by the physics cleanroom staff is about 1.6μm. The final etching for PECVD is as for the LTO made with the SPTS machine. The recipe used is the same as for LTO so $SiO_2_PR_2:1$, also done with a temperature of 10°C but since the thickness here is about 1.6μm and not the 2μm as for LTO, the time, here, is set for 4 minutes.

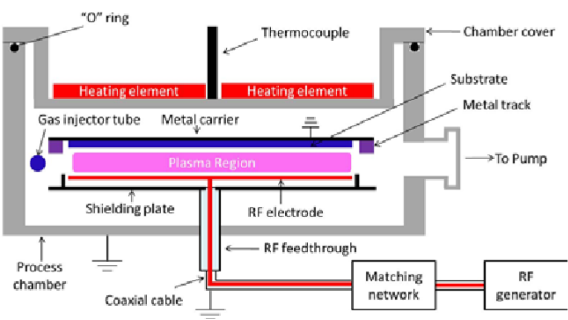


Figure 12: PECVD schema [11]

4.4 Parylene

The parylene is a polymer film which has a really good grip on the wafer. The parylene formula is C_8H_8, the molecules will attach themselves together. This capability is really useful since the parylene deposition will glue to the exact shape of the surface. The parylene deposition is made with a Comelec C-30-S, there is no training available for this machine in the CMI at the EPFL, but there is batch service on request every week. The principle of deposition is simple, first the solid dimmer is heated to 150°C to change to a vapor phase, then it diffuses to a Pyrolysis chamber at 670°C to be dissociated into monomers, those monomers diffuse into the deposition chamber, around 80°C where the wafer is waiting and it condensates into parylene layers.

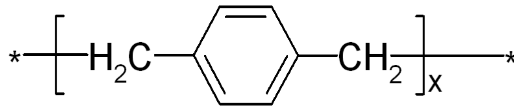


Figure 13: Parylene molecule [12]

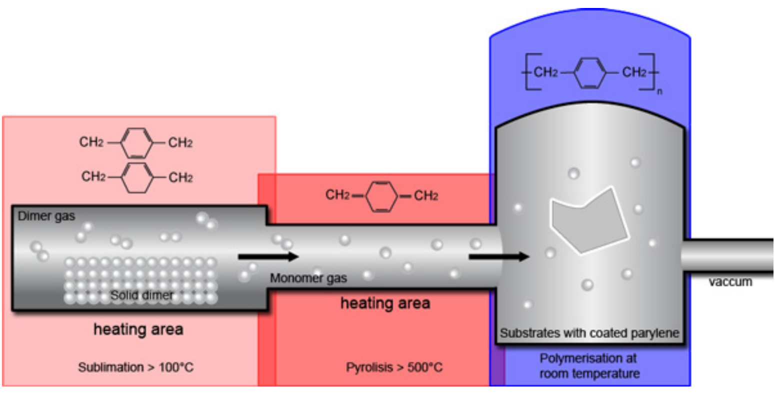


Figure 14: Parylene coating tool [13]

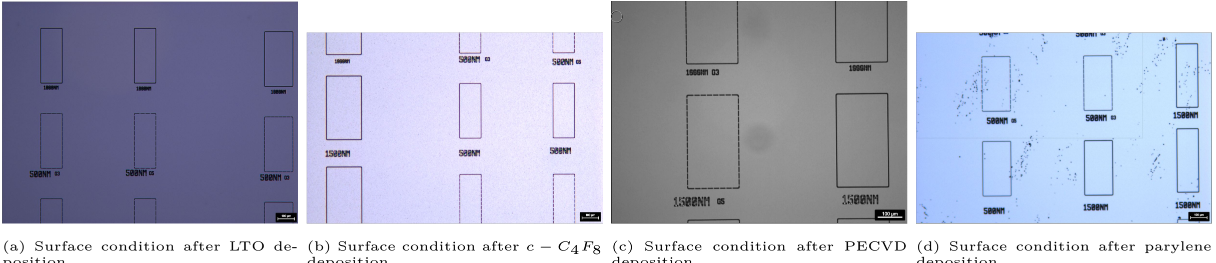
Here, the system works under a primary vacuum (few μbar), for this deposition a thickness of 2μm is made, to that 7.0g of parylene were loaded for a 100mm wafer. The run was made with an overnight degassing in the deposition machine, this is not necessary for this project, but an other user ask for it for the same run, the wafer is just under vacuum for a longer time than usual.
The final etching for the parylene deposition is a dry etching made with STS by S. Küzük.

5 Results

5.1 Surface roughness

In the following figures, the surface of the different wafers after deposition can be seen. In the figure 15d some points are present on the surface of the wafer, those points have an unidentified origin, but since a final etching will be done, they will not cause any problems. The following photos with PECVD are taken with a different

microscope than the others ones since they were taken an other day, this explain the change of the colors and zoom size.



(a) Surface condition after LTO deposition (b) Surface condition after $c - C_4F_8$ deposition (c) Surface condition after PECVD deposition (d) Surface condition after parylene deposition

Figure 15: Surface roughness before final etching

5.2 Obtained thickness before final etching

The results presented here are measured before the final etching (step 08 in the process flow), the photolithography writing was done on two different days since there were some problems with the VPG200 machine on the first day of writing and there was not any time to make all four wafers in one session, but the settings were the same for all wafers. The photos from which the results of the Table 2 are taken can be seen in the Appendix A.

Table 2: Summarizing of the obtained thickness after deposition but before the final etching, the 500, 1000 and 1500nm are the thickness presented in the Figure 9

Thickness designed	500nm	1000nm	1500nm
LTO	2.21 μm	2.69 μm	2.86 μm
$c - C_4F_8$	2.58 μm	2.78 μm	3.53 μm
PECVD	2.32 μm	2.68 μm	2.90 μm
Parylene	2.72 μm	2.85 μm	3.26 μm

The results shown before are to be taken with a grain of salt since the thickness of the trench depends on where the measurement was done. The following Figure 16 show different locations in the same wafer after PECVD deposition for two measurement of a 1500 nm thickness. In Figure 16a, the thickness of the "wall" is about 2.90 μm and in the Figure 16b this thickness is about 3.60 μm. Those differences can come from the laser writing made with the VPG 200 or some visual errors in the measurement method. These measures are made with on optical microscope, so if the settings are not perfect, the picture can still be a little blurred, which is not evident to detect at that scale and make it hard to measure the real thickness of the holes.

(a) 1500nm thickness with PECVD deposition in the G3 design (b) 1500nm thickness with PECVD deposition in the G5 design

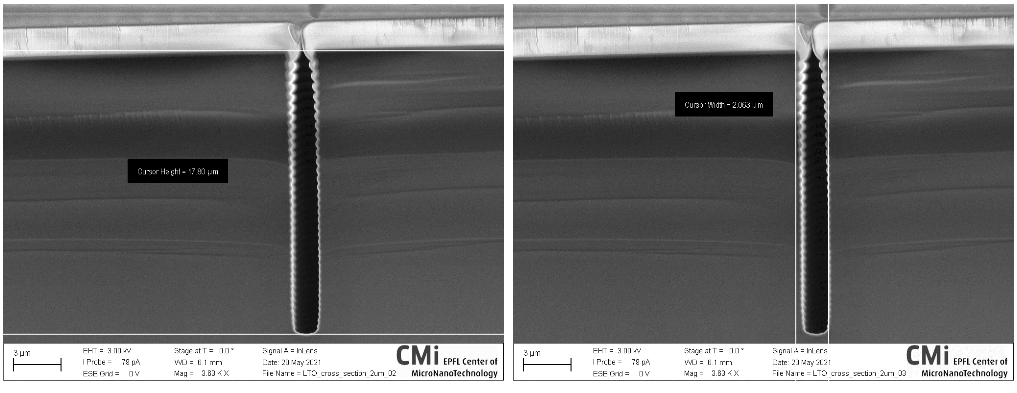
Figure 16: Comparison of two measurement for a 1500nm writing on a wafer after PECVD deposition at two different location

5.3 Cross-section before final etching

Here are the photos of the wafer's cross section, to be able to see those cross-sections, all wafers have been cut into small pieces and go through a SEM Zeiss Merlin, present in the zone 15 of the CMi cleanroom. Since, only the cross section of the wafers are visible though the SEM, it is impossible to see which initial thickness (500nm, 1000nm, 1500nm), we are currently seeing, some supposition will be done with the length of the hole, but it can be wrong. The deposits are easily seen through the SEM, since there are insulator, who charge themselves with electrons and shine in the images.

5.3.1 LTO

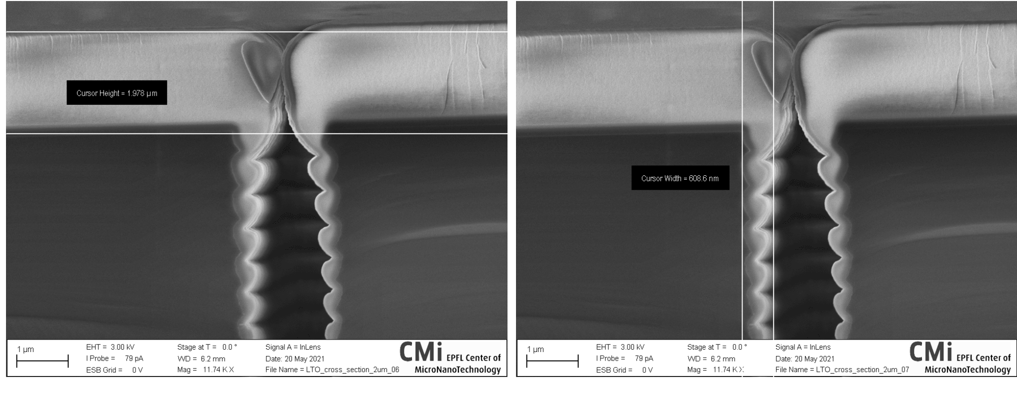
The Figure 17 below, shows the cross section of the LTO wafer, the first thing to remark is the depth of the hole shown in Figure 17a, all the trenches made in the step 03 of the process flow presented in appendix B are between 17μm and 21μm. In the Figure 17b, it can be seen that the width of the hole is about 2μm, by comparing with the Table 2, it is certainly a 500nm designed hole. The second thing to remark here, is the top of the trench being blocked by the deposition. By zooming on the top of the trench, it can be seen on the Figure 18a that indeed the deposition blocked the topside of the hole, but the thickness measured here is about 1.98μm which is really close to the thickness of 2μm asked in 4.1. The maximum thickness of the wall, in the upside of the trench is about 608nm, we can see that this wall make some waves, certainly due to the etching process. The Figure 19 shows a zoom of the trench's bottom, it can be seen that although the topside of the trench is blocked by the deposition, there is still a 120nm thick film of silicon dioxide which was deposited on the bottom.



(a) Height of the hole=17.80μm

(b) Width of the hole=2.063μm

Figure 17: Cross section of the LTO wafer, before final etching



(a) Zoom on the top of the trench, height of the deposition=1.978μm

(b) Zoom on the top of the trench, width of the wall=608nm

Figure 18: Cross section of the LTO, before final etching

Figure 19: Cross section of the LTO wafer through a SEM, zoom on the bottom of the trench, height of the deposition=119nm, before final etching

5.3.2 $c - C_4F_8$

For the AMS deposition presented in Figure 20, the main difference with the LTO's one presented before, is that the topside of the trench is not blocked by the deposition, this is due to the fact that the topside of the trench was peeled off during the breaking of the wafer. A second visible difference is the "waves" of the wall, in the Figure 22, this is not at all a wave form but more like smalls packs of deposition doing like rollers all around the edge of the trench. In the same Figure, the bottom of the hole can be seen and thanks to the trench's topside being not blocked the deposition here is thicker than the one on the LTO's hole, 238nm for AMS and 119nm for LTO, which is $2\times more$.

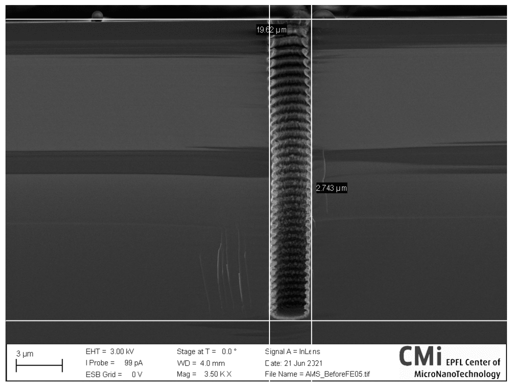
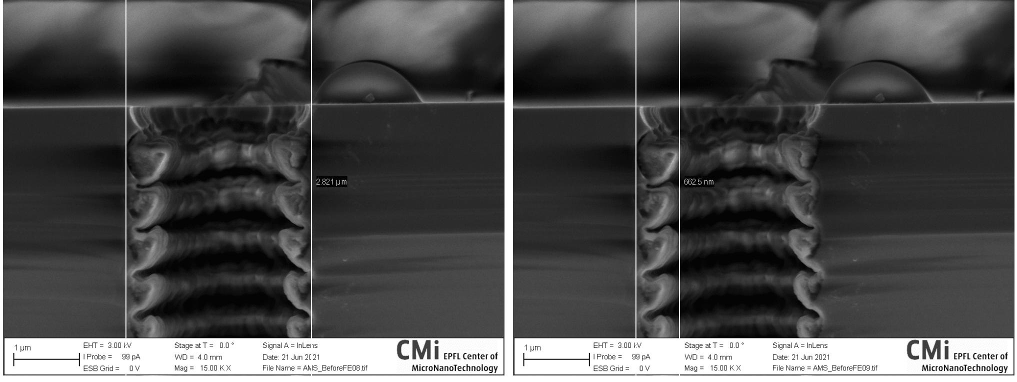


Figure 20: Cross section of the AMS wafer through a SEM, width of the hole=2.743μm, height of the hole=19.62μm, before final etching



(a) Zoom on the top of the trench, width of the hole=2.821μm (b) Zoom on the top of the trench, width of the wall=662nm

Figure 21: Cross section of the AMS wafer through SEM, before final etching

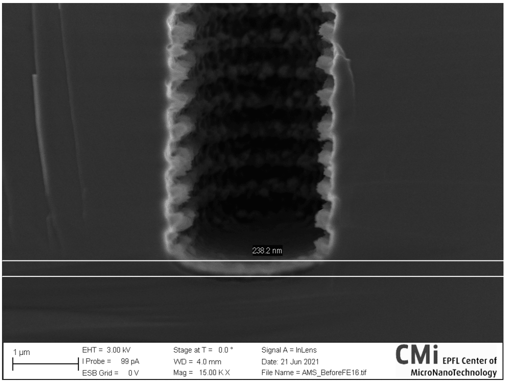


Figure 22: Cross section of the AMS wafer through a SEM, zoom on the bottom of the trench, height of the deposition=238nm, before final etching

5.3.3 PECVD

For the PECVD deposition, it can be seen in Figure 23, that the depth of the trench is about 20.19μm, which make one of the deepest trenches, in the Figure 24, that the deposition in the top of the wafer is about 1.556μm and the hole is still open in contrary to the LTO's one where the hole was blocked at the end. The thickness asked to the Physics clean room staff is of 1.6μm, so the 1.556μm is quite close. In the Figure 25, we can see the bottom of the trench where there is a deposition of about 74nm. This is the thickest deposition height in the bottom of the trenches. This can be for several reasons, first, the deposition made is one of the thicker ones too. The second reason can be that this trench is also one of the deepest, as said before.

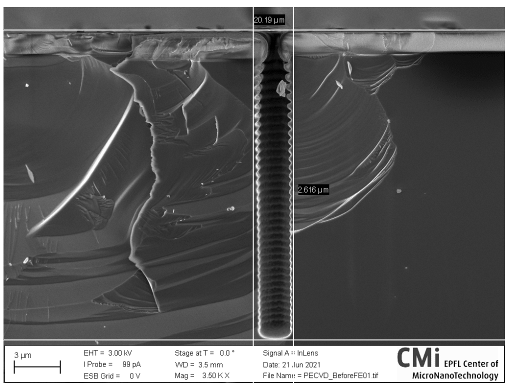


Figure 23: Cross section of the PECVD wafer through a SEM, depth of the trench=20.19μm and width of the hole=2.616μm, before final etching

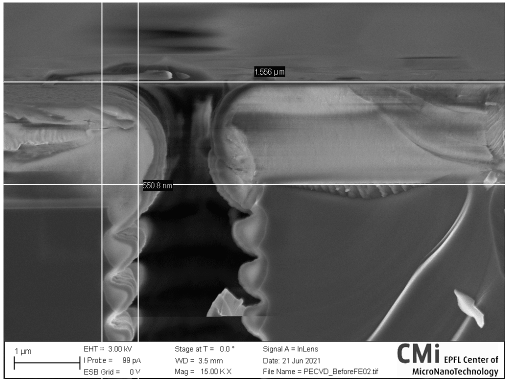


Figure 24: Cross section of the PECVD wafer through a SEM, zoom on the top of the trench, height of the deposition=1.556μm, width of the wall=551nm, before final etching

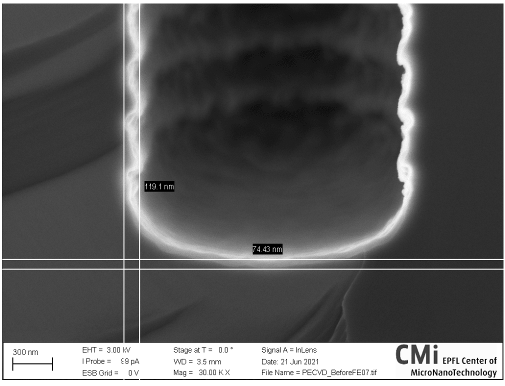


Figure 25: Cross section of the PECVD wafer through a SEM, zoom on the bottom of the trench, height of the deposition=74nm, before final etching

5.3.4 Parylene

The wafer with parylene deposition is impossible to see before the final etching. When the wafer is cut to be prepare for the SEM, the parylene film on the top overlapped on the cross section of the wafer, which make impossible to see anything.

5.4 After final etching

In the following section, the images after the different final etching techniques will be presented. Like said before those images are taken through the SEM Merlin in the zone 15 of the CMi cleanroom.

5.4.1 LTO

Here are the images of the LTO's wafer after the final etching done with the SPTS. Through the Figures 26 and 27, we can see that the top side of the wafer has been etched, and that the trench which was totally blocked before is now open, although there is still a very thin layer of silicon dioxide on the top of the wafer, visible thanks to the shininess of the SiO_2. During the etching, the SPTS machine showed that the silicon was reached, but maybe there was some errors due to the thickness of this layer and some additional seconds would be necessary to totally etched the silicon dioxide on the top of the wafer. In the Figure 28, we can remark that the silicon dioxide which was deposited in the bottom of the trench is still here, so the SPTS etching does not reach the bottom and the structure in the trench is untouched.

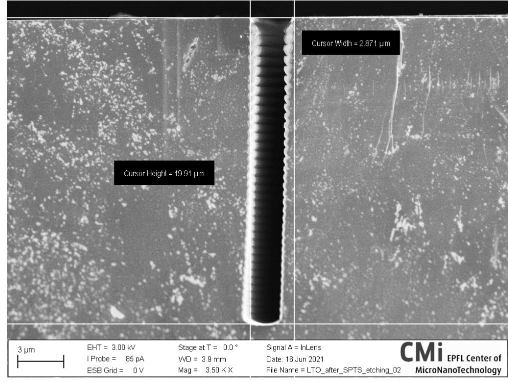


Figure 26: Cross section of the LTO wafer through a SEM, width of the hole=2.871μm and depth of the trench=19.91μm after final etching

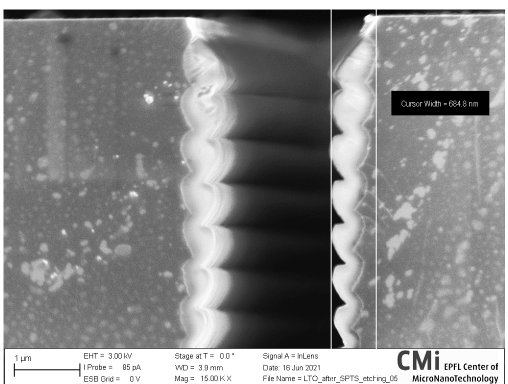


Figure 27: Cross section of the LTO wafer through a SEM, zoom on the top of the trench, width of the wall=684nm after final etching

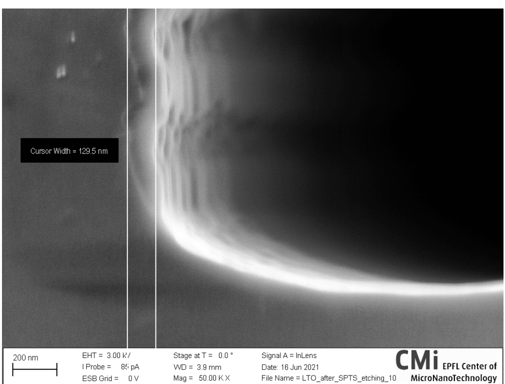


Figure 28: Cross section of the LTO wafer through a SEM, zoom on the bottom of the trench, width of the wall=129nm after final etching

5.4.2 $c - C_4F_8$

Like said before, the final etching was not done with the AMS wafer, since the topside of the deposition was totally peeled off during the breaking of the wafer for the SEM. Due to a lack of time and of need to re-fabricate this wafer, the final etching will not be analysed here.

5.4.3 PECVD

In this section all file names were written incorrectly during the SEM imaging session, it is stated as LTO_after_spts_etching_XX but it is indeed the PECVD wafer. Like for the LTO's one, the PECVD wafer reacted well to the SPTS etching. through the Figures 29 and 30, we can see that the top of the wafer is been etched, but like for the LTO's wafer a layer of deposition is still present on the top of the wafer. Here this layer is even thicker than for the LTO. Like during the etching of the LTO, the SPTS shows when the silicon is reached, but some extra seconds would have been necessary to avoid the error and totally etched the deposition. With the Figure 31, we can see that there is still some deposit on the bottom of the trench. We can also remark that for this trench, the wall and the bottom form an angle and not a smooth curve, this can be due to the etching done with the AMS200 during the step 03 of the Process flow or a particularity of the PECVD deposition. But since on the Figure 25 of the PECVD before the final etching, a smooth line is clearly visible, this particularity came surely of the fabrication of the trench.

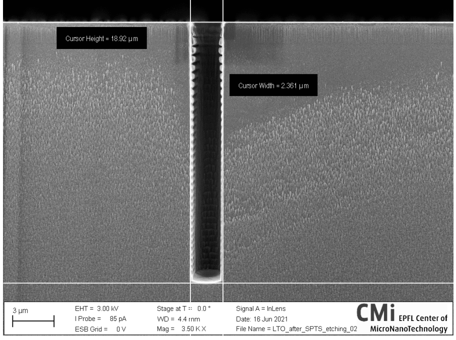


Figure 29: Cross section of the PECVD wafer through a SEM, depth of the trench=18.92μm and width of the hole=2.361μm, after final etching

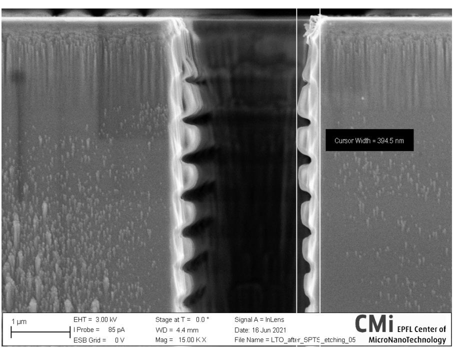


Figure 30: Cross section of the PECVD wafer through a SEM, zoom on the top of the trench, width of the wall=394nm after final etching

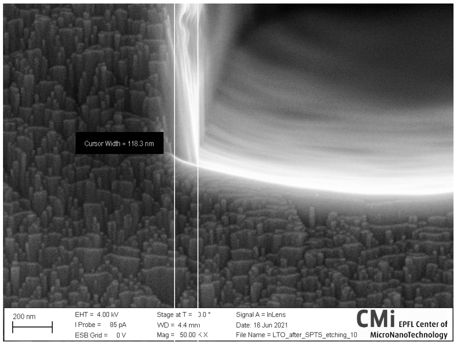
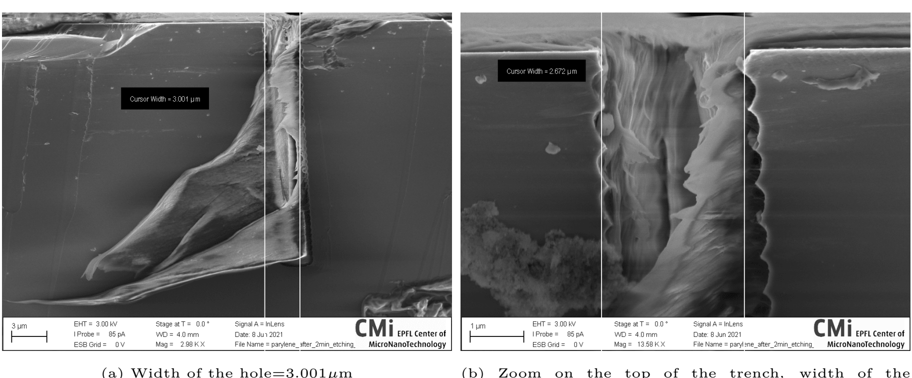


Figure 31: Cross section of the PECVD wafer through a SEM, zoom on the bottom of the trench, width of the wall=118nm after final etching

5.4.4 Parylene

For the parylene wafer wafer after the STS etching, we clearly can see that the parylene deposition was snatched off of the silicon surface. Certainly due to the break of the wafer to pass it though the SEM. But this shows that the parylene creates a solid film which is tough but which do not stick to the silicon surface. This can be seen on the Figure 32b, where the surface of the hole is clearly visible without parylene on it and the parylene film is totally removed.



(a) Width of the hole=3.001μm

(b) Zoom on the top of the trench, width of the hole=2.672

Figure 32: Cross section of the Parylene wafer through a SEM, after final etching

6 Conclusion

Finally, after going through the four deposition techniques, we have compared the differences and the similarities between those techniques. It is really hard to tell which one will be preferable for the usage in the "Lithium niobate bulk acoustic resonator", the LTO deposition method seems promising but since the width of the wall is only around 130nm in the bottom of the trench and this one is totally blocked, it will be complicated if those 130nm are not enough. The AMS deposition has a thicker deposition on the bottom of the trench (around 2 $\times$ the one in the LTO), but since the C_4F_8 peeled of during the breaking for the SEM, we can not say if the trenches are blocked or not with this method. The coating on the walls are also, non very conformal. And, since the final etching was not done during this project, a technique must be found and tested. As stated, an Argon milling method done with the AMS200 is recommend by L. Frehner in his PDM this was not done here due to the wafer having already been peeled off after the breaking for the SEM before the final etching. The PECVD method has the thinnest deposition on the bottom, but since only 1.6μm was deposit on the top and the trench was not blocked maybe by doing a thicker deposition on the top, there will be more deposit on the bottom, a thicker deposition can be tried. Finally, for the parylene deposition, since during the SEM it was impossible to see something, it is complicated to say much about this method. Maybe the resistance of the parylene could be used, but it must be done by knowing that the parylene will prefer to detach from the wall than to break and it will not be possible to analyse correctly the cross-section of a parylene deposition without breaking the wafer. I will conclude with a personal aspect, I never walked into a clean room before this project, all the techniques used were totally new to me. I enjoyed a lot discovering all those techniques. Through last semester class of Pr. Villanueva "Micro/nanomechanical device", I have gotten a brief theoretical introduction of the processes used to fabricate devices in the micro/nano scale but it mostly interested me how those methods are implemented practically. This project offered me a chance to use those methods and I really enjoyed it.

References

[1] "5 GHz laterally-excited bulk-wave resonators (XBARs) based on thin platelets of lithium niobate" V. Plessky, S. Yandrapalli, P.J. Turner, L.G. Villanueva, J. Koskela and R.B. Hammond, January 2019

[2] "5GHz Band n79 wideband microacoustic filter using thin Lithium Niobate membran" P.J. Turner, B. Garcia, V. Yantchev, G. Dyer, S. Yandrapalli, L. G. Villanueva, R.B. Hammond, and V. Plessky, May 2019

[3] "FABRICATION OF LITHIUM NIOBATE BULK ACOUSTIC RESONATOR FOR 5G FILTERS" Muhammad Faizan, Annalisa De Pastina1, Soumya Yandrapalli, Patrick J. Turner, Robert B. Hammond, Victor Plessky and Luis Guillermo Villanueva, June 2019

[4] "Buried microchannels for thermal management of silicon detectors", Lenaic Frehner, PDM, March 2020 pp. 33-36

[5] "https://www.epfl.ch/research/facilities/cmi/equipment/photolithography/evg-150-automatic-resist-processing-cluster/" ,CMI, EPFL

[6] "https://www.epfl.ch/research/facilities/cmi/equipment/photolithography/heidelberg-instruments-vpg200/", CMI, EPFL

[7] "https://www.epfl.ch/research/facilities/cmi/equipment/etching/ams200/", CMI, EPFL

[8] "https://www.epfl.ch/research/facilities/cmi/equipment/etching/spts-aps/", CMI, EPFL

[9] "https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/centrotherm-furnaces/", CMI, EPFL

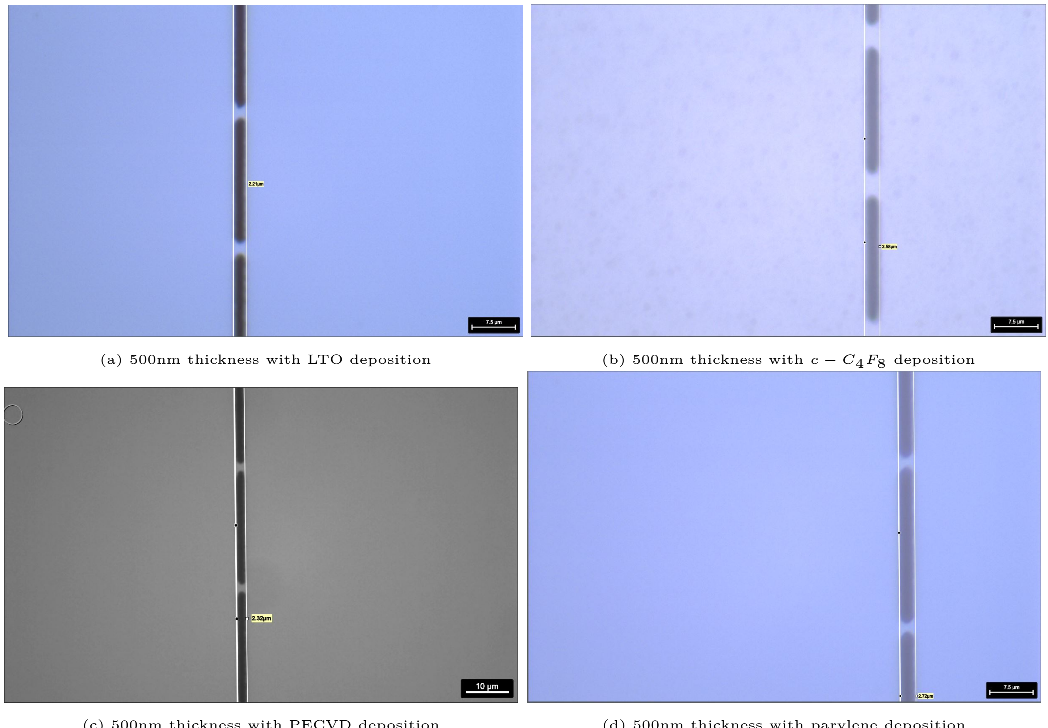
[10] "https://www.epfl.ch/schools/sb/research/iphys/fr/nos-services/salles-blanches/iii-v-lab/oxford-plasmalab-system-100-pecvd/", Iphys, EPFL

[11] "Doped Microcrystalline Silicon Layers for Solar Cells by 13.56 MHz Plasma-enhanced Chemical Vapour Deposition", Jidong Longa, Yunfeng Yina, Shing Yin R. Siana, Zekun Rena, Juan Wanga, Premachandran Vayalakkaraa, Selvaraj Venkataraja and Armin G. Aberle, Elsevier, February 2012

[12] "https://fr.wikipedia.org/wiki/Parylène", Wikipedia

[13] "https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/comelec-c-30-s/", CMI, EPFL

A Microscope's photos before final etching



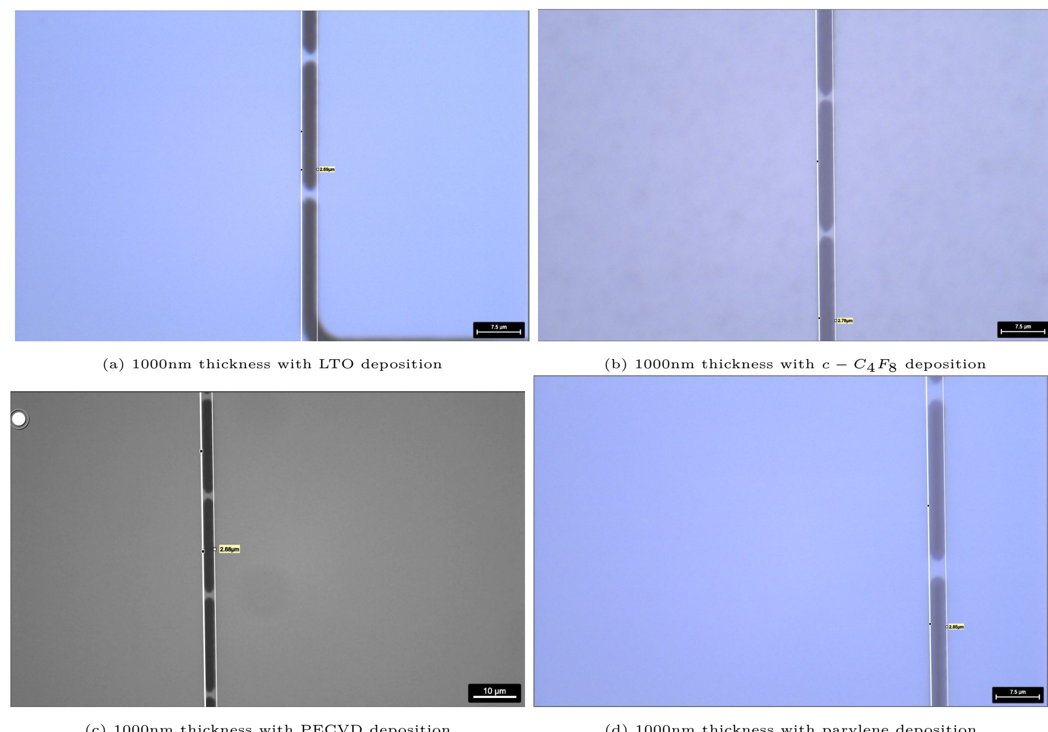
(a) 500nm thickness with LTO deposition

(b) 500nm thickness with $c - C_4F_8$ deposition

(c) 500nm thickness with PECVD deposition

(d) 500nm thickness with parylene deposition

Figure 33: 500nm measurement before final etching



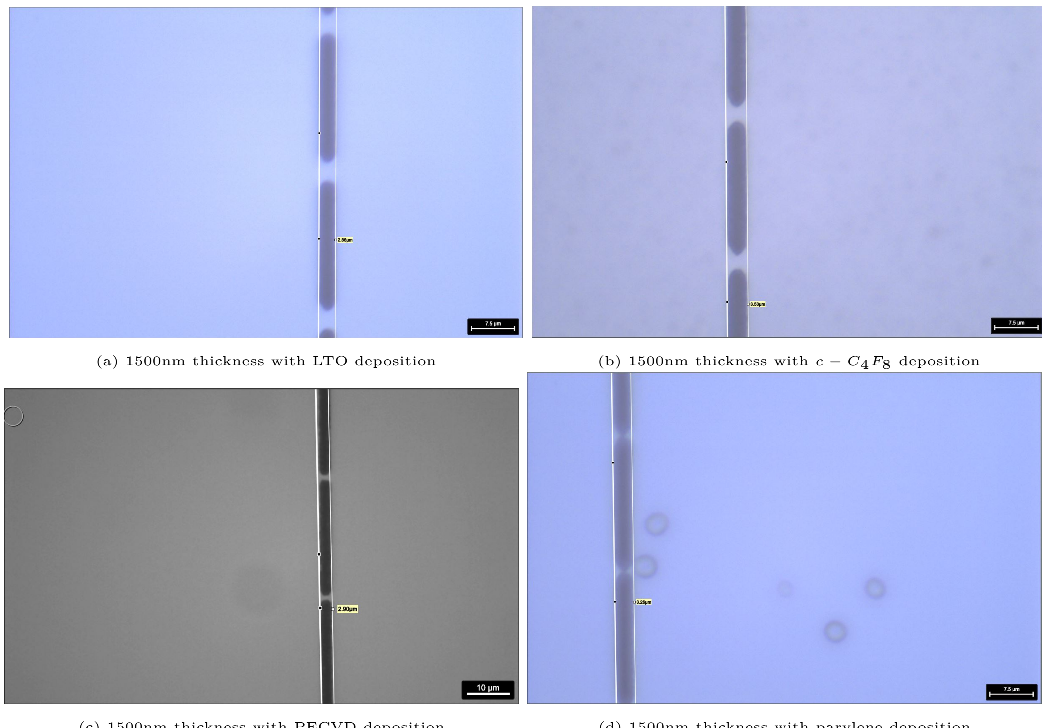
(a) 1000nm thickness with LTO deposition

(b) 1000nm thickness with $c - C_4F_8$ deposition

(c) 1000nm thickness with PECVD deposition

(d) 1000nm thickness with parylene deposition

Figure 34: 1000nm measurement before final etching



(a) 1500nm thickness with LTO deposition

(b) 1500nm thickness with $c - C_4F_8$ deposition

(c) 1500nm thickness with PECVD deposition

(d) 1500nm thickness with parylene deposition

Figure 35: 1500nm measurement before final etching

B Process Flow

Lab : Advanced NEMS Group
Operator Name : **Hugo Calamandrei**
Supervisor Name : Luis Guillermo Villanueva
Process Flow Date : 09.03.2021

Phone : +41 78 613 49 59
Office : BM 2922
E-mail : hugo.calamandrei@epfl.ch

CMi EPFL Center of MicroNanoTechnology

☑ Semestral Project ☐ Master Project ☐ Thesis ☐ Other

Silicon Oxide Walls

Description of the fabrication project

The aim of this semester project is the fabrication of thin (2-3µm) silicon oxide walls on a silicon substrate. The developed process flow will be later integrated into our device consists of a suspended membrane, 400 nm thick, with inter-digitated (IDT) electrodes on top. These walls will be used to limit the area of the silicon layer that will be etched using isotropic silicon etching (Si_release recipe in AMS).

Technologies used
Photolithography, Si etching, SEM observation, oxide deposition (LTO or PECVD) or alternatively parylene

Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**1 µm**	First Mask	Silicon etching
Substrate Type			
Silicon <100>, 4 inches			

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.
☑ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.
☑ No ☐ Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.
☑ No ☐ Yes => confirm pads design (size, pitch) and involved materials with CMi staff

Lab : Advanced NEMS Group
Operator Name : **Hugo Calamandrei**
Supervisor Name : Luis Guillermo Villanueva
Process Flow Date : 09.03.2021

Phone : +41 78 613 49 59
Office : BM 2922
E-mail : hugo.calamandrei@epfl.ch

Step-by-step process outline

Step	Process description	Cross-section after process
01	**Silicon Substrate**: *Si Test Wafer* Thickness: *520 µm*	Si
02	*Photolithography: Mask 1* Machine: HMDS, EVG150, VPG200 - AZ1512 1.1µm - Direct wafer writing on VPG	PR Si
03	*Si etching (DRIE)* Machine: AMS200 - Recipe: SOI_acc-- - Depth: 20 µm - Width changing from 2µm to 3µm	PR Si
04	*Photoresist Removal* Machine: Tepla and UFT1164 - Recipe: Strip_High - Remover UFT1165 Z02	Si
05	*Oxidation* Machine: LTO or PECVD *CMI Service or Physics Cleanroom* **Alternative Process: Parylene Deposition*	SiO_2 Si

06	*Dry etching* Machine: SPTS	SiO_2 Si