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New Technologies to Enhance the Figures-of-Merit of GaN Power Devices

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Abstract

Gallium Nitride (GaN) is a promising material that enabled groundbreaking developments in the field of optoelectronics and high-power radio frequency communication. More recently, GaN-based devices for power conversion applications have been proposed showing an excellent potential in reducing losses in power converters and leading to more compact and lightweight solutions. Thanks to Gallium Nitride wide band-gap, large breakdown electric field, and high electron mobility, GaN power devices lead to higher efficiency and smaller footprint compared to conventional silicon devices. Besides, their higher operating frequency results in a considerable size reduction for the passive components, thus further increasing the power density of the overall system. GaN power devices have recently entered the market and are gaining a considerable share for applications such as fast chargers, electric vehicles, data centers, and aerospace.

Despite its fast development, GaN power technology is not yet mature and several aspects ranging from the device design to its packaging and use in a real converter need to be investigated and improved for its widespread adoption. From a device point of view, the performance of current GaN power transistors is still far from the limit offered by the material, with further enhancements requiring a significant reduction in the on-resistance and increase in the breakdown voltage of the device. Besides, GaN Schottky barrier diodes (SBDs) still suffer from several shortcomings and are far from commercialization, which limits the versatility of the GaN power technology. In addition, despite the lateral architecture of GaN-on-Si power devices, GaN power integrated circuits (ICs) including multiple power devices are yet to be developed, which would enable further size and cost reduction, higher switching frequency, and the integration of additional control and sensing functionalities. Finally, the drastic footprint reduction of GaN power devices requires new thermal management techniques to effectively extract the resulting high heat-fluxes, which would otherwise prematurely limit the performance of the device.

This thesis aims at addressing the aforementioned challenges focusing on the performance improvement of the single power device, its monolithic integration into a power IC and use in a real converter, and the thermal management of the whole power integrated circuit.

To significantly improve the performance of power devices, a novel multi-channel tri-gate technology employing several two-dimensional electron gas (2DEG) channels in combination with a three-dimensional gate architecture is demonstrated. Thanks to the reduced resistance of the multi-channel platform and the superior 3D gate control, multi-channel tri-gate devices enable a considerable reduction of the device on-resistance for a certain breakdown voltage while also achieving key features for power devices such as Enhancement–mode operation and reduced current collapse. In addition, the concept of intrinsic polarization super junctions (i-PSJ) is introduced to further enhance the device performance by improving its off-state electric field distribution. A robust platform that enables

excellent charge matching for single- and multi-channel structures is proposed resulting in a flat electric field profile in the whole drift region. The potential of i-PSJs compared to conventional HEMTs is unveiled by deriving a model to describe the main figures-of-merit of GaN lateral devices, which shows a significant improvement in both $R_{ON,SP}$ vs V_{BR} and R_{ON} x E_{oss} figures-of-merit for i-PSJ devices.

Furthermore, high-performance GaN SBDs are demonstrated by properly designing the anode region, either with the use of a *p*-GaN cap layer or a tri-gate architecture, in order to protect the Schottky barrier while reducing the output charge. This results in excellent dc and switching characteristics for the proposed SBDs, which also present outstanding performance with respect to commercially available devices. The potential of GaN-on-Si power ICs is demonstrated by monolithically integrating several high-performance GaN SBDs to realize a magnetic less DC-DC boost converter. The proposed IC shows excellent potential for high-frequency operation combined with largely increased power density compared to Si and SiC solutions.

Lastly, to manage the unprecedented heat fluxes deriving from the drastic device miniaturization and monolithic integration, embedded liquid cooling directly in the device substrate is investigated showing its potential to greatly improve the device thermal performance without impacting its electrical characteristics.

The results presented in this thesis address several key challenges of GaN power devices and demonstrate the extraordinary potential of the GaN technology for high-efficiency, cost-effective, and ultra-compact future power conversion.

Keywords: GaN, power devices, HEMTs, SBDs, tri-gate, multi-channel, polarization super junctions, power IC, thermal management, microchannel cooling, cryogenic characterization

Sommario

Il nitruro di gallio (GaN) è un materiale estremamente promettente che ha permesso uno straordinario sviluppo dell'optoelettronica e della comunicazione a radiofrequenza e alta potenza. Più recentemente, dispositivi basati sul GaN sono stati proposti per applicazioni di conversione di potenza, dimostrando un eccellente potenziale nel ridurre le perdite nei convertitori e risultando in soluzioni più compatte e leggere. Grazie all'ampio band-gap del nitruro di gallio, al suo alto campo elettrico di rottura e la sua elevata mobilità, i dispositivi di potenza basati sul GaN presentano un'efficienza più elevata e dimensioni ridotte rispetto ai tipici dispositivi di silicio. Inoltre, la loro alta frequenza di utilizzo permette una notevole riduzione delle dimensioni dei componenti passivi, aumentando ulteriormente la densità di potenza dell'intero sistema. I dispositivi di potenza in GaN sono recentemente entrati sul mercato e stanno acquistando una quota importante per applicazioni come i caricatori veloci, i veicoli elettrici, i data centers e l'aviazione.

Nonostante questo rapido sviluppo, la tecnologia di potenza in GaN non è ancora matura e numerosi aspetti dalla progettazione del dispositivo al suo confezionamento e uso in un convertitore necessitano di essere studiati e migliorati per una adozione su larga scala. Dal punto di vista del dispositivo, le prestazioni degli attuali transistor di potenza in GaN sono ancora lontane dal limite offerto dal materiale, con ulteriori miglioramenti che richiedono una notevole riduzione della resistenza e un aumento della tensione di rottura del dispositivo. Inoltre i diodi a barriera Schottky in GaN presentano ancora molte limitazioni e sono lontani da essere commercializzati, limitando la versatilità della tecnologia di potenza in GaN. In più, nonostante l'architettura planare dei dispositivi in GaN su silicio, circuiti integrati di potenza in GaN che includano numerosi dispositivi di potenza non sono ancora stati sviluppati, il che permetterebbe un'ulteriore riduzione delle dimensioni e del costo, una frequenza di utilizzo più elevata e l'integrazione di aggiuntive funzionalità di controllo e monitoraggio. Infine, la drastica riduzione delle dimensioni dei dispositivi di potenza in GaN necessita di nuove tecniche di gestione termica per estrarre in modo efficace i risultanti elevati flussi di calore che altrimenti limiterebbero le prestazioni del dispositivo.

Lo scopo di questa tesi è di affrontare le suddette sfide concentrandosi sul miglioramento delle prestazioni del singolo dispositivo, sulla sua integrazione monolitica in un circuito integrato di potenza e uso in un vero convertitore, e sulla gestione termica dell'intero circuito integrato di potenza.

Per migliorare considerevolmente le prestazioni dei dispositivi di potenza, un'innovativa tecnologia basata su molteplici canali bidimensionali in combinazione con un'architettura di gate tridimensionale viene dimostrata. Grazie alla riduzione della resistenza nella piattaforma a multi-canale e al superiore controllo tridimensionale, i dispositivi a multi-canale con gate tridimensionale permettono una notevole riduzione della resistenza del dispositivo per una certa tensione di rottura e sono anche in grado di fornire caratteristiche fondamentali per ogni dispositivo di potenza come operazione in Enhamcement mode e ridotto collasso di corrente. Inoltre, viene introdotto il concetto della super giunzione a

polarizzazione intrinseca (i-PSJ) per potenziare ulteriormente le prestazioni del dispositivo, migliorando la distribuzione del campo elettrico nello stato spento. Viene proposta una robusta piattaforma che permette un'ottima compensazione di cariche per strutture a singolo e multi canale, portando a dispositivi che presentano un campo elettrico constante in tutta la regione di drift. Il potenziale delle i-PSJ in relazione con i tradizionali HEMTs è dimostrato derivando un modello che descrive le principali figure di merito dei dispositivi laterali in GaN e che mostra un notevole miglioramento sia nella figura di merito $R_{ON,SP}$ vs V_{BR} che in R_{ON} x E_{oss} per i dispositivi i-PSJ.

Inoltre, SBDs in GaN ad alte prestazioni sono dimostrati progettando adeguatamente la regione dell'anodo, sia servendosi di uno strato di *p*-GaN sia di un'architettura a gate tridimensionale, in modo da proteggere la barriera Schottky e ridurre la carica di output. Questa strategia risulta in eccellenti caratteristiche in dc e commutazione per i dispositivi proposti i quali presentano anche ottime prestazioni rispetto alle soluzioni presenti sul mercato. Il potenziale di circuiti integrati di potenza in GaN su silicio è dimostrato integrando monoliticamente diversi SBD in GaN ad alte prestazioni per realizzare un convertitore boost DC-DC senza componenti magnetici. Questo circuito integrato rivela un potenziale eccellente per l'utilizzo ad alta frequenza e un grande aumento nelle densità di potenza rispetto a soluzioni in Si e SiC.

Infine, per gestire i flussi di calore senza precedenti derivanti dalla drastica miniaturizzazione del dispositivo e della integrazione monolitica, un raffreddamento a liquido integrato nel substrato del dispositivo viene investigato dimostrando il suo grande potenziale per migliorare significativamente le prestazioni termiche del dispositivo senza incidere sulle caratteristiche elettriche.

I risultati presentati in questa tesi affrontano con successo le principali sfide dei dispositivi di potenza in GaN e dimostrano lo straordinario potenziale della tecnologia in GaN per una futura conversione di potenza ad alta efficienza, economica ed estremamente compatta.

Parole chiave: GaN, dispositivi di potenza, HEMTs, SBDs, gate tridimensionale, multi-canale, super giunzioni a polarizzazione, circuiti integrati di potenza, gestione termica, raffreddamento a micro canale, caratterizzazione criogenica.

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List of Reference Publications

This thesis is based on the results presented in the following publications.

Chapter 2: Multi-Channel Nanowire Devices for Low On-resistance and Enhancement-mode Operation

Section 2.2

L. Nela, M. Zhu, J. Ma, and E. Matioli, "High-performance nanowire-based E-mode Power GaN MOSHEMTs with large work- function gate metal", *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 439–442, 2019.

L. Nela, M. Zhu, J. Ma, and E. Matioli, "High-performance nanowire-based E-mode Power GaN MOSHEMTs" in *Compound Semiconductor Week*, 2019

Section 2.3

L. Nela *et al.*, "Multi-channel nanowire devices for efficient power conversion", *Nature Electronics*, vol. 4, pp. 284–290, 2021

L. Nela *et al.*, "High-Performance Enhancement-Mode AlGaN/GaN Multi-Channel Power Transistors" in *33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2021, pp. 143–146.

L. Nela, M. Xiao, Y. Zhang, and E. Matioli, "A Perspective on Multi-channel Technology for Next-Generation Power Devices", invited in *Applied Physics Letters* (under revision).

Section 2.4

L. Nela *et al.*, "Conformal Passivation of Multi-Channel GaN Power Transistors for Reduced Current Collapse", *IEEE Electron Device Lett.*, vol. 42, no. 1, pp. 86–89, 2021.

Chapter 3: Intrinsic Polarization Super Junctions Devices for Optimal Electric Field Management

Section 3.2

L.Nela, C. Erine, A. Miran Zadeh, and E. Matioli, "Intrinsic Polarization Super Junctions: Design of Single and Multi-Channel GaN Structures", *IEEE Transaction on Electron Devices,* 2022.

Section 3.3

L. Nela, C. Erine, M.V. Oropallo, and E. Matioli, "Figures-of-Merit of Lateral GaN Power Devices: modeling and comparison of HEMTs and PSJs*", IEEE Journal of the Electron Devices Society*, vol. 9, pp. 1066–1075, 2021.

Chapter 4: High-Performance GaN Lateral Schottky Barrier Diodes towards Power ICs

Section 4.2 **L. Nela,** G. Kampitsis, J. Ma, and E. Matioli, "Fast-Switching Tri-Anode Schottky Barrier Diodes for Monolithically Integrated GaN-on-Si Power Circuits", *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 99–102, 2020.

L. Nela, G. Kampitsis, H. K. Yildirim, R. Van Erp, J. Ma, and E. Matioli, "High-Frequency GaN-on-Si power integrated circuits based on Tri-Anode SBDs", *Proc. Int. Symp. Power Semicond. Devices ICs (ISPSD)*, pp. 517–520, 2020.

Section 4.3 **L. Nela,** R. Van Erp, G. Kampitsis, H. K. Yildirim, J. Ma, and E. Matioli, "Ultra-compact, high-frequency power integrated circuits based on GaN-on-Si Schottky Barrier Diodes", *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1269–1273, 2020.

Section 4.4 **L. Nela,** C. Erine, and E. Matioli, "*p*-GaN field plate for low leakage current in lateral GaN Schottky Barrier Diodes", *Applied Physics Letters*, 119, 263508, 2021.

Chapter 5: Thermal Management of High Power-Density GaN Devices and ICs

Section 5.2 **L.Nela,** R. van Erp, N. Perera, A. Jafari, C. Erine, and E.Matioli, "Impact of Embedded Liquid Cooling on the Electrical Characteristics of GaN-on-Si Power Transistors", *IEEE Electron Device Lett.*, vol. 42, no. 11, pp. 1642–1645, (2021)

Section 5.3 R. van Erp, R. Soleimanzadeh, **L. Nela,** G. Kampitsis, and E. Matioli, "Co-designing electronics with microfluidics for more sustainable cooling", *Nature*, vol. 585, no. 7824, pp. 211–216, 2020.

R. Van Erp, G. Kampitsis, **L. Nela,** R. S. Ardebili, and E. Matioli, "Embedded Microchannel Cooling for High Power-Density GaN-on-Si Power Integrated Circuits", *Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst. ITHERM*, pp. 53–59, 2020.

Appendix A: GaN Power Devices for Cryogenic Applications down to 4.2 K

Section A **L. Nela,** N. Perera, C. Erine, and E. Matioli, "Performance of GaN Power Devices for Cryogenic Applications down to 4.2 K", *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, 2020.

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1 Introduction

1.1 The role of Power Electronics

Power electronics is the technology that enables the conversion of electrical energy from one form to another. It acts as the interface between the energy source (power plant, photovoltaic cell, wind turbine) to the electrical load by properly modifying the voltage level, the current flow, and the signal frequency and waveform. Since the invention of the mercury-arc valve in 1902 by Hewitt, power electronics has developed tremendously in terms of efficiency, cost, reliability, and size. Like in several other domains of electronics, a major advance was represented by the transition to solid-state Silicon devices, which has enabled widespread adoption of power electronics for an unprecedented number of applications. Nowadays, power electronics has become a key technology of our modern society (Figure 1.1.1), controlling and converting about 40% [1], [2] of the world's electricity supply to the most adapted form. The increasing need for electrical power in our daily life, as well as the rapid development of renewable energy, are granting power conversion an even more central role in future technology, with an estimated 80% of the global electricity being processed by power electronics by 2030 [1], [2]. Following this rapidly growing trend, efficient, compact, and cost-effective power management solutions are becoming crucial.

The key components of every power conversion system are the solid-state semiconductor devices, such as transistors, diodes, and thyristors, depending on the topology. To a large extent, it is their performance that determines the system's efficiency, size, and operation. While in the past few decades such devices have been realized by the well-established Si technology, the rate of such improvement is rapidly reaching its limit despite all the sophisticated device architectures. Such limitations come from the intrinsic material properties of Silicon, thus requiring new materials specifically fitting power

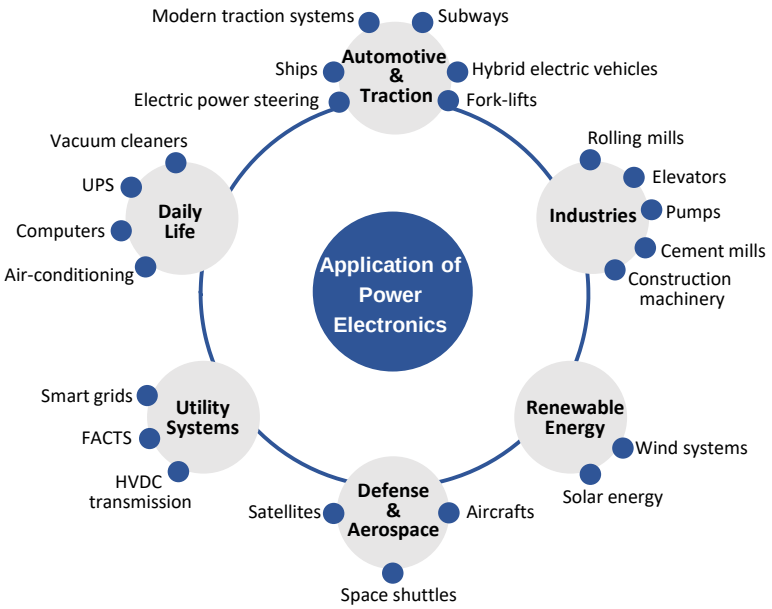


Figure 1.1.1: Applications of power electronics, adapted from Ref. [3].

electronics requirements. In this scenario, wide-band-gap (WBG) semiconductors have emerged as a new material platform for future compact and efficient power electronics thanks to their superior properties. In particular, Gallium Nitride (GaN), in combination with other alloys of the III-V nitride family, has shown extremely promising potential for power conversion, enabling to significantly reduce the device size while resulting in a much-improved performance (Figure 1.1.2 (a-b)). The excellent properties of Gallium Nitride have resulted in growing interest from the major semiconductor manufacturers, together with new start-up companies, to develop GaN power devices. This has led to the very fast development of the GaN technology (Figure 1.1.2 (c)), which, however, still holds a great unexplored potential ahead. In the next sections, the GaN material properties will be introduced, followed by the state-of-the-art of GaN power and their current challenges.

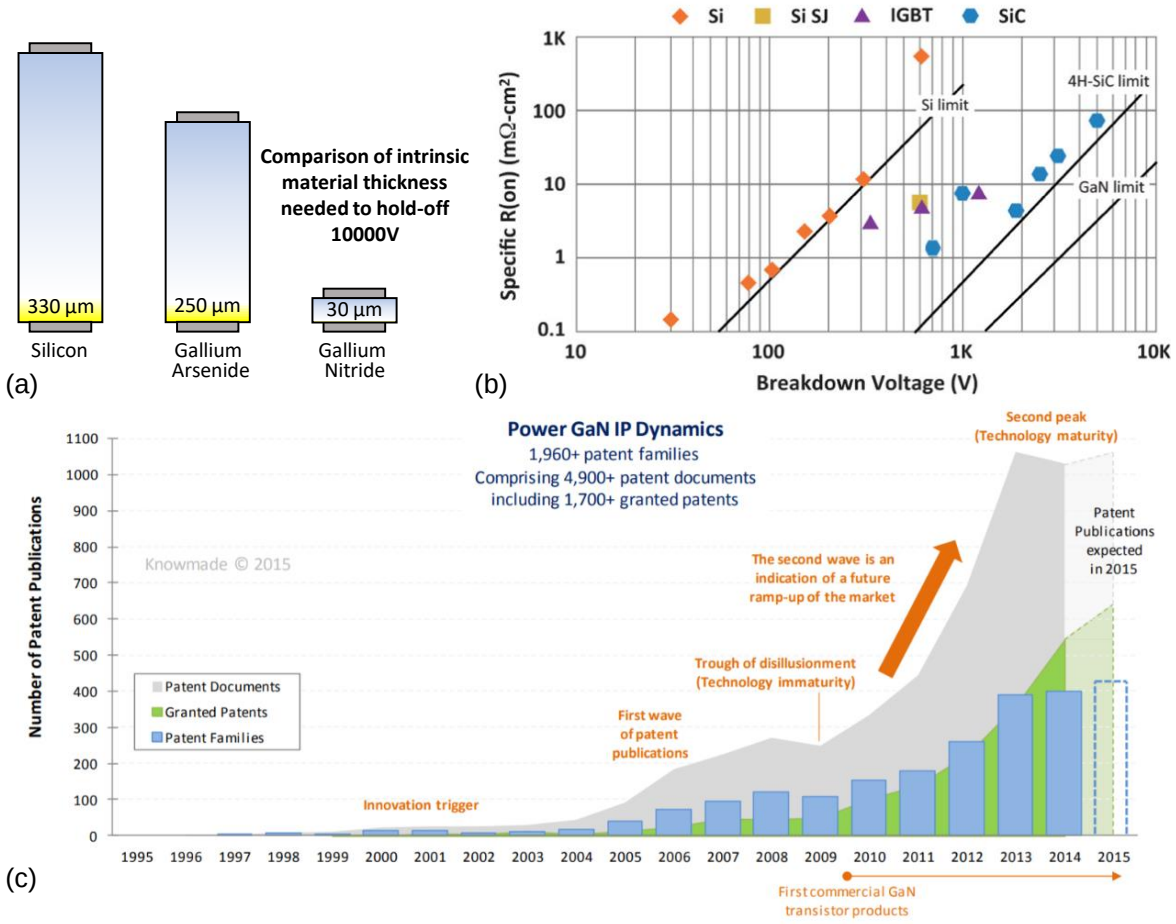


Figure 1.1.2: Advantages of GaN for power applications in terms of reduced size to hold large voltages and reduced resistance. (a) Enhanced GaN voltage blocking properties [4] (b) Specific on-resistance versus breakdown voltage benchmarks of Si, SiC, and GaN power [5] (c) Number of patents filed over the years for GaN power technology [6].

1.2 GaN Material Properties

Gallium Nitride belongs to the III-V Nitride family, which also includes AlN and InN. It is a binary semiconductor with a wurtzite crystal structure whose asymmetry results in a spontaneous polarization contribution. The most common GaN technology is based on an $Al_xGa_{1-x}N$/GaN heterostructure in which a thin AlGaN barrier is grown over a thick GaN layer. While both materials are polar, AlGaN has a higher polarization contribution. In addition, the AlGaN layer is strained due to the heteroepitaxy on GaN, which leads to an additional piezoelectric polarization contribution. The net polarization charges at the AlGaN/GaN discontinuity results in an accumulation of electrons strongly localized at the interface (two-dimensional electron gas or 2DEG) (Figure 1.2.1). The density of the 2DEG in AlGaN/GaN epitaxy is about 1×10^{13} cm^{-2}, but it can be increased by tuning the AlGaN barrier thickness and Al concentration. In addition, the absence of dopant impurities, together with the strong screening effect from the high-density 2DEG, results in high electron mobility up to 2200 $cm^2V^{-1}s^{-1}$, exceeding the value reachable in bulk GaN (1200 $cm^2V^{-1}s^{-1}$). The excellent performance of the AlGaN/GaN 2DEG in combination with the GaN material properties related to its wide band-gap results in an extremely promising platform for power devices.

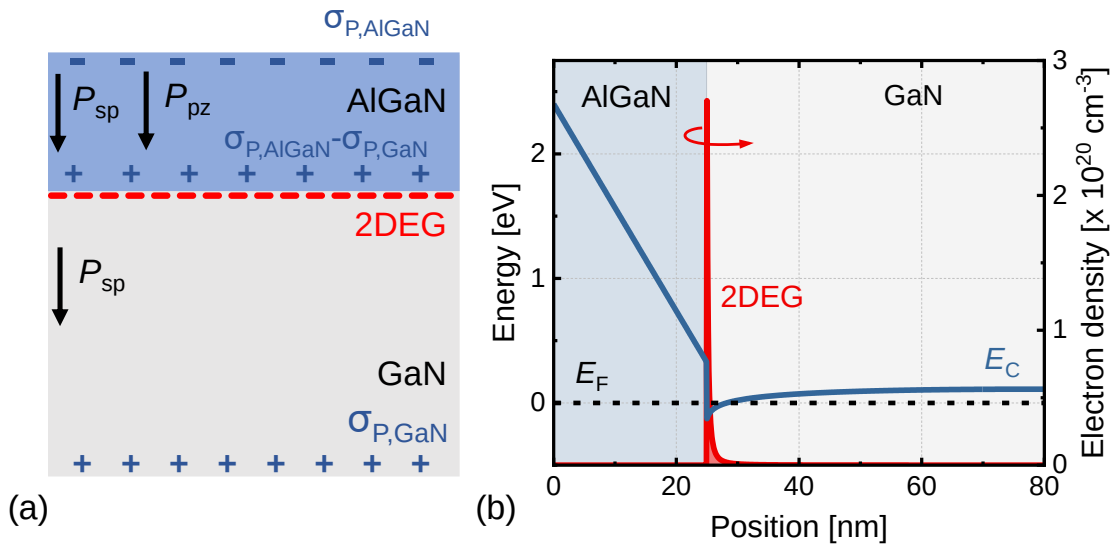


Figure 1.2.1: (a) Formation of 2DEG at the AlGaN/GaN interface due to the presence of polarization charges. (b) Bandstructure of the AlGaN/GaN heterostructure. A barrier thickness of 25 nm has been considered with an Al composition of 25%.

Overall, GaN offers a high breakdown field, large electron saturation velocity, and a high-density 2DEG with excellent mobility (Table 1.2.1). This results in excellent Baliga Figure of Merit (BFM), Baliga High-Frequency Figure of Merit (BHFFM), and Johnson's Figure of Merit (JFM), which are usually employed to determine the material suitability for high power and fast switching applications. Their superior values with respect to Si and SiC indicate low resistive and switching loss, making GaN an ideal candidate for efficient, fast-switching, and compact future power electronics (Table 1.2.1).

	Electron mobility [$cm^2V^{-1}s^{-1}$]	Saturation velocity [$\times 10^7$ cm/s]	Bandgap [eV]	Breakdown field [$\times 10^6$ V/cm]	BFM	BHFFM	JFM
Si	1350	1	1.12	0.3	1	1	1
4H-SiC	900	2	3.26	3	560	66	400
GaN	2200 (2DEG)	2.7	3.39	3.3	1730	161	880

Table 1.2.1: Comparison of Si, SiC, and GaN for power applications.

1.3 GaN Growth and Substrates

GaN epi-structures can be grown by different techniques and on different substrates. The main growth methods are Metallorganic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE). MBE is typically used for academic and research purposes due to the easier control of the growth parameters, which allows the precise tuning of the material composition and thickness. MOCVD is instead the most popular growth technique for the LED and HEMT industry thanks to its large throughput and good material quality.

GaN power devices are usually grown on foreign substrates due to the high cost and small size of GaN substrates. Table 1.3.1 shows the most popular substrates for GaN growth. In the case of heteroepitaxy on a foreign substrate, the lattice constant (α) and the thermal expansion difference (ΔCTE) between the substrate and GaN are of great importance as they can lead to considerable stress in the epilayer. If not properly managed, a large stress value results in damages to the GaN crystal structure such as cracks and dislocations. This is typically addressed by designing a complex buffer structure that compensates the tensile/compressive stress to the upper GaN layer during the cooling after the growth [7]–[9]. Despite the recent progress, the maximum thickness of the GaN heteroepitaxy that can be achieved on foreign substrates such as Si and Sapphire is typically limited to a few micrometers. Another important aspect to consider is the substrate thermal conductivity (*W*), which is important to manage the high heat-flux derived from the device miniaturization.

	GaN	SiC	Sapphire	Si (111)
Δα %	-	3.5	-16	16.9
ΔCTE %	-	25	-34	54
W [W/cm K]	1.3	3-3.8	0.5	1-1.5
Cost [€/cm^2]	30	10	1	0.1
Size [Inch]	4	6	8	12

Table 1.3.1: Comparison between the main substrates used for GaN growth [10], [11].

Despite these considerations, most power electronic applications are extremely cost-sensitive with cost-effective solutions being fundamental for the successful commercialization of GaN devices. Under this point of view, the GaN-on-Si platform offers a tremendous prospect thanks to the extremely low cost and large diameters Si substrates [10]. In addition, GaN-on-Si technology is compatible with conventional CMOS fabrication, allowing foundries to process GaN devices along with Si transistors, sharing the highly optimized fabrication line [12]. Such promising outlooks have drawn intensive research focus on GaN-on-Si growth, which has enabled enormous development in recent years.

The large CTE and lattice mismatch between GaN and Si has been addressed by careful design of the buffer structure. This typically includes graded AlGaN or superlattice layers to compensate for the stress of the GaN epilayer during cooling [7]–[9] (Figure 1.3.1 (a)). Thanks to this approach, 8-inch, crack-free GaN-on-Si epi-structures with 5 µm-thick GaN layers have been demonstrated and are commercially available (Figure 1.3.1 (b)) with on-going continuous improvements towards 12-inches

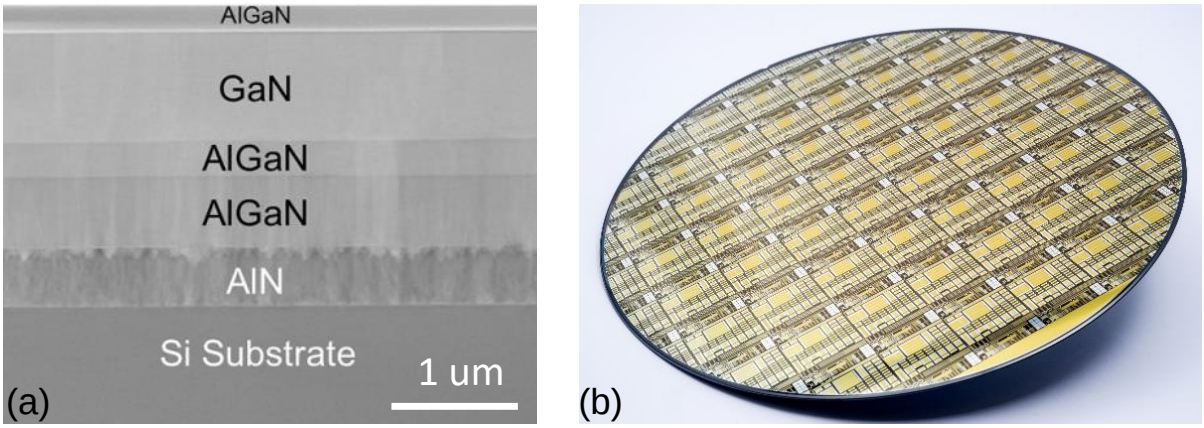


Figure 1.3.1: (a) GaN-on-Si epi-structure showing the buffer layers, the GaN channel, and the top AlGaN barrier [13] (b) 8-inch GaN-on-Si wafer grown by IMEC [14].

wafers and thicker GaN layers. A proper design of the buffer layers is of critical importance also to reduce the device leakage and improve its breakdown. The growth of GaN by MOCVD results in *n*-type unintentional doping due to the introduction of impurities, which significantly reduce the material resistivity and lead to a large leakage current for operation at high-voltage. Such a phenomenon can be tackled by the introduction of carbon atoms, either by extrinsic precursors or by adjusting the growth parameters. C atoms result in deep acceptor states and compensate electrons due to unintentionally doping. This technique has demonstrated significant leakage reduction and is currently employed in most commercial buffer layers. However, a judicious design of the carbon doping profile is necessary to avoid the trapping of electrons from the 2DEG, which may result in serious degradation of the device's dynamic performance [15].

Nowadays, GaN-on-Si technology is reaching its maturity with several vendors offering 650 V-rated solutions at an ever-decreasing price. Besides, promising increases in the wafer size up to 12 inches are expected in the near future. Thanks to such advances, most GaN devices manufacturers (e.g. Infineon, Texas Instruments, GaN System, EPC, Transphorm) adopted GaN-on-Si as a platform for their solutions. As a result, the price of GaN devices has been steadily decreasing over the last years, approaching Si devices and well below SiC ones, despite not being yet in mass production.

1.4 Current GaN power technology and open challenges

Since the first demonstration of an AlGaN/GaN HEMT [16] in 1993, GaN power technology has considerably developed addressing numerous challenges of the device fabrication and operation. Thanks to these efforts, significant improvement in the performance of GaN power devices has been achieved and several hindrances have been overcome. This resulted in the commercialization of the first 200 V Enhancement-mode GaN power device in 2010 [17], followed by the introduction of 650 V devices in 2014 [17]. Currently, the majority of commercial GaN power devices are based on lateral HEMT architecture, which enables high-performance and reduced cost thanks to the GaN-on-Si platform. Several GaN manufacturers, both fabless and with their own foundry, have appeared in the last years offering a large variety of solutions (Figure 1.4.1). Thanks to this fast development, the family of available GaN power devices has greatly expanded, offering competitive solutions in the voltage range from 30 V to 650 V, with significant further investments to enter the 1200 V market.

The excellent switching performance of GaN devices, the much-reduced footprint, and competitive cost are very interesting for a large number of applications. At the moment, the main market for GaN devices is represented by consumer electronics and, in particular, by fast chargers for smartphones and laptops. However, widespread adoption of GaN HEMTs is to be expected in the next few years also in the automotive market, especially for electric vehicles, to improve the performance of the DC/DC converters and onboard chargers, thus resulting in increasing mileage and faster recharge time. Finally,

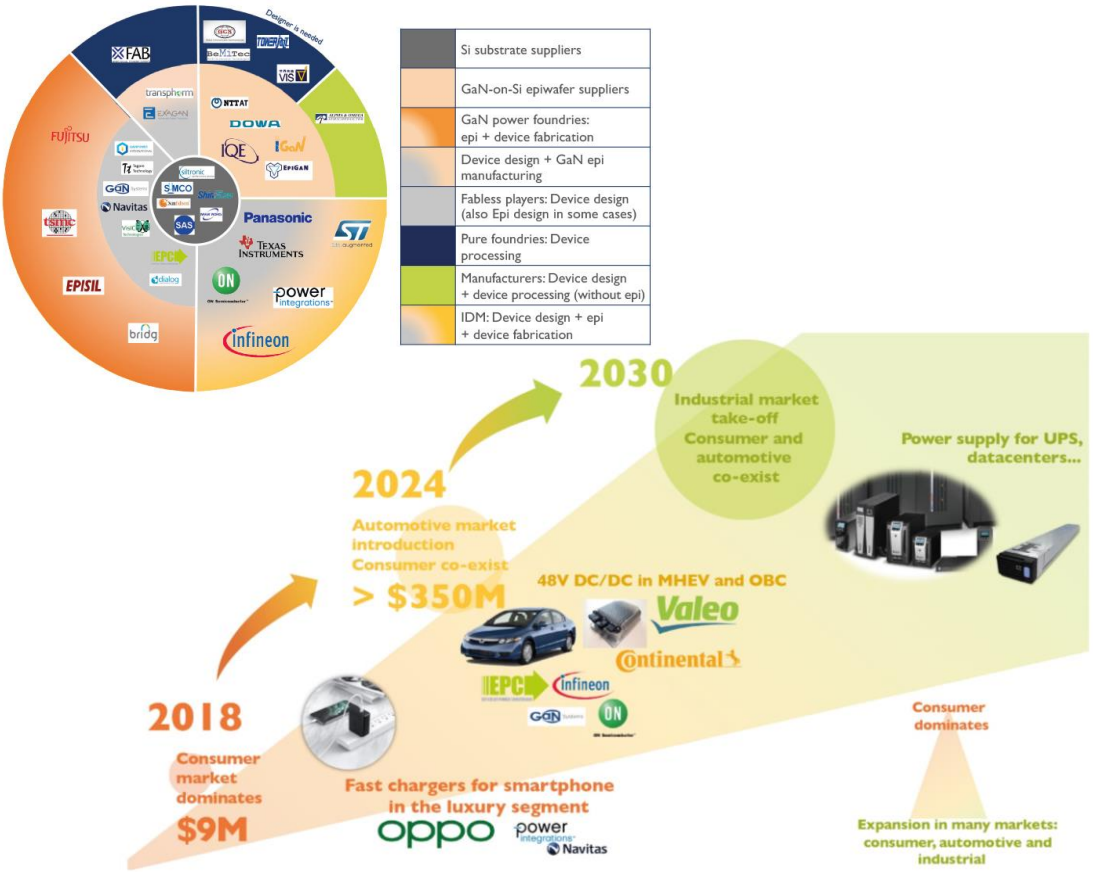


Figure 1.4.1: Power GaN industry overview in 2018 [18] and predicted development of the market for GaN power devices [19].

GaN devices will represent a key technology in the rapidly growing market of data centers in order to realize compact and high-efficiency DC/DC converters and UPS systems. Thanks to these promising applications, the GaN power device market is expected to rapidly grow in the next years reaching a significant market share (Figure 1.4.1).

However, despite this exciting outlook, GaN power devices still have a tremendous hidden potential that is yet to be exploited, and several open challenges remain for this technology. Thus, significant research activity, both at the academic and industrial level, is still ongoing to address these issues and improve the performance of GaN devices.

In particular, Enhancement-mode (E-mode) operation combined with low on-state resistance and reduction of the current collapse phenomena in GaN HEMTs still represents key challenges for the technology. Besides, despite the recent progress, the performance of GaN power devices is still far from the theoretical limits of the material. The key challenge is to further reduce the device resistance while maintaining high voltage blocking capability, thus resulting in more efficient and compact power devices. Furthermore, while the development of GaN HEMTs has been relatively fast, GaN SBDs have encountered a more difficult path and, at the moment, no GaN power SBD is commercially available, which represents a big shortcoming for the GaN power technology and limits its versatility and design possibilities.

In addition to these aspects related to the device design, significant challenges and opportunities start to emerge at the circuit and packaging level. For instance, the integration of several components to realize power ICs is a quickly developing field that promises further functionalities and cost reduction. Moreover, new solutions are emerging to manage the high-heat fluxes resulting from the aggressive device miniaturization and integration.

In the next sections, we will present in detail the approaches that are currently employed to address these challenges, focusing on their advantages and shortcomings. Finally, we will propose our solutions, which will be presented in this thesis.

1.4.1 E-mode Operation and V_{TH} vs R_{ON} Trade-off

AlGaN/GaN HEMTs are intrinsically Depletion-mode (D-mode) devices since a 2DEG is present at equilibrium due to the polarization contributions. However, D-mode operation is not suitable for power applications due to safety concerns and increased complexity for the gate driver. A large, positive threshold voltage (V_{TH}) would be highly desirable to guarantee a proper safety margin in case of spikes from the driving circuit. To be adopted as the new power devices platform, GaN HEMTs need to show high performance along with fully E-mode operation. Under this point of view, the progress has been slower and the first Enhancement mode (E-mode) GaN HEMT was commercialized only in 2010, 5 years after the first D-mode transistor. The difficulties in achieving E-mode operation arise from the large electron concentration in the channel region, which should be depleted without affecting the device conductivity. In addition, Normally-Off operation requires a large gate voltage (V_G) swing up to 10V, which leads to extremely large gate leakage for standard HEMT architectures based on a Schottky gate. Two main approaches have been proposed to achieve E-mode operation: design of the GaN HEMT device to shift V_{TH} to positive values or realization of E-mode operation at a circuit level.

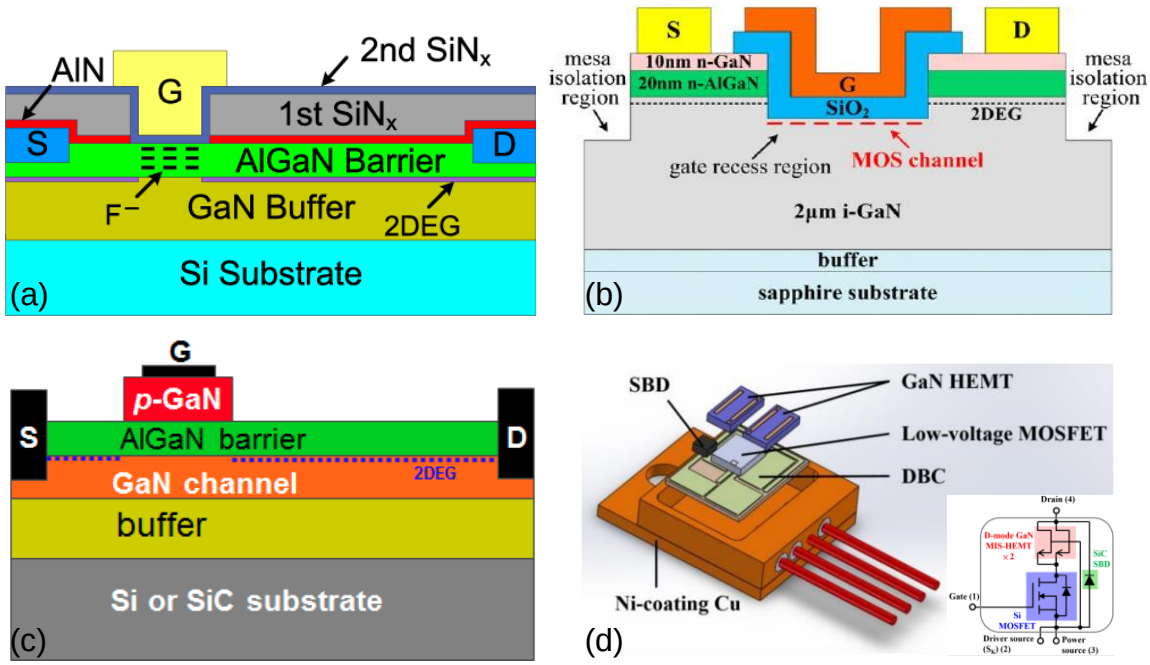


Figure 1.4.2: Proposed approaches to achieve E-mode operation. (a) Implantation of negatively charged fluorine ions in the AlGaN barrier under the gate region [20] (b) MOS-HEMT structure with fully recessed AlGaN barrier [21] (c) *p*-GaN cap layer [22] (d) External connection to a low-voltage Si device in a cascode configuration [23].

Some of the most common methods that act on the device design are based on *p*-type GaN cap-layers [24]–[28], fluorine implantation [29], [30], and gate recess [31]–[35] (Figure 1.4.2 (a-c)). These approaches rely on depleting the 2DEG under the gate by removing or treating the AlGaN barrier, or by depositing *p*-GaN over the barrier. While positive V_{TH} has been successfully achieved, the threshold voltage shift that can be obtained is limited thus requiring heterostructures with reduced N_s or introducing severe damages to part of the channel. This results in a trade-off between the threshold voltage and the on-resistance (V_{TH} vs R_{ON}), with E-mode devices that present degraded on-state performance with respect to the counterpart normally-on devices.

An alternative approach is to achieve E-mode operation at the circuit level by employing a cascode configuration in which a low-voltage (LV) Si MOSFET is externally combined to a high-voltage (HV) D-mode GaN HEMT (Figure 1.4.2 (d)). Such a method allows combining the simplified fabrication of high-performance D-mode GaN HEMT with the large V_{TH} and voltage swing of Si MOSFET, resulting in an appealing commercial solution, which is currently offered by Transphorm. Nevertheless, the introduction of the Si device mitigates the advantages of the GaN technology by limiting the operation at high temperatures or in harsh environments and by degrading the switching performance. In addition, a careful matching between the LV Si MOSFET and the HV GaN HEMT should be ensured to avoid early device failure and reliability concerns. Lastly, the co-packaging of the two devices results in an additional cost and parasitics due to interconnection.

For these reasons, truly E-mode devices are usually preferred and have bigger potential in terms of performance and cost reduction. At the moment, the most common technology for E-mode commercial devices is a *p*-GaN cap layer in combination with the partial barrier recess or regrowth [23]. Nevertheless, despite the recent developments, such devices still suffer from the trade-off between the threshold voltage and the on-resistance. For these reasons, alternative methods to improve the V_{TH} vs R_{ON} performance are currently under study and would be of great importance.

1.4.2 Dynamic On-resistance and Electric Field Management

GaN power devices are expected to be gain a significant market share in the low to medium power segment with voltage ratings up to 650 V and extensive research targeting 1200 V. To withstand such high voltages, effective solutions are required to manage the large electric field in the channel and preserve the device on-state performance.

While the AlGaN/GaN HEMT lateral architecture offers excellent on-state performance with a high-mobility 2DEG, it also suffers from severe challenges in the off-state. The large carrier concertation in the 2DEG results in a reduced extension of the depletion region and the lateral architecture favors a non-uniform field distribution, which presents a strong peak at the device gate edge. If not properly addressed, such a phenomenon can lead to premature device breakdown and a decrease of the overall device figure-of-merit.

In addition, the electrons in the 2DEG are very close to the surface and prone to severe trapping from surface states during the off state. This translates into an increase of the device dynamic R_{ON} with respect to the DC value (Figure 1.4.3 (a)). The de-trapping time of these electrons depends on the energy level of the trap, its cross-section, and the device temperature, varying from 100 ns to several seconds and significantly affecting the device performance. Besides, the dynamic R_{ON} strongly depends on the off-state electric field distribution, with a peaked profile favoring the trapping process. Additional trapping contributions can also come from the carbon doping of the buffer layer, which usually results in acceptor traps with a long time constant (Figure 1.4.3 (b)).

Nowadays, these challenges are typically addressed by employing three simultaneous approaches.

1. **Optimization of the off-state electric field distribution by the design of field plate structures.** Field plate electrodes facilitate the depletion of the 2DEG, splitting the peak electric field at the gate edge in numerous smaller peaks. By a careful design, it is possible to ensure that none of the peaks overcomes the material critical field, which improves the device breakdown (Figure 1.4.3 (c-d)). Yet, a judicious design of multiple field plates is typically very challenging and requires the optimization of several parameters such as the field plate length, overlap, and dielectric thickness. While simulation tools can provide some indications, a complex experimental characterization involving the optimization of the inter-dielectric layers is often required. In addition, the use of field plates increases the gate and output capacitance, thus degrading the switching performance and setting an important trade-off between the device DC and switching performance.

2. **Deposition of a surface passivation layer.** A dielectric passivation layer is typically deposited on top of the device to reduce the surface trap density and move the surface dangling bonds far from the 2DEG. The most common passivation layers comprise Si_3N_4, SiO_2, and AlN, although many other solutions have also been investigated [36]. The surface conditions before the deposition and the quality of the passivation layer are of great importance for a successful reduction of the current collapse.

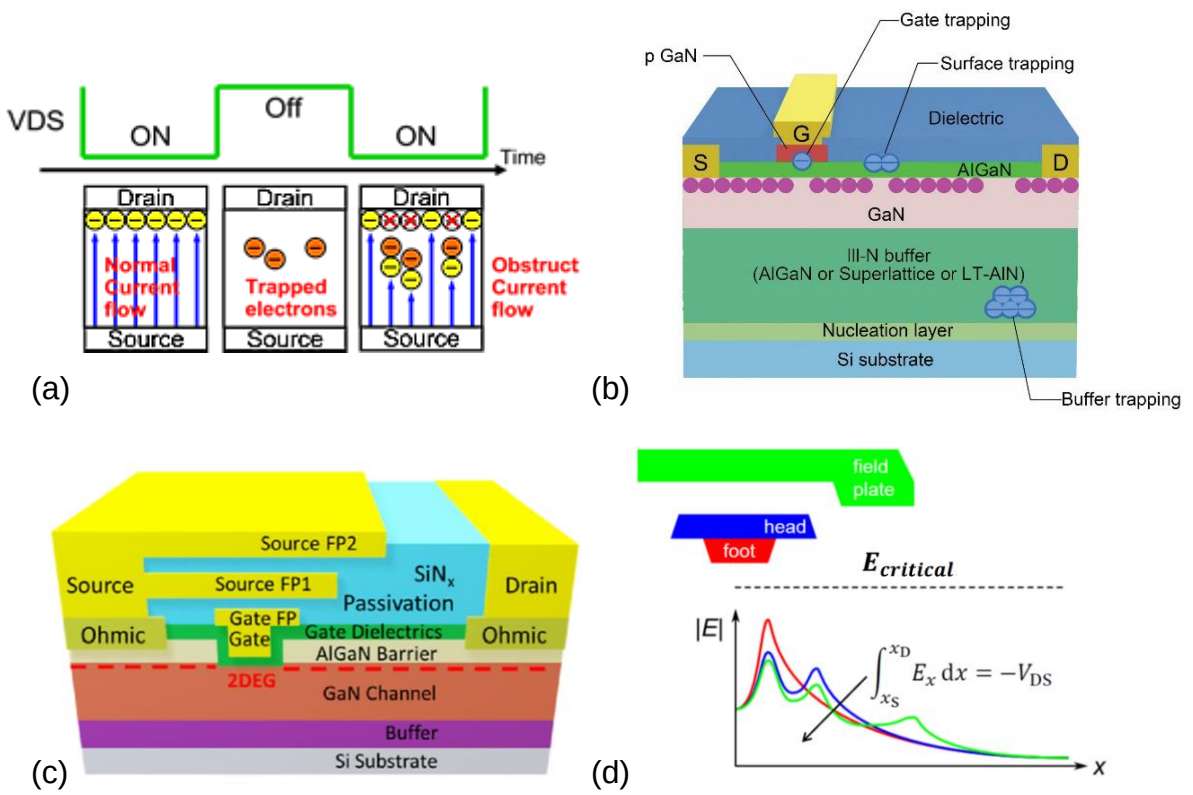


Figure 1.4.3: (a) Electron trapping mechanism during off-state and consequent reduction of the on current [37] (b) Different location of traps for a typical GaN HEMT [38] (c) Typical GaN HEMT structure with multiple field plates designed to optimize the electric field distribution in the off-state [39] (d) Improved electric field profile by the introduction of field plates [40].

3. **Careful doping of the GaN buffer.** While GaN buffers grown on Si substrate are often doped with carbon impurities to reduce the unintentional *n*-type doping resulting from the MOCVD growth (*Section 1.3*), carbon atoms can result in trapping centers for electrons in the 2DEG. To avoid this undesirable effect, the doping of the substrate needs to be minimized and the doping profile should be optimized to avoid large doping concentrations close to the 2DEG.

By combining these techniques, a low dynamic R_{ON} increase has been demonstrated up to 650 V, although significant differences are still observed among vendors and very careful process optimization is required to achieve such performance.

In addition, the presented approaches have been developed for conventional planar device architectures, which represent the commercially-available solutions at the moment. Achieving a reduced current collapse in more advanced device structures, such as the nanowire devices that are presented in this thesis, is yet to be demonstrated and requires the introduction of novel solutions, along with the optimization of the aforementioned approaches.

1.4.3 Improving the $R_{ON,sp}$ vs V_{BR} Trade-off

The specific on-resistance ($R_{ON,sp}$) vs breakdown voltage (V_{BR}) is one of the most important trade-offs for power devices. Reducing $R_{ON,sp}$ results in lower resistive loss and more devices per wafer and is therefore essential to enhance the efficiency and reduce the cost of power devices. However, it is extremely challenging to reduce $R_{ON,sp}$ without decreasing the breakdown voltage. This is because the desired V_{BR} ultimately determines the length of the required drift region, which in turn sets the device

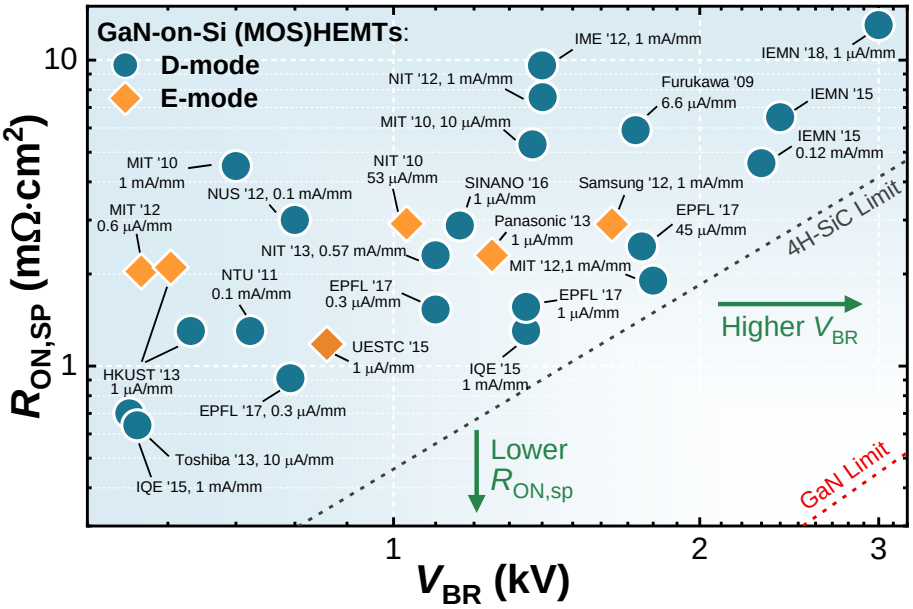


Figure 1.4.4: Performance of state-of-the-art GaN power HEMTs present in the literature.

dimensions and resistance. This results in a trade-off between the achievable breakdown voltage and specific on-resistance for a certain material, which was described by B. Jayant Baliga with the expression [41]:

$$\frac{V_{\mathrm{BR}}^2}{R_{\mathrm{ON,sp}}} = \frac{\varepsilon_s \mu E_c^3}{4} \qquad 1.1$$

where ε_s is the permittivity of the semiconductor, μ is the carriers' mobility, and E_C is the critical field. This expression is valid for an ideal, uniformly doped drift region of a unipolar device and sets a limit for the material.

Current GaN power devices are still far from the Gallium Nitride material limit (Figure 1.4.4), which leaves a lot of room for research and improvement. Two main approaches can be adopted to improve this trade-off: on the one hand one can try to reduce the device resistance by using a more conducting platform while maintaining the same blocking capabilities (Figure 1.4.4) On the other hand, one can optimize the off-state field distribution to achieve a larger breakdown voltage with the same drift region length, thus maintaining the same device resistance (Figure 1.4.4). Here, we investigate these two approaches and discuss the current state of the technology.

1. The conductivity of a semiconductor is the result of two main components, i.e. the carrier density (N_s for a 2DEG), which represents the number of mobile charges taking part in the conduction, and the mobility (μ), which describes how easily these charges can move. Thus, the 2DEG sheet resistance (R_{sh}) can be written as $R_{sh} = \frac{1}{q\mu N_s}$.

   To reduce R_{sh}, one can increase the carriers' concentration or their mobility. However, μ is determined, to a large extent, by the semiconductor structure and it is very challenging to increase, especially of a significant amount. On the other hand, achieving larger N_s is relatively easier, for instance by using barrier materials such as AlN or InAlN that present higher polarization than conventional $Al_{0.20}Ga_{0.8}N$.

Yet, obtaining a large N_s in a single channel structure typically reduces μ due to the increased scattering [42], setting a trade-off that ultimately limits the achievable reduction of the sheet resistance. In addition, a large carrier concentration increases the threshold voltage due to the more challenging electrostatic gate control and reduces the V_{BR} because of the more difficult electric field management.

Multi-channel heterostructures, in which multiple quantum wells with high-mobility two-dimensional electron gas (2DEG) channels are grown and stacked within the same semiconductor platform, have been proposed to address this issue [43]–[50]. The multi-channel heterostructure allows distributing a large number of carriers in several high-mobility parallel channels, overcoming the trade-off between the channel carriers' concentration (N_s) and their mobility (μ). This leads to a significant enhancement in N_s independently from μ and results in a considerable reduction of sheet resistance compared to conventional single quantum-well structures.

However, the adoption of multi-channel heterostructures for power electronics presents significant challenges, which are of fundamental importance for power devices. In particular, proper gate control and E-mode operation in these highly conductive 3D structures are yet to be demonstrated. Besides, achieving large breakdown voltage despite the large carrier density and the multiple channels demands novel field management solutions. Finally, proper passivation techniques to reduce current collapse in these devices are fundamental and require extensive investigation.

2. The off-state electric field in GaN HEMTs is highly non-uniform with a peak at the drain edge of the gate electrode, which significantly degrades the device's breakdown voltage (*Section 1.4.2*). In order to improve the field profile, field-plates (FPs) can be employed. Yet, the number of field plates that can be employed is limited and these structures cannot extend over the whole drift region. In particular, field plates significantly increase the complexity of the fabrication process and also result in large parasitic capacitance contribution, impacting the device switching losses. Finally, FPs cannot extend too close to the drain electrode as breakdown through the dielectric layer would occur.

   Thus, alternative methods are required to improve the off-state electric field distribution and increase the device's blocking performance. A possible strategy to obtain an ideally flat electric field profile consists of employing the Super Junction (SJ) concept, which was originally developed for Si devices. If one could achieve a balanced amount of electrons and holes with no fixed charge in the drift region, these mobile carriers could be depleted in the off-state resulting in a neutral depletion region and thus in a flat electric field profile. While in Si devices this is obtained by carefully tuning the doping concertation of *n*-type and *p*-type pillars, this is impossible in GaN due to the inefficient *p*-GaN doping and the absence of effective Mg implantation or high-quality *p*-GaN regrowth.

   Yet, the AlGaN/GaN lateral platform offers a unique alternative to conventional vertical SJs. In these structures, a two-dimensional electron and hole gas (2DEG and 2DHG) of equal carrier concentrations (N_s and P_s respectively) can be obtained naturally, thanks to the presence of matching polarization charges, enabling the realization of Polarization Super

Junctions (PSJs) [51]–[54]. The charge balance between the 2DEG and 2DHG, and the intrinsically matched polarization charges, can result in a neutral depletion region in the off-state, leading to a similar behavior to conventional, doping-based SJs.

Nevertheless, translating the matching polarization charges into mobile N_s and P_s of equal concentration is a challenging task due to the presence of ionized donor states at the top crystal surface, which provide electrons to the 2DEG and prevent the formation of a large-density 2DHG [55], [56]. Thus, key challenges of these structures such as achieving a small charge mismatch regardless of surface donor states and obtaining large N_s despite the thick cap remain unexplored. Besides, no thorough investigation of the behavior of intrinsic PSJ devices has been reported. For these reasons, the potential of intrinsic PSJ remains largely unexplored. A detailed quantitative analysis of the design and behavior of such devices is thus needed to address these challenges and is crucial for the development of the technology

1.4.4 High-Performance AlGaN/GaN Schottky Barrier Diodes

Power diodes are a fundamental component in most power converters' topologies are thus are particularly important for the development of the new GaN power technology. However, despite the great potential of GaN power devices, AlGaN/GaN SBDs have encountered a difficult development and, at the moment, SiC diodes represent the main wide-band-gap commercial solution.

The key challenge for GaN SBDs is the difficult management of the off-state electric field at the fragile Schottky barrier, which, if not properly treated, results in large leakage current and poor breakdown voltage. To address this problem, the voltage drop over the Schottky barrier should be minimized, which is typically achieved by using a field plate approach. While thick dielectric layers are usually employed for conventional FPs aimed at improving the channel depletion during the off-state, SBDs require the presence of a first FP after the Schottky contact with a very small pinch-off voltage (V_P) in order to reduce the voltage drop over the barrier. Yet, conventional field plate structures with no oxide already present a rather large negative V_P ~ - (4-5) V, which results in high off-state leakage for the SBD.

Recently, alternative approaches have been proposed to effectively address this issue. In particular, the use of a Tri-anode architecture [57]–[61] (Figure 1.4.5) or the partial recess of the AlGaN barrier [62], [63] have been shown to achieve FPs with V_P ~ -1 V, resulting in excellent DC performance with much reduced off-state leakage (Figure 1.4.5).

However, despite these promising results, these works focused only on the DC behavior of GaN SBDs while their dynamic performance is yet to be investigated. This is, however, of fundamental importance to assess their potential to improve the overall device efficiency and operate at high frequency. In addition, a thorough comparison with counterpart Si and SiC commercial devices is still lacking, which hides the full potential of GaN power devices compared to existing technologies. Finally, the GaN SBD behavior and performance in real circuit applications are still largely unexplored.

Besides, while Tri-anode structures and AlGaN barrier partial recess are effective in reducing the off-state leakage, they also require quite complex processing that is not yet widely available and may hinder

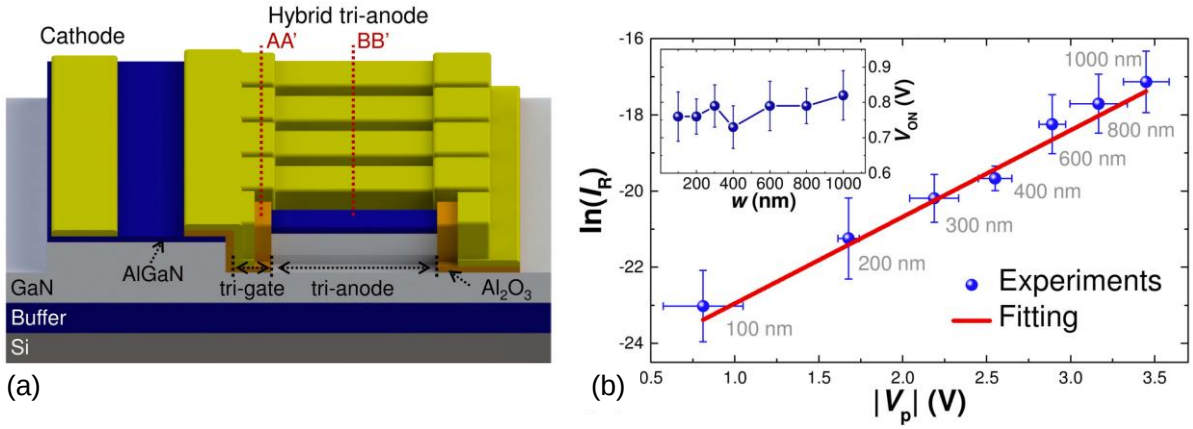


Figure 1.4.5: (a) Schematics of an AlGaN/GaN Tri-anode SBD [58] (b) SBD reverse leakage current as a function of the field plate pinch-off voltage (V_P), showing an exponential behavior. V_P can be effectively reduced by tuning the Tri-anode fin width [61].

their commercial adoption. In particular, Tri-anode devices need lithographic resolutions of about 200 nm [57]–[60] and SBDs with a partially recessed barrier require extremely precise control of the etching depth, which can be reproducibly achieved only by complex methods such as atomic layer etching [62], [63]. For these reasons, it is of great importance to investigate also alternative architectures based on currently available process technologies that could be directly adopted for commercialization.

1.4.5 Thermal Management of High-power Density GaN Devices

Thanks to its excellent material properties (*Section 1.2*), GaN has a great potential to dramatically reduce the footprint of power devices compared to conventional Si devices. Its large breakdown field enables shrinking significantly the drift region length for a certain breakdown voltage, thus reducing the device size and increasing its current capabilities. In addition, the shorter drift region, the high-mobility 2DEG, and the unipolar conduction in GaN lateral devices result in much-reduced switching losses. This enables GaN power devices to operate at high switching frequencies up to several MHz, thus considerably reducing the size of passive components and increasing the converter power density. Finally, the lateral architecture of GaN power devices enables the monolithic integration of serval devices on the same chip to realize ultra-compact power integrated circuits (ICs). These unique features open doors to power devices with unprecedented power densities and a much-reduced footprint.

Nevertheless, the ever-increasing power density of GaN power devices has resulted in unprecedented heat fluxes [64], which need to be properly managed. Excessive self-heating of the device results in a reduced component lifetime, degraded performance, and limited power density. In addition, the reduced device current capability due to self-heating requires paralleling several transistors for high-current applications, which increases the overall system cost and complexity.

Extracting such localized heat fluxes using conventional cooling approaches is extremely challenging. Typical thermal management solutions, such as forced-convection air-cooling, struggle to handle such large heat fluxes [65], and current alternative solutions like the use of high thermal conductivity substrates, e.g. SiC and diamond, are prohibitively expensive for widespread adoption. Thus, it is clear that novel thermal management solutions are fundamental to take full advantage of the

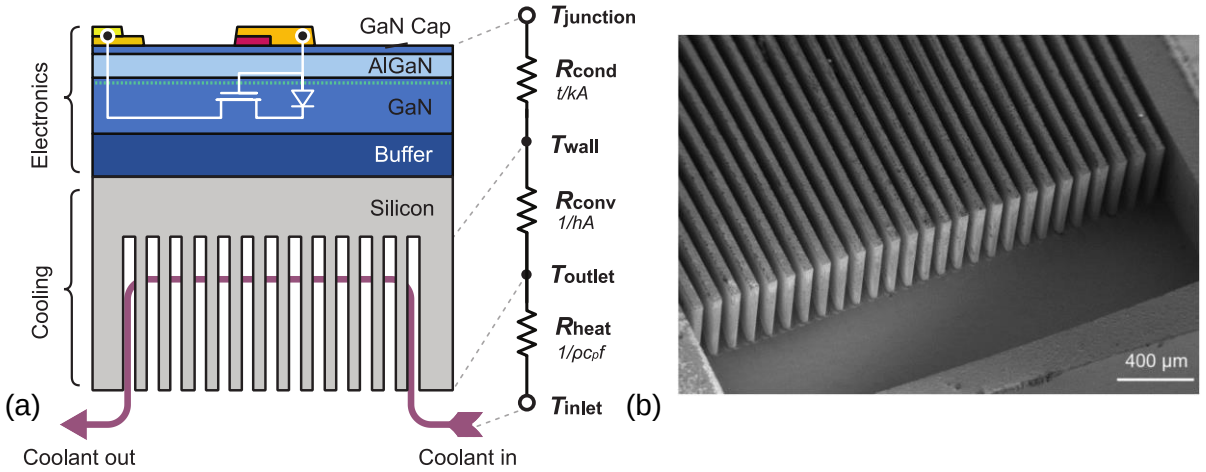


Figure 1.4.6: (a) Schematic illustration of the liquid-cooled GaN power device, where the silicon substrate functions as the cooling layer and the AlGaN/GaN epilayer provides the electronic properties [66]. (b) High aspect ratio microchannels etched in the device silicon substrate [66].

GaN power technology, whose development may otherwise be hindered by the poor thermal performance.

Instead of relying on high-thermal-conductivity substrates to spread to heat, a promising alternative is to take advantage of the cheap and large-area silicon substrate of GaN-on-Si structures (*see Section 1.3*) and transform it into a high-performance heat-sink able to handle and remove large heat fluxes (Figure 1.4.6). This technology is called embedded liquid cooling and was first proposed by Tuckerman and Pease [67], [68] in the ‘80s to manage the large heat fluxes in VLSI silicon circuits. Microchannels are etched directly in the silicon substrate and a coolant is flown to remove the heat (Figure 1.4.6). This technique enables bringing the coolant close to the heat source, thus avoiding the additional thermal resistance contribution linked to the package and the interface between the chip and the heat sink, while also increasing significantly the convective heat transfer (Figure 1.4.6 (a)). Overall, this enables extracting large heat fluxes without the need for aggressive heat spreading and large heat sinks.

While this approach has shown very promising results and has been extensively studied for silicon logic circuits [67]–[72] and for GaN-based RF applications [64], typical power devices present a vertical architecture, which prevents the micro-structuring of the substrate. For this reason, the integration of embedded liquid cooling in power devices is a rather unexplored field and its impact on the electrical and thermal performance of power transistors is unknown.

Yet, GaN-on-Si devices present a lateral device structure on a silicon substrate that is well-suited for deep etching, making it ideal for the integration of this technology. Further studies are required to show the potential of embedded liquid cooling as a thermal management solution for the GaN-on-Si power technology and its effect on both the electrical and thermal performance of GaN power devices.

1.4.6 GaN Devices for Harsh Environment Applications at Cryogenic Temperature

Gallium Nitride is an excellent semiconductor also for harsh environment applications. In particular, its large bandgap (3.4 eV compared to 1.12 eV for Si) enables operation at high temperatures without

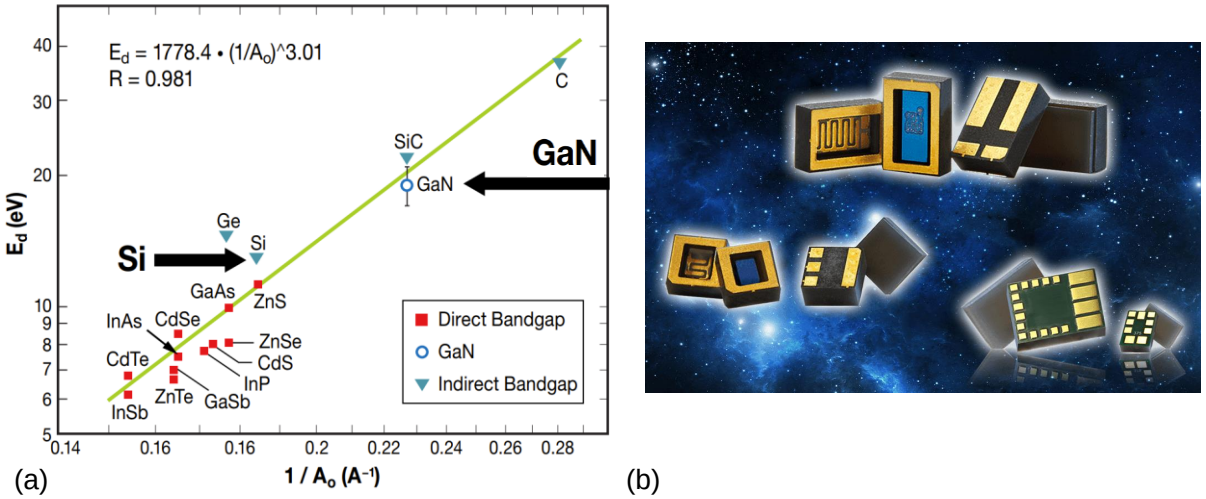


Figure 1.4.7: (a) Displacement energy as a function of the inverse of the lattice constant for various crystals [73]. (b) GaN power devices for space applications offered by EPC Space [74].

significant carriers thermal generation, and its strong atomic bonds (8.92 eV/atom for GaN compared to 2.34 eV/atom for Si [75]) results in high radiation tolerance [76] (Figure 1.4.7 (a)). Most importantly, thanks to its polar nature, GaN does not require doping to achieve a high density of free carriers, as is the case in conventional semiconductors. The absence of doping leads to much-improved stability in a wide range of temperatures and is particularly appealing for cryogenic applications in which doped semiconductors suffer from significant dopant freeze out.

Some of the most interesting examples of power electronics operating at cryogenic conditions are found in the space and aviation domain [77], [78]. GaN devices specifically targeted for space applications have recently been commercialized and by EPC Space [74] (Figure 1.4.7 (b)), among others, and major agencies, such as Nasa, are actively investigating GaN devices for their future missions [79], [80]. Other important applications in which the power conversion system is required to operate at cryogenic conditions can be found in superconducting machines such as superconducting magnets, energy storage systems, and superconducting motors [78], [81], [82]. While the power systems are typically thermally insulated and maintained at room temperature, this greatly increases their cost, size, and complexity. It would thus be highly beneficial to operate the power converter at cryogenic temperature, which however requires a clear understanding of the power devices' behavior in such conditions.

In particular, while some previous works have focused on the cryogenic characterization of a single commercial device (e.g. GaN Systems [79] and EPC [83]), these studies were typically performed down to 77 K, leaving the large temperature range below this value unexplored. Moreover, the low-temperature performance of common GaN HEMT architectures, such as Gate Injection Transistor (GIT) and Cascode, has never been reported, posing questions on their behavior in such conditions. Finally, it is still unclear how the device conduction, soft- and hard-switching losses vary at cryogenic temperature and which device architecture offers the best performance at such conditions. A thorough investigation and comparison of the performance of GaN commercial devices at cryogenic conditions are thus fundamental to providing guidelines for the design of power converters for cryogenic applications.

1.5 Thesis Outline

This thesis aims to overcome the challenges outlined in the previous sections and to open new fields of research for GaN power devices. The thesis is organized as follows:

Chapter 2 demonstrates the use of nanowire devices in combination with a Tri-gate architecture to achieve E-mode operation in AlGaN/GaN HEMTs while maintaining excellent on-state performance and large breakdown voltage.

Multi-Channel structures with multiple stacked 2DEGs are introduced to significantly increase the device's conductivity. By nanostructuring the gate region, E-mode operation is achieved despite the large carrier density, and the off-state electric field is properly managed, resulting in a large breakdown voltage in spite of the highly conducting structure. Thanks to this approach, multi-channel nanowire devices resulted in a more than fourfold decrease in $R_{ON,SP}$ with respect to the best-performing single-channel device with the same blocking performance and led to a very large high-power figure-of-merit of 3.8 $GWcm^{-2}$ for E-mode devices.

Finally, we demonstrate a novel surface passivation technology for multi-channel devices based on the conformal deposition of a low-pressure chemical vapor deposition (LPCVD) Si_3N_4 layer around the multi-channel fins. Such an approach led to a significant reduction of the dynamic on-resistance in multi-channel devices under large off-state voltages of 350 V and demonstrates that, in addition to the excellent DC performance, the multi-channel technology can offer reduced current collapse, unveiling the potential of this platform for power electronic applications.

Chapter 3 presents the potential of the Super Junction concept to improve the efficiency and reduce the footprint of AlGaN/GaN future power devices.

We introduce the concept of intrinsic Polarization Super Junctions (i-PSJ) and propose a simple yet robust platform that enables excellent charge matching for any surface condition, without relying on doping of the GaN cap. We show surface donor states as the origin of charge mismatch and provide a strategy to minimize their impact on the device performance. Simulated devices based on this structure show optimal carrier depletion with a flat electric field profile in the whole drift region. Finally, we investigate this concept in multi-channel structures, which enable to reduce the on-resistance without degrading the off-state performance, thus greatly improving the device figure-of-merit.

In order to show the full potential of i-PSJ, we propose a simple and yet accurate physical model to describe the main figures-of-merit of GaN lateral devices. We show that i-PSJs can result in up to a 10-fold decrease in specific on-resistance for the same breakdown voltage compared to HEMTs, which can be further improved by the use of multi-channel heterostructures. In addition, we demonstrate that i-PSJs result in a significant reduction of the R_{ON} x E_{oss} figure-of-merit both in the case of negligible and dominating parasitic contributions, thus leading to an improvement of both DC and switching losses in power conversion applications.

Chapter 4 investigates novel architectures for high-performance and fast-switching AlGaN/GaN Schottky barrier diodes.

The switching losses of Tri-anode SBDs are characterized, showing a more than 50% reduction in the device charge compared to conventional planar structure, confirmed both by capacitive and reverse-recovery measurements. Combined with the excellent DC performance, this results in a much improved $R_{ON} \cdot Q_{rr}$ figure-of-merit for Tri-anode devices with respect to conventional planar architectures.

The Tri-anode SBDs' excellent static and dynamic behavior is compared with state-of-the-art commercial Si and SiC devices showing much-improved performance. The potential of these devices in real circuit applications is demonstrated by realizing a diode-multiplier Integrated Circuit (IC), which included up to 8 monolithically integrated SBDs and operates as a high-frequency DC-DC magnetic-less boost converter. The IC performance and footprint are compared to the same circuit realized with discrete Si and SiC vertical devices, showing the potential of GaN power ICs for more efficient and compact power converters.

Lastly, we propose a simple AlGaN/GaN SBD planar architecture based on a *p*-GaN cap layer to achieve excellent off-state performance without the need for high lithographic resolutions or AlGaN barrier partial recess. By properly designing the AlGaN barrier and *p*-GaN cap, the voltage drop over the Schottky junction is effectively reduced while achieving a large carrier concentration in the access region. This results in good on-state performance along with a very low leakage current of ~1 nA/mm at 400V, which is maintained well below 100 nA/mm up to elevated temperatures of 150 °C. Most importantly, the proposed architecture relies on the well-established fabrication process of commercial *p*-GaN HEMTs and thus represents a promising and viable solution for future GaN diodes.

Chapter 5 addresses the thermal management of high power density GaN devices and ICs.

We demonstrate the integration of embedded liquid cooling on a 650 V, 50 mΩ GaN-on-Si commercial power device. We show no negative impact on the device DC or switching performance due to the embedded liquid cooling, which proves the robustness and validity of the technology. Besides, liquid-cooled devices exhibit more than 4× higher current capability and much-improved $R_{ON} \times E_{oss}$ figure-of-merit in a large output current range compared to forced-convection air-cooling, highlighting their potential for high-current applications. Finally, we compare deionized water and a dielectric fluid (3M Novec 7200) as coolants, revealing a trade-off between thermal performance and reliability during high-voltage operation.

In addition, we apply embedded liquid cooling to a GaN power IC realized by the high-performance Tri-anode SBDs presented in *Chapter 4*. Integrated liquid cooling led to a small temperature rise of only 0.34 K per watt of output power, enabling high power densities of 25 kW dm^{-3} for a temperature rise below 50 °C. This shows the potential of this approach to effectively manage the high-heat fluxes of GaN power ICs in which multiple components can be densely packed onto the same chip to increase the power density.

Appendix A investigates and compares the performance of GaN commercial power devices for cryogenic applications down to a temperature of 4.2 K.

We show that all of the tested devices can successfully operate at cryogenic temperature with an overall performance improvement. However, different GaN HEMT technologies lead to significant variations in device gate control and loss mechanisms, which are discussed based on the device structure. These results demonstrate the promising potential of the GaN technology for low-temperature applications and provide precious insights to properly design power systems operating under cryogenic temperatures and maximize their efficiency.

Chapter 6 draws the conclusion of the thesis and introduces future possible developments of the GaN power technology based on the results here presented.

2 Multi-Channel Nanowire Devices for Low On-resistance and Enhancement-mode Operation

2.1 Introduction

Enhancement-mode operation is an essential feature for power transistors, which is required to ensure fail-safe operation in case of a malfunctioning gate diving circuit or breakdown of the power device itself. As explained in *Chapter 1*, several methods have been proposed to achieve E-mode operation. The most common approaches comprise the use of a *p*-GaN cap-layer [24]–[28], or the AlGaN barrier recess in the gate region [31]–[35]. While positive V_{TH} has been successfully achieved and these methods are used in most commercial devices, the threshold voltage shift that can be obtained is normally limited thus requiring heterostructures with reduced N_s or introducing severe damages to part of the channel, which typically leads to degraded R_{ON} with respect to Depletion-mode (D-mode) devices and results in a V_{TH} vs R_{ON} trade-off.

Tri-gate devices in which the gate region is nanostructured into narrow nanowires conformably covered by the gate metal (Figure 2.1.1 (a-b)), offer a promising alternative solution to reach E-mode operation. While such architecture was first introduced for Si ultra-scale MOSFET in 2002 [84] to address the short channel effects, it was soon adopted for power devices. The first tri-gate GaN demonstration appeared in 2008 [85], followed by several other works which showed the numerous benefits of such architecture, such as the superior gate control, the large ON-OFF ratio, and small sub-threshold slope (*SS*), along with the reduced leakage current and the increased breakdown voltage [15]–[17].

The most interesting feature of the tri-gate is however its ability to modulate the device threshold voltage (V_{TH}) by simply tuning the nanowire width (w_{Nw}) ((Figure 2.1.1) (c)). Such an effect has been attributed to the partial AlGaN strain relaxation when patterned into fins and by the fin sidewalls depletion due to the side gate electrode [89]–[91]. This approach relies only on one lithography step to achieve positive threshold voltage and does not require any critical etching as for gate recess or *p*-GaN gates. However, devices employing this approach to reach E-mode operation typically show negative V_{TH} and suffer from performance degradation due to the small nanowires widths [92]–[95]. Novel approaches and further investigation of the physical mechanisms in narrow nanowires are required to further increase the threshold voltage to positive values and to resolve the performance degradation.

Besides achieving E-mode operation in conventional GaN HEMTs, the tri-gate technology can also enable novel devices architectures aimed at significantly enhancing the device performance. As discussed in *Section 1.4.3*, reducing the on-resistance is an effective way to reduce conduction losses and improve the efficiency of the device. Multi-Channel (MC) structures in which multiple 2DEG channels

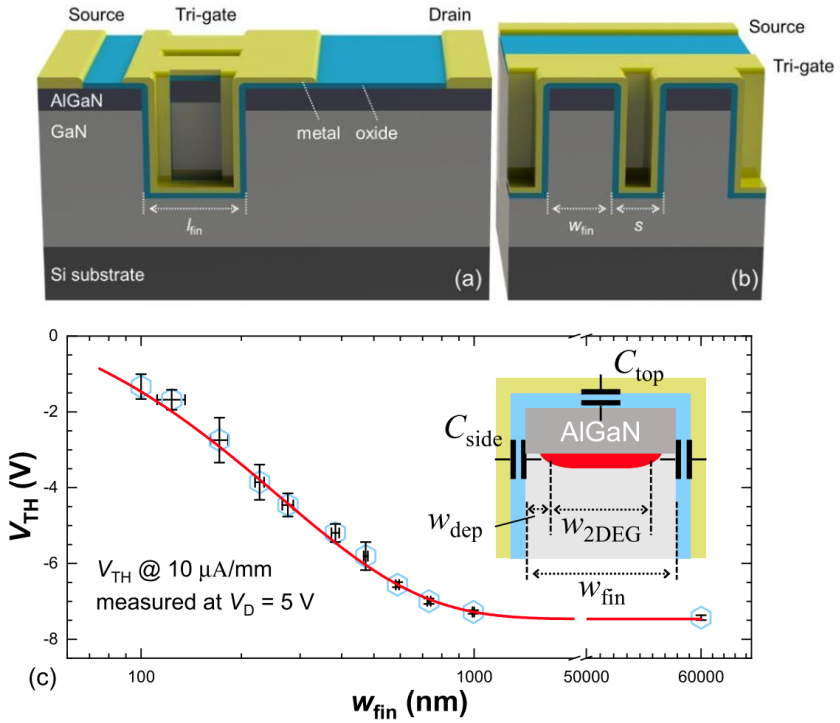


Figure 2.1.1: Schematics of (a) the tri-gate MOS-HEMTs and (b) its tri-gate region [96] (c) Dependence of V_{TH} on w_{NW}. The inset in (c) illustrates the effect of sidewall depletion in distributing the 2DEG across a fin [90].

are stacked on the same wafer have been recently proposed [91], [97]–[100], resulting in heterostructures with extremely high sheet carrier density above 1×10^{14} cm^{-2} and R_s down to 37 Ω/□ [99]. This enables a reduction of about 10 times in sheet resistance compared to conventional AlGaN/GaN single-channel heterostructures, which could lead to extremely high-efficiency power devices.

However, despite the promising potential of this platform, several challenges need to be addressed for the successful development of the multi-channel power technology. A major obstacle is represented by the poor top gate control over the buried channels, which greatly increases the leakage current, reduces the transconductance, and drastically limits V_{BR}. In addition, the large gate-to-channel separation leads to very negative $V_{TH,}$ which makes the use of such devices impossible in real applications. While conventional planar gates are not suitable to control the multiple channels since the gate potential is almost entirely shielded by the first channels, the integration of the tri-gate technology with the multi-channel platform would provide excellent control along with superior on-state performance. In addition, the tri-gate architecture could offer a way to reach E-mode operation, impossible to be achieved with standard planar techniques such as gate recess or *p*-GaN cap layer. Finally, novel approaches are required to manage the high off-state electric field in such highly conducting structures and avoid early breakdown of the device. Also under this point of view, the Tri-gate architecture can play an important role thanks to its ability to precisely tune the V_{TH} by simply modifying the nanowire width, which can enable a simple and effective design of FP structures in multi-channel devices.

In addition to achieving excellent DC behavior, the switching performance of GaN power HEMTs is of particular concern. As explained in *Section 1.4.2*, AlGaN/GaN power devices suffer from severe current collapse during high-voltage switching mainly due to electron trapping by surface states. While

this effect is typically addressed by depositing a surface passivation layer, the presence of the tri-gate architecture and of the multiple channels requires significant modifications to the device fabrication process and strongly influences the off-state electric field distribution, thus impacting the trapping mechanisms. Nevertheless, achieving proper passivation of multi-channel tri-gate devices and investigating their dynamic performance is of fundamental importance for the development of the multi-channel Tri-gate technology and requires further investigation and development.

This chapter is organized into three sections that address the aforementioned challenges.

1. In the first section, we investigate the use of nanowire devices to achieve E-mode operation in AlGaN/GaN single-channel heterostructures. By employing a large work-function gate metal, deposited over nanowires in the gate region, complete sidewall depletion and positive V_{TH} were achieved. In addition, a judicious design of the nanostructured gate geometry mitigated the performance degradation caused by the 2DEG removal, and also improved the device breakdown voltage by converting part of the gate electrode into a gate-connected field plate.

2. In the second section, we demonstrate multi-channel tri-gate HEMTs based on an AlGaN/GaN multiple channel heterostructure and a nanostructured gate region. We investigate in detail the design of the multi-channel platform, the electron transport and depletion in narrow multi-channel nanowires, and the approaches to achieve large breakdown voltage in highly conductive multi-channel power devices. Based on these results, we demonstrate E-mode multi-channel devices with very low on-resistance, much improved R_{ON}-vs-V_{TH} and R_{ON}-vs-V_{BR} benchmarks compared to the state-of-the-art, and best-in-class high-power figure-of-merit.

3. In the third section, we present multi-channel tri-gate power devices with reduced current collapse thanks to a high-quality Si_3N_4 conformal surface passivation layer. The detailed device fabrication process is reported and the impact of the tri-gate multi-channel architecture on the dynamic performance of power HEMTs is presented. Thanks to this approach, we demonstrate that multi-channel devices can be effectively passivated, offering reduced current collapse at high-voltage operation, which represents a key advance in the development of the multi-channel technology for power applications.

2.2 Nanowire-based E-mode Power GaN Transistors with Large Work-function Gate Metal

In this section, we present high-performance E-mode AlGaN/GaN MOS-HEMTs based on a large work-function gate metal. The large work-function gate metal stack enables complete sidewall depletion of the nanowires in the gate region and thus positive threshold voltage. In addition, we investigate the electron transport mechanisms in the nanowires structures and minimize the impact of the 2DEG removal on the on-state performance. Finally, we show an improved device breakdown voltage thanks to the conversion of part of the gate electrode into a gate-connected field plate.[1]

2.2.1 Device Structure and Fabrication

The devices were fabricated on a GaN-on-Si heterostructure consisting of 5.4 µm of buffer, 320 nm of unintentionally doped GaN (u-GaN) channel, 24.6 nm of $Al_{0.25}Ga_{0.75}N$ barrier, and 3.3 nm of u-GaN cap-layer. The electron concentration and mobility of the 2DEG from Hall measurements at room temperature were 1.3×10^{13} cm^{-2} and 1700 $cm^2/V{\cdot}s$, respectively. A scanning electron microscopy (SEM) image of the device channel is shown in Figure 2.2.1 (a). The fabrication process started with electron-beam lithography to define the mesa and nanowires in the gate region. The sample was then etched by Cl_2-based inductively coupled plasma etching (ICP) to a depth of 165 nm. The width of the 700 nm-long nanowires (w_{NW}) in the gate was varied from 15 nm to 40 nm to investigate the effect of sidewall depletion (Figure 2.2.1 (b)). The source and drain ohmic contacts were formed by a stack of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/Ni (60 nm)/Au (50 nm) and annealed at 780 °C for 30 s. 20 nm-thick SiO_2 was conformally deposited over the nanowires by atomic layer deposition (ALD) as a gate

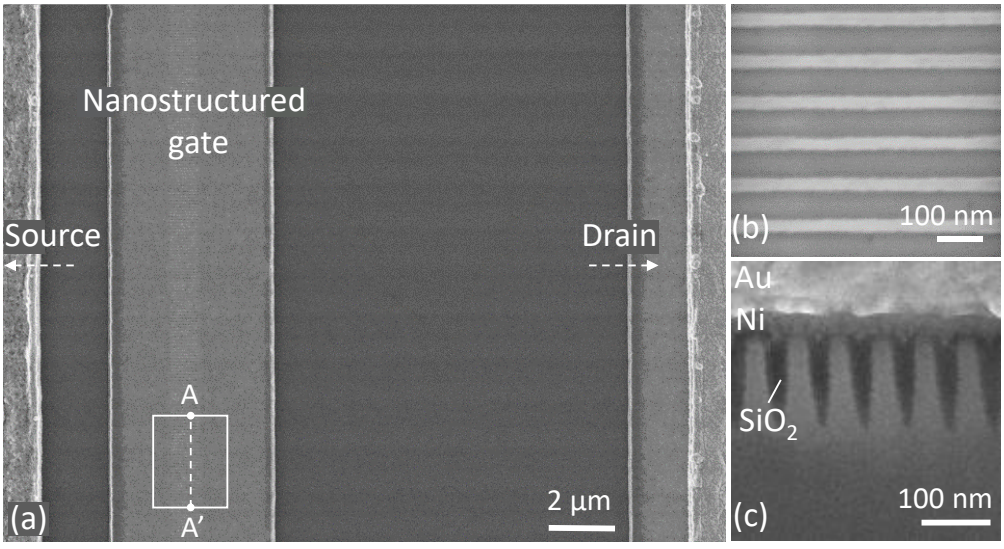


Figure 2.2.1: (a) Top-view SEM image of the device channel region, in which the nanostructured gate region is highlighted. (b) Zoomed SEM image of the nanowire region with 20 nm-wide fins and 50 nm spacing, before gate oxide deposition. (c) Cross-section SEM of the gate nanowires along the AA' line. The nanowires are conformally covered only by 20 nm ALD SiO_2, on top of which the Ni-Au or Pt-Au gate stacks were deposited.

[1] This section is based on **L. Nela**, M. Zhu, J. Ma, and E. Matioli, "High-performance nanowire-based E-mode Power GaN MOSHEMTs with large work- function gate metal", *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 439–442, 2019. © 2019 IEEE. **Contribution: First Author.**

dielectric. Two types of work-function metals deposited over the gate region were investigated: Ni/Au (50 nm/150 nm) and Pt/Au (50 nm/150 nm). A Focused Ion Beam (FIB) cross-section of the nanostructured gate region is shown in Figure 2.2.1 (c). Unlike in conventional tri-gate structures [86], [88], the gate metal did not penetrate too far in between nanowires due to the small spacing of 50 nm. The transistor dimensions are L_{GS} = 2 µm, L_G = 3 µm and L_{GD} = 10 µm, 15 µm and 20 µm. Device characteristics such as R_{ON}, I_{DS}, I_{OFF}, and transconductance (g_m) were normalized by the entire device footprint of 60 µm, rather than by the nanowire width.

2.2.2 Threshold Voltage Control and E-mode Operation

The I_{DS} versus V_{GS} transfer characteristics for transistors with standard Ni-Au gate metal stack are presented in Figure 2.2.2 (a). Reference devices with planar gates, co-fabricated on the same chip, presented normally-on behavior with V_{TH} = -4.8 V. A significant shift in V_{TH} of about 4 V was achieved by patterning 700 nm-long nanowires in the gate region with w_{NW} of 40 nm. As the nanowire width was reduced, V_{TH} further approached 0 V, which is mainly due to sidewalls depletion [89], [91], [94]. However, this is not enough to achieve fully E-mode operation, even for a nanowire width down to 15 nm (Figure 2.2.2 (a)). This result agrees well with previous works [87], [101] and illustrates the difficulty to achieve normally-off behavior relying solely on sidewall depletion.

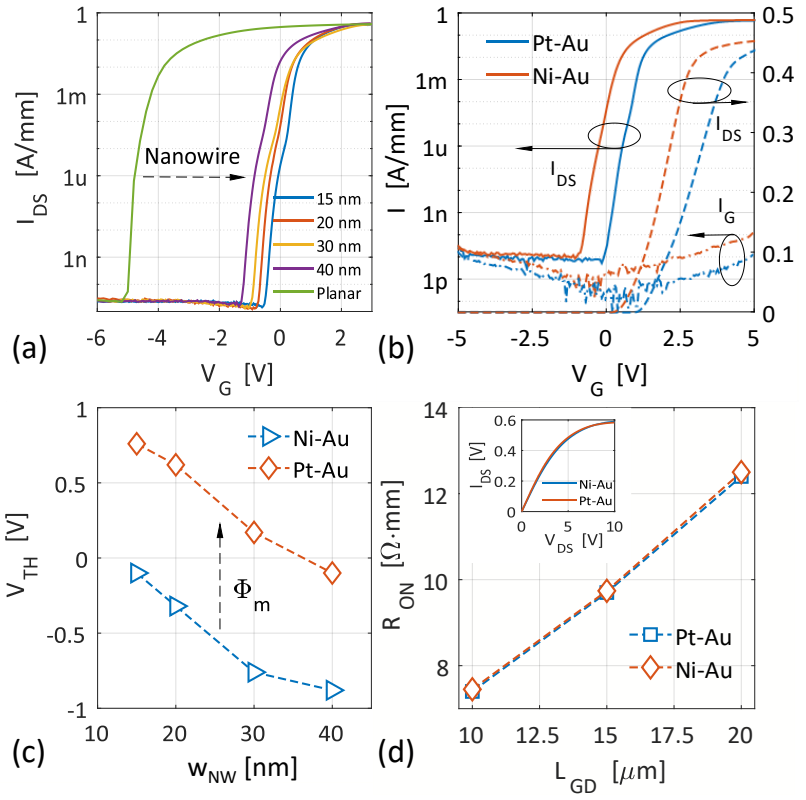


Figure 2.2.2: (a) Transfer curve for different nanowire width for Ni-Au gate stack at V_{DS}=5 V. As the nanowire width decreases, V_{TH} further approaches 0 V (b) Transfer curve comparison for the same nanowire width and spacing for Ni-Au and Pt-Au gate stack for V_{DS} = 5 V. The corresponding gate leakage for the two gate metal stacks is also shown. (c) V_{TH} (defined at 1 µA/mm) as a function of the nanowire width and gate metal. A positive V_{TH} shift of around 0.8 V is consistently observed between the two metal stacks for the different widths. (d) R_{ON} vs L_{GD} for the same nanowire width and spacing for Ni-Au and Pt-Au gate stack for a saturation gate voltage of 7 V. No difference in R_{ON} is observed between the gate metals. Inset: typical output curves for L_{GD}=10 µm for Ni and Pt gates.

To further shift V_{TH} to positive values, an additional mechanism based on the use of a large work-function (ϕ_m) gate metal was deployed. While a similar method has been proposed for *p*-GaN HEMTs [26], [102], its effect in the presence of a gate oxide requires additional studies. For a MOS-HEMT, the expression of V_{TH} is linearly dependent on the barrier height ϕ_B between the metal and the gate dielectric [30], [103], which can be increased by selecting a gate metal with larger ϕ_m. Indeed, neglecting bulk oxide and interface, the threshold can be expressed according to eq. 2.1 ([30], [103]):

$$V_{TH} = \frac{\phi_B}{q} - \frac{\Delta E_C}{q} - \frac{\phi_f}{q} - q\frac{t_b}{\varepsilon_b} Q_{GaN/AlGaN} - q\frac{t_{ox}}{\varepsilon_{ox}}(Q_{GaN/AlGaN} + Q_{Oxide/AlGaN}) \qquad 2.1$$

where ϕ_B is the metal-oxide barrier height, q is the electron charge, ΔE_C the conduction band offset the between GaN and the oxide, ϕ_f the energy difference between the intrinsic Fermi level and the conduction band edge of the GaN channel, t is the thickness, ε is the permittivity, and the subscripts *ox* and *b* refer to the oxide (SiO_2) and the barrier (AlGaN). $Q_{GaN/AlGaN}$ and $Q_{Oxide/AlGaN}$ are the charge densities at the oxide/AlGaN and the AlGaN/GaN interfaces. Since $\phi_B = \phi_m - \chi_s$ (where χ_s is the oxide electron affinity), its value can be adjusted acting on the metal work-function and a higher work function is expected to positively shift the threshold voltage.

To confirm this prediction, Pt-Au and Ni-Au gate stacks were deposited on co-fabricated devices and compared. The larger work-function of Pt (5.64-5.91 eV) [104] compared to that of Ni (5.04-5.35 eV) [105] resulted in a positive V_{TH} shift of about 0.8 V (Figure 2.2.2 (b)), which was consistent for all nanowire widths investigated (Figure 2.2.2 (c)), resulting in E-mode operation for devices with nanowire width below 30 nm. The observed shift agrees well with the work-function difference between the two metals and suggests that SiO_2/AlGaN interface Fermi level is unpinned, which is in agreement with Ref. [106]. In addition, the larger Pt work-function leads to a decrease of the forward gate leakage of about one order of magnitude (Figure 2.2.2 (b)). No difference in R_{ON} versus L_{GD} was observed between Ni-Au and Pt-Au gate stacks (Figure 2.2.2 (d)).

2.2.3 Device Performance and Benchmark

To determine the influence of w_{NW} on the device performance, R_{ON} and $I_{DS,\,SAT}$ were extracted from the device output curves and plotted versus their filling factor ($FF = w_{NW} / w_{Period}$) (Figure 2.2.3). No clear degradation was observed for *FF* varying from 0.45 to 0.23 since a decrease in the *FF* leads to a larger number of nanowires in the gate region, which enhances sidewall conduction and compensates

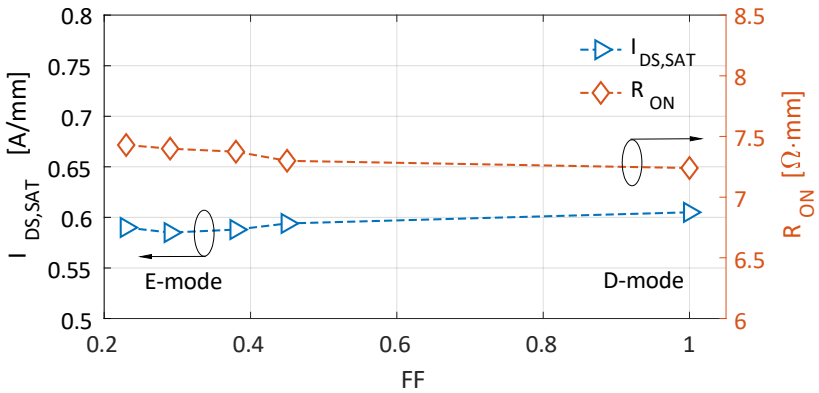


Figure 2.2.3: On-resistance (R_{ON}) and saturation current $I_{DS,\,SAT}$ versus filling factor (*FF*). The planar gate corresponds to *FF* = 1. A minor degradation in R_{ON}, smaller than 3%, is observed for the nanostructured gate devices.

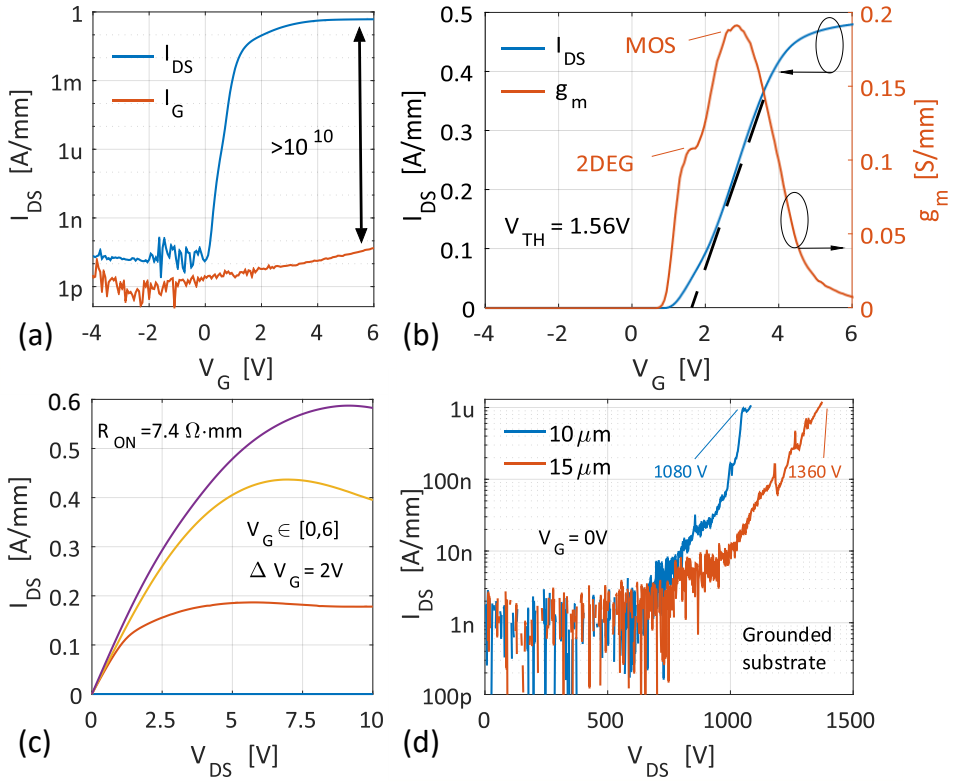


Figure 2.2.4: (a) Device transfer characteristic in logarithmic scale and the corresponding gate leakage for V_{DS} = 5 V. V_{TH} defined at 1 μA/mm is 0.64 V while the Subthreshold Slope (SS) is 110 mV/dec. (b) Linear scale transfer curve and transconductance g_m for V_{DS} = 5 V. V_{TH} from linear extrapolation is 1.56 V. g_m shows two convoluted peaks corresponding to conduction through the nanowire 2DEG and the MOS channel at the nanowire sidewalls (c) Output characteristics with V_G ranging from 0 V to 6 V with ΔV_G=2 V. (d) Breakdown characteristics for L_{GD} of 10 μm and 15 μm. The breakdown voltage is defined at I_{DS} = 1 μA/mm. All the device characteristics have been normalized by the total device footprint (60 μm).

for the loss of 2DEG due to etching. Even with respect to a planar gate device (FF = 1), the increase in R_{ON} due to the narrow nanowires in the gate is minor (~ 3%) (Figure 2.2.3). This is a remarkable result that offers large freedom in device design, as the nanowire width mainly affects the V_{TH} without degrading significantly the device output characteristics.

The transfer curve for a typical Pt-Au nanostructured device with w_{NW} of 20 nm and L_{GD} of 10 μm is shown in Figure 2.2.4 (a-b), presenting V_{TH} of 0.64 V at I_{DS} = 1 μA/mm, while from the linear extrapolation in linear scale, V_{TH} is 1.56 V. Thanks to the small gate dielectric leakage, the ratio of drain to gate current at V_G = 6 V is still $>10^{10}$. Although the gate metal does not fill the trenches between nanowires, as in typical tri-gate structures, the gate control is excellent with an ON/OFF ratio > 10^{10}, subthreshold slope (SS) of 110 mV/dec, large transconductance peak of 190 mS/mm and ultra-small leakage currents. The g_m curve exhibits two convoluted peaks at positive V_G corresponding to the conduction contribution from the 2DEG in the nanowire top layer and the MOS channel at the nanowire sidewalls (Figure 2.2.4 (b)). The transfer curve hysteresis from double sweep measurement was 0.35 V for V_G up to 3 V along with interface trap density D_{it} of about 1.3 × 10^{12} cm^{-2} eV^{-1} extracted for the subthreshold slope [31]. The output characteristics of the device shown in Figure 2.2.4 (c), reveals a R_{ON} of 7.4 Ω·mm for L_{GD} of 10 μm, corresponding to a very small $R_{ON, SP}$ of 1.33 mΩ·cm^2 (considering a 1.5 μm transfer length for each ohmic contact).

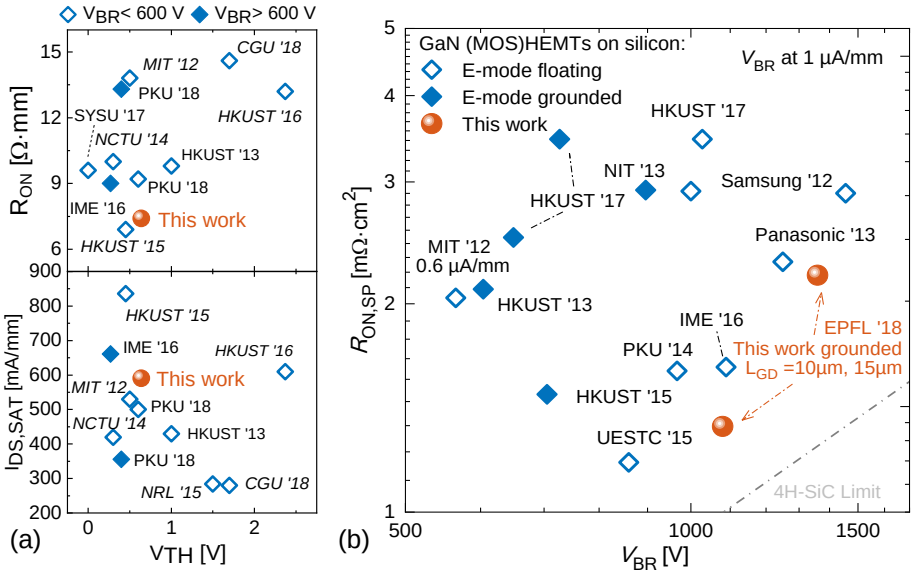


Figure 2.2.5: (a) R_{ON} and $I_{DS,\,SAT}$ versus V_{TH} benchmark for the presented devices compared with E-mode GaN-on-Silicon (MOS)HEMTs. Both V_{TH} and V_{BR} are defined for a current I_{DS} of 1 μA/mm. Devices presenting a large breakdown > 600 V are highlighted in solid blue. (b) $R_{ON,\,SP}$ vs V_{BR} benchmark for the presented devices against state-of-the-art GaN E-mode (MOS)HEMTs on Silicon. V_{BR} results determined with a grounded substrate are presented in solid blue. For a fair comparison, literature results with unspecified R_{ON}, $I_{DS,\,SAT}$, or I_R were not included.

The V_{BR} of these devices, defined at 1 μA/mm, was extracted for a V_G of 0 V with a grounded substrate (Figure 2.2.4 (d)), resulting in 1080 V and 1360 V for L_{GD} of 10 μm and 15 μm, respectively. The V_{BR} for L_{GD} 15 μm was limited by the vertical buffer V_{BR} of 1350 V, determined separately from 2 terminal breakdown measurements. The devices were then benchmarked against state-of-the-art E-mode GaN-on-Si (MOS)HEMTs, comparing $V_{TH,}$ R_{ON}, and $I_{DS,SAT}$ (Figure 2.2.5 (a)), and V_{BR} and $R_{ON,SP}$ (Figure 2.2.5 (b)). It is noteworthy that the R_{ON} of these nanowire-based devices was among the lowest values compared to E-mode GaN devices in the literature. This resulted in an excellent high-power FOM of 877 MW/cm^2 for L_{GD} of 10 μm.

In this section, we demonstrated high-performance E-mode AlGaN/GaN MOS-HEMTs based on a large work-function gate metal, deposited over nanowires in the gate region, which led to complete sidewall depletion and positive V_{TH}. In addition, a judicious design of the nanostructured gate geometry mitigated the performance degradation caused by the 2DEG removal, and also improved the device breakdown voltage by converting part of the gate electrode into a gate-connected field plate. This resulted in state-of-the-art E-mode devices with positive V_{TH} > 0.6 V at 1 μA/mm, low $R_{ON,\,SP}$ of 1.33 mΩ·cm^2, large I_{DS} up to 590 mA/mm, and high V_{BR} of 1080 V with a grounded substrate, which shows the potential of this technology for power applications.

2.3 High-Performance E-Mode Multi-Channel Power Transistors

AlGaN/GaN devices have shown great potential for efficient power conversion applications thanks to the excellent GaN material properties. However, despite the recent progress, their performance is still far from the theoretical limits of the material [41], as discussed in *Section 1.4.3*. The key challenge is to reduce the device resistance in the on-state (R_{ON}) while maintaining high voltage blocking capability (V_{BR}) in the off-state, which is typically summarized in a device figure-of-merit proportional to V_{BR}^2/R_{ON} [41], [107]. R_{ON} is ultimately limited by the semiconductor mobility (μ) and carrier density (N_s), whose product defines the channel electric conductivity. While μ is determined, to a large extent, by the semiconductor structure, increasing N_s is a much more effective approach to reduce the R_{ON}. However, a large N_s typically reduces μ [42], increases the threshold voltage (V_{TH}) due to the more challenging electrostatic gate control [108], and reduces the V_{BR} because of the more difficult electric field management [109].

A promising approach to address the N_s vs μ trade-off is with the use of multi-channel heterostructures [108]–[113], in which several barrier/channel layers are stacked to achieve multiple 2DEGs (Figure 2.3.1 (a-b)). The distribution of a large number of carriers in several high-mobility parallel channels enables increasing N_s without degrading μ. This leads to a significant enhancement in N_s independently from μ, and results in a reduction in sheet resistance (R_{sh}) with respect to conventional single quantum-well structures (Figure 2.3.1 (c)). While these structures have been proposed for RF applications [45], [100], [114], their use for power devices depends on very different requirements, which need to be separately addressed. In particular, enhancement-mode (E-mode) operation, large blocking voltage capabilities with reduced leakage current, and good stability during switching operation are fundamental features for power devices, which require novel solutions on a multi-channel platform.

In this section, we report multi-channel nanowire-based HEMTs, relying on a multiple channel heterostructure and a nanostructured gate region. The multi-channel heterostructure allows distributing

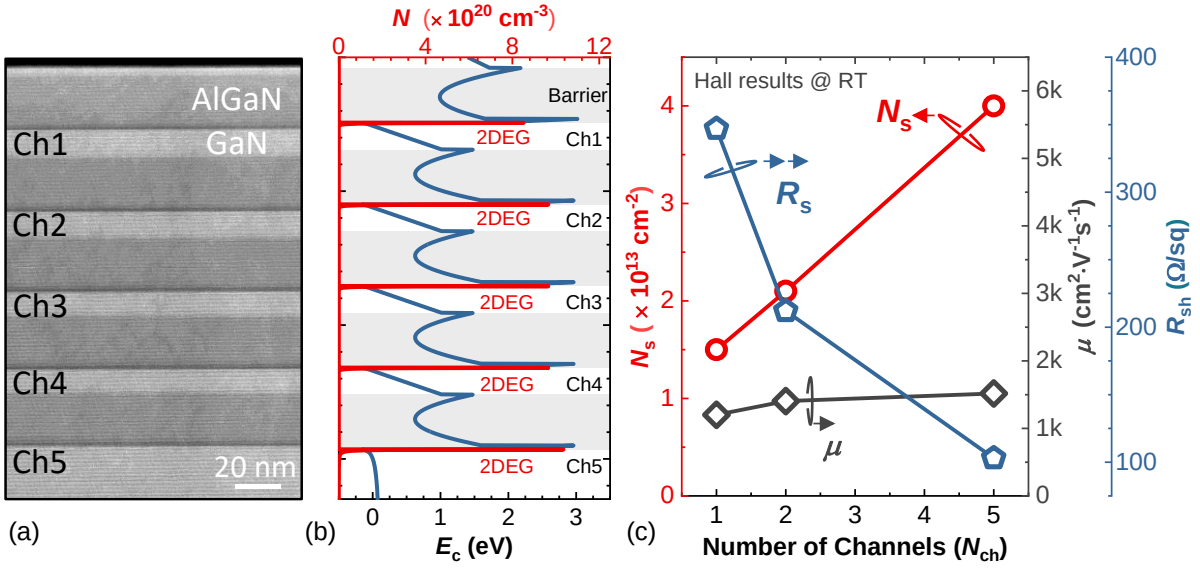


Figure 2.3.1: (a) HAADF STEM image of multi-channel AlGaN/GaN heterostructure with five parallel channels, whose simulated energy band diagram is shown in (b). (c) Dependence of the N_s, μ, and R_{sh} on the number of channels (N_{ch}), which were grown on sapphire substrates with undoped $Al_{0.3}Ga_{0.7}N$ barrier layers.

a large number of carriers in several high-mobility parallel channels, overcoming the major semiconductor trade-off between the channel carrier concentration (N_s) and their mobility (μ). The nanostructured gate [108], [109] provides simultaneous control of all the embedded channels and allows achieving E-mode operation despite the large carrier density. Finally, nanostructuring the gate region enables to effectively manage the large off-state electric field, leading to devices with reduced leakage current and large breakdown voltage in combination with very low on-resistance. [1]

2.3.1 Device Architecture and Fabrication

The device fabrication started with e-beam lithography to define the nanowires and mesa of the device using hydrogen silsesquioxane (HSQ) as a resist (see *Appendix C* for the detailed process flow). The HSQ was converted into SiO_x by the electron beam and then used as the hard mask for nanowires and mesa etching. Proximity error correction techniques were used to properly adjust the electron dose and achieve dense arrays of nanowires. The mesa and nanowires were patterned by Ar/Cl_2 inductively coupled plasma (ICP) dry etching with a depth of 250 nm. After that, 5 cycles of O_2 plasma/HCl treatment was implemented to reduce the damages caused by the dry etching, especially at the nanowire sidewalls. In each of the cycles, the devices were exposed to O_2 plasma for 1 minute in a barrel plasma stripper, at a power of 600 W, and then dipped into 37% HCl solution for 1 minute. During this process, the remaining HSQ-based SiOx from the etching served as the mask to protect the surface of the heterostructures from the plasma and was later removed by buffer oxide etching (BOE). Then ohmic metals stack (Ti/Al/Ti/Ni/Au) was evaporated in source/drain regions, and alloyed at 780 ºC for 30 seconds in N_2 atmosphere. 25 nm of SiO_2 were deposited by atomic layer deposition as the gate

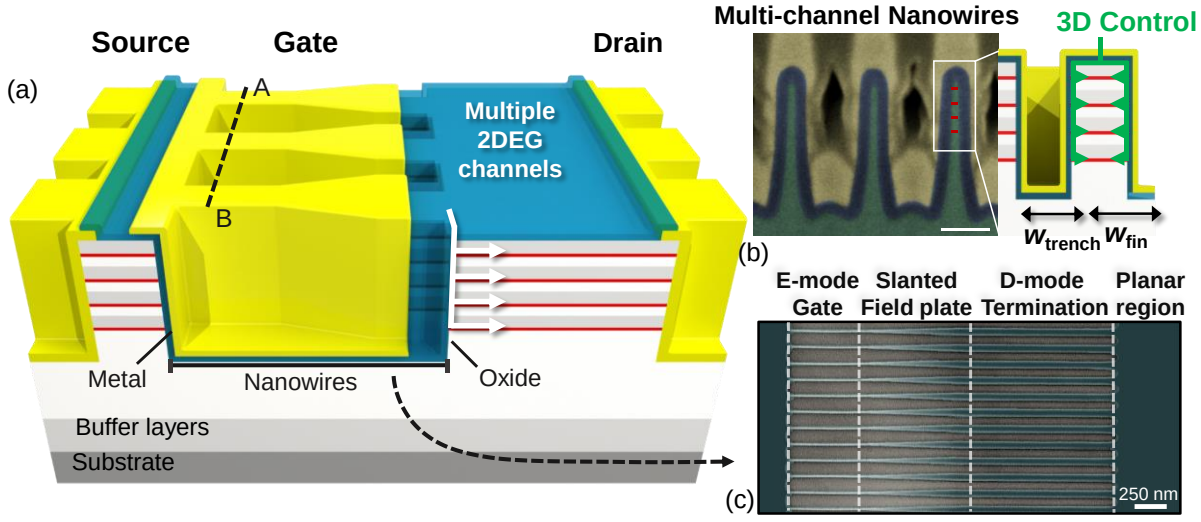


Figure 2.3.2: (a) Three-dimensional schematics of the proposed multi-channel device, featuring multiple parallel channels, to yield extremely low R_{ON}, controlled 3-dimensionally by a tri-gate electrode. The tri-gate is terminated in the nanowire region, rather than on the planar region, to better distribute the electric field and result in high V_{BR}. (b) FIB cross-section and schematics of the multi-channel nanowires covered by the tri-gate structure along the AB line in figure (a). The tri-gate enables a simultaneous 3D control over all the multiple channels in the nanowire. The scale bar is 100 nm. (c) Top SEM image of the nanostructured gate area (before the gate oxide and electrode deposition) which includes, starting from the source side, an e-mode region achieved by 15 nm-wide nanowires, and a slanted region terminated on 100 nm-wide d-mode nanowires for optimal electric field management.

[1] This section is based on **L. Nela** *et al.*, "Multi-channel nanowire devices for efficient power conversion", *Nature Electronics*, vol. 4, pp. 284–290, 2021. **Contribution: First Author**

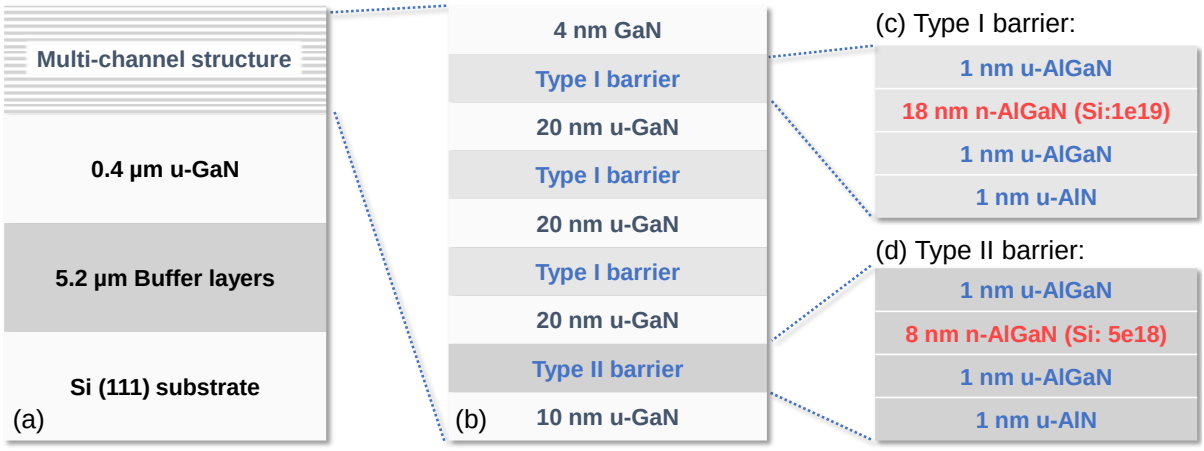


Figure 2.3.3: (a)-(d) Schematics of the design of the multi-channel AlGaN/GaN structure grown on a 6-inch Silicon substrate

dielectric, which was selectively removed by wet etching in source/drain regions to open the contacts. Finally, the gate electrode was defined by e-beam lithography using a double layer PMMA resist, followed by the deposition of a Pt (40 nm) - Au (100 nm) metal stack by evaporation.

Figure 2.3.2 outlines the 3D and cross-sectional schematics of the devices, together with the SEM top view of the nanowire region. The multi-channels are structured into nanowires in the gate region of the device, on which a 3-dimensional gate electrode (tri-gate) [31], [86] is formed to control the parallel channels through the sidewall portions of the nanowire (Figure 2.3.2 (b)). The nanowire width on the source side is tuned to shift the V_{TH} to positive values and achieve enhancement-mode operation, which is an essential requirement for power devices and extremely challenging to achieve in high conductivity materials. The drain-side termination of the nanowire is designed with an angled shape to form a slanted field plate that effectively distributes the high electric fields (Figure 2.3.2 (c)), resulting in a large V_{BR}.

2.3.2 Design of the Multi-Channel Heterostructure

Multi-channel nanowire MOSHEMTs were realized on a 4x-channel AlGaN/GaN epitaxy grown on a silicon substrate. This structure takes advantage of the excellent material capabilities of GaN for power devices integrated on large-area Si substrates through heteroepitaxy [17], [41], rendering a cost-effective platform that has a great prospect for efficient energy conversion [115]–[117]. The heterostructure was carefully designed to yield low R_{sh} in a small thickness, which is important to facilitate the fabrication of tri-gates around the nanowires, and also results in a negligible increase in epitaxial growth time and cost. Figure 2.3.3 (a) and (b) show the schematic of the structure containing 4 channels, in which the top 3 channels were formed by 20 nm $Al_{0.25}GaN$ barrier layers, selectively doped with a Si concentration of 1×10^{19} cm^{-3} (Type I) (Figure 2.3.3 (c)), followed by 1 nm AlN spacer and 20 nm-thick GaN channel layers. The bottom channel consisted of a 10 nm $Al_{0.25}GaN$ barrier, selectively doped with Si concentration of 5×10^{18} cm^{-3} (Type II) (Figure 2.3.3 (d)). This design resulted in a low R_{sh} of 83 ohm/sq and a large N_s of 3.9×10^{13} cm^{-2}, which is nearly 4-times higher compared to conventional AlGaN/GaN single-channel structures. Thanks to the carrier spreading in the four channels, a very high μ of 1930 $cm^2 \cdot V^{-1}s^{-1}$ was achieved despite such high N_s, rendering a significant enhancement in channel conductivity over counterpart single-channel structures, even when compared

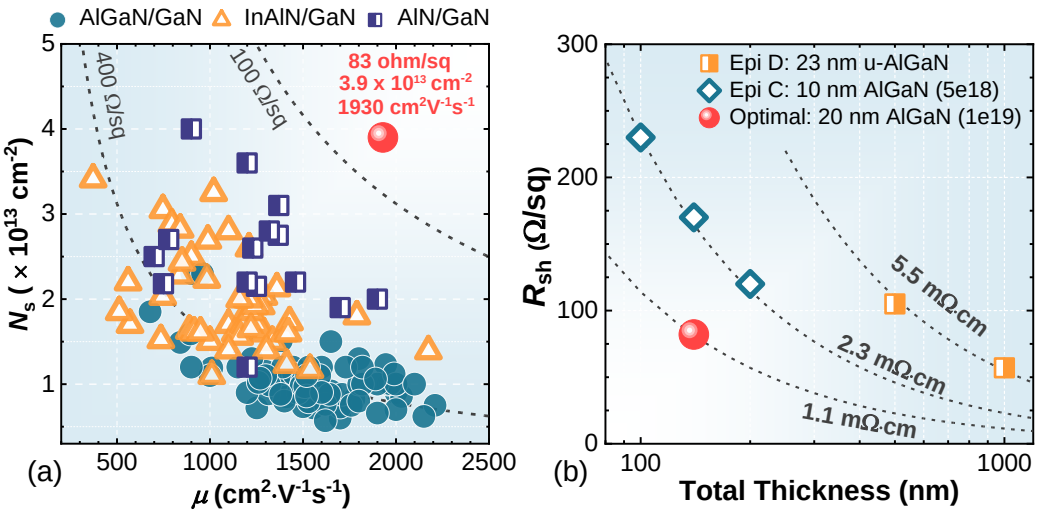


Figure 2.3.4: (a) Benchmark of the sheet resistance (R_{sh}) of the 4-channel heterostructure in this work against conventional single-channel GaN-based heterostructures in the literature, with AlGaN, InAlN, and AlN barriers. High μ of 1930 $cm^2 \cdot V^{-1}s^{-1}$ was achieved in combination with a large N_s of 3.9 x 10^{13} cm^{-2}, resulting in R_{sh} of 83 Ω/sq. (b) Dependence of R_{sh} on the heterostructure thickness in multi-channel structures having different barrier thickness and doping. The optimized design resulted in a very low R_{sh} of 83 Ω/sq with a total heterostructure thickness of only 130 nm.

to different barrier materials (Figure 2.3.4 (a)). In addition, after optimizing the epitaxial structure (Figure 2.3.4 (b)), the small R_{sh} was achieved using only 4 channels with a small total thickness of ~130 nm, thanks to the Type I barrier layers. This facilitates the tri-gate fabrication by reducing the aspect ratio of the nanowires. The bottom barrier was thinner and less doped to enable the control of the bottom-most channel, which is the farthest from the top gate and the most prone to possible punch-through in the OFF state.

2.3.3 Gate Control and Enhancement-Mode Operation

Such excellent conductivity achieved with multi-channel structures would be of little value unless it can be electrostatically controlled and modulated. Conventional planar gate electrodes cannot turn off all the embedded multi-channels due to the electric field shielding from the top channel to the ones underneath and to the large gate-to-channel distance. The tri-gate structure around the multi-channel nanowires [45], [100], [108] offers instead a superior electrostatic control thanks to its 3D architecture, which enables simultaneous side gate control on all of the embedded channels. As shown in Figure 2.3.5, the planar-gate devices could not be turned off even at a high gate voltage (V_G) of -50 V. In contrast, the tri-gate is far more effective in controlling the multi-channel structures and results in a high I_{ON}/I_{OFF} ratio ~ 10^{10}. In addition to pinching off the channels, the tri-gate enabled the simultaneous modulation of all the parallel 2DEGs. The flat and small transconductance (g_m) characteristic in wide nanowires, exhibiting multiple peaks, is caused by the successive turn-on of the parallel channels by V_G (Figure 2.3.5). However, in narrow nanowires (50 nm and below), the distinct peaks merged into a single large and sharp peak, indicating the simultaneous modulation of all parallel channels thanks to the dominant sidewall gate control, relative to the top gate (for more details on the nanowire width uniformity and interface quality please refer to *Appendix E*).

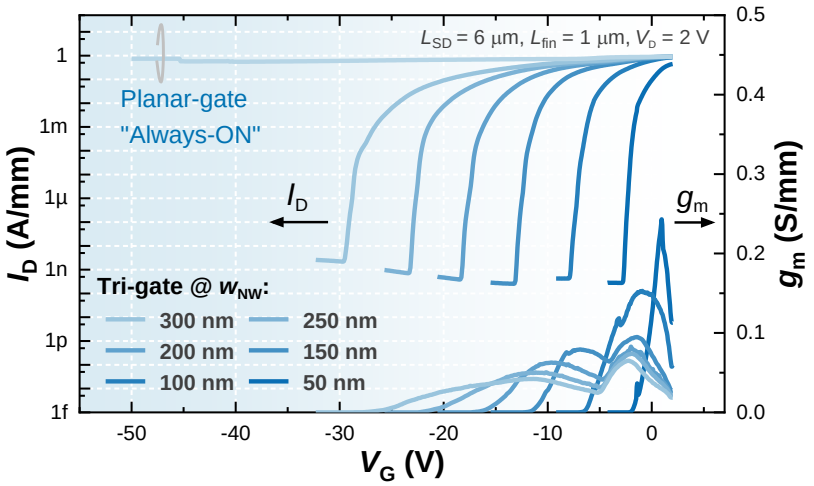


Figure 2.3.5: Transfer characteristics of multi-channel MOSHEMTs based on a planar gate and on tri-gates with different w_{NW}.

Besides providing excellent electrostatic control on the multi-channel heterostructure, the tri-gate architecture enables tuning the device V_{TH} by changing the width of the nanowires (w_{NW}), as shown by the drastic decrease of V_{TH} when w_{NW} was reduced (Figure 2.3.5). This is due to the enhanced tri-gate control and the sidewall depletion contribution in narrow nanowires. However, achieving positive V_{TH} in such high-conducting structures is challenging and requires further investigation of sidewall depletion in multi-channel nanowires. To determine the minimum nanowire width required to achieve E-mode operation, the *I-V* characteristics of Fat-FET having the whole drift region patterned with nanowires (bottom inset in Figure 2.3.6 (a)) was measured, from which the nanowire conductance (G_{NW}) was extracted (Figure 2.3.6 (a)). By linear fit of G_{NW} versus the nanowire width (w_{NW}), a nanowire sidewalls depletion (w_{Depl}) of 16.5 nm was calculated for gate voltage (V_G) of 0 V. As V_G increased, w_{Depl} decreased showing the effective gate control over the nanowire (top inset in Figure 2.3.6 (a)). The value of the depletion width indicates the minimum nanowire width to achieve E-mode operation since for $w_{NW} < 2w_{Depl}$ the depletion regions from the two sidewalls merge in the center and eliminate the 2DEG (Figure 2.3.6 (b)).

While in general a much higher gate voltage is required to turn off a multi-channel nanowire with respect to a single-channel one due to its larger carrier density, for small nanowire widths such a

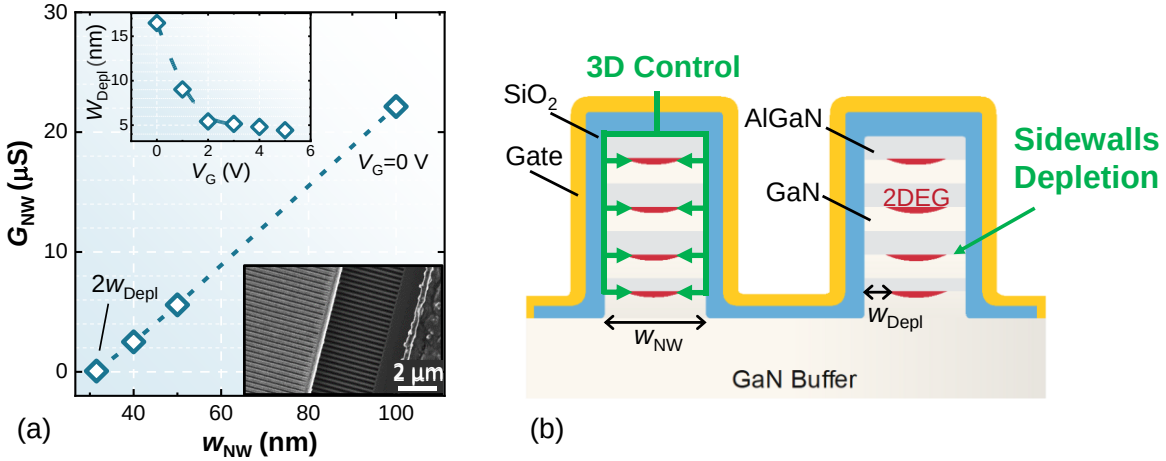


Figure 2.3.6: (a) Extraction of the multi-channel nanowire sidewalls depletion by using the conductance method. (b) Cross-sectional schematics of the tri-gate region and the different mechanisms depleting the multiple 2DEGs to achieve E-mode operation.

difference becomes smaller and multi-channel devices show very similar V_{TH} with respect to the single-channel counterpart for w_{NW} below 50 nm, despite the much larger N_s (Figure 2.3.7 (a)). This is due to the predominant side gate control and to the strong sidewalls depletion at such narrow widths, which is similar for multi- and single-channel nanowires.

The evaluation of the sidewalls depletion width is consistent with the device transfer curves, which indicate 30 nm as the minimum nanowire width to achieve positive V_{TH} (Figure 2.3.7 (b)). To further shift V_{TH} to positive values, the conventional Ni-Au gate metal stack was replaced by a Pt-Au gate metal (similarly to what was presented in *Section 2.2*), resulting in a threshold voltage increase of about 0.5 V, with consistent behavior for different w_{NW} (Figure 2.3.7 (b)). The use of high work-function Pt metallization was crucial to shift the V_{TH} to more positive values, which is of great importance for the fail-safe operation of power devices. Despite the high N_s of 3.9×10^{13} cm^{-2} in the epitaxy, a V_{TH} of +1.8 V evaluated by linear extrapolation of the I_D-V_G curve (+0.85 V at 1 µA/mm) was achieved, along with a low I_{OFF} of only 57 pA/mm at V_G = 0 V and a high ON/OFF ratio over 10^{10}, revealing excellent E-mode operation (Figure 2.3.7 (c)).

In addition, excellent stability of the device V_{TH} was demonstrated both during high-frequency switching by gate lag measurements [118] and during high-temperature operation up to 150 °C. Figure 2.3.8 (a) shows the schematics of the gate lag measurement employed to determine the V_{TH} stability of the device. First, the device is stressed for a time t_{off} = 5 ms during which a quiescent gate voltage $V_{G,q}$ is applied to cause trapping in the gate stack. The quiescent drain voltage $V_{D,q}$ is 0 V to avoid any drain lag contribution or device heating. Then the gate voltage V_G is set to 7 V and the drain voltage V_D to 1 V for a short time t_{on} = 5 µs, during which the drain current (I_D) is measured. The measured I_D is normalized to the value obtained at $V_{G,q}$ = 7 V, i.e. when the gate voltage is kept constant and thus no stress is applied. Trapping in the gate stack and instability of the device V_{TH} result in a variation of the measured I_D depending on the value of the applied $V_{G,q}$.

A negligible gate lag effect is observed for the multi-channel devices with a reduction in the on-state current of less than 5 % in the whole measurement range, which proves their excellent V_{TH} stability (Figure 2.3.8 (a)). Moreover, multi-channel devices show reduced gate lag with respect to the single-channel references, which instead present a current decrease of 20 % at $V_{G,q}$ of -3 V. Such behavior is

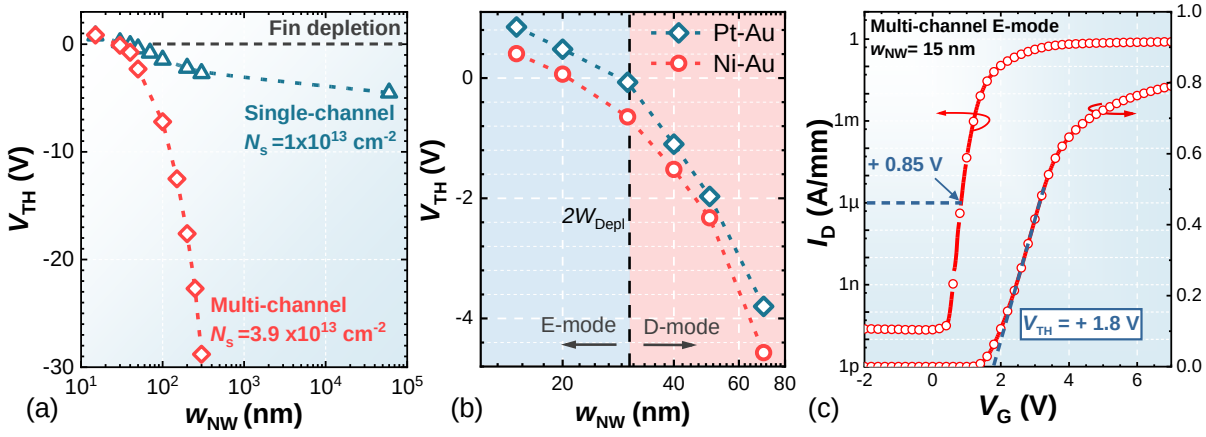


Figure 2.3.7: (a) V_{TH} as a function of the nanowire width for single- and multi-channel devices. (b) V_{TH} as a function of w_{NW} for multi-channel devices having conventional Ni-Au and Pt-Au gate metal stack. (c) Transfer characteristics of an E-mode multi-channel MOSHEMT, with w_{NW} of 15 nm in the E-mode gate region (Figure 2.3.2 (c)), L_{GD} of 10 µm and Pt/Au gate metals.

likely due to the multi-channel larger carrier concentration that results in a weaker influence of the traps in the gate dielectric on the device V_{TH}.

In addition, the temperature dependence of V_{TH} in multi-channel E-mode devices was investigated (Figure 2.3.8 (b)). A very constant V_{TH} can be observed in the whole measurement range up to 150 ºC with the device maintaining full E-mode operation also at high temperatures and showing only a minor V_{TH} shift of 50 mV. These results show the excellent stability of the device threshold voltage in the proposed multi-channel E-mode HEMTs.

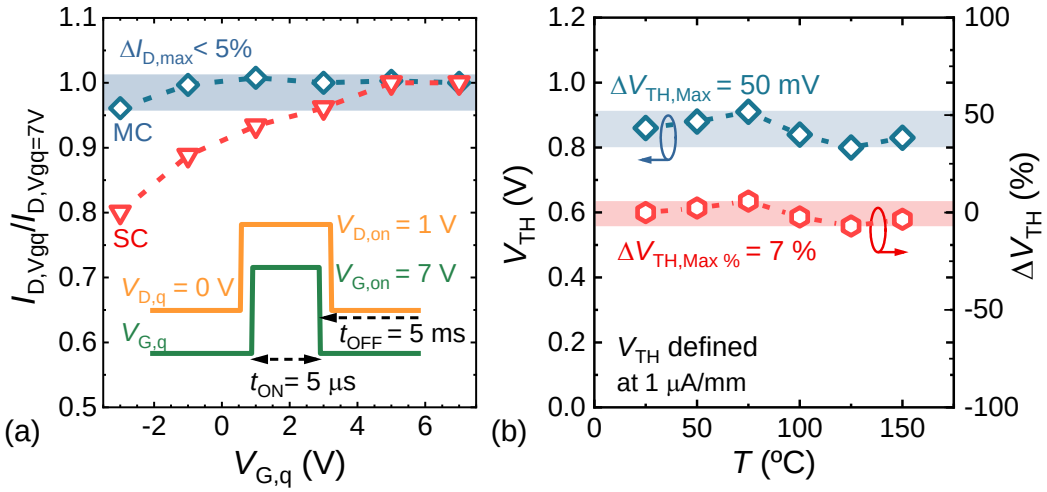


Figure 2.3.8: (a) Gate lag measurement as a function of $V_{G,q}$ for the presented multi-channel devices, and for a reference single-channel device having similar V_{TH}. (b) V_{TH} as a function of temperature (T) for the presented multi-channel devices.

2.3.4 Transport in Multi-Channel Nanowires and On-State Performance

The use of narrow nanowires having widths of few tens on nanometers requires a clear understanding of the electron conduction in such nanostructures to avoid a large degradation of the device on-state performance. To this end, Hall-Bar structures were fabricated (Figure 2.3.9 (a)), which enable determining the mobility and carrier concentration in multi-channel nanowire down to ~ 20 nm. The electron mobility in multi-channel nanowires measured by gated hall bar at different gate voltages (V_G) and nanowire width (w_{NW}) is shown in Figure 2.3.9 (b). μ shows a typical bell-shaped curve with the peak mobility shifting to higher V_G as w_{NW} decreases (Figure 2.3.9 (b)). While a mobility decrease is expected in narrow nanowires due to roughness scattering [119], [120] and donor-like states on the sidewalls [121], [122], a high peak μ above 1800 $cm^2 \cdot V^{-1}s^{-1}$ was maintained down to 70 nm-wide nanowires (Figure 2.3.9 (c)). Besides, large mobility above 1200 $cm^2 \cdot V^{-1}s^{-1}$ was measured for nanowires as narrow as 20 nm at a gate voltage of 5 V. This results in extremely small R_{sh} even for E-mode nanowires, which is still much lower than in conventional single-channel planar structures. In particular, a very low sheet resistance R_s of 150 Ω/sq for 20 nm E-mode nanowires was measured, which is about half of the typical sheet resistance of conventional planar single-channel heterostructures (Figure 2.3.9 (d)).

Thanks to the excellent electron transport in narrow multi-channel nanowires, multi-channel tri-gate devices presented extremely low R_{ON}, which is highly desirable for efficient power devices. With a gate-to-drain distance (L_{GD}) of 10 µm, the R_{ON} was 2.5 Ω·mm for D-mode (50 nm-wide tri-gate) and 3.2 Ω·mm for E-mode (15 nm-wide tri-gate) multi-channel tri-gate devices, respectively (Figure 2.3.10

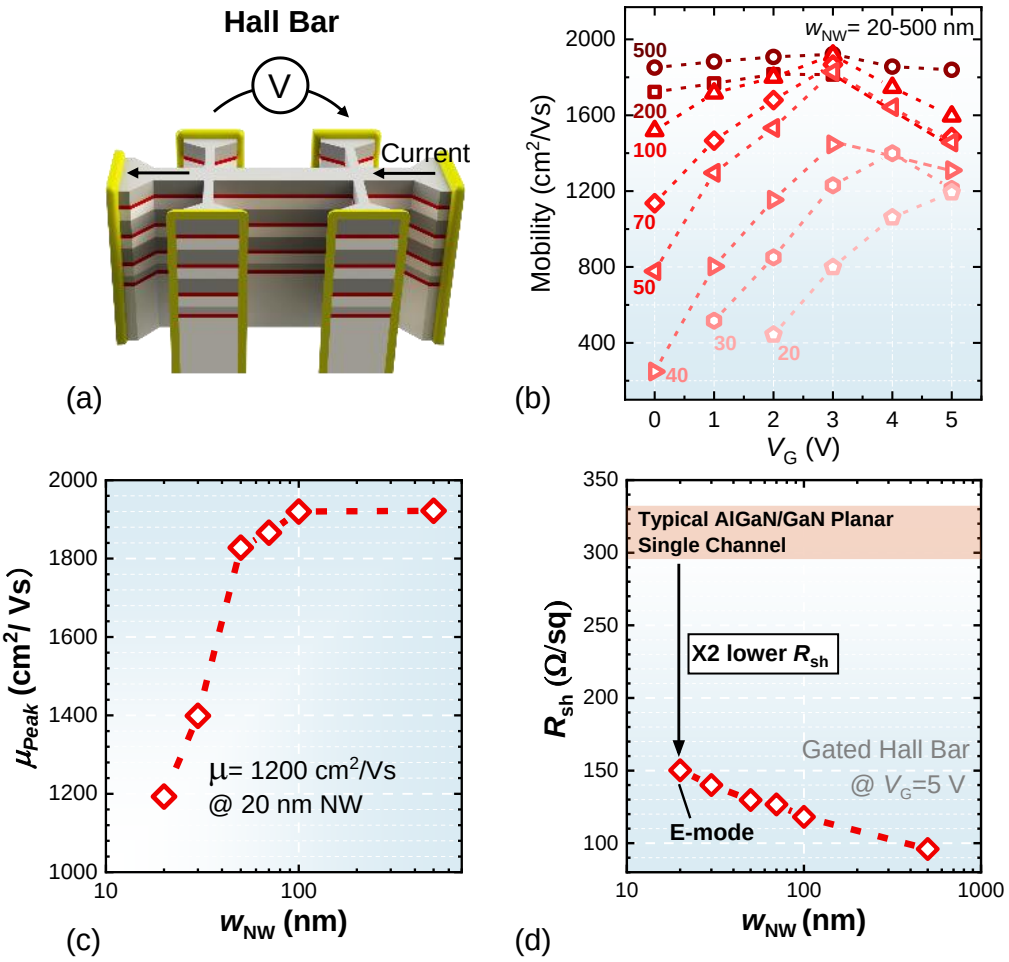


Figure 2.3.9: (a) 3D schematics of the Hall-Bar structure employed to measure the mobility and electron concentration of multi-channel nanowires. (b) Electron mobility in multi-channel nanowires measured by gated hall bar at different gate voltages (V_G) and nanowire width (w_{NW}). (c) Peak mobility as a function of the nanowire width extracted from figure b. (d) Sheet resistance as a function of w_{NW} for multi-channel nanowires.

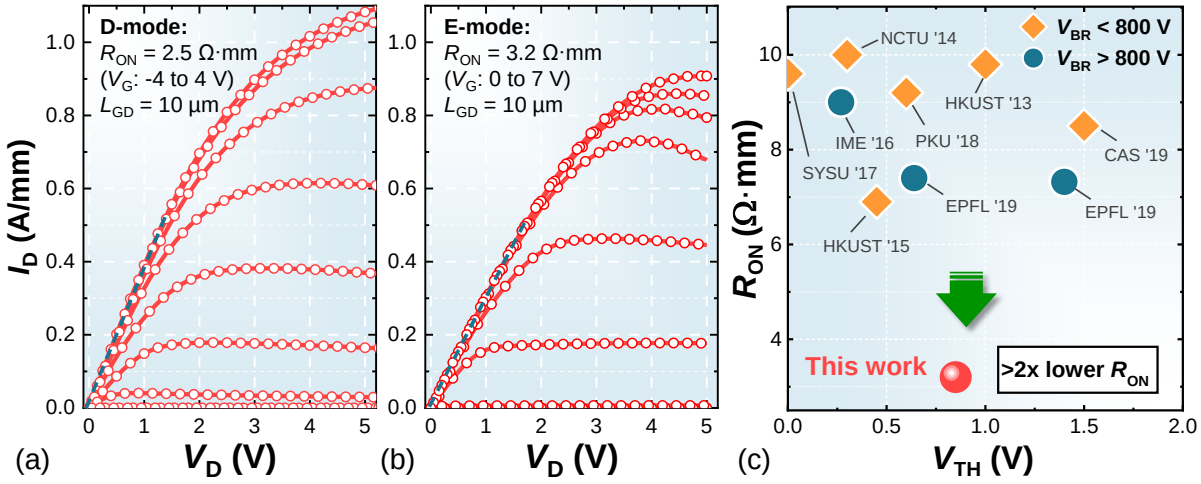


Figure 2.3.10: (a) Output characteristics of D-mode and (b) E-mode multi-channel MOSHEMTs showing the very low on-resistance for both devices. The current and all other values were normalized by the entire width of the device. (c) R_{ON} versus V_{TH} benchmark for the presented multi-channel E-mode devices compared to state-of-the-art single-channel devices present in the literature. Multi-channel devices show a more than 2x-lower R_{ON} for the same V_{TH} with respect to the single-channel counterpart. V_{TH} has been defined at 1μA/mm.

(a-b)). This resulted in a more than a two-fold reduction in the R_{ON} with respect to the best performing single-channel E-mode power device with similar V_{TH}, as shown in Figure 2.3.10 (c).

2.3.5 Off-state Electric-Field Management Strategy

For power conversion applications, in addition to small R_{ON} and E-mode operation, high V_{BR} is of major importance. For this reason, a reduced R_{ON} is a little value unless it is combined with large voltage blocking capabilities, which is more challenging in highly conductive structures. This was achieved in multi-channel devices by engineering the termination of the tri-gate electrode. While planar field plates (FPs) are usually implemented in single-channel devices to address the uneven distribution of the electric field in off state and reach higher V_{BR}, they are less suited for high-conductivity multi-channel devices. Figure 2.3.11 (a) shows the deterioration of the measured V_{BR} from single-channel to multi-channel Depletion-mode (D-mode) devices, as the conductivity of the heterostructure was increased

(R_{sh} reduced). While the V_{BR} in single-channel devices with R_{sh} of 280 Ω/sq was 1.3 kV, it dropped to ~40 V in multi-channel structures with R_{sh} below 170 Ω/sq. Such a decrease is due to the inability of the planar FP to deplete all the multi-channels beneath as a result of the high N_s and the shielding effect previously discussed, which limits its effectiveness as a field plate and causes premature device breakdown. This shows that planar FPs are not adapted for multi-channel structures and reveals the need for novel 3D field plates. By replacing the FP termination on the planar region with a tri-gate field plate termination on the D-mode portion of the nanowires (see Figure 2.3.2 (c)), the V_{BR} was greatly enhanced to about 600 V (Figure 2.3.11 (a)). In addition, the introduction of a 3D field plate based on a slanted nanowire design (slanted field plate region in Figure 2.3.2 (c)) resulted in a further V_{BR} enhancement to 1300 V (below 1 µA/mm), along with a small I_{OFF} below 20 nA/mm at V_D = 600 V (Figure 2.3.11 (b)). This high V_{BR} value represents a more than 35x-times improvement with respect to the conventional planar FP architecture. Such significant enhancement is due to two main reasons: i. the gate electrode terminated in the nanowire region with a 3D architecture (Figure 2.3.2 (a)), instead of a planar structure on top of the multi-channels, which can more effectively deplete all of the channels and avoid early oxide breakdown; ii. the tri-gate structure based on a slanted nanowire design [88]

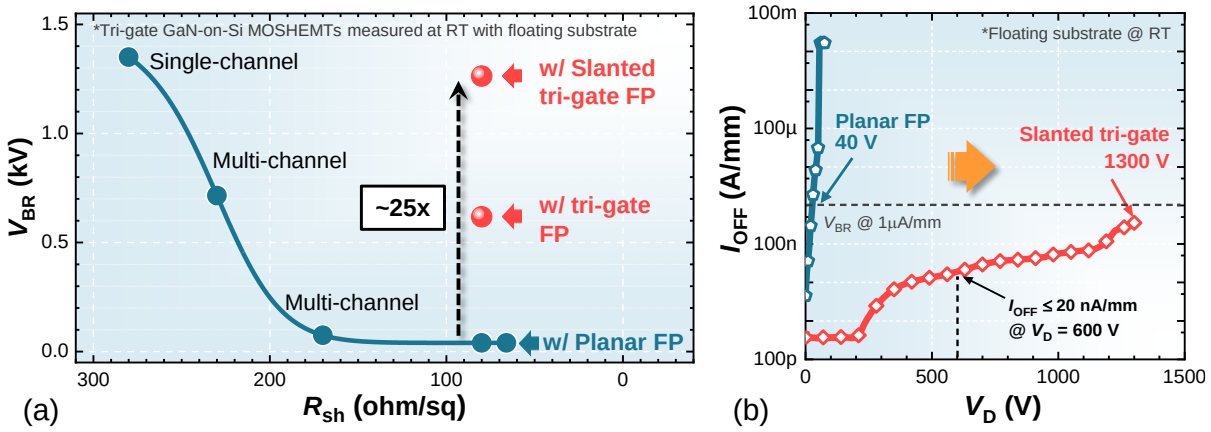


Figure 2.3.11: (a) Dependence of hard V_{BR} versus R_{sh} in different multi-channel structures. A significant enhancement in V_{BR} was achieved by introducing a tri-gate and slanted tri-gate 3D field plate with respect to conventional planar designs. (b) Comparison of OFF-state breakdown characteristics of multi-channel tri-gate MOSHEMTs with planar FP and slanted tri-gate FP. The slanted tri-gate FP led to an improved potential distribution, resulting in a high V_{BR} of 1300 V. The V_{BR} has been defined at 1 µA/mm

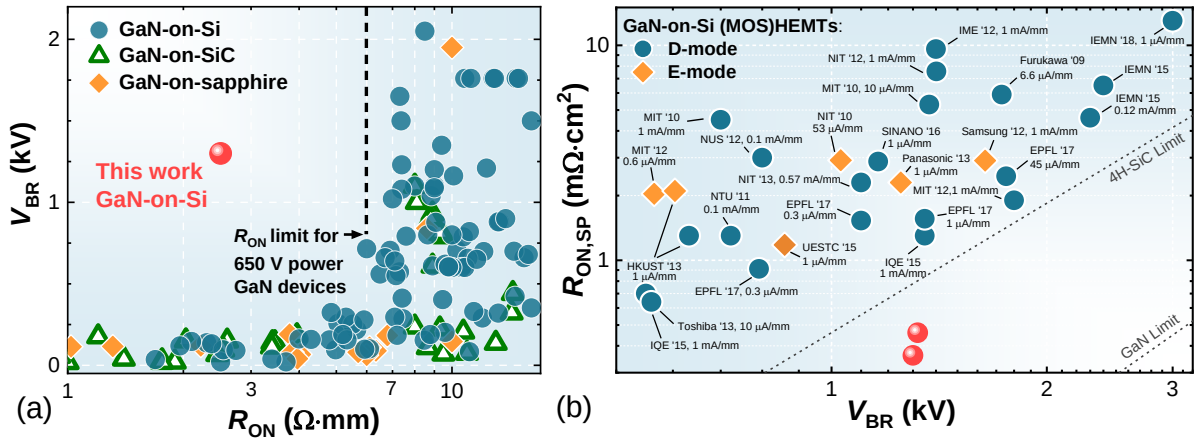


Figure 2.3.12: (a) V_{BR} versus R_{ON} and (b) $R_{ON,SP}$ versus V_{BR} benchmarks of the slanted tri-gate multi-channel MOSHEMTs against conventional single-channel GaN (MOS)HEMTs in the literature. Multi-channel devices surpass the material figure-of-merit limit of 4H-SiC, showing a substantial improvement with respect to single-channel devices and a record figure-of-merit of 4.6 GW/cm^2 for D-mode devices and 3.8 GW/cm^2 for E-mode devices.

effectively distributes the electric field, enhancing the V_{BR} (for more details on the role of Tri-gate field plates please refer to *Appendix E*).

The unique combination of the ultra-low R_{ON} and high V_{BR} in E-mode multi-channel nanowire devices renders a significant advance in performance from conventional single-channel devices. Firstly, the multi-channel devices surpassed the observed limit of R_{ON} for lateral GaN power devices (Figure 2.3.12 (a)), by considerably reducing the R_{ON} from ≧ 7 Ω·mm in 600/650 V-rated single-channel devices to 2.5 Ω·mm for D-mode and 3.2 Ω·mm for E-mode multi-channel devices, while keeping a high V_{BR} of 1300 V. This resulted in a more than 4-fold decrease in specific on-resistance $R_{ON,SP}$ with respect to the best performing single-channel device with the same blocking performance (Figure 2.3.12 (b)). The multi-channel devices achieved a record figure-of-merit of 4.6 GW/cm^2 for D-mode devices and 3.8 GW/cm^2 for E-mode devices, which represents a substantial improvement with respect to the single-channel counterpart (Figure 2.3.12 (b)). This is the first time that GaN lateral devices, both D-mode and E-mode, surpass the figure-of-merit limit of 4H-SiC semiconductors. These results reveal the potential of multi-channel nanowire-based devices for high-efficiency and ultra-compact power applications.

In this section, we demonstrated multi-channel tri-gate HEMT based on a multiple channel heterostructure and a nanostructured gate region. Thanks to this approach, E-mode devices showing very low specific on-resistance combined with large breakdown voltage were achieved. The capabilities and advantages of these devices result from the combination of a multi-channel platform and carefully designed nanowires, addressing various important trade-offs, while offering state-of-the-art performance with respect to current technologies. The proposed technology also offers opportunities for further innovation in electronic devices. The reduction of R_{ON} via the inclusion of more channels is an approach that could be applied to other types of electronic devices, including Schottky barrier diodes [110], RF switches, and amplifiers [45], [100], [114], ultra-wide-band-gap semiconductor materials, such as Ga_2O_3 [123]–[125], and high-mobility III-Vs, such as InGaAs and InAs [126].

2.4 Surface Passivation of Multi-Channel Tri-Gate Power Devices

The use of a high-quality surface passivation layer is of fundamental importance for power devices to reduce electron trapping in the off-state and avoid severe current collapse. One of the most common and effective approaches is to employ a Si_3N_4 layer deposited by low-pressure chemical vapor deposition (LPCVD) [127]–[129]. The high deposition temperature and the low pressure result in a high-quality passivation layer that effectively reduces the trapping sites at the device top interface. However, the integration of such a layer in the fabrication process flow of tri-gate devices is not trivial. In particular, the incompatibility of the deposition process with any metal and its high conformality require substantial modification of the process flow. In addition, the impact of the tri-gate architecture on the device's current collapse is yet to be investigated. Finally, the gate termination in the nanowire region of multi-channel devices necessitates novel passivation solutions specifically targeted for this device architecture.

In particular, we have shown in the previous section (*Section 2.3*) that tri-gate-based field-plate structures are required to manage the large off-state electric fields in multichannel devices. Such an architecture demands effective passivation of both the top AlGaN surface and the nanowires sidewalls, which combined with the presence of multiple 2DEGs, poses additional challenges for the passivation of multi-channel devices. This leaves unanswered the important question of whether multi-channel devices can be effectively passivated and whether conventional surface passivation techniques can be applied to such devices.

In this section, we present a surface passivation technology for multi-channel devices based on a conformal deposition of a thin SiO_2 interlayer followed by an LPCVD Si_3N_4 layer around the multi-channel nanowires, which enables to effectively reduce the electron traps both at the AlGaN top surface and at the nanowire sidewalls. This approach led to a significant reduction of the dynamic on-resistance in multi-channel devices under large off-state voltages of 350 V and comparable dynamic performance with passivated single-channel reference devices.[1]

2.4.1 Device Design and Fabrication

The multi-channel AlGaN/GaN heterostructure included 4 parallel 2DEG channels. The top 3 channels were composed of 20 nm Si-doped AlGaN barrier (with Si concentration of 10^{19} cm^{-3}), 1 nm AlN spacer, and a 20 nm GaN channel layer, while the last channel consisted of a 10 nm AlGaN barrier with 5×10^{18} cm^{-3} Si doping, 1 nm AlN spacer and 20 nm GaN channel. More details on the design of the heterostructure can be found in *Section 2.3*. The Hall mobility and carrier concentration of the multi-channel structure were 1930 $cm^2 \cdot V^{-1}s^{-1}$ and 3.9×10^{13} cm^{-2} respectively, resulting in a sheet resistance of 83 Ω/sq.

The fabrication started with electron-beam lithography to define the device mesa and the tri-gate structures in the gate region (Figure 2.4.1 (a-c)). The sample was then etched by Cl_2-based inductively coupled plasma etching (ICP) to a depth of 280 nm. The design of the tri-gate region is shown in Figure 2.4.1 (b) and is similar to the one described in *Section 2.3*. An O_2 plasma/ HCl cycled treatment was

[1] This section is based on **L. Nela** *et al.*, "Conformal Passivation of Multi-Channel GaN Power Transistors for Reduced Current Collapse", *IEEE Electron Device Lett.*, vol. 42, no. 1, pp. 86–89, 2021. © 2021 IEEE. **Contribution: First Author.**

performed to minimize etching damages on the nanowires sidewalls, followed by RCA cleaning of the sample. A 100 nm-thick LPCVD Si_3N_4 passivation layer was deposited at 770° C with a flow of 30 sccm of SiH_2Cl_2 and 180 sccm of NH_3 at a chamber pressure of 100 mT.

After the LPCVD deposition, nanowire structures aligned along the m-direction showed a strong crystallographic etching that caused significant damages to their sidewalls (Figure 2.4.2 (a)) and even their complete removal for widths below 300 nm. No significant etching was instead observed for the m- and c-planes. This issue was possibly due to GaN surface desorption during the LPCVD process [130], [131], and was successfully resolved by the introduction of a 2 nm-thick SiO_2 interlayer. The SiO_2 was deposited by atomic layer deposition (ALD) before the LPCVD deposition and effectively protected the surface, resulting in no etching of the tri-gate sidewalls (Figure 2.4.2 (b)). This was particularly important since the slanted portions of the nanowires would be completely deformed after the LPCVD Si_3N_4 deposition.

The LPCVD Si_3N_4 was removed in the gate and contact regions with low power (30 W) RIE etching. Since the 100 nm-thick Si_3N_4 filled the trenches between the nanowires (Figure 2.4.1 (c)), about 150 nm of over-etching was performed to remove the passivation layer and enable the formation of the tri-gate structure around all of the embedded channels. Ohmic contacts were formed by a Ti/Al/Ti/Ni/Au metal stack, and annealed at 780° C for 30 s. A 25 nm-thick layer of SiO_2 was deposited by ALD at 300° C and served as the gate oxide, followed by a Pt/Au (40 nm / 100 nm) gate metal stack. The device dimensions are L_{GS} = 1 µm, L_G = 1.5 µm and L_{GD} = 10 µm.

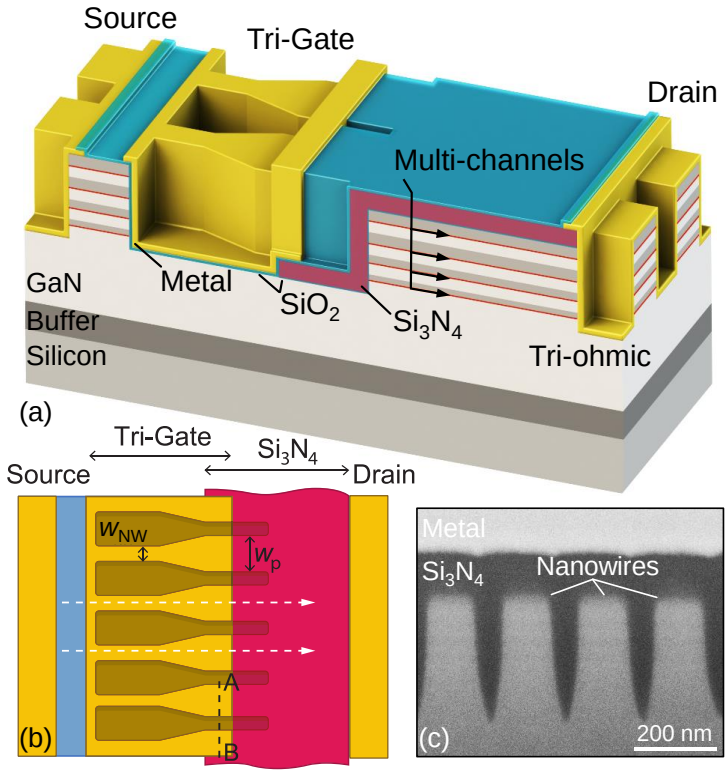


Figure 2.4.1: (a) 3D schematics of the multi-channel tri-gate MOSHEMT with LPCVD Si_3N_4 passivation layer. (b) Top-view schematics of the Tri-gate region indicating the nanowire dimensions. (c) Focused Ion Beam (FIB) cross-section along the AB line in (b) showing the passivated multi-channel nanowires conformably covered by the LPCVD Si_3N_4 passivation layer.

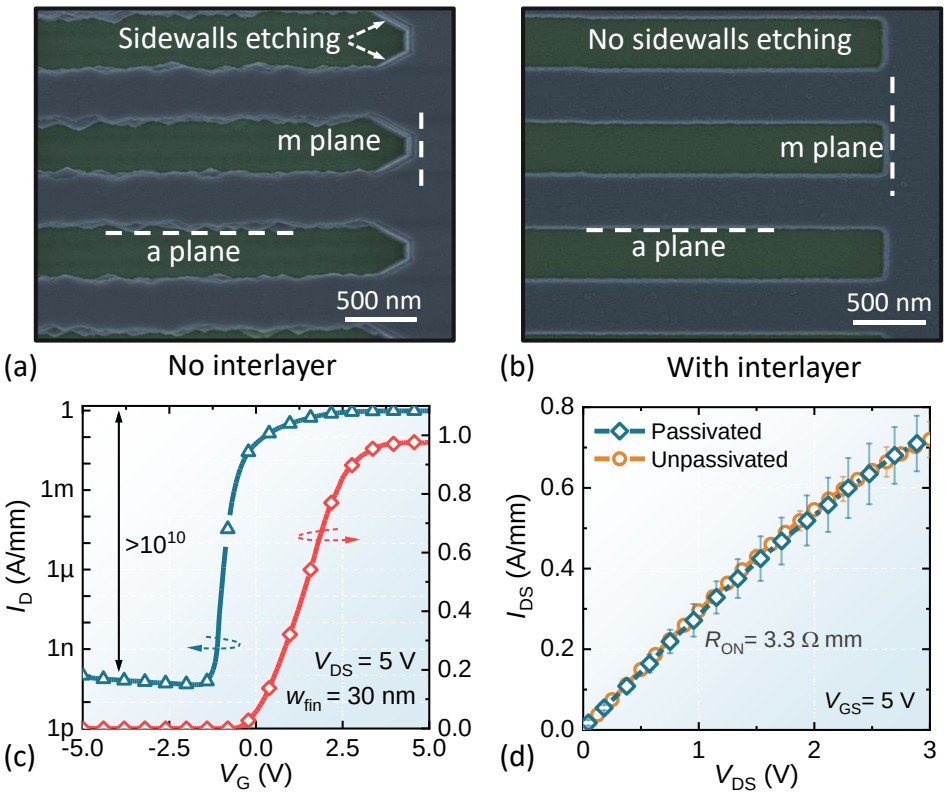


Figure 2.4.2: (a) SEM image of multi-channel fins after the 100 nm LPCVD Si_3N_4 deposition without and with (b) a 2 nm-thick SiO_2 protective interlayer. (c) DC transfer curve of the passivated device after the Si_3N_4 etching in the Tri-gate region. w_p was set to 100 nm (d) DC output curve of multi-channel devices with and without the passivation layer showing similar R_{ON}.

Reference single-channel devices were co-fabricated in the same batch undergoing the same fabrication process. w_{NW} was set to 30 nm throughout the paper since, while beneficial to tune the threshold voltage of the device (*Section 2.3.3*), it showed no impact on the dynamic on-resistance. All quantities have been normalized by the total device width (W = 60 µm).

2.4.2 Dynamic Performance of Multi-Channel Tri-gate HEMTs

The transfer characteristic of a multi-channel tri-gate device having a nanowire width of 30 nm is shown in Figure 2.4.2 (c). The Si_3N_4 removal in the trenches between nanowires allowed to form the tri-gate structure around all of the embedded channels. This leads to excellent control over the multi-channel structure, resulting in high I_{ON}/I_{OFF} above 10^{10}. Thanks to the optimized etching recipe and the large carrier density of the multi-channel heterostructure, the Si_3N_4 over-etching in the trench region did not significantly affect the device output curve. A very low DC on-resistance (R_{ON}) of 3.3 Ω·mm was measured, which corresponds to a specific on-resistance ($R_{ON,sp}$) of 0.51 mΩ·cm^2. This value is very similar to the one from reference un-passivated devices (Figure 2.4.2 (d)), confirming no noticeable degradation as a result of the Si_3N_4 removal.

To effectively manage the high off-state field in such conducting heterostructures, multi-channel devices require tri-gate-based field-plate solutions with the gate electrode terminating in the nanowire region rather than on the planar portion [109] (Figure 2.4.1 (a-b) and *Section 2.3.5*). This leads to the exposure of new crystal surfaces after the nanowire etching and damages during the dry etching process, potentially resulting in additional trapping sites on the nanowire sidewalls (Figure 2.4.3 (a)). To

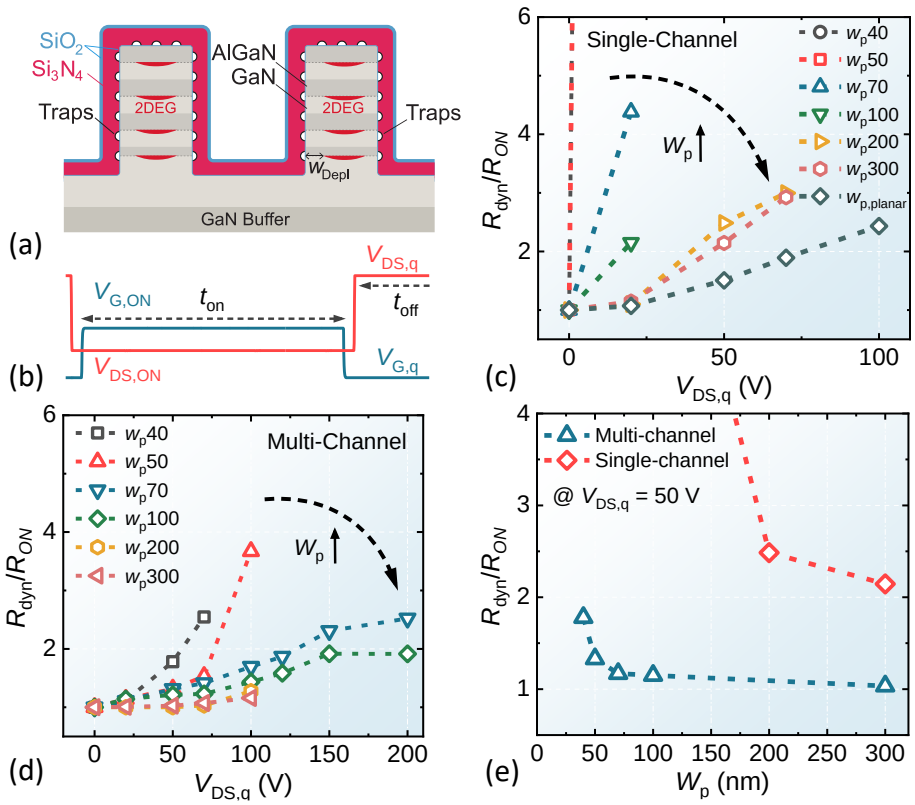


Figure 2.4.3: (a) Cross-section illustration of the passivated multi-channel nanowires highlighting the presence of sidewalls traps. (b) Schematics of the $R_{ON,dyn}$ measurement. (c) Normalized R_{dyn} for the single-channel reference devices and the multi-channel devices (d) as a function of $V_{DS,q}$ for different tri-gate termination widths w_p. $w_{p,planar}$ stands for the conventional termination for single-channel devices on the planar region. w_{NW} was set to 30 nm. (e) Normalized R_{dyn} comparison as a function of w_p for single- and multi-channel devices at $V_{DS,q}$ of 50 V.

investigate the effect of sidewalls traps on the dynamic behavior, devices with different tri-gate termination width w_p (Figure 2.4.1 (a)) were fabricated both on single- and multi-channel heterostructures and their dynamic on-resistance (R_{dyn}) was extracted by pulsed *I-V* characteristics (Figure 2.4.3 (b)). The device was stressed in the OFF state at quiescent drain voltage ($V_{DS,q}$) for a time (t_{off}) and then suddenly turned ON for a short time t_{on} during which the output curve was measured. For this measurement t_{on} was set to 50 µs and t_{off} to 5 ms, resulting in a duty cycle of 1%. In the OFF state, the quiescent gate voltage ($V_{G,q}$) was -3 V while the quiescent drain voltage ($V_{DS,q}$) was varied. In the ON state, V_G was 5 V and V_{DS} was swept from 0 V to 3 V.

Figure 2.4.3 (c) shows the normalized R_{dyn} as a function of $V_{DS,q}$ at different w_p for the reference single-channel devices. Despite the passivation layer, devices with small w_p show highly degraded dynamic performance, which drastically improved as w_p increases. Such behavior confirms the presence of sidewalls traps, whose effect increases significantly as the nanowire termination width is reduced, degrading R_{dyn}. While a similar trend of R_{dyn} with w_p is observed for multi-channel devices (Figure 2.4.3 (d)), its increase is lower with respect to the single-channel case and becomes considerable only for small $w_p < 50$ nm. Such an effect can be explained by the reduced effectiveness of the trapped electrons, acting as a virtual gate [132], in depleting the multi-channel nanowires. This is due to the much higher carrier density in the multi-channel heterostructure (almost 4x larger than the single-channel case) and to the weak influence exerted by the top AlGaN surface traps on the buried channels. Similarly to the

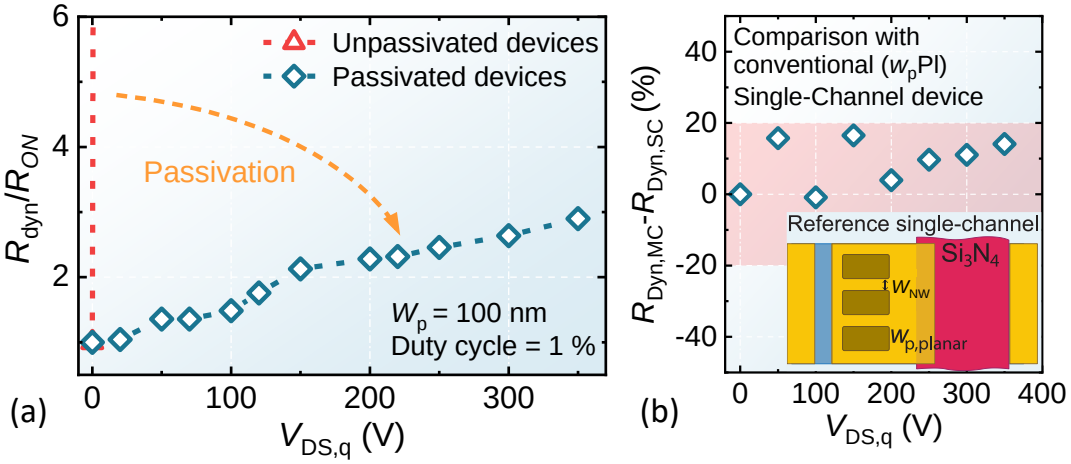


Figure 2.4.4: (a) Normalized R_{dyn} comparison for the multi-channel devices with and without the LPCVD Si_3N_4 passivation layer. (b) Difference (normalized by the average) between normalized R_{dyn} for multi- and single-channel devices. Single-channel devices with conventional planar gate termination ($w_{p,planar}$) were considered for the comparison (bottom right inset).

channel control by the tri-gate structure for which, at a given nanowire width, a larger gate voltage is required to turn off a multi-channel device (Figure 2.3.7 (a) and [109]), trapped electrons acting as a virtual gate are much less effective in depleting a multi-channel nanowire rather than a single-channel one. For this reason, much smaller values of w_p are required to have a good dynamic performance for multi-channel devices, which is shown in Figure 2.4.3 (e) where R_{dyn} as a function of w_p is compared for single- and multi-channel devices at a fixed $V_{DS,q}$. While multi-channel devices present quite constant R_{dyn} for w_p above 70 nm, single-channel devices require w_p of 200-300 nm to obtain a reasonable but still much higher R_{dyn} than for multi-channels. Most importantly, effective multi-channel device passivation can be achieved in the w_p range between 70 – 150 nm (Figure 2.4.3 (e)), which is the range required to achieve proper electric field management, as larger w_p designs result in degradation of the device blocking capability [109].

The dynamic behavior of multi-channel devices with and without the passivation layer is shown in Figure 2.4.4 (a). While un-passivated devices present almost no current for $V_{DS,q}$ as low as 20 V, passivated devices show reduced R_{dyn} up to $V_{DS,q}$ of 350 V, demonstrating that effective passivation at high operating voltage can be achieved for multi-channel devices. Notably, their dynamic performance is comparable to the one of reference single-channel MOSHEMTs with a planar gate termination, which is the conventional and optimal architecture for single-channel devices (Figure 2.4.4 (b)). This indicates that the presence of traps on the multi-channel nanowire sidewalls can be effectively suppressed and that good dynamic performance, comparable to the single-channel devices for a given passivation technique, can be achieved for multi-channel MOSHEMTs. Further improvements are possible by tuning the etching process to reduce the damages to the nanowire sidewalls and by optimizing the deposition of the protective interlayer and LPCVD Si_3N_4.

In this section, we presented a surface passivation technology for multi-channel devices based on a conformal SiO_2/Si_3N_4 passivation layer around the multi-channel nanowires. Thanks to this approach, multi-channel MOSHEMTs with significantly reduced dynamic R_{ON} up to large charging voltages of 350 V and comparable dynamic performance with respect to single-channel reference devices were achieved. These results prove that the multi-channel devices can present excellent DC and dynamic performances, showing the potential of this technology for future power devices.

3 Intrinsic Polarization Super Junctions Devices for Optimal Electric Field Management

3.1 Introduction

The performance of power devices is largely determined by their on-state resistance (R_{ON}) and breakdown voltage (V_{BR}). A reduction in R_{ON} while maintaining high V_{BR} would result in reduced losses and hence in higher energy efficiency in power conversion. However, this is extremely challenging due to the inherent trade-off in semiconductors between the carrier density and the breakdown voltage, which is described by a figure-of-merit proportional to V_{BR}^2/R_{ON} (*Section 1.4.3*). While GaN offers excellent material properties including large critical electric field and high-mobility carriers in the 2DEG, the current performance of GaN devices is very far from what could be achieved with this semiconductor. In particular, the lateral architecture of GaN HEMTs combined with the large density of the two-dimensional electron gas (2DEG) results in a peaked off-state electric field at the gate edge and in a non-uniform field distribution in the depletion region. This limits the useful portion of the access region that can hold large off-state voltages and severely reduces the maximum achievable breakdown voltage (V_{BR}).

In order to address the non-uniformity of the off-state electric field, Super Junctions (SJs) have been proposed for Silicon power devices. The origin of the off-state electric field non-uniformity in semiconductor devices is the presence of a net charge in the depleted region (see *Appendix D*). This charge contribution originates from ionized dopants whose corresponding mobile carrier has been depleted, thus resulting in a net fixed charge. In a conventional 1D device geometry, this leads to a triangular electric field profile (in the case of a uniform doping concentration) whose slope is proportional to the doping concentration. Since both the device conductivity (determining the R_{ON}) and the electric field slope (inversely proportional to V_{BR}) increase with the doping concertation, this sets a trade-off between R_{ON} and V_{BR}.

A clever solution to overcome this trade-off is to achieve a neutral depletion region, which would result in an ideal constant electric field profile. In silicon power devices, this condition is obtained by employing a 2D doping profile with interchanging *p*-type and *n*-type pillars. Such structures were proposed in the ‘90s for Si vertical power devices and have enabled decoupling the doping concentration, and thus the R_{ON}, from the device breakdown voltage. This resulted in a major improvement in the device performance with a significant decrease of the resistance for a certain (V_{BR}), which led to significantly overcoming the one-dimensional Si material limit [133], [134].

As Wide Band-Gap (WBG) semiconductors, such as GaN, are emerging thanks to their superior properties, the application of the SJ concept to these better-performing materials could lead to great improvements in the state-of-the-art [39], [135], [136]. Yet, GaN SJs are still out of reach, hindered by

the difficulties in achieving selective and highly-doped *p*-type regions, due to the absence of effective Mg implantation or high-quality *p*-GaN regrowth [137], [138].

However, the AlGaN/GaN lateral platform offers a unique alternative to conventional vertical SJs. To address the *p*-GaN doping limitation, polarization super junctions (PSJs) have been proposed [51], [52], [54], [135], [136], [139], which take advantage of the polarization fields naturally formed in GaN heterostructures to achieve charge balance. In these structures, a two-dimensional electron and hole gas (2DEG and 2DHG) of equal carrier concentrations (N_s and P_s respectively) can be obtained naturally, thanks to the presence of matching polarization charges. The charge compensation between electrons in the 2DEG and holes in the 2DHG results in an overall neutral drift region and thus in a flat off-state electric field profile, leading to a similar behavior to conventional, doping-based SJs.

Nevertheless, translating the matching polarization charges into mobile N_s and P_s of equal concentration is a challenging task due to the presence of ionized donor states at the top crystal surface, which provide electrons to the 2DEG and prevent the formation of a large-density 2DHG [55], [56]. This mechanism results in a considerable charge mismatch and thus in a non-uniform off-state electric field profile. A detailed quantitative analysis of the design and behavior of such devices is thus needed to address these challenges and is crucial for the development of the technology.

In addition, while a flat electric field profile intuitively results in improved blocking capabilities, a quantitative analysis of the performance improvement enabled by PSJs with respect to conventional HEMTs is lacking, with current comparisons limited to the case of uniformly doped power devices [54]. This is due to two main reasons. On the one hand, while the performance limit of vertical devices is well understood, the FOMs of lateral devices are not properly described by current models. Indeed, although the on-resistance versus V_{BR} material limit is often used to show the potential of GaN compared to Si or SiC, such an approach cannot be used to accurately compare GaN HEMT and PSJ devices. In particular, while a uniform off-state field profile is typically assumed to extract the material limit [140], this assumption is not valid for HEMTs which, similarly to doped devices, present fixed charges in the depleted drift region [55], [56]. On the other hand, the lack of simple analytical models describing the off-state of PSJs and HEMTs does not allow easily comparing the performance of these devices and thus unveil the potential of polarization super junctions.

Moreover, an accurate investigation of PSJ switching performance is yet to be reported and some concerns are present due to the large charge depletion that is achieved in such devices, which could hinder their high-frequency operation. For these reasons, a detailed analysis of the behavior of PSJs and of the possible performance improvements compared to conventional HEMT devices is fundamental to assessing the validity and potential of the proposed technology.

This chapter is organized into two sections that address the aforementioned challenges.

1. In the first section, we propose a simple and robust platform for AlGaN/GaN intrinsic Polarization Super Junctions that enables excellent charge matching for any surface condition, without relying on doping of the GaN cap. We investigate the role of surface donor states in determining the charge mismatch and provide a strategy to minimize their impact on the device performance. Simulated devices based on this structure show optimal carrier depletion with a flat electric field profile in the whole drift region. Finally, we extend this concept to multi-channel i-PSJ structures. We demonstrate a

much-reduced sheet resistance and present a robust strategy to achieve charge balance, which enables reducing the on-resistance without degrading the off-state performance, thus greatly improving the device figure-of-merit.

2. In the second section, we develop a simple and yet accurate physical model to describe the off-state behavior and main figures-of-merit of lateral GaN devices. Based on this model, we investigate and compare both the DC and switching losses of PSJs and HEMTs, showing the promising potential of polarization super junctions to enable more efficient devices for power conversion applications.

3.2 Design of AlGaN/GaN Intrinsic Polarization Super Junction Devices

Polarization Super Junctions should enable to overcome the challenging GaN *p*-doping by relying instead on matching polarization charges to achieve charge balance. However, translating the matching polarization charges into mobile N_s and P_s of equal concentration is a challenging task. This is because of the presence of ionized donor states at the top crystal surface, which provide electrons to the 2DEG and prevent the formation of a large-density, mobile 2DHG [55], [56].

The most common strategies to address these issues comprise the use of a *p*-doped GaN cap layer to provide holes to the 2DHG [141]–[144] or the compensation between a *p*-GaN cap layer and an *n*-type delta-doped region [139], [145]. Yet, the introduction of a *p*-doped cap defeats the purpose of PSJs, leading to the typical challenges in charge balancing as in conventional doped SJs, aggravated by the difficult *p*-GaN doping and the severe effect from surface trapping in lateral architectures. In particular, the use of a *p*-GaN cap requires the precise control of its thickness and especially of its doping level, which is very challenging due to the inefficient Mg activation and to its thermal back diffusion [146], [147]. Besides, the strong dependence of the Mg activation on temperature [146], [147] leads to an increased carrier mismatch ($\Delta=N_s-P_s$) when the device heats up during operation, thus resulting in an early breakdown (for a more in-depth comparison with PSJ devices with a *p*-GaN cap, please refer to *Appendix D*).

Previous works [51], [53] have also claimed the demonstration of PSJ devices by employing usual AlGaN/GaN HEMTs structures without any GaN cap on top, which were referred to as natural PSJ. However, in usual AlGaN/GaN HEMTs, no 2DHG can be formed due to the presence of ionized donor states at the top crystal surface, which provide electrons to the 2DEG [55], [56]. These states represent a fixed net charge contribution, which determines the off-state electric field and hinders any super junction effect. This is confirmed by the fact that these devices show the same behavior and off-state performance as normal HEMTs reported in the literature [148], [149]. While electron trapping in the off-state can mitigate this net charge contribution thanks to virtual gate effects, such mechanisms result in severe current collapse and thus are highly undesirable. Finally, PSJ devices based on 3D polarization doping have also been proposed [52], [150]. Yet, these devices require a challenging control of the growth parameters to ensure a very precise $Al_xGa_{1-x}N$ graded profile over thick layers and suffer from reduced carrier mobility due to the strong alloy scattering.

To address these limitations, in this section, we propose a simple and robust platform for intrinsic PSJ (i-PSJ) based on a thick undoped GaN cap layer, which enables achieving charge balancing regardless of the surface and temperature conditions, without any need for precisely controlled doping.[1] Although heterostructures with undoped GaN cap were reported [55], [151] and the presence of a 2DHG was shown experimentally [146], [147], [152], these studies did not focus on the design of i-PSJs. Thus, key challenges of these structures such as achieving a small charge mismatch regardless of surface donor states and obtaining large N_s despite the thick cap remain unexplored. Here, we show that by employing a thick undoped GaN cap excellent intrinsic matching between N_s and P_s is obtained and

[1] This section is based on **L. Nela** *et al.*, "Intrinsic Polarization Super Junctions: Design of Single and Multi-Channel GaN Structures", *IEEE Transaction on Electron Devices*, 2022. **Contribution: First Author.**

maintained for any surface condition while still achieving a large 2DEG density. Simulated devices based on this heterostructure show the typical SJ behavior with a neutral drift region, which results in an ideal constant off-state electric field. The effect of donor states at the GaN top surface on the carrier mismatch is discussed and the role of the charge imbalance on the device performance is presented.

Besides, to significantly reduce the device on-resistance, we investigate intrinsic multi-channel PSJs, in which several channels are stacked to decrease the heterostructure sheet resistance. In particular, we address the main challenges of these structures, namely the population of all the buried channels and charge matching. Multi-channel structures typically employ doping of the barrier to increase the carrier concentration in the buried channels [108], [109], [113]. This strategy however results in fixed donor charges in the off-state and is thus not suitable for PSJs. Another possibility consists of including both *n*-type doping in the barrier and *p*-type doping in the GaN channel to balance the fixed charges [139]. Yet, this approach is very difficult to implement in GaN devices due to the strong Mg memory effect and inefficient activation, which prevent an accurate control of the doping level, resulting in a large charge mismatch. In addition, it should be noted that charge matching for all of the channels, including the top and bottom ones, should be achieved as any charge mismatch would limit the breakdown voltage of the device [53].

Here, we propose an intrinsic multi-channel structure with a thick undoped GaN cap as an optimal platform for multi-channel i-PSJ. We demonstrate that large carrier densities and reduced sheet resistance can be achieved also for intrinsic multi-channels and we present a robust strategy to achieve proper charge balance in multi-channel structures. Simulated devices based on this approach show a flat off-state electric field profile despite the increased carrier density and thus have the potential to greatly improve Baliga's figure-of-merit.

3.2.1 Design and Charge Matching for Single-Channel Heterostructures

The first step to designing a charge-balanced heterostructure is to identify the source of the electrons in the 2DEG. Indeed, while at equilibrium charge neutrality is always guaranteed in the structure, during the off-state mobile electrons are depleted by the high voltage. If these electrons have been generated by the formation of other mobile carriers (e.g. holes), these can also be depleted, resulting in a neutral drift region and in a SJ behavior. However, if the source of the 2DEG is fixed charges, such as surface donor states, these cannot be depleted and result in a net charge contribution in the drift region, thus affecting the off-state electric field as in conventional doping-based devices.

Figure 3.2.1 (a) shows the investigated heterostructure, which comprises a GaN channel, an AlGaN barrier, and a GaN un-doped cap. This results in a 2DEG at the bottom GaN/AlGaN interface and, depending on the conditions, in a 2DHG at the top GaN/AlGaN interface. Donor states with an energy level E_D are located at the GaN cap/insulator interface due to the presence of the crystal surface. While the structure is similar to conventional GaN HEMT heterostructures, increasing the undoped GaN cap thickness (t_c) enables to reach charge matching between 2DEG and 2DHG, which offers an excellent platform for intrinsic PSJs.

Typical HEMT heterostructures employ a very thin (~2-3 nm) GaN cap, whose main purpose is to protect the AlGaN barrier during processing. In this case, the N_s in the 2DEG is entirely generated by ionized surface donor states [55], [56] (Figure 3.2.1 (a-b)). While electrons in the 2DEG are mobile

charges that are depleted during the off-state, ionized surface donors are fixed positive charges that remain in the depleted region and directly affect the field profile in the off-state. Thus, while the presence of matching polarization charges is a necessary condition for PSJs, this is not sufficient to achieve any super junction effect in conventional HEMT structures. In particular, the key mechanism lies in translating the matched polarization charges into a mobile 2DHG and 2DEG of equal concentration. In this case, the N_s in the 2DEG is entirely generated by mobile holes in the 2DHG that can be depleted in the off-state, resulting in a neutral drift region. This favorable condition can be achieved by adjusting the GaN cap thickness. As t_c increases, more and more electrons in the 2DEG originate from the valence band at the top AlGaN interface, rather than from ionized surface donor traps, forming a 2DHG with hole concentration P_s (Figure 3.2.1 (b)). The difference between the mobile N_s and P_s, i.e. the charge mismatch $\Delta=N_s-P_s$, corresponds to the density of ionized donor states at the top GaN cap surface (Figure 3.2.1 (b)) and is a direct indicator of the net fixed charges in the depletion region. For large thicknesses of the cap, P_s further increases and approaches very closely the N_s value, leading to an intrinsic negligible charge mismatch (Figure 3.2.1 (b)).

In the absence of a top metal, the Fermi level at the GaN surface is determined by the energy level of the donor traps [56]. While experimental values are present in the literature [55], [56], the exact E_D (or its distribution) highly depends on the surface conditions, which are unpredictable and can influence the Δ value. Figure 3.2.1 (c) shows that a considerable dependence of Δ on the trap energy is present for small t_c, which however becomes negligible as t_c increases. This allows achieving a minimal carrier

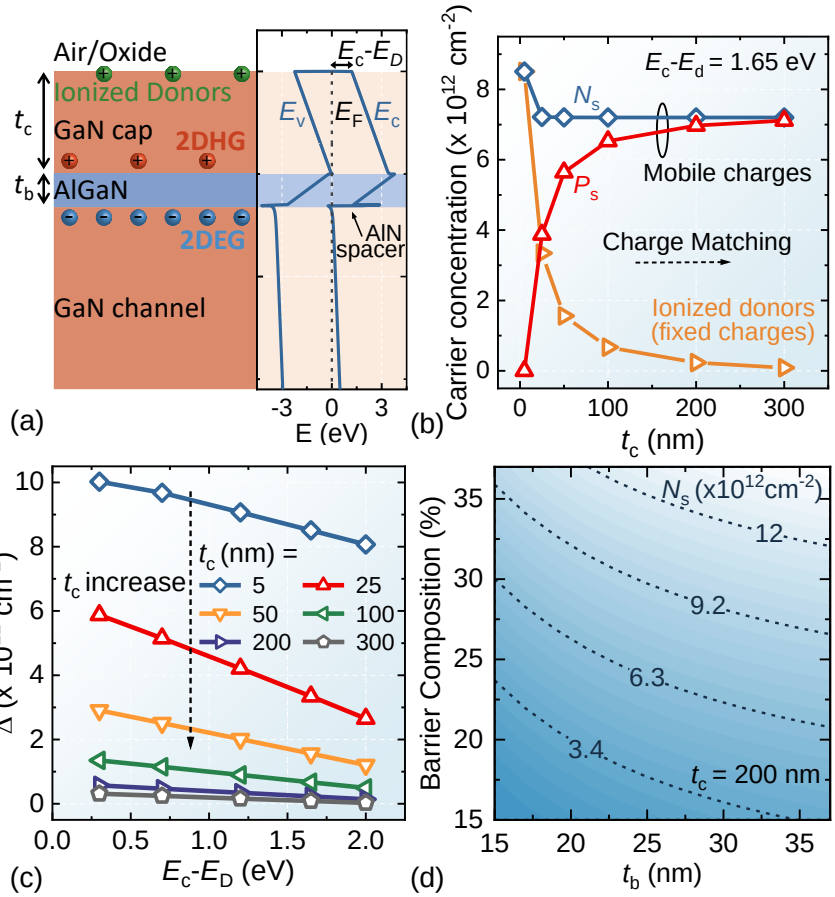


Figure 3.2.1: (a) Investigated heterostructure and corresponding band structure. (b) N_s and P_s as a function of the GaN cap thickness (t_c). (c) Carrier mismatch (Δ) as a function of the donor states energy for different t_c. (d) N_s as a function of the AlGaN barrier thickness and composition for a 200 nm-thick cap.

mismatch regardless of the presence of top donor states, thus preventing any influence from the surface conditions on Δ. Despite the presence of a thick cap layer (t_c = 200 nm), large N_s values can still be obtained by employing realistic barrier thicknesses and compositions (Figure 3.2.1 (d)), which makes the proposed heterostructure an excellent and robust platform for intrinsic PSJs.

3.2.2 Single-Channel i-PSJ Devices

To understand the potential of charge balance to improve the off-state electric field distribution, we focus our analysis on the drift region of an i-PSJ device. It should be noted that the carrier depletion and electric field in the drift region are equivalent for a diode and a transistor (with the anode corresponding to the gate and the cathode to the drain). Therefore, the proposed concept and analysis are general and valid for both types of devices. The heterostructures comprises a 30 nm-thick $Al_{0.25}GaN$ barrier, and a 200 nm-thick UID cap (Figure 3.2.2 (a)), leading to N_s of 0.8 x 10^{13} cm^{-2} and Δ < 0.5 x 10^{12} cm^{-2}. A first electrode (cathode or drain) with work-function (Φ_b) of 4.2 eV provides ohmic contact to the 2DEG and Schottky contact to the 2DHG, while a second electrode (anode or gate) (Φ_b=5.2 eV) provides a barrier to electrons in the 2DEG. A top ohmic contact to the 2DHG is realized by a p^{++}-GaN layer (whose aim is only to improve the contact to the 2DHG but has no role in the charge matching) and a metal electrode [153], which is connected to the anode or gate (please refer to *Appendix D* for

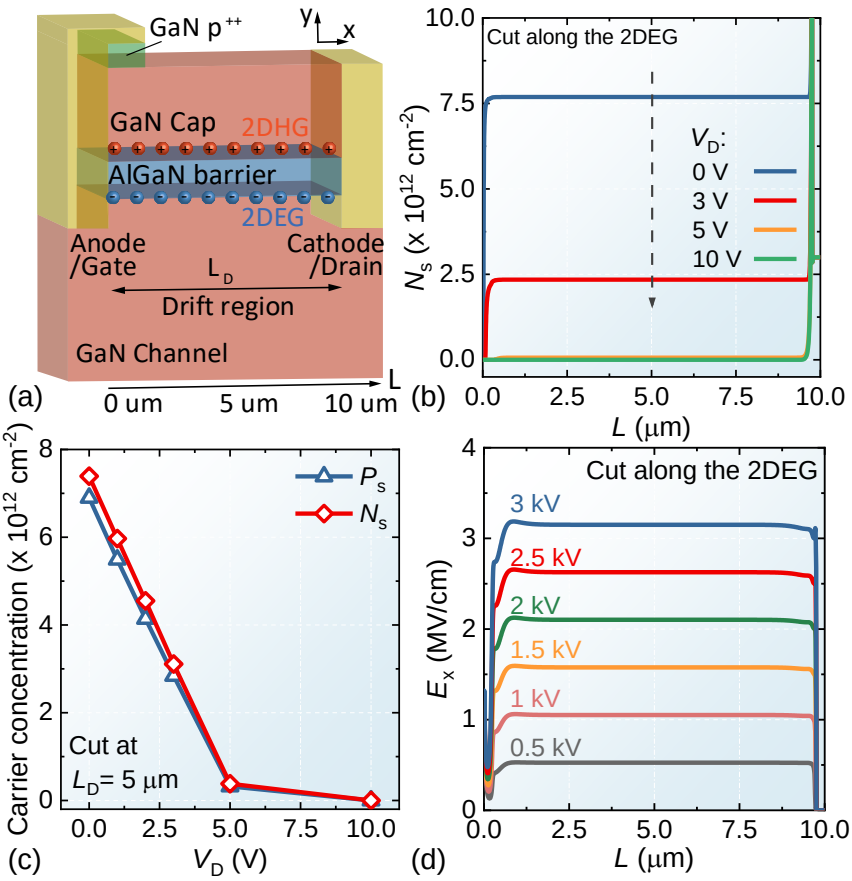


Figure 3.2.2: (a) Schematic of the drift region of an i-PSJ device. (b) N_s profile at the AlGaN/GaN bottom interface as a function of the reverse voltage. (c) N_s and P_s cut in the middle of the drift region as a function of V_D. (d) E_x profile at the AlGaN/GaN bottom interface for different V_D.

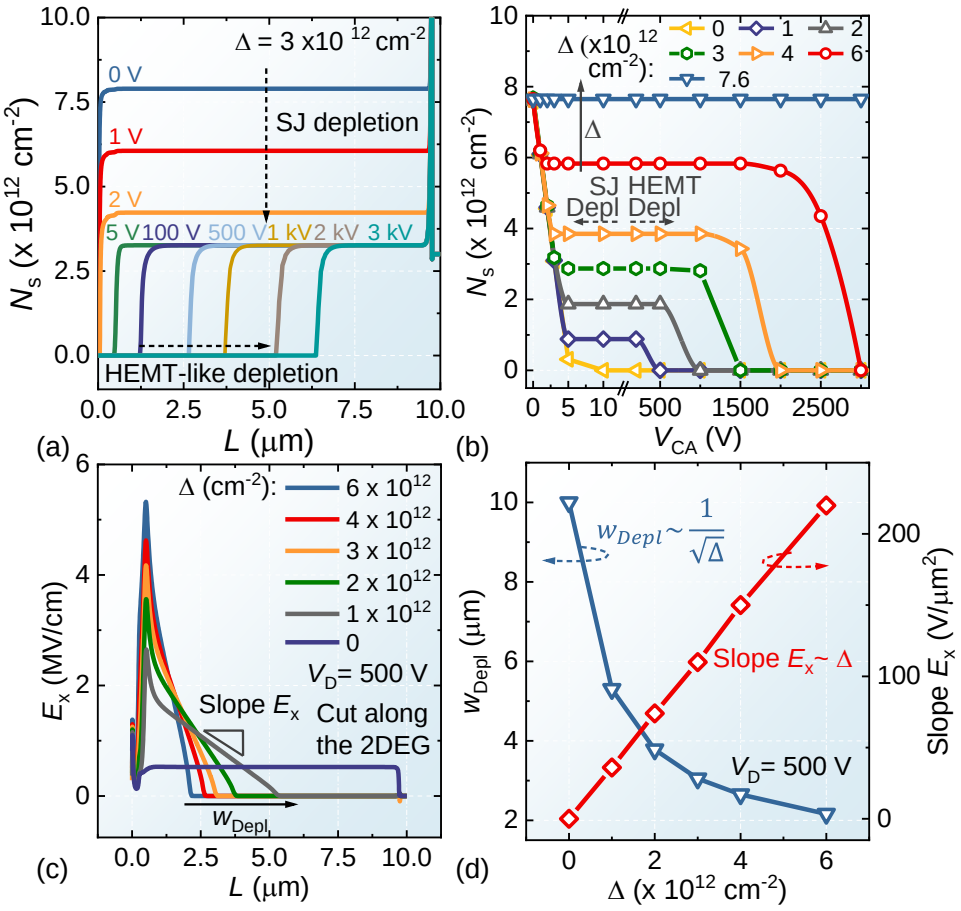


Figure 3.2.3: (a) N_s profile as a function of V_D for a PSJ device with Δ of 3 x 10^{12} cm^{-2} for different V_D (b) N_s concentration at L_D = 5 μm as a function of V_D and Δ (c) E_x profile for V_D =500 V for different mismatch values. (d) W_{Depl} and slope of E_x as a function of Δ for V_D =500 V.

more details on the contact to the 2DHG). The device simulation was performed using Silvaco Atlas software and employing its built-in material parameters [154].

Contrary to conventional devices in which the charge depletion in the off-state extends from the anode (or gate) towards to cathode (or drain), the intrinsic PSJ device shows a uniform and simultaneous depletion of the 2DEG in the whole drift region (L_D) (Figure 3.2.2 (b)). Most importantly, a full carrier depletion is achieved at an extremely low voltage over the drift region (V_D) of ~ 5 V, with the same behavior for both N_s and P_s (Figure 3.2.2 (c)). This results in an electric field profile that is flat along the whole drift region (Figure 3.2.2 (d)), which is a clear feature of SJs and allows significantly increasing the device V_{BR}.

Unbalanced structures were investigated to determine the effect of the carrier mismatch on the device performance. Figure 3.2.3 (a) shows the carrier depletion for a PSJ device having Δ ~ 3 x 10^{12} cm^{-2}. Two different processes can be identified: first, the device behaves as a PSJ with a uniform carrier depletion down to the value of Δ for V_D of only a few Volts (Figure 3.2.3 (b)). At this point, conventional depletion occurs, as in the case of typical HEMT-like devices, which grows from the anode (or gate) to the cathode (or drain) and requires very large V_D values to expand. This results in a degradation of the off-state field distribution as the mismatch increases (Figure 3.2.3 (c)). The depletion width (W_{Depl}) reduces and the E_x slope rises as Δ increases, leading to the typical triangular shape of the electric field in conventional HEMT structures. Besides, it is possible to observe that $W_{Depl} \sim 1/\sqrt{\Delta}$ and the slope of E_x

~ Δ (Figure 3.2.3 (d)), which is the typical behavior of conventional HEMTs and shows that unmatched PSJs behave as a HEMT device having $N_s = \Delta$. It should be noted that, while electron trapping in the off-state can mitigate the net charge contribution thanks to virtual gate effects and thus smoothen the electric field peak, this mechanism results in severe current collapse, and thus it is highly undesirable.

The effect of Δ on the device off-state behavior does not depend on the origin of the mismatch. Thus, the presented analysis can be also employed to account for other sources of mismatch, such as possible impurities in the GaN layers, which have not been directly included in the simulation due to their strong dependence on the growth technique and parameters.

3.2.3 Design and Charge Matching for Multi-Channel Heterostructures

Since for charge-balanced intrinsic PSJs N_s can be decoupled from the off-state electric field, reducing the sheet resistance (R_{sh}) of conventional single-channel heterostructure would in principle improve the performance of the device. However, a significant R_{sh} reduction in such structures is challenging to achieve due to the trade-off between the carrier concentration and mobility [109], [113]. Multi-channel heterostructures [50], [109]–[111], [113], [155] having multiple stacked AlGaN/GaN layers allow overcoming this limitation by distributing a large N_s in several parallel 2DEGs [109], [113] (*Section 2.3*). However, two main challenges need to be addressed to achieve multi-channel intrinsic polarization super junctions. The first one consists of achieving a large carrier density in the buried channels without employing *n*-type doping of the barrier, which would result in fixed donor charges in the off-state. The second challenge is to obtain a charge-balanced structure without relying on the doping of the GaN channels [139]. The absence of *p*-type doping in the GaN layers is fundamental since the strong Mg memory effect, observed in GaN *p*-doping, would be very detrimental to the charge balance and the electron mobility due to the increased carrier scattering. Besides, charge matching for all of the channels is a fundamental requirement to achieve an effective super-junction depletion since any charge mismatch would limit the device voltage blocking capability [53].

The proposed intrinsic multi-channel structure with a top GaN cap is shown in Figure 3.2.4 (a), with the corresponding bandstructure reported in Figure 3.2.4 (b). In general, a multi-channel stack

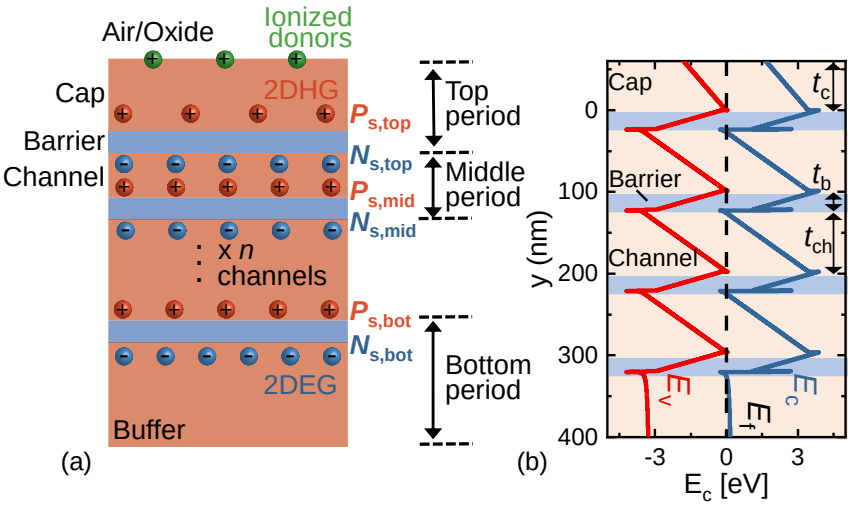


Figure 3.2.4: (a) Cross-sectional schematic and (b) bandstructure of the multi-channel heterostructure under study.

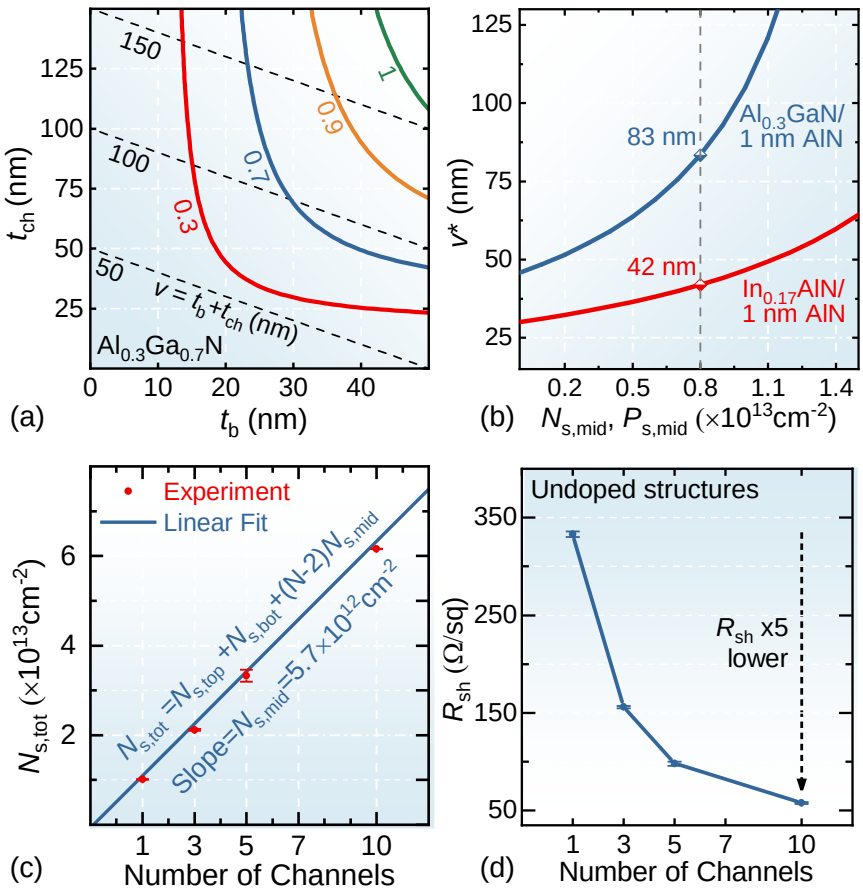


Figure 3.2.5: (a) $N_{s,mid}$ as a function of the barrier and GaN channel thickness for an intrinsic multi-channel heterostructure with an $Al_{0.3}GaN$ barrier and a 1 nm-thick AlN interlayer. (b) Minimum possible period thickness for the middle channels as a function of the desired carrier density. (c) Total electron concentration and (d) sheet resistance as a function of the number of channels for the grown multi-channel structures.

comprises a top and bottom channel, and n middle channels. While the 2DEG concentration of the bottom channel is similar to the single-channel case, and thus is typically large, particular care should be taken to populate the 2DEGs of the middle and top channels due to the finite thickness of the GaN channel. In the absence of n-type doping, the electron concentration in these channels ($N_{s,top}$ and $N_{s,mid}$ (Figure 3.2.4 (a)) depends both on the barrier and GaN channel thickness (t_b and t_{ch}). A proper combination of t_b and t_{ch} should be selected to achieve the desired electron concentration and avoid unpopulated channels [156]. This sets a corresponding channel period ($v = t_b + t_{ch}$), determining the total heterostructures thickness (Figure 3.2.5 (a)), which should be minimized to facilitate the device fabrication. By knowing the dependence of $N_{s,mid}$ on t_b and t_{ch}, the minimum possible period (v^*) to achieve a certain electron concentration can be calculated [156]. Limitations in the maximum achievable barrier thickness could result in a slight increase of this lower bound. Figure 3.2.5 (b) shows that for a conventional $Al_{0.3}GaN$ barrier with a 1 nm-thick AlN interlayer, v^* could be of about 80 nm to reach a large $N_{s,mid}$ of 8 x 10^{12} cm^{-2} in the middle channels. Besides, v^* can be further reduced by employing a higher polarization barrier material such as $In_{0.17}AlN$, which leads to a twofold reduction of v^* compared to $Al_{0.3}GaN$, enabling to stack more channels and increase the total electron concentration ($N_{s,tot}$).

The feasibility of this approach based on undoped layers was experimentally verified by growing intrinsic multi-channel heterostructures with a different number of channels, each comprising a 23 nm

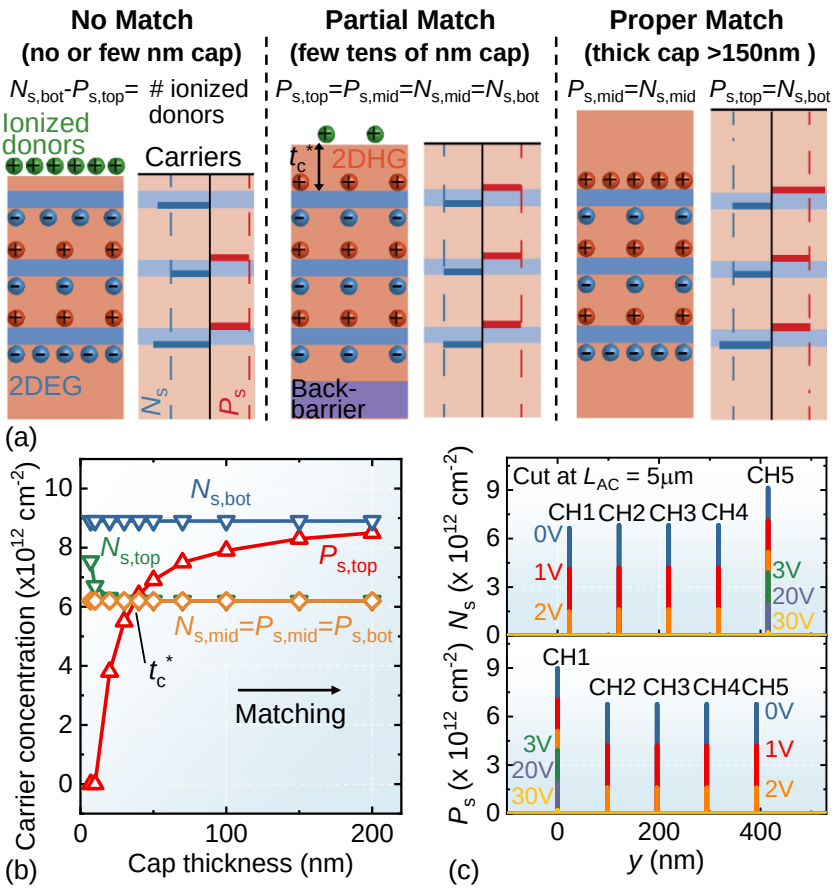


Figure 3.2.6: (a) Different matching strategies for an intrinsic multi-channel heterostructure (b) Electrons and holes concentration in the different channels as a function of the GaN cap thickness (c) N_s and P_s depletion in the 5 channels i-PSJ device as a function of V_D.

$Al_{0.3}GaN$ barrier, a 0.8 nm AlN spacer, and a 75 nm GaN channel. A linear increase of $N_{s,tot}$ with the number of channels is observed, which confirms the successful population of all the middle channels with an $N_{s,mid}$ of about 6 x 10^{12} cm^{-2} (Figure 3.2.5 (c)). This enables a significant enhancement of total electron density as the number of channels is increased, thus resulting in a large reduction of the sheet resistance from 340 Ω/sq for a single channel down to about 58 Ω/sq for a 10-channel structure, even without employing any *n*-type doping of the barrier (Figure 3.2.5 (d)).

The charge-balancing approach based on a thick GaN cap proposed for single-channel devices can also be applied to multi-channel structures to realize multi-channel intrinsic PSJs. Besides, in the absence of doping, the N_s and P_s of the buried middle channels are intrinsically matched because of charge conservation, i.e. $P_{s,mid} = N_{s,mid}$. However, charge matching for all of the channels, including especially also the top and bottom channels, is required to achieve an effective super-junction depletion. While a GaN cap is always necessary to ensure the presence of the top 2DHG ($P_{s,top}$) (Figure 3.2.6 (a)), as in the case of a single-channel, two different strategies can be investigated for multi-channel structures.

1. One can set all the N_s and P_s to be equal for all channels, i.e. $P_{s,top}= N_{s,top}= P_{s,mid} = N_{s,mid} = P_{s,bot} =N_{s,bot}$. To this end, the thickness of the GaN cap should be properly designed (t_c^* in Figure 3.2.6 (b)) to achieve $P_{s,top} = P_{s,mid,}$ as very thick GaN cap layers would result in an excess of holes (Figure 3.2.6 (a-b)). In addition, $N_{s,bot}$ should be reduced to match the

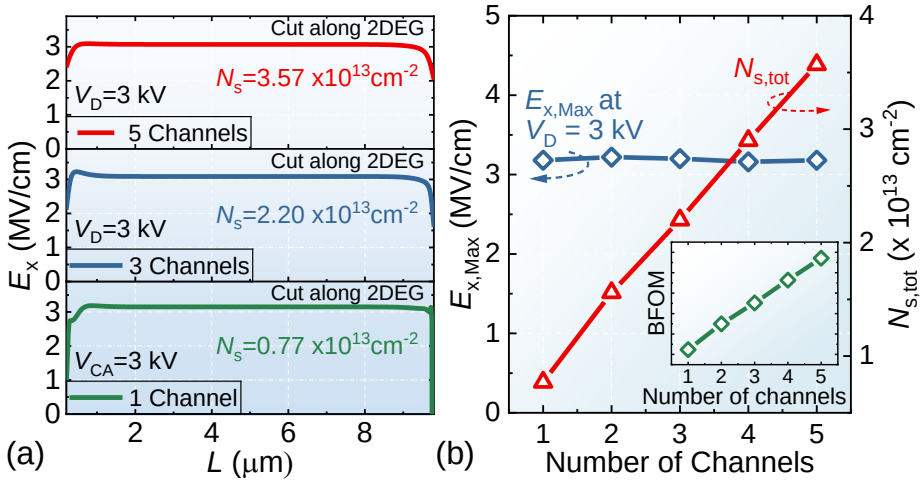


Figure 3.2.7: (a) Off-state E_x profile for a 1-,3-, and 5- channel i-PSJ device. (b) Maximum E_x and N_s as a function of the number of channels. The inset shows the linear growth of Baliga's figure-of-merit (BFOM) with the number of channels.

concentration of the middle channels by employing, for instance, a back-barrier layer (Figure 3.2.6 (a)). However, in this approach, the small cap thickness still results in ionized surface donors at the top surface (as shown in Figure 3.2.1 (b)). This leads to a fixed net charge contribution preventing proper charge matching with this strategy.

2. A second possibility consists of matching the top 2DHG and the bottom 2DEG independently from the middle channels, i.e. $P_{s,top} = N_{s,bot}$ and $N_{s,top} = P_{s,mid} = N_{s,mid} = P_{s,bot}$. In this case, the GaN cap just needs to be thick enough, as in the single-channel case, and no back-barrier is required (Figure 3.2.6 (a-b)). This method is more robust since the thick GaN cap prevents the ionization of surface donor states (Figure 3.2.1 (b)) and no precise tuning of the back-barrier is required.

A multi-channel i-PSJ based on this structure was simulated to investigate the off-state performance of a charge-balanced multi-channel device. The multi-channel stack herein investigated comprises 5 channels with a 23 nm-thick $Al_{0.3}GaN$ barrier, a 75 nm-thick GaN channel, and a 200 nm-thick GaN cap. This is structure is similar to the ones presented in Figure 3.2.5 (c-d) and in [50] showing the feasibility of such an approach. Intrinsic PSJ multi-channel devices based on this structure show a two-step depletion of the drift region. Depletion of all of the carriers in the middle channels occurs first at a V_D of ~ 3 V (Figure 3.2.6 (c)), followed by the depletion of the top 2DHG and bottom 2DEG, which have a higher carrier concentration, at V_D of ~ 30 V (Figure 3.2.6 (c)). Since a full carrier depletion is achieved at very low reverse voltage, similarly to the single-channel case, a flat E_x profile is obtained in the whole drift region (Figure 3.2.7 (a)). Most importantly, due to the efficient PSJ carrier depletion, the electric field value is independent of N_s. Therefore N_s can be significantly enlarged by adding more channels without affecting the device breakdown (Figure 3.2.7 (b)). This results in linear growth of Baliga's figure-of-merit as the number of channels is increased (inset in Figure 3.2.7 (b)), potentially overcoming the 1D GaN material limit and leading to a great improvement in the performance of GaN power devices.

In this section, we proposed a simple and robust approach to realize both single- and multi-channel intrinsic PSJ without any need for a *p*-GaN cap layer and precisely controlled doping level. Excellent intrinsic matching between was achieved and maintained for any surface condition, thus providing a

robust platform for i-PSJs. An i-PSJ device based on this approach was simulated and showed the typical SJ behavior with an ideal constant electric field in the whole drift region. The effect of donor states at the GaN top surface on the carrier mismatch was discussed and its influence on the device performance minimized. Finally, we extended this concept to intrinsic multi-channel structures, showing that much-reduced sheet resistance and excellent charge matching can be achieved simultaneously. Simulated devices based on this approach showed a flat off-state electric field profile despite the increased carrier density and thus have the potential to greatly improve Baliga's figure-of-merit.

3.3 Figures-of-Merit of Lateral GaN Power Devices: Modeling and Comparison of HEMTs and PSJs

Despite the great potential of polarization super junctions, a quantitative understanding of the figure-of-merit improvements that PSJs could achieve is missing, which is crucial to determine the validity of the technology before investing in further developments. In particular, the lack of accurate models describing the figures-of-merit of GaN lateral devices and comparing the off-state behavior of HEMTs and PSJs leads to an overestimation of HEMTs' achievable performance, which hides the full potential of PSJs. Besides, an accurate investigation of PSJs switching performance is yet to be reported.

In this section, we provide a detailed analysis and comparison of the main figures-of-merit describing the DC and switching performance of HEMT and PSJ devices. We propose a simple analytical model to describe the off-state behavior of HEMTs and PSJs based on the different carrier depletion mechanisms involved in such devices. From these results, we compare the $R_{ON,sp}$ vs V_{BR} performance of PSJs and HEMTs and demonstrate that a more than a 10-time decrease in $R_{ON,sp}$ for the same V_{BR} can be achieved by PSJs with sheet resistance (R_{sh}) of 300 Ω/sq. We show that this performance can be much improved by the use of multi-channel heterostructures to reduce R_{sh} down to ~60 Ω/sq [108]–[113]. In addition, we compare the switching losses of PSJs and HEMTs showing that a significant improvement in the R_{ON} x E_{oss} figure-of-merit, where E_{oss} is the energy stored in the device output capacitance, is achieved by PSJ devices both in the case of negligible and dominating parasitic contributions. This model enables a proper evaluation of the main figures-of-merit of lateral GaN power devices and presents the potential of PSJs to reduce both the DC and switching losses in power devices.[1]

3.3.1 Modeling

The main difference in the off-state behavior between PSJs and HEMTs comes from the origin of the 2DEG. In conventional GaN HEMTs, in which no GaN cap (or at most a thin cap of a few nanometers) is present on top of the AlGaN barrier, the source of electrons in the 2DEG are donor states at the

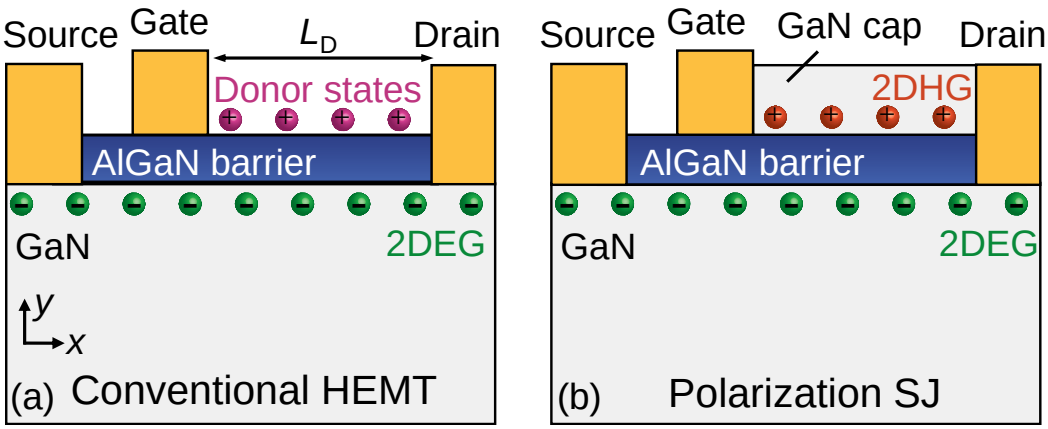


Figure 3.3.1: (a) Schematic of conventional HEMT device and (b) of a Polarization Super Junction device.

[1] This section is based on **L. Nela,** C.Erine, M.V. Oropallo, and E.Matioli, "Figures-of-Merit of Lateral GaN Power Devices: modeling and comparison of HEMTs and PSJs", *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 1066–1075, (2021). © 2021 IEEE. **Contribution: First Author.**

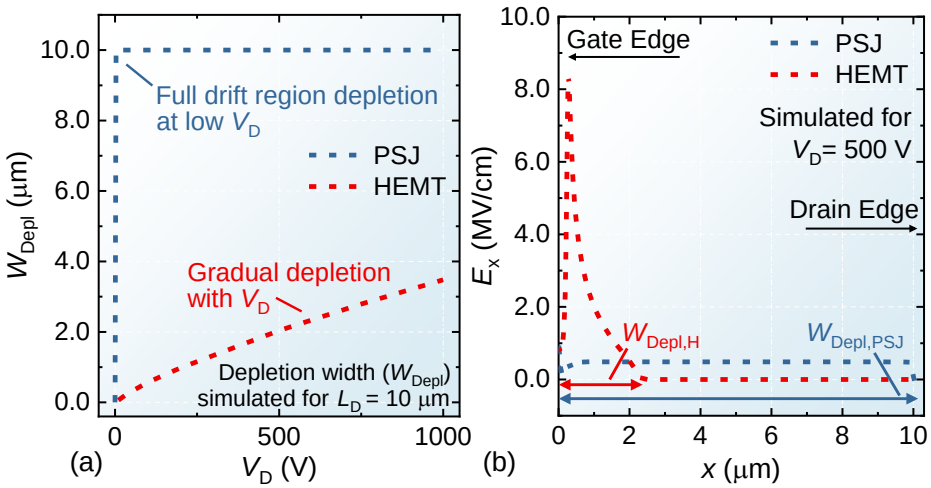


Figure 3.3.2: (a) Simulated carrier depletion width calculated from the gate edge (W_{Depl}) as a function of the off-state voltage for PSJs and HEMTs having the same drift region length. (b) Simulated off-state electric field profile in the 2DEG region along L_D for a PSJ and a HEMT device. All the simulation results presented in this section were obtained by employing the Atlas Silvaco software and using its built-in material parameters [154]. The polarization scale has been set to 0.92.

interface [55], [56] (Figure 3.3.1 (a)). These states are ionized by the polarization field, donating their electrons to the 2DEG and being left with a positive fixed charge with the same magnitude of 2DEG carrier concentration (N_s), similarly to what occurs in usual *n*-type doped semiconductors (*Section 3.2* and *Appendix D*). On the contrary, in the case of PSJs, the thick GaN cap enables the formation of a 2DHG at the top AlGaN barrier interface having the same carrier concentration of the 2DEG [146], [147] (Figure 3.3.1 (b)). The 2DHG provides the electrons to the 2DEG, without requiring the ionization of the donor states at the top interface. The key difference with respect to conventional HEMTs lies in the fact that the holes in the 2DHG are mobile and thus can be depleted in the off-state (if a proper ohmic contact between the gate/anode and the 2DHG is provided), while ionized donors are fixed charges which affect the off-state electric field profile according to the Poisson equation. This results in a neutral drift region in the off-state for PSJs, while positive fixed charges still remain in the case of HEMTs (*Section 3.2*).

To model such behaviors, the carrier depletion mechanisms for the two kinds of devices need to be investigated. Figure 3.3.2 (a) shows the simulated carrier depletion width (W_{Depl}) as a function of the off-state voltage (V_D) for a PSJ and a HEMT device. It should be noted that the off-state depletion of the drift region of a diode and a transistor are equivalent, which enables employing the same general model for both devices. Throughout the section, dashed lines represent simulated results while solid lines are used for the analytical model. Blue lines are employed for PSJs while red is used for HEMTs.

PSJ devices show a complete carrier depletion of the whole drift region length (L_D) for V_D of only a few volts. Such a depletion occurs for both electrons and holes, resulting in a neutral drift region. On the other side, HEMTs present a smaller W_{Depl}, which requires much larger V_D values to grow and more closely resembles the case of doped semiconductors. The two different depletion mechanisms are directly linked to the off-state electric field profile in such devices. The efficient carrier depletion and the neutral drift region of PSJs lead to a flat electric field profile in the whole L_D while the smaller W_{Depl} along with the presence of fixed positive charges in the depletion region result in a non-uniform electric field profile with a peaked shape for HEMTs (Figure 3.3.2 (b)). While based on these results PSJ devices intuitively should present improved off-state performance, an analytical model describing these devices is necessary to draw more quantitative conclusions while maintaining a detailed understanding of the

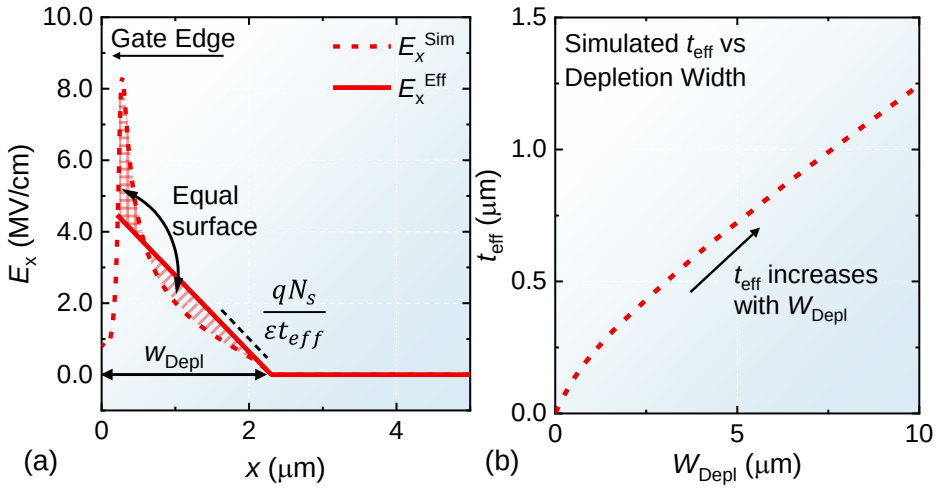


Figure 3.3.3: (a) Simulated off-state electric field (E_x^{Sim}) along L_D in the 2DEG region for a HEMT device and corresponding approximated linear field profile (E_x^{Eff}) assumed in the model. (b) t_{eff} as a function of the depletion width extracted from the device simulation.

physical mechanisms involved. In addition, this would enable determining the upper-performance limit of HEMTs and PSJs and properly estimating their potential and figures-of-merit for power conversion applications.

The off-state electric field profile for a HEMT is in general a complex function due to the device's two-dimensional architecture. Indeed, while a uniformly-doped semiconductor can be considered as a 1D problem, the presence of a sheet charge requires a two-dimensional treatment. Typical mathematical methods to address this problem are based on conformal mapping methods [157]–[161], which however result in very complicated and non-analytical solutions. Here, we propose a simplified approach that leads to an analytical solution enabling direct comparison with PSJs, while still accurately describing the physical mechanisms that determine the device operation. In particular, the HEMT off-state electric field ($E_{x,HEMT}$) along the drift region direction (x) in the 2DEG region is approximated by a linear function having W_{Depl} as x-axis intercept and a slope such that the voltage drop in the depleted region is conserved (Figure 3.3.3 (a)). The resulting expression is:

$$E_{x,HEMT} = \frac{qN_{s,HEMT}}{\varepsilon t_{eff}}\left(x - W_{Depl}\right) \qquad 3.1$$

where q is the magnitude of the electronic charge, $N_{s,HEMT}$ is the 2DEG concentration in the HEMT device and ε is GaN dielectric constant. t_{eff} is a geometrical parameter (in cm) which accounts for the electric field extension in the vertical direction due to its 2D distribution between the gate electrode and the undepleted 2DEG. This model enables us to treat a HEMT similarly to a conventional 1D doped device, greatly simplifying the mathematical expressions. It should be noted that the assumption of a linear field overestimates the breakdown voltage of HEMT devices, which in reality presents a more peaked electric field profile. However, since the goal of this work is to present the potential of PSJs with respect to conventional HEMT structures, this assumption only results in an underestimation of the performance improvement brought by PSJ. Besides, this model represents an improvement compared to previous works, in which the E_x profile of HEMTs is assumed to be flat in the whole drift region [140]. Such a hypothesis is not physically accurate due to the presence of ionized donor states with a positive charge and actually describes the case of PSJ devices, preventing a fair comparison between the two device architectures. The geometrical parameter t_{eff} accounts for the 2D distribution of

the electric field between the gate electrode and the edge of the undepleted 2DEG. For this reason, it only depends on the device's geometrical parameters, such as the gate metal thickness and the dielectric constant of the passivation layer, and the depletion width, i.e. the separation between the gate electrode and the undepleted 2DEG. In particular, t_{eff} increases as W_{Depl} grows due to the more 2D shape of the electric field (Figure 3.3.3 (b)). t_{eff} is instead independent of the specific combination of N_s and V_D that was required to achieve a certain depletion width. Indeed, such a combination only influences the magnitude of the electric field but not its distribution. While a mathematical formula for t_{eff} is challenging to obtain, its value can be extracted by considering W_{Depl} vs V_D from simulations (Figure 3.3.2 (a)) and using the expression:

$$t_{\mathrm{eff}} = \frac{qN_{\mathrm{s,HEMT}}W_{\mathrm{Depl}}^2}{2\varepsilon V_{\mathrm{D}}} \qquad 3.2$$

which is derived from eq. 3.1. Figure 3.3.3 (b) shows t_{eff} as a function of W_{Depl} for a HEMT with a 30 nm-thick $Al_{0.25}GaN$ barrier, 100 nm-thick gate contact, and 200 nm-thick Si_3N_4 passivation layer. Since the field distribution, and thus $t_{eff,}$ depends on the exact device structure, slight adjustments to t_{eff} may be required in case a very different device architecture is used. However, for conventional device architectures, variations of t_{eff} well below 10 % are expected

To model the off-state behavior of PSJs, the carrier depletion in these devices needs to be properly described. Figure 3.3.4 (a) shows the N_s as a function of the off-state voltage for different $Al_{0.25}GaN$ barrier thicknesses (t_b). While the N_s value at equilibrium (V_D = 0 V) increases for larger t_b, the carrier depletion varies linearly with the off-state voltage for all barrier thicknesses, which can be described by introducing an effective barrier capacitance (C_b) from the linear fit of the N_s vs V_D curve. Figure 3.3.4 (b) shows that C_b, extracted from Figure 3.3.4 (a), increases linearly with the inverse of the barrier thickness (t_b^{-1}), with a slope equal to the dielectric constant of the AlGaN barrier. This behavior allows us to model the carrier depletion in PSJs with a simple parallel plate capacitor having the barrier as the insulator between the sheet charges of the 2DHG and 2DEG, with the gate providing an ohmic contact to the 2DHG and the drain to the 2DEG (Figure 3.3.4 (b) inset). The 2DHG can be seen as acting

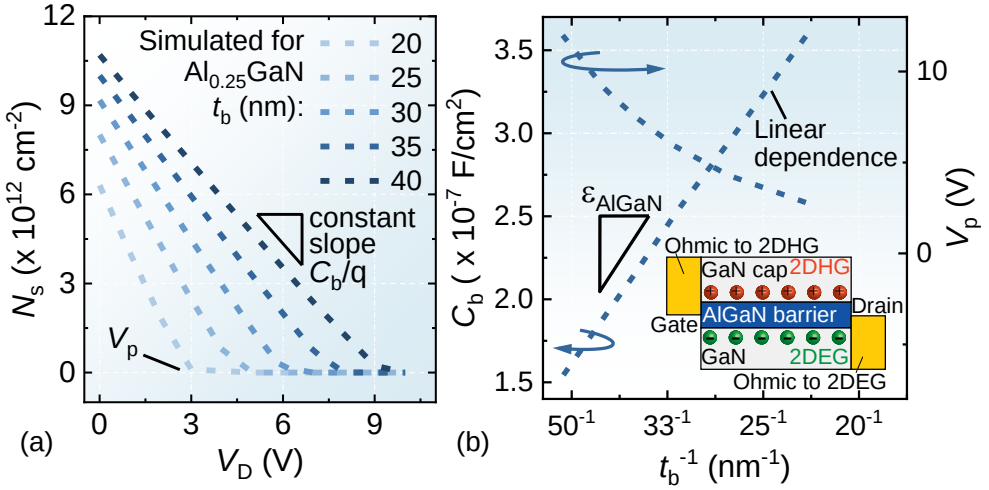


Figure 3.3.4: (a) Simulated carrier concentration N_s as a function of V_D for different $Al_{0.25}GaN$ barrier thicknesses. N_s was extracted by integrating the electron concentration in the 2DEG region along the vertical direction. A cut in the middle of the device's drift region was taken to avoid any possible carrier depletion from the contacts. (b) Barrier capacitance (C_b) and PSJ pinch off-voltage (V_p), extracted from Figure 3.3.4 (a), as a function of the barrier thickness. The bottom-right inset shows a schematic of the simplified parallel plate capacitor model used to describe carrier depletion in PSJ devices.

similarly to a usual gate that forms a parallel-plate capacitor and uniformly depletes the 2DEG over the whole drift region, with a threshold voltage comparable to that of a typical Schottky gate. It should be noted that such a model is valid because of the small pinch-off voltage (V_p) required to completely deplete PSJ devices (Figure 3.3.4 (b)) and the large Schottky barrier present between the drain metal and the 2DHG. In this condition, the conventional lateral depletion at the edges of the electrodes is negligible with respect to the drift region length and no significant leakage is present through the Schottky barrier. Besides, the barrier thickness is much smaller than L_D, which allows neglecting the parasitic capacitance between the two electrodes. The pinch-off voltage is only a few Volts for any realistic value of AlGaN barrier thickness (Figure 3.3.4 (b)) and could be further reduced by employing higher polarization materials for the barrier, such as InAlN or AlN, which enable reducing t_b for a given N_s. Thanks to the small value of V_p compared to the breakdown voltage values considered in this work, the off-state electric field profile can be considered approximately flat in the whole PSJ drift region ($L_{D,PSJ}$) and be given by:

$$E_{x,PSJ} = -\frac{V_D}{L_{D,PSJ}} \tag{3.3}$$

3.3.2 Static Figure-of-Merit Comparison

Based on the electric field profiles for HEMTs and PSJs described in eqs. 3.1 and 3.3, we can compare the DC performance of the devices. It should be noted that TCAD simulation was only employed to extract the t_{eff} parameter and to show the different physical mechanisms involved. The following analysis on the device figure-of-merit is entirely based on an analytical treatment. The breakdown voltage is typically obtained by considering the onset of avalanche breakdown by impact ionization, with the ionization integral being simplified by using Fulop's power law [140], [162]. Solving the resulting ionization integral using eqs. 3.1 and 3.3, and considering a complete depletion of the drift region, as in the case of a well-designed power device, one obtains a relation between V_{BR} and the drift region length for both device types:

$$V_{BR,PSJ}\,[\mathrm{V}] = 0.94 \times 10^6\, L_{D,PSJ}^{6/7}\,[\mathrm{cm}] \tag{3.4}$$

$$V_{BR,HEMT}\,[\mathrm{V}] = 0.63 \times 10^6\, L_{D,HEMT}^{6/7}\,[\mathrm{cm}] \tag{3.5}$$

These expressions, which depend only on the E_x profile and not on the carrier concentration, set an important link between the drift region length of PSJs and HEMTs. In particular, for a given V_{BR}, $L_{D,PSJ} = 0.67 \times L_{D,HEMT}$, which means that PSJ devices can have a shorter drift region to hold the same voltage thanks to the improved off-state electric field profile. Besides, one obtains also a relation between V_{BR} and N_s for HEMTs

$$V_{BR,HEMT}[\mathrm{V}] = 2.5 \times 10^{15} \times \left(N_{s,HEMT}[\mathrm{cm}^{-2}]/t_{eff}[\mathrm{cm}]\right)^{-3/4} \tag{3.6}$$

while, thanks to the very small value of V_p for any realistic carrier concentration, in a first approximation V_{BR} does not depend on N_s in PSJs.

For a lateral device, the specific on-resistance ($R_{ON,SP}$) is given by:

$$R_{\mathrm{ON,SP}} = \frac{L_{\mathrm{D}}^2}{q\mu N_{\mathrm{s}}} \tag{3.7}$$

with μ the electron mobility. By inserting eq. 3.4 (for a PSJ) and eqs. 3.5, and 3.6 (for a HEMT) in eq. 3.7, one can extract the expression of the device minimum $R_{\mathrm{ON,SP}}$ achievable for a certain V_{BR}, which represents the main figure-of-merit to assess the upper-performance limit of power devices:

$$R_{\mathrm{ON,sp,HEMT}}\,[\Omega \text{ x cm}^2] = \frac{5.2 \text{ x } 10^{-16}}{\mu[\mathrm{cm^2/Vs}]\, t_{\mathrm{eff}}[\mathrm{cm}]} V_{\mathrm{BR}}^{11/3}[\mathrm{V}] \tag{3.8}$$

$$R_{\mathrm{ON,sp,PSJ}}\,[\Omega \text{ x cm}^2] = 1.15 \text{ x } 10^{-14} \text{ x } R_{\mathrm{sh}}[\Omega] V_{\mathrm{BR}}^{7/3}[\mathrm{V}] \tag{3.9}$$

where R_{sh} is the heterostructure sheet resistance ($R_{\mathrm{sh}} = 1/q\mu N_{\mathrm{s}}$). To obtain t_{eff} as a function of V_{BR}, one can apply eq. 3.5 to Figure 3.3.3 (b) in order to link W_{Depl} to V_{BR} since, for a well-designed power HEMT, W_{Depl} corresponds to L_{D} at the breakdown. Figure 3.3.5 (a) shows the dependence of t_{eff} on V_{BR}, which can be inserted in eq. 3.8 to plot HEMTs' specific on-resistance (Figure 3.3.5 (b)). To further simplify eq. 3.8 and obtain a more general expression, one can approximate t_{eff} as a linear function of V_{BR} (Figure 3.3.5 (a)). In addition, eq. 3.9 can be expressed as a function of N_{s} to offer a direct comparison between $R_{\mathrm{ON,sp,HEMT}}$ and $R_{\mathrm{ON,sp,PSJ}}$:

$$R_{\mathrm{ON,sp,HEMT}}[\Omega \text{ x cm}^2] = \frac{7\,x\,10^{-9}}{\mu\left[\frac{\mathrm{cm}^2}{\mathrm{Vs}}\right]} V_{\mathrm{BR}}^{8/3}[\mathrm{V}] \tag{3.10}$$

$$R_{\mathrm{ON,sp,PSJ}}\,[\Omega \text{ x cm}^2] = \frac{0.7 \text{ x } 10^5}{\mu\left[\frac{\mathrm{cm}^2}{\mathrm{Vs}}\right] N_{\mathrm{s}}[\mathrm{cm}^{-2}]} V_{\mathrm{BR}}^{7/3}[\mathrm{V}] \tag{3.11}$$

Finally, the reduction in the specific on-resistance for PSJs compared to HEMTs can be derived considering the ratio between eqs. 3.11 and 3.10 and assuming the same mobility for the two devices:

$$\frac{R_{\mathrm{ON,sp,PSJ}}}{R_{\mathrm{ON,sp,HEMT}}} = \frac{1}{N_{\mathrm{s}}[\text{x } 10^{13}\mathrm{cm}^{-2}] V_{\mathrm{BR}}^{1/3}[\mathrm{V}]} \tag{3.12}$$

A significant improvement in the $R_{\mathrm{ON,SP}}$ vs V_{BR} limit can be achieved by PSJs using conventional AlGaN/GaN single-channel heterostructures. For instance, $R_{\mathrm{ON,SP,PSJ}}$ can be reduced up to 10 times compared to $R_{\mathrm{ON,SP,HEMT}}$ for typical heterostructures having $R_{\mathrm{sh}} \sim 300\ \Omega$/sq (or $N_{\mathrm{s}} \sim 1 \text{ x } 10^{13}$ cm^{-2}) for a breakdown voltage of 1000 V (Figure 3.3.5 (b)), with a further reduction when devices with larger V_{BR} are considered (eq. 3.12). It should be noted that often the electric field profile of HEMT devices is approximated to be flat in the whole L_{D}, which however erroneously results in the same $R_{\mathrm{ON,SP}}$ vs V_{BR} limit as for PSJ devices. Nevertheless, as previously explained, such an assumption is not physically accurate and leads to an overestimation of the potential of HEMT devices. This explains why real HEMTs present performance very far from this limit, which is instead properly described by the proposed model (Figure 3.3.5 (b)).

In addition, we observe that for HEMTs, the V_{BR} depends on N_{s} (see eq. 3.6) and thus the carrier concentration does not appear in eqs. 3.8 and 3.10. This is the usual situation for conventional semiconductor devices for which there is a trade-off between the carrier concentration and the blocking capabilities. On the contrary, R_{sh} (and thus N_{s}) does not affect the off-state electric field (eq. 3.3) and

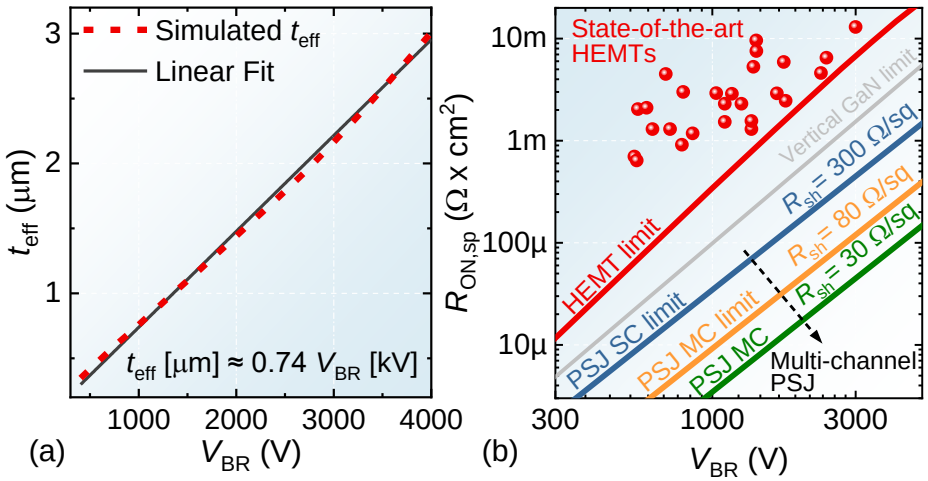


Figure 3.3.5: (a) t_{eff} as a function of the breakdown voltage extracted from Figure 3.3.3 and eq. 3.5, and corresponding linear fit (in black). (b) $R_{ON,SP}$ vs V_{BR} benchmark for HEMTs and PSJs with single and multiple channel heterostructures (SC and MC respectively) calculated from eqs. 3.8 and 3.9. Electron mobility of 2000 cm^2/Vs was used. The solid lines represent the calculated theoretical limits for each architecture while the performance of state-of-the-art HEMTs devices in literature is reported in red dots.

the breakdown voltage for PSJs (eqs. 3.9 and 3.11), which allows increasing the device conductivity without degrading its blocking performance. While, one could achieve a low sheet resistance in conventional single-channel heterostructures by proper design of an AlN or AlInN barrier, a more effective way to significantly reduce the heterostructure R_{sh} is by using multiple parallel channels, which enable to increase the carrier concentration without degrading the mobility [50], [109], [113]. Besides, the growth of the multi-channel structure typically requires only a small increase in the growth time compared to the rest of the heterostructure, thus providing a cost-effective solution to significantly reduce the on-resistance in power devices. Following this approach, AlGaN/GaN multi-channel heterostructures with R_{sh} ~ 60 Ω/sq have been shown experimentally (see *Section 3.2.3*), both with doped and undoped barrier layers, and power devices based on these structures have been demonstrated [108]–[110], [112], [113], revealing the feasibility of achieving high voltages in such high conductivity structures. Further increase in the number of channels and higher polarization barrier materials (such as lattice-matched InAlN [163] and AlN [99]) have resulted in structures with R_{sh} value down to ~ 30 Ω/sq. As shown in Figure 3.3.5 (b), the reduced sheet resistance of multi-channel PSJ devices would enable a considerable improvement in the $R_{ON,SP}$ vs V_{BR} trade-off, resulting in a decrease of the device resistance without affecting its off-state behavior.

3.3.3 Switching Losses Comparison

The different carrier depletion mechanisms in HEMTs and PSJs directly impact the device output capacitance (C_{oss}), which largely determines its switching losses. In particular, during hard switching, the energy stored in C_{oss} (E_{oss}) is dissipated at each switching cycle, resulting in the following expression for the hard-switching losses [164]–[166] (where losses during the turn-off are typically negligible for GaN devices and thus not considered [167], [168]):

$$P_{SW} = f E_{oss} + P_{IV} \qquad 3.13$$

where f is the operating frequency and P_{IV} is a term related to the current-voltage overlap during the switching transition.

The device C_{oss} can be modeled as the sum of a first term describing the carrier depletion in the drift region [60], [157], [169] (which depends on V_D), and a second contribution (C_p) related to the device geometry and the parasitic capacitance terms (which is independent on voltage) [157], [170]. According to the previous analysis on the carrier depletion (Figure 3.3.3 and Figure 3.3.4), we can approximate C_{oss} as a step function for PSJs and as an increasing function $\sim 1/\sqrt{V_D}$ for HEMTs:

$$C_{\text{oss,PSJ}} = \begin{cases} C_b L_{\text{D,PSJ}} + C_p & \text{for} \quad V_D \le V_p \\ C_p & \text{for} \quad V_D > V_p \end{cases} \tag{3.14}$$

$$C_{\text{oss,HEMT}} = \sqrt{\frac{q\varepsilon t_{\text{eff}} N_{\text{s,HEMT}}}{2V_D}} + C_p \tag{3.15}$$

By integrating eq. 3.14 and 3.15 with respect to V_D, the device output charge Q_{oss} is obtained, and a second integration results in E_{oss}:

$$E_{\text{oss,PSJ}} = \begin{cases} {}^1\!/_2\, C_b V_D^2 L_{\text{D,PSJ}} + {}^1\!/_2\, C_p V_D^2 & \text{for } V_D \le V_p \\ {}^1\!/_2\, C_b V_p^2 L_{\text{D,PSJ}} + {}^1\!/_2\, C_p V_D^2 & \text{for } V_D > V_p \end{cases} \tag{3.16}$$

$$E_{\text{oss,HEMT}} \ge \frac{\sqrt{2\varepsilon q N_{\text{s,HEMT}} t_{\text{eff}}}}{3} V_D^{3/2} + \frac{1}{2} C_p V_D^2 \tag{3.17}$$

where the $\ge$ sign in eq. 3.17 results from assuming t_{eff} to be an increasing function with V_D, which is verified in Figure 3.3.3 (b). In order to analyze this result, two different cases will be considered, i.e. the situation in which the carrier depletion is the main term in C_{oss} (C_p negligible) and the case in which C_p is instead the dominant term. The relative magnitude of the two terms can strongly depend on the device structure and its packaging strategy, making it useful to consider both cases. Besides, to compare devices having the same V_{BR}, eqs. 3.4, 3.5, and 3.6 will be considered, which impose $L_{\text{D,PSJ}} = 0.67 \text{ x } L_{\text{D,HEMT}}$ and set a relation between the HEMT carrier density and its V_{BR}.

The output charge for a negligible C_p is shown in Figure 3.3.6 (a). Since Q_{oss} directly depends on the depletion width, a similar behavior as in Figure 3.3.2 (a) is observed, with the PSJ output charge increasing sharply with V_D until the full drift region depletion at $V_D = V_p$ and with the HEMT Q_{oss} gradually rising over the whole V_D range. These differences in the Q_{oss} vs V_D profile result in an E_{oss} value that is larger for PSJs at low operating voltages but becomes much smaller than that of HEMTs when large V_D values are considered (Figure 3.3.6 (b)). In particular, comparing the important switching figure-of-merit (FOM) R_{ON} x E_{oss} at the device rated voltage for PSJs and HEMTs, an important relationship is obtained:

$$\frac{R_{\text{ON,PSJ}} \text{ x } E_{\text{oss,PSJ}}}{R_{\text{ON,HEMT}} \text{ x } E_{\text{oss,HEMT}}} = 0.67 \frac{V_p}{V_{BR}} \quad \text{for} \quad C_p = 0 \tag{3.18}$$

Since the PSJs pinch-off voltage V_p is much smaller than the breakdown voltage of typical power devices (Figure 3.3.4 (b)), PSJs enable to achieve a significant reduction in the R_{ON} x E_{oss} FOM, which increases as devices with larger voltage ratings are considered.

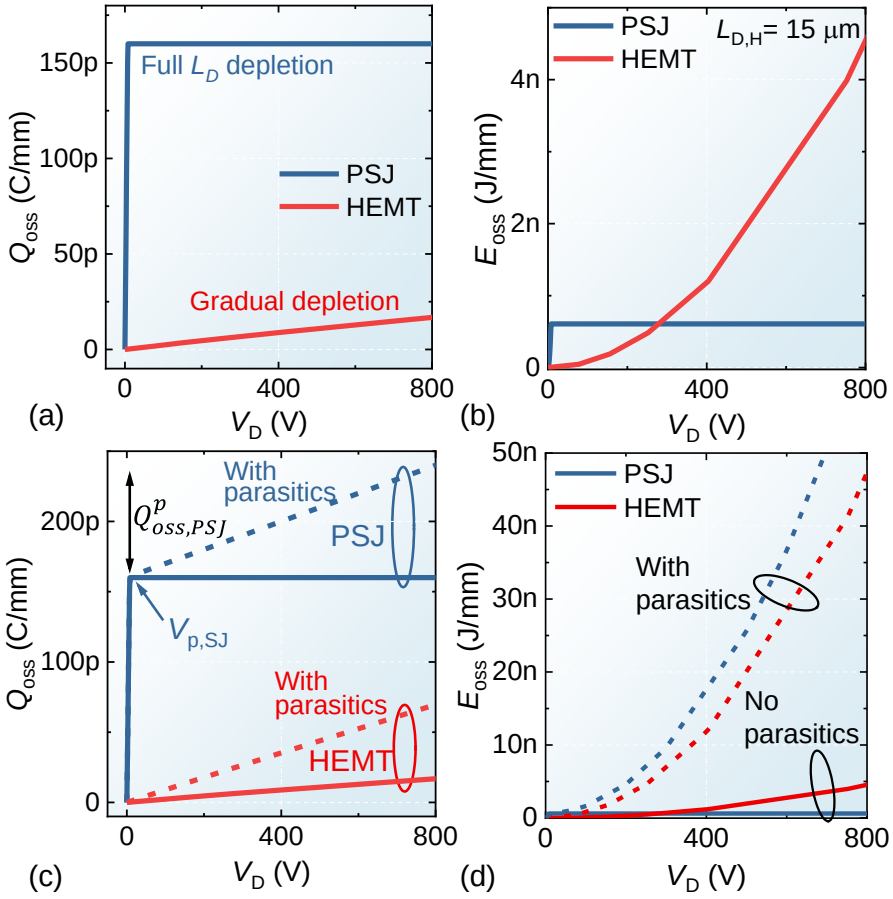


Figure 3.3.6: (a) Q_{oss} and (b) E_{oss} as a function of V_D for HEMT and PSJ devices in the case of negligible C_p calculated from eqs. 3.16 and 3.17. (c) Q_{oss} and (d) E_{oss} as a function of V_D for HEMT and PSJ devices for a negligible (solid lines) and non-negligible (dotted lines) parasitic capacitance contribution. In the case of non-negligible C_p, its value was set to 1 pF/cm for PSJs and 0.66 pF/cm for HEMTs, which reflects the different L_D required by the two devices to achieve the same V_{BR}.

In real power devices, parasitic capacitance contributions to C_{oss} related to the device geometry rather than the drift region depletion can become significant depending on the device architecture. While an exact estimation requires the precise knowledge of the device structure, here a C_p of 1 pF/cm for $L_{D,PSJ}$ of 10 µm is assumed, which is a typical value for multi-finger scaled-up devices [157], [159]. Besides, we consider $C_p \sim 1/L_D$, resulting in a C_p value of 0.66 pF/cm for $L_{D,HEMT}$ of 15 µm. This assumption is favorable for HEMTs as parasitic terms usually have a weaker dependence on L_D for typical device dimensions [157], [159], [171].

Figure 3.3.6 (c) presents Q_{oss} as a function of V_D for non-negligible C_p. As a result of the parasitic contributions, an increase of Q_{oss} is observed, which is larger for PSJs due to the shorter drift region length. The corresponding E_{oss} vs V_D curves are presented in Figure 3.3.6 (b), which shows a dominant contribution from the C_p term with respect to the depletion contribution. In this situation, PSJs present a larger E_{oss} value, due to their shorter L_D. However, a fair comparison between the two devices requires considering the R_{ON} x E_{oss} FOM:

$$\frac{R_{ON,PSJ} \text{ x } E_{oss,PSJ}}{R_{ON,HEMT} \text{ x } E_{oss,HEMT}} = \frac{3.4 \text{ x } 10^{20} \text{x } t_{eff}[\text{cm}]}{N_{s,PSJ}[\text{cm}^{-2}] V_{BR}^{4/3}[\text{V}]} \qquad 3.19$$

which can be further simplified in case the linear fit of t_{eff} vs V_{BR} (Figure 3.3.5 (a)) is used:

$$\frac{R_{\mathrm{ON,PSJ}} \times E_{\mathrm{oss,PSJ}}}{R_{\mathrm{ON,HEMT}} \times E_{\mathrm{oss,HEMT}}} = \frac{2.5}{N_{\mathrm{s,PSJ}}[\times 10^{13}\,\mathrm{cm}^{-2}]V_{\mathrm{BR}}^{1/3}[\mathrm{V}]} \qquad 3.20$$

The decoupling of N_s from the off-state performance for PSJ devices results in a better R_{ON} x E_{oss} FOM, which improves as the device V_{BR} increases (Figure 3.3.7). Besides, by employing multi-channel structures with larger N_s it is possible to further reduce R_{ON} x E_{oss} to values 10 times lower than for HEMT devices.

Finally, for what concerns the P_{IV} contribution in eq. 3.13, this term is proportional to the external load current and is linked to the time required to discharge C_{oss} through the device channel. This time is usually determined by the circuit operation and by the addition of an external gate resistor to control the *dV/dt*. In these conditions, HEMTs and PSJs would exhibit similar P_{IV} as this term is entirely controlled by the external circuit. However, in the absence of a gate resistor or in the case of very low gate-path resistance, the transition speed depends only on the device properties. In this case, the strong non-linearity of C_{oss} for PSJ devices (see eq. 3.14) results in a reduced overlap term at high voltages with respect to HEMTs. This is due to the efficient carrier depletion in PSJs, which leads to a very low C_{oss} value for off-state voltages above the pinch-off and translates in a reduction of the P_{IV} overlap term compared to HEMTs, similarly to what has been reported for Si devices [172]. Thus, since for PSJ devices the P_{IV} term is smaller or equal than for HEMTs while the E_{oss} contribution is much-reduced for any condition, we can conclude that PSJs result in a significant decrease of the overall switching losses.

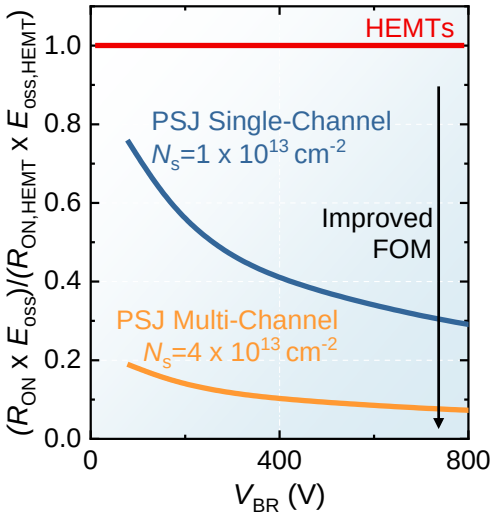


Figure 3.3.7: Ratio between the R_{ON} x E_{oss} figure-of-merit for PSJs and HEMTs in the case of non-negligible parasitic capacitance contributions calculated from eq. 3.19.

3.3.4 Model Boundaries

GaN lateral devices typically present a large density of traps at the heterostructure top interface. Electrons trapped in these surface states during the off-state partly deplete the 2DEG close to the gate edge and alleviate the electric field peak, resulting in an improvement of the device breakdown voltage [132], [173]–[175] through a virtual gate effect. Yet, this mechanism is highly undesirable as it degrades the device resistance in the on-state, resulting in current collapse phenomena [36], [176]. A similar reasoning can also be applied to trap states in the buffer layer, which are often introduced to increase

its resistivity but can act as trapping centers for electrons in the 2DEG (*Section 2.4*). Thus, a more meaningful indicator of the device performance is represented by the dynamic on-resistance rather than the DC R_{ON}, which does not take into account trapping effects. In this work, the presence of trap states has not been considered as the exact estimation of their density and energy level is highly dependent on the device design and passivation strategy. However, all the analyses here reported remain valid by simply replacing R_{ON} with the dynamic on-resistance ($R_{ON,dyn}$) measured for experimental devices.

GaN layers also present a certain concentration of unintentional impurities (e.g. Si or O) due to contaminations during the growth, which can act as fixed net charges and affect the electric field profile. Nevertheless, recent advances in MOCVD growth have enabled impurity concentrations as low as 3 x 10^{15} cm^{-3} [177], [178], preventing significant effects on the device's off-state behavior. In this work, the role of impurities has not been included since their concentration can vary significantly depending on the growth technique and parameters, which prevents drawing any general conclusion. However, in the case of a significant presence of impurities, this can be readily accounted for in the presented equations by including an additional fixed net charge term.

Finally, GaN HEMTs usually also have few field plate (FP) structures (*Section 1.4.2*). While the analytical treatment of field plates is rather straightforward [157], [160], their design varies significantly from device to device making it difficult to provide a general model. Yet, some considerations can be drawn. One of the main goals of FPs is to reduce the electric field peak at the gate edge. While the field profile in the FPs region differs from the one here presented, FPs typically extend only for a few microns and the majority of the off-state voltage falls on the portion of the drift region without FP. This situation is well described by the proposed model, which can be extended to include the presence of FPs [157], [160] once the precise device structure under investigation is known. Finally, the use of FPs results in an increased C_{oss} parasitic contribution (C_p) due to the reduced distance between electrodes, which increases the switching losses and poses an additional trade-off between E_{oss} and the blocking performance. The proposed model and analysis offer precious general insights into the operation mechanisms of two investigated devices and can be easily adapted to a specific device architecture, once its precise structure is known.

In this section, we provided a detailed analysis and comparison of the main figures-of-merit describing the DC and switching performance of HEMT and PSJ devices. We proposed a simple analytical model to describe the off-state behavior of HEMTs and PSJs based on the different carrier depletion mechanisms involved in such devices. Based on these results, we showed that a 10-times decrease in $R_{ON,sp}$ for the same V_{BR} can be achieved by single-channel PSJs, which can be further improved by the use of multi-channel heterostructures to reduce the sheet resistance. In addition, we compared the switching losses of PSJs and HEMTs showing that PSJ devices result in a significant improvement in the R_{ON} x E_{oss} figure-of-merit both in the case of negligible and dominating parasitic contributions. This model enables a proper evaluation of the main figures-of-merit of lateral GaN power devices and shows the potential of PSJs to reduce both the DC and switching losses in power devices.

4 High-Performance GaN Lateral Schottky Barrier Diodes towards Power ICs

4.1 Introduction

High-voltage SBDs are a fundamental building block for any power conversion circuit. Some of the most common applications include protection systems, antiparallel diodes for MOSFET reverse conduction, and charge pump architectures. Besides, the architecture simplicity coming from the absence of driving circuits makes such topologies easy to design, robust and cost-effective. GaN-on-Si transistors have shown excellent performance thanks to the superior material properties of the AlGaN/GaN heterostructure and similar consideration should apply to Schottky Barrier Diodes (SBDs) too. Besides, the shared GaN-on-Si platform would allow for straightforward monolithic integration of power HEMTs and SBDs, paving the way to future power integrated circuits (ICs).

Yet, while GaN transistors have quickly developed and many commercial solutions are provided by several vendors, no GaN SBD is on the market. This absence is typically filled by SiC diodes, which rely on more mature technology and have shown excellent performance. Nevertheless, the development of GaN SBDs is a key requirement for GaN full maturity and widespread adoption. On one hand, discrete GaN SBDs would provide a competitive alternative to SiC devices in terms of performance while bringing a significant price reduction, thanks to the cost-effective GaN-on-Si platform. On the other hand, the integration of multiple GaN SBDs and HEMTs on the same chip would significantly expand the design possibilities, enabling power ICs with a large variety of topologies and able to operate at high frequency. This would further reduce the overall circuit cost while resulting in more compact and efficient solutions.

One of the main hindrances to AlGaN/GaN diodes development is the intrinsic trade-off in SBDs between the device forward characteristics and its reverse blocking capabilities. In conventional SBDs architectures, such a trade-off is summarized by the Schottky barrier: a large barrier results in reduced leakage current (I_R) and increased turn-on voltage (V_{ON}) and while a small barrier leads to good forward characteristics at the expense of large device leakage and low breakdown voltage (V_{BR}). Such a situation is exacerbated by the AlGaN/GaN lateral architecture, which results in uneven electric field distribution in the channel with a large potential drop on the Schottky barrier. Efficient power diodes require at the same time low I_R and good blocking capabilities, in combination with reduced forward voltage (V_F) to minimize conduction losses.

Recent works have shown significant improvement in the SBDs performance by relying on different architectures such as recessed anodes [46], [179], [180], field plates [62], [181] and Tri-Gate / Tri-anode hybrid structures [57]–[59], [88], [110]. In particular, GaN SBDs adopting a Tri-anode architecture have demonstrated large breakdown voltage (V_{BR}) up to 2 kV with low turn-on voltage and on-resistance

[59]. However, despite these remarkable results, previous works focused only on the SBD DC performance, trying to optimize the V_F vs I_R trade-off. On the contrary, the switching performance of AlGaN/GaN Tri-anode devices is still unexplored. Nevertheless, a careful assessment of the switching losses in power diodes is essential for an overall improvement of device efficiency. Switching losses occur every time the diode is commuted from the conducting state to the off-state and strongly depend on the charge that is stored in the device. While GaN devices promise to significantly increase converters' operating frequency, a careful study of the device switching mechanism is of great importance. Indeed, at MHz frequency the diode switching losses can become comparable or even larger than the conduction contribution, greatly influencing the device operation.

In particular, despite the promising DC performance of Tri-Gate / Tri-anode devices, the effect of the Tri-Gate 3D architecture on the switching behavior of lateral AlGaN/GaN-based devices has not yet been investigated and there are concerns about the possible capacitance increase due to its 3D nature, as it has been reported for other technologies such as bulk FinFETs [182]. Therefore, it is fundamental to investigate the switching performance of GaN Tri-anode devices to determine their potential to operate at high-frequency.

In addition, the monolithic integration of several fast-switching and high-performance GaN SBDs on the same chip or together with GaN HEMTs would significantly expand the design possibilities, enabling power ICs with a large variety of topologies and able to operate at high-frequency. For example, the increased switching frequency represents a key advantage for converter architectures based on switching capacitors, in which no magnetic components are needed, as this would enable higher power transfer with reduced passive component size, leading to ultra-compact, high-efficiency power converters [183], [184]. Possible applications that would highly benefit from such features, and operate in the few hundreds of Watts range, include photovoltaics, lighting, and robotics, among others [185]. Despite the great potential of such technology, few works have focused on the switching performance of GaN SBDs and on their comparison with counterpart Si and SiC devices. In addition, the GaN ICs' behavior and performance in real circuit applications are still largely unexplored.

Finally, while the Tri-gate / Tri-anode architecture offers great advantages for GaN SBDs as it enables excellent DC and switching performance, it also requires lithographic resolutions ~ 200 nm. While a significant improvement in the lithographic resolution is expected in the coming years for GaN process lines, especially because of the increasing number of integrated GaN logic devices required for the device driving, alternative SBD architectures based on a readily available fabrication process would be very appealing as they could be immediately adopted and enable fast-commercialization of GaN SBDs.

This chapter is organized into three sections that address the aforementioned challenges.

1. In the first section, we investigate the impact of the Tri-anode architecture on the SBD switching performance. We show that Tri-anode SBDs can offer not only excellent DC performance but can also significantly improve the diode dynamic performance, which is explained considering the different depletion mechanisms of Tri-anode devices. This results in a significant decrease in the R_{ON} x E_{oss} figure-of-merit with respect to conventional GaN SBDs architectures and thus in more efficient devices.

2. In the second section, we compare the presented devices to similarly-rated Si fast-recovery diodes and SiC SBDs, showing their reduced reverse-recovery charge and excellent dynamic behavior. The potential of the presented diodes for high-frequency integrated power circuits is demonstrated by integrating 8 diodes on the same chip, to realize a monolithically integrated diode multiplier operating at 1 MHz and able to provide up to 8x multiplication of the input voltage. The GaN IC performance is compared to the same circuit realized by discrete Si and SiC commercial devices, showing a significant improvement in high-frequency operation along with a large size reduction.

3. Finally, we propose an alternative AlGaN/GaN SBD planar architecture based on a *p*-GaN cap layer to achieve excellent off-state performance with a very low off-state leakage current. By properly designing the AlGaN barrier and *p*-GaN cap, the voltage drop over the Schottky junction is effectively limited while the carrier density in the access region can be increased, thus leading to a low sheet resistance. This results in good on-state performance combined with a very low leakage current ~1 nA/mm at 400V, which is maintained well below 100 nA/mm up to elevated temperatures of 150 C. Most importantly, the proposed architecture relies on the well-established fabrication process of commercial *p*-GaN HEMTs and thus represents a promising and viable solution for future GaN diodes.

4.2 Switching Performance of GaN Tri-Anode SBDs

While a reduced off-state leakage and a low diode forward voltage are features of great importance to reduce the device DC power dissipation both in on- and off-state, this is not the only loss contribution that should be taken into account when assessing the diode performance. In particular, every time the device is commutated from the on- to the off-state an additional switching loss contribution should be considered. Depending on the circuit operating frequency, switching losses can become comparable or even dominant compared to conduction ones. This is particularly true for GaN power circuits, which operate at much higher frequencies than conventional Si power devices. In this section, we investigate the switching performance of Tri-anode SBDs and compare it to conventional diodes based on a planar architecture[1].

4.2.1 Fabrication and DC Performance

In order to assess the Tri-anode switching behavior, scaled-up devices were fabricated based on a multi-finger approach (Figure 4.2.1 (a)). This is important since the characterization of small test devices is heavily influenced by the presence of parasitics in the measurement system. In addition, techniques such as a double pulse tester would be impossible to be implemented on small current devices.

The devices were fabricated on a GaN-on-Si heterostructure consisting of 4.2 µm of buffer, 420 nm of unintentionally doped GaN (u-GaN) channel, 20 nm of $Al_{0.25}Ga_{0.75}N$ barrier, and 2.9 nm of u-GaN cap-layer. The epi-structure presented electron concentration and mobility of the two-dimensional electron gas (2DEG) from Hall measurements at room temperature of 1.25×10^{13} cm^{-2} and 1700 cm^2/Vs,

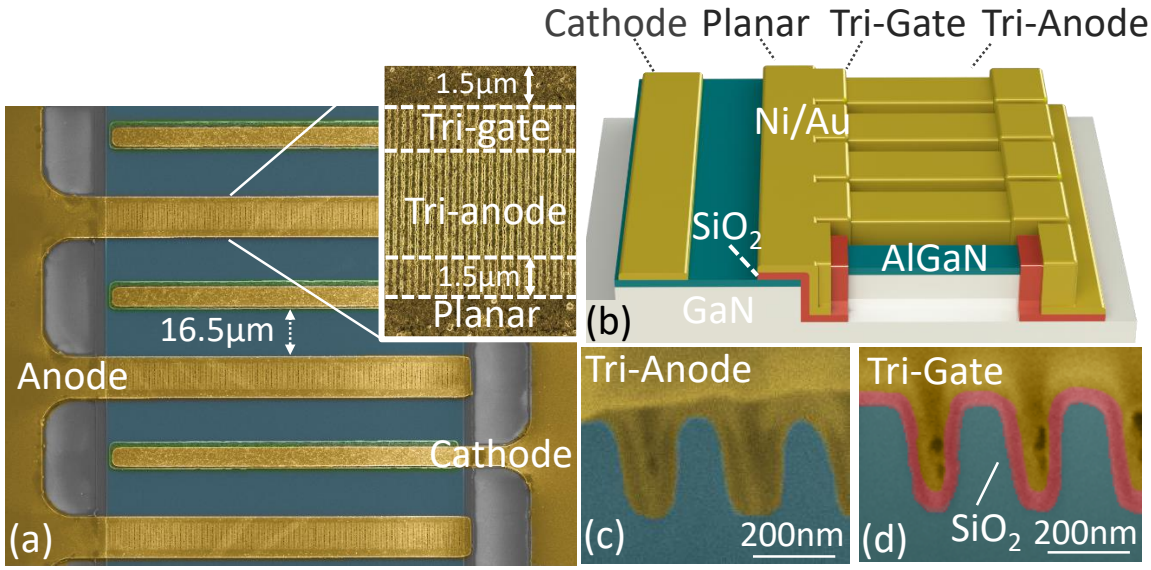


Figure 4.2.1: (a) SEM image of the scaled-up SBD fingers. The right-hand inset zooms on the anode finger, highlighting the Tri-Anode, the Tri-Gate, and the planar region. The Tri-Gate and the Planar length is 1.5 µm. For the planar device, no nanowire is etched and the planar MOS region is 3 µm-long (b) Device schematics (c-d) Focused Ion Beam (FIB) cross-section of the Tri-Anode and the Tri-Gate structure for 100 nm-wide nanowires with 100 nm spacing.

[1] This section is based on **L. Nela,** G. Kampitsis, J. Ma, and E. Matioli, "Fast-Switching Tri-Anode Schottky Barrier Diodes for Monolithically Integrated GaN-on-Si Power Circuits", *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 99–102, 2020. © 2020 IEEE. **Contribution: First Author**

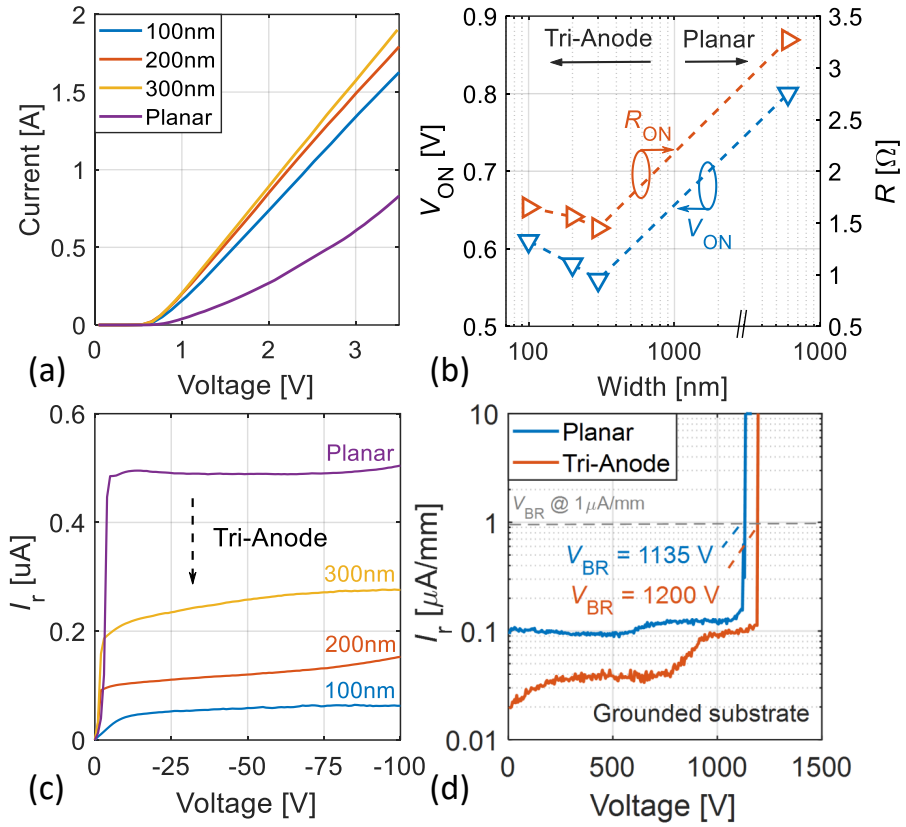


Figure 4.2.2: (a) SBD I-V curve for a planar device and Tri-Anode diodes with different widths. (b) Turn-on voltage (V_{ON}) and on-resistance (R_{ON}) for planar and Tri-anode devices with different widths. (c) Diode reverse leakage current (d) Breakdown voltage for a planar and Tri-anode SBD (w_{NW} = 200 nm). V_{BR} has been defined at 1 μA/mm with a grounded substrate.

respectively. The fabrication process started with a 200 nm LPCVD Si_3N_4 deposition to passivate the device surface. The passivation layer was then patterned using wet etching (HF 50%). The mesa and nanowires in the anode region were defined by ZEP electron-beam resist and then etched by Cl_2-based inductively coupled plasma etching (ICP) to a depth of 200 nm. The cathode ohmic contact was formed by lift-off of a metal stack of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/Ni (60 nm)/Au (50 nm), which was annealed at 780 °C for 30 s. A 20 nm-thick SiO_2 layer was conformally deposited by ALD and then removed in the Schottky anode region by wet etching. Lastly, the anode contact was formed by Ni (50 nm)/Au (100 nm), followed by the deposition of thick metal pads for the interconnections.

The width of the nanowires in the anode region was varied from 100 nm to 300 nm (W100, W200, and W300), while the spacing between the nanowires was fixed to 100 nm. The cathode to anode distance was set to 16.5 μm and 50 alternating anode-cathode fingers were integrated for a total device active width of 9.9 mm. Conventional diodes based on a planar architecture were co-fabricated on the same chip and used as reference devices. To ensure a fair comparison, the same total field plate length of 3 μm was designed for both the Tri-anode and the planar devices, with the only difference between the two structures consisting of the 1.5 μm-long Tri-gate region and Tri-anode contact (Figure 4.2.1).

The Tri-anode architecture leads to a significant improvement of the diode DC performance with respect to the planar reference, as shown in Figure 4.2.2. On the one hand, the diode turn-on voltage is reduced thanks to the 2DEG Schottky side contact (Figure 4.2.2 (a-b)) while, on the other hand, the reverse leakage current decreases thanks to the electric field shielding by the Tri-gate field plate (Figure

4.2.2 (c)). This results in high-performing devices with low forward voltage (V_F) and high breakdown voltage V_{BR} of 1200 V (Figure 4.2.2 (d)).

4.2.2 Switching Characterization

To understand the switching behavior of Tri-anode SBDs, their off-state *C-V* curve was measured by a Keysight B1505 analyzer. The device capacitance was extracted through a small signal excitation with a frequency of 1 MHz and amplitude of 100 mV. Figure 4.2.3 (a) shows a comparison of the off-state diode capacitance as a function of the reverse voltage (V_R) for Tri-anode devices having different widths and the planar reference. Three different regions can be identified: for V_R < -5 V the capacitance is small the field plate structure has already been depleted and the device capacitance is dominated by the buffer and access regions contribution. For V_R > -5 V, the field plate region turns on, leading to a first step in the capacitance curve, followed by a second step corresponding to the Schottky region contribution. While this sequence is consistent for all the architectures considered, the capacitance value and the position of the steps strongly depend on the device design. All devices share a planar field plate region, which is responsible for the first capacitance step at V_R = 5 V. For planar devices, this is followed by a second step, corresponding to the planar Schottky contact. For Tri-anode devices, instead, a second step corresponding to the Tri-gate region appears, which merges with a third step resulting from the Schottky Tri-anode contribution. It is possible to notice that the position of such capacitance steps is not fixed and depends on the nanowire width (w_{NW}). In particular, as w_{NW} is reduced, the Tri-gate and Tri-anode turn-on shift closer to 0 V. This is a direct consequence of the nanowires threshold voltage dependence on the width, as explained in detail in *Chapter 2*, and it is the very reason for the decrease leakage current in Tri-anode devices (Figure 4.2.2 (c)). Apart from being beneficial for the diode blocking performance, the introduction of a nanostructure anode region results in a decrease in the device's capacitance. While this may seem counterintuitive because of the 3D structure of the anode electrode, it can be explained considering the distinction between the single nanowire and the entire device footprint. The capacitance for each nanowire indeed increases due to the 3D metal contact around the

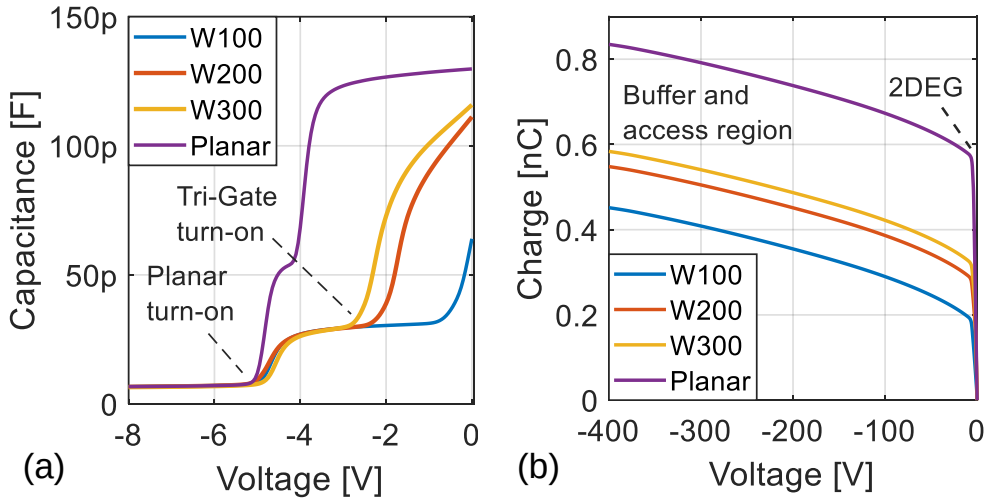


Figure 4.2.3: (a) Capacitance versus reverse voltage (V_R) curve for Tri-anode and Planar diodes. (b) SBD reverse charge obtained by integrating the capacitance curve for $V_R \in$ [-400 ; 0] V.

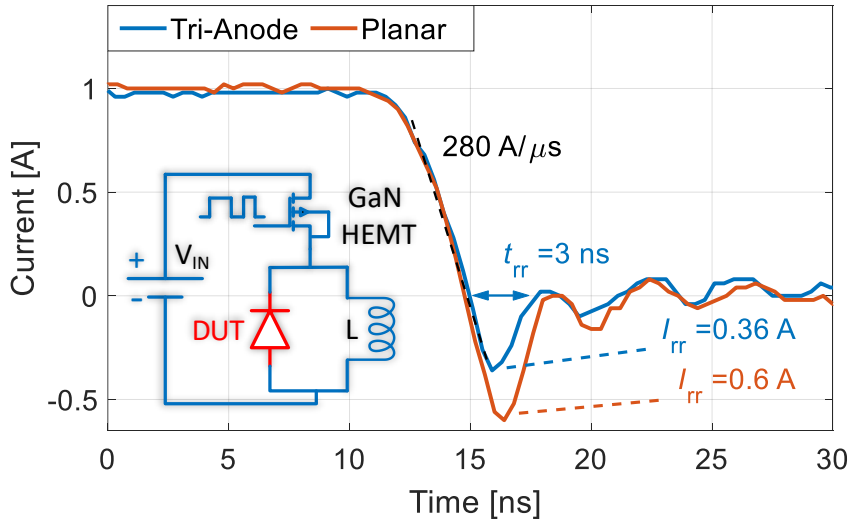


Figure 4.2.4: Reverse recovery measurement for a planar GaN SBD and a Tri-anode SBD with w_{NW} of 200 nm. The *di/dt* was set to 280 A/μs and the reverse voltage to -100 V. The double pulse circuit used in the experiment is shown on the bottom left.

nanowire, which results in improved control. However, the overall device capacitance decreases due to the partial 2DEG removal in the trench region and to the diminished charge in the nanowire as a consequence of sidewalls depletion and strain relaxation. This behavior results in a decrease in the capacitive charge for the Tri-anode devices with respect to the planar reference, which further reduces as the nanowire width decreases (Figure 4.2.3 (b)).

To confirm these results, a diode reverse recovery measurement was performed through the use of a double-pulse tester circuit (DPT) [186]–[188] (Figure 4.2.4). Such a technique allows observing the effect of the total on and off-state device charge when the diode is suddenly switched off with a high *di/dt*. A first pulse charges the inductor to the desired current, which is then forced through the diode during the dead time. A second pulse then causes the SBD's abrupt transition to the off-state, allowing the measurement of the recovery time and charge. The diode forward current (I_F) was set to 1 A, the reverse voltage to -100 V, and the *di/dt* to 280 A/μs, determined by the gate resistor of the top-side transistor.

Figure 4.2.4 shows a decrease in the diode reverse recovery for the Tri-anode SBD (w_{NW} = 200 nm) with respect to the planar reference, resulting in a 50% decrease in the reverse recovery charge (Q_{rr}).

	Planar	W300	W200	W100
t_{rr} [ns]	4	3.5	3	3
I_{rr} [A]	0.5	0.44	0.3	0.25
Q_{rr} [nC]	1.02	0.9	0.5	0.3
$R_{ON}\cdot Q_{rr}$ [nC·Ω]	3.5	1.3	0.62	0.49

Table 4.2.1: t_{rr}, I_{rr}, Q_{rr}, and $R_{ON}\cdot Q_{rr}$ comparison for planar and Tri-anode diodes with different nanowire widths. The forward current (I_F) was set to 1 A and the reverse voltage (V_{rr}) to -50 V.

While the Q_{rr} can be significantly reduced by tuning w_{NW}, the device on-resistance (R_{ON}) is only slightly affected by the nanowire widths considered in this study (Figure 4.2.1 (b)). This is an important result as it leads to a considerable $R_{ON} \cdot Q_{rr}$ figure-of-merit reduction for the Tri-Anode architecture, which can be tuned by adjusting the Tri-anode width (Table 4.2.1).

In this section, we performed a thorough investigation of the switching performance of GaN Tri-anode SBDs. The presented results demonstrate that the Tri-anode architecture is not only highly beneficial for the diode DC performance, but can also significantly improve its switching behavior. In particular, a considerable reduction in the $R_{ON} \cdot Q_{rr}$ figure-of-merit was demonstrated for Tri-anode SBDs with respect to conventional planar devices, which shows their great potential for fast-switching power applications.

4.3 High-Frequency Power ICs based on Tri-Anode GaN SBDs

In the previous section (*Section 4.2*), we have demonstrated the potential of Tri-anode SBDs to reduce the $R_{ON} \cdot Q_{rr}$ figure-of-merit compared to conventional GaN diodes architectures and thus to efficiently operate at high switching frequencies. In this section, we benchmark the performance of the proposed devices with state-of-the-art commercial SBDs based on Si and SiC. In addition, we demonstrate the potential of GaN Tri-anode devices to realize ultra-compact power integrated circuits able to efficiently operate in the MHz regime. Finally, we compare the same DC-DC boost converter realized with the proposed GaN Tri-anode SBDs, and with Si and SiC commercial devices, showing a significant improvement in high-frequency operation along with a large size reduction.[1]

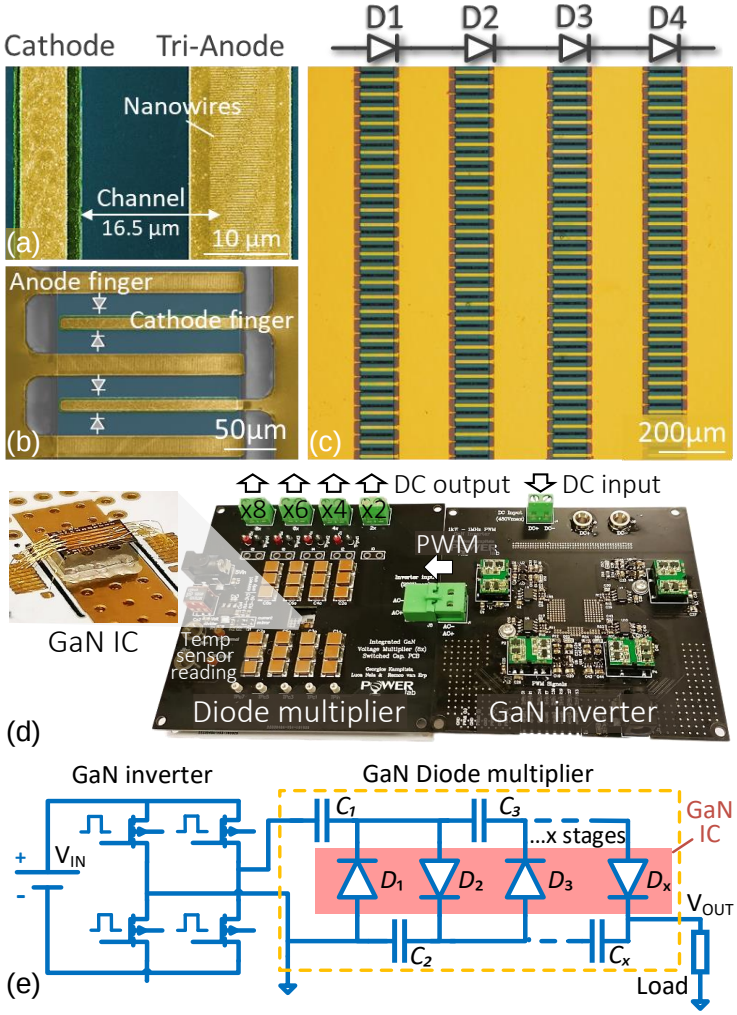


Figure 4.3.1: (a) SEM image of the Tri-Anode SBD channel region and (b) of the multi-finger scaled-up device. (c) Optical microscope image of the 4-stage diode multiplier IC. (d) PCB testing setup for the diode multiplier IC which includes an inverter to generate the PWM signal and the capacitors for the voltage boosting. In the left-hand inset, a picture of the wire-bonded chip is shown. (e) Circuit schematics of the DC-DC magnetic-less boost converter. The capacitance value of the multilayer capacitors C_1, C_2, C_3 has been set to 6.6 µF from the simulation of the circuit.

[1] This section is based on **L. Nela,** R. Van Erp, G. Kampitsis, H. K. Yildirim, J. Ma, and E. Matioli, "Ultra-compact, high-frequency power integrated circuits based on GaN-on-Si Schottky Barrier Diodes", *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1269–1273, 2020. © 2020 IEEE. **Contribution: First Author.**

The GaN Tri-anode diodes and the monolithically integrated ICs were fabricated on a 6'' GaN-on-Si heterostructure consisting of 4.2 µm of buffer, 420 nm of unintentionally-doped GaN (u-GaN) channel, 20 nm of $Al_{0.25}Ga_{0.75}N$ barrier, and 2.9 nm of u-GaN cap-layer. The fabrication steps are the same as the ones reported in *Section 4.2*. Scaled-up devices were achieved by a multi-finger approach, paralleling 50 fingers for a total device width of 9.9 mm. The diode multiplier IC was realized by properly interconnecting 4 to 8 diodes on the same chip (Figure 4.3.1 (a-c)). The GaN IC was combined with a GaN inverter circuit to realize a DC-DC boost converter (Figure 4.3.1 (d)). The input DC signal is converted into a PWM by the full-bridge inverter and then amplified and rectified by the diode multiplier IC and output capacitors. The voltage amplification depends on the number of stages (in this case x4, x6, and x8 outputs are available). An integrated on-chip temperature sensor was included, whose value is read through a current mirror circuit. The complete circuit schematic is presented in Figure 4.3.1 (e).

4.3.1GaN Tri-Anode SBD Comparison with State-of-the-Art Si and SiC

The individual Tri-anode GaN SBD I-V shows forward voltage (V_F) of 2.2 V at a current I_F of 1 A, and ON/OFF ratio higher than 10^7 at a reverse voltage V_R of -400 V (Figure 4.3.2 (a)). Such good DC performance is in agreement with the result in *Section 4.2* and our previous works on the subject [58], [59]. To characterize the SBD switching performance and compare the losses associated with its turn-off, a double-pulse-tester (DPT) measurement was performed (see *Section 4.2*). Figure 4.3.2 (b) shows

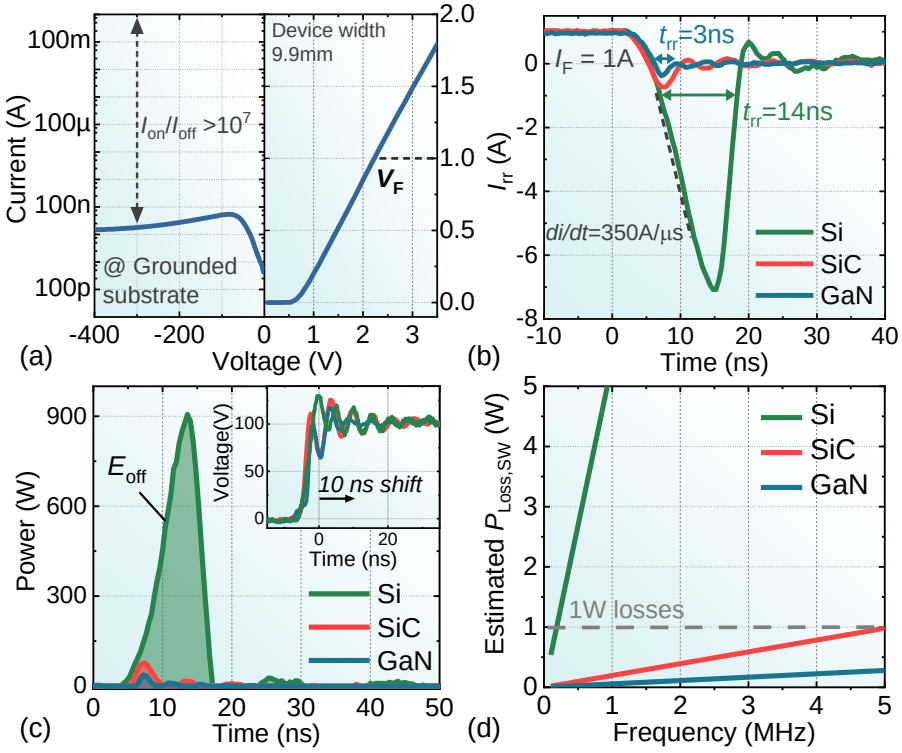


Figure 4.3.2: (a) I-V curve for the Tri-Anode devices. (b) Reverse-recovery measurement comparing GaN Tri-Anode SBDs, Si FRDs, and SiC diodes. The reverse voltage was set to -100 V, the *di/dt* to 350 A/µs, and the forward current in the on-state to 1 A. (c) Instantaneous power loss at the diode turn-off and corresponding dissipated energy E_{off}. The current and voltage-probe synchronization was achieved by applying a 10 ns correction (inset). (d) Estimated diode switching losses as a function of frequency obtained from the device E_{off}.

the Tri-anode SBD reverse-recovery behavior, which is compared to a commercial Si fast-recovery diode (FRD) [189] and SiC SBD [190] with a similar rating. The Tri-anode GaN SBD significantly outperforms the Si device in terms of reverse-recovery time (t_{rr}), current (I_{rr}), and overall charge (Q_{rr}), and compares well to the SiC device. Such improvement comes from the superior AlGaN/GaN material properties for power applications, such as high electron mobility and large critical electric field (Table 1.2.1), combined with the excellent Tri-anode architecture [60]. The total reverse-recovery charge for the three devices, obtained from the time-integration of I_{rr}, is reported in Table 4.3.1, which also shows a significant improvement in the $Q_{rr} \cdot V_F$ figure-of-merit for the GaN Tri-anode devices.

To extract the losses associated with each diode turn-off event, the voltage over the diode during the reverse-recovery measurement was recorded and multiplied point-by-point by I_{rr} to obtain the instantaneous power loss. Calibration of the voltage and current probes over a resistive load was performed to ensure a synchronous measurement. Figure 4.3.2 (c) shows a comparison of the instantaneous diode power loss at each turn-off, highlighting a large peak for the Si FRD and a much-reduced value for the SiC and GaN SBDs. By time-integrating the power peak of Figure 4.3.2 (c) it is possible to extract the switching energy loss (E_{off}) at each cycle (Table 4.3.1) and thus estimate the switching losses for the three devices at different frequencies. From Figure 4.3.2 (d), it is clear that the Si FRD cannot operate above a few hundreds of kHz without significant switching losses, while the SiC and GaN SBD represent a suitable solution for the MHz range.

	Si FRD	SiC SBD	GaN Tri-anode
Q_{rr} [nC]	51	2.1	0.6
E_{off} [µJ]	5.4	0.2	0.056
$V_F \cdot Q_{rr}$ [V·nC]	127.5	3.36	1.4

Table 4.3.1: Comparison of Q_{rr}, E_{off} and $V_F \cdot Q_{rr}$ extracted from Figure 4.3.2 for the GaN Tri-anode devices and the reference Si FRD and SiC SBD. The forward voltage V_F has been defined at a current of 1 A.

4.3.2 Monolithic Integration and Power IC Converter

The promising performance from the single diode characterization was applied to a real circuit application, as a diode multiplier, able to perform DC-DC boost conversion. To this end, four to eight of the presented Tri-anode GaN diodes were monolithically integrated on the same chip to realize the desired IC, which was tested using the setup shown in Figure 4.3.1 (d). Figure 4.3.3 (a) demonstrates the operation of the 4-diode circuit that is able to boost and rectify the input PWM signal generated by the inverter into a DC output (V_{OUT}). The circuit operating frequency is 1 MHz. An important advantage of the diode multiplier topology is its modularity that allows to easily enhance the V_{OUT} multiplication factor by increasing the number of stages. Each stage is composed of two diodes and two capacitors (Figure 4.3.1 (e)). Figure 4.3.3 (b) reports the output voltage for a diode multiplier with 4, 6, and 8 stages at the same V_{IN}, successfully showing an increase in the boosting ratio. Figure 4.3.3 (c) shows V_{OUT} as a function of V_{IN} for a four-diode multiplier (left) and as a function of the number of stages for the same input voltage (right). The multiplication factor for the four-diode multiplier is 3.82, slightly

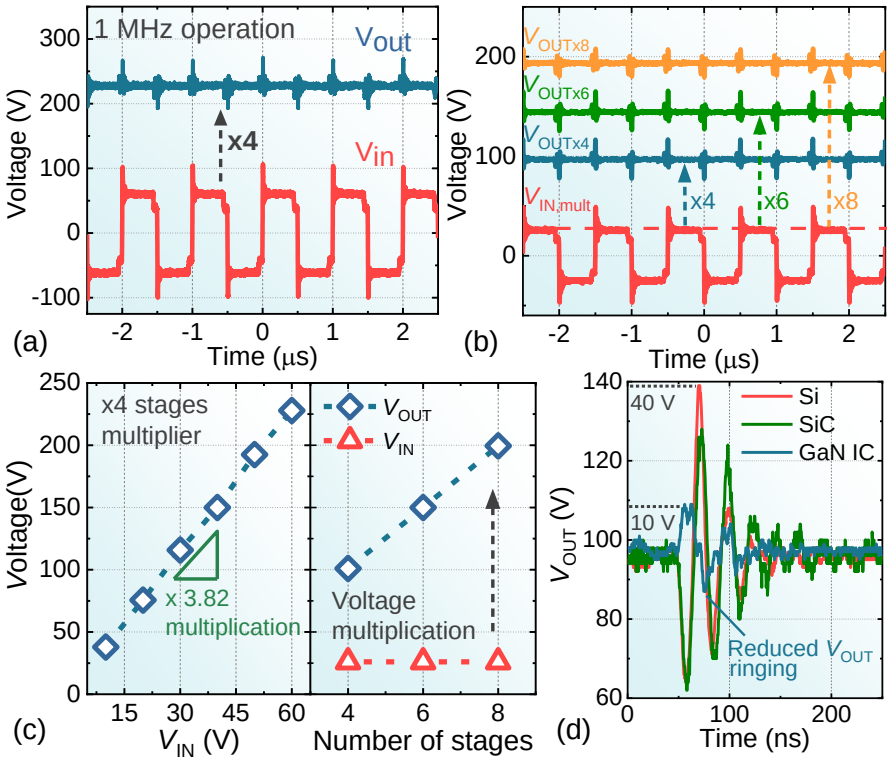


Figure 4.3.3: (a) Operation of the 4-stage diode multiplier IC for input signal frequency of 1 MHz. (b) Output voltage for the same V_{IN} for a 4, 6, and 8 stages diode multiplier (c) V_{OUT} as a function of V_{IN} for a 4-stage diode multiplier (left) and as a function of the number of stages for the same V_{IN} (right). (d) V_{OUT} ringing comparison for a diode multiplier realized with the presented GaN IC and by discrete Si and SiC reference devices.

lower than the theoretical value of 4 due to the losses over the 4 diodes. The shorter interconnections and lower parasitics contribution from the GaN IC result in an important decrease of the output voltage ringing and overshoot with respect to the reference circuit realized with Si or SiC discrete devices (Figure 4.3.3 (d)). It should be noted that the 1 MHz operating frequency was chosen to comply with the capacitors and inverter specifications and was not limited by the GaN IC, which could operate at higher frequencies.

While power ICs can significantly enhance the power density, careful thermal management solutions and temperature monitoring are of extreme importance to deal with such high heat fluxes. A continuous, near-junction temperature tracking is important to avoid device over-heating, increase its reliability and monitor its losses. To this end, an on-chip sensing resistor [191] was designed in close proximity to the GaN IC to control its temperature during operation. By monitoring the IC temperature with a thermal camera (Figure 4.3.4 (a)) and simultaneously measuring the resistor value, the temperature sensor was calibrated resulting in a sensitivity of 1.05 K/Ω (Figure 4.3.4 (b)). In addition, by connecting the diodes in series and dissipating a known DC power over the IC, the sensor resistance was linked to the IC dissipated power, to extract the device's thermal resistance. This enables, after proper calibration, continuous monitoring of the IC losses during its operation with a simple electrical measurement.

The diode multiplier GaN ICs was compared to the same circuit realized by Si and SiC discrete devices. Thanks to its lateral architecture, AlGaN/GaN devices can be easily integrated on the same chip to realize power ICs. However, this is not the case for Si and SiC devices whose vertical device architecture requires the use of discrete components, or sophisticated and expensive back-end

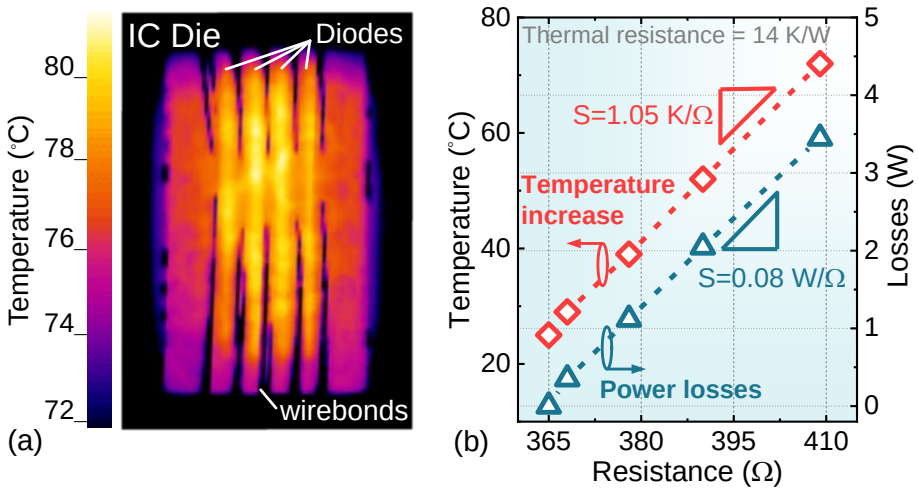


Figure 4.3.4: (a) Thermal image of the 4-diode multiplier IC during operation obtained using a FLIR SC3000 IR camera. A uniform emissivity was obtained by coating the device surface with black paint. (b) Integrated sensor calibration with the IC temperature and the IC dissipated power showing good linearity and a sensitivity of S_{th} = 1.05 K/Ω and S_P=0.08W/Ω, respectively.

techniques to co-package multiple devices together. This results in a drastic size reduction and power density increase for GaN ICs, in which 6 power diodes could be integrated into a chip size of 2.3 mm x 3.6 mm, leading to a more than 10 times reduction in footprint with respect to similarly-rated surface-mounted Si and SiC discrete diodes (Figure 4.3.5 (a)). In addition, the reduction of the interconnection parasitics thanks to the ICs' monolithic integration enables high-frequency operation with minimum ringing and overshoot voltage, as seen in Figure 4.3.3 (d).

Figure 4.3.5 (b) shows the losses as a function of the operating frequency for 4-stage diode multipliers realized with discrete Si FRDs, SiC SBDs, and the GaN ICs at the same output power. The losses for all devices were extracted from thermal measurement by IR camera. While the different diodes were chosen to have similar V_F and current ratings, and thus show comparable conduction losses, the total loss contribution as a function of the frequency strongly depends on the device technology. In particular, the diode multiplier realized with Si diodes shows a rapid loss increase as the frequency is raised. Such a trend is due to the Si FRD large reverse-recovery charge, which results in a substantial energy loss at each turn-off event (Figure 4.3.2 (c)). This leads to significant switching losses, which completely dominate over conduction losses, and rapidly increase until the circuit fails due to thermal runaway. The GaN IC diode multiplier and the one realized with SiC discrete devices show instead only a moderate loss increase from an operating frequency of 100 kHz to 1 MHz, benefiting from the much-reduced diode E_{off} with respect to the Si devices (Figure 4.3.2 (c)). In this case, conduction losses, which are constant in frequency, represent the main contribution. The behavior of the different diode multiplier circuits agrees well with the single-diode switching performance characterization shown in Figure 4.3.2. Thanks to the reduced switching losses, the GaN IC is able to properly operate in the MHz range with a minimum loss increase. Such high operating frequency, combined with the reduced ringing from the IC design, is very promising for switching-capacitor architectures since it allows reducing the overall capacitor value and size and significantly increasing the converter output power.

In this section, we presented the promising potential of Tri-anode GaN-on-Si SBDs for future high-frequency power applications. The results from the Tri-anode lateral diodes significantly outperform Si FRD and are comparable with SiC SBDs. In addition, Tri-anode devices can be monolithically integrated to realize power ICs able to operate at high frequency, thanks to the reduced diode switching

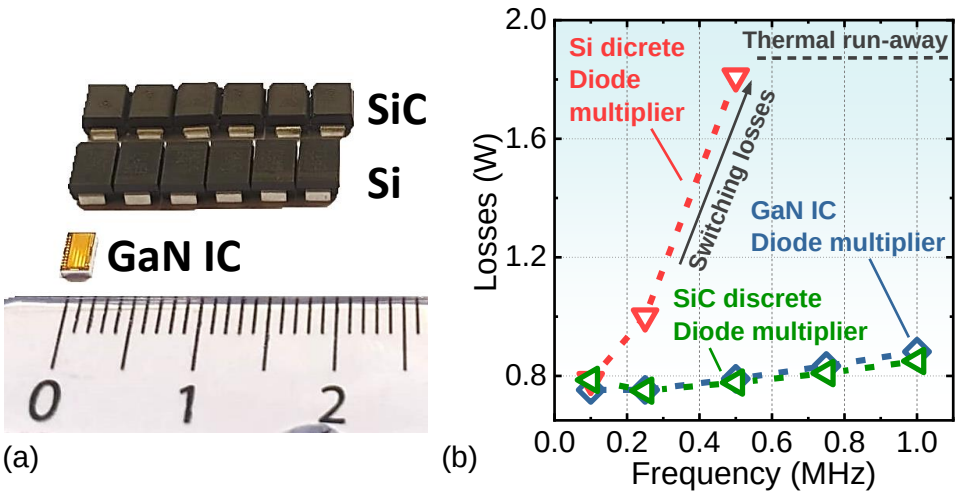


Figure 4.3.5: (a) Size comparison for the Tri-Anode GaN-on-Si 6-stage diode multiplier ICs with respect to the same circuit realized with discrete vertical surface mounted Si and SiC devices. (b) Losses as a function of frequency for the GaN IC and the reference circuits made of Si and SiC discrete devices. The losses were evaluated at a constant output power by thermal measurement.

losses and low interconnection parasitics. This is demonstrated by realizing a diode multiplier IC that includes up to 8 diodes on the same chip and is able to operate as a DC-DC magnetic-less boost converter with x8 multiplication factor at a frequency of 1 MHz, which cannot be matched by Si FRD devices. In addition, the monolithic device integration enables a significant reduction of the device footprint, which is more than 10 times smaller than for Si and SiC discrete devices, paving the way to compact and cost-effective solutions. Lastly, the IC platform enables the integration of an on-chip sensor for electrical, real-time monitoring of the circuit temperature and losses. These results demonstrate the promising potential of Tri-anode GaN-on-Si SBDs for future compact, fast-switching, and cost-effective power ICs.

4.4 *p*-GaN Field Plate for Low-leakage Current in Lateral GaN Schottky Barrier Diodes

One of the main challenges for GaN SBDs is represented by the difficult management of the off-state electric field at the fragile Schottky barrier, which, if not properly managed, results in large leakage current and poor breakdown voltage. Besides, the blocking performance of GaN SBDs further degrades at elevated temperatures, which is, however, the typical operation condition of wide band-gap power devices. The key to reducing the high off-state leakage is to limit the maximum voltage drop on the Schottky barrier by engineering field plate (FP) structures with a pinch-off voltage (V_P) close to 0 V aimed at protecting the junction [59], [63]. This is, however, challenging as conventional field plate structures with no oxide already present a rather large negative V_P ~ - (4-5) V, which results in large off-state leakage for the SBD.

Alternative strategies proposed in the literature include the use of a Tri-anode architecture [57]–[60], as seen in *Sections 4.2* and *4.3*, or the partial recess of the AlGaN barrier [62], [63] to achieve FPs with V_P ~ -2V. Nevertheless, while these approaches have been demonstrated to be effective in reducing the off-state leakage and have achieved excellent device performance, they require dedicated device processing that is not widely available at the time being. In particular, Tri-anode devices need lithographic resolution ~ 200 nm [57]–[60], which is not yet available in GaN power devices' process lines. SBDs relying on a partially recessed barrier require instead extremely precise control of the etching depth, which can be obtained only by complex methods such as atomic layer etching [62], [63].

Here, we propose a simple AlGaN/GaN SBD architecture based on a *p*-GaN cap layer to achieve excellent off-state performance with a very low off-state leakage current.[1] While approaches based on a *p*-GaN edge termination have been investigated, previous works were aimed at very different architectures, such as SBDs with multiple channels [111], [192] or with a RESURF (Reduced Surface Field [193]) layer [145]. The role of the *p*-GaN field plate in these structures was not to reduce the off-state leakage but rather to improve the electric field distribution in the drift region, similarly to conventional field plates. For these reasons, the design and physical mechanisms behind the operation of the *p*-GaN field plate differed significantly from the one here presented, which is instead specifically aimed at reducing the off-state leakage. In addition, the design and operation of the proposed *p*-GaN field plate are different also compared to conventional enhancement-mode (E-mode) *p*-GaN HEMTs for which the pinch-off voltage should be as positive as possible. In particular, to achieve a low leakage current, the *p*-GaN field plate should be designed to present a slightly negative V_P. Indeed, a too negative V_p would result in similar behavior as for conventional FPs [111], which are not effective in properly protecting the Schottky junction and result in a large off-state leakage. On the contrary, a positive pinch-off voltage in the *p*-GaN region, as in *p*-GaN E-mode HEMTs would lead to a degradation of the SBD turn-on voltage.

In this section, we show that by properly tuning the AlGaN barrier and *p*-GaN cap, a *p*–GaN field plate with V_p close to 0 V is achieved, which effectively limits the voltage drop over the Schottky junction. Besides, tuning the AlGaN barrier also enables to increase the carrier density in the access

[1] This section is based on **L. Nela,** C. Erine, and E. Matioli, "*p*-GaN field plate for low leakage current in lateral GaN Schottky Barrier Diodes", *Applied Physics Letters*, 119, 263508, 2021. **Contribution: First Author.**

region compared to usual *p*-GaN based devices, thus leading to a low sheet resistance. This results in good on-state performance combined with a very low leakage current ~1 nA/mm at 400V, which is maintained well below 100 nA/mm up to elevated temperatures of 150 °C. In addition, this architecture shares the well-established fabrication process of commercial *p*-GaN HEMTs and can benefit from the extensive research on these devices, which could significantly accelerate its development.

4.4.1 Device Design and Fabrication

The devices were fabricated on a GaN-on-Si heterostructure comprising a 5.2 µm of buffer, 420 nm of unintentionally doped GaN (u-GaN) channel, 0.7 nm of AlN spacer, 20 nm of $Al_{0.25}Ga_{0.75}N$ barrier, and 75 nm of *p*-GaN cap-layer with a Mg concentration of 3×10^{19} cm^{-3}. The device fabrication started with the removal of the *p*-GaN cap layer from the access and contact region by a low-damage, slow-etch-rate Cl_2/Ar-based inductively coupled plasma (ICP) etching. The device mesa was defined by ICP etching to a depth of 250 nm. The cathode was formed by a stack of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/Ni (60 nm)/Au (50 nm) and annealed at 780 °C for 30 s, followed by the deposition of a 25 nm-thick SiO_2 layer by atomic layer deposition (ALD). The oxide was patterned by wet etching and a Ni/Au (50 nm / 120 nm) metal stack was evaporated to serve as anode contact

Figure 4.4.1 shows the cross-sectional schematic and the scanning electron microscope (SEM) top-view of the proposed device. The device anode-to-cathode distance (L_{AC}) is 14 µm, measured from the cathode edge to the end of the *p*-GaN FP (Figure 4.4.1 (b)), while the device width is 60 µm. All quantities reported in the manuscript have been normalized by the total device width (60 µm). Reference devices with fully removed *p*-GaN cap layer and Tri-anode structures were co-fabricated on the same chip.

4.4.2 Leakage Control Mechanism and Device Performance

To reduce the voltage drop on the Schottky barrier during the off-state, the heterostructure should be properly designed. To this end, the V_P of the *p*-GaN field plate that protects the Schottky junction (Figure 4.4.1 (a)) should be adjusted to be slightly negative. Indeed, too positive V_P would result in a degraded diode turn-on voltage while too negative values would lead to a large leakage current, as

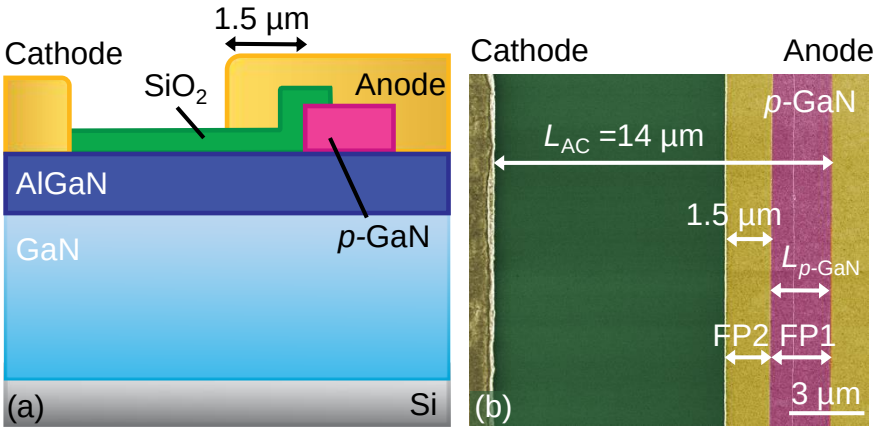


Figure 4.4.1: (a) Schematics and (b) top SEM view of the proposed AlGaN/GaN SBD with *p*-GaN cap field plate in the anode region.

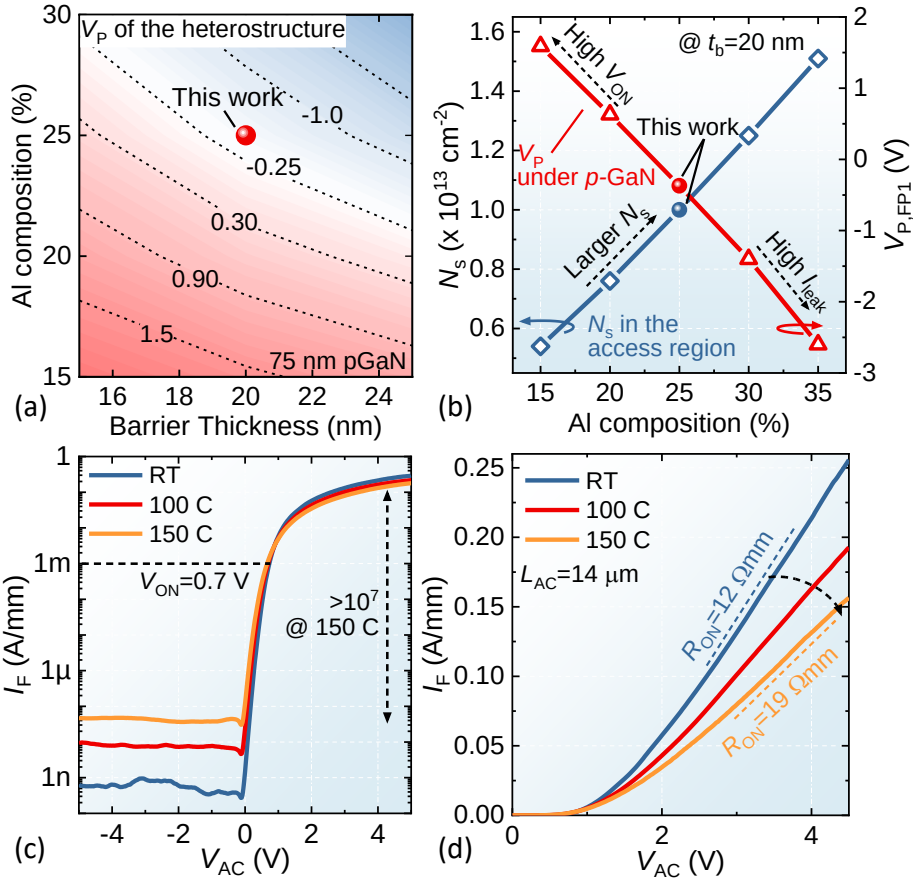


Figure 4.4.2: (a) Simulated V_P of a heterostructure with a 75 nm-thick *p*-GaN layer as a function of the AlGaN barrier thickness and Al composition. (b) Simulated N_s in the access region (with no *p*-GaN) and V_P under the *p*-GaN cap for a 20 nm-thick AlGaN barrier as a function of its Al composition. (c) I-V curves for the proposed *p*-GaN SBD in logarithmic (c) and linear (d) scale at different temperatures.

shown in the following sections. While varying the thickness and doping of the *p*-GaN layer does not impact significantly the V_P of the *p*-GaN field plate, tuning the AlGaN barrier is an effective approach to set the V_P. Figure 4.4.2 (a) illustrates the simulated V_P of a heterostructure with a 75 nm-thick *p*-GaN cap layer as a function of the AlGaN barrier thickness and composition. The simulation was performed by employing Atlas Silvaco software. The 20 nm-thick $Al_{0.25}Ga_{0.75}N$ barrier employed in this work results in a V_P ~ -0.4 V, which satisfies the requirements aforementioned. Besides, the use of a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier leads to a large two-dimensional electron gas (2DEG) concentration (N_s) in the access region (where the *p*-GaN cap is removed) (Figure 4.4.2 (b)). This results in a low sheet resistance (R_{sh}) in the drift region, reducing the device on-resistance. Finally, while the proposed structure differs from the typical *p*-GaN heterostructures used for E-mode transistors, it was shown that E-mode devices can be realized on this platform by employing a Tri-gate architecture [194], hence enabling the integration of E-mode HEMTs and SBDs on the same chip.

Figure 4.4.2 (c-d) presents the I-V curve for the proposed devices. The SBD shows a turn-on voltage (V_{ON}) of 0.7 V at 1 mA/mm (Figure 4.4.2 (c)), which is a typical value for Ni/Au anode contact [58], [181] and confirm no degradation in the diode turn-on due to the *p*-GaN layer. Besides, thanks to the effective *p*-GaN field plate, an excellent I_{ON}/I_{OFF} above 10^9 at room temperature (RT) is obtained, whose value is maintained above 10^7 even at 150 °C. The large N_s in the access region also results in a low R_{ON} of 12 Ω·mm for a L_{AC} of 14 µm (Figure 4.4.2 (d)), which increases to 19 Ω·mm at 150 °C, showing the

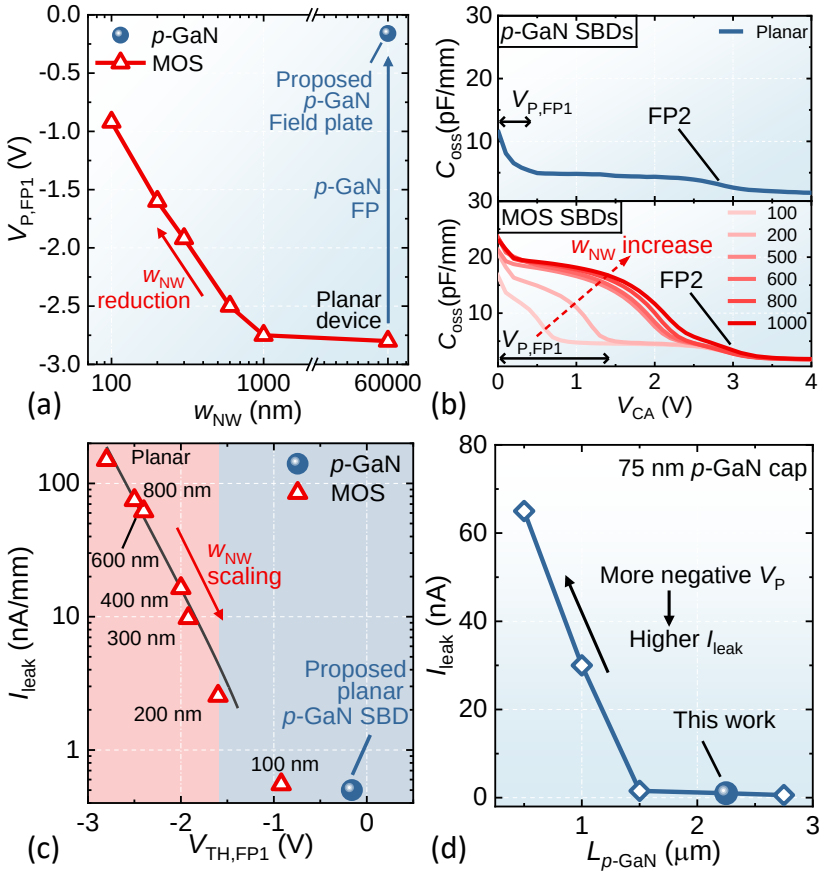


Figure 4.4.3: (a) $V_{P,FP1}$ as a function of the nanowire width for *p*-GaN and MOS devices. (b) Output capacitance for *p*-GaN and MOS SBDs Tri-anode devices having different nanowire width (c) SBD leakage current (extracted at 20 V) as a function of the $V_{P,FP1}$. (d) Off-state current as a function of the *p*-GaN FP length ($L_{p\text{-GaN}}$).

device's potential to operate at high temperatures. It should be noted that the majority of the on-state current goes through the AlGaN/anode metal interface (Figure 4.4.1 (a)) rather than through the *p*-GaN layer, which was verified both by TCAD simulations and experimentally. Indeed, the presence of an anode region in direct contact with the AlGaN barrier is fundamental to ensure low V_{ON} and R_{ON}, which would be degraded by the conduction through the *p*-GaN layer.

To investigate the role of the *p*-GaN field plate in reducing the SBD off-state leakage, reference *p*-GaN Tri-anode and usual MOS Tri-anode devices [57]–[60] were considered (Figure 4.4.3 (a)). While the proposed *p*-GaN SBDs are based on a conventional planar architecture (see Figure 4.4.1), the use of a Tri-anode enables a gradual tuning of the field plate 1 (FP1 in Figure 4.4.1 (a)) pinch-off voltage ($V_{P,FP1}$). This provides a more complete understanding of the physical mechanisms involved and enables deriving a relation between $V_{P,FP1}$ and the leakage current. However, while employing a Tri-anode architecture is a convenient method to gradually shift $V_{P,FP1}$, the presented analysis is general. Indeed, it also applies to other techniques such as the use of a *p*-GaN cap layer (as here presented) or the partial recess of the barrier [62], [63]. In addition, while the device L_{AC} influences the breakdown voltage, the value of the off-state current up to a few hundred of V is mainly determined by the leakage through the Schottky barrier thus the presented analysis is general and can be applied to SBDs with different lengths.

Figure 4.4.3 (a) shows that a planar MOS field-plate presents a rather negative $V_{P,FP1}$ of -2.8 V, which reduces as the Tri-anode nanowire width (w_{NW}) decreases (Figure 4.4.3 (a), red arrow). On the contrary,

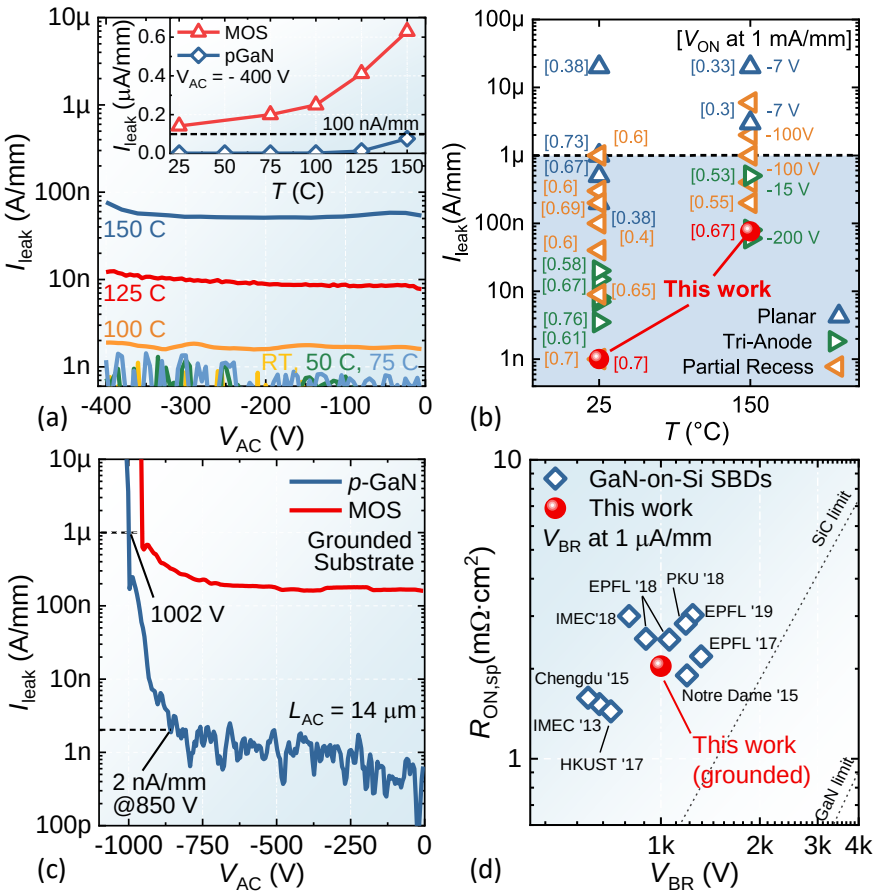


Figure 4.4.4: (a) Off-state leakage current for a *p*-GaN SBD at different temperatures. Inset: I_{leak} as a function of temperature at a reverse voltage of 400 V for a planar *p*-GaN and MOS SBD (b) I_{leak} at RT and 150 °C for state-of-the-art SBDs present in the literature [9], [46], [58]–[60], [62], [63], [110], [137], [179], [181], [195]–[198]. The corresponding diode V_{ON} is shown in brackets. The off-state voltage is 400 V unless differently specified. (c) Breakdown curve for a planar *p*-GaN and MOS SBD with L_{AC} of 14 µm and grounded substrate. (d) $R_{ON,sp}$ vs V_{BR} benchmark for the proposed *p*-GaN SBD compared to state-of-the-art GaN-on-Si lateral SBDs present in the literature [9], [46], [58]–[60], [110], [181], [196]–[198]. The breakdown has been defined at an off-state current of 1 µA/mm and a 3 µm transfer length, adding up to L_{AC}, has been considered to evaluate $R_{ON,sp}$.

the proposed *p*-GaN field plate enables achieving slightly negative (-0.25 V) $V_{P,FP1}$ even for a planar device (Figure 4.4.3 (a), blue arrow), in agreement with the simulation in Figure 4.4.2 (a-b). This behavior is confirmed by the SBD output capacitance (C_{oss}) (Figure 4.4.3 (b)), which shows a very small $V_{P,FP1}$ for *p*-GaN devices, and an instead rather large $V_{P,FP1}$ for MOS devices, with a strong dependence on w_{NW}. The role of $V_{P,FP1}$ is fundamental as its value represents the voltage drop on the Schottky barrier, which directly determines the electric field at the barrier and the SBD leakage current (I_{leak}) [59], [61], as shown in Figure 4.4.3 (c). Indeed, negative values below ~ -2 V of $V_{P,FP1}$ result in an exponential increase of the SBD leakage current due to the enhanced conduction through the Schottky barrier. On the contrary, the small $V_{P,FP1}$ of *p*-GaN SBDs results in a very low leakage <1 nA/mm even for planar devices, proving the effectiveness of the proposed approach. It should be noted that while a similar approach based on a *p*-GaN layer was proposed for field-effect rectifiers [199], [200], this typically results in a large off-state current due to the very strong dependence of I_{leak} on the exact $V_{P,FP1}$ value. In the proposed *p*-GaN SBDs, the presence of a Schottky barrier allows more tolerance on $V_{P,FP1}$ (Figure 4.4.3 (c)), enabling to achieve extremely low off-state leakage. Another important aspect to consider when designing the *p*-GaN FP is the $V_{P,FP1}$ dependence on its length. Indeed, for too short FP lengths ($L_{p\text{-GaN}}$), the field plate pinch-off voltage reduces, as shown in Ref. [194], which results in an increase

of the leakage current (Figure 4.4.3 (d)). On the contrary, $L_{p\text{-GaN}}$ values above 1.5 µm ensure $V_{P,FP1}$ close to 0 V and a considerable reduction of the off-state leakage.

Thanks to the small voltage drop on the Schottky barrier, the proposed *p*-GaN SBDs results in very low leakage current even during high-temperature operation with I_{leak} ~ 2 nA/mm at 400 V and 100 °C, and well below 100 nA/mm at 150 °C (Figure 4.4.4 (a)). This offers an important advantage over devices with no *p*-GaN FP that instead show a large leakage increase at high temperatures (inset in Figure 4.4.4 (a)). In particular, the presented *p*-GaN SBDs show a largely reduced leakage current both at RT and 150 °C compared to state-of-the-art devices based on a planar field plate strategy (Figure 4.4.4 (b)). They also show very competitive performance compared to Tri-anode and partially recessed devices, which however require a more complex fabrication process. Finally, the *p*-GaN SBDs present a breakdown voltage of 1kV at 1 µA/mm for a L_{AC} of 14 µm, showing a significant leakage current reduction compared to reference MOS devices with I_{leak} below 2 nA/mm up to V_{CA} of 850 V (Figure 4.4.4 (c)). This results in an excellent $R_{ON,sp}$ vs V_{BR} benchmark for the proposed *p*-GaN SBDs compared with state-of-the-art GaN-on-Si lateral SBDs in the literature (Figure 4.4.4 (d)), which proves the great potential of the proposed devices for power conversion applications.

In conclusion, in this section, we proposed an AlGaN/GaN SBD architecture based on a *p*-GaN cap layer to achieve excellent off-state performance with a very low off-state leakage current. By a proper design of the heterostructure, the voltage drop over the Schottky junction was effectively reduced while a large carrier density in the access region was achieved. This led to good on-state performance combined with a very low leakage current both at RT and up to 150 °C. Finally, the proposed device is particularly appealing as it shares the well-established fabrication process of commercial *p*-GaN HEMTs and thus represents a promising and viable solution for future GaN SBDs.

5 Thermal Management of High Power-Density GaN Devices and ICs

5.1 Introduction

Wide band-gap semiconductors, such as GaN, have the potential to dramatically reduce the footprint of power devices thanks to their excellent material properties. This has resulted in major improvements in the V_{BR}^2 /R_{ON} figure-of-merit compared to conventional Si power transistors [17], [201] (*Chapter 2* and *3*). Besides, the reduction in device size, in combination with the lateral nature of GaN power devices, enables monolithic integration of multiple components into compact power ICs, largely increasing the power density (*Section 4.3*). However, this also leads to significantly higher heat fluxes [64] with respect to silicon power devices, which, if not properly managed, degrade performance due to self-heating and limit any further device miniaturization. In particular, premature self-heating of the device leads to a reduced component lifetime, degraded performance, and limited power density. In addition, the reduced current capability of the device as a result of self-heating requires paralleling several transistors for high-current applications, which increases the overall system cost and complexity.

Typical thermal management solutions, such as forced-convection air-cooling, struggle to handle such large heat fluxes [65], and current alternative solutions like the use of high thermal conductivity substrates, e.g. SiC and diamond, are prohibitively expensive for widespread adoption (see Table 5.1.1). The silicon substrate has a significantly lower thermal conductivity (150 W/mK) but is orders of magnitude more cost-effective. As such, most successfully commercialized GaN devices for power electronics applications have focused on using a silicon substrate. Yet, the substrate provides little functionality to the electronic device, other than carrying the few micrometers of AlGaN/GaN epi-layer that provides the active region for the electronics.

Embedded liquid cooling by etching microchannels in the device substrate, through which a coolant is flown, is an effective and well-established technique to cope with high heat fluxes. In particular, this approach has been introduced in the ‘80s for silicon logic [67]–[71] and was later proposed for GaN-based RF applications [64]. However, its adoption by power devices is typically limited by their vertical

Substrate	*k* [W/mk]	*Cost* [$/cm^2]
Sapphire	40	10^0
Si	150	$<10^0$
SiC	380	10^1
Diamond	2200	10^3

Table 5.1.1: Properties of non-native substrates for GaN electronics [66]

architecture, which prevents the micro-structuring of the substrate. Yet, GaN-on-Si devices present a lateral device structure on a silicon substrate that is well-suited for deep etching, making it ideal for the integration of this technology.

In a conventional indirect cooling configuration, the heat flux generated in the active layer propagates through multiple materials and interfaces, such as the device packaging and the thermal interface material (TIM), before reaching the ambient air, resulting in a large thermal resistance (*Appendix B*). In embedded liquid cooling, the heat sink is directly integrated inside the chip, resulting in direct cooling of the device. In particular, this approach enables the complete removal of the thermal resistance contributions linked to the device package and the TIM, while also greatly reducing the convective thermal resistance (*Appendix B*). Thanks to this approach, direct cooling methods based on microchannels [67], [202], pin fins [203], [204], impinging jets [205], and manifold microchannels [206], [207] have been successfully demonstrated to very high heat fluxes, surpassing 1 kW/cm^2, which is extremely promising for high-power density GaN devices. For these reasons, the integration of embedded liquid cooling into GaN-on-Si power devices is a promising approach to manage the resulting high-heat fluxes and to enable ultra-compact power converters with unprecedented power densities by turning the GaN-on-Si substrate into a cost-effective, high thermal performance platform.

Moreover, besides demonstrating the promising thermal performance of this technology, a thorough characterization of the impact of embedded liquid cooling on GaN-on-Si power devices' electrical performance, especially at high voltages, is required. This is crucial to rule out any degradation in the device performance due to the embedded liquid cooling and to validate the technology. In particular, previous works have shown that the removal of the substrate in GaN-on-Si devices may cause increased switching losses [208], [209], potentially outweighing the benefits from the improved device cooling. Furthermore, the choice of the best type of coolant for embedded liquid cooling of power devices is not yet clear nor is its influence on the device's operation.

This chapter is divided into two sections whose purpose is to demonstrate embedded liquid cooling as a new thermal management solution for GaN-on-Si power devices and to show its potential for high power density GaN ICs.

1. In the first section, we integrate embedded liquid cooling on a 650 V, 50 mΩ GaN-on-Si commercial power device. We investigate the impact of embedded liquid cooling on the DC and switching characteristics of the device and demonstrate no performance degradation. In addition, we demonstrate that much higher current capabilities and an improved $R_{ON} \times E_{oss}$ figure-of-merit in a large output current range can be achieved by the proposed approach, compared to forced-convection air-cooling. Finally, we compare deionized water and a dielectric fluid (3M Novec 7200), revealing a trade-off between thermal performance and reliability during high-voltage operation.

2. In the second section, we demonstrate the potential of embedded liquid cooling to manage the high heat fluxes of GaN power ICs. To this end, we apply embedded liquid cooling on a monolithically integrated full-wave bridge rectifier (FWBR) realized with the high-performance Tri-anode GaN Schottky SBDs presented in *Chapter 4*, demonstrating improved thermal and electrical performance.

5.2 Impact of Embedded Liquid Cooling on the Electrical Characteristics of GaN-on-Si Power Transistors

In this section, we investigate the integration of liquid cooling on 650 V, 50 mΩ GaN-on-Si commercial power devices. We perform a thorough characterization of the device DC and switching characteristics and demonstrate no degradation as a consequence of the channel etching in the Si substrate or the liquid flow. Besides, we show that much higher current capabilities and an improved $R_{ON} \times E_{oss}$ figure-of-merit in a large output current range can be achieved by the proposed approach, compared to forced-convection air-cooling. Finally, we present that, while deionized (DI) water provides better thermal performance as a coolant, the dielectric fluid 3M Novec 7200 results in improved package reliability during high-voltage operation.[1]

5.2.1 Experimental Setup and Fabrication

The device under test (DUT) is a 650 V, 50 mΩ GaN-on-Si commercial power transistor with a 4 mm × 2.4 mm wafer-level chip-scale package (WLCSP), exposed-backside Si substrate, and land grid array (LGA) solder bumps. No internal connection is present between the source and the substrate, which is floating. However, a similar characterization to the one here presented was performed on a 100 V GaN-on-Si power device with substrate internally grounded, which showed the same behavior as the one here reported. Commercial devices were selected for this study as they offer a repeatable and stable platform to evaluate the impact of embedded liquid cooling on the device's performance, especially at high voltages. Micro-channels were defined on the DUT's backside by optical lithography followed by deep reactive ion etching (DRIE) of the Si substrate (Figure 5.2.1(a)). This process relies on simple wafer-scale post-processing, which enables the substrate microstructuring of several chips in a full wafer at the same time, and thus can be very cost-effective (see *Appendix B*). The channel width and spacing were both set to 50 µm while their depth was 330 µm, leaving about 50 µm of Si between

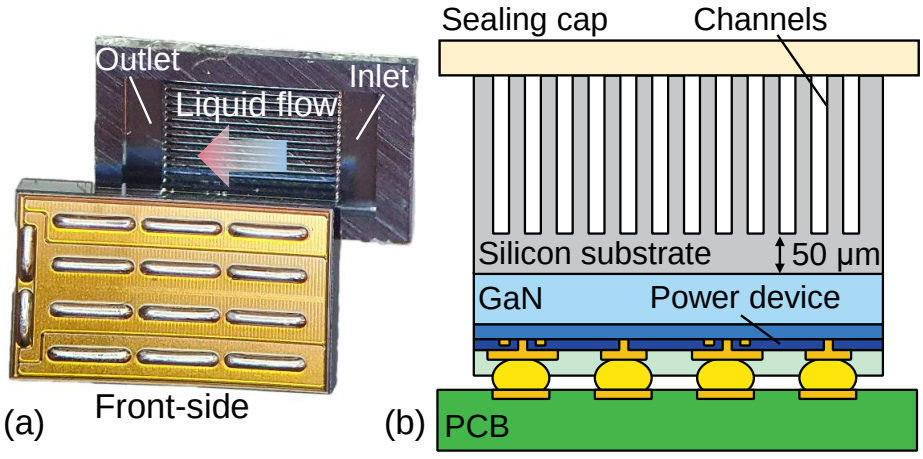


Figure 5.2.1: (a) Top view of the front- and back-side of the 650 V, 50 mΩ commercial GaN power device investigated in this study. On the backside, the micro-channels etched in the Si substrate for the embedded liquid cooling are visible. The device dimensions are 4 mm × 2.4 mm (b) Cross-sectional schematics of the liquid-cooled DUTs mounted on the testing PCB.

[1] This section is based on **L.Nela,** R. van Erp, N. Perera, A. Jafari, C. Erine, and E.Matioli, "Impact of Embedded Liquid Cooling on the Electrical Characteristics of GaN-on-Si Power Transistors", *IEEE Electron Device Lett.*., vol. 42, no. 11, pp. 1642–1645, (2021). © 2021 IEEE. **Contribution: First Author.**

the channels and the GaN buffer layers. While the remaining Si layer does not impact significantly the overall thermal resistance [66], it preserves the chip's mechanical stability and provides a common potential to the device substrate. Reference transistors with the same design but completely removed Si substrate showed early failure during switching operation, likely due to an uneven potential distribution in the GaN buffer layer as a result of the missing connection to the substrate, and thus were not characterized in this work. Two larger (0.5 mm × 1.7 mm) openings at the device edges provided the inlet and outlet for the coolant (Figure 5.2.1 (a)). Further analyses on the microchannels geometry optimization, in particular on the optimal width and its impact on the thermal resistance and pressure drop, and on the long-term stability under different flow conditions can be found in [202], [210], [211].

Following the micro-channel etching, the devices were soldered to a PCB for testing (Figure 5.2.1 (b)). The device temperature was monitored through a thermistor placed close to the DUT, which was first calibrated to the device surface temperature using an infrared camera. Devices with no microchannels in the Si substrate (*Unetched*) were used as a reference to compare the electrical performance. For the thermal characterization, reference devices with no heatsink under natural convection (*No cooling*) and with a heat sink and fan with a nominal thermal resistance of 5 K/W (*Fan + heat sink,*) were considered. The performance of DI water (*Water cooled*) and the dielectric fluid Novec 7200 (*Novec* cooled) were compared at the same flow rate of 280 µl/s, which resulted in a pressure drop of 500 mbar. Statistical analyses were performed on at least 8 devices of each kind.

5.2.2 DC and Switching Characterization

Figure 5.2.2 (a) shows the threshold voltage (V_{TH}), extracted at 1 mA, and the peak transconductance (g_m) for four different cases: 1. unetched DUTs (*unetched*); 2. DUTs with etched microchannels in the backside with no fluid flowing (*Air*), 3. with DI water cooling (*water*), and 4. with dielectric coolant Novec 7200 cooling (*Novec*). No appreciable variation between the different conditions was observed, suggesting that the device gate control is unaffected by the embedded liquid cooling. However, the DUTs output characteristic highly benefited from the more efficient cooling. While the on-resistance (R_{ON}) at room temperature (RT) was the same for all DUTs, about 48 mΩ, the achievable drain current (I_D) for uncooled transistors was strongly limited by the device self-heating (Figure 5.2.2 (b), blue curve), which significantly reduced the transistor's maximum current capability. The use of a heat sink and fan alleviated the self-heating degradation but still resulted in an early saturation of the maximum I_D. On the contrary, DUTs with embedded liquid cooling showed a much-reduced R_{ON} increase due to self-heating with no I_D saturation in the measured range, which enabled achieving a drain current more than 4 times larger than with conventional cooling techniques (Figure 5.2.2 (b)). This resulted in a considerable reduction of the DUT conduction losses and in an increase of its current capability, offering a promising solution to reduce the need for device parallelization in high-current applications.

The off-state leakage current of the DUTs was measured up to the rated device voltage and showed no noticeable variation between unetched and liquid-cooled devices (Figure 5.2.2 (c)). However, a significant difference between devices cooled with DI water and Novec 7200 was observed in case of failure of the liquid cooling package (Figure 5.2.2 (d)). A water leak was particularly detrimental for the DUT voltage blocking capabilities as the liquid easily ionized and created a low resistivity connection between the device terminals, leading to high leakage current and device failure. On the contrary, a Novec 7200 leak did not impact at all the device off-state leakage (Figure 5.2.2 (d)). This is

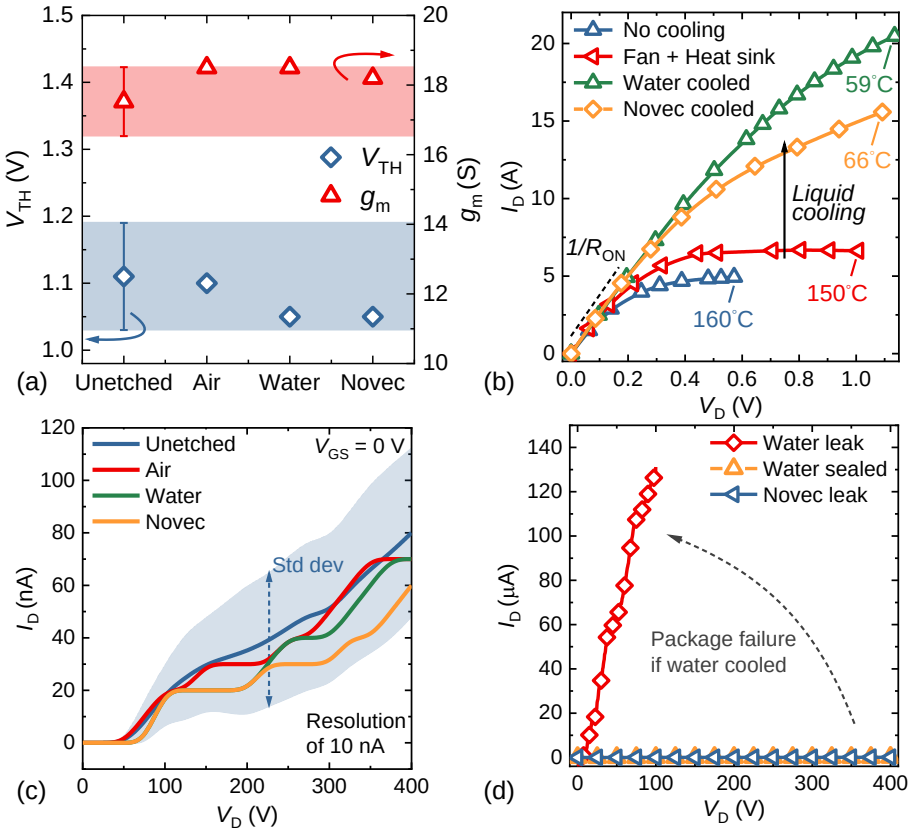


Figure 5.2.2: (a) V_{TH} (at 1 mA) and peak g_m extracted from the device pulsed transfer curve. (b) DC output curve for the DUTs. The liquid coolant flow rate was set to 280 µl/s. (c) Off-state leakage up to 400 V. The resolution of the current measurement is 10 nA. (d) Off-state leakage in case of package failure with DI water and Novec 7200 as coolants flowing in the device.

because Novec 7200 is a dielectric fluid that is not sensitive to high voltage, thus resulting in no additional leakage and improved system reliability in case of a package failure.

GaN power devices suffer from increased R_{ON} during high-voltage switching operation due to electron trapping at the top AlGaN interface and in the GaN buffer (*Sections 1.4.2* and *2.4*). Previous works have shown an additional dynamic R_{ON} ($R_{ON,Dyn}$) degradation following the Si substrate removal as a consequence of the newly created GaN buffer-to-air interface on the device backside [208], [209]. To characterize $R_{ON,Dyn}$ for devices with embedded liquid cooling, pulsed *I-V* measurements were performed. The DUTs were stressed in the off-state (V_G = 0 V) for t_{off} of 5 ms at a quiescent drain bias ($V_{D,q}$) and then shorty turned on (V_G = 5 V) for a time t_{on} of 50 µs during which their on-resistance was measured. Figure 5.2.3 (a) presents the typical $R_{ON,Dyn}$ degradation for unetched devices, which reached about 2 times the DC value for $V_{DS,q}$ of 200 V, and then saturated. However, no relevant variation was observed as a consequence of the micro-channels etching or the coolant flow (Figure 5.2.3 (b)). Indeed, the remaining Si layer between the GaN and the microchannels prevents the formation of additional trapping sites at the bottom GaN buffer interface and any variation in $R_{ON,Dyn}$.

Due to the high operating frequencies at which GaN devices are typically employed, switching losses represent an important contribution to the overall device efficiency. Switching losses are typically categorized as soft- and hard-switching, depending on the circuit topology and operating conditions. Soft-switching losses are caused by the non-ideal charging and discharging of the device output capacitance (while the device is OFF) and become relevant in power circuits designed for high-frequency operation such as resonant converters. Hard-switching losses occur instead when a device is

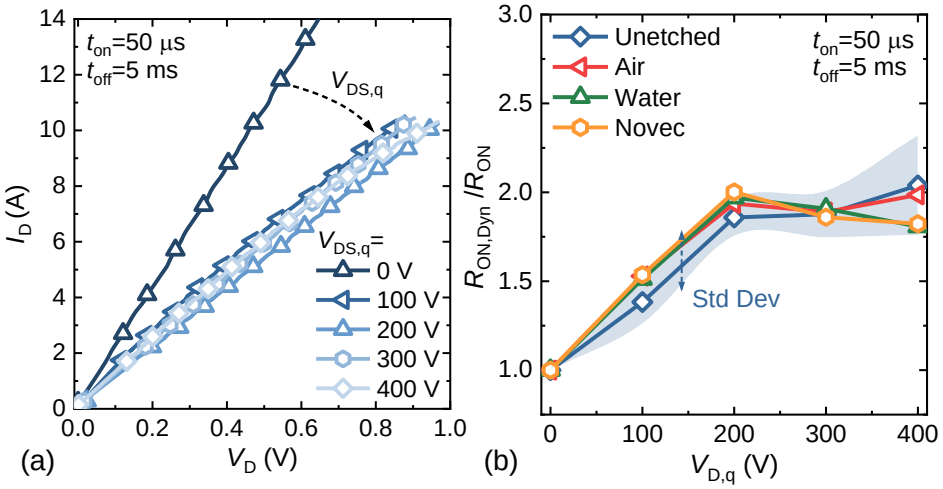


Figure 5.2.3: (a) Pulsed *I-V* characteristics of an unetched device for different $V_{D,q}$. (b) Dynamic on-resistance as a function of $V_{D,q}$ for unetched DUTs and devices with embedded liquid cooling.

turned on while still subjected to a large V_{DS}. They depend on the energy stored in the DUT output capacitance (E_{oss}) and on the current and voltage overlap during the turn-on transient.

A Sawyer Tower (ST) measurement was performed to characterize the switching losses of DUTs with embedded liquid cooling. The transistor source and gate electrodes were connected and a reference capacitor (C_{ref}) was introduced between the DUTs source and the ground (Figure 5.2.4 (a)). The device output charge (Q_{oss}) as a function of the drain to source voltage (v_{DS}) was obtained by applying a large-signal sinusoidal input voltage (v_{IN}) and measuring the voltage over the reference capacitor (v_{REF}). By considering the hysteresis loop of Q_{oss} versus v_{DS}, the energy dissipated at each soft-switching cycle (E_{Diss}) was extracted [212]. Figure 5.2.4 (a) shows a rather small E_{Diss} value [164], [212] (extracted at 100 kHz with v_{DS} of 400 V) for unetched devices, which was maintained without significant variations for DUTs with etched microchannels and with embedded liquid cooling. To confirm this behavior also at higher switching frequencies, the equivalent series resistance (R_s) of the output capacitance C_{oss} was considered (Figure 5.2.4 (b)). This method, based on a small signal excitation, has shown good matching with results from ST [213], [214] and allows investigating soft-switching losses at frequencies in the order of tens of MHz, which is challenging for techniques based on large-signal excitations, such as the ST. No appreciable variation of R_s up to 20 MHz was observed (Figure 5.2.4 (b)), which demonstrates that soft-switching losses are not affected by embedded liquid cooling and indicates that traps in the GaN buffer are the main responsible for determining E_{Diss} in these devices [215], [216], which were not affected by introducing microchannels in the silicon substrate.

By integrating the Q_{oss} versus v_{DS} curve obtained from the ST measurement (Figure 5.2.4 (c)), one can extract the energy stored (E_{oss}) in the device output capacitance, which is dissipated at each hard-switching cycle and represents an important term in hard-switching losses [166], as shown in eq. 5.1:

$$P_{SW,hard} = f \times E_{oss} + P_{VI}(R_g, g_m) \qquad 5.1$$

Since the microchannel etching and the liquid flow do not impact the Q_{oss} nor its dependence on v_{DS}, a constant E_{oss} value is measured for all the DUTs (inset in Figure 5.2.4 (c)). The current-voltage overlap

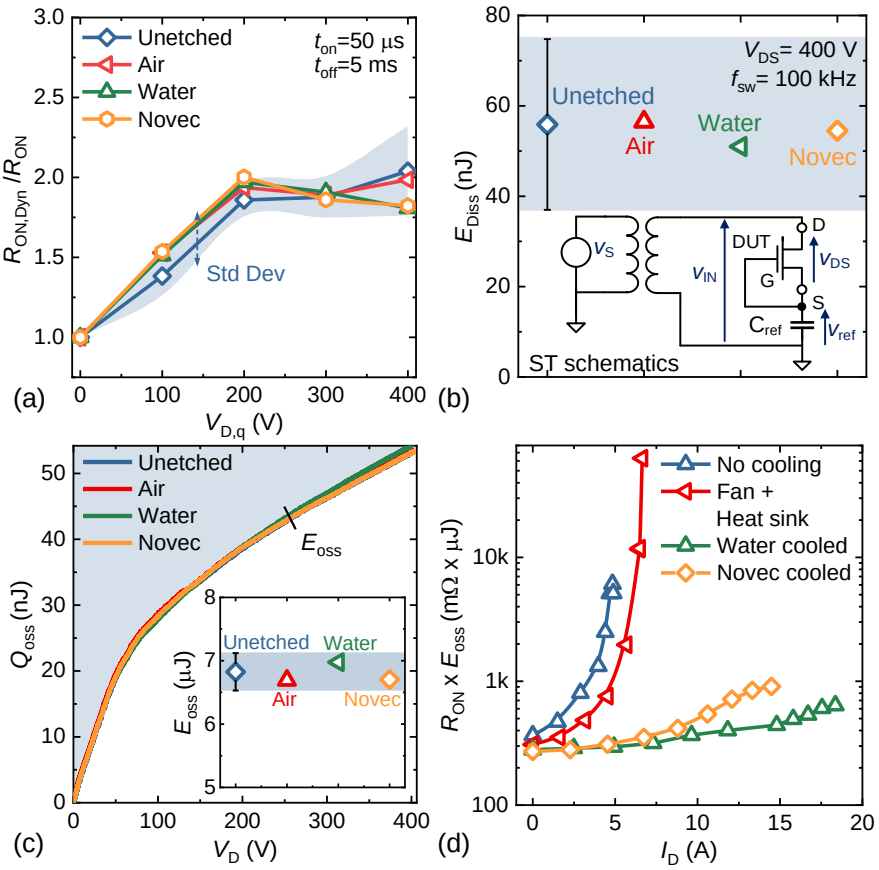
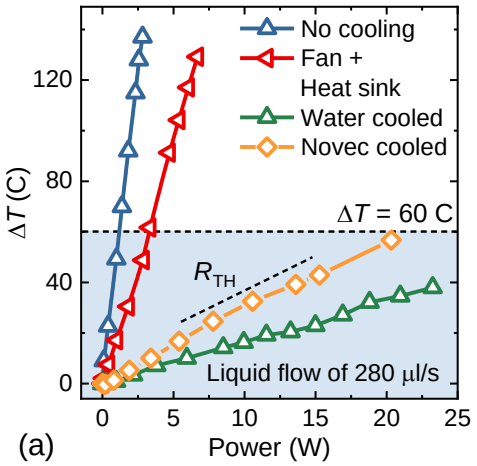


Figure 5.2.4: (a) E_{Diss} at 100 kHz and v_{DS} of 400 V for the DUTs. The bottom inset shows the ST measurement setup. (b) R_s as a function of frequency for a drain voltage of 40 V. (b) Q_{oss} as a function of v_{DS} and corresponding E_{oss} extracted from the curve integration. (d) $R_{ON} \times E_{oss}$ figure-of-merit as a function of the device drain current.

term (P_{VI}) is linked to the load current and to the time required to discharge C_{oss} through the channel, which is typically controlled by using an external gate resistor (R_g). In its absence or in the case of very low gate-path resistance, the turn-on time is determined by the device transconductance (g_m) [165], whose value is the same for all DUTs (Figure 5.2.2 (a)). Thus, it is possible to conclude that embedded liquid cooling does not affect the device's hard-switching losses. On the other hand, the important device figure-of-merit $R_{ON} \times E_{oss}$, which summarizes the contribution of conduction and hard-switching losses, is greatly improved with embedded liquid cooling. Thanks to the reduced device self-heating, a low $R_{ON} \times E_{oss}$ value can be maintained for much larger output currents (Figure 5.2.4 (d)), which ensures efficient operation for high-current applications and reduces the need for device oversizing. Besides, no coupling between the electrical signal and the coolant was observed up to a frequency of ~ 6 GHz, which was determined by measuring the transmission parameter (S_{21}) of a waveguide realized on a similar structure with embedded liquid cooling. This shows that no significant electrical coupling to the coolant is present in the whole frequency domain relevant to power electronics.

The improved thermal performance of embedded liquid cooling can be appreciated considering the DUTs temperature as a function of the power dissipated over the device and the corresponding thermal resistance (R_{TH}). While for uncooled DUTs and transistors cooled with traditional heat sink and fan only a few Watts can be dissipated before reaching high temperatures above 150 °C, embedded liquid cooling ensures much-reduced temperature rise, significantly improving the device efficiency and reliability, and expanding the maximum allowed power dissipation over the device (Figure 5.2.5 (a)). This translates into a 12-fold reduction in thermal resistance for devices with embedded liquid cooling



	R_{TH} (K/W)	P_{Max} (W)*	Heat flux (W/cm^2)*
No cooling	47.8	1.2	13
Fan + Heat sink	19.5	3	32
Water cooling	1.6	37.5	390
Novec cooling	2.95	21	220

*For ΔT_{Max} of 60 °C

(b)

Figure 5.2.5: (a) DUTs temperature as a function of the dissipated power over the device for different cooling techniques. (b) R_{TH} and maximum power and heat flux that can be extracted for a temperature rise of 60 °C.

(compared to fan + heat sink) and into the ability to manage much larger heat fluxes (Figure 5.2.5 (b)), which is a key requirement to take full advantage of GaN power devices miniaturization. Figure 5.2.5 also shows the dependence of the embedded liquid cooling thermal performance on the type of coolant employed. The use of Novec 7200 results in an R_{TH} which is almost double the one of DI water at the same flow rate. Such a difference can be explained by the larger heat capacity of water (c_p = 4.18 kJ/kg^{-1}K^{-1}) with respect to Novec 7200 (c_p = 1.22 kJ/kg^{-1}K^{-1}), which allows to more efficiently absorb and extract heat from the device (*Appendix B*). Nevertheless, as shown in Figure 5.2.2 (d), Novec 7200 leads to improved reliability in case of package failure, which is extremely important for power electronics. The choice of the optimal cooling taking into account the trade-off between the thermal performance and the package reliability should be based on the specific application.

In this section, we have demonstrated 650 V, 50 mΩ GaN-on-Si commercial power devices with embedded liquid cooling in the device substrate. The presented results show the potential of this thermal management technology to drastically improve the device's performance, resulting in higher current capability and much-reduced $R_{ON} \times E_{oss}$ figure-of-merit in a large output current range compared to forced-convection air-cooling. On the other hand, no degradation of the device DC or switching characteristics has been observed as a consequence of the embedded liquid cooling, which proves the robustness of the proposed approach. Finally, we compared the performance of DI water and Novec 7200 for embedded liquid cooling, which provides useful guidelines for an optimal coolant choice depending on the specific application.

5.3 Embedded Liquid Cooling of GaN Power ICs

The lateral nature of AlGaN/GaN electronics enables the monolithic integration of multiple power devices onto a single substrate, as presented in *Section 4.3*. This opens up opportunities for power electronics, whereby an entire converter can be integrated on a small chip, with a great potential for energy, cost, and space savings. However, as more components are integrated on the same chip, higher heat fluxes need to be properly managed to avoid limiting the maximum output power of the chip.

To demonstrate the potential of embedded cooling of GaN-on-Si power ICs, here we consider a monolithically integrated full-bridge rectifier. Four of the high-performance Tri-anode Schottky barrier diodes presented in *Chapter 4* were monolithically integrated on the same chip and connected to realize a Full Wave Bridge Rectifier (FWBR) able to provide AC-DC power conversion. At the end of the device fabrication, the chip top side was coated with a photoresist as a protective layer, before flipping the substrate and temporarily bonding it to a carrier wafer. This enables the fabrication process on the silicon substrate. Microchannel structures with a channel width and spacing of 50 µm were patterned using optical lithography, followed by a deep reactive ion etching step (DRIE) to create high aspect ratio microchannels with a depth of 500 µm. Finally, the substrate was detached from the carrier wafer and diced into individual power ICs, which were wire bonded to a testing PCB. [1]

Figure 5.3.1 (a-c) shows the power ICs and the experimental setup employed to characterize its operation. Thanks to the small Tri-anode SBDs reverse recovery charge (see *Section 4.2*), the FWBR can properly operate at a frequency of 1 MHz without signal distortion (Figure 5.3.1 (d)) or overheating due to excessive switching losses. Moreover, by adding an output smoothing capacitor, full AC-to-DC rectification was achieved, with minimum output ripple thanks to the high-frequency operation.

Embedded liquid cooling was integrated into the power ICs by employing a three-layer PCB that was used to guide the coolant to the microchannels in the chip's substrate (Figure 5.3.2 (a-b)). The converter with integrated liquid cooling is shown in Figure 5.3.2 (c-d) and presents a very compact form factor

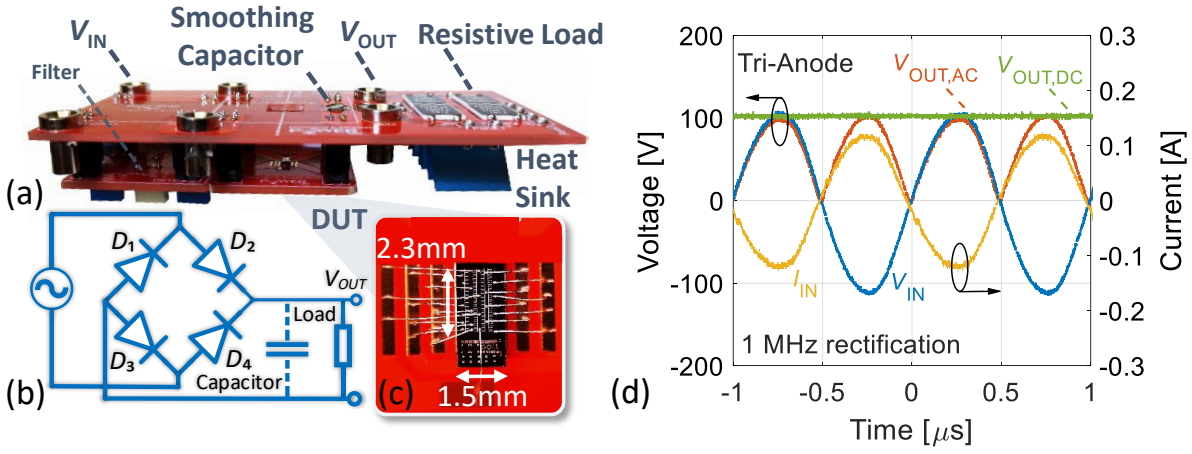


Figure 5.3.1: (a-c) PCB setup for the FWBR testing with the corresponding circuit schematics and image of the wire-bonded die. (d) 1 MHz full-wave rectification for a Tri-Anode based FWBR with a 200 V peak-to-peak signal. Full AC-to-DC rectification was achieved by the addition of an output smoothing capacitor.

[1] This section is based on R. van Erp, R. Soleimanzadeh, **L. Nela,** G. Kampitsis, and E. Matioli, "Co-designing electronics with microfluidics for more sustainable cooling", *Nature*, vol. 585, no. 7824, pp. 211–216, 2020. **Contribution:** design, fabrication, and characterization of the GaN power IC. Support to the microchannel etching, liquid cooling packaging, and device testing.

(4 cm x 2 cm) and proper rectifying operation (Figure 5.3.2 (e)). Embedded liquid cooling led to a small temperature rise of 0.34 K per watt of output power. For a maximum temperature rise of 60 K, this single die can thus produce an output power of 176 W at a flow rate of only 0.8 ml s^{-1}. Furthermore, the reduced operating temperature led to an increased conversion efficiency (Figure 5.3.2 (f)) by eliminating self-heating degradation from the electrical performance. The AC–DC converter was experimentally evaluated up to 120 W of output power, while the temperature rise stayed below 50 K (Figure 5.3.2 (g)). Considering the small converter volume (4.8 cm^3), this corresponds to a high power density of 25 kW dm^{-3}. Moreover, since all cooling occurs within its footprint, multiple devices can be

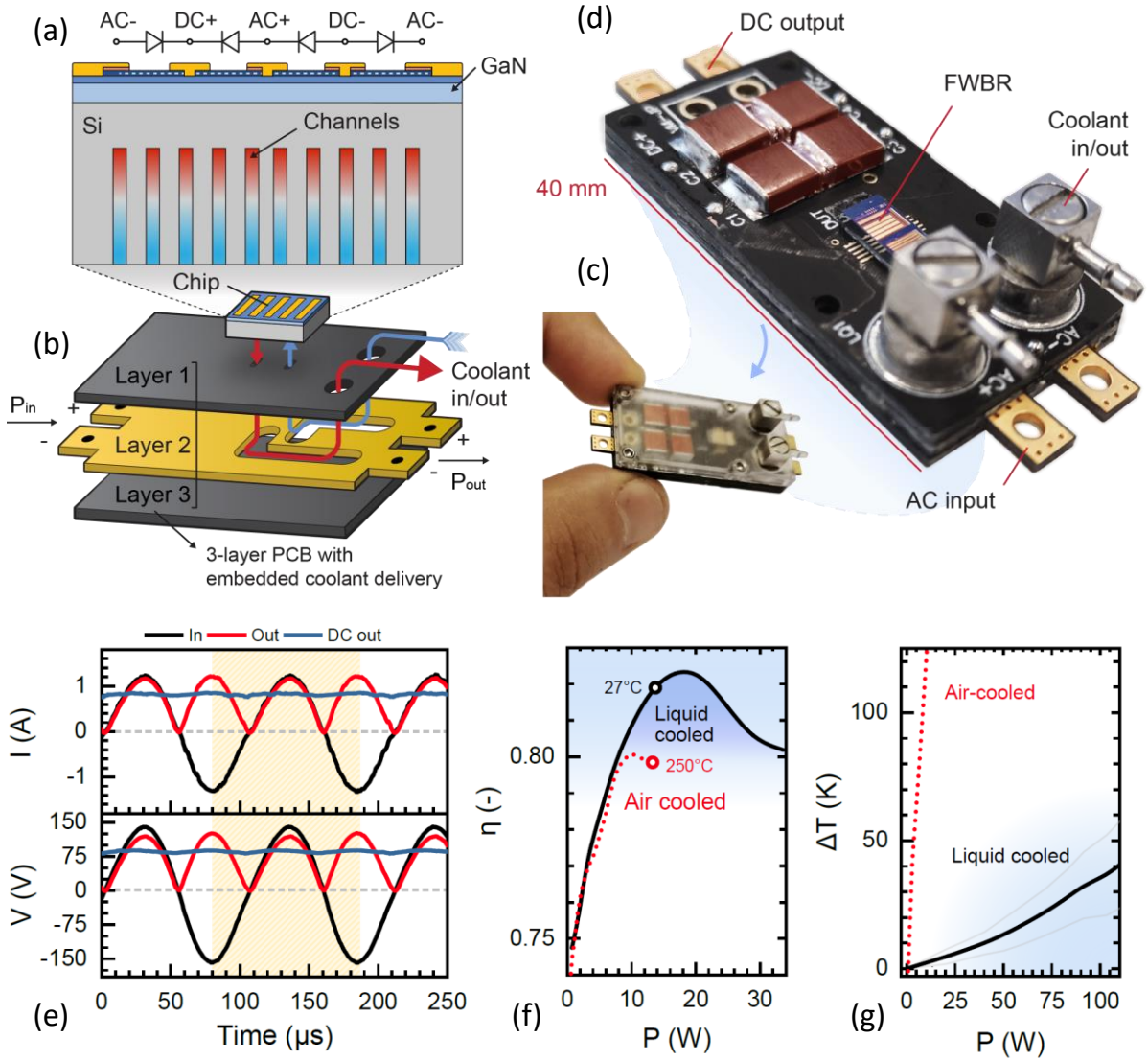


Figure 5.3.2: (a) Schematic of the ultra-compact liquid-cooled power IC based on four GaN power Schottky barrier diodes integrated on a single chip in a full-bridge configuration. (b) A PCB-embedded coolant delivery was developed to feed the coolant to the device. (c-d) Photograph of the full 120-W ac–dc converter with coolant delivery to the liquid-cooled power integrated circuit. (e) Rectification waveforms of the converter while being liquid cooled. The black curve represents the 150-V AC input, the red and blue curves are the output waveforms before and after the smoothing capacitor filter. (f) Efficiency versus output power for the air-cooled and liquid-cooled AC–DC converter. At identical output power, the liquid-cooled converter exhibits substantially higher efficiency owing to the elimination of self-heating degradation. (g) Temperature rise versus output power, showing a much higher temperature at equal output power for the air-cooled device compared to the embedded liquid cooling, which causes a large self-heating degradation.

densely packed onto the same PCB to increase the output power. This is a clear benefit over conventional heat sinks relying on heat spreading to large areas.

In this section, the concept of substrate-embedded microchannel cooling of GaN-on-Si power ICs was demonstrated. Heat fluxes of up to 417 W/cm^2 were effectively managed, resulting in a maximum device temperature below 60 K. Much larger heat fluxes could be removed by embedding the cooling directly into the semiconductor die compared to conventional air-cooling techniques. In addition, by effectively reducing device self-heating, embedded liquid cooling enabled a 30 times increase of the power ICs output power. These results demonstrate the potential to realize ultra-compact high-power converters by combining the unique GaN-on-Si lateral platform and embedded liquid cooling.

6 Conclusion and Future Directions

6.1 Achieved Results

This thesis focuses on the major challenges of lateral GaN high-voltage power devices presented in *Chapter 1*.

Improving the $R_{ON,sp}$ vs V_{BR} trade-off. The fundamental trade-off in power devices between the specific on-resistance and the breakdown voltage was improved based on two different approaches.

On the one hand, multi-channel power devices were designed to significantly decrease the on-resistance while maintaining outstanding blocking performance. A nanostructures gate region was employed to enable excellent control over all of the embedded channels, achieve E-mode operation, and effectively manage the off-state electric field in such highly conducting heterostructures. In addition, a novel surface passivation technique, conformal to the multi-channel nanowires, was developed to ensure reduced current collapse up to high off-state voltages

On the other hand, we investigated the potential of the Super Junction concept to improve the off-state electric field distribution, and thus increase the device breakdown voltage. A novel device architecture called intrinsic Polarization Super Junction (i-PSJ) was proposed, enabling excellent charge matching for any surface condition, without relying on doping of the GaN cap, which led to simulated devices with a flat electric field profile in the whole drift region. The potential of i-PSJ devices was revealed by introducing a physical model to compare the off-state behavior of i-PSJ and HEMT devices, which demonstrated a significant improvement in both DC and switching losses for i-PSJ devices.

Novel architectures for high-efficiency AlGaN/GaN Schottky barrier diodes. We presented the potential of Tri-anode SBDs to improve not only the DC behavior but also to reduce the switching losses compared to conventional planar architectures, as shown by the much decreased $R_{ON} \cdot Q_{rr}$ figure-of-merit. We demonstrated that GaN Tri-anode devices can also outperform state-of-the-art commercial Si and SiC devices and have a great potential for power ICs thanks to their lateral structure. The potential of the proposed Tri-anode SBDs was shown by realizing a DC-DC magnetic-less boost converter based on the monolithic integration of 8 of the presented diodes, which enabled higher switching frequency and much-increased power density compared to the same circuit realized with discrete Si and SiC vertical devices.

Lastly, we proposed a simple AlGaN/GaN SBD planar architecture based on a *p*-GaN cap layer to achieve excellent on- and off-state performance without the need of high lithographic resolution or AlGaN barrier partial recess. Such an architecture relies on the well-established fabrication process of commercial *p*-GaN HEMTs and paves the way to quick adoption and commercialization of GaN power SBDs.

Thermal management of high-power-density GaN power devices and ICs. We investigated the impact of embedded liquid cooling on the thermal and electrical performance of GaN power devices. No degradation of the device DC or switching performance due to the embedded liquid cooling was observed, which proves the robustness and validity of the technology. Yet, a significant improvement in the device's thermal performance was demonstrated. 650 V, 50 mΩ GaN-on-Si commercial power devices with embedded liquid showed reduced thermal resistance, more than 4× higher current capability, and much-improved $R_{ON} \times E_{oss}$ figure-of-merit in a large output current range compared to forced-convection air-cooling.

Applied to GaN power ICs based on Tri-anode SBDs, embedded liquid cooling led to a small temperature rise of only 0.34 K per Watt of output power, enabling high power densities of 25 kW dm^{-3} for a temperature rise below 50 °C. These results demonstrate the potential of embedded liquid cooling to effectively manage the high-heat fluxes of GaN power ICs in which multiple components can be densely packed onto the same chip to increase the power density.

In conclusion, this thesis addresses many of the major challenges for GaN power devices. In the first part, novel device architectures, such as multi-channels nanowire devices and i-PSJs, are proposed to improve the performance of GaN power HEMTs while achieving fundamental requirements for power transistors such as E-mode operation and reduced current collapse. Then, the development of a fundamental component for power circuits such as the power SBD is addressed by proposing novel architectures aimed at the reduction of DC and switching losses. The potential of such technology is demonstrated by realizing a high-frequency and ultra-compact power integrated circuit operating as a DC-DC boost converter with improved performance compared to the use of Si and SiC devices. Finally, the thermal management of such high-power density devices is addressed by the use of embedded liquid cooling, which enables the extraction of the extremely high heat fluxes resulting from the device miniaturization and integration that was achieved in the previous chapters.

6.2 Future Directions

Based on the results presented in this thesis, some future research directions are suggested as follows.

Further improvement of $R_{ON,sp}$ vs V_{BR} by multi-channel i-PSJ. In this thesis, we have shown the ability of the multi-channel platform to drastically reduce the device resistance and the potential of i-PSJ devices to significantly improve the off-state electric field distribution. The combination of these two concepts could have a revolutionary impact on the performance of GaN power devices, as shown in *Chapter 3*. Multi-channel heterostructures with excellent charge balance have already been presented in this work, as well as the effectiveness of the tri-gate architecture to control all of the embedded channels. The main challenges remaining are linked to the device fabrication and, in particular, to achieving a proper side contact to the buried 2DHGs. The most promising strategy consists of the regrowth of a high-quality *p*-GaN layer. While this process would require some optimization to reduce

the *n*-type impurities at the regrowth interface, high-quality regrowth of *p*-GaN layers has been demonstrated in several works [217]–[219], proving the feasibility of this technology.

Multi-channel i-PSJ could open completely new horizons for GaN power devices, similar to what Super Junctions have represented for Si devices, leading to an unprecedented reduction in both DC and switching losses.

AlGaN/GaN Power Schottky Diodes. Despite their slower development, GaN lateral SBDs could soon reach full maturity and find their way to commercialization. The main challenges for GaN SBDs have been resolved and these devices show improved performance compared to state-of-the-art commercial Si and SiC devices (*Chapter 4*). Besides, the architecture proposed in *Section 4.4* shares the well-established fabrication process of commercial *p*-GaN HEMTs and could enable a quicker adoption and commercialization of GaN power SBDs. The main research effort will focus on process optimization and especially on the behavior of such devices in real circuit applications. While we have shown the potential of GaN SBDs for ultra-compact and high-frequency applications in *Section 4.3*, further research is still necessary to determine their impact in different applications, to create Spice models, and to take full advantage of their excellent properties.

Monolithically integrated Power ICs. We have presented the potential of GaN power ICs based on Tri-anode SBDs in *Chapter 4*. A promising next step would consist in the integration of both high-performance HEMTs and SBDs to realize fully monolithically integrated power converters. This approach would enable further miniaturization of the converter size and would allow taking full advantage of the high switching frequency of GaN devices by reducing the interconnection parasitics. While, up to now, most of the efforts by GaN manufacturers were aimed at the integration of the gate driver with the power device, 80 V monolithically integrated half-bridge chips have been recently commercialized by EPC, showing the potential of such an approach. Yet, the development of this technology for higher voltage rating and multiple components will require a deeper understanding of the role of the substrate and the introduction of new isolation techniques, such as GaN-on-SOI. Nevertheless, the potential of power ICs, which is unique to GaN-on-Si devices, is outstanding and could enable a new generation of power converters monolithically integrated on a single chip, enabling unprecedented power densities, excellent performance, and reduced cost.

Embedded liquid cooling for GaN devices. *Chapter 5* presented the great importance of novel and effective thermal management solutions to address the large heat fluxes in GaN power devices and ICs. We have demonstrated the outstanding potential of embedded liquid cooling for high power density devices and converters focusing on the impact of embedded liquid cooling on the electrical and thermal performance of GaN power devices. While embedded liquid cooling at the power device level was here extensively investigated, further research efforts are necessary to optimize the external liquid cooling system, which comprises the pump, the heat exchanger, and the connections. To favor the commercialization of such technology, closed-loop systems with reduced size and power consumption, together with excellent long-term reliability, should be designed. In addition, passive systems based on

the heat pipe principle could lead to simpler and more efficient solutions. While these technical challenges would require some optimization and custom designs depending on the specific application, embedded liquid cooling for GaN devices could take inspiration from the numerous already commercially available liquid cooling systems and rapidly develop. The adoption of such technology for power modules and EV applications would result in a significant increase in the power density of GaN devices and enable taking full advantage of their excellent performance.

A GaN Power Devices for Cryogenic Applications down to 4.2 K

While the potential of GaN devices in power electronic circuits is the focus of an extensive research effort, typical characterizations occur at room temperature or, at most, up to 150°C. Yet, there are numerous applications in which power devices need to effectively operate between room temperature down to extreme cryogenic temperatures of ~ 4 K, either because of the environmental conditions (e.g. outer space) or of the system requirements (e.g. superconducting systems). Some of the most interesting examples of power electronics operating at cryogenic conditions are found in the space and aviation domain [77], [78], and in superconducting machines such as superconducting magnets, energy storage systems, and superconducting motors [78], [81], [82]. While for such applications the power systems are typically thermally insulated and maintained at room temperature, this greatly increases their cost, size, and complexity. It would thus be highly beneficial to operate the power converter at cryogenic temperature, which however requires a clear understanding of the power devices' behavior in such conditions.[1]

Typical Si and SiC power devices, along with GaN vertical devices, rely on doping of the semiconductor material and show two main effects as the operating temperature is decreased [78], [220], [221]. On the one side, the carrier mobility increases due to the reduced electron-phonon interaction, which is highly beneficial for device performance. On the other side, however, the freeze-out of dopants results in a reduction of the carrier density, leading to increased channel resistance. The predominant effect depends on the exact operating temperature but their partial compensation leads to Si and SiC power devices that present, depending on the particular device structure, only a mild improvement or even degradation of the low-temperature performance [78]. GaN HEMTs, instead, do not require any doping to achieve a large concentration of electrons in the channel as the carriers are generated by the polarization mismatch between the AlGaN barrier and the GaN layer [222]. Since this phenomenon is independent of temperature, GaN HEMTs benefit from the increased carrier mobility at low temperatures, without suffering any carrier freeze-out.

Despite the promising potential of the GaN technology for cryogenic applications, very few works have investigated the performance of GaN HEMTs in such conditions. In particular, some interesting works have focused on the characterization of a single commercial device (e.g. GaN Systems [79] and EPC [83]), confirming a significant performance improvement. However, these studies were typically performed down to 77 K, leaving the large temperature range below this value unexplored. Moreover, the low-temperature performance of common GaN HEMT architectures, such as Gate Injection Transistor (GIT) and Cascode, has never been reported, posing questions on their behavior in such conditions. Finally, it is still unclear how the device conduction, soft- and hard-switching losses vary at cryogenic temperature and which contribution becomes dominant.

[1] This section is based on **L. Nela,** N. Perera, C. Erine, and E. Matioli, "Performance of GaN Power Devices for Cryogenic Applications down to 4.2 K", *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, 2020. © 2020 IEEE. **Contribution: First Author.**

In this section, we investigate cryogenic cooling for GaN power devices by performing a thorough characterization of the device DC and switching performance in such conditions. We characterize and compare the performance of four GaN commercial power devices based on the most common device technologies, i.e. *p*-GaN Schottky gate, GIT and Cascode, in the wide temperature range between 400 K and 4.2 K. The different losses contributions (conduction, hard- and soft- switching) as well as the device gate control are analyzed and compared as a function of temperature. Significant variations are observed depending on the technology considered, which are discussed and explained based on the device architecture. The presented results clearly show the potential of GaN power devices at cryogenic temperatures and provide insightful guidelines for the design of power converters operating in such conditions.

A.1 Experimental Setup

The device characterization was performed in a Lakeshore CPX-VF cryogenic probe station (Figure A1 (a)). Two identical transistors were soldered on a PCB (Figure A1 (b)) and mounted on the probe station thermal stage, whose temperature (T) was varied between 400 K and 4.2 K. Liquid helium refrigerant was used to lower the stage temperature, which was controlled by a PID feedback loop for optimal stabilization within 0.1 K. The measurements were performed under vacuum condition (10^{-4} mbar at 300 K) to avoid any condensation. Two transistors were used to provide the device DC and switching characterization simultaneously. The gate and source terminals of one device were shorted and a 10 nF (C0G multi-layer ceramic) capacitor C_{ref} was added to perform Sawyer-Tower (ST) measurements [212] to determine the device switching losses (Figure A1 (c)). The input sinusoidal voltage was provided by a 33600A Keysight waveform generator and amplified by a WMA-300 Falco Systems high-voltage amplifier. The voltage signals were read by an MDO3104 Tektronix oscilloscope.

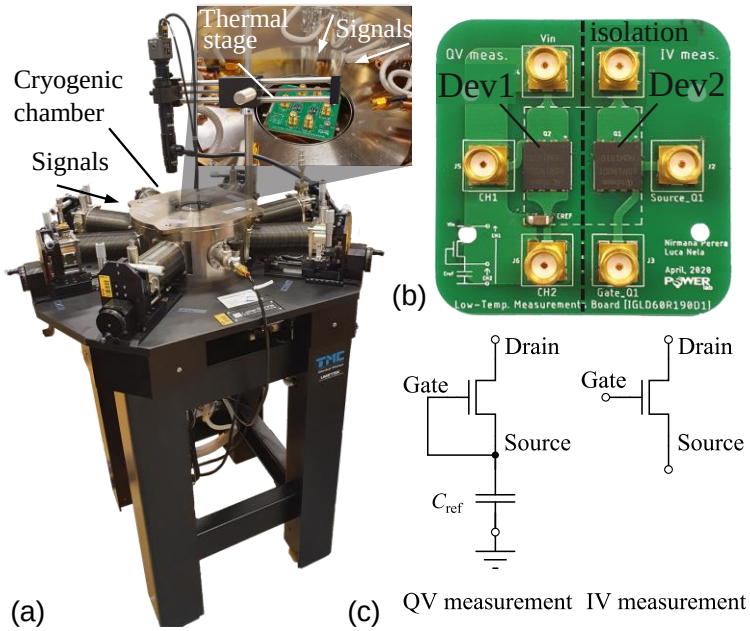


Figure A1: (a) Cryogenic probe station used for the device characterization. The inset shows the testing PCB mounted on the probe station thermal stage (b) Two identical devices were mounted on the same PCB to allow their switching and DC characterization according to the circuit schematics shown in (c)

It should be noted that the C_{ref} value was monitored with temperature and showed no variation. The three terminals of the other transistor were individually connected to a Keysight B1505 analyzer to perform the DC characterization of the device (Figure A1 (c)). Four commercial devices (DUTs) with similar current and voltage ratings but different device technology were characterized and compared (Table A1).

Index	Producer	Name	Gate technology	R_{ON} [mΩ]	V_{DS} [V]	Q_{oss} [nC]
T1	GaN Systems	GS66502B	Schottky *p*-GaN	200	650	16
T2	Transphorm	TPH3206PSB	Cascode	150	650	44
T3	Panasonic	PGA26E19BA	Ohmic *p*-GaN (GIT)	140	600	17
T4	Infineon	IGLD60R190D1	Ohmic *p*-GaN (GIT)	140	600	16

Table A1: Devices investigated in this work and their typical ratings reported in the datasheet. Q_{oss} is extracted for V_{DS}=400 V

A.2 Gate Control Mechanisms and Conduction Losses

Figure A2 (a) shows the GIT T3 transfer curve as a function of temperature, from which a noticeable positive shift of the characteristic is observable. The device threshold voltage (V_{TH}) was extracted at a drain-to-source current (I_{DS}) of 1 mA, as suggested in the datasheet, and compared with the one from the other HEMTs technologies. A significant discrepancy between the devices in the value and behavior of V_{TH} versus T is observed (Figure A2 (b)). GIT devices (T3 and T4) present a quite constant but slowly increasing V_{TH} as the temperature is decreased, with the smallest variation among all of the devices, which confirms the excellent V_{TH} stability of such technology [223]. T2 shows, instead, a large increase of the threshold voltage at cryogenic temperatures, which well agrees with the behavior of the Si device employed to achieve enhancement-mode operation. However, thanks to the gate robustness of such architecture, cascode devices can be driven with large gate voltages (V_G), allowing to compensate for the V_{TH} drift by increasing the driving V_G. On the other side, T1 presents a significant V_{TH} decrease from 1.6 V at room temperature (RT) down to ~1 V at 4.2 K. Such effect, which is consistent with Ref. [79], should be carefully considered when designing the gate driving system as the reduced off-state margin may result in dangerous false turn-on events.

Figure A2 (c) illustrates the behavior of the DUTs on-resistance (R_{ON}) as a function of temperature. Thanks to the electron mobility (μ) increase, all of the transistors show a considerable R_{ON} reduction as the temperature is decreased. This is followed by a plateau region for lower T due to the μ saturation as a consequence of crystal defects. Yet, while the trend is similar for all of the devices, the amount of such reduction strongly depends on the HEMT technology, which can be better appreciated by considering the normalized R_{ON} value to the room temperature one (Figure A2 (d)). T1 and T2 show a very large R_{ON} decrease of ~ 6 times with respect to the RT value, with the onset of the low-temperature plateau region around 100 K. Such a trend agrees well with the sheet resistance (R_{sh}) reduction of the AlGaN/GaN two-dimensional electron gas (2DEG) as a result of the carrier mobility increase. On the other hand, the two GIT devices present only a ~ 2-fold R_{ON} reduction at cryogenic temperatures and

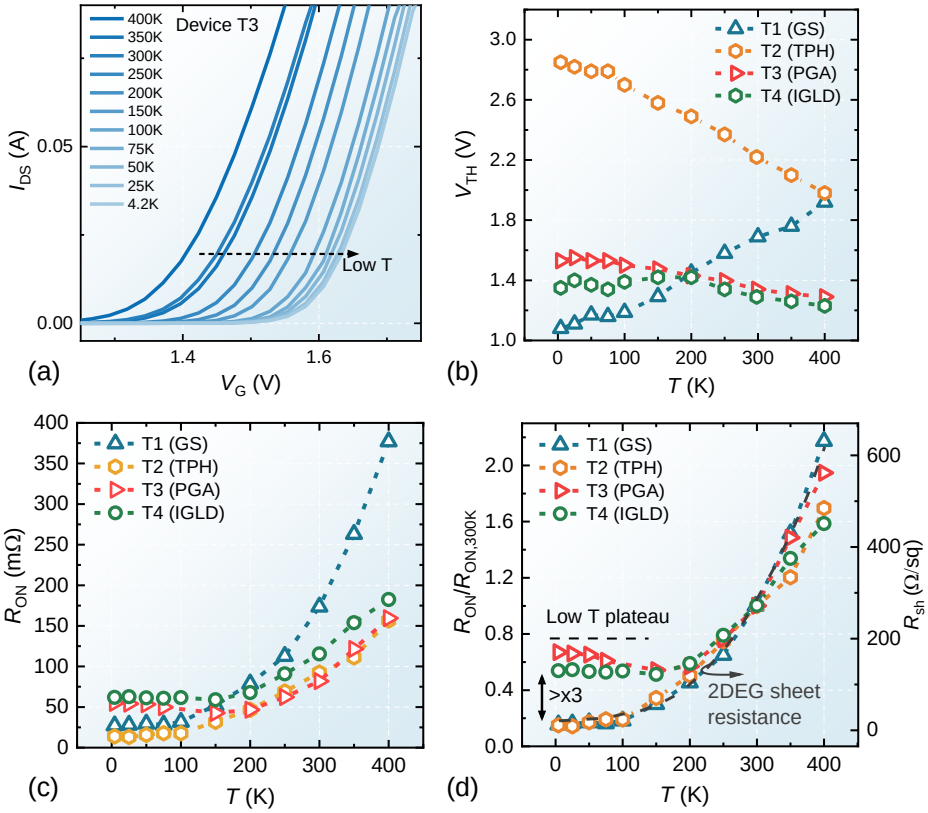


Figure A2: (a) Transfer characteristics for T3 from 400 K to 4.2 K (b) V_{TH} as a function of temperature for the four DUTs. V_{TH} was uniformly defined at a drain-to-source current of 1 mA (c) Comparison of the devices on-resistance as a function of temperature (d) Normalized R_{ON} with respect to the room temperature value for the four DUTs. The right y-axis shows the typical temperature dependence of the 2DEG sheet resistance (R_{sh}).

show a premature onset of the low-temperature plateau. This behavior may be due to the introduction of defects in the gate region during the AlGaN partial recess, which limits the low-temperature mobility. Such diverse behavior among different technologies directly reflects on the device conduction losses and driving circuit, and should be carefully taken into account when choosing the most suitable power transistor for low-temperature applications.

A.3 Switching Losses

Depending on the operation conditions of the circuit, power devices are subjected to either soft- or hard- switching losses. While these loss mechanisms are broadly studied at RT conditions, their behavior at cryogenic temperature is yet to be fully investigated.

In particular, soft-switching losses occur due to the non-ideal charging and discharging of the device output capacitance (C_{oss}) and become relevant in high-frequency power electronic circuits, such as resonant and quasi-resonant converters [224]. Soft-switching losses are typically characterized by a Sawyer Tower measurement (Figure A3 (a)), which allows determining the discrepancies between the C_{oss} charging and discharging processes. To this end, the transistor source and gate terminals were shorted and a reference linear capacitor (C_{ref}) was introduced between the source of the device and the circuit ground. By applying a large-signal sinusoidal input voltage (v_{IN}) and measuring the voltage over the reference capacitor (v_{REF}), the transistor output charge (Q_{oss}) versus drain-to-source voltage (v_{DS})

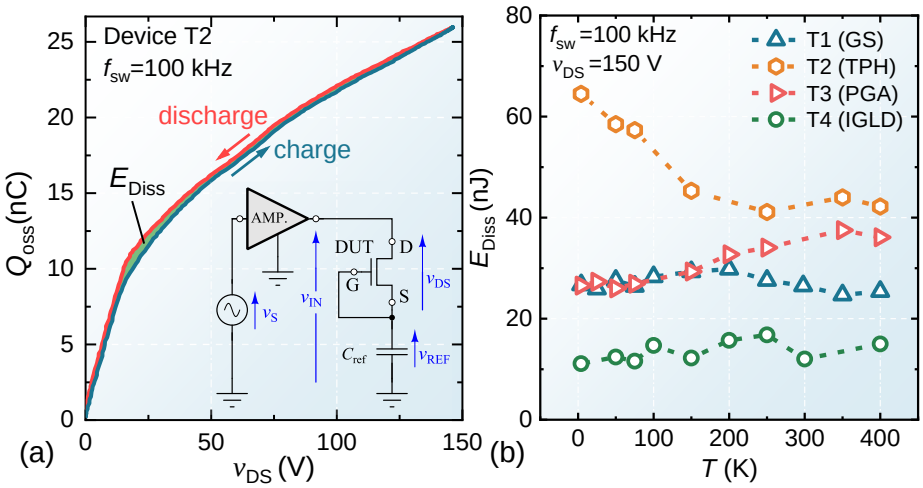


Figure A3: (a) Sawyer-Tower measurement for T2. The circuit schematic of the measurement setup is shown in the bottom right inset. (b) E_{Diss} as a function of temperature for the four DUTs.

was obtained. It was thus possible to extract the energy dissipated at each switching cycle (E_{Diss}) by considering the hysteresis loop between the charging and discharging paths (Figure A3 (a) and *Section 5.2*). An important feature of this technique is represented by the use of a purely sinusoidal excitation, which avoids the use of signals containing higher frequency harmonics (e.g. square waves). This allows to accurately characterize the DUTs inside the cryogenic chamber at frequencies in the range of several hundreds of kHz despite the long interconnections required in such measurement.

The value of E_{Diss} as a function of temperature for four DUTs is shown in Figure A3 (b), where different trends can be observed. While T1 shows quite independent behavior in temperature, T3 presents about a 30 % decrease in E_{Diss} at 4.2 K with respect to the RT value. T2 displays, instead, a significant increase of more than 70 % of the RT value. Finally, T4 exhibits relatively small E_{Diss} values, within the measurement setup accuracy (estimated to be ±5 nJ), and thus will not be considered. It should be noted that the variation of the soft-switching losses does not agree with any channel dependencies reported in Figure A2. This confirms the recently proposed theories [215], [216], [225] in which the causes of soft-switching losses are attributed to the GaN resistive buffer and the Si substrate, rather than to the channel properties or the presence of stray charges (as for Super Junction Si devices). The consistent E_{Diss} increase for T2 may be due to the more efficient electron trapping in the GaN buffer at low temperatures [216]. However, the different behavior among the DUTs suggests that such mechanisms strongly depend on the exact energy level of the trapping sites. Since each manufacturer typically employs a custom epi-structure, the switching loss values and temperature behavior are expected to vary significantly according to the exact GaN buffer composition and Si substrate choice. It is however possible to safely assume that soft-switching losses present a weaker temperature dependence with respect to conduction losses.

Hard-switching losses occur when a transistor is switched on while it still holds a large voltage at its drain-to-source terminals. Standard methods to evaluate these losses are based on a double-pulse test (DPT) circuit [165], [166]. Nevertheless, such a technique is very challenging at cryogenic temperatures due to the long wiring required to connect the device inside the cryogenic chamber [79], which has a significant impact on the measurement accuracy. It is however possible to draw important conclusions on the temperature behavior of hard-switching losses by exploiting the presented results, without the use of a DPT measurement.

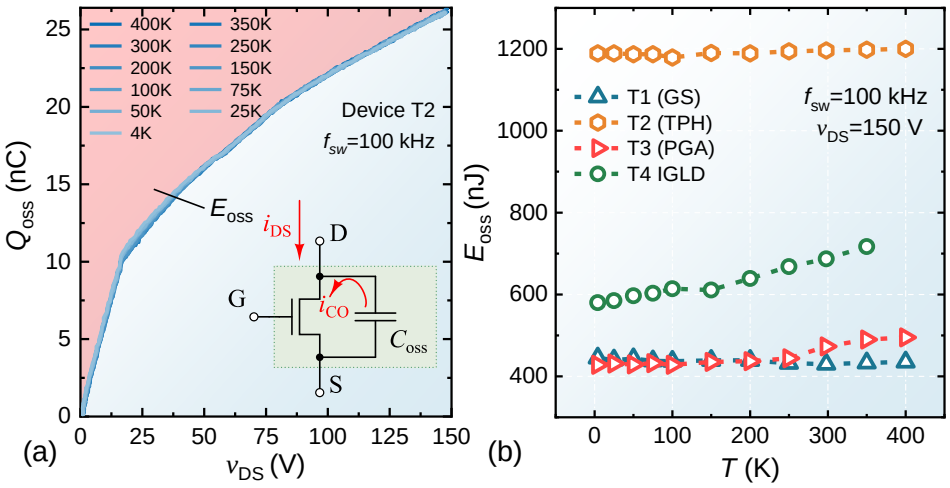


Figure A4: (a) E_{oss} extraction from the Q_{oss} versus v_{DS} characteristic. In the bottom right inset, the circuit schematic of a device under hard-switching operation is shown. (b) E_{oss} as a function of temperature for the four DUTs.

While hard-switching losses comprise a turn-on and turn-off loss term, turn-off losses can typically be neglected for GaN devices due to their large transconductance and *dv/dt* capability [167], [168]. The main hard-switching losses contribution is thus represented by turn-on losses, which can be expressed as a sum of two terms [165], [166]:

$$P_{\mathrm{SW,hard}} = f \times E_{\mathrm{oss}} + P_{\mathrm{VI}}(g_{\mathrm{m}}) \qquad \text{A1}$$

where f is the switching frequency, E_{oss} is the energy stored in the transistor output capacitance at a certain off-state v_{DS} value (Figure A4 (a)) and P_{VI} is the loss term associated with the external load current flowing from the circuit through the device channel during the discharging of C_{oss}. Figure A4 (a) shows the extraction of the device E_{oss} values for different temperatures, obtained from the integration of the transistor Q_{oss} versus v_{DS} curve. A comparison of E_{oss} as a function of temperature for the four DUTs is shown in Figure A4 (b). T1 and T2 present a very constant E_{oss} value throughout the whole temperature range, which is in agreement with the temperature-independent behavior of the 2DEG concentration. On the other hand, T3 and T4 show a mild E_{oss} decrease to about 90 % of the RT value at 4.2 K. The contribution of E_{oss} to hard-switching losses is thus quite constant in a wide temperature range. On the other hand, the second term in (eq. A1), P_{VI}, is proportional to the external load current and is linked to the time required to discharge C_{oss} through the device channel by the current i_{CO} (inset in Figure A4 (a)). The discharging time, if not entirely controlled by an external gate resistor, depends on device trans-conductance g_m, which increases significantly with decreasing temperature [165] due to its linear dependence on the carrier mobility (Figure A2 (c-d)). Hence, while the E_{oss} contribution is fairly independent of temperature, the value of the P_{VI} term could decrease considerably at cryogenic conditions with a behavior similar to what is shown in Figure A2 (d). Hard-switching losses thus decrease at low temperatures with a reduction becoming more pronounced as the load current increases.

Overall, some important trends in the different losses contributions at cryogenic temperatures can be identified (Table A2). Conduction losses show the most significant decrease, which is larger (~6x) for conventional HEMT technologies (T1 and T2) with respect to the GIT devices (~2x). Soft-switching losses present a weaker temperature dependence without any common trend between the different technologies. For hard-switching losses, while the E_{oss} component demonstrated to be temperature

insensitive, the total loss value decreases due to the enhanced device g_m. Thus, while the precise improvement depends on the circuit operation, GaN power devices show much-enhanced efficiency at cryogenic temperatures.

Index	$R_{ON,RT}$ [mΩ]	$R_{ON,4K}$/ $R_{ON,RT}$	$E_{Diss,RT}$ [nJ]	$E_{Diss,4K}$/ $E_{Diss,RT}$	$E_{oss,RT}$ [nJ]	$E_{oss,4K}$ / $E_{oss,RT}$
T1	200	0.14	27	1	430	1
T2	150	0.15	42	1.73	1196	1
T3	140	0.66	35	0.76	473	0.9
T4	140	0.54	-	-	687	0.85

Table A2: Comparison of R_{ON}, E_{Diss}, and E_{oss} at 300 K and 4.2 K for the DUTs.

In this section, we characterized and compared the performance of the most common GaN commercial power devices in a wide temperature range between 400 K and 4.2 K. All of the tested devices can successfully operate at cryogenic temperature with an overall performance improvement. However, the different GaN HEMT technologies lead to significant variations in the device gate control and loss mechanisms, which have been explained according to the device structure. The presented results prove the promising potential of the GaN technology for low-temperature applications and provide the circuit designers with precious insights to maximize converters' efficiency in such conditions.

B Thermal Performance of Embedded Microchannel Cooling

While a detailed investigation of the thermal performance of embedded microchannel cooling is not the main goal of this thesis, this appendix aims to give an overview of this topic to better understand the results presented in *Chapter 5*.

In order to understand the advantages of embedded microchannel liquid cooling with respect to more conventional liquid cooling techniques, it is important to analyze the different contributions to the thermal resistance in the two structures. Figure B1 highlights all thermal resistance contributions for a device cooled with conventional or indirect liquid cooling (e.g. using a cold plate) and with embedded liquid cooling using microchannels. In indirect cooling, the heat is extracted by contacting a cold plate to the packaged device and using a thermal interface material (TIM) to reduce the thermal resistance due to the interface. The heat thus travels from the heat source through the Si substrate to the package, it then crosses the TIM and spreads in the cold plate, where is transferred by convection to the coolant.

This kind of approach comes with the drawback of additional thermal resistance due to the interface between the die and the cold plate (R_{TIM}) and the junction-to-case thermal resistance ($R_{j\text{-}c}$) due to the device package. These two components of thermal resistance can be seen as fixed values, independent of the design of the cold plate structure. As a result, this defines an upper limit to the maximum power that can be extracted from the device. When R_{TIM} and $R_{j\text{-}c}$ are the dominant values in the total thermal resistance, optimization of the other contributions, such as the cold plate, will yield a diminishing reduction in the junction temperature. The exact values of R_{TIM} and $R_{j\text{-}c}$ highly depend on the specific cooling solution but they can be relevant in the case of high-performance cold plates. For instance, R_{TIM} varies considerably depending on the exact material and packaging solution adopted but typically adds about 0.5 cm^2k/W to total thermal resistance. $R_{j\text{-}c}$ can introduce an additional thermal resistance

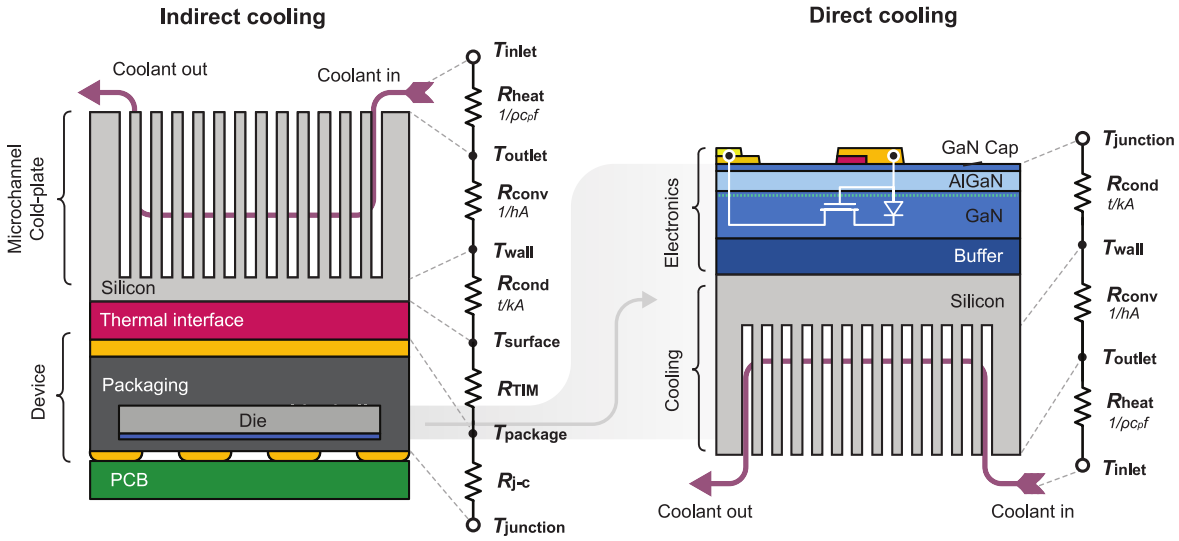


Figure B1: (a) Cross-section schematic of conventional indirect water cooling and (b) embedded microchannel liquid cooling highlighting the different thermal resistance contributions in the two structures [226].

contribution of about 0.1 cm^{2}k/W for a wafer-scale-chip-level packaging, around 0.2-0.3 cm^{2}k/W for an embedded component package, and up to 2-3 cm^{2}k/W for a conventional TO247 package. By using embedded microchannel cooling, these terms are completely eliminated.

In addition to these contributions, one needs to consider the thermal resistance terms that are common between the two structures (Figure B2). In particular, there are three factors to consider:

1. The conduction term through the Si substrate:

$$R_{\text{cond}} = \frac{t_{\text{Si}}}{k_{\text{Si}} A_{\text{chip}}}$$

where t_{Si} is the thickness of the remaining Si layer, k_{Si} is the silicon thermal conductivity, and A_{chip} is the area of the chip.

2. The convection term linked to the heat transfer from the silicon substrate to the coolant:

$$R_{\text{conv}} = \frac{1}{hA_{\text{surf}}} = \frac{w_c/2}{Nu \text{ x } k \text{ x } A_{\text{surf}}}$$

where h is the heat transfer coefficient, w_c is the width of the channel or pipe through which the coolant is flown, Nu is the Nusselt number, k is the thermal conductivity of the coolant and A_{surf} is the surface through which convective heat transfer to the coolant can occur.

3. Lastly, the term linked to the coolant heat capacity:

$$R_{\text{heat}} = \frac{1}{\rho c_{\text{p}} f}$$

where ρ is the density, c_{p} is the specific heat of the fluid, and f is the flow rate.

The conduction term link to the heat conduction through the Si substrate is typically small. Indeed, if we consider the case shown in this work (t_{si} = 50 µm, k_{Si} = 1.5 W/cm·k, and A_{chip} 2.4 mm x 4 mm), the R_{cond} contribution is 0.03 k/W, compared to a total thermal resistance of 1.6 k/W. With respect to a 500

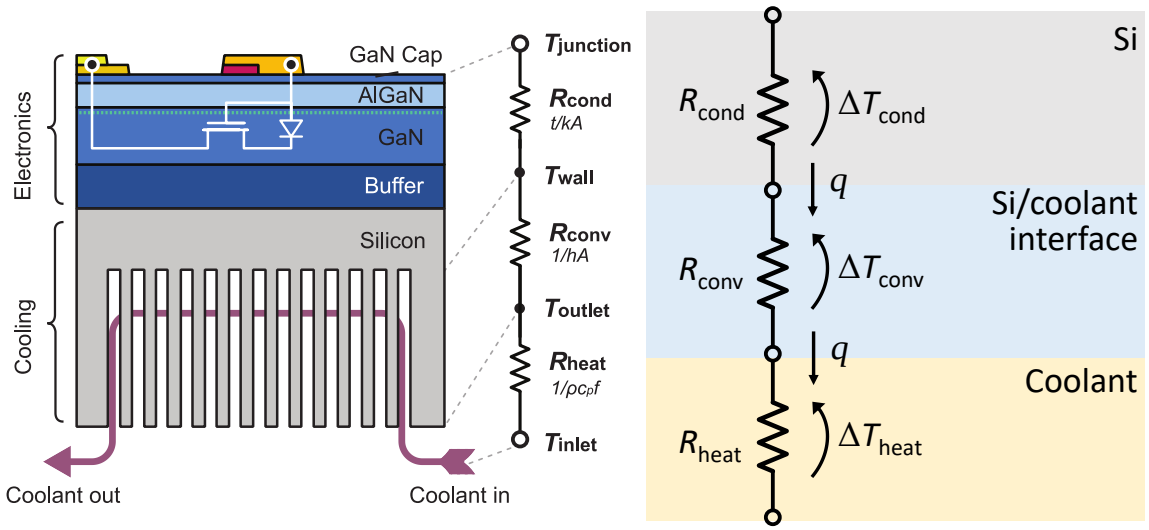


Figure B2: Schematic of the different thermal resistance contributions in the structure with embedded liquid cooling.

µm-thick Si substrate, the decrease in the conduction thermal resistance through the silicon layer is ~ 0.27 k/W. This also means that the thickness of the remaining Si substrate does not influence significantly the overall R_{th}. The R_{heat} contribution mainly depends on the type of coolant used and the flow rate. Thus, no significant difference is expected between the two techniques.

Finally, we have to consider the convection term. Indeed, the main goal of embedded liquid cooling is to significantly decrease the convection term by acting on two main aspects:

1. In the case of micro-channel cooling, the surface through which convection heat transfer occurs (A_{surf}) is much larger than the area of the chip, i.e. $A_{surf} > A_{chip}$, which is one of the main advantages of this cooling technique with respect to conventional liquid. This can be easily understood considering the 3D topology of the microchannels (Figure B3 (a)) since not only the top surface of the microchannel can exchange heat but also its sidewalls. Considering the geometry of the microchannels, we can define a parameter

$$\alpha = \frac{A_{\text{surf}}}{A_{chip}} = \frac{w_c + 2z}{w_c + w_w}$$

where w_w is the spacing between the microchannels and z is the height of the microchannels (Figure B3 (a)). As the channel width reduces, the surface available for the heat exchange increases greatly, as shown by the sharp growth of α (Figure B3 (b)). This mechanism significantly increases the effective heat transfer and reduces the convective thermal resistance for devices with embedded liquid cooling. For instance, considering the channel dimensions used in this work A_{surf} = 7.1 x A_{chip}. This means that the heat has a surface 7 times larger than the area of the chip to cross the Si/coolant interface and be removed by the coolant.

2. The use of narrow microchannels significantly reduces w_c compared to conventional liquid cooling, which significantly increases the heat transfer coefficient. For instance, w_c in the case of conventional liquid cooling is large (in the order of centimeters) and A_{surf} is rather small due to the large pipe diameter and spacing between the pipe turns, which result in a small surface through which the heat can be exchanged (Figure B4 (a)). Advanced cold plates can result in significantly reduced thermal resistance by employing instead a smaller channel diameter down

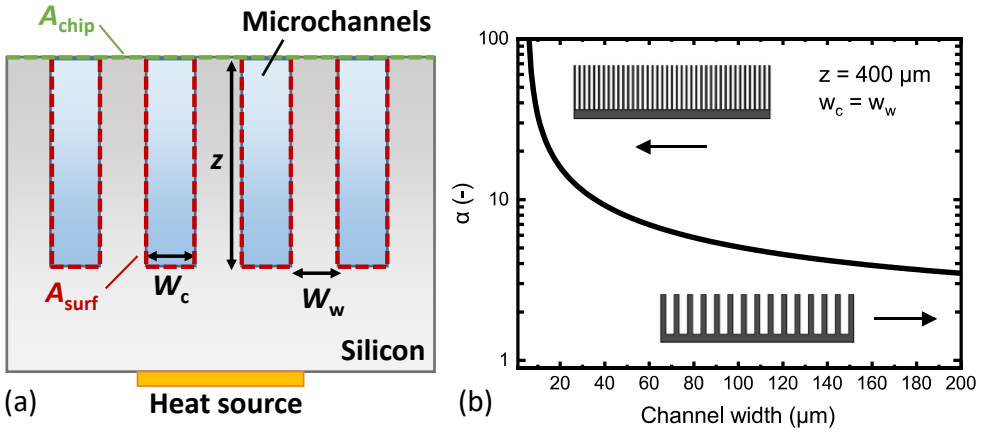


Figure B3: Microchannels cross-section showing the heat-exchange surface between Si and the coolant. (b) Ratio between A_{surf} and A_{chip} as a function of the channel width.

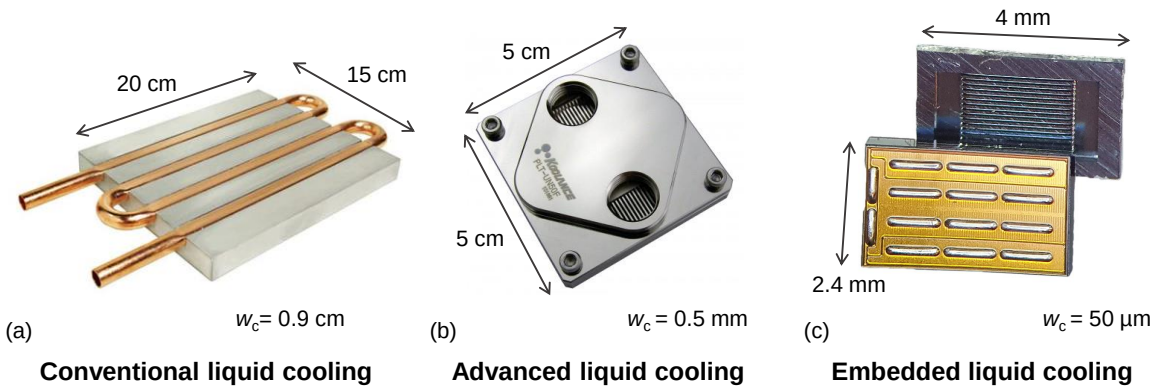


Figure B4: (a) Picture of a conventional liquid cooling solution, (b) of an advanced cold plate with channel dimension of 0.5 mm, and (c) of the investigated DUT with embedded liquid cooling. w_c is the dimension of the channel through which the coolant is flown. The images for the conventional liquid cooling and the advanced liquid cooling have been obtained from [227], [228], respectively.

to ~ 500 µm (Figure B4 (b)). In this case, w_c reduces considerably as well as the surface available for heat transfer. In the presented device with embedded liquid cooling, the channel diameter is reduced to 50 µm, which yields a 10x decrease in w_c (Figure B4 (c)).

Thanks to these mechanisms, embedded liquid cooling enables a significant reduction of the convection term of the thermal resistance (R_{conv}) compared to other more conventional liquid cooling techniques, as shown in Table B1. In addition to the strong reduction in R_{conv}, embedded liquid cooling leads to the complete elimination of any contributions due to the thermal interface material and the package, as previously explained, which are instead present both for conventional and advanced indirect liquid cooling strategies, as is shown in Figure B5 (a).

In order to further compare embedded liquid cooling with commercially available advanced liquid cooling solutions, we can consider a benchmark of the coefficient of performance versus the heat flux that can be extracted. The coefficient of performance (COP) is defined as the ratio of the power that can be extracted divided by the pumping power to drive the coolant through the chip. The higher the COP, the more efficient the heat extraction from the chip is. From Figure B5 (b), one can notice that embedded liquid cooling represents a significant advance with respect to typical commercially available advanced liquid cooling solutions as it enables extracting larger heat fluxes while maintaining excellent COP.

In addition to the improved thermal performance, embedded liquid cooling has a very promising potential also from the cost point of view. In particular, the etching of the microchannels in the device's backside relies on a simple wafer-scale post-processing method that enables the fabrication of the

	Conventional liquid cooling	Advanced liquid cooling	Embedded liquid cooling
R_{conv} (cm^2 k/W)	1.95	0.76	0.1

Table B1. R_{conv} comparison for the three presented methods. The data for the conventional liquid cooling and the advanced liquid cooling has been obtained from [227], [228], respectively.

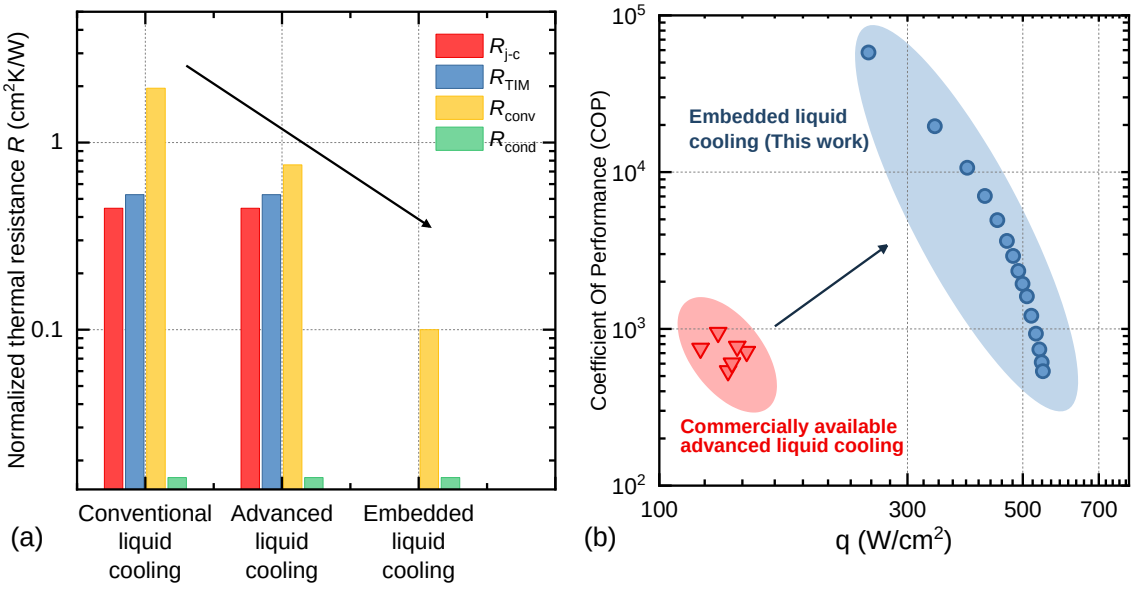


Figure B5: (a) Comparison (from measured data) of the different thermal resistance contributions for conventional, advanced, and embedded liquid cooling. (b) Coefficient of performance (COP) versus heat flux (q) that can be extracted for commercially available advanced liquid cooling solutions and the present embedded liquid cooling [226].

embedded heat sink in the device substrate for all the chips in the full wafer at the same time and thus can achieve high volume production and be very low-cost.

The added cost of the deep reactive ion etching (DRIE) step per chip can be very low when considering standard 8-inch GaN-on-Si wafers and it is expected to remain well below 0.50 USD per chip, making it highly cost-effective [229]. For instance, even in our university facility, the cost per chip of the DRIE step (including the lithography) when considering a 4-inch wafer and the device size of the DUT is about 0.20 USD per chip. In addition, the top sealing cap can be manufactured using injection molding for a unit price well below 1 USD, when sufficiently large volumes are requested.

For instance, in comparison, the heat sink used as a reference with forced air cooling is sold for 8.00 USD, which shows the potential of the proposed method to be very cost-effective with respect to convection air cooling. Also if we consider the conventional and advanced indirect liquid cooling techniques reported in Table B1 and Figure B4, it is clear that the proposed method is very competitive in terms of cost per performance (Figure B6). A much-reduced price per Watts of extracted heat is achieved compared to conventional liquid cooling and an improved price/performance can also be obtained compared to more advanced liquid cooling approaches. Besides, further cost reduction is expected with the future increase of the GaN-on-Si wafer size and the mass production of this solution.

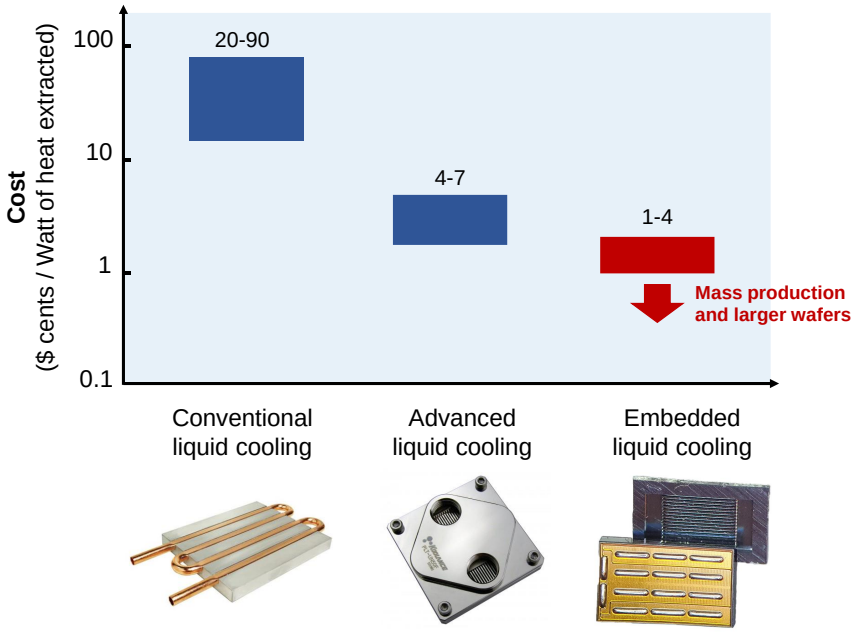


Figure B6: (a) Comparison of the cost per Watt of extracted heat for different cooling methods. A temperature rise of 60 °C has been considered. The data for conventional liquid cooling and advanced liquid cooling has been extracted from [227], [228], respectively. The data for embedded liquid cooling is based on measured data and the above analysis.

C Detailed Fabrication Process of GaN Lateral Devices

The fabrication of the devices reported in this thesis was performed in the Center of Micronanotechnology (CMi) and the IPHYS cleanroom at EPFL. Here below, the detailed fabrication process flow is presented.

Step	Description	Process
01	Wafer Dicing	Substrate: GaN-on-Si or GaN-on-Sapphire PR Coating before dicing to protect the surface Dicing from the top Standard chip size: 2 cm x 1.8 cm Remove PR after dicing with REM1165
02	Alignment marks definition	**Photolithography** Resist: AZ1512 (positive) Coating 6000 rpm Bake 1'30'' at 100 ºC (108°C set on the hotplate in Z13) Dose: 42, Defocus: 0, Laser: 405 nm Development: 35'' in AZ-726MIF 30'' O_2 plasma descum **ICP dry etching** Etchant: Ar/Cl2 (recipe gan_slo in STS in Z2) Etching depth: 500 nm (ER ~ 1.9 nm/s) PR removal in REM1165
03	Mesa and Nanowire definition	**Electron Beam Lithography** 5' in O2 plasma at 600 W for cleaning and HSQ adhesion Resist: HSQ 2% Coating: 2000 rpm – 6000 rpm depending on the desired resolution and etching depth Dose: 1650, beta = 12, eta = 1.5

		Development: 2’ 15’’ in TMAH 25 % *For high-resolution features (<~20 nm) separate exposures for large pads and nanowires* 5’ in O_2 plasma at 600 W to harden the HSQ **ICP dry etching** Etchant: Ar/Cl2 (recipe gan_slo in STS in Z2) Etching depth: 200-500 nm depending on the heterostructure
04	2nd mesa definition for isolation	**Photolithography** Resist: nLOF 2020 (negative) Coating 6000 rpm Bake 1’15’’ at 118 ºC (110°C set on the hotplate in Z13) Dose: 42, Defocus: 0, Laser: 375 nm Post-exposure bake 1’15’’ at 118 ºC (110°C set on the hotplate in Z13) Development: 45’’ in AZ-726MIF 30’’ O_2 plasma descum **ICP dry etching** Etchant: Ar/Cl2 (recipe gan_slo in STS in Z2) Etching depth: 350 nm PR removal in REM1165 + 5’ O_2 cleaning
05	Cycled treatment to reduce sidewalls damages	1’ in 600 W O_2 plasma 1’ in HCl 37% Repeat 4 times
06	HSQ stripping	5’ in BOE 7:1
07	LPCVD Si_3N_4 deposition (for multi-channel passivated devices)	2 nm SiO_2 oxide by ALD as interlayer RCA without HF + Piranha cleaning 100 nm Si_3N_4 by LPCVD
08	Passivation layer definition (for multi-channel passivated devices)	**Electron Beam Lithography** PR PMMA double layer 1st layer: PMMA-495-A8

		Coating: 7000 rpm for 1’ Baking at 180 °C for 7’30’’ Cooling 2nd layer: PMMA-495-A4 Coating: 4500 rpm for 1’ Baking at 180 °C for 7’30’’ Cooling Dose: 825, beta = 24 , eta = 0.6 Development 3’ in MiBK:IPA 1:3 + 1’ in IPA **Hard Mask evaporation and lift-off** Metal: Cr/Au/Cr/Au Thickness: 20/100/20/100 nm Lift-off: in 1165 @ 80 ºC **Si_3N_4 etching** RIE etching (ICMP) Recipe SiN_std at 30W (ER 10nm/min) Wet etching of Au (3’) and Cr (1’) to remove the hard mask
09	Ohmic contact formation	**Photolithography** Double PR layer Resist: LOR 5A (positive) Coating 3000 rpm Bake 4’10’’ at 170 ºC (184°C set on the hotplate in Z13) Resist: AZ1512 (positive) Coating 3000 rpm Bake 1’30’’ at 100 ºC (108°C set on the hotplate in Z13) Dose: 42, Defocus: -2, Laser: 405 nm Development: 1’05’’ in AZ-726MIF 30’’ O_2 plasma descum **Ohmic metal evaporation and lift-off** Metal: Ti/Al/Ti/Ni/Au Thickness: 20/120/40/60/50 nm Lift-off: in 1165 @ 80 ºC Annealing at 780 ºC for 30’’

10	Gate Oxide deposition	Atomic layer deposition (ALD in Z4) Conditioning of the chamber: ~25 nm SiO_2 dummy runs SiO_2 25 nm @ 300 ºC
11	Definition of the oxide layer	**Photolithography** Resist: AZ1512 (positive) HDMS treatment for adhesion Coating 6000 rpm Bake 1'30'' at 100 ºC (108°C set on the hotplate in Z13) Dose: 42, Defocus: 0, Laser: 405 nm Development: 35'' in AZ-726MIF 30'' O_2 plasma descum **Wet Etching** Wet etching 1' in HF 1% Etch rate ~ 0.66 nm/s PR removal in REM1165 + 30' O_2 cleaning to remove HDMS
12	Gate/Anode electrode definition	**Electron Beam Lithography** PR PMMA double layer 1st layer: PMMA-495-A8 Coating: 7000 rpm for 1' Baking at 180 °C for 7'30'' Cooling 2nd layer: PMMA-495-A4 Coating: 4500 rpm for 1' Baking at 180 °C for 7'30'' Cooling Dose: 825, beta = 24 , eta = 0.6 Development 3' in MiBK:IPA 1:3 + 1' in IPA **Gate metal evaporation and lift-off** Metal: Ni/Au or Ni/Pt/Au Thickness: 50/120 nm or 0.5/50/120 nm Lift-off: in 1165 @ 80 ºC

13	Definition of the micro-channels on the backside (only for embedded micro-channel cooling)	**Photolithography** Resist: nLOF2070 (negative) Coating 1000 rpm Bake 1'30'' at 100 ºC (108°C set on the hotplate in Z13) Dose: 220, Defocus: 0, Laser: 375 nm Post-exposure bake 1'30'' at 115 ºC (123°C set on the hotplate in Z13) Development: 2'50'' in AZ-726MIF 30'' O_2 plasma descum Mounting on a carrier wafer with 2 µm thermal oxide on top (to protect it from etching) **DRIE etching** SOI accurate ++++ for 1h and 20 min, etching depth ~ 500 µm Release and PR removal in acetone
14	Dicing (for scaled-up devices)	PR Coating before dicing to protect the surface Dicing from the top Remove PR after dicing with REM1165
15	Wire bonding (for scaled-up devices)	Sticking to a PCB using Silver paste Bake to harden to silver paste Wire bonding with Au 25 µm wire Glob-top if necessary

D Principles and Simulation of Intrinsic Polarization Super Junctions

D.1 Concept and Operating Principles of Polarization Super Junctions

To understand why charge balance is important and how it is achieved, it is instructive to start by considering a conventional doped semiconductor arranged in a Schottky diode configuration (the exact same conclusions hold for the drift region of a transistor too) (Figure D1 (a)). In such a device, dopant impurities are introduced in the crystal to increase its carrier density with respect to the material's intrinsic concentration. Donor dopant impurities ionize and result in mobile electrons, which can be displaced by an electric field, and in fixed charges, which are instead not mobile. At equilibrium (considering the depletion due to the built-in potential negligible for simplicity) charge neutrality needs to be satisfied and for each vertical cut at a certain x coordinate (Figure D1 (a)) the concentration of electrons is equal to that of ionized impurities, resulting in a zero net charge Q_{NET}. As a reverse voltage V_{CA} is applied in the off-state, mobile electrons tend to move to the cathode, resulting in an electron-depleted region at the anode edge (Figure D1 (b)). Ionized donors are instead not mobile and thus remain fixed at their position. Hence a certain uncompensated net charge is left in the depleted region, which results (in the simple case of uniform doping) in a linearly increasing electric field due to the Poisson equation $\nabla \cdot E = Q/\varepsilon$. Hence, the origin of this non-constant electric field is the presence of a net charge in the depleted region, which originates from the fact that electrons are mobile while the source of these electrons (the ionized donors) are not.

If we consider now HEMTs, the first step to determine their depletion behavior is to identify the source of the electrons in the 2DEG (Figure D1 (c)). This is a key point that is often neglected but is fundamental for any off-state analysis. Indeed, electrons in the 2DEG need to originate from some source that, in order to satisfy charge neutrality at equilibrium, has to carry the same charge with the opposite sign. In conventional AlGaN/GaN HEMTs with no or thin GaN cap, no 2DHG can be formed at the top AlGaN interface and it is widely accepted that surface donor states at the top interface are the source of the 2DEG (see Refs. [42], [55], [56], [151]). It should be noted that these states are not just a result of surface contamination or device processing but they intrinsically originate due to the presence of a crystal surface termination. These donor states ionize, thus becoming positively charged, and provide electrons to the 2DEG. At equilibrium, the 2DEG concentration equals that of ionized surface donor states, resulting in charge neutrality. This situation is very similar to one presented before for a simple doped semiconductor. In the off-state, mobile electrons are evacuated through the cathode while ionized donor states are not mobile and thus are fixed in their position (Figure D1 (d)). This results in the formation of a net charge in the depletion region, which is equal to the density of ionized surface donor states and thus to the N_s value. The net charge in the depletion region determines the off-state electric field profile similarly as in conventional doped semiconductors with the only difference of the two-dimensional device architecture, which affects the exact shape of the field.

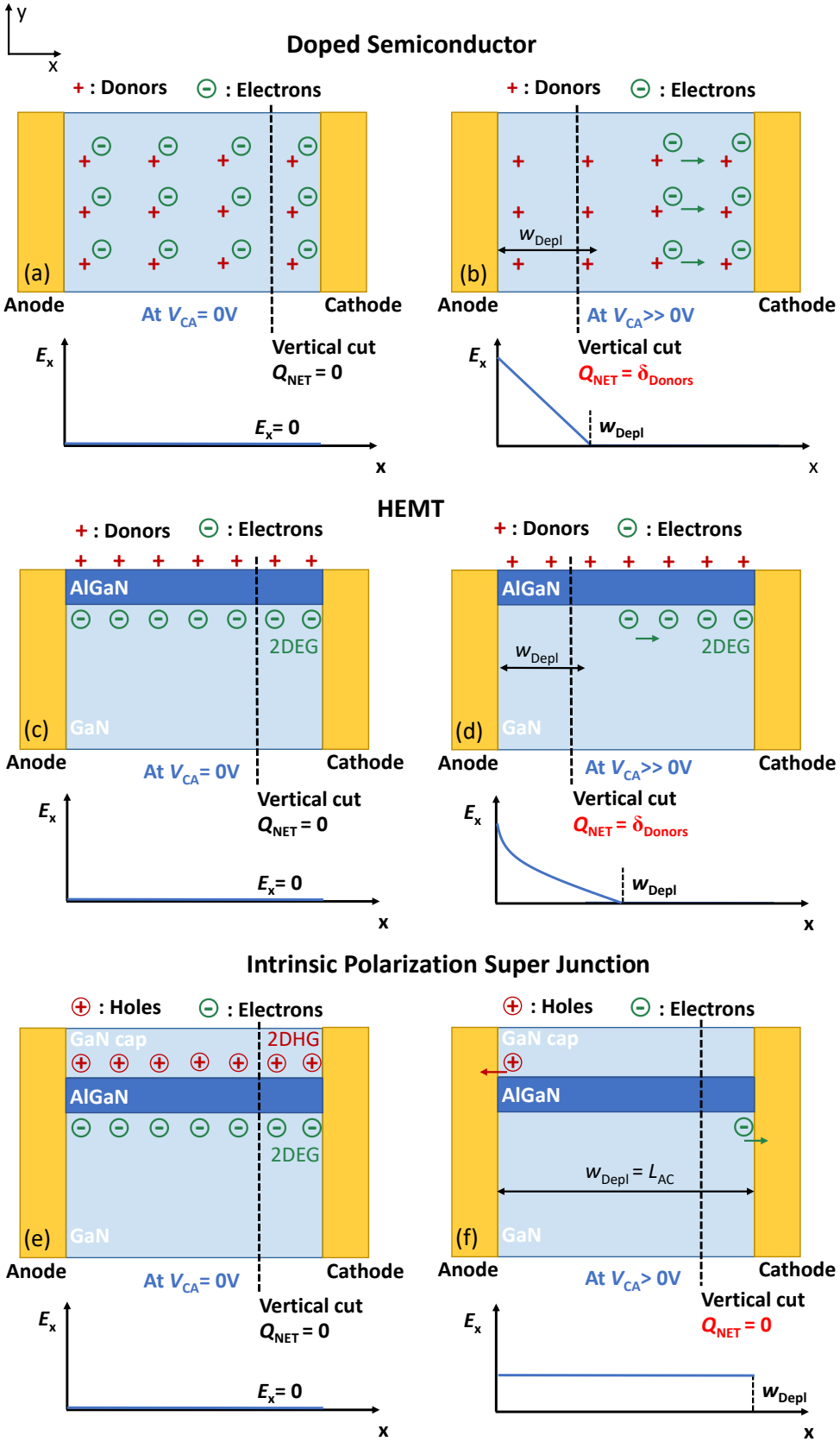


Figure D1: Charge distribution and electric field at equilibrium and in the off-state for a Schottky diode based on (a-b) a conventional doped semiconductor, (c-d) a HEMT-like structure, and (e-f) an intrinsic polarization super junction. Circled charges are mobile while charges without any circle are fixed. The carrier depletion at the anode side due to the built-in potential has been considered negligible for simplicity.

The key mechanism of the proposed intrinsic polarization super junction device is to replace the source of the 2DEG with mobile carriers rather than fixed charges (Figure D1 (e)). This allows depleting both the electrons and their source in the off-state. The introduction of a thick GaN cap enables achieving a 2DHG at the GaN/AlGaN interface, which provides the source of the electrons in the 2DEG (Figure D2 and [55], [56], [151]). In this way, no surface donor state is ionized and electrons in the 2DEG are entirely generated by holes in the 2DHG. At equilibrium, charge conservation is guaranteed by having an equal concentration of hole in the 2DHG and electrons in the 2DEG, respectively. In the off-state, mobile electrons are depleted through the cathode and mobile holes are evacuated through the anode, which results in a neutral depletion region with no net charge left and thus in an ideal flat electric field profile (Figure D1 (f)). The key concept of the proposed devices is that both holes and electrons are mobile charges that can be depleted in the off-state while no fixed ionized donor state is required to form the 2DEG.

For these reasons, the charge mismatch parameter $\Delta=\delta_{Donors}=N_s-P_s$ is considered since it effectively indicates how much of the electron concentration (N_s) originates from mobile holes (P_s) and what is the amount of ionized surface donor states (δ_{Donor}) that act as fixed net charges and influence the off-state electric field (Figure D2).

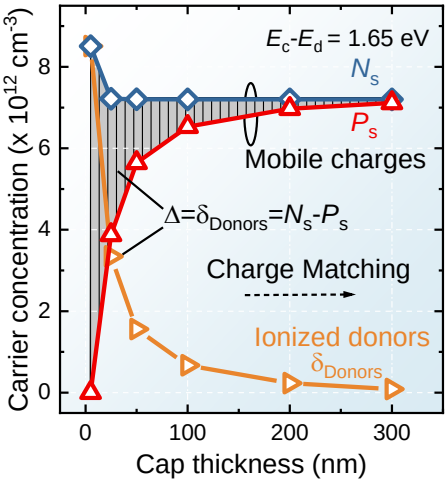


Figure D2: N_s, P_s, and ionized surface donors as a function of the GaN cap thickness. The grey area is the difference N_s- P_s=Δ that represents the fixed net charge in the depletion region. This corresponds to the orange curve i.e. the density of ionized surface donor states.

D.2 Comparison with Devices with *p*-GaN Cap

The use of an intrinsic GaN cap presents several advantages compared to previously proposed PSJ devices with a *p*-GaN cap, for which charge balancing is extremely challenging.

1. The fact that in a GaN/AlGaN/GaN heterostructure the net sum of the polarization charges for a certain cross-section (along the c-axis) is null ensures P_s and N_s of equal concentration in intrinsic structures, provided that a proper strategy is employed to avoid the ionization of surface states. The introduction of *p*-type dopant impurities alters this natural balance. In this case, the density of the 2DHG is determined by the amount of activated *p*-type dopants since activated dopants generate holes that are swept by the polarization field in the 2DHG. Thus, to ensure a proper matching between N_s and P_s, the *p*-GaN cap thickness, doping level, and doping activation need to be precisely controlled and determined. For instance, a too thick barrier would result in an excess of holes and thus in a significant carrier mismatch (Figure D3 (a)). In a similar way, a variation of the exact dopant concentration or activation ratio can also lead to a large mismatch (Figure D3 (b)). However, precise control of these parameters is very challenging due to the inefficient Mg activation and to its thermal back diffusion during the growth [146], [147]. This results in a very difficult estimation of the number of activated dopants introduced in the structure, which leads to a significant carrier mismatch. Thus, in heterostructures with a *p*-GaN cap, the charge matching relies on the precise and very challenging control of the *p*-GaN doping while in the proposed structure with an intrinsic cap charge matching is naturally guaranteed as long as a thick cap is used to avoid the ionization of surface states. This results in a much more robust and straightforward solution.

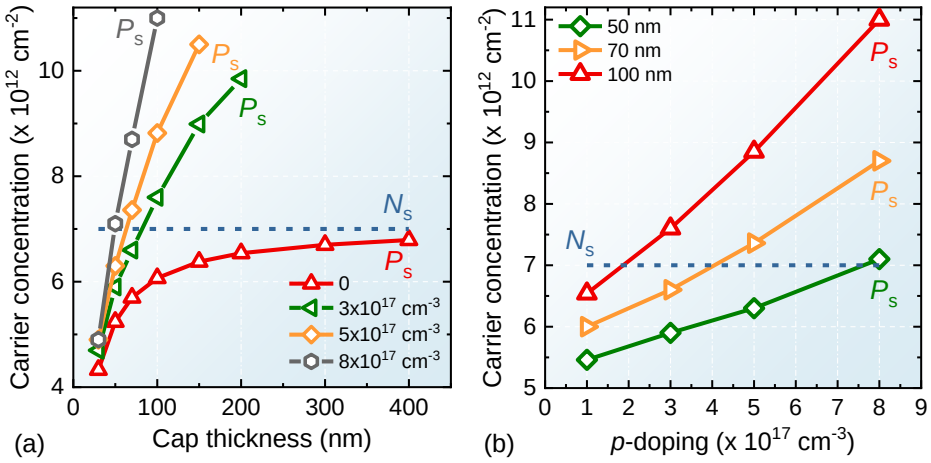


Figure D3: (a) Carrier concentration as a function of the GaN cap thickness for intrinsic and *p*-doped cap layers. (b) Carrier concentration as a function of the *p*-GaN cap doping for different cap thicknesses.

2. In addition, even provided that the cap thickness and doping activation are perfectly controlled and a proper charge matching is achieved, the reduced *p*-GaN cap thickness compared to the case of an intrinsic cap (Figure D3 (a)) results in a strong dependence on the exact energy distribution of the surface states. For instance, in the case of a 30 nm-thick *p*-GaN cap, as reported in Ref. [230], a significant dependence of the 2DHG density on the exact energy level of the surface

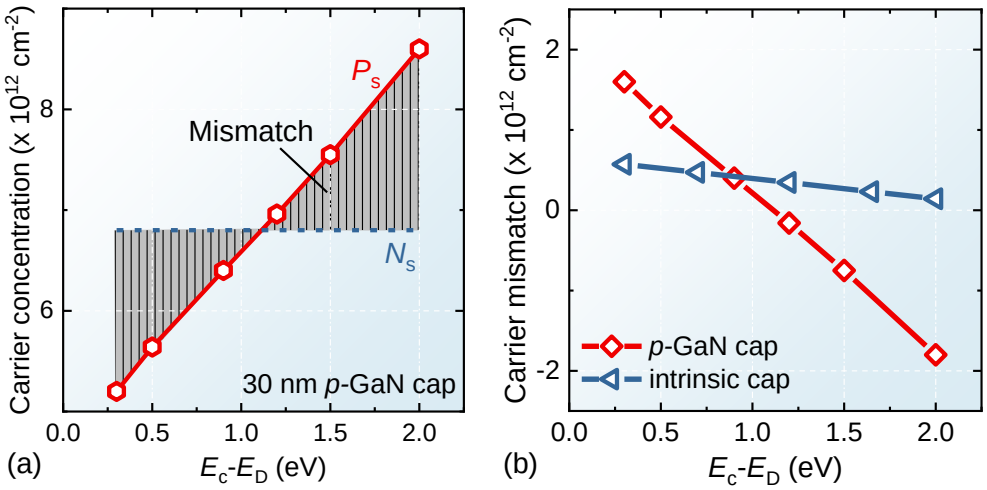


Figure D4: (a) Carrier concentration as a function of the surface donors energy level for the structure with a *p*-GaN cap shown in Ref. [230] (b) Influence of the energy level of the surface donors on the mismatch for a structure with a *p*-GaN cap [230] and an intrinsic GaN cap, as here proposed.

states is present (Figure D4 (a)). The use of a thick intrinsic cap, as here proposed, is instead much more effective in significantly reducing this effect due to its large thickness (Figure D4). Thus, on top of the difficulties to precisely control the ionized dopant density, a large dependence on the exact surface conditions is present for the approach based on a *p*-GaN cap.

3. Finally, even if one could achieve proper charge matching precisely controlling the amount of ionized *p*-type dopants and the surface conditions, the Mg ionization ratio strongly depends on the temperature. In particular, the Mg ionization increases significantly (up to several times) in the range from room temperature (RT) to 150 °C, as shown in Refs. [146], [147], which is however the typical operating condition of a power device. This means that, even if minimized at RT, the carrier mismatch increases significantly when the device heats up during operation, resulting in degraded off-state performance.

The approach proposed in this work based on the use of an intrinsic GaN cap layer resolves all of these problems since relies on the presence of matching polarization charges rather than on the introduction of external dopants to achieve charge balance.

D.3 Contact to the 2DHG

When a PSJ device is switched from the ON state to the OFF state and vice-versa, electrons are depleted/injected through the drain/cathode electrode, which provides ohmic contact to the 2DEG, while holes are depleted/injected through the gate/anode electrode. While an ohmic contact between the drain/cathode electrode and the 2DEG is not problematic, particular care should be given to achieve proper contact to the 2DHG. This is required to effectively inject/deplete the holes in the 2DHG in a short time, without impacting the switching speed of the device. In particular, too large contact resistance would result in a long turn-on/off time, severely limiting the achievable switching frequency. A recent work on a similar structure has investigated in detail this phenomenon [139]. Based on their conclusions, the turn-on speed of the device is not affected as long as the contact resistance to the holes is below ~ 10^{-1} -10^{-2} Ω·cm^2. This range of contact resistance is achievable, considering that *p*-type ohmic contact resistivity ranging from 1 × 10^{-6} Ω·cm^2 to 1 × 10^{-4} Ω·cm^2 can be routinely obtained [231]. However, a proper design of the 2DHG contact should be implemented, especially in the case of an intrinsic GaN cap.

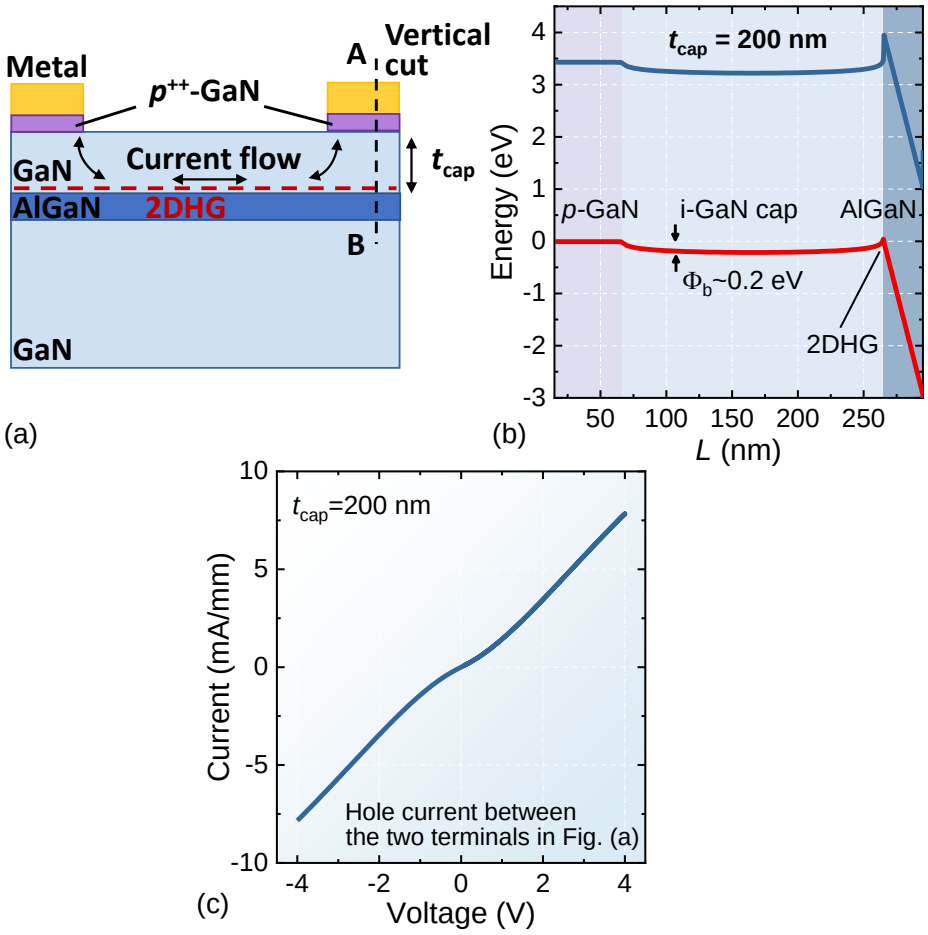


Figure D5: (a) Cross-section of the structure investigated to understand the top contact to the 2DHG (b) Bandstructure along the AB cut in Fig. for the cap employed in this work (200 nm). (c) Hole current between the two terminals in Fig. (a) as a function of the applied voltage.

In the device here presented (Figure 3.2.2 (a)), a p^{++}-GaN layer with a Ni/Au contact on top has been introduced to improve the contact to the 2DHG (Figure D5 (a)). This p^{++}-GaN layer can be either grown during the heterostructure epitaxy and then removed in the access region or realized by other techniques under development such as selective area regrowth [217]–[219] or ion implantation [232]–[234]. In this structure, the large-density 2DHG at the cap/AlGaN interface and the highly doped p^{++}-GaN contact layer at the top significantly lift the valence band close to the Fermi level and result only in a minor Schottky barrier (Figure D5 (b)). Thanks to this mechanism, good contact between the top p^{++}-GaN and the 2DHG can be established and a hole current can flow with a small Schottky barrier, as shown in Figure D5 (c) for the structure presented in Figure D5 (a).

D.4 TCAD Simulation for PSJ Devices

Here below is the source code that was adapted to simulate the different i-PSJ devices with Atlas Silvaco.

```
go atlas simflags="-P 12"
##### SET VARIABLES #####
# Distance Anode to Cathode
set Lac=10
# Cap Thickness
set Tcap=0.2
# Buffer Thickness
set Tbuf=0.5
# Background Doping
set uid=0
# Barrier Thickness
set Tb=0.030
# AlN Thickness
set Taln=0.0007
# Barrier Composition
set bcomp=0.25
# Barrier Doping
set n=0
# p-contact Doping
set pp=1e19
#Oxide thickness on the top and bottom of the structure
set oxbox=0.1
#contact length
set Lc=0.1
# Length of the hole contact
```

```
set Lpc=1
#contact height on top of the barrier
set Hc=$Tcap/2
#contact height on the bottom
set Hcb=$Tb+$Taln+0.4
#polarization scale (matching experimental data)
set psc=0.92
#Energy level of the donor surface states
set edonor=3.43-1.65

##### MESH DEFINITION #####

mesh width=1000

#Mesh on x direction
#left contact start
x.m l=-$Lc s=0.05
#left contact end
x.m l=0 s=0.005
#1/4 of the device
x.m l=$Lac/4 s=0.05
#middle of the device
x.m l=$Lac/2 s=0.1
#3/4 of the device
x.m l=3*$Lac/4 s=0.05
#right contact start
x.m l=$Lac s=0.005
#right contact end
x.m l=$Lac+$Lc s=0.05
```

```
#Mesh on y direction
#top of the structure
y.m l=-$Tcap-$oxbox s=0.02
#top of cap
y.m l=-$Tcap s=0.02
#middle of the cap
y.m l=-$Tcap/2 s=0.01
#top of barrier
y.m l=0 s=0.0005
#middle of barrier
y.m l=$Tb/2 s=0.002
#bottom of barrier
y.m l=$Tb s=0.0005
#bottom of AlN
y.m l=$Tb+$Taln s=0.0001
#2DEG region
y.m l=$Tb+$Taln+0.05 s=0.005
#bottom of buffer
y.m l=$Tb+$Taln+$Tbuf s=0.05
#bottom of the oxide box
#y.m l=$Tb+$Taln+$Tbuf+$oxbox s=1

##### REGION DEFINITION #####
#Insulator at the top of the Device
region num=1 mat=Air y.min=-$Tcap-$oxbox y.max=-$Tcap insulator
# GaN cap
region num=3 mat=GaN y.min=-$Tcap y.max=0 donors=$uid polar.scale = $psc
# AlGaN barrier
region num=4 mat=AlGaN x.comp=$bcomp y.min=0 y.max=$Tb donors=$n+$uid polar.scale = $psc
```

```
# AlN spacer

region num=8 mat=AlN y.min=$Tb y.max=$Tb+$Taln donors=$uid polar.scale = $psc

# Buffer Layer

region num=5 mat=GaN y.min=$Tb+$Taln y.max=$Tb+$Taln+$Tbuf donors=$uid polar.scale = $psc
substrate

#p++ top contact

region num=2 mat=GaN y.min=-$Tcap-$oxbox y.max=-$Tcap x.min=-$Lc x.max=$Lpc
acceptors=$pp polar.scale = $psc


#Anode Electrode

elec num=1 name=anode x.min=-$Lc x.max=0 y.min=-$Hc y.max=$Hcb

#Cathode Electrode

elec num=2 name=cathode x.min=$Lac x.max=$Lac+$Lc y.min=-$Hc y.max=$Hcb

#top p-GaN electrode (contact for Holes)

elec num=3 name=anode1 y.min=-$Tcap-$oxbox y.max=-$Tcap-$oxbox x.min=$Lpc-0.75
x.max=$Lpc-0.25


#Anode work-function

contact name=anode workfun=5.5

#Cathode work-function

contact name=cathode workfun=4.2

# Connection between the Anode and the contact for Holes

contact name=anode1 common=anode



#set material permittivity

material region=3 epsilon=10.1

material region=5 epsilon=10.1

material region=2 epsilon=10.1
```

```
material region=6 epsilon=10.1

material region=4 epsilon=9.7175

material region=8 epsilon=8.57


# Set Ionized Donor States in case of a charge unbalanced structure

#inttrap e.level=$edonor donor density=0.6e13 degen=1 sign=1e-16 sigp=1e-16 s.x y.min=-$Tcap y.max=-$Tcap x.min=0 x.max=$Lac


model ganfet


##### OUTPUT #####


output con.band val.band

solve init

save outf=Output_0V.str


solve name=anode vfinal=-1 vstep=-0.1

save outf= Output_1V.str


solve name=anode vfinal=-2 vstep=-0.25

save outf= Output_2V.str


solve name=anode vfinal=-3 vstep=-0.5

save outf= Output_3V.str


solve name=anode vfinal=-5 vstep=-1

save outf= Output_5V.str


solve name=anode vfinal=-10 vstep=-1

save outf= Output_10V.str
```

```
solve name=anode vfinal=-20 vstep=-2.5
save outf= Output_20V.str

solve name=anode vfinal=-50 vstep=-15
save outf= Output_50V.str

solve name=anode vfinal=-100 vstep=-25
save outf= Output_100V.str

solve name=anode vfinal=-200 vstep=-25
save outf= Output_200V.str

solve name=anode vfinal=-500 vstep=-50
save outf= Output_500V.str

solve name=anode vfinal=-3000 vstep=-100
save outf= Output_3000V.str
```

E Multi-Channel Nanowires Properties and Field Management

E.1 Uniformity and Interface Quality in Multi-Channel Nanowires

Achieving a good uniformity of the nanowire width along the vertical direction (c-axis) is of great importance to ensure the same threshold voltage for all of the embedded channels and achieve E-mode operation. Indeed, an enlargement of the nanowire width would result in a variation of V_{TH} for the bottom channels, preventing their simultaneous control and precluding E-mode operation. Yet, perfectly vertical sidewalls are very challenging to achieve by ICP etching, which typically results in a slanted profile. For the presented multi-channel nanowire, the process flow has been optimized by properly tuning the ICP power and employing an HSQ hard mask. This approach greatly improved the verticality of the achieved nanowires.

Nevertheless, a certain etching angle is still expected and its impact on the device performance needs to be considered. To this end, we monitored this phenomenon both by direct imaging and by considering

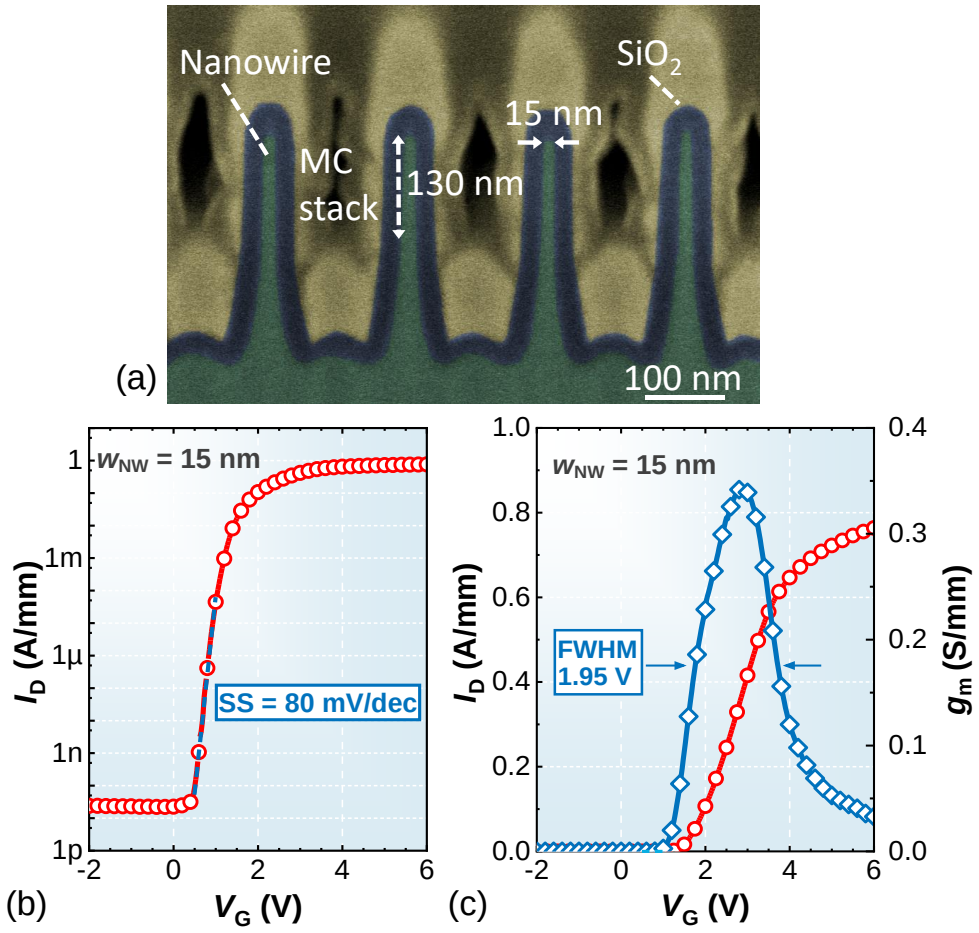


Figure E1: (a) FIB cross-section of the multi-channel nanowires (b) Transfer curve in logarithmic and (c) linear scale for E-mode multi-channel devices with a nanowire width of 15 nm.

the electric performance of the device. Figure E1 (a) shows the Focused Ion Beam (FIB) cross-section of 15-nm wide nanowires in the E-mode gate region. The nanowires are conformably covered by the 25 nm-thick ALD SiO_2 oxide and the gate metal. Vertical nanowire sidewalls can be observed in the region where the multi-channel heterostructure is present (the top 130 nm). The slight enlargement at the base does not affect in any way the device operation as no conducting channel is present there.

These hypotheses were confirmed by the transfer curve of the device. Indeed, a Subthreshold Slope (SS) of 80 mV/dec is measured at room temperature (Figure E1 (b)), and a transconductance (g_m) with a sharp peak of 350 mS/mm and a narrow FWHM of 1.95 V is observed (Figure E1 (c)). The small SS and g_m FWHM indicate excellent width uniformity between the different channels as any significant enlargement of the bottom channel widths would have resulted in a degraded SS and a broad g_m.

In addition to the good uniformity of the nanowire width, the nanowire sidewalls need to be smooth and present a high-quality interface since any interface roughness would degrade the carrier mobility. To determine the interface properties of the multi-channel nanowires, a high-resolution TEM cross-section of the GaN/SiO_2 region was taken (Figure E2). The TEM image shows a smooth surface with no evident roughness above ~ 1 nm. The good quality of the multi-channel nanowires interface was confirmed by the excellent carrier mobility down to very small widths, which is reported in Figure 2.3.9.

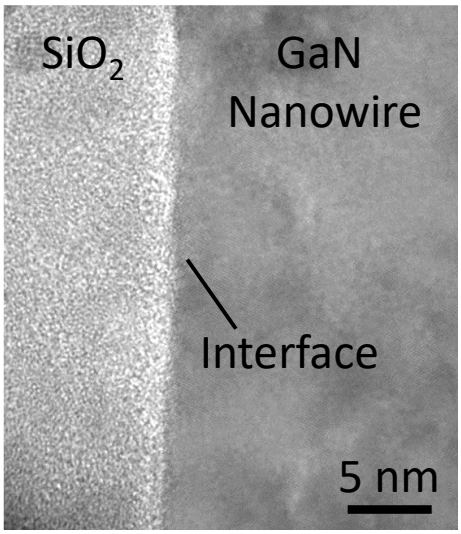


Figure E2: TEM cross-section showing the interface between the multi-channel nanowire and the ALD SiO_2 gate oxide.

E.2 Multi-Channel Nanowires for Improved Field Management

As presented in *Section 2.3.5*, conventional planar field plates (Figure E3 (a)) are not effective in managing the off-state field in highly conducting multi-channel devices. This is because a planar electrode is not able to deplete all of the embedded channels due to the large distance between the metal and the bottom channels and the electric field shielding from the upper channels (Figure 2.3.5). Such a phenomenon results in the inability of the planar field plate to deplete the region underneath and leads to the breakdown of the field plate stack itself at very low off-state voltages.

A much more effective strategy consists of employing a Tri-Gate terminated field plate (Figure E3 (b)). As shown in Figure 2.3.5, multi-channels nanowires can be effectively controlled by a Tri-gate electrode, thus preventing any breakdown of the field plate stack. For this reason, multi-channel devices with a Tri-gate field plate result in an improved breakdown voltage of ~ 600 V (Figure 2.3.11).

However, the use of a Tri-gate field plate offers even greater potential. In particular, a unique feature of multi-channel nanowires is the possibility to tune their threshold voltage by adjusting the nanowire width (Figure 2.3.7). This enables realizing multiple field plates with adjustable threshold or pinch-off voltage simply by varying the width of the nanowire (Figure E4 (a-b)), which can be done in a single lithography step. The optimal nanowire shape is a slanted geometry (Figure E4 (c)) [59], [88], leading

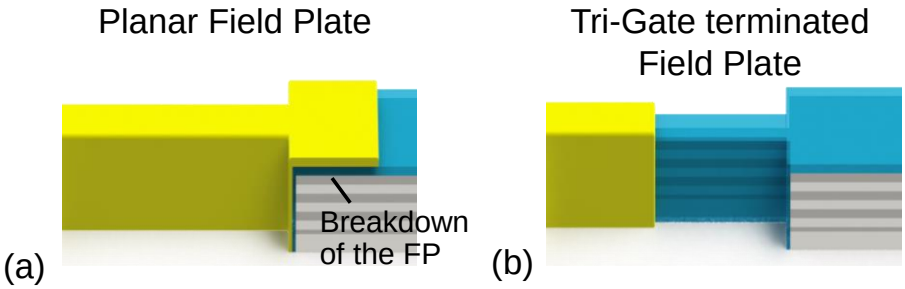


Figure E3: (a) Schematic of a conventional Planar Field Plate (FP) and (b) a Tri-Gate terminated Field Plate.

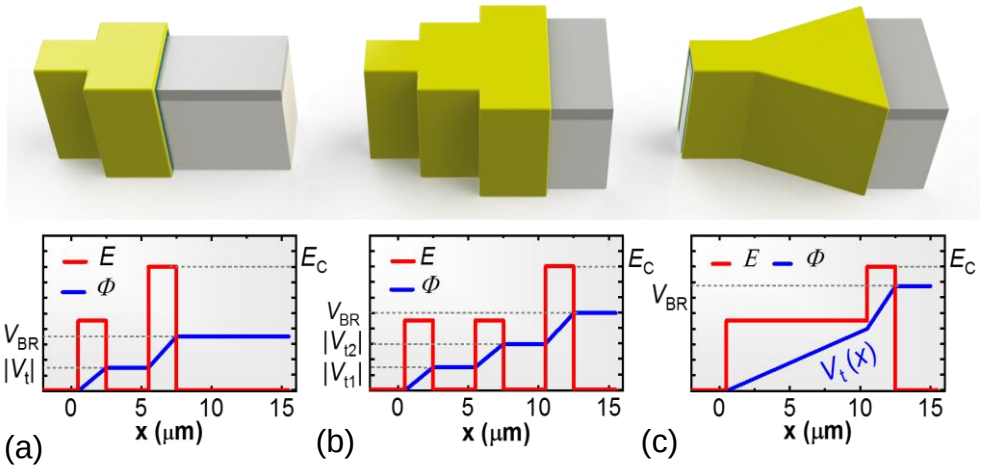


Figure E4: (a-c) Effect of the nanowire width on the channel potential profile during off-state stress. Each increase in the nanowire width leads to an increase of its threshold voltage V_{TH}, which acts as a field plate. The optimal design consists of a gradual increase in w_{NW}, achieved by a slanted nanowire design. This results in a smooth pinch-off voltage profile along the nanowire, which effectively reduces the electric field peak [59], [88].

to a gradual increase of the field plate V_{TH}. This approach enables an optimal field distribution in the field plate region and results in a significant improvement of the device breakdown voltage, as shown in Figure 2.3.11.

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Curriculum Vitae

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STRENGTHS

- Extensive expertise in simulation, design, and characterization of semiconductor devices
- Solid experimental background with strong skills in advanced micro/nanofabrication
- Project management and communication in a multi-cultural environment

EDUCATION

Swiss Federal Institute of Technology (EPFL) — Lausanne, Switzerland
Ph.D. in Microsystems and Microelectronics — 04/2018 – 05/2022

Politecnico di Torino — Torino, Italy
Master degree in Nanotechnology for the ICTs — 10/2015 – 10/2017
Final average: 30/30, Final grade: 110 cum laude/110

Université Paris Diderot — Paris, France
Master degree in Quantum devices — 2016/09 - 2017/07
Final average: 18.11/20, first average mark in the class and mention "Très Bien"

Politecnico di Torino — Torino, Italy
Bachelor degree in Physical Engineering — 2012/09-2015/10
Final average: 29.82/30, Final grade: 110 cum laude/110

PROFESSIONAL EXPERIENCE

Power and Wide Band-Gap Electronics Research Laboratory (EPFL) — Lausanne, Switzerland
RESEARCH ASSISTANT, Ph.D. — 04/2018 - Present

My goal was to develop innovative solutions for efficient and cost-effective power conversion within a European consortium including major players in the semiconductor industry. I successfully completed strictly timed work packages involving several partner institutions and addressing the main challenges in this field.

- I designed and fabricated novel GaN power integrated circuits (ICs) for high-frequency DC-DC boost converters with a 10x smaller footprint and improved efficiency compared to commercial solutions
- I developed novel thermal management solutions by embedded liquid cooling, leading to a 10x decrease in the device thermal resistance and 4x larger output current
- I demonstrated nanowire-based multi-channel power devices with more than 2x better performance than the state-of-the-art, leading to much-improved power conversion efficiency and reduced cost

IBM Thomas J. Watson Research Center, NY, USA New York, USA
RESEARCH ASSISTANT 03/2017 – 09/2017

- In a 6 month period, I demonstrated a 4" flexible pressure sensor based on an active matrix of Carbon Nanotubes Thin-Film Transistors which has great potential as artificial skin in robotics and prosthetics
- I fabricated CNTs-based flexible logic circuits with a record-high switching frequency for wearable sensor applications

Phelma Minatech-INP Grenoble, France
SUMMER INTERNSHIP 06/2015 – 07/2015

- I fabricated and characterized Silicon Solar Cells for portable applications

COMPETENCES

Design and testing of semiconductor devices	Advanced Micro/Nanofabrication	Semiconductor device simulation
	Cleanroom processing	TCAD simulation
Thermal management	Advanced imaging and inspection tools	Data Analysis
Power Electronics	Material characterization	Programming
Optoelectronic devices	Mask design	Managing and presentation skills

TECHNICAL SKILLS

- **Semiconductor Devices Characterization:** Static and Pulsed Measurements, High-Voltage tests, Hall characterization, Cryogenic measurements, Switching Losses Characterization, Double Pulse Tester, Thermal Management, Reliability, Pressure Sensors.
- **Simulation and design:** TCAD Silvaco Atlas, LT Spice, NextNano, LEdit
- **Programming and data analysis:** Matlab, OriginLab, Labview, C language, MS Office, Photoshop
- **Advanced Micro/Nanofabrication:** Lithography (Electron Beam Lithography, Photolithography, Mask Design, and Fabrication), Thin Film Deposition (ALD, LPCVD, PECVD, Sputtering, Evaporation), Thin Film Etching (RIE, ICP, Bosh Process, Vapor Etching, Wet Etching, FIB), Packaging (Dicing, Wire-bonding, Soldering, Thermal Management, Liquid Cooling), Characterization (SEM, FIB, AFM, EBIC, Optical Microscopy, Raman spectroscopy), Flexible Electronics (Polyimide, PDMS, Packaging, Wearable Sensors).
- **Industrial Training:** lab safety/clean room, worked for 4 years in an ISO 5 cleanroom, wet bench training for highly hazardous chemicals (e.g HF, TMAH)

INTERPERSONAL SKILLS

- Great project management skills in a multi-cultural and multi-lingual (EN/ FR/ IT) environment (project leader with academic and industrial partners, supervisor of 6 master students, negotiation for instruments purchase and repair)
- Excellent written and oral communication skills (4 oral lectures in technical conferences, lecturer as a teaching assistant at EPFL, strong expertise in written communication with 14 journal publications and 2 grant proposals)

LANGUAGES AND PERSONAL DETAILS

English (Fluent, C1-C2)	French (Intermediate, B2)	Italian (Native)
Date of birth 10/11/1993	Working permit B (EU citizen, Italian)	Driving license B

Extracurricular Activities: Basketball player at a competitive level for 7 years, Snowboarding (regional champion in 2008), outdoor climbing, traveling (more than 50 countries visited)

ACHIEVEMENTS AND AWARDS

Swiss Nanotechnology Ph.D. Award 2021
Best first-author publication in Nanotechnology in 2020 by a Ph.D. student from a Swiss institution

Charitat Award – International Symposium on Power Semiconductor Devices and ICs (ISPSD) 2021 2021
Award for the best young researcher first author and presenter of a paper at the conference

Featured Nature Electronics Publication 2021
More than 20 news outlets including EPFL news, Tech Xplore, Swiss Info, and AAAS

Charitat Award - International Symposium on Power Semiconductor Devices and ICs (ISPSD) 2020 2020
Award for the best young researcher first author and presenter of a paper at the conference

MIEM Excellence Scholarship - Université Sorbonne de Paris 2016-2017
Excellence scholarship of 10000 € aimed at attracting the best foreign students to France.

PUBLICATIONS

First-author of 11 journal papers and co-author of 9 journal publications (Google Scholar).
4 Oral Presentations at the leading International Conferences including one invited talk, and **16 conference papers.**
Reviewer for *Nature Electronics, Transaction on Power Electronics and on Electron Devices, Electron Device Letters*

Journal Publications (First-Author):

1. **L.Nela,** C. Erine, A. Miran Zadeh, and E. Matioli, "Intrinsic Polarization Super Junctions: Design of Single and Multi-Channel GaN Structures", *IEEE Transaction on Electron Devices*, 2022.
2. **L. Nela,** C. Erine, and E. Matioli, "*p*-GaN Field Plate for Low Leakage Current in Lateral GaN Schottky Barrier Diodes", *Applied Physics Letters*, 119, 263508, 2021
3. **L. Nela**, C. Erine, M. V. Oropallo, and E. Matioli, "Figures-of-Merit of Lateral GaN Power Devices: modeling and comparison of HEMTs and PSJs," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 1066–1075, 2021.
4. **L. Nela**, R. Van Erp, N. Perera, A. Jafari, C. Erine, and E. Matioli, "Impact of Embedded Liquid Cooling on the Electrical Characteristics of GaN-on-Si Power Transistors," *IEEE Electron Device Lett.*, vol. 42, no. 11, pp. 1642–1645, 2021, doi: 10.1109/LED.2021.3114056. **Selected as Editor's Pick.**
5. **L. Nela**, C. Erine, P. Xiang, V. Tileli, T. Wang, K. Cheng, and E. Matioli, "Multi-channel nanowire devices for efficient power conversion," *Nature Electronics*, vol. 4, pp. 284–290, 2021, doi: 10.1038/s41928-021-00550-8.
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