ME-401 Projet de Génie Mécanique 1

— Semester Project — Fabrication of glass suspended microchannel resonators

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I would like to thank Prof. Villanueva for having allowed me to work on this project. It was fascinating to see how things are done on a nanoscopic level, and being able discover and work in the CMi cleanrooms was a privilege. Of course, I would like to thank Damien Maillard, who always answered the many questions I had. This project would not have been possible without his precious help.

Abstract

The goal of this project was to study if the fabrication of glass suspended microchannel resonators was possible. Through trial and error, the process parameters were determined, starting from the ideal dose in the dry etching process. The ideal size was determined by choosing a dose that guaranteed that all holes were properly opened, while keeping the critical dimensions (CD). This allowed us to keep holes small enough to be able to fill them later on in the process. The ideal was found to be 24 mJ/cm^2. The next step of the project was to determine the right cleaning methods of the microchannels. After some unfruitful attempts, a cleaning process that worked was found. Its main steps are HF 1% during 3 minutes, followed by 1 minute in a KOH 9:1 IPA bath at room temperature. Finally, sputter deposition and LPCVD were tested to close the microchannels, with both presenting some advantages and disadvantages. During this final step, the stress buildup in the SiO_2 film showed, creating cracks in the membrane. For this reason, this process flow is not viable to fabricate glass suspended microchannel resonators.

Contents

1 Introduction

Microchannel resonators are used to weigh particles as they flow through a hollowed out cantilever, achieving a precision to the nearest femtogram. Such precision is achieved by measuring the shift in resonance frequency of the electronically actuated cantilever. Classically fabricated using Silicon nitride, this project aims to make use of silicon oxyde. Silicon Oxyde (SiO_2), better known as glass, does have a higher rigidity, so a higher quality factor Q, but its main characteristic of interest is its low thermal conductivity. This allows the microresonnator to be used for calorimetry applications, as less heat is going to escape.
This presents a couple of challenges, as SiO_2 has not been used to build microchannel resonators before by the ANEMS group at EPFL. More than just having to test out variable options for ourselves, SiO_2 is also a challenging material to work with, as its non-conductive properties render it hard to look at in a Scanning Electron Microscope.

2 Process Flow

The first step in any project that takes place at CMi is to determine its process flow. The process flow from a similar project, entitled "Optimization of Channel Design and Fabrication for suspended microchannel resonators" was taken and adapted to the specific needs generated by the particularities of working with SiO_2 instead of low-stress Silicon Nitride (ls-SiNx). After consultation with Damien Maillard and the CMi staff, the initial Process flow was approved and can be found in the Annex.

The most substantial differences between the processes are the cleaning of the microchannels (Steps 7, 8 and 9) after the dry-etching of the channels. Indeed, we anticipate that the 30" BHF step would be detrimental to the integrity of the SiO_2 layer. This is due to some chemicals having radically different etch rates in different materials.

3 Determination of Etch rates

To determine the length of time the wafers will have to be exposed to the chemicals, their respective etch rates will have to be determined. The first step was to research if these etch rates were already known. After some research [1] [2], it was determined that it would be better to determine the etch rates experimentally, as accurate data was not available.

To determine the etch rates of certain chemical on the SiO_2, two clean wafers, covered with a layer of SiO_2 were used. The thickness of the SiO_2 layers were measured using the FilMetrics F54 Automated Thickness Mapping Systems. The results can be seen in Table 1 below.

The next step was to expose the wafers to the different processes that we wanted to measure:

- The first process involved HF diluted to 1%. The wafer was immersed in HF 1% for 3 minutes, followed by immersion in water and IPA to remove the HF.
- The second process involved KOH (40%) 9:1 IPA heated to 50°C. The wafer was immersed for 2 minutes, followed by an immersion in water to remove the solution.

The final step in determining the etch rate of each process was to measure the thickness of the SiO_2 layer again. The results can be seen in Table 1 below.

Table 1: Etch rates using the different processes

Process	Thickness before etch (nm)	Thickness after etch (nm)	Etch duration (min)	Etch rate (nm/min)
HF 1%, RT	491 ± 2	473 ± 1.7	3	6
KOH (40%) 9:1 IPA, 50°C	491 ± 1.2	489 ± 1.2	2	1

[1] Pauline Stevic (July 19 2018) *BOE / HF – Silicon dioxide Etching Standard Operating Procedure*

[2] Mitsushi Itano, Frederick W . Kern, Jr., Masayuki Miyashita, and Tadahiro Ohmi, Member, IEEE (3 August, 1993) *Particle Removal from Silicon Wafer Surface in Wet Cleaning Process*

The observed etch rates will be used later on to determine the immersion time of the wafers during the cleaning phase of the fabrication of the microchannels.

4 Optimisation of process parameters

The parameters that still need to be precisely determined are the dose in step 4 of the process flow, as well as the exact time the wafers have to be in the different acids and bases in steps 7, 8 and 9.

4.1 Dose (mJ/cm^2)

One of the important parameters that would influence the fabrication process of the microchannels would be the dose used in the lithography process in step 3 of the process flow. To test the effects of each dose, test wafers with microchannels were created. Each set of 4 microchannels was exposed to a different dose, ranging from 16 to 32 mJ/cm^2, with an interval of 1 mJ/cm^2 between each set. Using the Scanning Electron Microscope, the size of the holes according to the dose was determined. Results can be found in Table 2.

Table 2: Size of holes in function of Dose

Dose (mJ/cm2)	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
width (nm)	430,9	412,2	413,8	441,3	446,8	415,7			364,4	360,1	340,3	317,3	325,2	334,1	304,8	311,6	279,6
height (nm)	502	412,2	419,8	406,6	410,8	407,8			374,4	360,1	341,8	339,9	307	327,2	304,8	292,1	268,4
average (nm)	466,45	412,2	416,8	423,95	428,8	411,75			369,4	360,1	341,05	328,6	316,1	330,65	304,8	301,85	274

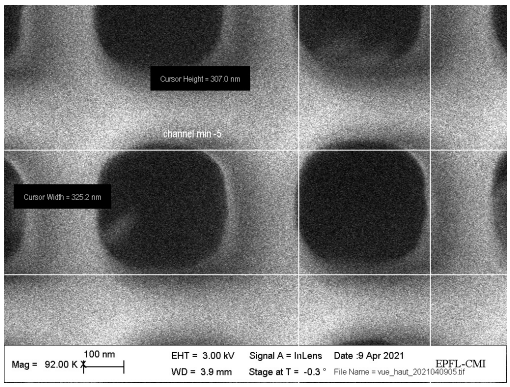
After a closer look at the data and the photos taken with the SEM, one can see that some data points do not seem correct. Indeed, the height and width of each hole should theoretically be the same. These errors were due to an astigmatism present during one of the SEM sessions. The effects of this astigmatism can be seen in Figure 1a, and can be compared to a different image where astigmatism is not present (Figure 1b). Therefore, all elements where the height and width differed more than 15 nm were removed and the results can be seen in Table 3. This gave a new table from which a Graph 2 can be drawn.

Table 3: Size of holes in function of Dose with cleaned data

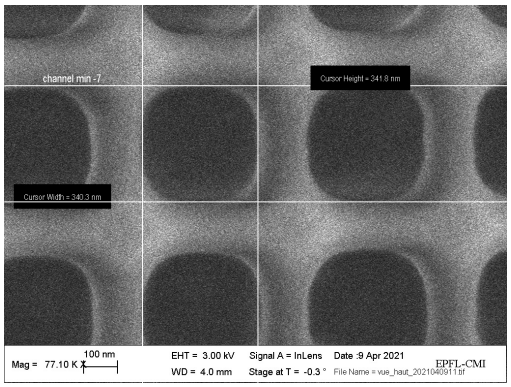
Dose (mJ/cm2)	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
width (nm)		412,2	413,8			415,7			364,4	360,1	340,3	317,3	325,2	334,1	304,8		279,6
height (nm)		412,2	419,8			407,8			374,4	360,1	341,8	339,9	307	327,2	304,8		268,4
average (nm)		412,2	416,8			411,75			369,4	360,1	341,05	328,6	316,1	330,65	304,8		274

On the graph, the polynomial trendline equation corresponding to the average between the width and the height of each hole can be seen. This function allows us to estimate the size of each hole according to the dose in mJ/cm^2. The equation is:

$$y = -0,0385 \cdot x^2 - 3,8676 \cdot x + 429,31 \tag{1}$$



(a) Dose: 16 mJ/cm^2, Astigmatism present



(b) Dose: 17 mJ/cm^2, no astigmatism present

Figure 1: The subtle difference between photos that present astigmatism and those that don't

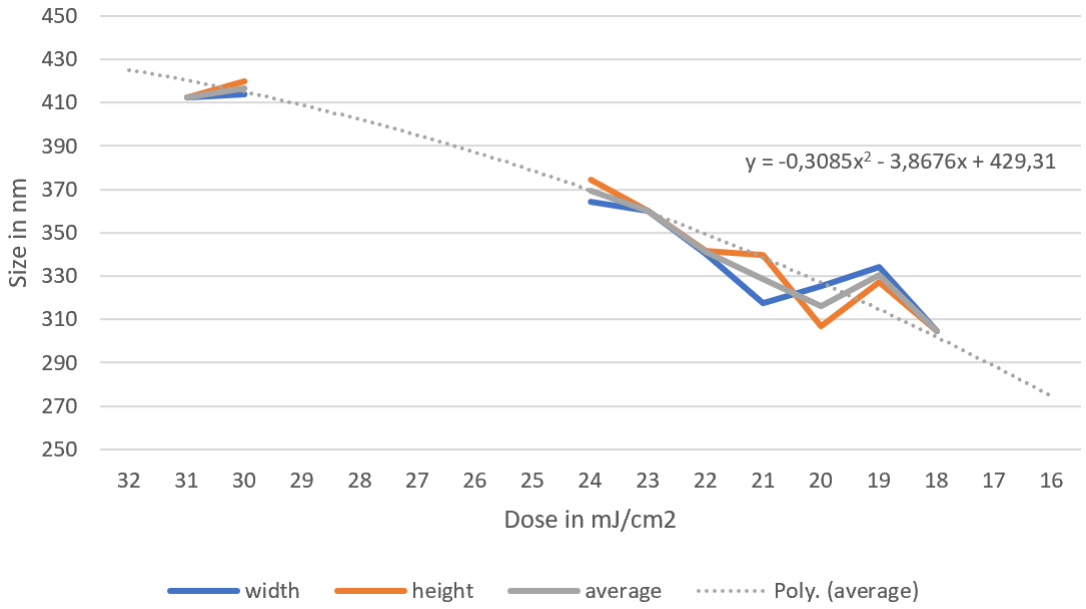


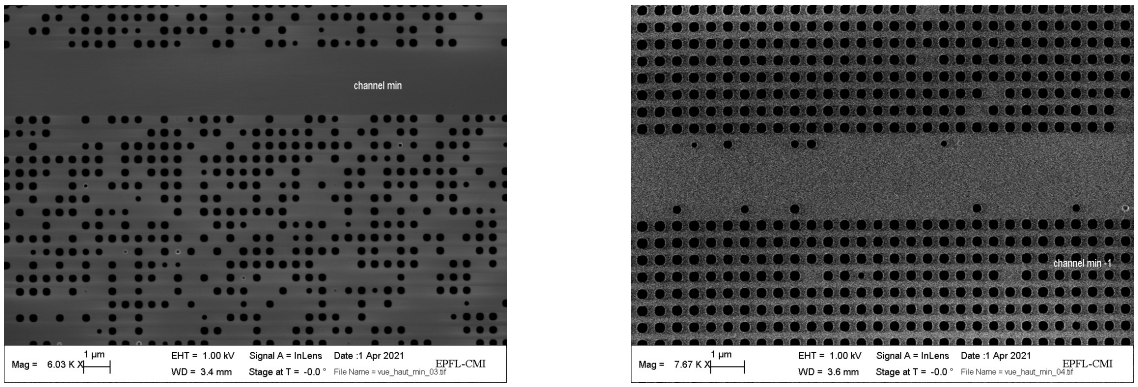
Figure 2: Size of holes according to dose, cleaned data

y corresponds to the size of one side of the holes and x corresponds to the dose in mJ/cm^2.

Other than the size of the holes, the other deciding factor in the determination of the ideal dose was if all of the holes were complete. Indeed, some holes were not entirely formed for low doses (see Figure 3).

It was also observed that if the dose was too strong, the structure would not hold, and the roof of the channels could come loose (See figure 4).

The ideal dose was therefore chosen to be at 24 mJ/cm^2, creating square holes of average side length of 369.4 nm.



(a) Dose: 16 mJ/cm^2 **(b)** Dose: 17 mJ/cm^2

Figure 3: Incomplete holes due to insufficient dosage

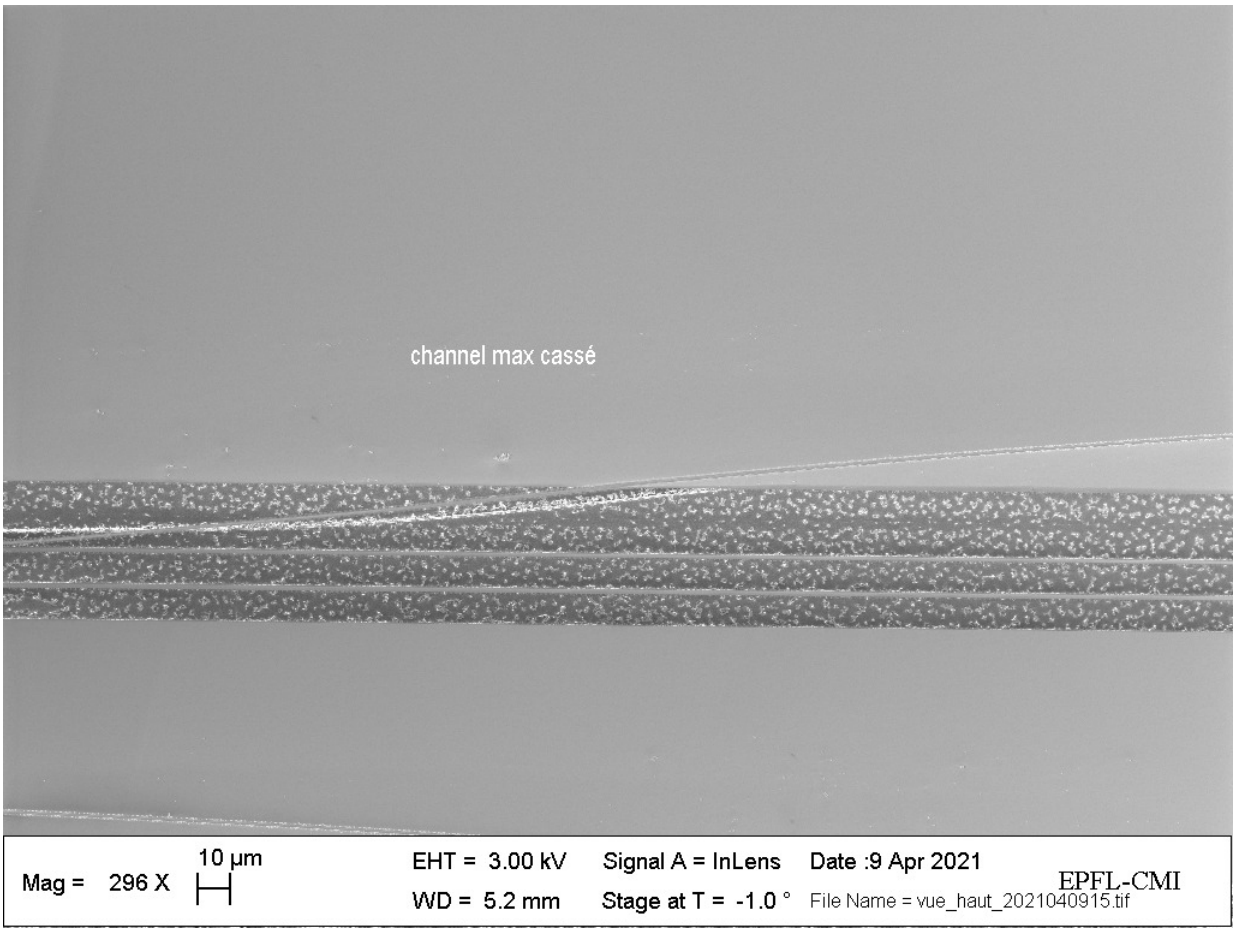


Figure 4: Ruptured microchannels subjected to 32 mJ/cm^2

4.2 Microchannel cleaning methods

After the determination of the optimal dose in the lithography step, the next parameter that has to be optimised is the microchannel cleaning. Indeed, native oxide will form in the channels, and if not removed, can act as a mask for the KOH etching later on. To remove this, the wafers are submerged in a HF 1% solution. Following the determination of the etch rates, one can expect that a 3 minute bath in HF 1% will remove about 18 nm of native

oxyde, more than what is expected to be present.
Following the HF bath, the wafers need to be exposed to a KOH solution to clean up the Si on the insides of the microchannels.

The first cleaning test on microchannels was set up.

This cleaning is rendered complicated, as ideally, one should have access to both Acid Wet Bench and Base Wet Bench simultaneously. Moreover, the wafers need to go from acid to base, then back to acid, where they have to stay for 2 hours for neutralisation. The timing therefore has to be extremely precise, and all processes involved have to be optimised to minimize time loss and going over the reserved time at each bench.

The first cleaning test was done in this order:

- First of all, a bath in HF 1% during three minutes on the Acid Wet Bench
- Then, to remove the HF, the wafer sections were then rinsed in three consecutive DI water baths.
- Still in their last water bath, the wafer sections were then transported to the Base Wet Bench
- Once on the Base Wet Bench, the KOH mixture had to be prepared. This consisted in creating a KOH (40%) 9:1 IPA mixture, and heating it up to 50°C using a magnetic stirring hot plate.
- Once the wanted temperature was achieved, the wafer sections were inserted into the mixture, and left for three minutes.
- Once the three minutes over, the wafer sections were again rinsed in three separate DI water containers, and the transported back to the Acid Wet Bench,
- The wafer sections were left to sit for at least two hours in HCl 37% for neutralization.
- Finally, the wafers were again rinsed three times in DI water.

The results of this first test can be seen in Figure 5, and it can be observed that the thin walls between the microchannels have been destroyed by an exposure to the heated KOH solution that lasted too long.
One can also see the effect that the size of holes has on the cleaning process. The image in top left was exposed to 23 mJ/cm^2, the one on top right to 22 mJ/cm^2, bottom left to 18 mJ/cm^2 and finally bottom right to 17 mJ/cm^2.

The second cleaning test was done on wafer section that had been exposed to larger doses and consisted in the following steps:

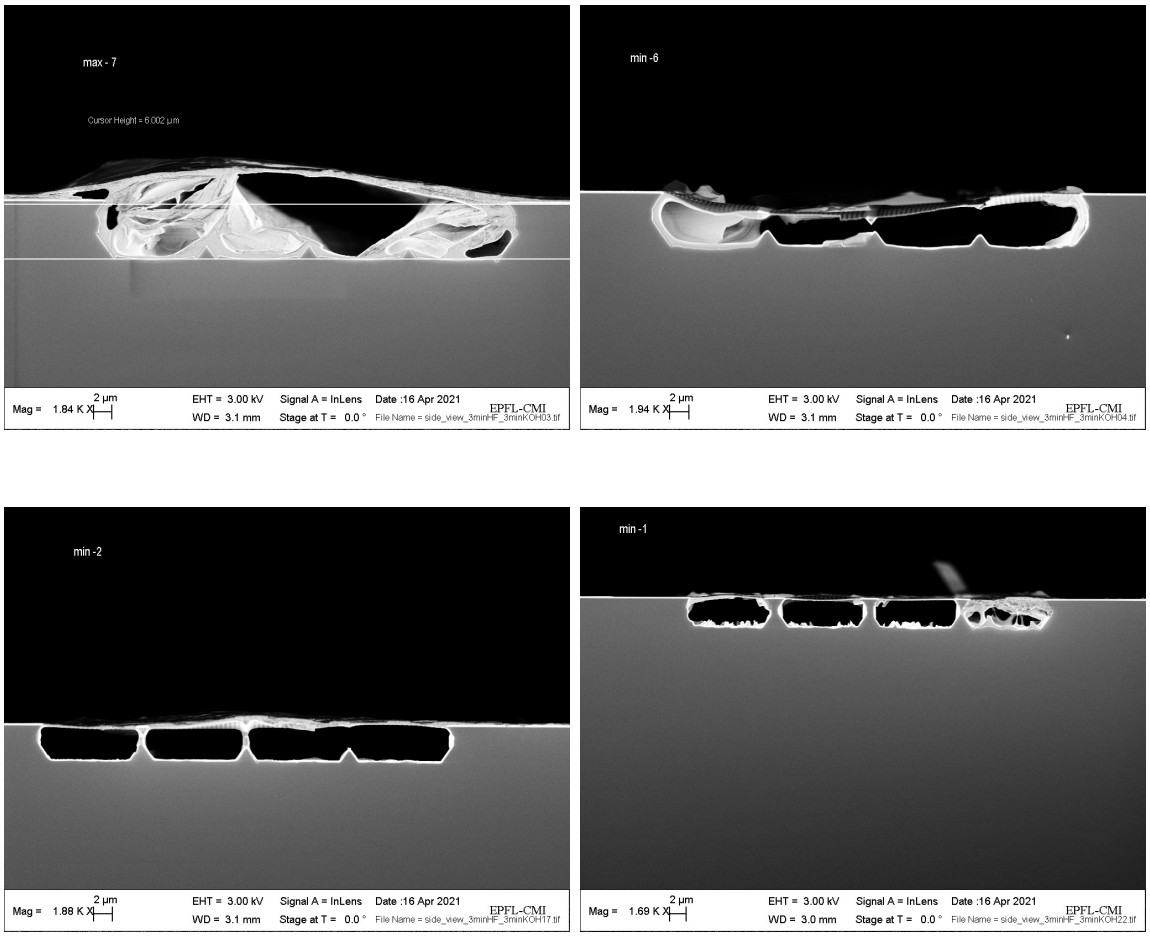


Figure 5: Different side views of 3 min HF and 3 min KOH at 50°C cleaning

- 3 minutes in HF 1%
- 1 minute in KOH (40%) 9:1 IPA at 50°C
- Neutralization in HCl 37% for at least 2 hours

In between each step, the wafer sections were rinsed with 3 baths of DI water.
The results can be seen in Figure 6. Again, the effects of the size of the holes can be seen. Indeed, the bigger the holes, the more the chemicals can enter the microchannels and be in contact with the thin microchannel walls. Top left corresponds to the biggest holes, with a dose of 32 mJ/cm^2, top right 28 mJ/cm^2, bottom left 27 mJ/cm^2 and finally bottom right 25 mJ/cm^2.
We can observe that being exposed to the KOH mixture at 50°C for 1 minute is still too long, as the walls are destroyed or too thin.

To reduce the speed at which the KOH mixture attacks the Si, two options presented themselves:

- We could either reduce the time further and keep the temperature at 50°C

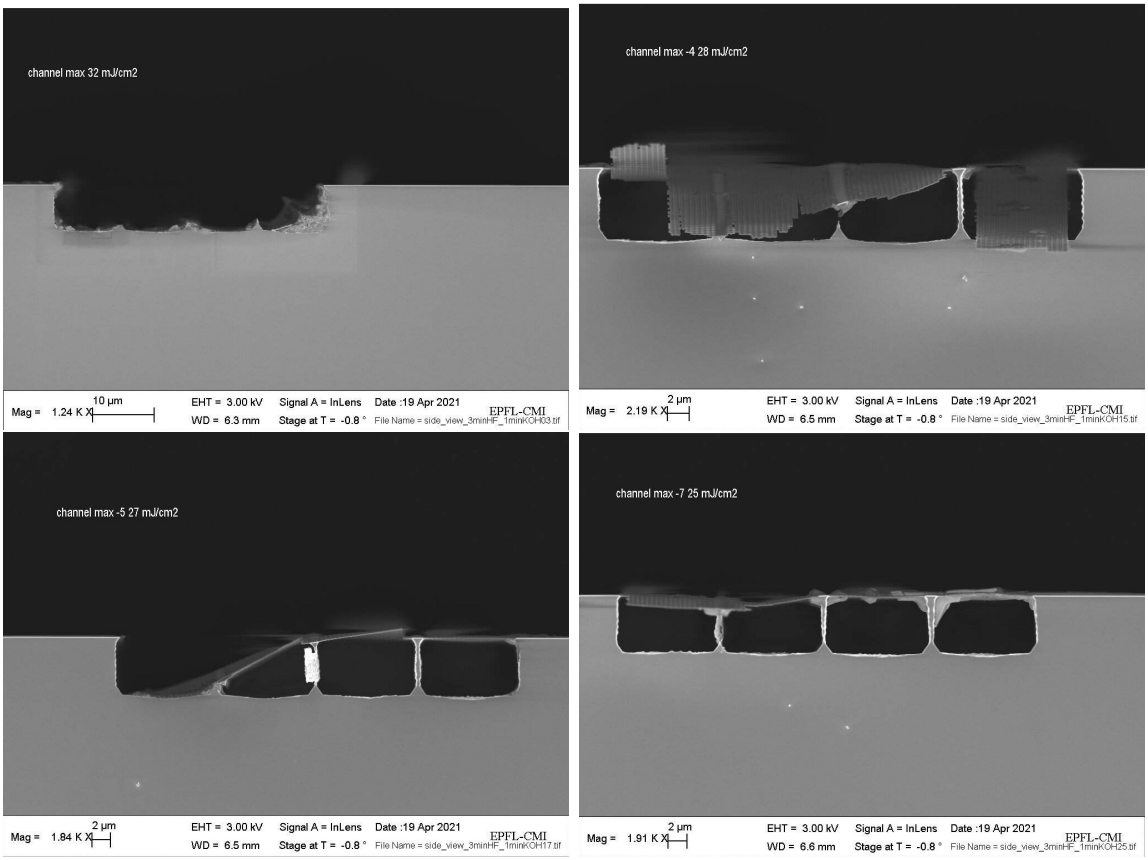


Figure 6: Different side views of 3 min HF and 1 min KOH at 50°C cleaning

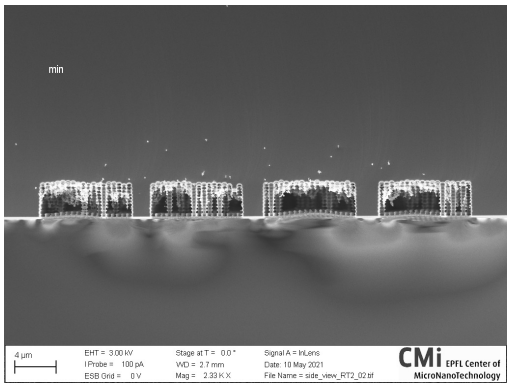
- or we could reduce the temperature to room temperature, slowing down the etch rate of the KOH solution in the Si.

To simplify the process, it was therefore decided to forego the heating of the KOH mixture and to operate at room temperature. The third cleaning test consisted in doing the same steps as for the first two, but this time the wafers were only exposed to the KOH solution for 1 minute at room temperature.
The results of this cleaning test can be seen in Figure 7.

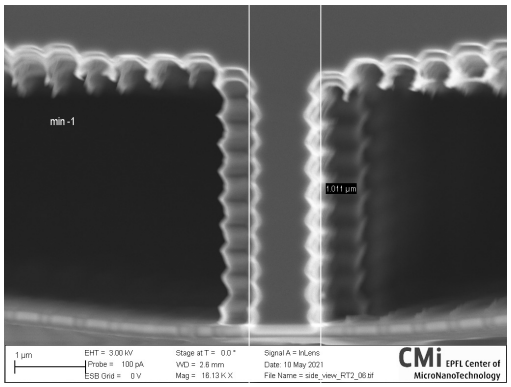
As can be seen in Figure 7, the dose, thus the size of the holes has a great impact on the cleaning process.

Figure 7a shows us the side view of the channels, previously exposed to 16 mJ/cm^2, after cleaning. We can observe that the channels are not cleaned well enough, and that there are still some left over "pillars" that were not entirely removed by the baths.

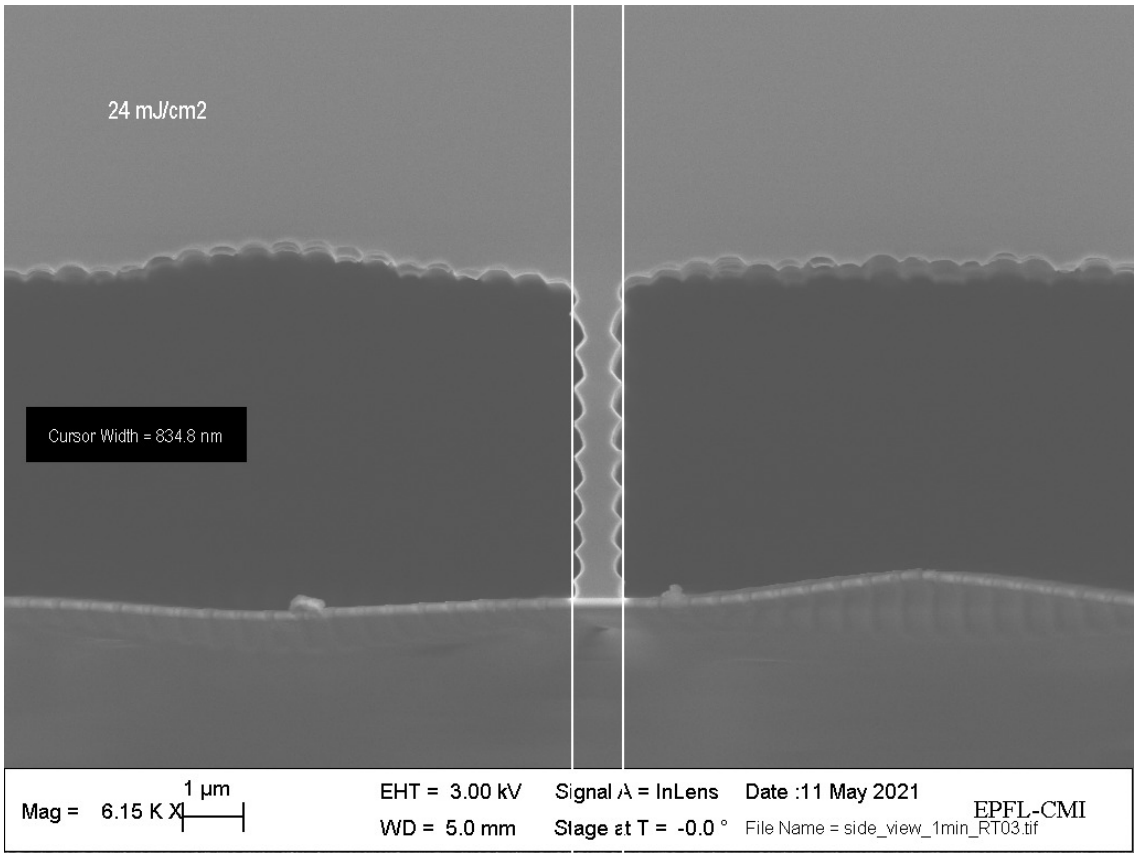
Already a dose higher, at 17 mJ/cm^2 (Figure 7b), the pillars are all but destroyed, and only a small amount of extra material is left. The surface inside the microchannels is still very rough, meaning that, for this dose, the length of time the wafer sections are exposed to the KOH solution is not long enough. The width of the thinnest wall between two microchannels



(a) Dose: 16 mJ/cm^2



(b) Dose: 17 mJ/cm^2, width of thinnest wall



(c) Dose: 24 mJ/cm^2, width of thinnest wall

Figure 7: Different side views of 3 min HF and 1 min KOH at RT cleaning

was also measured in at 1.011 μm.

At 24 mJ/cm^2 (Figure 7c), all extra residue is removed. In this case, the thinnest wall only measures 834.8 nm, almost 200 nm less than the channels exposed at 17 mJ/cm^2. The interior surface of the channels are smoother, meaning that the SiO_2 deposition in the next steps of fabrication will be of much higher quality.

We have therefore determined a cleaning process that works for the fabrication of this specific type of microchannels:

- Start off with a 3 minutes HF 1% bath.
- Rinse three times in DI water to stop the effects of the HF.
- Transport the wafers or wafer sections, without letting them dry, to the Base Wet Bench.
- Insert the wafers or wafer sections into the KOH solution for 1 minute. This solution is a KOH (40%) 9:1 IPA mixture at room temperature.
- Rinse three times in DI water to stop the effects of the KOH solution.
- Neutralize the wafers/ wafer sections in HCl for at least 2 hours.
- Rinse three times in DI water.

It is important to note that this cleaning process is optimised for a dose of 24 mJ/cm^2, or for holes sized around 370 nm. If the holes are of a different size, or if the dose is different, the time lengths of the different cleaning baths has to be adapted.

5 Closing of the channels

Up until now, we have determined the dose needed and the size of holes to which this corresponds. Using this information, we determined the appropriate cleaning process, leaving us with clean channels in Si underneath a thin film of SiO_2, as can be seen in Figure 8.

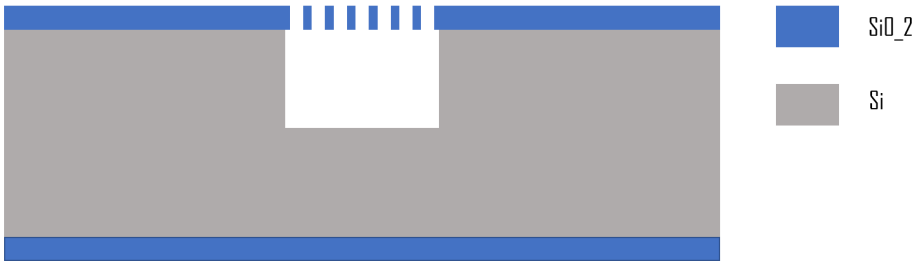


Figure 8: State of the fabrication after cleaning

The next step in the process flow is to create SiO_2 walls inside the channels, and to close the holes on top of the channels. To do this, there are several options available to us.

5.1 Sputter Deposition

The first method tested to close the channels is sputter deposition. This type of physical vapor deposition consists in ejecting material from a source material, also known as "target" onto the wafer.
In our case, a 400 nm SiO_2 sputter deposition was done using the Spider 600 in Z04. A side view can be seen in Figure 9.

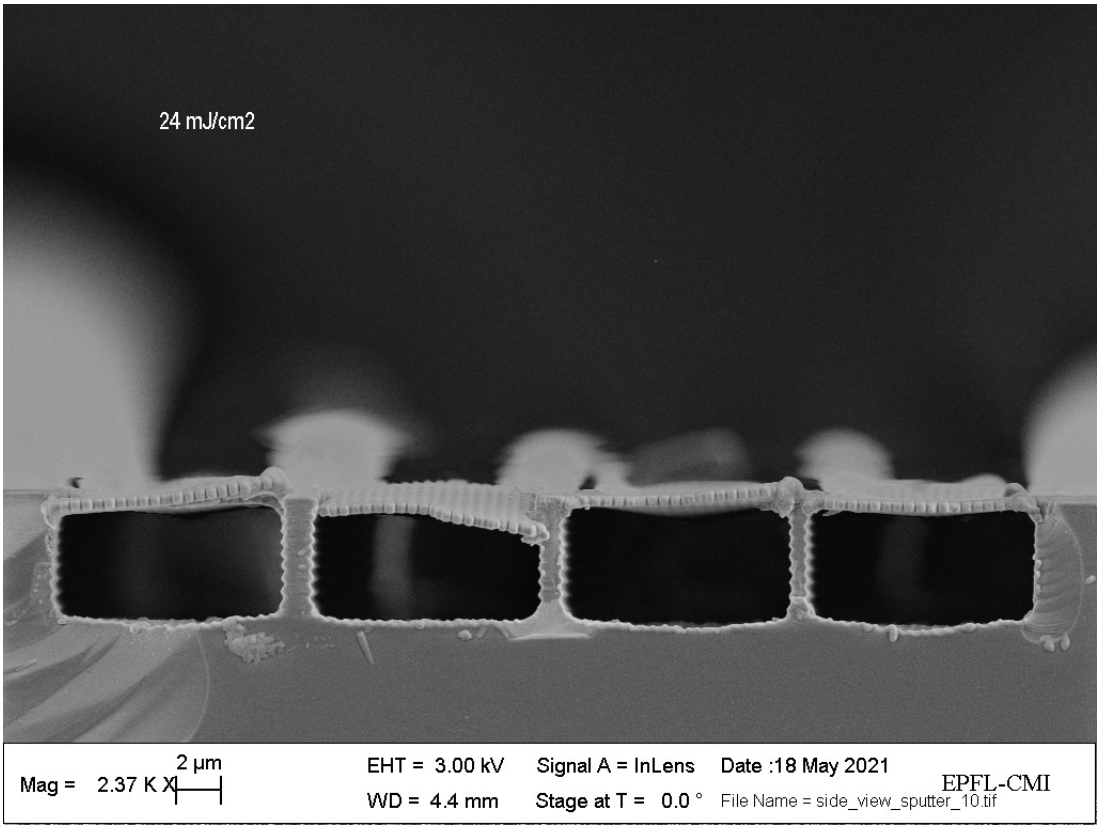


Figure 9: Side view after sputter deposition

From Figure 9, we can see that the channels are not closed up, probably due to the fact that the 400 nm layer deposition was too thin. In order to see if the the holes have gotten smaller or not, a closer look can be taken in Figure 11. Indeed, the initial size of the holes corresponding to this dose is 370 nm, after the sputter deposition, they are now only 80 nm. We can therefore conclude that the holes have indeed gotten smaller, and we can assume that if the thickness of the added SiO_2 were to be increased, the holes would eventually close up. One can also observe that from all these side views (Figures 9, 11, 12 and 10), the channels seem to be intact for the most part. In Figure 9, we can see that the roofs of the channels seem to have broken off to some extent, but we can assume that this happened while cleaving the wafers for observational purposes after the sputter deposition.

In this case again, we can see the effects the initial dose has on the rest of the process. If we take a look at Figure 12, corresponding to a dose of 16 mJ/cm^2, we can see that

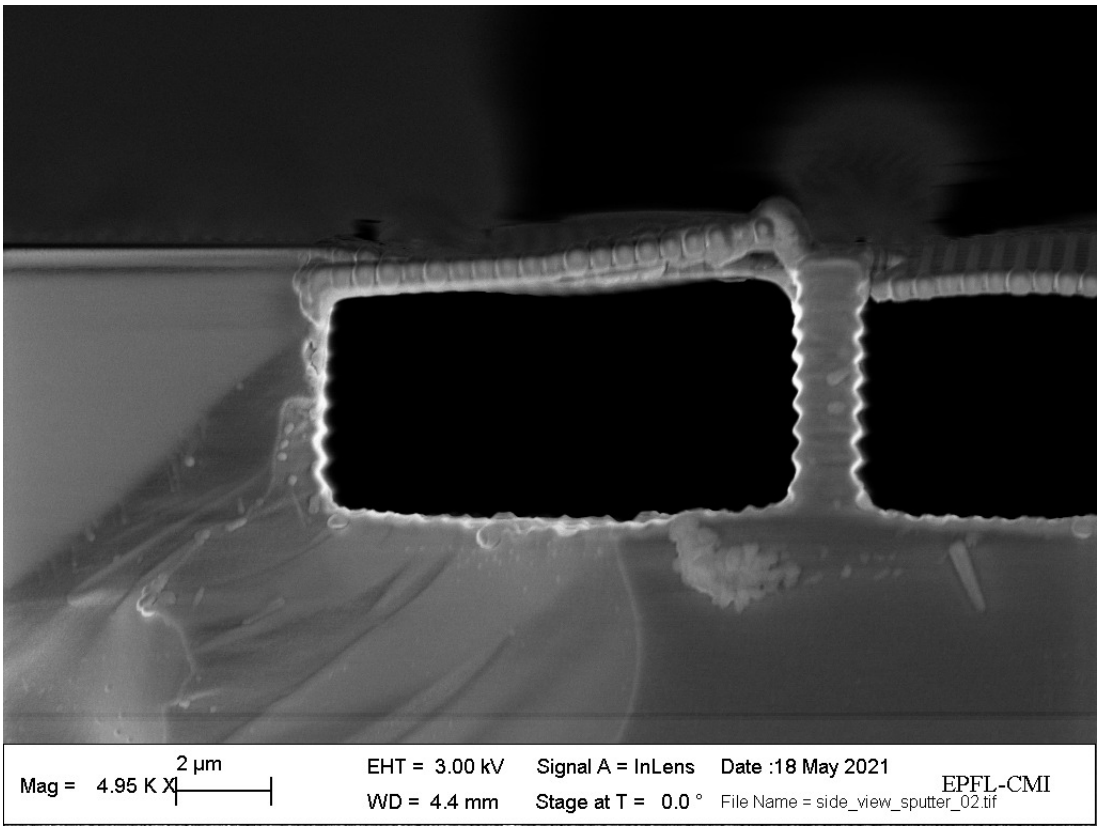


Figure 10: Side view of channels exposed to 24 mJ/cm^2 after sputter deposition

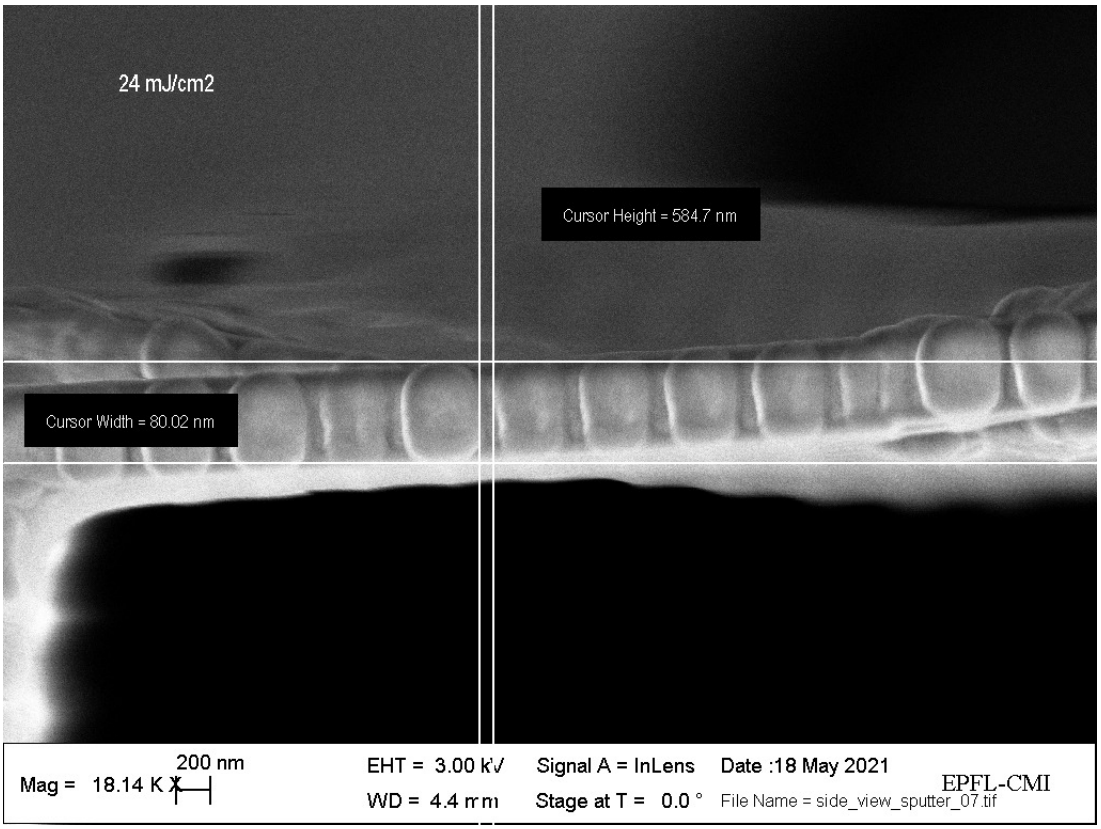


Figure 11: Size of holes after sputter deposition

the initial holes are not big enough to let through enough material to build a a full SiO_2 surface in the inside of the microchannels. Indeed, it causes some small accumulations of the deposition on the bottom of the channels, but nothing on the side walls. This is therefore another confirmation of the choice of a dose of 24 mJ/cm^2.

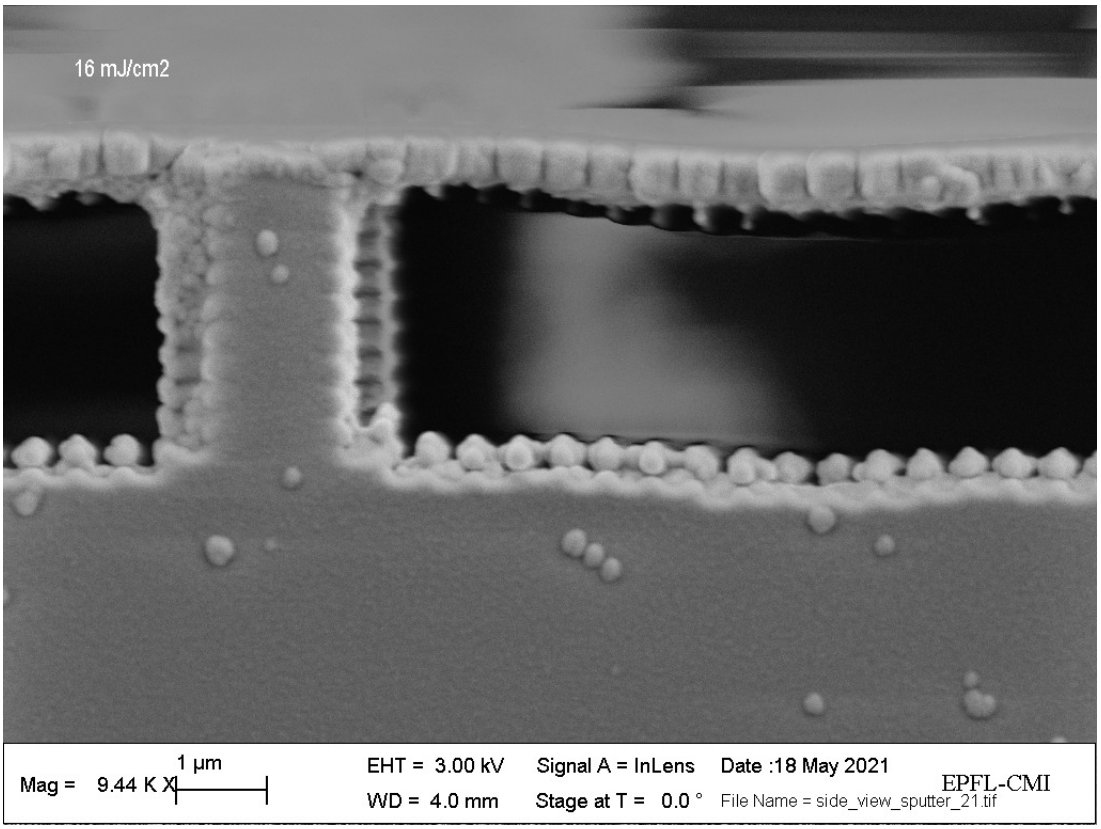


Figure 12: Side view of channels exposed to 16 mJ/cm^2 after sputter deposition

5.2 LPCVD

The second option was to use a Low pressure chemical vapor deposition process. As its name indicates, this process uses chemical vapor deposition induced by a high temperature to build a thin film on the wafer. Two options existed:

- TEOS (Tetra Ethyl Ortho Silicate), process done at 710 °C and 200 mT
- or LTO (Low Thermal Oxide), process done at 425°C and 120 mT

After consultation with CMi staff, it was decided that the best option would be the TEOS process, as the quality of the deposition would be higher. Higher quality does however come with a drawback, as the temperature reached during this process could have some negative side effects.

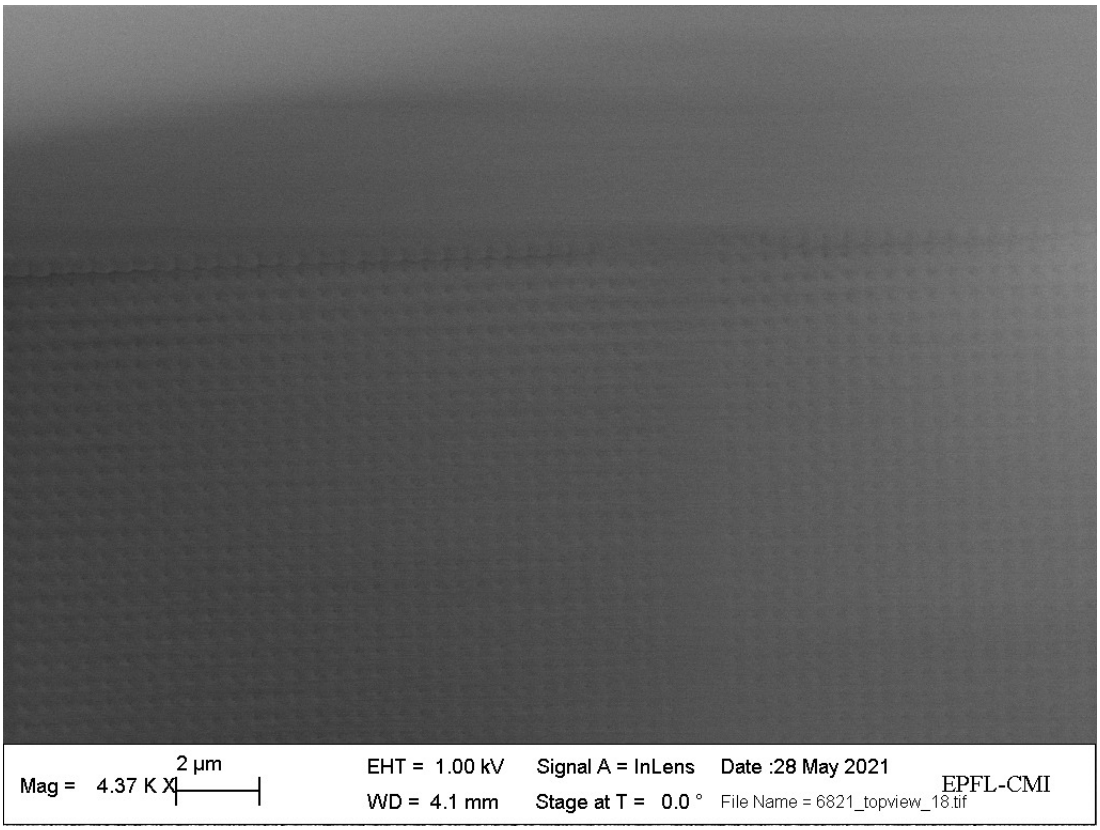


Figure 13: Top view of the holes after 500 nm TEOS

After a 500 nm deposition, the first step was to look at the wafers from the top. This gave two very important results: First of all, as can be seen in Figure 13, the holes seem to be filled. However, looking at the top of the wafers also revealed cracks in the roof of the devices. These can be seen in Figures 14 and 15.

Indeed, on most of the devices, the part where the channels are the largest shows some cracks, as can be seen in Figure 14. On one occasion, it was even observed that a crack formed on the thinnest part of the microchannel, as can be seen in Figure 15.
A side view of the cleaved microchannel can be seen in Figure 16. The image was taken at an angle in order to remove the saturation caused by the non conductive SiO_2. In this image, we can also observe the buckling of the roof. This buckling is probably what causes the cracks to appear. Finally, the TEOS process is very efficient in coating the inside walls of the microchannels in SiO_2. The coated thickness is measured in Figure 17.

5.3 Comparison between the different techniques

Comparing the two different techniques, there are several advantages and disadvantages for each technique. Indeed, the sputter deposition is a very easy process to do, we have however, not yet tested if the holes would close up all the way if the thickness were to be increased.
The LPCVD has a higher quality, but also a big disadvantage, as the cracks appear in the

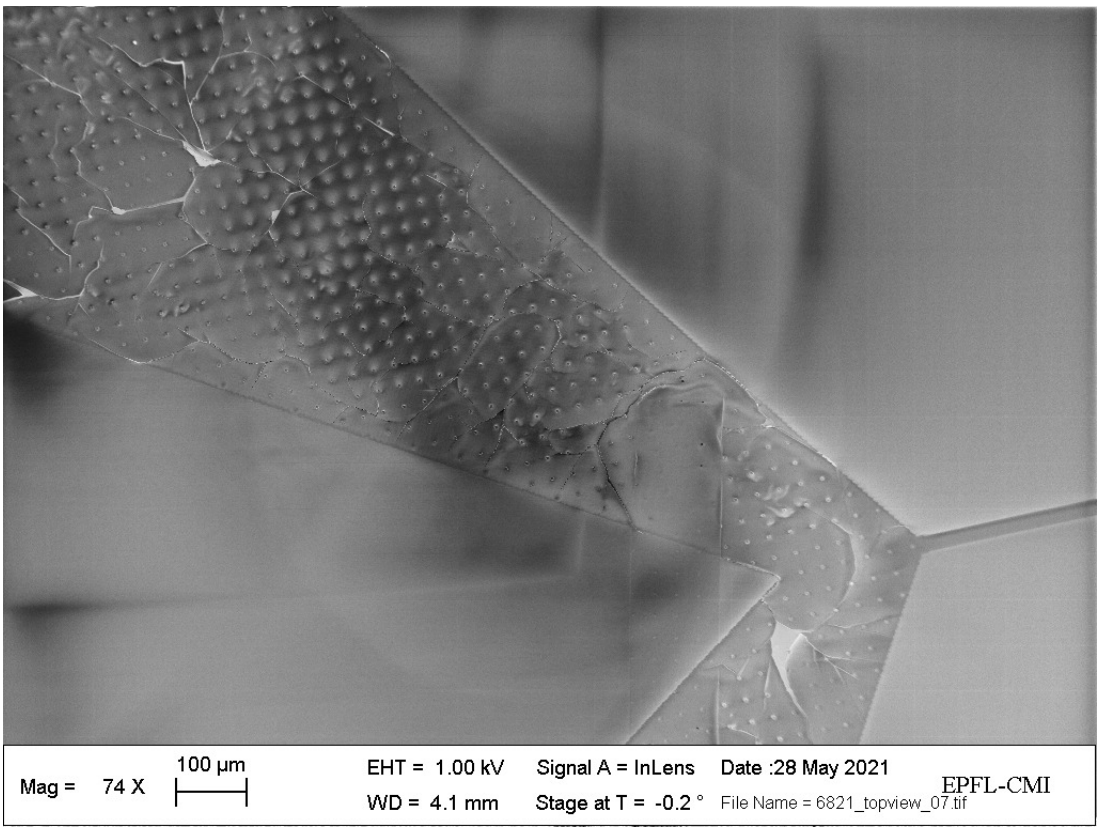


Figure 14: Cracks appear after the TEOS process

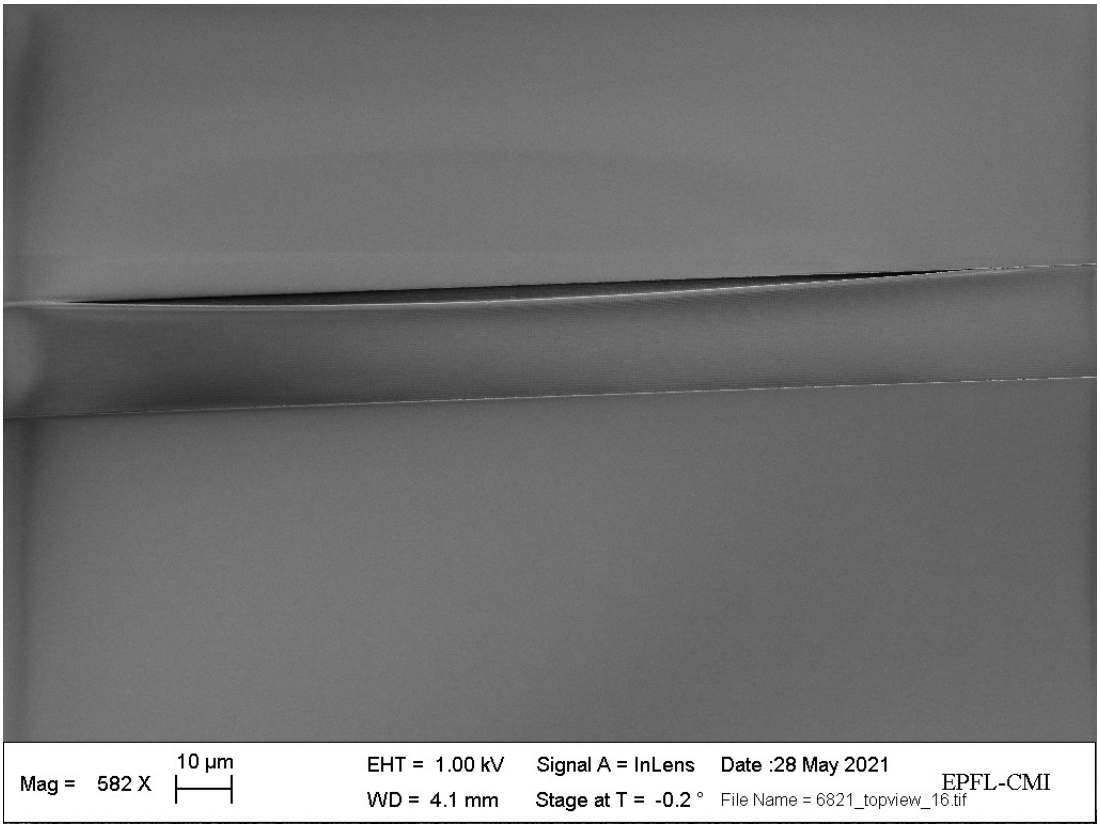


Figure 15: Cracks appear after the TEOS process

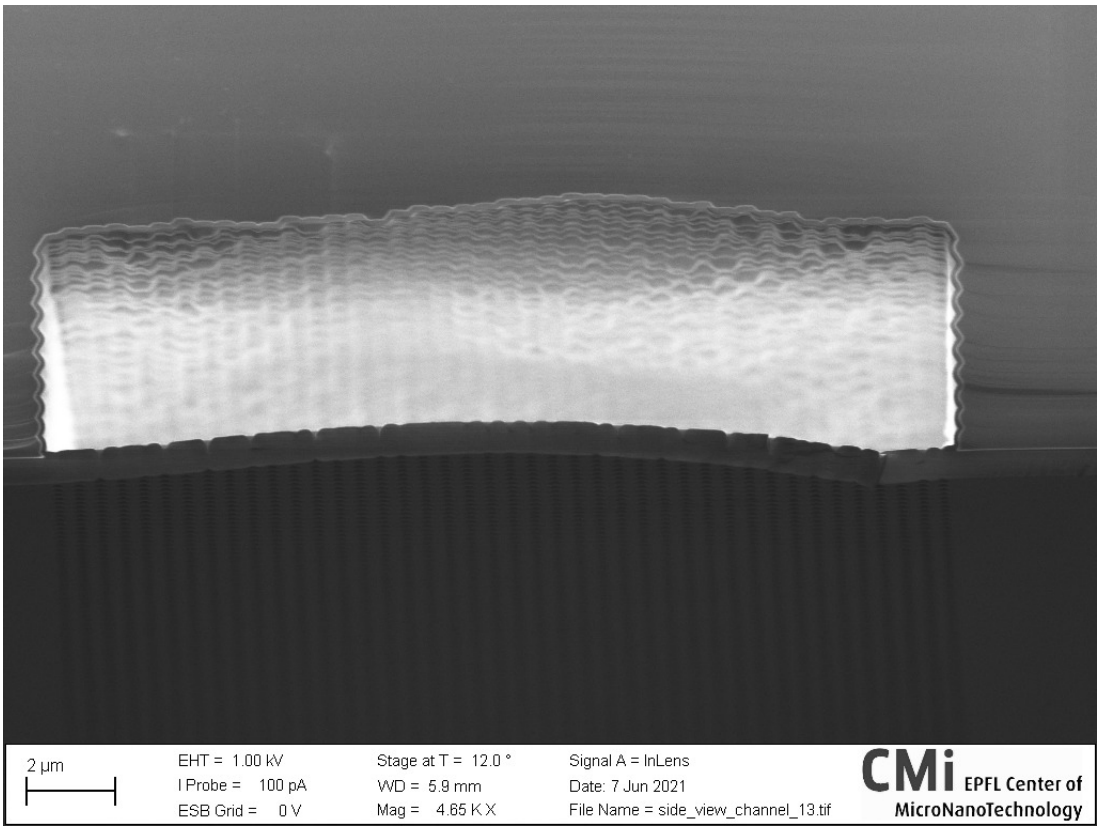


Figure 16: Side view of the TEOS coated channels

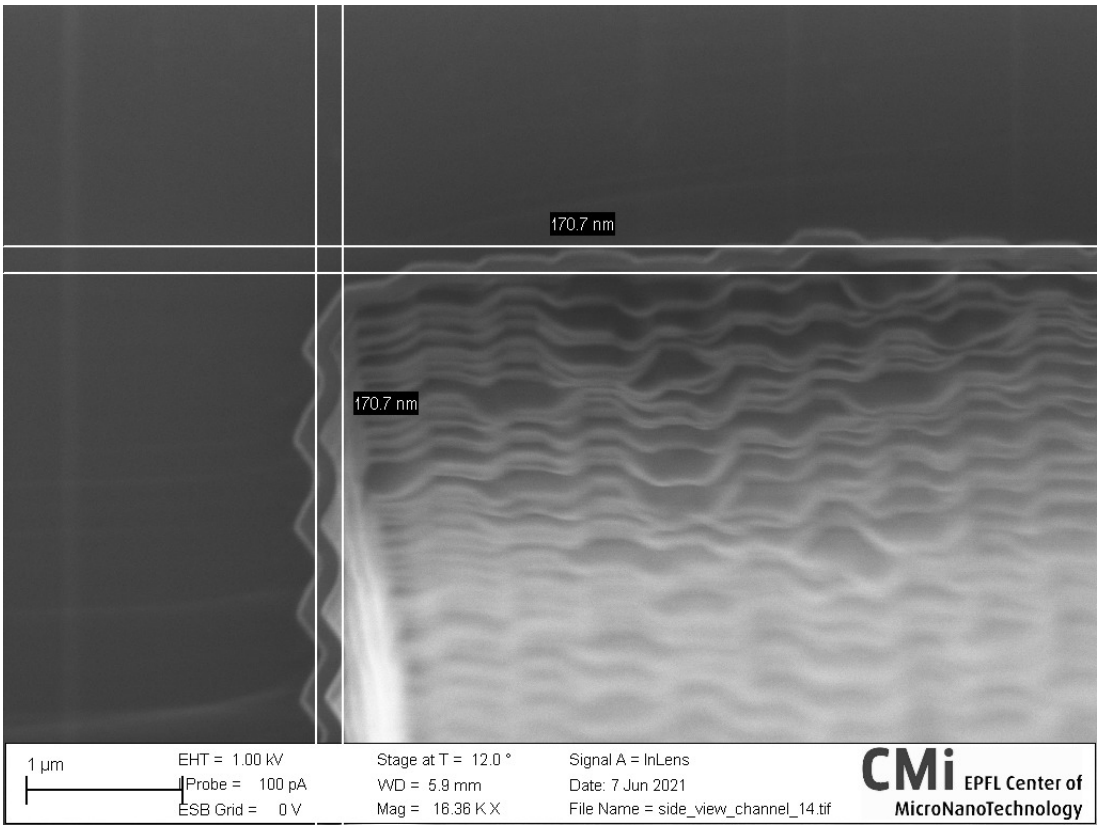


Figure 17: Thickness of SiO_2 coating inside the microchannels

roofs of the microchannels. The most probable cause for these cracks is the stress present in the SiO_2 membrane.
This specific and last part of the mechanical aspect of this project still needs some attention to determine the best way to close up the microchannels.

6 Conclusion

To conclude, this project was an adaptation by trial and error of an already existing process flow to a new kind of material. After determination of the optimal dose for the dry etching process, a cleaning method was devised, taking into account the specific characteristics of the materials in use. The final process flow can be found in the annex. However, this project did not find a viable way to fabricate glass suspended microchannel resonators. The main problem is the stress in the SiO_2 layer that induces cracks in the membranes. A next possible step would be to include a layer of tensile stressed silicon nitride to conteract the compressive stresses in the SiO_2.

two different methods to close the channels were tested and compared. The process flow for the fabrication of glass suspended microchannel resonators.

7 ANNEX

Initial Process Flow after modification

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CMi EPFL Center of MicroNanoTechnology

☒ Semestral Project ☐ Master Project ☐ Thesis ☐ Other

Optimization of Channel Design and Fabrication for suspended microchannel resonators

Description of the fabrication project

We fabricate suspended microchannel resonators, using silicon oxide (SiO_2) as structural material. Microchannels are etched in silicon through Bosch process, and cleaned with diluted HF and KOH.
The purpose of the project is to fabricate the suspended microchannels that are made of silicon oxide (SiO_2). The shape of the microchannels will be etched directly in a silicon substrate on which SiO_2 layers has been deposited previously. The sidewalls and the bottom of the microchannels will be defined by depositing of SiO_2 on the etched shape. The micro-channels will be closed by the deposition as well. The microchannels will be then released from the substrate to form the suspended microchannels.

Technologies used			
DUV lithography, Dry and wet etching, RCA cleaning, LPCDV SiO_2 deposition, SEM			
Photolithography masks			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**200 nm**	First layer	Stepper
2	**20 µm**	2um	Release
Substrate Type			
Silicon <100>, Ø100mm, 525um thick, Single Side polished, Prime, p type, 0.1-0.5 Ohm.cm Thin film : 200nm SiO_2.			

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.
☒ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.
☒ No ☐ Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.
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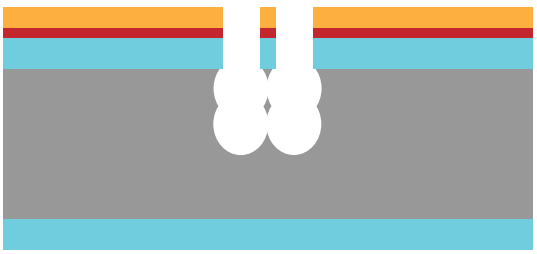
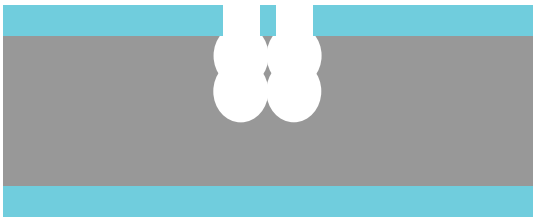
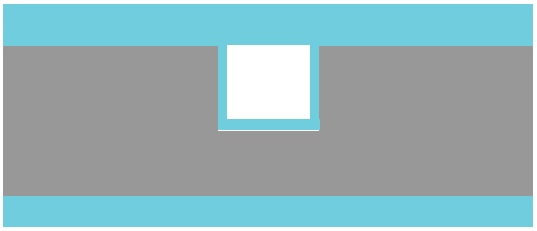
Step-by-step process outline

Step	Process description	Cross-section after process
A0	**6'' reticle mask** Fabricated externally	
01	**Substrate**: ***Si test+SiO_2 (200 nm)***	
02	*Photoresist coating* Material: *DUV42P + JSR KrF M35G* Machine: *ACS200* Thickness: *1200 nm*	
03	*DUV lithography + Development* Machine: *ASML PAS 5500/350c + ACS200*	
04	*Dry etching* Material: *DUV42P + SiO_2* Machine: *SPTS APS* Depth: *60 nm + 200 nm*	
05	*Dry Etching* Material: *Si* Machine: *AMS 200* Thickness: *6 μm*	

06	*PR removal* Material: *DUV42P + JSR KrF M35G* Machine: *Tepla Gigabatch*	
07	*Immersing to remove residues* Solution: HF 1% Time: *to be determined* Arias Acid wet bench Z14 Keep in beaker containing water to move it to Arias solvent wet bench Z14	
08	*Immersing to remove HF* Solution: *Water followed by IPA (to reduce surface tension)* Arias solvent wet bench Z14	
09	*Immersing to remove residues* Solution: KOH (40%) + IPA (9:1) Time: *25* Arias Base wet bench Z14	
10	*2h neutralization HCl 37%* Arias Acid wet bench Z14	
11	*SEM Inspection* Machine: *SEM Zeiss Leo*	

12	*RCA cleaning (without SRD)*	
13	*LPCVD (done by the staff, RCA)* Material: SiO_2 Thickness: *300 nm*	

Final process flow

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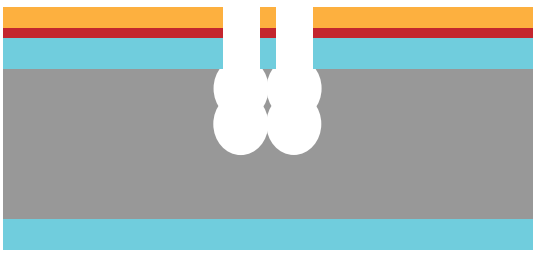
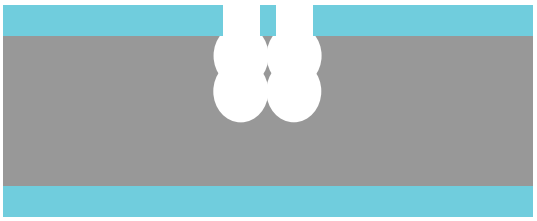
05	*Dry Etching* Material: *Si* Machine: *AMS 200* Thickness: *6 μm*	

06	*PR removal* Material: *DUV42P + JSR KrF M35G* Machine: *Tepla Gigabatch*	
07	*Immersing to remove residues* Solution: HF 1% Time: *3 minutes* Arias Acid wet bench Z14 Keep in beaker containing water to move it to Arias solvent wet bench Z14	
08	*Immersing 3 times to remove HF* Solution: DI water Arias Acid wet bench Z14	
09	*Immersing to remove residues* Solution: KOH (40%) + IPA (9:1) Time: *1 minute* Arias Base wet bench Z14	
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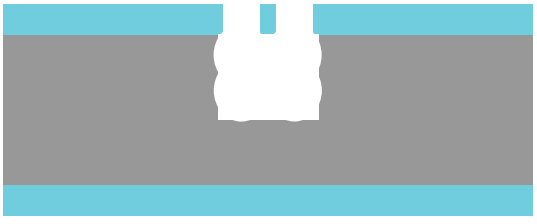
12	*RCA cleaning (without HF)*	

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13	*LPCVD (done by the staff, RCA)* *t.b.d (TEOS, LTO, or other)* Material: SiO_2 Thickness: 5*00 nm*