Hard-Switching Losses in Power FETs: the Role of Output Capacitance

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***Abstract*— For certain field-effect transistors (FETs) in soft-switching operation, the large-signal behaviour of their output capacitance ($C_\mathbf{o}$) has shown to deviate considerably from the datasheet values. This can have a significant effect on hard-switching losses if the output charge value is also different for a given voltage. However, standard hard-switching tests are incapable of fully setting apart the contributions from $C_\mathbf{o}$, whereas existing methods tailored to characterize $C_\mathbf{o}$ losses in soft-switching operations subject $C_\mathbf{o}$ to a fundamentally different charge–discharge process, and hence, might not predict the correct behaviour for hard switching. To address this, first we analyse and establish the particular charge–discharge conditions that $C_\mathbf{o}$ undergoes in hard-switching circuits by considering a half bridge at no-load conditions. We show that the channel of the switching device incurs a fixed energy loss during the turn-ON process, which is separated into co-energy and stored energy components of the top and bottom devices, respectively. Exploiting this, a new measurement technique is developed to obtain charge versus voltage (QV) curves of devices subjected to actual hard switching. Experimental results for commercial Si, SiC and GaN devices show that the effective charge-capacity of $C_\mathbf{o}$ for hard switching can considerably vary from the values based on datasheets or the Sawyer–Tower circuit; this could greatly undermine efficiency and thermal optimizations in design phases.**

***Index Terms*—co-energy, hard switching, no-load circuit, output capacitance ($C_\mathbf{o}$), QV curves, Sawyer–Tower, switching losses.**

Nomenclature

C_{dc}	dc-link capacitance.
C_o	Output capacitance (of a field-effect transistor).
C_{oss}	Small-signal output capacitance.
d	Duty ratio in hard switching.
E_o	Energy stored in device output capacitance.
E_o^*	co-energy related to device output capacitance.
E_{oss}	Small-signal value of E_o reported in datasheets.
E_{on}	Total turn-ON energy loss of a switching device.
$E_{on\text{-}C_o}$	Contribution of device output capacitances to the total turn-ON energy loss of a device in leg-configuration.
$E_{on\text{-}VI}$	Turn-ON energy loss related to external load current.
f	$= 1/T$. Frequency of ac excitation signals.
f_{sw}	$= 1/T_{sw}$. Switching frequency.
i_{CH}	Channel current.
i_{DS}	Drain current.
i_{CO}	Current through output capacitance.
i_{in}	Total instantaneous input current.
I_{in}	Average input current.
i_L	External load current (assumed constant at I_L).
P_{in}	Average input power.
Q_o	Output charge.
Q_{oss}	Small-signal output charge.
R_{ch}	Instantaneous resistance of device channel.
$R_{DS(on)}$	ON-state resistance of device channel.
R_{GH}	External gate resistance in turn-ON path.
R_{GL}	External gate resistance in turn-OFF path.
S_1	Bottom device in leg-configuration.
S_2	Top device in leg-configuration.
T_d	Dead time.
v_{DS}	Instantaneous drain–source voltage.
V_{DS}	dc-bias voltage on drain–source terminals.
v_{GS}	Instantaneous gate–source voltage.
$V_{GS(th)}$	Gate–source threshold voltage.
V_{dc}	dc-link (or bus) voltage.
V_m	Peak value of small-signal ac excitation voltages.
V_p	Peak value of large-signal voltages.

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I. Introduction

HIGH-frequency (HF) power converters play an important role in high-power-density applications [1]–[3]. For soft-switching circuits operating in such frequencies, large-signal hysteresis losses caused by the output capacitance of certain field-effect transistors (FETs) can be a major hindrance [3]–[5]. In 30-A devices for example, these losses vary from a few tens of nanojoules to a few microjoules at 400-V operation, for frequencies below 1 MHz [4]. In contrast, hard-switching energy losses, dominated by the turn-ON loss [6], are typically around 50–500 μJ at 400 V for the same devices. But more importantly, in hard-switching converters, the role of C_o is fundamentally different as opposed to in soft-switching operation. Therefore, the effects of any large-signal anomaly in C_o for hard-switching operation—for instance, a change in output charge—first need to be understood from a topological perspective. This article introduces an energy-based method to capture and isolate the losses related to output capacitance in hard-switching circuits. Based on the proposed concepts, an experimental technique relying on average electrical measurements is developed to obtain the output-charge versus voltage (QV) curve for a given FET, which is true to the charge capacity of C_o in actual hard switching. The technique can create different switching speeds and is independent of dead-time, switching frequency and device on-resistance, making it a potent tool to characterize QV behaviour and C_o losses.

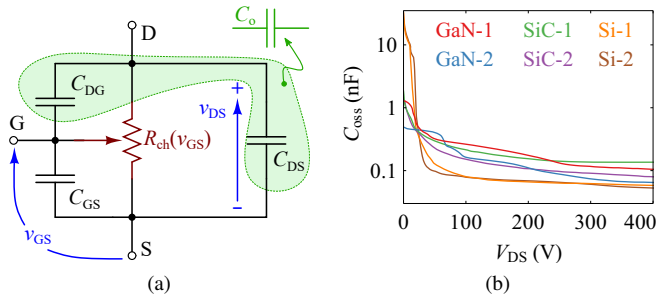

Fig. 1. (a) Model of a FET showing its output capacitance, $C_o = C_{DG} + C_{DS}$. The channel of the FET can be represented as a variable resistance $R_{ch}(v_{GS})$ dependent on v_{GS}. (b) Variation of datasheet-given small-signal output capacitance, C_{oss}, with V_{DS} for the commercial power FETs tested in this study, which have a current rating in the vicinity of 30 A (see Table I).

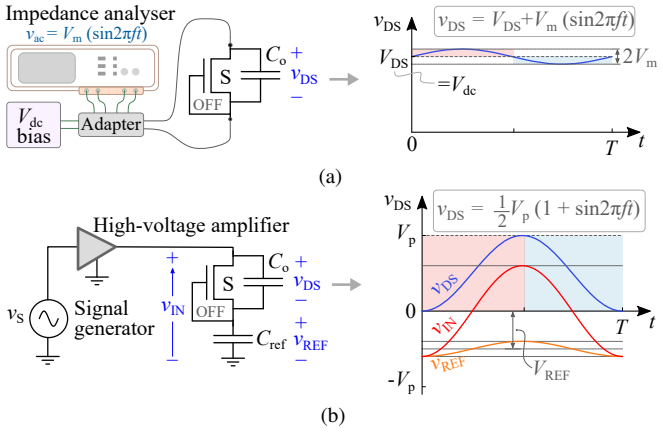

Fig. 2. (a) Small-signal output-capacitance versus voltage curves are generally measured with impedance analysers or curve tracers. A small sinusoidal-excitation-signal v_{ac} in mV range, with a peak–peak value of $2V_m$ and frequency $f = 1/T$, on top of a dc-bias voltage V_{dc} is applied to the device drain–source terminals, while v_{GS} is kept at 0 V. The imaginary part of the measured impedance is used to derive C_{oss} versus V_{DS} values. (b) Sawyer–Tower circuit (see Appendix A for additional details) can be used to observe the large-signal behaviour of C_o at the same frequency, but with the excitation signal having a peak–peak value $V_p \gg 2V_m$, approaching the value of V_{dc}.

Our previous work [7] on the subject presented the interpretation of the capacitive co-energy loss in hard-switching circuits, and a no-load method to decouple and separately calculate both stored and co-energy components. The method was experimentally validated with a thermal loss-estimation technique. Building upon this previous work, here we analyse in detail the role of output capacitance in hard-switching circuits and deliver important findings by comparing C_o-characterization methods. Section II of the article gives a review on C_o and different circuit mechanisms that dictate its behaviour, followed by motivations for this work. In Section III, the charging process of C_o and the co-energy component is detailed, developing the first principles to identify $Q_o \cdot V_{dc}$ as the loss contribution of C_o for a hard-switched device. The unique behaviour of the no-load circuit configuration is analysed in Section IV, highlighting its different operating modes; then the experimental method to obtain QV curves is presented and verified. In Section V, we provide a comprehensive comparison of the QV behaviour of Si, SiC and GaN devices in small-signal, soft-switching and hard-switching conditions, which is followed by a discussion in Section VI and conclusions in Section VII. Appendix A gives a summary of the Sawyer–Tower method and Appendix B provides mathematical details of the co-energy theory. An extensive discussion on practical and measurement considerations is given in Appendix C.

II. Background, Motivation and General Principles

With the growth of power MOSFET technology, HF soft-switching converters have been widely researched to push existing power density limits [3], [8], [9]. In doing so, Fedison et al. found an unexpected loss mechanism related to the output capacitance [Figure 1(a)] of silicon super-junction (Si-SJ) MOSFETs [9], which could not be explained with the capacitance versus voltage (CV) curves from datasheets.

In device datasheets, output capacitance is given as a small-signal parameter, typically notated as C_{oss}. Fig. 1(b) plots C_{oss} versus V_{DS} curves for the set of commercial devices that are studied in this work. These small-signal plots are obtained using impedance measurements based on a mV-level excitation voltage (v_{ac}) on top of a large dc-bias voltage (V_{dc}) as Fig. 2(a) illustrates. Evidently, with such an excitation, the process of storing (and discharging) electric charges into (and from) C_o is dictated by v_{ac}, and hence the term *small-signal excitation*. However, the anomalies observed by Fedison et al. [9] could only be explained by the subsequent investigations on the large-signal behaviour of C_o, where the related losses were attributed to a hysteresis loss in the charge–discharge paths of C_o [10]. Methods like the Sawyer-Tower circuit were then adapted to subject C_o to *large-signal excitations* [11]. In these methods, as Fig. 2(b) depicts, C_o is subjected to a much larger ac excitation voltage in comparison to small-signal methods, with peak–peak voltages reaching to values such as 400 V.

Recent research has also shown C_o anomalies in GaN and silicon carbide (SiC) devices in soft-switching circuits [3]–[5], [12], [13]. Then it follows logically to investigate the large-signal behaviour of C_o in hard-switching circuits. For example, an error in the estimation of Q_o could translate to a considerable change in power loss at f_{sw} of several hundreds of kilohertz. Additional research has shown that the QV curves of certain device types, obtained with small-signal methods at different frequencies, and with the Sawyer–Tower circuit, exhibit a large offset in Q_o in comparison to datasheet curves [3], [14]. This is an important sign that C_o-related losses in hard switching could also be different in actual large-signal operation. Several recent research efforts have investigated such behaviour [15], [16]. Section III-B of this article discusses their implications and limitations.

A better perspective on the role of output capacitance in creating losses could be gained by realizing that the charge–discharge process of C_o is topology-dictated, as illustrated in Fig. 3. In conventional PWM switching, the charging and discharging of C_o are confined to the switching transitions [marked by blue and red highlights in Fig. 3(c)]. For example, in the double-pulse-test (DPT) circuit, $C_{o,S2}$ gets charged by the dc voltage source during the turn-ON transition of S_1 where the channel of S_1 acts as a series resistance, $R_{ch,S1}$; this creates an additional energy loss in $R_{ch,S1}$ known as the co-energy

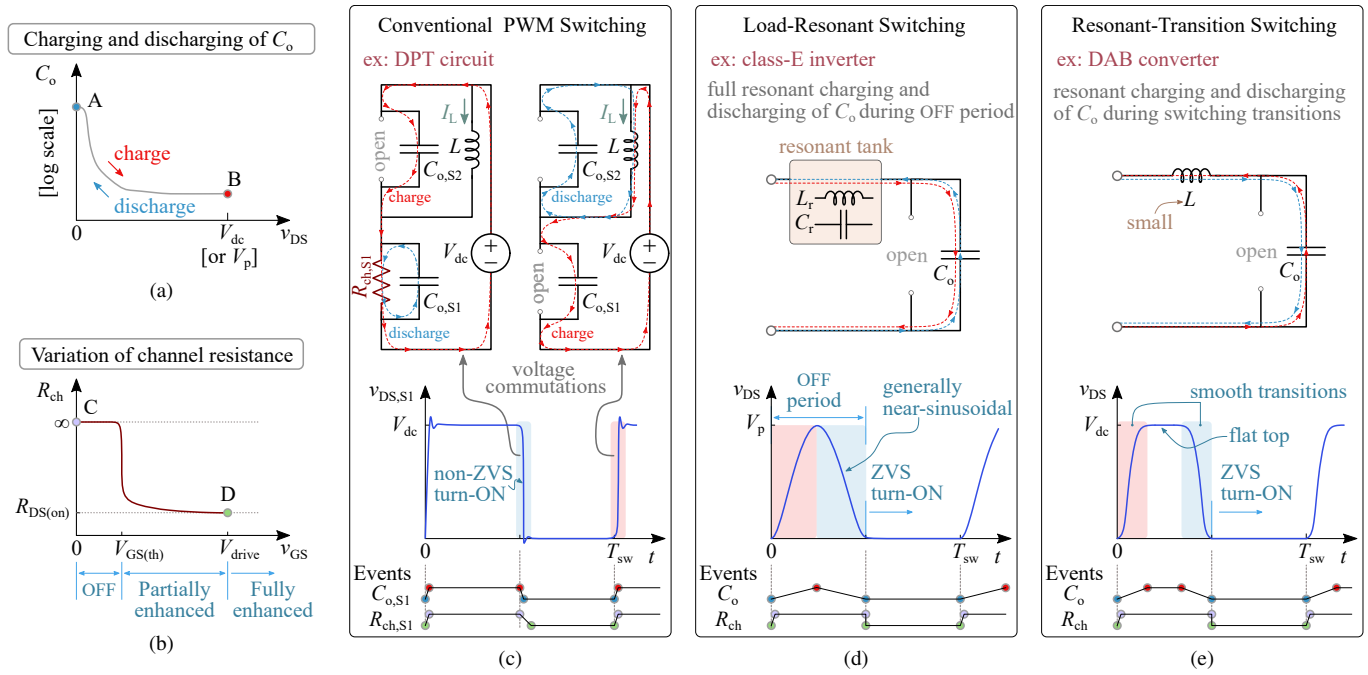

Fig. 3. Behaviour of C_o in different topologies. (a) During the charging and discharging processes, C_o traverses the paths A–B and B–A, respectively. (b) The channel resistance (R_{ch}) of the device takes the paths C–D and D–C during its ON and OFF transitions, respectively. The coincidence or non-coincidence of the paths of C_o and R_{ch}, and their nature, are topology-dependent. This is highlighted by the events indicated in sub-figures (c), (d) and (e). For a given device, the output-capacitance losses are dependent on how the charge–discharge process is dictated by the circuit (i.e., the voltage waveform across C_o is determined by the topology and energy source). In this regard, and generally speaking, three different scenarios can be found: (c) conventional PWM switching (note: $C_{o,S1}$ and $C_{o,S2}$ are bottom- and top-device output capacitances, respectively); (d) load-resonant switching; and (e) resonant-transition switching.

loss [7], which is discussed in Section III. In contrast, the charging of $C_{o,S1}$ is dictated by the inductor L which does not create the same co-energy loss situation. In the class-E inverter [Fig. 3(d)], which is a load-resonant soft-switching converter [17], the complete charge–discharge cycle of C_o is spread through the OFF state, unlike in conventional PWM converters. More importantly, here the process is dictated by the resonant load-inductance, and not the dc voltage source. Thus, any resulting losses are purely due to the hysteretic behaviour of C_o. In resonant-transition switching [Fig. 3(e)], the charge–discharge process is again dictated by an inductance used to achieve zero-voltage-switching (ZVS) [18], although this process happens only during switching transitions; and any resulting loss related to C_o is purely hysteretic [19].

This analysis shows that a generic measurement technique would not correctly capture the loss related to C_o, as the loss depends on how C_o is being treated in a topology. On the one hand, methods like the Sawyer–Tower technique and its variations [11], do not recreate the actual hard-switching process, and hence, are unsuitable to characterize hard-switching losses. In the Sawyer-Tower circuit, device drain–source terminals experience an excitation similar to what is shown in Fig. 3(d), and a basic operational difference exists as an ac voltage source is used to charge and discharge C_o. On the other hand, the standard methods used for hard-switching tests cannot separate the individual contribution of C_o from the total switching loss; this is due to the existence of load current that complicates the analysis as well as any measurements [20], [21]. To find a comprehensive solution, first, we investigate the fundamental concepts related to the charging process of C_o in hard switching (Section III) and then extend the developed concepts for a suitable measurement technique (Section IV).

III. Charging of a Capacitor and Co-energy Loss

A. Stored Energy and co-energy Concepts

A typical charge versus voltage curve of a transistor output capacitance is shown in Fig. 4(a), where an example for a real transistor is given in Fig. 4(b). For the charging process from 0 to Q_o, the energy stored in the capacitance is given as

$$E_o = \int_0^{Q_o} v_{DS}\, dQ. \tag{1}$$

E_o is also equal to the *discharge loss* when C_o is discharged.

The integral given in (2) defines the *co-energy* component related to the output capacitance [7], [22].

$$E_o^* = \int_0^{V_{dc}} Q\, dv_{DS} \tag{2}$$

Fig. 4(a) also shows that the addition of E_o and E_o^* results in

$$E_o + E_o^* = Q_o V_{dc}. \tag{3}$$

The detailed derivations of these equations are given in Appendix B. Fig. 5 shows a circuit where C_o of a field-effect transistor is charged with a dc voltage source, in series with a resistor R. The energy distributions for the charging process show that irrespective of the value or the time variation of R, both the stored energy (E_C) and the energy loss in R (E_R) converge to fixed values at the end of the transient. More importantly, E_R converges to the co-energy of C_o, E_o^*. The

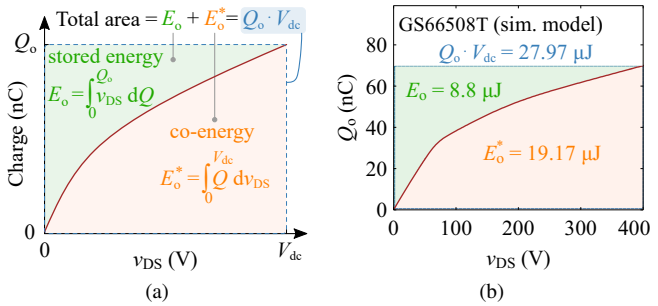

Fig. 4. (a) Stored energy and co-energy components related to the output capacitance of a FET (which is a nonlinear function of v_{DS}) can be identified on a charge versus voltage (QV) plot. (b) QV curve of a GaN HEMT (GS66508T) based on the data extracted from the manufacturer simulation model (version 4.0) for *LTspice XVII*.

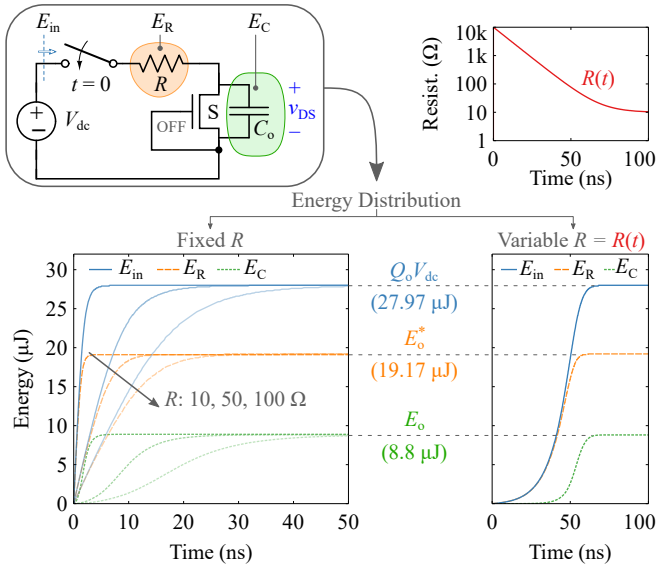

Fig. 5. A GaN HEMT (GS66508T) model, with its gate–source terminals shorted, is put in series with a resistor, R, and an ideal dc voltage source V_{dc} = 400 V. The circuit is turned ON at $t = 0$, and C_o of the FET is charged. An *LTspice* simulation is carried out for five different fixed values of R, and for a case where R is made to behave as a time-dependent function $R(t)$. The energy stored in C_o, lost in R, and supplied by the voltage source are denoted as E_C, E_R, and E_{in}, respectively; each component converges to a fixed value irrespective of the value or the time dependence of R.

results also show that the energy (E_{in}) supplied by the fixed voltage source is only determined by the product $Q_o V_{dc}$.

This analysis indicates that when a power electronic topology dictates an operating condition where C_o is charged with a fixed voltage source, such as the case presented for $C_{o,S2}$ in Fig. 3(c), an energy loss equivalent to the co-energy is dissipated in the resistive path, irrespective of the value of resistance; in this regard, the co-energy can be considered as a *charge loss*. If the stored energy is also lost due to hard turn-ON in a subsequent operating mode, then all of E_{in} ($= Q_o V_{dc}$) is completely lost in the circuit. This is the basis of the presented no-load technique (Section IV-A). Note that if either the charging or the discharging of C_o is achieved by a transfer of inductive energy through resonance [19], [23] as in the cases shown in Figs. 3(d) and 3(e), or with an ac voltage source [Fig. 2(b)], any related loss is of hysteretic nature.

B. Historical Background on co-energy and $Q_o V_{dc}$ Loss

The co-energy component creates a *real* energy loss when a capacitor is charged by a fixed dc voltage source [7], [23].[1] While this loss looks quite foreign—and even counter-intuitive—for a power electronic circuit,[2] it is a known topic in switched-capacitor circuits [26], [27], and in the research on optimal charging of capacitors [28], [29].

A profound discussion on the losses associated with the charging and discharging of C_o is found in an article by Gauen in 1989 [23]. The article specifically addresses, and separates, charge and discharge losses based on small-signal capacitance curves, with individual attention to the contributions from C_{DS} and C_{DG}. The more recent articles by Miftakhutdinov [15] and Deboy et al. [30] consider the co-energy component as a charge loss and a Q_{oss}-related loss, respectively; the works also describe $Q_o \cdot V_{dc}$ as the total C_o-related loss for hard switching. The two articles also emphasize the importance of the use of large-signal capacitance curves to estimate these losses, with particular reference to the large-signal anomalies reported by Fedison et al. for Si-SJ devices [10]. In relation to a DPT circuit, Jones et al. [31] and Hou et al. [25] analysed the effects of co-energy loss, however treating it as a 'Q_{oss} loss mechanism' occurring at the switch-node.

In the domain of soft-switching converters, in 2012, Elferich used the terms 'co-energy'[3] and 'dual energy' to represent the energy associated with the area below a QV curve [as in Fig. 4(a)] in relation to an analysis on ZVS transition energy [22]. The ideas were also discussed by the subsequent work by Oeder et al. [32] in the estimation of switching losses in resonant converters.

Using energy balance for a switching period in ZVS operation, Kasper et al. showed $Q_o \cdot V_{dc}$ as the upper limit of partial-ZVS operation, which reflects a fully hard-switched condition [19]. This is the basis for the subsequent works by Azura Anderson et al. [33], [34] and Guacci et al. [16] on the analysis of *minimum* hard-switching losses in bridge and multi-level topologies. The authors employ calorimetric measurements to assess switching losses in both soft- and hard-switching conditions. The test circuits possess a special mode with *zero-current switching*—a half-bridge operating at no load—which permits the calculation of $Q_o \cdot V_{dc}$ loss. Regarding the electrical measurement of C_o-related losses in hard switching, Miftakhutdinov utilized (in 2014 [35] and in 2017 [15]) a half-bridge circuit without any load to evaluate $Q_o V_{dc}$ loss. However, the details of the circuit operation, and measurement technique and its limitations were not discussed.

[1]It should also be noted that the standard gate-loss equation $P_G = f_{sw} \cdot Q_G \cdot V_{drive}$ is based on the same principle [24].

[2]It is possible that the observation of the co-energy loss had been veiled by another apparent discrepancy in conventional loss analysis in relation to measured and theoretical switching energies: the externally measured $i_{DS} \cdot v_{DS}$ underestimates the turn-ON loss and overestimates the turn-OFF loss [20]. This was eventually clarified in several works by distinguishing between channel and drain currents [6], [20], [21], [25].

[3]We prefer the term co-energy as it provides the much-needed distinction for this energy component; the terms charge loss and Q_{oss} loss are often confusing and do not set themselves apart from the stored energy in a meaningful way.

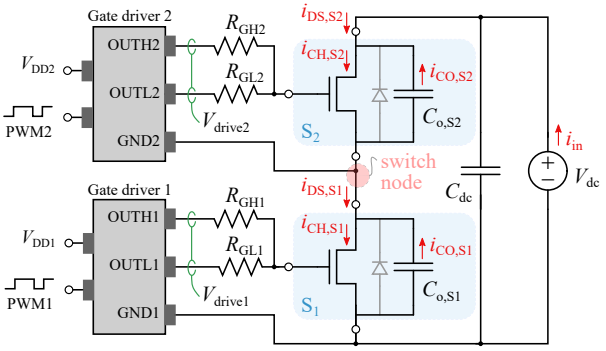

Fig. 6. No-load topology consists of a half-bridge circuit where the bottom and top devices (S_1 and S_2) are switched complementarily with asymmetrical gate driving. A dc-link capacitance C_{dc} is placed very close to the switching devices. C_o of each device is represented as a capacitance in parallel with drain–source terminals. Any third-quadrant operation (denoted by the diodes) is inhibited due to the non-existence of any load current at the switch-node.

Although all these research works have addressed either the $Q_o \cdot V_{dc}$ loss or the importance of large-signal measurements, a comprehensive synthesis of these ideas with a clear focus on basic hard-switching operation is missing. In particular, a theoretical explanation as to how the co-energy loss takes place in a simple inverter leg needs to be clarified from a circuit perspective. And finally, we believe a comparison of the QV curves based on small-signal and Sawyer–Tower methods to that of related to hard switching could bring forth additional insights. We address these considerations in as follows.

IV. Analysis of the No-load Circuit and Experimental Verification

In this section, stored energy and co-energy concepts are applied to a no-load circuit. The circuit is then experimentally verified and utilized to generate QV curves.

A. No-load Circuit

The no-load circuit is shown in Fig. 6. The switch node is left floating, involving zero load current. The channel, drain, and output-capacitance currents are also shown [7]. The circuit features an asymmetrical gate-driving scheme, the importance of which is described in Section VI-C. The operation of the circuit can be analysed through six operating modes as Fig. 7 illustrates, where important waveforms during switching transitions are given in Fig. 8. Throughout this work, the following is maintained for the external gate-driver resistor values: $R_{GH1} = R_{GH2}$ and is denoted by the general term R_{GH}; $R_{GL1} = R_{GL2}$ and is denoted by the general term R_{GL}.

During the turn-on transition of S_1 (t_1–t_2 in Fig. 7), no current commutations take place as there is zero load current. Therefore, as soon as v_{GS} approaches $V_{GS(th)}$, the voltage commutation commences, unlike in a DPT circuit [7].[4] Since the channel of S_1 is now conducting (although not fully enhanced as Fig. 1(a) depicts), its output capacitance $C_{o,S1}$ discharges through its own channel, adding a current component $i_{CO,S1}$ to the channel. While this self-discharge happens in S_1, the output

[4]An analysis for the DPT circuit can be found in our previous work [7].

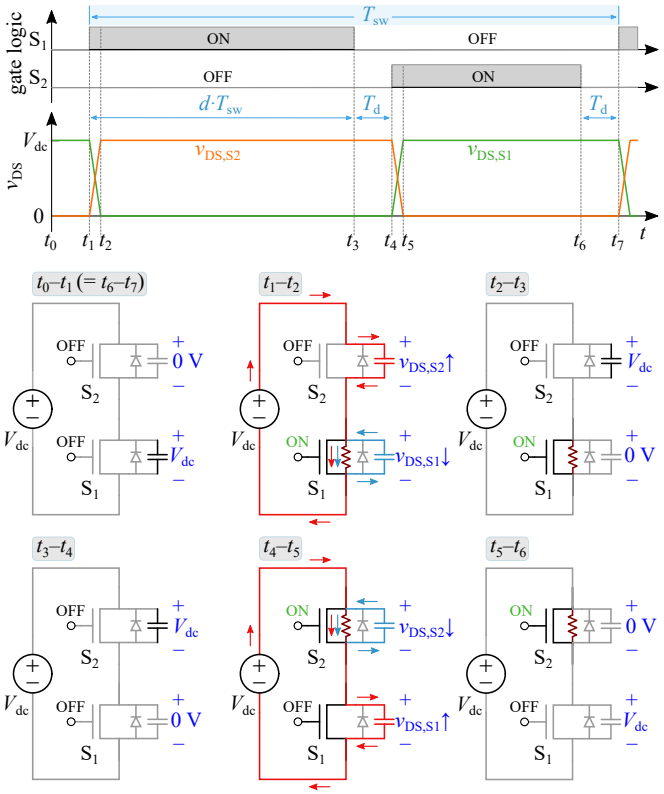

Fig. 7. Operation of the no-load circuit can be divided into six modes, where $T_{sw} = 1/f_{sw}$ is the switching period, T_d is the dead-time, and d is the duty ratio. During the dead-times (t_0–t_1 and t_3–t_4), as well as during the on-periods (t_2–t_3 for S_1 and t_5–t_6 for S_2), no charge or discharge process related to output capacitances occurs; such a process would only take place during switching transitions. During t_1–t_2, $C_{o,S1}$ gets discharged while $C_{o,S2}$ gets charged; during t_4–t_5, $C_{o,S1}$ gets charged while $C_{o,S2}$ gets discharged. The fixed voltage source V_{dc} acts as the energy source for the two charging processes.

capacitance of S_2, $C_{o,S2}$, gets charged by the dc voltage source; this causes an additional second current component to pass through the channel of S_1 such that $i_{CH,S1} = i_{CO,S1} + (-i_{CO,S2})$ (see Fig. 8). For this charging process of $C_{o,S2}$, the channel of S_1 acts as a resistance (variable in nature as both Fig. 1(a) and Fig. 5 describe) in series with the dc voltage source; thus, this loss is independent of the value or nature of R_{ch}.

At the end of the voltage commutation period, two loss components are identified in the channel of S_1, which are caused solely due to device capacitances. The first is the discharge loss of $C_{o,S1}$ that is equal to the energy that was stored in $C_{o,S1}$ at off-state (equal to $E_{o,S1}$). The second is the loss incurred due to the charging of the output capacitance of the complementary device ($C_{o,S2}$) that is equal to the co-energy of $C_{o,S2}$, $E^*_{o,S2}$. Thus, the total energy loss in S_1 at its turn-on transition in the no-load circuit—due to the charging and discharging of device output capacitances—is equal to

$$E_{\text{on-C}_o\text{(NL)}} = E_{o,S1} + E^*_{o,S2}. \tag{4}$$

And for the case where $S_1 = S_2$, which is the typical case in half-bridge configurations, using (3) and (4) we get

$$E_{\text{on-C}_o\text{(NL)}} = E_o + E^*_o = Q_o V_{dc}. \tag{5}$$

The same analysis can be carried out for the turn-on transition of S_2 (t_4–t_5 in Fig. 7). As Fig. 7 illustrates, all the other

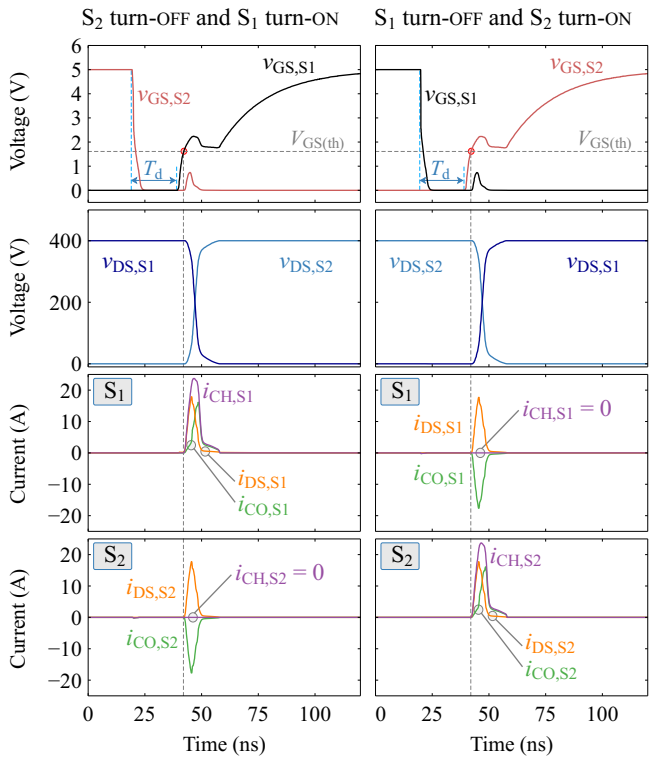

Fig. 8. *LTspice* simulation results showing the turn-ON and turn-OFF transitions of S_1 and S_2 in the no-load circuit, where V_{dc} = 400 V, f_{sw} = 100 kHz, d = 0.5, T_d = 20 ns, R_{GH} = 20 Ω and R_{GL} = 0.1 Ω. During the dead-times, the voltages $v_{DS,S1}$ and $v_{DS,S2}$ stay at their before-dead-time values as there is no load current to charge or discharge the switch-node capacitance. When a device turns ON, it experiences a channel current larger than its drain current due the discharge of its output capacitance; the already-OFF device experiences zero current in its channel.

operating modes in the circuit are inactive[5] modes that do not involve any charge–discharge processes of C_o, and therefore assume no change in v_{DS}, as Fig. 8 also shows. Thus, the total energy

$$E_{in(NL)} = 2\, Q_o V_{dc} \tag{6}$$

drawn from the dc voltage source in each switching cycle is completely dissipated as heat. It is important to note that during practical operation, C_{dc} acts as the dc voltage source that supplies the energy ($E_{on\text{-}C_o(NL)}$) required for a single switching transition. C_{dc} then gets charged by the external voltage source before the next switching transition takes place; this process however involves negligible energy loss. This is because as C_{dc} is very large, the voltage drop caused by the extraction of an amount of charge equal to Q_o is insignificant.

The above analysis shows that the input energy in the no-load circuit is independent of 1) the time variations of R_{ch} and its on-state value $R_{DS(on)}$ (see also Section VI-C); 2) dead-time and duty cycle, as energy-transfers take place only during voltage-commutation periods; and 3) switching frequency, as long as Q_o does not show any frequency dependence [4].

[5]Note: during the dead times, the topology does not allow any transfer of charge, and thus, only one device holds off the dc-link voltage. The reasons are as follows: 1) as the circuit involves no load-current, any external charging or discharging does not take place through the switch node; 2) the input supply V_{dc}, for example during t_3–t_4, cannot charge $C_{o,S1}$, as $C_{o,S2}$ is holding a voltage equal to V_{dc}, not allowing a charging current to commence.

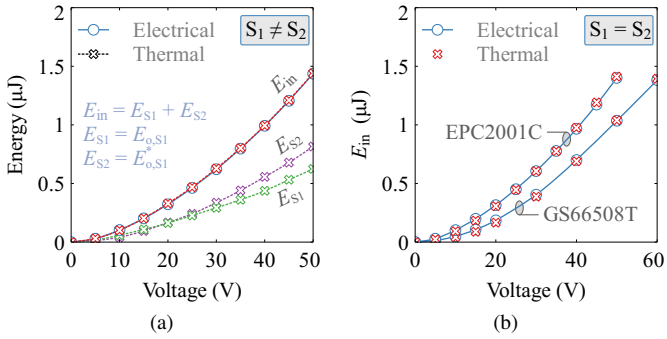

Fig. 9. (a) Experimental verification of the presented concepts with thermal loss measurements. Energies dissipated in S_1 and S_2 in the no-load circuit during a switching cycle are denoted as E_{S1} and E_{S2}, respectively. Here, S_1 is an EPC2001C GaN HEMT; and S_2 is an EPC2037 GaN HEMT, which has negligible C_o compared to an EPC2001C device, making $E_{o,S2} = E^*_{o,S2} \approx 0$. Thus, E_{S1} represents the stored energy in $C_{o,S1}$, whereas E_{S2} represents the co-energy of $C_{o,S1}$. Conditions: $R_{GH} = R_{GL}$ = 1.1 Ω, f_{sw} = 500 kHz, T_d = 40 ns. The addition of thermally measured E_{S1} and E_{S2} agrees well with electrically measured total input energy, E_{in}, validating the presented concepts. (b) Thermal validation for the case of $S_1 = S_2$, which is the basis for the proposed QV measurement method: one half-bridge is made with EPC2001C devices while the other is made with GS66508T devices. Conditions: $R_{GH} = R_{GL}$ = 2.2 Ω, f_{sw} = 500 kHz and T_d = 40 ns.

Moreover, $E_{in(NL)}$ is not affected by any C_o-hysteresis as it is determined by the final Q_o value.

B. Verification of Concepts and Experimental Approach

Here, we experimentally demonstrate the existence of co-energy using the thermal loss estimation method utilized in our previous work [7]. Then using the same thermal technique, we verify the electrical measurements used in the proposed QV measurement technique, before applying it to compare commercial devices, as presented in Section V.

A special device selection in the no-load circuit is used to verify the co-energy concept. If the devices are chosen such that $Q_{o,S2}|_{V_{dc}} \ll Q_{o,S1}|_{V_{dc}}$, then $E_{o,S2} = E^*_{o,S2} \approx 0$. This means that the total loss in S_1, E_{S1}, is only caused by $E_{o,S1}$ and the total loss in S_2, E_{S2}, is only caused by $E^*_{o,S1}$. Thus, S_1 and S_2 become two physically-separate heat sources representative of $E_{o,S1}$ and $E^*_{o,S1}$, respectively. Two GaN HEMTs were selected where $Q_{o,S1}|_{50\,V}$ = 30.55 nC (EPC2001C) and $Q_{o,S2}|_{50\,V}$ = 0.59 nC (EPC2037). Then the energy losses in S_1 and S_2 were calculated [7] and are plotted in Fig. 9(a). The separation of $E_{o,S1}$ and $E^*_{o,S1}$ shows the existence of co-energy loss.

The developed QV measurement method is based on the measurement *average* electrical input power P_{in} (see also the Appendix C). The input energy E_{in} is then calculated by P_{in}/f_{sw}. Electrically measured E_{in} for the circuit in Fig. 9(a) shows very good agreement with the total input energy calculated based on the thermal measurements (= $E_{S1} + E_{S2}$), thus validating the accuracy of electrical measurements. Measurements for two no-load circuits for the case where $S_1 = S_2$ are shown in Fig. 9(b); the thermal and electrical results show excellent agreement. Using (6), we obtain that $P_{in} = E_{in} \cdot f_{sw} = 2\, Q_o V_{dc} \cdot f_{sw}$. Thus, the QV curves are obtained by calculating Q_o at each sweep-step of V_{dc} as

$$Q_o = \frac{1}{2}\frac{P_{in}}{V_{dc} f_{sw}}. \tag{7}$$

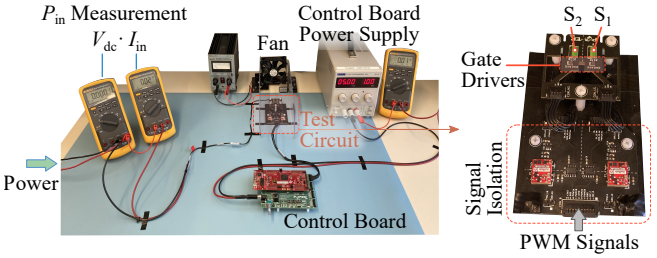

Fig. 10. Experimental test system with electrical measurements. The gate-driver supply voltages and the PWM signals were isolated using two dc-dc converters and digital-signal-isolators.

TABLE I
DEVICES EVALUATED IN SECTION V

Label	Part Number	Voltage (V)	Current Rating (A) @ T_C = 25 °C
GaN-1	TPH3212PS	650	27
GaN-2	GS66508T	650	30
SiC-1	MSC060SMA070B	700	39
SiC-2	C3M0065090D	900	36
Si-1	STW38N65M5	650	30
Si-2	NTHL110N65S3F	650	30

Fig. 10 shows the experimental system with measurement equipment, the control unit and one of the no-load circuits. A *MAGNA Power* TSD800-18/380 power supply was used to supply dc-link voltages up to 400 V. The dc-link capacitance was 2.2 μF. The average input current I_{in} and voltage are measured using Fluke 87V digital multimeters (DMMs).

V. Main Results: *QV* Curves in Hard Switching

The developed measurement method was applied to compare GaN, SiC, Si devices with similar voltage and current ratings (Table I), and the obtained *QV* curves are shown in Figs. 11 to 13, respectively. The datasheet-based curves (marked by solid black lines) were obtained by integrating C_{oss} with v_{DS}. The Sawyer–Tower measurements (marked by red and blue dashed lines for charge and discharge processes) were performed at an excitation frequency of 100 kHz and a peak voltage (V_p) of 400 V [4].

The hard-switching results for the two GaN devices closely follow the datasheet values (with a maximum deviation of 9 % for device GaN-2 at 100 < V_{dc} < 200 V). The Sawyer-Tower curves also exhibit good agreement up to 300 V but tend to deviate moderately beyond that. Sawyer–Tower results for device GaN-1 from a previous work have shown that the hysteresis pattern emerges suddenly after V_p > 100–150 V [4], when different V_p values were tested; in Fig. 11(a), the hard-switching curves do not show any abrupt deviation in their trends above 100 V, affirming that $E_{in(NL)}$ depends only on the final Q_o value and that C_o-hysteresis has no effect on it. The tests were repeated using different samples of the devices[6] and the results (marked by additional circles on the two plots in Fig. 11) further confirm the validity of the measurements.

[6]The variation between the results for different pairs (2x of GaN-1 and 3x of GaN-2) of samples is not significant and is around 2–5 % for the whole range of V_{dc}. The slight differences are due to the small variations in device properties between different samples of the same product, as small-signal measurements in Fig. 14 indicate.

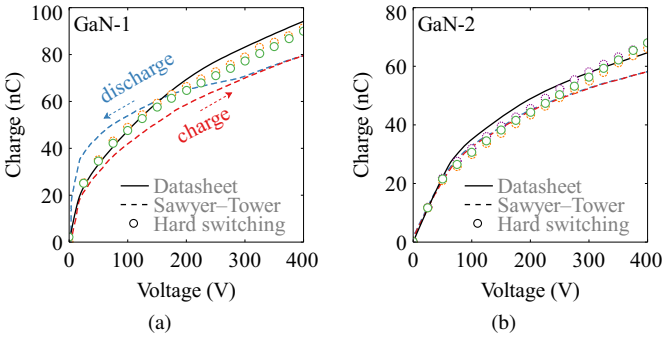

Fig. 11. Experimental *QV* curves obtained using the proposed hard-switching method (marked by circles) for two different GaN HEMT device types, where f_{sw} = 100 kHz, d = 0.5 and T_d = 100 ns. Results are also compared with curves based on datasheets and Sawyer–Tower method. To show that the results are repeatable, a device-sampling was carried out for (a) two pairs (solid and dashed circles) of GaN-1 devices with R_{GH} = R_{GL} = 47 Ω, and (b) three pairs (solid, dashed, and dotted circles) of GaN-2 devices with R_{GH} = 10 Ω and R_{GL} = 1 Ω. For both device types, the results for hard-switching follow the datasheet-based values quite closely.

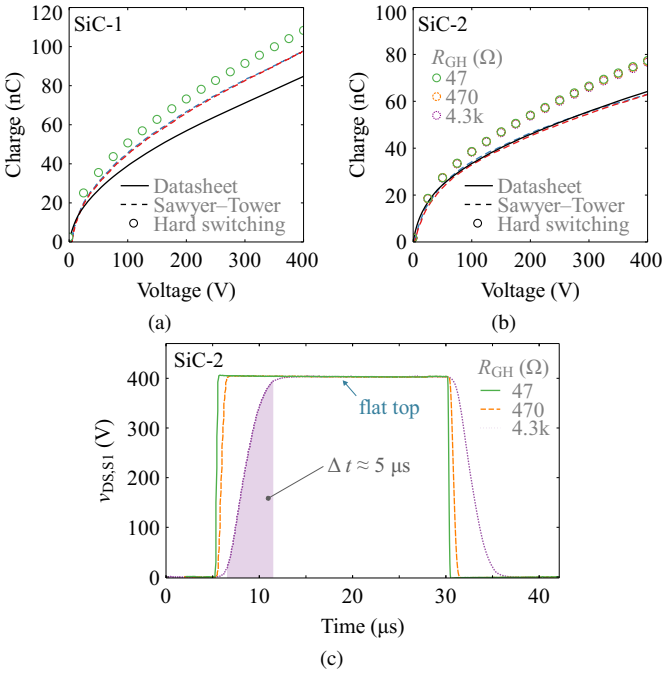

Fig. 12. Experimental *QV* curves obtained using the proposed hard-switching method for two different SiC device types: under the conditions (a) f_{sw} = 100 kHz, d = 0.5, T_d = 100 ns, R_{GH} = 47 Ω and R_{GL} = 1 Ω; (b) f_{sw} = 20 kHz, d = 0.5, T_d = 2 μs and R_{GL} = 1 Ω. For device SiC-2, the switching speed in hard switching was varied by changing R_{GH}: 47 Ω (solid circles), 470 Ω (dashed circles) and 4.3 kΩ (dotted circles). The results show that the *QV* curves exhibit no dependence on switching speed. The slowing down of the switching speed with increasing R_{GH} can be seen in (c) the v_{DS} waveforms.

Results for the two SiC devices (Fig. 12) indicate that the Q_o values in hard switching is considerably different in comparison to the datasheet values. Although the Sawyer-Tower measurements agree well with the datasheet curve for device SiC-2, it is not the case for device SiC-1. This shows that neither the small-signal curves nor the large-signal soft-switching curves can correctly predict the actual charge capacity for hard switching. To understand if this difference is due to any high-frequency effects, as hard switching is achieved at large dv/dt values, the switching speed was decreased for

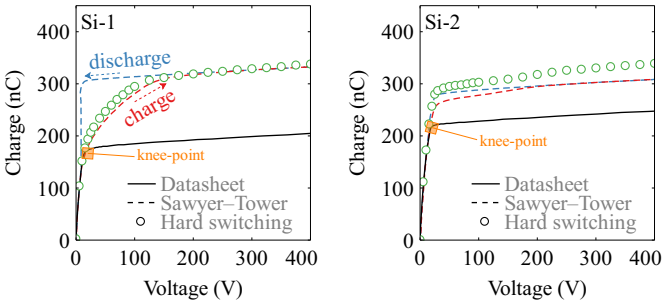

Fig. 13. Experimental QV curves obtained using the proposed hard-switching method for two different Si-SJ device types are compared with respective curves based on datasheets and Sawyer–Tower method. The conditions are: d = 0.5, T_d = 100 ns, R_{GH} = 47 Ω and R_{GL} = 1 Ω. A low f_{sw} of 20 kHz was used to keep the power dissipations in the devices low as the Si-SJ devices have much larger Q_o values (≈ 300 nC at 400 V).

device SiC-2 by increasing the R_{GH} value up to two orders of magnitude as Fig. 12(b) shows. The corresponding v_{DS} waveforms are given in Fig. 12(c), where the slowest speed (for R_{GH} = 4.3 kΩ) corresponds to charge and discharge times of ≈ 5 μs each, which matches in frequency for a 100-kHz excitation in the Sawyer–Tower circuit. The results indicate that Q_o stays unchanged with switching speed. One possible explanation of this lies in the topological difference between hard-switching and Sawyer–Tower circuits. In the former, C_o is allowed a considerable fully-OFF state after the transient (where v_{DS} is settled at V_{dc}), which allows the stored charge to settle to the dc electric field created by V_{dc}. In the latter on the other hand, the OFF-state voltage is continuously changing and a flat top in v_{DS} is never achieved, and the charges are subjected to a time varying electric field; this might create a different overall charge capacity in C_o.

For the Si-SJ devices (Fig. 13), the Q_o values in hard switching are significantly larger in comparison to the datasheet values beyond the knee-point voltages (marked by squares). The Sawyer-Tower curves lie close to the hard-switching curves, indicating that the large-signal behaviour of C_o is considerably different to datasheet values. This observation is in agreement with the works by Zulauf et al. [3], [14], where the Sawyer–Tower measurements showed considerable discrepancies for Q_o, in comparison to datasheet values. Our results further indicate that the hard-switching charge capacity in Si-SJ devices could vary from the Sawyer–Tower curves as can be observed for device Si-2.

VI. Discussion

A. Interpretation of the Results

As datasheet values could differ from the tested batch of devices, small-signal CV measurements on five samples of each device type were performed. The measured small-signal output charge values for each transistor, normalized with respect to their corresponding datasheet values, are plotted in Fig. 14. All devices are contained within a 10 % variation from datasheet values, apart from device Si-1, which shows a 20 % variation. The results for the samples of the GaN devices and device SiC-2 stay very close to their datasheet values.

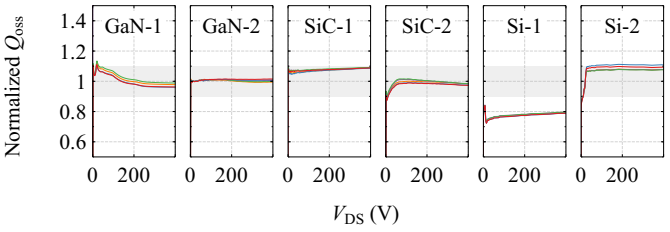

Fig. 14. Small-signal measurement results showing normalized Q_{oss} values (measured/datasheet) for a dc sweep of V_{DS} = 0 to 400 V. Five samples of each tested device-type were measured with a Keysight B1505A curve tracer at an excitation frequency of 100 kHz. The light-grey areas correspond to a ± 10 % variation from the datasheet values.

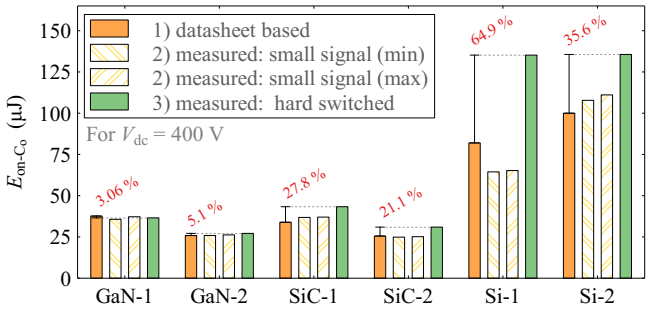

Fig. 15. Comparison of measured (hard-switching method) and datasheet-based $E_{on\text{-}C_o}$ at 400 V for the devices studied in this work. $E_{on\text{-}C_o}$ based on the small-signal measurements in Fig. 14 are also shown (only the cases with lowest and highest Q_{oss} values are included). The percentage differences between the datasheet and measured hard-switching results are not negligible for SiC and Si-SJ devices. This directly affects the accuracy of E_{on} as $E_{on\text{-}C_o}$ is a load-independent contribution–see (8).

Fig. 15 compares $E_{on\text{-}C_o}$ at 400 V for the tested devices, evaluated using the small-signal methods (datasheet and measured) and the hard-switching method (measured). For the two GaN-devices, all three methods show good agreement with differences contained within 5 %. On the other hand, for example, device SiC-2 shows a 21.1 % difference between datasheet and measured hard-switching values, which translates to a 0.211 × 25.56 μJ = 5.39 μJ difference in energy loss; and at a f_{sw} of 200 kHz, this means an additional power loss of 1 W, which is not negligible. The devices Si-1 and Si-2 show significant differences around 64.9 % and 35.6 % between methods 1 and 3, which cannot be explained even by the measured small-signal values. These results reveal two very important aspects about the large-signal behaviour of Q_o in hard switching:

1) highly dependent on the semiconductor technology and the structures used within a given technology.
2) for certain devices, it cannot be predicted correctly with either the datasheet, or the large-signal curves related to soft-switching operation.

In addition, the proposed measurement technique could be utilized to identify if Q_o exhibits any frequency- or dv/dt-dependence in hard switching by changing the value R_{GH} to control the switching speed (as was shown for device SiC-2). For a device without such dependence, the energy related to the turn-ON process stays independent of R_{GH}, and hence of the switching speed, as Fig. 16 shows. This is because, although the increase of R_{GH} increases the time duration of the voltage commutation period, at the same time it decreases

TABLE II
COMPARISON OF E_{ON} AND $E_{ON\text{-}C_o}$ VALUES OF THE TESTED DEVICES

Device	Conditions for E_{on} Measurement [Datasheet]						E_{on} (μJ) [Datasheet][1]	$E_{on\text{-}C_o}$ (μJ) [Datasheet, at 400 V][2]	$E_{on\text{-}C_o}$ (μJ) [Measured, at 400 V][3]
	V_{dc} (V)	I_L (A)	$V_{drive\text{-}OFF}$ (V)	$V_{drive\text{-}ON}$ (V)	R_G (Ω)	L (μH)			
GaN-1	-	-	-	-	-	-	-	37.7	36.6
GaN-2	400	15	0	6	10/1	40	47.5	25.8	27.2
SiC-1	470	20	−5	20	4	-	130	33.9	43.3
SiC-2	400	20	−4	15	2.5	65.7	343	25.6	31
Si-1	400	20	-	-	10	50	260	82	135.2
Si-2	-	-	-	-	-	-	-	100	135.6

[1]Value directly given in datasheets; [2]Value calculated based on C_{oss} curve from datasheet; [3]Measured using experimental no-load circuit.

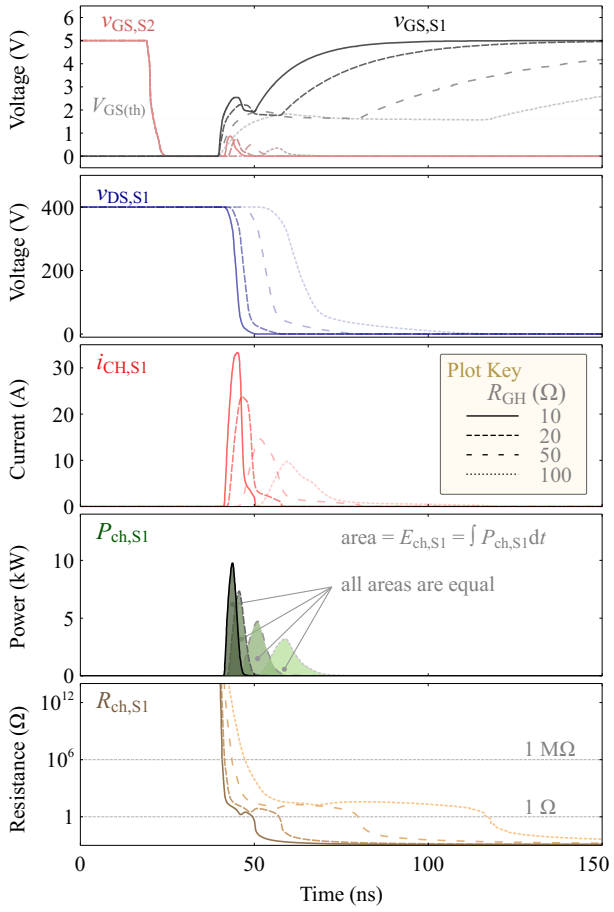

Fig. 16. *LTspice* simulation results detailing the turn-ON transient of S_1 in the no-load circuit for different switching speeds, achieved by sweeping the value of R_{GH}. GS66508T GaN HEMT spice models were used. With increasing R_{GH}, the duration of the transient increases, whereas the peak values of the channel current decreases. This effectively makes the energy dissipation in the channel, $E_{ch,S1}$, the same for all R_{GH} values (i.e., $E_{ch,S1}$ is independent of the switching speed). The relevant variation of channel resistance is also shown, which also has no effect on $E_{ch,S1}$. Conditions: V_{dc} = 400 V, f_{sw} = 100 kHz, d = 0.5, T_d = 20 ns and R_{GL} = 0.1 Ω.

the peak value of the channel current. The variation of the channel resistance is also shown in Fig. 16.

B. Hard-Switching Losses in Loaded Conditions

In a hard-switching half-bridge with an external load current i_L at the switch node, the total turn-ON energy loss in a FET can be described as

$$E_{on} = E_{on\text{-}C_o} + E_{on\text{-}VI}. \tag{8}$$

The existence of $E_{on\text{-}C_o}$ depends on the topology and its value is solely determined by the Q_o value of the device. For example, in the DPT circuit [Fig. 3(c)], $E_{on\text{-}C_o}$ for S_1 is equals to $E_o + E_o^*$. However, the turn-ON process for S_2 is different and depends on T_d: if T_d is large enough, S_2 achieves ZVS turn-ON (facilitated by i_L), and hence, $E_{on\text{-}C_o}$ would be zero; and if T_d if too small, then S_2 undergoes a partial-ZVS condition.

In contrast to $E_{on\text{-}C_o}$, the quantity $E_{on\text{-}VI}$ is a result of the product between v_{DS} and i_L [25]. For a constant load current ($i_L = I_L$), the magnitude of $E_{on\text{-}VI}$ mainly depends on the value of dv_{DS}/dt during the miller plateau, which can be controlled by the gate-driver circuit [21]. For this case, a quadratic equation in I_L can be used to model E_{on} as

$$E_{on} = a + b \cdot I_L + c \cdot I_L^2, \tag{9}$$

where $a = E_{on\text{-}C_o}$, and b and c are circuit-specific coefficients. Such a modelling is used in the recent work by Guacci et al. to experimentally characterize hard-switching losses in 200-V Si and GaN devices [16].

Table II lists E_{on} (given in datasheet) and $E_{on\text{-}C_o}$ (calculated based on datasheet C_{oss} and measured) of the tested devices. For most of the devices, $E_{on\text{-}C_o}$ is a considerable portion of E_{on}. And the lower the value of I_L, the less significant the $E_{on\text{-}VI}$ component in (8) becomes, increasing the significance of $E_{on\text{-}C_o}$ in the total turn-ON loss. Thus, it is important that manufacturers provide large-signal Q_o (or C_o) curves in device datasheets. It is favourable that the E_{on} parameter (if given) is separated into two parts in the datasheets as given by (8); this distinguishes between the effects of C_o and I_L on the turn-ON loss. These efforts help the circuit designers to make an informed decision on device selection for optimum designs.

C. Gate-driver Voltage and Asymmetrical Gate Driving

For the experiments in Section V, the gate-driver supply voltages were set to $V_{DD1} = V_{DD2} = V_{DD} = 5$ V (see Fig. 6). For all the tested devices $V_{GS(th)} < 5$ V. In addition, we tested V_{DD} values of 9, 12 and 15 V for the devices Si-1 and SiC-2. The resulting QV curves matched well with the 5-V case; as different V_{DD} values create different $R_{DS(on)}$ values, this further proves the independence of $Q_o \cdot V_{dc}$ on $R_{DS(on)}$ for a given device.

Asymmetrical gate driving is extremely important, especially for GaN devices, when R_{GH} values of 10 Ω or lower are used. The low Q_G of GaN devices and low R_{GH} values create very large dv_{DS}/dt values for the device that turns ON. This could eventually cause a false triggering (partial turn-ON event)

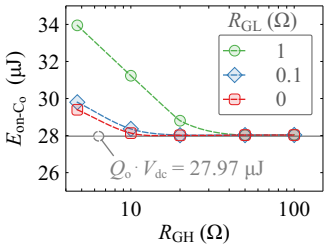

Fig. 17. Simulation results for device GaN-2 showing how $E_{\text{on-C}_\text{o}}$ could deviate from expected values due to the cross-conduction events resulting from the false triggering of the OFF device. The lower the value of R_{GH}, the greater the dv_{DS}/dt value, increasing the current due to Miller effect. By using an asymmetrical gate driver with low R_{GL} values, this could generally be solved. The reason $E_{\text{on-C}_\text{o}} > Q_o V_{dc}$ for $R_{GH} < 10$ and $R_{GL} = 0$ is the internal-gate-terminal resistance (= 1 Ω) used in the device simulation model.

in the OFF-state device, which results in a cross-conduction in the inverter leg.[7] As Fig. 17 shows, such a condition causes for observations where $E_{\text{on-C}_\text{o}} > Q_o V_{dc}$: the increased switching energy observed by Guacci et al. [16] for a 200-V Si device in zero-current operation is due to this reason. Asymmetrical gate driving with a very-low R_{GL} value is required to keep the OFF-state device's gate-voltage spikes below $V_{GS(th)}$. In all our experiments this was achieved by using an R_{GL} of 1 Ω. Although Fig. 17 suggests using an $R_{GL} \leq 0.1$ Ω for device GaN-2, 1 Ω was enough as the current limit of the gate driver inhibits very large dv_{DS}/dt conditions. The minimum value of T_d is limited by the value of R_{GL}; T_d should be large enough to fully accommodate the turn-OFF transients of v_{GS}.

VII. Conclusion

In this article, we have revisited the fundamental concepts of hard switching and shown the distinct role of device output capacitance in creating switching losses. It was shown that when a device is fully hard switched during its turn-ON process, a fixed energy loss is incurred in the device channel equal to $Q_o \cdot V_{dc}$, which is separated into co-energy and stored energy components of the top and bottom device output capacitances. Based on this theoretical foundation, an easy-to-implement technique to obtain large-signal QV curves of the output capacitance of FETs under actual hard switching was presented. The method uses a no-load half-bridge circuit with asymmetrical gate driving and is independent of dead-time and device $R_{DS(on)}$. It was then applied to characterize commercial Si, SiC and GaN devices. The results showed that for certain device types, neither the datasheet nor the Sawyer–Tower values represent the actual charge capacity of C_o in hard-switching operation. We emphasize that

- $Q_o \cdot V_{dc}$ is the proper measure for a fully hard-switched device, such as the switching device in a DPT circuit.
- small-signal values of charge or stored-energy related to C_o do not necessarily translate to large-signal values.
- large-signal behaviour of Q_o in soft-switching operation, does not correspond to the large-signal behaviour in hard switching. This is because the two operations subject C_o to fundamentally different charging mechanisms.

[7]The spikes in the gate voltage $v_{GS,S2}$ observed in Fig. 16 are due to this high dv_{DS}/dt condition and can be seen to reduce with increasing R_{GH}.

Appendix A
Sawyer–Tower Technique

The Sawyer–Tower circuit is traditionally used for the characterization of ferroelectric capacitors [36], [37]. Recently, the technique has been adapted to study hysteresis losses in the output capacitance of FETs [3], [10], [11]. A summary of the technique is presented as follows.[8]

A signal generator, high-voltage amplifier, fixed linear capacitor (termed as the reference capacitor C_{ref}), and the device under test (DUT) constitute the circuit as shown in Fig. 2(b) (Section II). The technique relies on only two voltage measurements: v_{IN} and v_{REF}.[9] In this circuit, the DUT is effectively a capacitance equal to C_o for positive v_{DS} values [11], as the gate–source terminals of the DUT are shorted, i.e., $v_{GS} = 0$ V. The signal-generator output is amplified by the high-voltage amplifier to a large-signal voltage (v_{IN}), which is then applied to the series combination of the DUT and C_{ref}. The circuit creates a dc bias (V_{REF}) across C_{ref} in steady state [11], causing v_{DS} to vary between 0 V and V_p [see Fig. 2(b)]. Thus, the ac voltage ($v_{ref} = v_{REF} - V_{REF}$) across C_{ref} is proportional to the variation of charge in C_{ref}: $\Delta Q_{ref} = C_{ref} \cdot v_{ref}$. As the same ac current flows through C_{ref} and C_o in steady state, we get

$$Q_o \propto C_{ref} \cdot v_{ref}. \tag{10}$$

The QV curves are obtained by mapping Q_o to v_{DS} (= $v_{IN} - v_{REF}$) in time domain, using a computer program such as MATLAB® or Origin.

Appendix B
Mathematical Derivation of Co-energy Loss

Fig. 18 shows a circuit where a capacitance C (either linear or non-linear) is being charged by an ideal dc voltage source V_{dc}, in series with a resistance R. The current (i) and charge (Q) delivered from the supply are both functions of time t. The charging process starts at $t = 0$ and ends at $t \to \infty$. The following analysis shows that the final energy components in the process are functions of only V_{dc} and the charge capacity of C, which we denote as Q_1.

The total energy supplied by the dc voltage source at the end of charging is,

$$E_{in} = \int_0^\infty V_{dc} \cdot i\, dt = V_{dc} \int_0^\infty i\, dt. \tag{11}$$

Realizing that $\int_0^\infty i\, dt$ is equal to the total charge (Q_1) supplied by the source at the end of the charging process, we get

$$E_{in} = Q_1 \cdot V_{dc}. \tag{12}$$

This indicates that the energy supplied by the source is independent of R and depends only on V_{dc} and Q_1.

Next, the energy stored in the capacitance is calculated as

$$E_C = \int_0^\infty v_C \cdot i\, dt. \tag{13}$$

[8]For additional details on the operation of the circuit and its usage, please refer to our recent work on this technique [11].

[9]The two voltages can be measured with a standard oscilloscope and passive voltage-probes: in our experiments we used a Tektronix MDO3104 oscilloscope (1 GHz) accompanied by TPP1000 passive voltage probes (1 GHz). The probe-end uses the MMCX square-pin adapter 131-9717-xx.

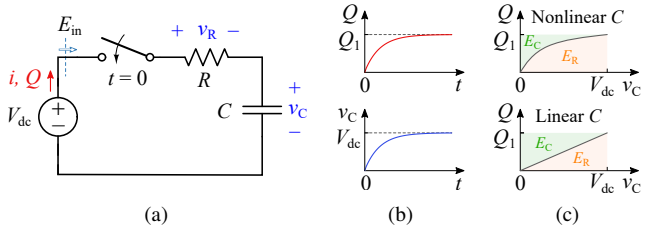

Fig. 18. (a) An ideal dc voltage source, V_{dc}, charges a capacitance C in series with a resistance R. The circuit is turned ON at $t = 0$. At $t \gg RC$, (b) the charging process is complete with $v_C = V_{dc}$, and a total charge equal to Q_1 is supplied by the source, which is stored in C. (c) QV curves showing the energy distribution for linear and nonlinear C.

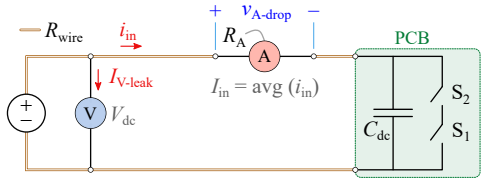

Fig. 19. Placement of voltage and current measurement units to measure the average input power. R_{wire} is the dc resistance of wires from the dc power supply to the dc-link capacitance C_{dc}; R_A is the insertion resistance of the ammeter and was measured to be 1.8 Ω in the mA-range setting.

Using the definition of current, i.e., $i = dQ/dt$, a variable change is applied for the above integral as $idt = dQ$, where $Q = 0$ at $t = 0$, and $Q = Q_1$ at $t = \infty$. This gives

$$E_C = \int_0^{Q_1} v_C \cdot dQ. \tag{14}$$

Finally, the energy lost in R is calculated as

$$\begin{aligned} E_R &= \int_0^{\infty} v_R \cdot i\, dt = \int_0^{\infty} (V_{dc} - v_C) \cdot i\, dt \\ E_R &= \int_0^{\infty} V_{dc} \cdot i\, dt - \int_0^{\infty} v_C \cdot i\, dt. \end{aligned} \tag{15}$$

Identifying that the two integrals on the RHS of (15) are given by (12) and (14), we get

$$E_R = E_{in} - E_C = Q_1 \cdot V_{dc} - E_C \tag{16}$$

Since $Q_1 \cdot V_{dc}$ is the total area in a QV plot [see Fig. 4(a)], according to (16) E_R, can be expressed as

$$E_R = \int_0^{V_{dc}} Q dv_C. \tag{17}$$

The integral on the RHS in (17) is defined as the co-energy of C. This shows that the energy loss in R is independent of the value of R, but depends only on the QV curve of C.

Appendix C
Measurement and Practical Considerations

1) Average Current and Voltage Measurements: The current i_{in} drawn from the input power source contains high-frequency components at $2f_{sw}$ and above. Thus, if the measurement hardware does not contain any averaging process before ADC sampling, the measurements could be erroneous. We have used a Fluke 87V DMM as it contains an analogue 2-pole filter (with poles around 5 Hz) that implements an accurate averaging process before the ADC sampling takes place. Both the average voltage and current measurements have very good accuracies and high resolutions (see Table III).

TABLE III
Specifications of Average Measurements with Fluke 87V DMM

Measurement	Type	Used Range	Resolution	Accuracy[1]
V_{dc}	Average	0–600 V	0.1 V	± (0.05 % + 1)
I_{in}	Average	0–60 mA	0.01 mA	± (0.2 % + 4)

[1] For a measured value M, a ± (X % + Y) accuracy means an absolute error of ± [$0.01MX + (Y \cdot$ Resolution)].

TABLE IV
Datasheet-provided Drain—Source Leakage Currents

Device	I_{DSS} (μA)		V_{DS} (V) [$v_{GS} = 0$ V]
	Typical	Max	
GaN-1	3	30	650
GaN-2	2	50	650
SiC-1	-	100	700
SiC-2	1	100	900
Si-1	-	1	650
Si-2	-	10	650

2) Loading Effects of DMMs: As shown in Fig. 19, the voltage measurement takes places before the current measurement. This means that the ammeter measures the actual current going into the circuit. Therefore, any current ($I_{V\text{-leak}}$) flowing through the voltmeter does not affect the measurements. Furthermore, the voltage-drop across the line ($= i_{in} \cdot (R_A + R_{wire})$) is negligible compared to the measured input voltage range used in this work (50–400 V). Note that the average input current I_{in} is less than 30 mA in our measurements (based on our observations, the instantaneous current i_{in} could have a peak of two times I_{in}). An example can be considered: for $i_{in} = 0.1$ A and $R_{wire} = 3$ Ω, which is an extreme case, $v_{A\text{-drop}} = 0.1 \times (1.8 + 3) \approx 0.5$ V. Thus, line resistances have negligible effects on the measurement results.

3) Probing of the Switch Node: It is advised not to place voltage probes across the switch-node during the P_{in} measurements; the added capacitance of the probe increases the switch-node capacitance and hence the measured I_{in}. The error in $\Delta Q_o/\Delta v_{DS}$ could be quite significant at high v_{DS} values where device capacitances could be as low as 50 pF; the probe capacitances are usually around 5–10 pF. For instance, we have observed an 8 nC increase in Q_o at 400 V for device SiC-2 when a Tektronix THDP0200 differential voltage probe was placed across the switch-node.

4) Drain–Source Leakage Current (I_{DSS}): In the OFF state of a device, I_{DSS} creates a power loss equal to $I_{DSS} \cdot V_{dc}$. Ideally, this loss should be deducted from P_{in} to get the C_o related losses. For the devices tested in this work, I_{DSS} is less than 100 μA (see Table IV), where the measured I_{in} is around 3–20 mA at $V_{dc} = 400$ V. Generally, typical I_{DSS} values are much lower than the maximum values. Thus, the effects of I_{DSS} are negligible. In addition, we measured I_{DSS} of several samples of the tested devices using a power device analyser; all values were below 20 μA for $V_{dc} = 400$ V.

5) Selection of dc-link Capacitance: The value of C_{dc} should be large enough not to cause a large drop in voltage during the switching transients. A large ripple voltage in C_{dc} could cause additional losses in the circuit due its equivalent series resistance (ESR). Also, Class-II multilayer ceramic

(MLC) capacitors such as X7T and X7R types exhibit a decrease in their capacitance at high voltages [11]; this should also be considered when selecting the type and value of C_{dc}.

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