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Hybrid Modular Multilevel Converter for Pumped Hydro Storage Applications

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Dedicated to my family

Abstract

Energy balance in a power system must be maintained at all times, regardless of the variations in generation and consumption. Power systems have been historically developed to ensure such a balance, based on fairly good daily load curve prediction. Even today, the dominant share of electrical energy is generated by base generating units, large coal- or nuclear power plants, operated at constant power output for optimal efficiency. Daily profile of discrepancy between the consumption and the base generation varies with social and industrial activities. Large Pumped Hydro Storage Plants (PHSPs) are introduced to the power system to accumulate the excess of energy during the low demand (nighttime), and provide it back during the high demand (daytime).

As we are heading towards the Renewable Energy Sources (RES)-dominated power systems, their stochastic nature and ever-increasing share are altering the daily load curve of the system, increasing the need for highly-flexible energy storage capacities. Further, the PHSP strategy of accumulating the energy during the nighttime to provide it back during the daytime is not profitable anymore in the deregulated market, where high volumes of RES-generated energy can become available midday. Thus, from both engineering and commercial interests, PHSPs must be enabled to respond faster and provide a higher array of ancillary services to keep up the pace with the power system evolution. While we are witnessing scaling-up of alternative energy storage facilities, e.g. battery-based, PHSPs readily offer by far the highest share of energy storage capacity in the power system. High flexibility can be yielded through conversion of existing fixed-speed PHSPs to variable speed operation, by decoupling the machine from the grid by an AC-AC power electronics converter.

The Modular Multilevel Converter (MMC) is inherently scalable to the voltage and power levels of machines typically found in large PHSPs, i.e. 6 kV to 20 kV and 80 MVA to 400 MVA, and this thesis is based around its implementation in variable speed PHSP retrofitting scenario. To operate the machines originally designed for sine-wave grid power supply, at rated torque and over the entire frequency range for the highest flexibility, the MMC-specific internal energy balancing actions have to be performed in a machine-friendly way. Starting from the two extreme reference designs – a Half-Bridge (HB)-only Indirect MMC (I-MMC) requiring prohibitively high Common-Mode (CM)-voltage stress to the machine, and a Full-Bridge (FB)-Active Front-End (AFE)-based I-MMC providing CM-voltage-free operation at prohibitively high losses, the thesis introduces two novel control- and design methods based on Hybrid MMC (H-MMC) AFE, where hybrid refers to a mix of HB and FB Submodules (SMs) in each branch.

The first method offers reduced CM-voltage stress to the machine, at 56 % FB SM share in the AFE stage, while not compromising the grid-code compatibility. The CM-voltage reduction is achieved by reducing DC link voltage reference with machine speed down to 50 %, requiring less-severe balancing action in the Low Frequency (LF) operating region. The second method enables CM-voltage-free rated-torque machine operation over the full speed range, through down-to-zero DC link voltage reduction capability, requiring 62 % FB SM share in the AFE. DC link voltage reference variation with the machine speed in Variable Speed Drive (VSD) MMC eliminates the need for CM-voltage-based balancing intervention in the LF region. While this method cannot operate at unity grid-side power factor below rated machine speed, thus not offering full grid-code compatibility, a design trade-off is offered between the attainable power factor range and FB SM share. A comprehensive set of test scenarios has been performed for each of the newly introduced methods to verify the validity.

Keywords pumped hydro storage, hydroelectric power generation, hybrid modular multilevel converter, mixed cell converter, AC-DC converter, converter control, retrofit

Résumé

L'équilibre énergétique d'un système électrique doit être maintenu à tout instant, quelles que soient les variations de la production et de la consommation. Les systèmes électriques ont été historiquement développés pour assurer un tel équilibre, sur la base d'une assez bonne prévision de la courbe de charge quotidienne. Aujourd'hui encore, la part dominante de l'énergie électrique est produite par des unités de production de base, de grandes centrales à charbon ou nucléaires, exploitées à puissance constante pour une efficacité optimale. Le profil quotidien de l'écart entre la consommation et la production de base varie en fonction des activités sociales et industrielles. De grandes centrales hydroélectriques de pompage (PHSP) sont introduites dans le système électrique pour accumuler l'excès d'énergie pendant la faible demande (la nuit) et le restituer pendant la forte demande (le jour).

Alors que nous nous dirigeons vers des systèmes électriques dominés par les sources d'énergie renouvelables (SER), leur nature stochastique et leur part toujours croissante modifient la courbe de charge quotidienne du système, ce qui augmente le besoin de capacités de stockage d'énergie hautement flexibles. De plus, la stratégie PHSP consistant à accumuler l'énergie pendant la nuit pour la restituer pendant la journée n'est plus rentable sur le marché déréglementé, où de gros volumes d'énergie produite par les SER peuvent devenir disponibles en milieu de journée. Par conséquent, d'un point de vue technique et commercial, les PHSPs doivent être en mesure de réagir plus rapidement et de fournir un éventail plus large de services auxiliaires pour suivre le rythme de l'évolution du système électrique. Alors que nous assistons à la mise à l'échelle des installations de stockage d'énergie alternative, par exemple à base de batteries, les PHSP offrent de loin la plus grande part de capacité de stockage d'énergie dans le système électrique. Une grande flexibilité peut être obtenue en convertissant les PHSP à vitesse fixe existantes en un fonctionnement à vitesse variable, en découplant la machine du réseau par un convertisseur électronique de puissance AC-AC.

Le convertisseur modulaire multi-niveaux (MMC) est intrinsèquement adaptable aux niveaux de tension et de puissance des machines que l'on trouve généralement dans les grands PHSP, c'est-à-dire 6 kV to 20 kV et 80 MVA to 400 MVA, et cette thèse est fondée sur sa mise en œuvre dans un scénario de rétrofit de PHSP à vitesse variable. Pour faire fonctionner les machines conçues à l'origine pour l'alimentation sinusoïdale du réseau, au couple nominal et sur toute la plage de fréquence pour une flexibilité maximale, les actions d'équilibrage de l'énergie interne spécifiques à la MMC doivent être réalisées de manière adaptée pour la machine. En partant de deux conceptions de référence extrêmes - un MMC indirect (I-MMC) uniquement en demi-pont (HB) nécessitant une tension de mode commun (CM) prohibitive pour la machine, et un I-MMC fondé sur un front actif (AFE) en pont complet (FB) fournissant un fonctionnement sans tension de mode commun avec des pertes prohibitives, la thèse présente deux nouvelles méthodes de contrôle et de conception fondées sur l'AFE du MMC hybride (H-MMC), où hybride fait référence à un mélange de sous-modules (SMs) HB et FB dans chaque branche.

La première méthode permet de réduire la tension de la machine, avec une part de 56 % de SM FB dans l'étage AFE, sans compromettre la compatibilité avec le code de réseau. La réduction de tension CM est obtenue en réduisant la référence de tension de liaison CC avec une vitesse de machine réduite jusqu'à 50 %, ce qui nécessite une action d'équilibrage moins sévère dans la région de fonctionnement à basse fréquence (LF). La deuxième méthode permet un fonctionnement de la machine sans tension CM à couple nominal sur toute la plage de vitesse, grâce à une capacité de réduction de la tension de liaison CC jusqu'à zéro, nécessitant une part de 62 % de FB SM dans l'AFE. La variation de la référence de tension de liaison CC en fonction de la vitesse de la machine dans le MMC à entraînement à vitesse variable (VSD) élimine la nécessité d'une intervention d'équilibrage fondée sur la tension CM dans la

région LF. Bien que cette méthode ne puisse pas fonctionner à un facteur de puissance unitaire côté réseau en dessous de la vitesse nominale de la machine, n'offrant donc pas une compatibilité totale avec le code de réseau, un compromis de conception est offert entre la plage de facteur de puissance atteignable et la part de FB SM. Un ensemble complet de scénarios d'essai a été réalisé pour chacune des méthodes nouvellement introduite afin d'en vérifier la validité.

Mots clés: stockage hydroélectrique par pompage, production d'énergie hydroélectrique, convertisseur multiniveau modulaire hybride, convertisseur à cellules mixtes, convertisseur AC-DC, contrôle du convertisseur, rétrofit.

Acknowledgments

A clear conscience is the sure sign of a bad memory.
Mark Twain

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Lausanne, October 2021
Miodrag Basić

List of Abbreviations

3PH	Three-Phase
AC	Alternating Current
AC/AC	Three-Phase to Three-Phase
AFE	Active Front-End
CCC	Circulating Current Control
CFSM	Converter-Fed Synchronous Machine
CHB	Cascaded H-Bridge
CM	Common-Mode
D-MMC	Direct MMC
DC	Direct Current
DC/3-AC	Direct to Three-Phase
DDSRF	Double Decoupled Synchronous Reference Frame
DFIM	Doubly-Fed Induction Machine
EMF	Electromotive Force
FB	Full-Bridge
FOC	Field-Oriented Control
FVSC	Flexible Voltage Support Control
GCC	Grid Current Control
H-MMC	Hybrid MMC
HB	Half-Bridge
HF	High Frequency
HV	High Voltage
HVDC	High Voltage Direct Current
I-MMC	Indirect MMC
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
INU	Inverter Unit

KVL	Kirchhoff's voltage law
LF	Low Frequency
LSC-PWM	Level-Shifted Carrier PWM
LVRT	Low Voltage Ride-Through
MAS	Maximum Area Saturator
MMC	Modular Multilevel Converter
MV	Medium Voltage
NLM	Nearest-Level Modulation
OPP	Optimized Pulse Patterns
PEBB	Power Electronic Building Block
PEL	Power Electronics Laboratory
PHSP	Pumped Hydro Storage Plant
PLL	Phase-Locked Loop
PS	Proportional Saturator
PSC	Phase-Shifted Carrier
PSC-PWM	Phase-Shifted Carrier PWM
PV	Photo-Voltaic
RES	Renewable Energy Sources
SFC	Static Frequency Converter
SM	Submodule
SMC	Submodule Cluster
SRF	Synchronous Reference Frame
STATCOM	Static Synchronous Compensator
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TSO	Transmission System Operator
VS	Variable Speed

VSC Voltage Source Converter
VSD Variable Speed Drive

WRSM Wound-Rotor Synchronous Machine

List of Symbols

C_{SM}	SM capacitance
C_{br}	Branch capacitance
L_{br}	Branch inductance
L_{g}	Grid equivalent inductance
M_{br}	Branch mutual inductance
N_{SM}	Number of submodules per branch
P^*	Active power reference
P	Active power
Q^*	Reactive power reference
Q	Reactive power
R_{SM}	SM equivalent resistance
R_{br}	Branch resistance
R_{g}	Grid equivalent resistance
S	Apparent power
V_{DC}	DC link voltage
V_{SM}	Submodule voltage
ω_{g}	Fundamental grid angular frequency
ω_{s}	MMC AC-side electrical angular frequency
ψ_{g}	Grid current-phasor angle
ψ_{s}	MMC AC-side current-phasor angle
ψ_{dq}	dq angle
θ_{g}	Grid voltage-phasor angle
θ_{s}	MMC AC-side voltage-phasor angle
φ_{g}	Grid voltage to current phase shift
φ_{s}	MMC AC-side voltage to current phase shift
$f_{\mathrm{sw,app}}$	Apparent switching frequency
f_{sw}	Switching frequency
f_g	Fundamental grid frequency
i_{c}	Circulating current
i_g	Grid current
k_{br}	Branch inductance coupling coefficient
m_p, m_n	Branch modulation indices
m_{s}	AC-side modulation index
$v^*_{\mathrm{g\{a,b,c\}}}$	GCC voltage references

v_{CM}	Common Mode voltage
v_c	Summed phase-leg inserted voltage
v_g	AC grid voltage
v_s	Differential phase-leg voltage
$v_{C\Sigma p}$, $v_{C\Sigma n}$	Summed branch capacitor voltages
$v_{C\Sigma}^{\Delta}$	Differential phase-leg capacitor voltage
$v_{C\Sigma}^{\Sigma}$	Summed phase-leg capacitor voltage

Contents

1 Introduction

1.1 Background

It is well known that, to maintain equilibrium in a classical power system, rate of electrical energy generation must equal rate of consumption at all times. Consumption is varying throughout the day, being significantly higher during daytime than during night (**Fig. 1.1**). On the other hand, big thermal power plants, e.g. coal and nuclear, that are globally still the dominant source of electrical energy [1], feature start-up times measured in hours or days and, once online, operate at highest efficiency while outputting constant power. Energy balancing is thus achieved by utilizing a number of such big thermal plants as base generation units of constant power output, a number of more flexible plants, e.g. gas powered and hydro, as balancing units of variable power output, and a number of reserve units for cases of big system-level disturbances.

One way to reduce the share of balancing and spinning reserve units in the overall installed generation capacity is to establish flexible grid-scale energy storage systems. By storing excess of energy from constant output plants at times of lower demand, typically throughout the night, these units can offer peaking power to the grid during high demands, typically during the daytime.

1.1.1 Fixed speed Pumped Hydro Storage Plants (PHSPs)

PHSP is a grid-connected energy storage system, consisting of two water reservoirs at different elevations – an upper and a lower one. By pumping water from the lower to the upper reservoir, using a grid-supplied electrical machine and a hydraulic pump, the energy is stored in potential form. Delivery of energy is realized by reverting water back to the lower reservoir, through a turbine circuit. A turbine-coupled electrical generator provides electrical energy back to the grid. The reservoirs' volume and altitude difference determine the amount of stored energy. The first units were constructed during 1890s, in the mountain regions of Switzerland and Italy. A significant deployment of PHSPs, however, only began in 1960s to 1970s, when their flexibility was recognized as a good complement to base-load coal and nuclear power plants. [4]–[6].

Traditionally, PHSP units are used for pumping during off-peak hours, allowing the base-load plants to operate at constant, optimal power point, regardless of current consumption. During peak hours, PHSPs are operated in generation mode, to balance production-demand and provide "peak-shaving".

From today's perspective, PHSP represents a well-established and proven technology, having been in global use for decades. With an overall efficiency typically ranging between 70 and 85%, they offer the most efficient means of storing electrical energy at large scales [4], [5]. Featuring short start-up times and high flexibility, these have by far the highest share in installed capacity compared to all

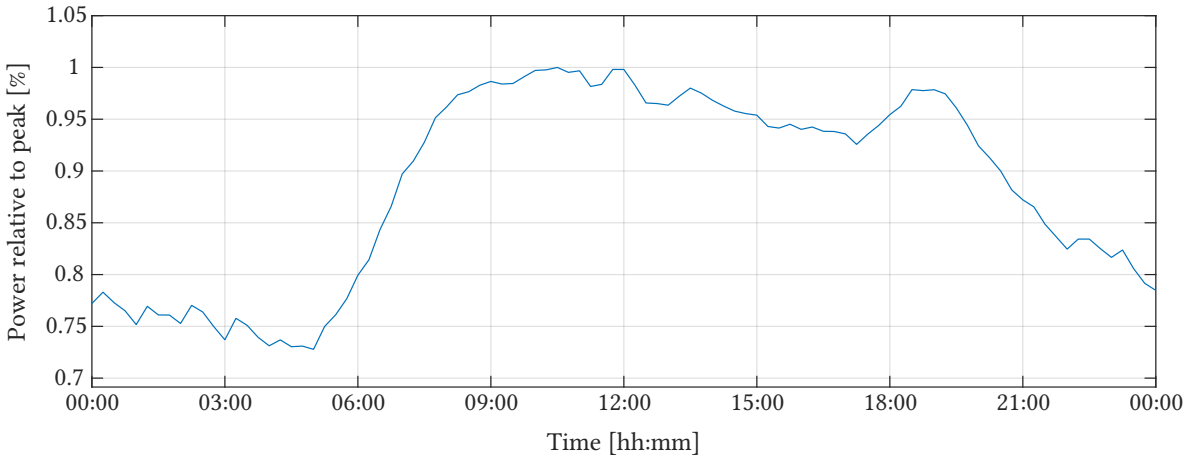


Fig. 1.1 Daily energy consumption profile in Switzerland, on a winter working day of 2018. The plot is based on aggregated energy data of the Swiss control block, and is accurate to 2 % [2], [3].

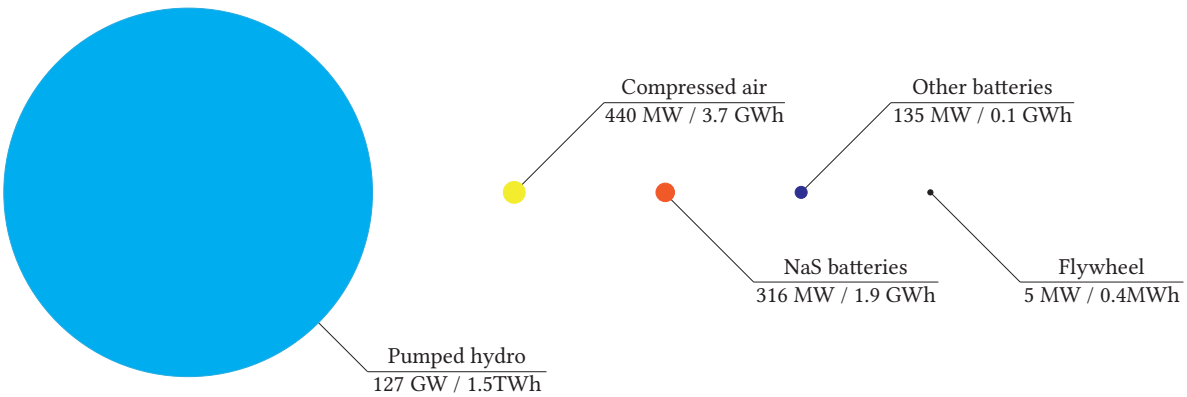


Fig. 1.2 Global electrical energy storage share. Installed generating power and storage capacity are shown for dominant storage systems. *Other* batteries include: Li-ion, Ni-Cd, lead-acid and Redox.

energy storage techniques, reaching over 127 GW , or 3% of installed generating capacity worldwide (**Fig. 1.2**) [7], [8].

A fixed-speed PHSP is based on a grid-connected synchronous machine, and a specific hydraulic system. The synchronous machine is connected to transmission grid through a step-up transformer and thus operates at fixed frequency. The hydraulic system is most commonly realized utilizing a reversible pump-turbine unit of Francis type [5]. In this case, a change of operating regime (generation/pumping) requires a change of direction of rotation. Another option is a so-called ternary system, where turbine and pump are built as separate units and connected to a single synchronous machine. This approach enables independent optimization of both pump and turbine, along with faster switch-over between operating regimes, as direction of rotation can be the same.

1.1.2 Power system evolution and deregulation

Supported by various government incentives from economical side and advances in power electronics from technological side, Renewable Energy Sources (RES) have gained a significant market share in recent years. The most dominant in terms of installed power, Photo-Voltaic (PV) and wind sources,

are however inherently stochastic, highly dependent on weather conditions, and thus challenging to predict over longer time horizons. With a total share in globally installed generation capacity currently being more than 1591 GW for wind, and 855 GW for PV plants [9], these intermittent sources require a counter-balance in form of a reliable and fast storage system, for production-load balancing. Regarding Transmission System Operators (TSOs) scheduling models, it has been shown that the share of installed wind plants has a direct impact on the amount and type of the required operation reserves [10], [11].

An additional challenge to traditional operation of PHSPs has been set by gradual deregulation of once centralized electrical energy markets. This change has, in general, introduced wholesale markets for exchange of electrical energy and services:

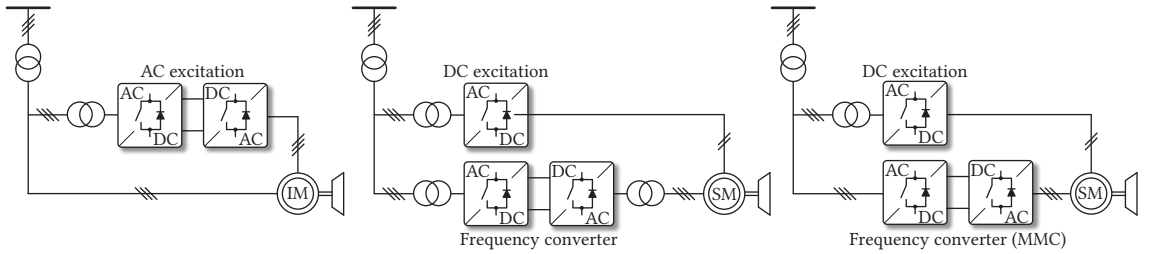
- *Spot* market, for day-ahead exchange.
- *Intraday* market, compensating for deviations in planned day-ahead production and consumption schedules [12].
- *Futures* market, managing energy exchange over longer time horizons.
- *Ancillary* markets, organized for various services, e.g. frequency regulation, reactive power control, voltage support during Low Voltage Ride-Through (LVRT), power reserves.

Nowadays, as a consequence of the aforementioned penetration of volatile RES, considerable peaks and dips in production and demand can occur throughout the day (PV, wind) and night (wind). With prices being formed based on demand and offer on the market, the once fairly estimable daily cost curve of electrical energy can now be significantly deviated. Profitability of traditional operation of PHSPs is directly proportional to the ratio of peak and off-peak cost of electrical energy on the spot markets. On the other hand, ancillary services markets are considerably enlarged due to the aforementioned effects of RES uncertainties.

In this sense, the introduction of power electronic converters to PHSPs can provide higher control flexibility, increasing their presence and making them more competitive in ancillary markets. Advances in power electronics, in both switching devices blocking capabilities and topologies, have enabled converter power ratings that match some PHSP machines' ratings [13]. Implementation of such converters to PHSPs is possible for both Converter-Fed Synchronous Machines (CFSMs), and Doubly-Fed Induction Machines (DFIMs) (**Fig. 1.3**). In both cases, they offer decoupling of machine's mechanical speed from the grid frequency.

In practice, this means a machine can be controlled in a way to operate at variable mechanical speed, while maintaining fixed electrical frequency at grid terminals, which offers multiple benefits:

- Expansion of power-frequency regulation to both pumping and turbine mode.
- Higher overall efficiency, through operation at the optimal speed from the hydraulic system perspective, for a given head level.
- Extension of operating range, in terms of maximal to minimal head ratio, compared to fixed-speed PHSPs – 1,45 compared to 1,25 is claimed in [5].
- Instantaneous injection of considerable power spikes to the grid in case of disturbances, by exploiting rotor as a flywheel. The use of this feature effectively allows for reduction of grid spinning reserve [14].



(a) (b) (c)

Fig. 1.3 Variable speed PHSP configurations: (a) DFIM; (b) CFSM; (c) CFSM realized with Modular Multilevel Converter (MMC). The main advantage of the MMC is the scalability to machine- and grid-side voltage level without the need for additional transformers.

- Reduced hydraulic stress and, consequently, expected increase in hydraulic machines' lifetime.

By offering both energy at the spot market and ancillary services like power-frequency regulation, a PHSP could increase overall profitability. Some researchers suggest that this strategy could potentially double the daily income of a PHSP, utilizing certain heuristic algorithms to decide on capacity placement between the markets [10], [15]. In a real-world example of the Portuguese power system, secondary regulation reserve is shown to be the most important source of revenue for a PHSP [16].

1.2 Variable speed PHSPs

1.2.1 Doubly-fed induction machines

The DFIM configuration (**Fig. 1.3**) is the most consolidated technology used for variable speed PHSPs, especially for machines of high power ratings, exceeding 100 MW. The advantage of this configuration is the fact that the converter has to be rated at only a fraction of the nominal power of the machine to achieve usually ±10% of speed variation [14]. This, in turn, provides roughly ±30% of pumping power variation [14]. Converters of these power levels are technologically available, making DFIM an already established technology. A list of variable speed units over 100 MW known to the author, currently in operation or under construction, is given in **Tab. 1.1** , based on [4], [17]–[20].

However, in contrast to the aforementioned variable speed operation benefits, several drawbacks exist for the DFIM configuration.

- The wound rotor is complex in design, introduces slip rings as an additional maintenance issue, and has a limited power rating according to cooling capabilities of the machine, limiting the available speed range and starting torque.
- Limited starting torque, in return, may be insufficient when switching between generation and pumping, requiring a dewatering procedure, a time- and resource-consuming task.
- During grid faults resulting in short circuit, low voltage ride-through (LVRT) proves to be challenging for DFIM. High rotor currents in short circuit conditions reach values well above rated, overloading the converter. In case rotor supply converter enters protected mode, rotor windings are short-circuited, and DFIM acts as a consumer of reactive power, negatively contributing to LVRT situation.

Tab. 1.1 Variable speed PHSP units above 100 MW currently in operation or under construction, arranged by individual power rating. Only two installations are based on CFSM: Grimsel being a retrofit and Galgenbichl comprising new machines and converters.

Name	Country	Type	Turbine power [MW]	No. of units	Total power [MW]
Kazunogawa	Japan	DFIM	460	2	920
Okawachi	Japan	DFIM	395	2	790
Frades 2	Portugal	DFIM	390	2	780
Venda Nova 3	Portugal	DFIM	380	2	760
Okukiyotsu 2	Japan	DFIM	340	1	340
Omarugawa	Japan	DFIM	330	3	990
Okutataragi	Japan	DFIM	320	2	640
Omarugawa	Japan	DFIM	310	1	310
Shiobara	Japan	DFIM	309	1	309
Fengning	China	DFIM	300	2	600
Goldisthal	Germany	DFIM	265	2	530
Linth-Limmern	Switzerland	DFIM	250	4	1000
Tehri	India	DFIM	250	4	1000
Kyogoku	Japan	DFIM	230	2	460
Avče	Slovenia	DFIM	180	1	180
Nant de Drance	Switzerland	DFIM	150	6	900
Takami 2	Japan	DFIM	103	1	103
Hatta	United Arab Emirates	DFIM	125	2	250
Grimsel 2	Switzerland	CFSM	100	1	100
Galgenbichl	Austria	CFSM	80	2	160

- Special requirements for DFIM during LVRT thus require the machine to be controlled for some time during the fault. In practice, this means that converter must be oversized to withstand the requirement.
- If an existing PHSP is considered for conversion to DFIM variable speed unit, one must account for additional mechanical requirements imposed by the more complex and heavier rotor.

1.2.2 Converter-fed synchronous machines

Recent advances in power electronics semiconductors and topologies have enabled full-size converter between machine and grid to be considered [13], in what is called CFSM configuration (**Fig. 1.3**). The use of a standard synchronous machine decoupled from the grid through the converter offers considerable benefits compared to DFIM solution.

- Retrofit of an existing fixed-speed PHSP, if available cavern space permits, is possible without replacement of the machine itself.
- Higher rotational speeds can be achieved, thanks to a less complex rotor design.
- Rated torque is available from zero speed.
- No need for additional pole-reversing installation, as a change in rotating magnetic field

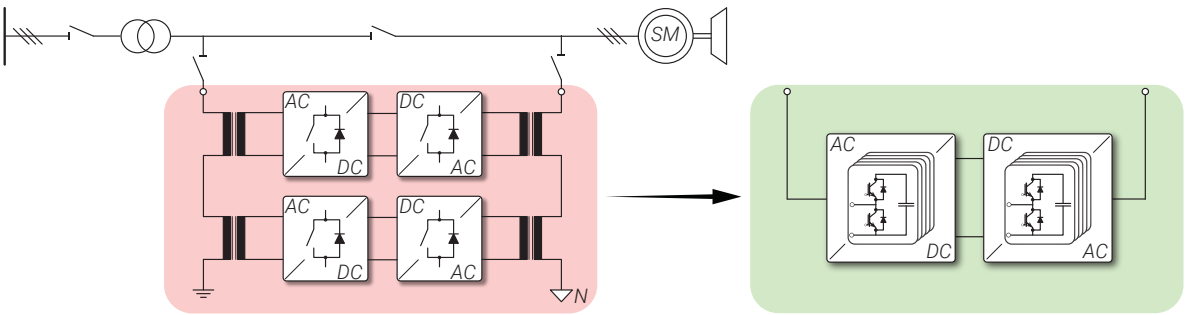


Fig. 1.4 CFSM layout in Grimsel 2 PHSP, including converter bypass switch for turbine regime and interleaved converters (red); equivalent prospective MMC solution is depicted to the right (green).

direction of the machine can be achieved through appropriate change in converter output voltage references.

- Better short-circuit handling, as converter current limit can be freely parametrized and, for instance, limited to 1 p.u. Plant behavior is not defined by the nature of the machine.
- Considerable reactive power can be delivered to the grid in support of LVRT situations.
- Static Synchronous Compensator (STATCOM) functionality – reactive power is supplied from the converter, and available even when the machine is at standstill. In case of new installations, machine can be designed for higher power factor, i.e. more compact size.

1.2.3 Power range of interest

The field of interest of this thesis falls into the large-PHSP power range, as in **Tab. 1.2**. The absolute majority of installed variable speed units in this range of power ratings are DFIM, with only two CFSM unit sets on the list (**Tab. 1.1**). Lower-power CFSM units, of up to 50 MW, for heads up to 250 m and flow rates of 40 m^3/h, have been proposed as a means of local balancing, to be placed in the vicinity of stochastic RES plants [18]. These power levels can be processed through readily available power electronic converter technologies.

Regarding higher-power-rated converters for CFSM units in the order of 100 MW and up, which can be found in existing PHSP installations, and are the focus of this research, there are only two installations based on CFSM currently in operation. The first is a 100 MW unit installed in Grimsel 2 power plant, located in Switzerland. The plant comprises four 90 MW/13.5 kV ternary machine units [13]. One of the machine sets has been retrofitted with a full size power electronic converter supply. The second represents a new installation in Galgenbichl power plant in Austria. The project comprises two new 80 MW/18 kV machine sets and matching converters [19], [21].

In case of Grimsel 2 retrofit project, where the original machine set has been kept, due to technical limitations in available technology, the required power has been achieved through the parallel operation of two 50 MW back-to-back monolithic multilevel converters, developed by ABB, and based on Integrated Gate-Commutated Thyristors (IGCTs). Currently available semiconductor devices in this power range do not enable both high enough voltage and current levels to match typical machine ratings, implying the use of both grid- and machine-side converter transformers. The converter layout in presented in **Fig. 1.4**. It should be noted that this form of converter stacking produces beneficial multilevel output voltage waveforms. The achieved pumping power range is 60 MW to 100 MW [13].

Tab. 1.2 Typical synchronous machine ratings in PHSP applications.

Stator voltage (line-to-line)	V_{LL} =6 kV to 30 kV
Stator current (RMS)	I_{RMS} =2 kA to 8 kA
Apparent power	S_n =80 MVA to 400 MVA

Regarding the Galgenbichl plant project, both new machines and matching converters are delivered. Thus, freedom of machine-converter group optimization is available, which has led to the 30 Hz rated machine frequency design and the world's first use of Direct MMC (D-MMC) in PHSP applications [19], [22]. As it will be shown in the following section, retrofit of existing PHSPs to the variable speed operation is the focus of this thesis, where no freedom in machine design exists. In such applications, where nominal machine- and grid-frequency are equal, Indirect MMC (I-MMC) is preferable over D-MMC [23]. However, due to topology-specific control requirements, Half-Bridge (HB)-based I-MMC imposes prohibitively high Common-Mode (CM)-voltage-stress to the machine, originally designed for sine-wave grid voltage supply. Overcoming this retrofit shortcoming of I-MMC, through PHSP-oriented design and specific control of Hybrid MMC (H-MMC)-based Active Front-End (AFE), comprising a mix of HB and Full-Bridge (FB) Submodules (SMs) in each branch, is the contribution space and the motivation of this work.

1.3 Motivations

1.3.1 Monolithic multilevel converter technology limitations

Voltage levels of 3.3 kV to 6.6 kV line-to-line are at limits of reach for majority of today's Medium Voltage (MV) converters, not considering topologies that require specific transformers and can thus achieve higher voltages, e.g. Robicon Cascaded H-Bridge (CHB) [24]. The rating can be multiplied through series connection of converter units, by means of interleaving transformers as in **Fig. 1.4**. A higher voltage rating can alternatively be achieved by stacking semiconductors within a single converter arm, as in [25]. Further increase in current rating is possible through parallel operation of such units. **Tab. 1.3** provides an overview of maximum ratings for MV monolithic Voltage Source Converters (VSCs), as advertised by some of the major manufacturers [25]–[27].

It should be noted that GE MV7's higher voltage rating is achieved through stacking of eight low voltage Insulated Gate Bipolar Transistor (IGBT) modules. The manufacturer also advertises possibility of up to 300 MW output power through parallel operation of listed units. Similarly, Siemens utilizes three three-level neutral-point-clamped converters in parallel for listed rating.

Tab. 1.3 Maximum achievable monolithic converters power ratings, as advertised by some of the major manufacturers.

Manufacturer	Model	Technology	Voltage	Power
ABB	ACS 6000	3-L IGCT	3.3 kV	36 MW
GE	MV 7	5-L IGBT	13.8 kV	37 MW
Siemens	SINAMICS SM 150	3-L IGCT	3.3 kV	30 MW

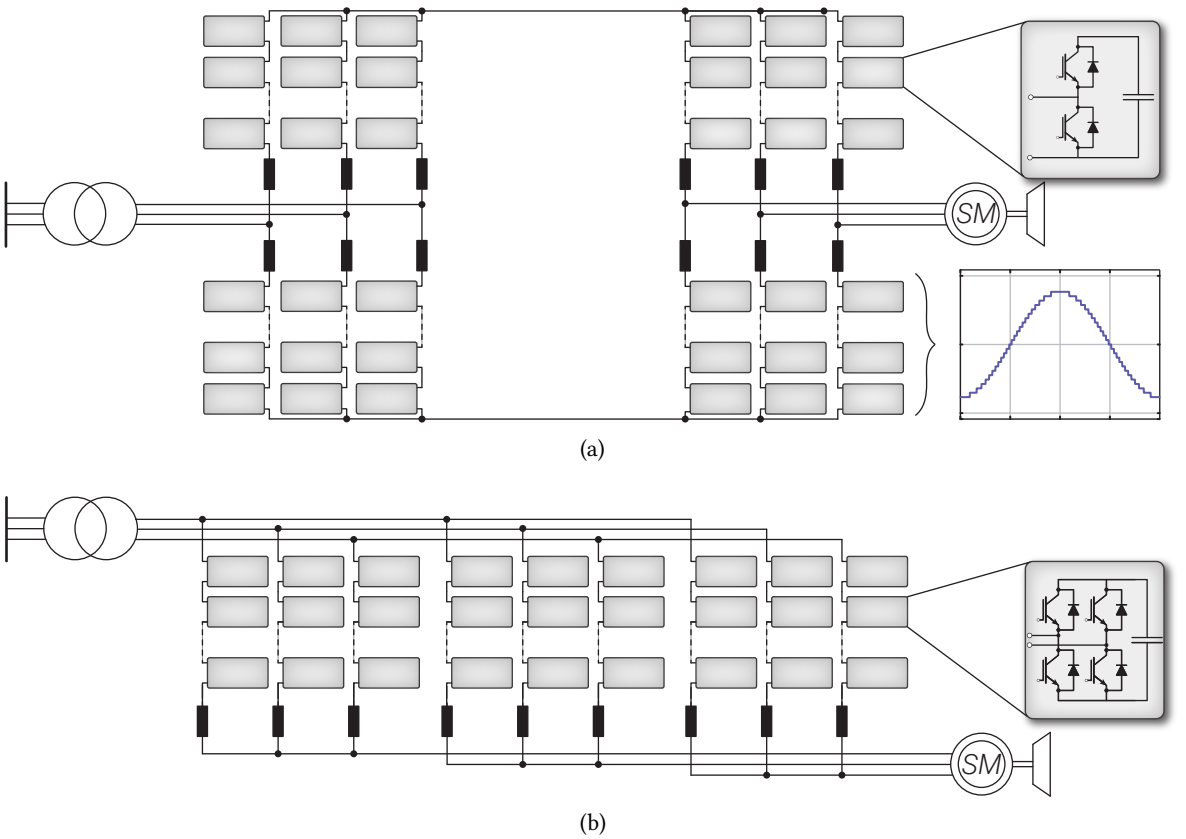


Fig. 1.5 I-MMC (a) and D-MMC (b) topologies. I-MMC is a preferable choice for retrofit applications, offering arbitrary frequency selection for grid and machine side, output voltage waveform beneficial for old machines without insulation reinforcement for converter operation; half-bridge submodules can be used. D-MMC can be considered for new installations, requiring different grid and machine side frequencies. This topology requires full-bridge submodules, and features single-stage conversion. Converter bypass has not been drawn for simplicity.

The scalability, however, is limited. As in **Fig. 1.4**, each additional series-connected converter requires a set of grid- and machine-side interleaving transformers. In case of limited number of levels, high dv/dt values can be putting extra stress to machine windings' insulation. PHSP units that are candidates for conversion from fixed- to variable speed are based on older synchronous machines designed for grid voltage waveforms. The insulation of these machines, subjected to high dv/dt stresses of VSC output, could age significantly faster and deteriorate. This limitation introduces the need for filtering, which directly translates to additional space, losses and financial requirements, with first two being critical in limited cavern spaces. Looking at the equipment displacement in [28], it can be seen that passive components, i.e. transformers and filters, take up roughly half of the total volume. Limited voltage levels require higher current ratings to achieve desired power levels. This, in turn, leads to problems with handling high short circuit currents in case of converter faults. Issues with harmonic distortions could, depending on power system regulations, require additional filtering on grid side.

1.3.2 MMC perspectives for PHSP

To achieve very high power levels implied by the PHSP application, independently of current semiconductor technology limitations, a topology with better scalability is required. The MMC is a promising alternative to monolithic converters. In scenarios where two Alternating Current (AC) systems are to be interconnected, there are two possible topologies – I-MMC and D-MMC, both depicted in **Fig. 1.5**. Indirect, or back-to-back MMC is well established in point-to-point High Voltage Direct Current (HVDC) bulk energy transmission systems. D-MMC found its use in Static Frequency Converters (SFCs) for railway interties, as an interface between three-phase 50 Hz public grid and single-phase 16.7 Hz railway supply; a reference to a recent 2×40 MW unit in Geneva, Switzerland can be found in [29]. In these established applications, MMC is interfacing two grids of fixed frequencies, while in case of PHSP, electric machine side of the installation operates at variable frequency. Variable frequency drive operation of MMC, including Low Frequency (LF) regimes, has been studied. It is shown that MMC driven machine can output significant levels of torque from zero speed onward [30]–[32].

On the other hand, the concept of MMC [33] overcomes voltage scaling limitations through simple stacking of unrestricted number of SMs in converter arms **Fig. 1.5**. The SMs can be realized as unipolar HB or bipolar FB units, using well-established semiconductor components. This strategy makes PHSP machine voltage levels reachable within a single converter, while dismissing the need for interleaving transformers. The potential use of I-MMC in hydro applications has been firstly discussed to a certain level in [24]. Further, IGCT-based D-MMC for PHSP has been proposed in [23]. The first, and so far the only, application of MMC in PHSP has been realized recently in the Galgenbichl project (**Tab. 1.1**). In this application, the machine has been designed along with the converter, and eventually rated at 30 Hz for optimization purposes [22]. D-MMC topology used in Galgenbichl project is, however, not a preferable solution when it comes to retrofit applications, where exclusively grid-frequency machines are found, as it will be discussed later [23].

1.4 MMC scaling for PHSP applications

Based on technological constraints in winding insulation and thermal management, synchronous machines currently in operation, and those expected in new installations, could roughly be fitted in the ratings displayed in **Tab. 1.2**. This is the range of interest for the converter design.

The building block of an MMC is a SM, comprising standard switching elements (IGBT or IGCT) predominantly either in HB or FB configuration, and a capacitor bank. Converter arms are realized as strings of these SMs, making very high voltage levels achievable with available semiconductor technologies.

Multilevel converter scalability depends on the choice of basic building blocks. In very high power applications, it is preferable to design a converter using the so-called Power Electronic Building Blocks (PEBBs), as for instance introduced in [34], [35]. A PEBB comprises power switches, accompanying control, communication and protection circuits, thus making for complete subsystem for easy scaling.

Regarding semiconductor technology at high power levels, the use of ”presspack” housing could be beneficial, as in case of component fault, it safely fails to short-circuit state. The converter can continue the operation utilizing redundant SMs, providing high availability. Both IGBT and thyristor-based IGCT presspacks are available for kV voltage levels. While an advantage of IGBT may be higher

Tab. 1.4 Estimated rated DC link voltage and current, based on ABB proposal [35].

Cell variant	DC link voltage	Current rating
a	5.0 kV	420 A
b	3.6 kV	583 A
c	2.5 kV	840 A
d	1.8 kV	1167 A

attainable switching frequency, IGCT offers superiorly low on-state losses, with a limitation of lower switching frequencies. As can be shown, apparent switching frequency of an HB-based MMC arm, for Phase-Shifted Carrier PWM (PSC-PWM) modulation, equals:

$$f_{\mathrm{sw,app}} = N_{\mathrm{SM}} \cdot f_{\mathrm{sw}} \tag{1.1}$$

where N_{SM} represents number of SMs per converter arm, and f_{sw} equals SM switching frequency. While (1.1) holds true for many forms of multilevel converters, an MMC has a considerably higher number of levels N_{SM}. This means a satisfactory apparent frequency can be achieved with reduced SM level f_{sw}. Yet, in high-power applications high switching frequencies are prohibitive due to thermal and efficiency constraints, and the use of Optimized Pulse Patterns (OPP) or other fundamental switching methods is more likely [36]. A high-power IGCT-based PEBB has been introduced by ABB in [34], containing two FB-type SMs, of ratings "b" from **Tab. 1.4**, in a single cabinet assembly. Three more alternatives have been given, favoring either higher voltage or higher current capability, while at fixed power rating. Based on data from [34], estimated rated Direct Current (DC) link voltage and current rating of the cells are given in **Tab. 1.4**.

MMC can be scaled up in voltage to meet machine rated voltage by stacking SMs in series, and scaled up in current rating by connecting SMs within a branch or entire branches in parallel. Considering the aforementioned PEBBs, variants b and d can be considered for MMC PHSP application. Ratings "b" were chosen as a solution already implemented by ABB. With voltage being easily scalable in MMC in contrast to the current rating, PEBB type d proves interesting as the modification option with highest current rating. **Fig. 1.6** displays achievable power-voltage range for PEBB b and PEBB d, as well as PHSP range of interest.

Since majority of the area of interest cannot be covered through the use of considered cells, parallel connection has also been investigated [37], [38]. Paralleling PEBBs or branches steepens P(V) curve, bringing MMC solution to the desired application range. It can be noted that PEBB units aiming future PHSP applications should favor higher current ratings, as this enables operation with less PEBBs or converter branches in parallel.

1.4.1 Indirect MMC for PHSP applications

As shown, MMC arm strings can be scaled to real-world PHSP ratings. I-MMC enables use of either HB or FB SMs, with a total of 12 arms due to back-to-back configuration. Due to decentralized energy storage and rather different energy management compared to monolithic VSCs, some limitations are imposed on LF operation of these converters with variable speed drives [30]. It has been shown that I-MMC can be implemented in control of drives with quadratic load, such is a pump, with very little additional control action. However, operation at constant machine torque over the complete

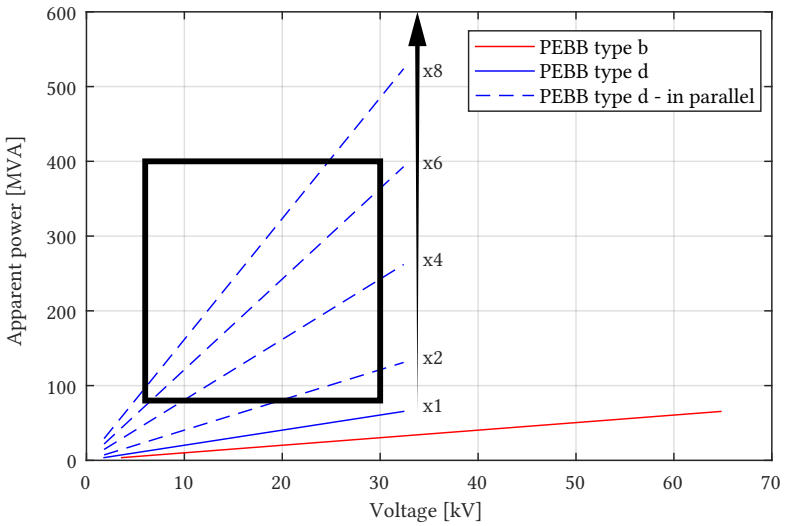


Fig. 1.6 Achievable power-voltage range of I-MMC using PEBB b, PEBB d and parallel PEBB d building blocks. The square represents PHSP range of interest.

frequency range, which would enable PHSP pumping/turbine changeover without de-watering, is only possible when SM balancing is ensured. This can be performed through additional CM voltage and balancing current injection [30], [31], at the price of high CM voltage stress to the machine and higher converter current requirements. Alternatively, CM-voltage-free operation, beneficial to the old machines designed for sine-wave supply voltage, can be enabled through variable DC link voltage operation, at the expense of utilizing lossier FB SMs within the grid-side converter stage [39]–[41].

1.4.2 Direct MMC for PHSP applications

On the other hand, D-MMC is regarded as suitable for low-speed high-torque applications, owing to output current overload capability in low-frequency range, which can be in range of 200% of nominal. This feature enables high torque to be achieved at low speeds, starting from standstill [42]. In contrast to I-MMC, D-MMC topology requires FB cells to be used, while comprising lower arm count of nine for the whole converter.

1.4.3 Indirect MMC for PHSP retrofit

The above stated makes both converter layouts suitable candidates for PHSP applications. I-MMC is, however, advantageous when it comes to retrofit applications. As opposed to D-MMC, I-MMC is the preferred topology when synchronous machine and grid rated frequencies are equal, which is the case in existing fixed-speed plants [23]. The research work thus focuses on I-MMC solution for PHSP, and in particular on the utilization of H-MMC, comprising a mix of HB and FB SMs within each branch.

The motivation for research work in this domain is to exploit the possibility of qualitative leap in PHSP performance through the implementation of MMC solution. The use of MMC technology is expected to lead towards numerous advantages:

- Increase of PHSP flexibility towards the grid side, to support further integration of RES in

power system.

- Freely scalable, transformer-less and filter-less CFSM PHSP design, as depicted in **Fig. 1.4**.
- High converter availability through SM redundancy.
- Increase in efficiency of hydraulic side, i.e. better use of storage resources.

1.5 Objectives

Principal research outcomes of the thesis are as follows:

- Development of a novel control methods for H-MMC, minimizing impact on machine insulation. Apart from being the enabling factor for retrofit of existing PHSP units to variable speed operation, this is also beneficial regarding design constraints of machines for new plants.
- Development of a novel design method for H-MMC AFE operated over an arbitrary, down-to-zero, DC link voltage range. The method offers a trade-off between attainable DC link voltage range, power factor and minimal FB SM share.
- Development of a novel design methods of H-MMC for CFSM PHSP applications, enabling a trade-off between grid support capabilities, allowable machine CM-voltage stress and minimization of FB SM share.

1.6 Outline of the thesis

Following *Chapter 1*, the thesis is structured in the following manner.

Chapter 2 introduces modeling approach to an individual Direct to Three-Phase (DC/3-AC) MMC. Derivation of governing equations is presented , converter-specific energy balancing methods are implemented, control loops are identified. Based on the results, back-to-back operation of two Three-Phase (3PH) MMCs, forming an I-MMC, is thoroughly analyzed. At this point, the converter operation is analyzed for an intertie application between two fixed AC grids of different fundamental frequencies, namely 50 Hz and 60 Hz. Control actions of individual converters are defined – *rectifier MMC* controls common DC link voltage, dictating active power exchange with grid 1; *inverter MMC* controls power exchange with grid 2, to meet the desired *P-Q* profile. This diversification leads to modifications of control loops of the two stages, which is described and implemented. Finally, switched model of an I-MMC is developed in *PLECS* software package.

Chapter 3 focuses on synchronous machine modeling, as the next step in analysis of PHSP MMC solution. Machine ratings matching Power Electronics Laboratory (PEL) medium voltage research platform prototype are analyzed. Vector control for CFSM is implemented to inverter MMC stage of the previously developed I-MMC model. Machine operation in the the zero-to-rated frequency region, is investigated. CM-voltage-based machine-side stage energy balancing is implemented, enabling operation at rated torque over the entire frequency range. PHSP-specific operating regimes are tested on the model. Start-stop sequences and operation mode switch-over between pumping and generating are considered. Grid-side control is extended for grid code compatibility. Upon detection of grid voltage or frequency deviation, converter response complies with the grid code requirements. Grid support capabilities of PHSP in such events has been analyzed and supported by in-depth simulation

results. An essential drawback of HB-based MMC in Variable Speed Drive (VSD) retrofit applications is identified: prohibitively high CM voltage machine stress at low-frequency operation.

Chapter 4 addresses the nature of MMC SM energy oscillations and their dependence on output frequency, output current and DC link voltage level. It is shown that machine-friendly CM-voltage-free MMC operation over the entire frequency range, and at rated machine torque, can be performed through variable DC link voltage control, without additional balancing control action compared to rated-frequency converter operation. Grid-side stage of the I-MMC is replaced by a FB-based design. DC link voltage control is implemented to allow for the CM-voltage-free operation. Machine start-up operating sequence, pumping/turbine change-over and LVRT sequence are demonstrated. The reference design comprising FB-based AFE stage is the starting point for H-MMC AFE development, leading to reduced CM-voltage machine stress at reduced FB SM share in the AFE converter stage.

Chapter 5 proposes a reduced CM-voltage-stress operation of PHSP at reduced FB count in the grid-side stage compared to *Chapter 4*. A novel control and appropriate design approach for H-MMC topology, as a grid-side stage of an I-MMC, enabling operation at variable DC link voltage and arbitrary power factor has been introduced. Insertion voltage sharing between HB and FB SMs is presented. An additional internal energy balancing loop for balancing between HB and FB SM clusters of each branch has been developed. Sizing and operation at typical operating points are compared to equally-rated I-MMC with FB-based grid-side stage of *Chapter 4*. Performance is compared to other existing H-MMC solutions. Converter design, in terms of required FB share, for arbitrary DC link voltage reduction at unity grid-side power factor, has been presented.

Chapter 6 proposes a novel H-MMC control and design method for further reduction of FB SM share in the grid-side stage of a PHSP I-MMC, while offering CM-voltage-free operation over the entire machine speed range. Starting from branch insertion voltage references, FB and HB insertion voltage sharing and reference alteration has been performed in such a way to ensure inherently balanced converter without additional control actions. An additional, corrective balancing control action is introduced for transient stability. While reduced FB SM share comes at the price of reduced power factor towards the grid at reduced machine speeds, a H-MMC design method for the proposed control approach has been presented, enabling a trade-off between attainable DC link voltage reduction range, available power factor range and minimal FB SM share. Operation limits of the presented control method have been verified. Machine start-up control sequence has been demonstrated.

Chapter 7 summarizes the thesis results and provides an outlook for future work.

1.7 List of publications

Journal papers:

J1. M. Basić, M. Utvić, and D. Dujić, "Hybrid modular multilevel converter design and control for variable speed pumped hydro storage plants," *IEEE Access*, vol. 9, pp. 140 050–140 065, 2021

J2. M. Basić and D. Dujić, "Hybrid modular multilevel converter for variable dc link voltage operation," *CPSS Transactions on Power Electronics and Applications*, vol. 6, no. 2, pp. 178–190, 2021

Conference papers:

C1. M. Basić, A. Schwery, and D. Dujić, "Highly Flexible Indirect Modular Multilevel Converter for High Power Pumped Hydro Storage Plants," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, IEEE, Oct. 2020, pp. 5290–5295

C2. M. Basić, S. Milovanović, and D. Dujić, "Comparison of two Modular Multilevel Converter Internal Energy Balancing Methods," in *2019 20th International Symposium on Power Electronics (Ee)*, IEEE, Oct. 2019, pp. 1–8

C3. M. Basić, P. C. O. Silva, and D. Dujić, "High Power Electronics Innovation Perspectives for Pumped Storage Power Plants," 2018

2
Indirect MMC Modeling

This chapter presents I-MMC modeling approach. Single converter stage dynamics is derived. MMC-specific internal energy balancing controllers are implemented. Higher level grid-side control structures are added, respecting differences in rectifier and inverter stage operation. Individual control loops, as well as back-to-back operation of the I-MMC have been validated.

2.1 MMC governing equations

Within the thesis, common MMC nomenclature is used, as depicted in **Fig. 2.1**. Basic building element of the converter is a SM. Each branch comprises a string of N_{SM} series connected SMs, and a branch inductance, denoted L_{br}, for protection and branch current control capability. Each of the three phase legs incorporates an upper (positive) and a lower (negative) branch.

Per-phase equivalent circuit of a DC/3-AC MMC, for the purpose of converter dynamics analysis, is displayed in **Fig. 2.2**. MMC branches comprise two-terminal SMs, as previously illustrated in **Fig. 2.1**. Energy storage is distributed, so that each SM comprises capacitor bank of C_{SM}. As there is no external fixed voltage power supply to individual SMs, number of levels can be freely chosen and scaled to application. Consequently, however, capacitor voltage levels are not defined, but rather floating. To ensure equal voltage distribution among SMs and proper operation of the converter, level of charge, i.e. energy, of each C_{SM} has to be controlled.

Individual SMs' capacitor voltage levels are denoted v^i_{cpx} and v^i_{cnx} for positive and negative branches, respectively, where x denotes phase and i index of the SM within the branch string. For simplicity, the entire string of branch SMs is presented through an equivalent capacitance $C_{\mathrm{br}} = C_{SM}/N_{SM}$, charged

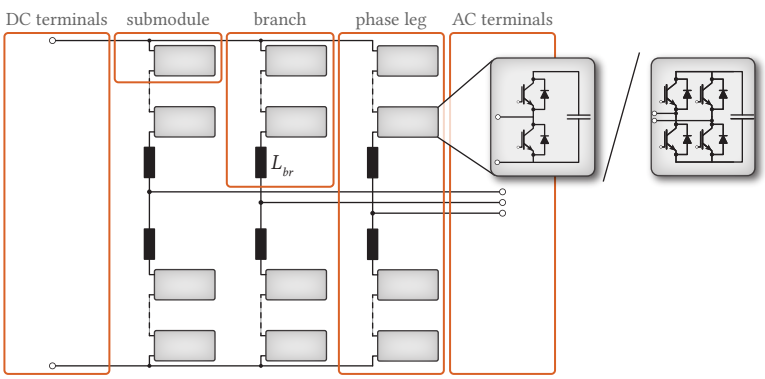


Fig. 2.1 Basic structure and nomenclature of a DC/3-AC MMC.

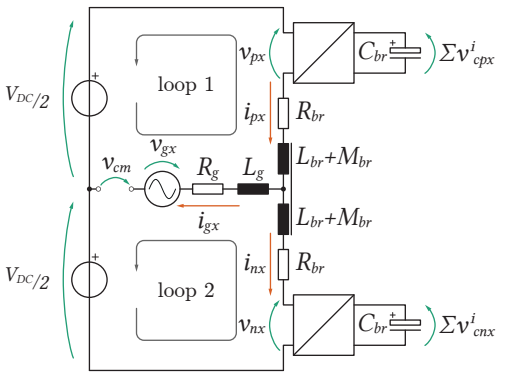


Fig. 2.2 Equivalent circuit of one phase leg of MMC.

to the sum of all capacitor voltages within the branch. If SM capacitor voltages are measured, it is straight-forward to determine modulation index of each branch for required instantaneous output voltage [43]. In MMC, modulation index is referred to as *insertion index*, as it essentially determines which portion of available distributed capacitor voltage is to be "inserted" in branch circuit. There are various switching strategies developed to achieve this; to reveal converter controllability, one can neglect switching behavior of SMs and assume branch-level voltage at terminals of the equivalent SM, $v_{\{p,n\}x}$, is equal to insertion index portion of total available capacitor voltage:

$$v_{\{p,n\}x} = m_{\{p,n\}x} \cdot \sum_{i=1}^{N} v^i_{c\{p,n\}x} \tag{2.1}$$

where $m_{\{p,n\}} \in [0,1]$ denotes SM insertion index. In case SM-level switching action is taken into consideration, instantaneous voltage $v_{\{p,n\}x}$ is defined as:

$$v_{\{p,n\}x} = \sum_{i=1}^{N} \left(s^i_{\{p,n\}x} \cdot v^i_{c\{p,n\}x} \right) \tag{2.2}$$

where $s^i_{\{p,n\}x}$ is a binary insertion function, that determines state of switches for each of the SMs.

Branch inductors are coupled with a factor k_{br}, mutual inductance being defined as $M_{br} = k_{br} L_{br}$. Converter losses are modeled through branch resistances R_{br}. In this case, grid is modeled as star-connected 3PH voltage source behind impedance. Grid impedance is represented by R_{g} and L_{g}, grid-side voltage by v_g and CM voltage component by v_{CM}.

Grid currents are defined through upper and lower branch currents as:

$$i_{gx} = i_{px} - i_{nx} \tag{2.3}$$

Kirchhoff's voltage law (KVL) equations can be written from two loops in **Fig. 2.2**:

$$\frac{V_{dc}}{2} = v_{CM} + v_{gx} + v_{px} + R_g \left(i_{px} - i_{nx} \right) + L_g \frac{d\left(i_{px} - i_{nx} \right)}{dt} + L_{br} \frac{di_{px}}{dt} - M_{br} \frac{di_{nx}}{dt} + R_{br} i_{px} \tag{2.4}$$

$$\frac{V_{dc}}{2} = -v_{CM} - v_{gx} + v_{nx} - R_g \left(i_{px} - i_{nx} \right) - L_g \frac{d\left(i_{px} - i_{nx} \right)}{dt} + L_{br} \frac{di_{nx}}{dt} - M_{br} \frac{di_{px}}{dt} + R_{br} i_{nx} \tag{2.5}$$

Further addition and subtraction of (2.4) and (2.5) leads to:

$$V_{dc} = v_{px} + v_{nx} + (L_{br} - M_{br}) \frac{d\left(i_{px} + i_{nx}\right)}{dt} + R_{br}\left(i_{px} + i_{nx}\right) \tag{2.6}$$

$$0 = v_{px} - v_{nx} + 2v_{CM} + 2v_g + \left(L_{br} + M_{br} + 2L_g\right) \frac{d\left(i_{px} - i_{nx}\right)}{dt} + \left(2R_g + R_{br}\right)\left(i_{px} - i_{nx}\right) \tag{2.7}$$

If we define the following quantities:

$$v_{cx} = \frac{v_{nx} + v_{px}}{2} \qquad \text{total inserted leg voltage} \tag{2.8}$$

$$v_{sx} = \frac{v_{nx} - v_{px}}{2} \qquad \text{differential phase-leg voltage} \tag{2.9}$$

$$i_{cx} = \frac{i_{px} + i_{nx}}{2} \qquad \text{circulating current} \tag{2.10}$$

$$i_{\{p,n\}x} = i_{cx} \pm \frac{i_{gx}}{2} \qquad \text{positive- and negative-branch currents} \tag{2.11}$$

Equations (2.6) and (2.7) can be rewritten as:

$$V_{dc} - v_{cx} = 2\left(L_{br} - M_{br}\right) \frac{di_c}{dt} + 2R_{br} i_c \tag{2.12}$$

$$v_{sx} - v_{gx} - v_{CM} = \left(L_g + \frac{L_{br} + M_{br}}{2}\right) \frac{di_{gx}}{dt} + \left(R_g + \frac{R_{br}}{2}\right) i_{gx} \tag{2.13}$$

By observing (2.12) and (2.13), it can be seen that grid current i_g and MMC-specific circulating current i_c are controllable through v_s and v_c, respectively. Power at which the energy is exchanged through AC and DC terminals can thus be independently controlled. Another conclusion is that freedom in design of branch inductors, more specifically freedom in choice of coupling coefficient k_{br}, means either grid- or circulating current filtering can be preferred:

$$k_{br} \begin{cases} > 0 & i_g \text{ filtering preferred} \\ < 0 & i_c \text{ filtering preferred} \end{cases}$$

In PHSP applications, with grid-code requirements on one AC side and synchronous machine stress on the other, filtering of AC-side current i_g is preferred. Thus, positive coupling coefficient has been chosen.

As aforementioned, MMC structure requires control of energy distribution among the SMs' capacitor banks, i.e. energy balancing. Capacitor dynamics is determined by the rate of charge or discharge. In case of an averaged model, being on the SM level and starting from (2.1), the following is true:

$$C_{SM} \frac{dv^i_{c\{p,n\}x}}{dt} = m_{\{p,n\}x} i_{\{p,n\}x} \tag{2.14}$$

Different modulation techniques can be applied, resulting in different energy balancing of SMs within a converter branch. At the higher level, capacitor voltage dynamics and energy distribution between upper and lower branches within a phase-leg, as well as between phase-legs, can be observed in

the same fashion, regardless of modulation approach and, consequently, insertion index calculation strategy. Starting from (2.14), capacitor voltage dynamics at branch level is determined:

$$v_{c\Sigma\{p,n\}x} = \sum_{i}^{N_{\mathrm{SM}}} v^{i}_{c\{p,n\}x} \tag{2.15}$$

$$C_{\mathrm{br}} \frac{dv_{c\Sigma\{p,n\}x}}{dt} = m_{\{p,n\}x} i_{\{p,n\}x} \tag{2.16}$$

which leads to sum (2.17) and differential (2.18) phase-leg voltage values:

$$v_{c\Sigma\Sigma x} = v_{c\Sigma px} + v_{c\Sigma nx} \tag{2.17}$$

$$v_{c\Sigma\Delta x} = \frac{v_{c\Sigma nx} - v_{c\Sigma px}}{2} \tag{2.18}$$

The aim of branch-level energy controller is to manage energy distribution among MMC branches. It is achieved by equalizing sum voltage levels of all three phases (2.17), at the same time driving differential voltage levels of upper and lower phase-leg's branches to zero (2.18).

2.2 Converter control outline

I-MMC model has been developed, as presented in **Fig. 2.3**. Looking at a single conversion stage, one can diversify:

- *MMC SMs* – power stage and appropriate voltage and current measurements
- *Internal MMC control* – topology-specific control loops:
  - Energy balancing: control of horizontal and vertical energy distribution among SMs, and of total energy stored in the converter
  - Circulating current control used for energy balancing actions
  - Individual SM insertion commands
- *Higher-level control* structures, used regardless of the selected topology:
  - Phase-Locked Loop (PLL) for synchronization with the grid
  - Grid Current Control (GCC) to achieve desired power of energy exchange towards the grid
  - DC link voltage control, indirectly through total energy control, handled by the rectifier stage
  - P/Q control towards the 60 Hz grid, handled by the inverter stage

Converter control structure is shown in more detail in **Fig. 2.4**. Apart from well-known higher level control blocks, topology-specific energy balancing structures can be identified. The differences in realization of certain control blocks for rectifier and inverter stages are stressed in the figure, and explained further within the chapter.

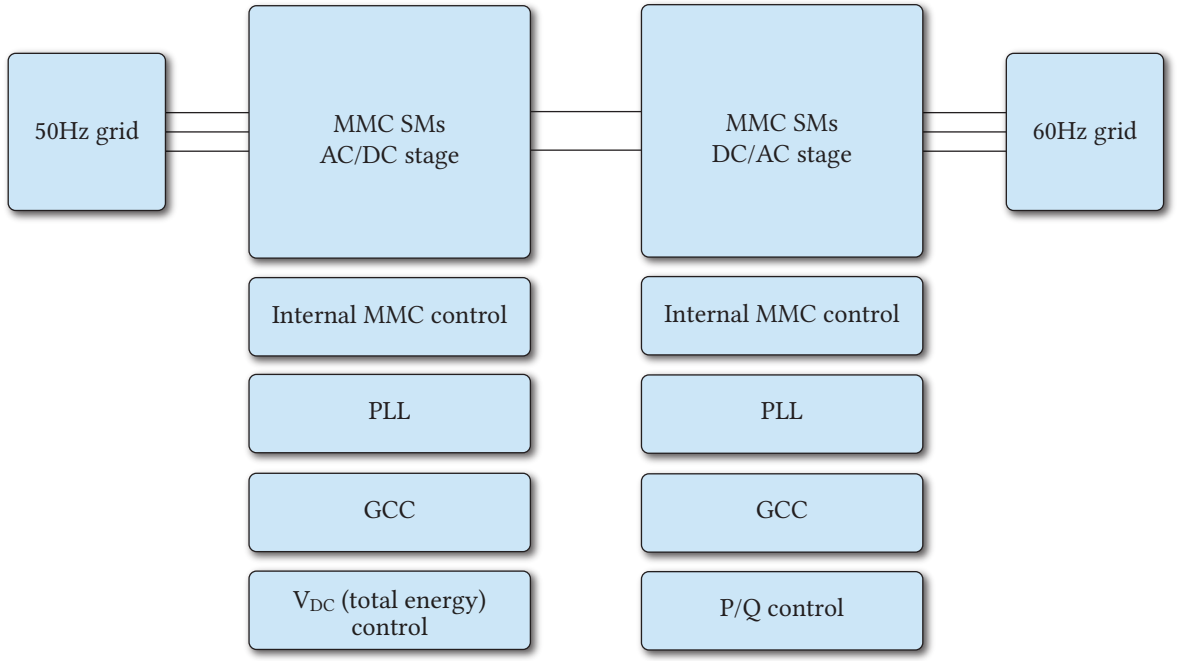


Fig. 2.3 Overview of the developed I-MMC model, interfacing two AC grids of different frequencies. Rectifier and inverter stages are connected to 50 Hz and 60 Hz grids, respectively.

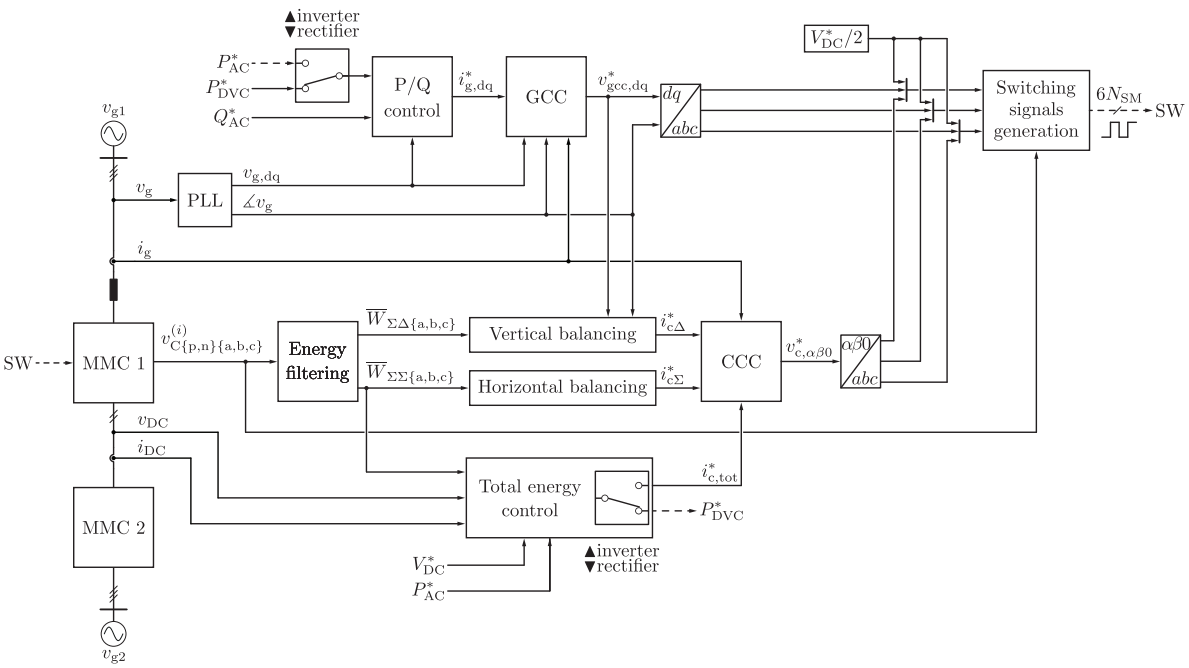


Fig. 2.4 DC/3-AC MMC control structure is presented, including the most important signals. Difference between rectifier and inverter MMC application can be seen in the way total energy is controlled, output voltages generated, and power references calculated. Reference values are marked by an asterisk. The following sections describe each block in detail.

2.3 Internal MMC control

Distributed energy storage, the enabling element of MMC scalability and redundancy, requires special attention from control perspective. Converter branches are realized as strings of two-terminal SMs, with each SM acting as a voltage source. Voltage amplitude is naturally not fixed but rather determined by the state of charge of SM's capacitor bank, C_{SM}. Thus, equal average voltage level of each SM capacitor bank within the MMC must be ensured, regardless of the slight differences in actual SM capacitances due to manufacturing tolerances, or unequal loading due to transient operating events. Utilizing three sets of branch-level controllers, and one SM-level controller, energy storage can be balanced:

- Total – level of stored energy in MMC corresponds to nominal charge of all SMs
- Horizontal – all three phase-legs store equal amounts of energies
- Vertical – within each phase-leg, upper and lower arm evenly share energy storage
- Local – SM equal capacitor voltage level for each SM within a converter branch

2.3.1 Branch-level energy ripple dynamics

Expanding (2.16) with (2.11), the following is obtained:

$$C_{br}\frac{dv_{c\Sigma px}}{dt} = m_{px}\left(i_{cx} + \frac{i_{gx}}{2}\right) \tag{2.19}$$

$$C_{br}\frac{dv_{c\Sigma nx}}{dt} = m_{nx}\left(i_{cx} - \frac{i_{gx}}{2}\right) \tag{2.20}$$

where ideal insertion indexes can be defined from (2.8) and (2.9):

$$v_{cx} = \frac{m_{px}v_{c\Sigma px} + m_{nx}v_{c\Sigma nx}}{2} \tag{2.21}$$

$$v_{sx} = \frac{-m_{px}v_{c\Sigma px} + m_{nx}v_{c\Sigma nx}}{2} \tag{2.22}$$

After adding and subtracting obtained expressions (2.21) and (2.22), ideal insertion indexes can be retrieved:

$$m_{px} = \frac{v_{cx}^{*} - v_{sx}^{*}}{v_{c\Sigma px}} \tag{2.23}$$

$$m_{nx} = \frac{v_{cx}^{*} + v_{sx}^{*}}{v_{c\Sigma nx}} \tag{2.24}$$

Returning (2.23) and (2.24) into (2.19) and (2.20), multiplying with $v_{c\Sigma\{p,n\}x}$ and keeping in mind that $dv(t)\cdot dv(t)/dt = 1/2dv^2(x)/dt$, sum energy dynamics of positive and negative branches can be identified.

$$\frac{dW_{px}}{dt} = \frac{1}{2}\frac{C_{br}d\left(v_{c\Sigma px}^2\right)}{dt} = \left(v_{cx}^{*} - v_{sx}^{*}\right)\left(i_{gx}/2 + i_{cx}\right) \tag{2.25}$$

$$\frac{dW_{nx}}{dt} = \frac{1}{2}\frac{C_{br}d\left(v_{c\Sigma nx}^2\right)}{dt} = \left(v_{cx}^{*} + v_{sx}^{*}\right)\left(-i_{gx}/2 + i_{cx}\right) \tag{2.26}$$

To observe energy imbalances between phases and between upper and lower branches of individual phases, one should observe sum and difference of upper and lower branches, respectively.

$$\frac{dW_{\Sigma x}}{dt} = \frac{dW_{px}}{dt} + \frac{dW_{nx}}{dt} = 2v_{cx}^{*}i_{cx} - v_{sx}^{*}i_{gx} \tag{2.27}$$

$$\frac{dW_{\Delta x}}{dt} = \frac{dW_{px}}{dt} - \frac{dW_{nx}}{dt} = v_{cx}^{*}i_{gx} - 2v_{sx}^{*}i_{cx} \tag{2.28}$$

Starting from time-domain representation of v_s and i_g, namely $v_s = \hat{v}_s \cos\left(\omega_g t\right)$ and $i_g = \hat{i}_g \cos\left(\omega_g t + \varphi_g\right)$, while considering $v_c^{*} \approx V_{DC}/2$, expressions (2.27) and (2.28) can be rewritten to reveal converter energy dynamics (2.29) and (2.30). AC-terminal angular frequency and phase shift between voltage and current phasors are denoted by ω_g and φ_g, respectively.

$$\frac{dW_{\Sigma x}}{dt} = \underbrace{V_{dc}i_{cx}}_{\substack{P_{DC}\text{ and}\\ \text{balancing}}} \underbrace{- \frac{\hat{v}_{sx}\hat{i}_{gx}}{2}\cos(\varphi_g)}_{P_{AC}\text{ per phase}} \underbrace{- \frac{\hat{v}_{sx}\hat{i}_{gx}}{2}\cos(2\omega_g t + \varphi_g)}_{\text{zero average}} \tag{2.29}$$

$$\frac{dW_{\Delta x}}{dt} = \underbrace{\frac{V_{dc}\hat{i}_{gx}}{2}\cos(\omega_g t + \varphi_g)}_{\text{zero average}} \underbrace{- 2\hat{v}_{sx}i_{cx}\cos(\omega_g t + \varphi_g)}_{\text{balancing}} \tag{2.30}$$

From (2.29), the dual purpose of the circulating current DC component is revealed. Firstly, it controls active power exchange with the DC link, equalizing it with the AC terminals power demand (P_{AC}). Secondly, it controls the energy exchange with the remaining converter legs, equalizing horizontal energy distribution. Further, based on (2.30), it is straightforward to conclude that the AC component of the circulating current $i_c^{\sim} = \hat{i}_c^{\sim}\cos(\omega t + \Psi)$ can be used to obtain the leg energy balance in vertical direction. Denoting the angle displacement between this component and the leg differential voltage component v_s by Φ, yields

$$\frac{dW_{\Delta x}}{dt} = -\hat{v}_{sx}\hat{i}_{cx}^{\sim}\cos(\Phi) \tag{2.31}$$

In general, Φ can be arbitrarily chosen. Phase alignment of the above mentioned voltage and current components is assumed throughout this chapter, i.e. $\Phi = 0$.

Total energy control ensures matching of the powers at which the energy is exchanged between the DC and AC terminals through the adjustment of the DC link current reference i_{DC}^{*}. Thus, circulating current can be expressed as:

$$i_c = \underbrace{i_{DC}/3 + i_{c\Sigma}}_{=\bar{i}_c} + \underbrace{i_{c\Delta}}_{=i_c^{\sim}} \tag{2.32}$$

Nonetheless, horizontal (through $i_{c\Sigma}$) and vertical (through $i_{c\Delta}$) balancing actions are purely internal to the MMC and should not be seen either from the AC or the DC terminals. Consequently, the proper energy balancing criteria can be mathematically formulated as:

$$\sum \vec{i}_{c\{a,b,c\}} = i_{DC} \tag{2.33}$$

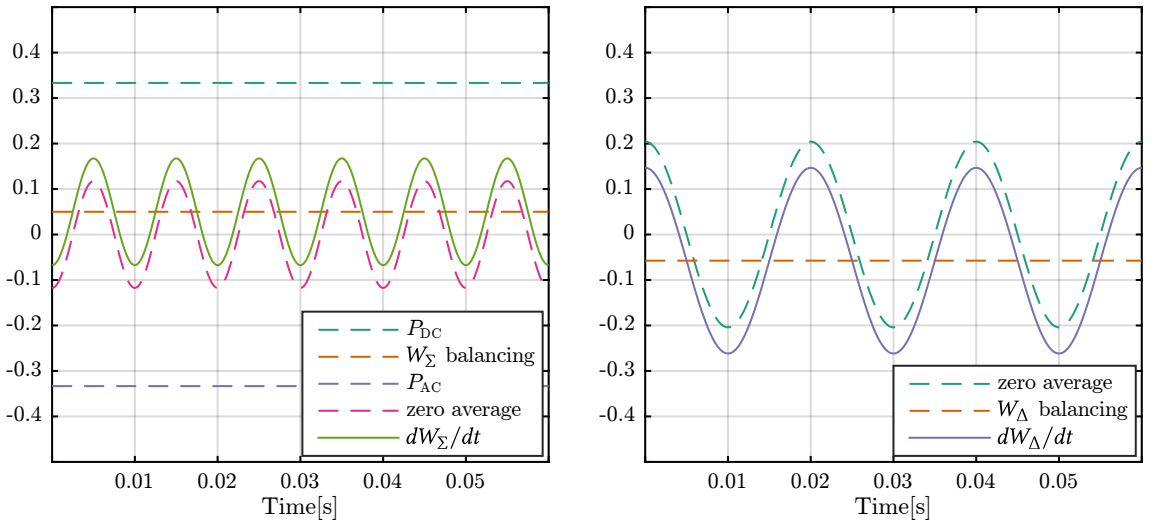


Fig. 2.5 Visualization of MMC energy dynamics, analytically expressed in (2.29) and (2.30). (a) presents sum energy dynamics: powers of exchange with AC and DC terminals are equal and of opposite sign; zero average oscillating component is present; sum energy balancing action is of DC nature, and offsets resulting value. (b) illustrates differential energy dynamics: oscillating component is of zero average value; differential energy balancing action is phase-aligned with differential voltage, and thus introduces power offset for balancing purpose.

Integration of expressions (2.29) and (2.30) unveils dynamics of sum and differential energies:

$$W_{\Sigma x} = \underbrace{-\frac{\hat{v}_{sx}\hat{i}_{gx}}{4\omega_g} sin\left(2\omega_g t + \varphi\right)}_{\Delta W_\Sigma} + W_{\Sigma 0} \tag{2.34}$$

$$W_{\Delta x} = \underbrace{-\frac{V_{DC}\hat{i}_{gx}}{2\omega_g} sin\left(\omega_g t + \varphi\right) - \frac{2\hat{v}_{gx}\hat{i}_{cx}}{\omega_g} sin\left(\omega_g t + \varphi\right)}_{\Delta W_\Delta} + W_{\Delta 0} \tag{2.35}$$

Second term in (2.34), $W_{\Sigma 0}$, represents average stored energy per phase leg, and should be set to one third of total energy reference (2.52). Third term in (2.35), $W_{\Delta 0}$, corresponds to average difference of energies stored in upper and lower arms of a phase, and should be naturally set to zero.

2.3.2 Energy measurement and filtering

It is clear from both (2.34) and (2.35) and **Fig. 2.5** that sum and differential energy distribution within an MMC has both average and time-varying terms. Concerning balancing, it is of interest to control average terms. Measured energies are thus filtered prior to feeding controllers, to remove components varying at fundamental ($\omega_0 = \omega_g$) and double the fundamental ($\omega_0 = 2\omega_g$) frequency. Two series notch filters were used, characterized by the following transfer function:

$$H(s) = \frac{s^2 + \omega_0^2}{s^2 + s\omega_c + \omega_0^2} \tag{2.36}$$

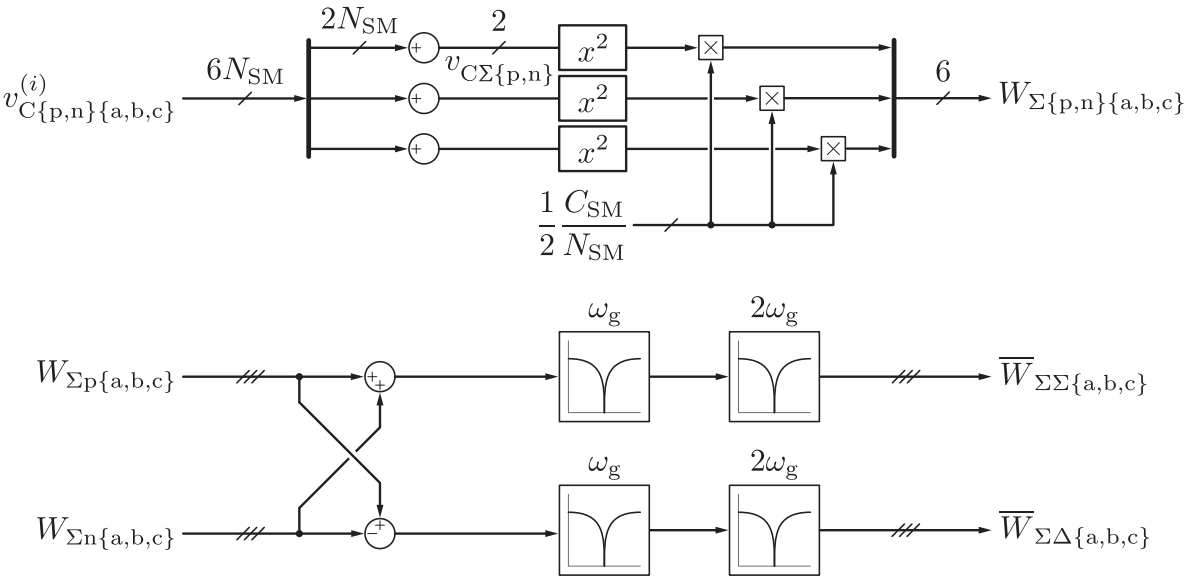


Fig. 2.6 Energy measurement and filtering of inherent oscillations through ω_{g} and $2\omega_{\mathrm{g}}$ notch filters. Average sum and differential values are fed to energy balancing controllers.

where ω_0 represents central rejection frequency and ω_c – rejection band width. Energy measurement and filtering is implemented as in **Fig. 2.6**.

2.3.3 Horizontal energy balancing

Analyzing expressions for sum phase-leg energies (2.34) in $\alpha\beta 0$ domain, horizontal energy balancing can be discussed.

$$W_{\Sigma\alpha} = \frac{2}{3}\left(W_{\Sigma\mathrm{a}} - \frac{W_{\Sigma\mathrm{b}} + W_{\Sigma\mathrm{c}}}{2}\right) \tag{2.37}$$

$$W_{\Sigma\beta} = \frac{2}{3}\frac{\sqrt{3}}{2}\left(W_{\Sigma\mathrm{b}} - W_{\Sigma\mathrm{c}}\right) \tag{2.38}$$

$$W_{\Sigma 0} = \frac{1}{3}\left(W_{\Sigma\mathrm{a}} + W_{\Sigma\mathrm{b}} + W_{\Sigma\mathrm{c}}\right) \tag{2.39}$$

It can be seen from (2.37) to (2.39) that, in case $W_{\Sigma\alpha} = W_{\Sigma\beta} = 0$, phase legs store the same amount of energy, which is desirable, determined by the common mode component $W_{\Sigma 0}$.

$$W_{\Sigma\beta} = 0 \rightarrow W_{\Sigma\mathrm{b}} = W_{\Sigma\mathrm{c}} \tag{2.40}$$

$$W_{\Sigma\alpha} = 0 \rightarrow W_{\Sigma\mathrm{a}} = W_{\Sigma\mathrm{b}} = W_{\Sigma\mathrm{c}} \tag{2.41}$$

The aim of horizontal and total (**Sec. 2.3.5**) energy control actions is to ensure there is no energy exchange with DC link in steady-state, other than that for supplying active power (P_{AC}) to the load. Since balancing aims to control average energy values, looking at (2.29), first and second terms should be equalized by means of circulating current control. Transforming controllable terms of (2.29), i.e. those containing i_{c}, to $\alpha\beta 0$ domain, (2.42) to (2.44) is obtained.

$$\overline{\frac{dW^*_{\Sigma\alpha}}{dt}} = \frac{2}{3}V_{\mathrm{DC}}\underbrace{\left(i_{\mathrm{ca}} - \frac{i_{\mathrm{cb}} + i_{\mathrm{cc}}}{2}\right)}_{i_{c\alpha}} = 0 \tag{2.42}$$

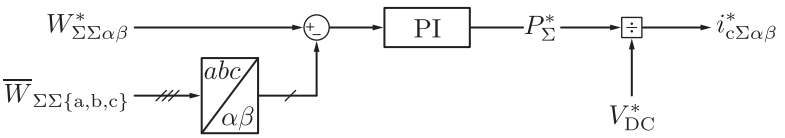


Fig. 2.7 Horizontal energy balancing implementation for one MMC stage. Observed energy is a filtered value, as average components are of interest. To achieve even horizontal energy distribution, $\alpha\beta$ components are referenced to zero.

$$\overline{\frac{dW^*_{\Sigma\beta}}{dt}} = \frac{2}{3} V_{DC} \underbrace{\frac{\sqrt{3}}{2}\left(i_{cb} - i_{cc}\right)}_{i_{c\beta}} = 0 \tag{2.43}$$

$$\overline{\frac{dW^*_{\Sigma 0}}{dt}} = \frac{2}{3} V_{DC} \underbrace{\frac{1}{2}\left(i_{ca} + i_{cb} + i_{cc}\right)}_{i_{c0}} = P_{DC} \tag{2.44}$$

Imposing zero mean power of energy exchange with DC link ensures equal sum state of charge of all three phase-legs, as in (2.42) and (2.43). Horizontal energy balancing action is implemented as in **Fig. 2.7**. Filtered mean measured value of sum energies is fed to the controller, where $\alpha\beta$ components are driven to zero.

2.3.4 Vertical energy balancing

The aim of vertical control action is to balance the energies stored in upper and lower branches at phase-leg level. From (2.28) and (2.35), circulating current can be controlled to suppress $W_{\Delta 0}$.

Applying balancing current references calculated in per-phase manner is not acceptable, as one cannot guarantee $\Sigma i_{c\Delta\{a,b,c\}} = 0$. Non-zero sum of per-phase circulating current components causes additional and unwanted active power exchange. For proper control action, an approach presented in [44] has been applied, which essentially assumes two steps:

- Calculation of appropriate in-phase circulating current amplitudes to achieve desired vertical energy corrections.
- For each injected active (in-phase) component, appropriate reactive (in-quadrature) components for remaining two phases are calculated, so that sum of currents equals zero. The in-quadrature components ensure that no disturbance from the control action is visible from the DC side (**Fig. 2.8**).

From **Fig. 2.8**, observing phase *a* balancing action, current components are:

$$\left|i^*_{c\Delta a}\right| = \hat{i}^*_{c\Delta a} \qquad \left|i^a_{c\Delta b}\right| = \left|i^a_{c\Delta c}\right| = \frac{\hat{i}^*_{c\Delta a}}{2\cos(\pi/6)} \tag{2.45}$$

Resulting balancing current references for all three phases are given and converted to *di*0 domain in

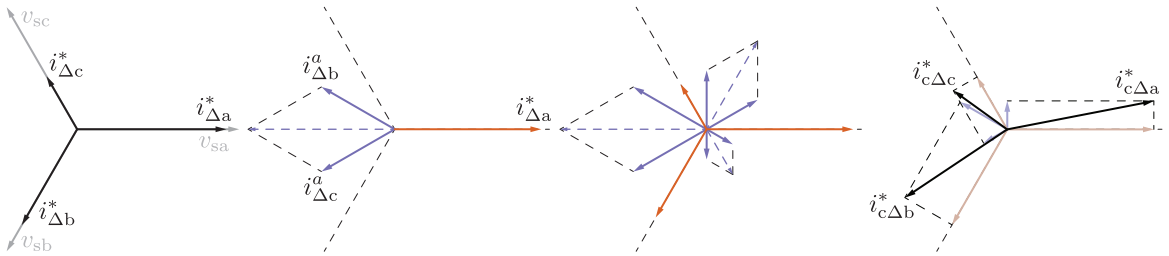


Fig. 2.8 Principle of vertical energy balancing currents injection is shown from left to right. Sum of per-phase generated current references differs from zero (a). For control action in observed phase, additional in-quadrature currents are injected in the remaining two phases (b). The same is done for all three control action current references (c). Consequently, final zero-sum references are obtained (d). In this way, no disturbance is visible from the converter terminals.

(2.46) and (2.47) to (2.49), where phase a is aligned with phase-axis and operator $a = e^{j2\pi/3}$.

$$\begin{bmatrix} \underline{i}^*_{\Delta 0} \\ \underline{i}^*_{\Delta d} \\ \underline{i}^*_{\Delta i} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \underbrace{\begin{bmatrix} 1 & j\frac{a}{\sqrt{3}} & -j\frac{a^2}{\sqrt{3}} \\ -j\frac{a^2}{\sqrt{3}} & 1 & j\frac{a}{\sqrt{3}} \\ j\frac{a}{\sqrt{3}} & -j\frac{a^2}{\sqrt{3}} & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 & 0 \\ 0 & a^2 & 0 \\ 0 & 0 & a \end{bmatrix}\begin{bmatrix} |\underline{i}^*_{\Delta a}| \\ |\underline{i}^*_{\Delta b}| \\ |\underline{i}^*_{\Delta c}| \end{bmatrix}}_{\underline{i}^*_{\Delta\{a,b,c\}}} \tag{2.46}$$

$$\underline{i}^*_{\Delta d} = \frac{1}{3}\left[|\underline{i}^*_{\Delta a}| + |\underline{i}^*_{\Delta b}| + |\underline{i}^*_{\Delta c}|\right] \tag{2.47}$$

$$\underline{i}^*_{\Delta i} = \frac{2}{3}\left[|\underline{i}^*_{\Delta a}| - \frac{1}{2}\left(|\underline{i}^*_{\Delta b}| + |\underline{i}^*_{\Delta c}|\right)\right] + j\frac{2}{3}\left[0 + \frac{\sqrt{3}}{2}|\underline{i}^*_{\Delta b}| - \frac{\sqrt{3}}{2}|\underline{i}^*_{\Delta c}|\right] \tag{2.48}$$

$$\underline{i}^*_{\Delta 0} = 0 \tag{2.49}$$

If one recalls Clarke transformation, an analogy can be made between obtained $di0$ components and $abc \rightarrow \alpha\beta 0$ conversion matrix output (2.50).

$$\underline{i}^*_{\Delta d} \xrightarrow{\alpha\beta 0} i^*_{\Delta 0} \qquad\qquad \underline{i}^*_{\Delta i} \xrightarrow{\alpha\beta 0} i^*_{\Delta\alpha} + j i^*_{\Delta\beta} \tag{2.50}$$

Implementation of vertical energy balancing is thus realized in $\alpha\beta 0$ domain, as presented in **Fig. 2.9**. Angle ψ_Δ represents position of GCC output voltage reference vector, with regards to phase axis:

$$\psi_\Delta = \varphi_{g,PLL} + \theta_{dq,GCC} \tag{2.51}$$

where $\varphi_{g,PLL}$ and $\theta_{dq,GCC}$ are grid phase angle obtained from PLL and GCC output voltage vector angle with regards to d axis, respectively.

2.3.5 Total energy control

Total energy stored in six branches of MMC is controlled according to the rated SM capacitor voltage and capacitance (2.52) and is performed differently for the two conversion stages within an I-MMC.

$$W^*_{total} = 6\frac{C_{br}\left(N_{SM}V^*_{SM}\right)^2}{2} = 3N_{SM}C_{SM}V^{*2}_{SM} \tag{2.52}$$

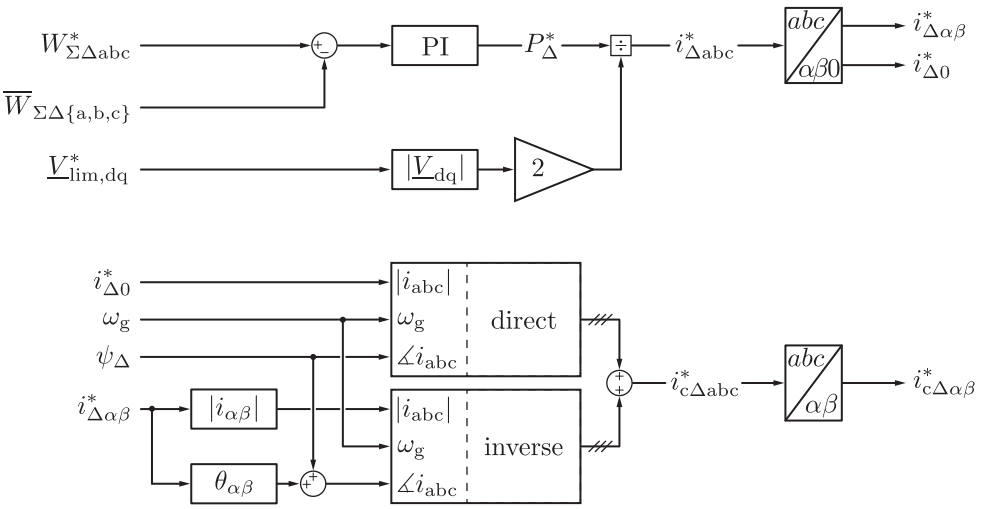


Fig. 2.9 Implementation of vertical energy balancing control. Differential energy reference is naturally set to zero in *abc* system, to equalize vertical phase-leg-level energy distribution. Voltage amplitude is obtained directly from GCC *dq* reference, as utilized Clarke transformation is voltage amplitude invariant.

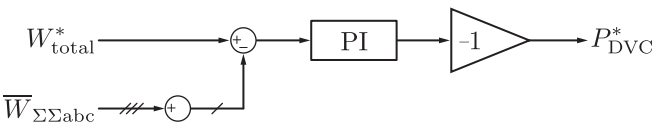


Fig. 2.10 DC link voltage control through total energy control of rectifier stage. Averaged energy component is taken into account, while inherent energy oscillations at ω_g and $2\omega_\mathrm{g}$ are filtered. *DVC* stands for indirect DC link voltage control action through total energy control action.

Rectifier stage comprises indirect DC link voltage control, realized as an energy controller which ensures equal active power of energy exchange between rectifier and grid on one hand, and between the two conversion stages on the other, thus ensuring stable voltage level towards the inverter. Rectifier stage is thus acting as a voltage source towards inverter stage. Balancing action is realized as described in **Fig. 2.10**. As can be seen in (2.52), it performs total energy control.

Inverter stage regulates state of charge of the entire converter by acting on circulating current control. It is clear from (2.44) that zero-sequence $i_{\mathrm{c}0}$ control leads to active power exchange balancing between the AC grid and the DC link. Consequently, average level of SMs' capacitor charge is nominal and constant. Control action implementation is presented in **Fig. 2.11**.

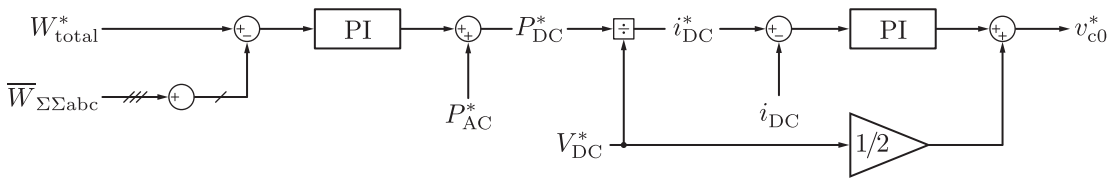


Fig. 2.11 Total energy control implementation for inverter stage MMC.

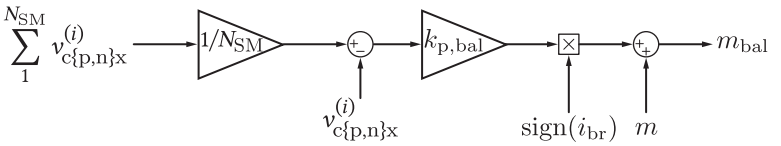


Fig. 2.12 Local SM balancing is implemented through alteration of insertion index m. Total available branch voltage, i.e. the sum of SM voltages is divided by N_{SM}, compared to measured SM capacitor voltage, and multiplied by an empirically determined local balancing gain $k_{p,bal}$. Based on the branch current polarity, the insertion index modification sign is determined to achieve corrective SM charging or discharging.

2.3.6 MMC voltage references generation

Converter output voltage references for upper and lower branches are calculated as a superposition of GCC output control action and MMC-specific balancing voltage references generated by Circulating Current Control (CCC), as depicted in **Fig. 2.4**. SMs' insertion indexes are then calculated according to (2.23) and (2.24), where $v_{c\Sigma\{p,n\}x}$ are measured values.

2.3.7 SM voltage balancing

As previously presented, the appropriate horizontal and vertical balancing controllers ensure equal energy distribution on phase-level among upper and lower branches, as well as on converter-level among phase-legs. To prevent deterioration of output voltage quality, equal energy, i.e. voltage, distribution on intra-branch level must be realized. SM capacitor voltage level is measured and compared with reference value. Corrections are performed through slight modification of individual SMs' insertion indexes, governed by a proportional action controller [45]. SM-level local balancing has been implemented as in **Fig. 2.12**. In case actual capacitor voltage differs from reference, insertion index is increased or decreased, depending on branch current sign, to achieve capacitor charging or discharging. For example, for positive voltage error and negative current sign, insertion index is decreased. Initial insertion indexes, obtained from higher level control (2.23) and (2.24) are corrected:

$$m_{\{p,n\}x,bal}^{(i)} = \frac{v_{cx}^{*} \mp v_{sx}^{*}}{v_{c\Sigma\{p,n\}x}} + \mathrm{sign}\left(i_{br,x}\right)\left(V_{SM}^{*} - v_{C}^{(i)}\right) k_{p,bal} \tag{2.53}$$

where x and (i) denote phase and SM index, respectively.

2.3.8 Modulation

There are numerous modulation techniques applied to MMCs – carrier-based Level-Shifted Carrier PWM (LSC-PWM) and PSC-PWM, Nearest-Level Modulation (NLM), OPP, to name a few. In high-SM-count MMC applications, e.g. HVDC inter-ties, the use of NLM is common due to high output voltage resolution [46], [47]. Medium-voltage applications, however, comprise far fewer SMs. Inheriting modulation of HVDC installations would result in poor output voltage waveform quality, further followed by significant current harmonic distortion [46]. A method to adapt modulation approach to medium-voltage installations, by combining nearest-level and pulse-width modulation, is presented in [46]. Another approach can naturally be the use of PSC-PWM modulation, introduced for multilevel converters in [48]. In such a case, N_{SM}-times higher apparent switching frequency at the converter branch terminals, with respect to SM switching frequency, ensures high-quality output voltage waveform, i.e. low total harmonic distortion. At this point, PSC-PWM modulation is implemented.

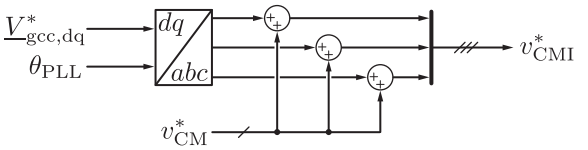


Fig. 2.13 CM voltage injection principle. Injection of CM voltage components, denoted v_{CM}, does not introduce additional currents in ungrounded star systems.

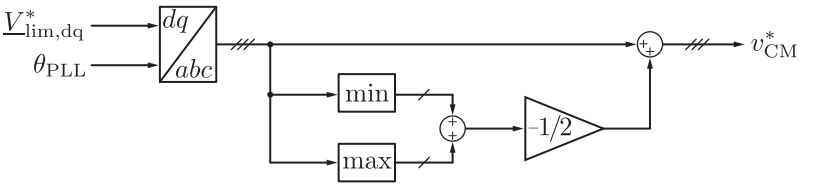


Fig. 2.14 CM voltage injection implementation utilizing min/max method.

2.3.8.1 Common-mode voltage injection

In ungrounded systems, e.g. MMC interfaced to the grid through an isolated-star transformer, or driving an AC machine, the introduction of zero-sequence component in output voltage waveform does not induce additional current components (**Fig. 2.13**). On the other hand, it is well known that DC link utilization of a VSC can be improved by means of CM voltages injection (2.54).

$$V_{\mathrm{max,CMI}} = \frac{V_{DC}}{\sqrt{3}} = 1{,}15 V_{\mathrm{max}} \tag{2.54}$$

An increase of 15% is significant in high-power applications in terms of both capacitor and overall DC bus voltage ratings. The so-called min-max, or symmetrical references approach is implemented, as in **Fig. 2.14**. Reference amplitudes are altered in a way that maximum and minimum values at any given time are equal and of opposite sign.

2.4 Higher level control

2.4.1 Grid synchronization

To properly synchronize the converter towards the grid, and achieve desired P/Q rate of energy exchange, knowledge of $\vec{v}_g$ vector amplitude and angle is necessary. At this point, the basic PLL block depicted in **Fig. 2.15** is used for the purpose, being adequate for balanced grid conditions studies.

In the dq system used for converter control in this thesis, grid voltage vector is aligned with d-axis. Thus, grid voltage angle is obtained from a PI controller driving amplitude-normalized v_q component to zero. For faster angle detection, fundamental grid frequency ω_{g} is fed forward. Integration of the resulting angular frequency and $[0, 2\pi)$ range wrap-up provide the grid voltage angle estimation θ_{PLL}.

2.4.2 Grid current control

GCC computes converter output voltage references $v^*_{\mathrm{g\{a,b,c\}}}$, based on current requirements from the higher-level controller: V_{DC}/Q in case of rectifier or P/Q in case of inverter MMC stage (**Fig. 2.17**).

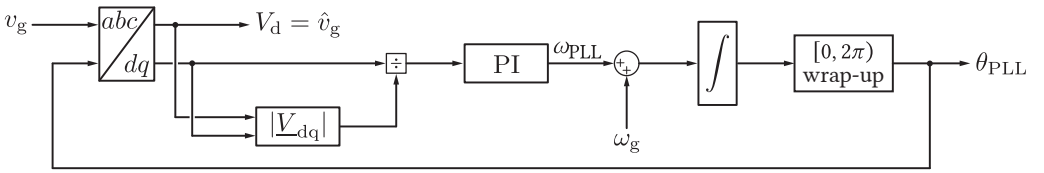


Fig. 2.15 PLL implementation used in the model is presented. q-component of grid voltage is scaled to unitary signal, using actual grid voltage amplitude. In this way, symmetrical voltage amplitude variations do not affect PLL performance. Assuming good tracking of grid angle, q-component is driven to zero. Consequently, grid voltage is aligned with d-axis of converter's GCC.

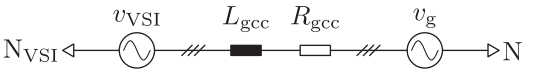


Fig. 2.16 Simplified overview of ideal VSC GCC through equivalent impedance.

Measured voltage (v_g) and current (i_g) values, current reference and PLL-based angle are sampled at apparent switching frequency:

$$f_{sampling} = f_{sw,app} = f_{sw} \cdot N_{SM} \tag{2.55}$$

In principle, grid current control approach for an MMC is the same as for two-level VSC. A simplified situation, where VSC is represented as a 3PH controllable ideal source is sufficient for the analysis (**Fig. 2.16**). Following KVL equations and migrating to dq-domain, the following is true:

$$\underline{V}_{dq} = R_{gcc}\underline{i}_{dq} + L_{gcc}\frac{d\underline{i}_{dq}}{dt} + j\omega L_{gcc}\underline{i}_{dq} + \underline{V}_{g,dq} \tag{2.56}$$

$$\frac{d\underline{i}_{dq}}{dt} = \frac{1}{L_{gcc}}\left(\underline{V}_{dq} - \underline{V}_{g,dq} - R_{gcc}\underline{i}_{dq} - j\omega L_{gcc}\underline{i}_{dq}\right) \tag{2.57}$$

where L_{gcc} and R_{gcc} are components of the equivalent impedance seen by the GCC.

$$L_{gcc} = L_{br,AC} + L_g = L_{br}(1 + k_{br})/2 + L_g \tag{2.58}$$

Taking that q-axis advances over d, the following scalar form follows, and is implemented in GCC **Fig. 2.17**:

$$\frac{di_d}{dt} = \frac{1}{L_{gcc}}\left(V_d - V_{g,d} - R_{gcc}i_d + \omega L_{gcc}i_q\right) \tag{2.59}$$

$$\frac{di_q}{dt} = \frac{1}{L_{gcc}}\left(V_q - V_{g,q} - R_{gcc}i_q - \omega L_{gcc}i_d\right) \tag{2.60}$$

2.4.2.1 Output voltage limitation

Due to physical constraints in available control voltage reserve, output of GCC controller must be limited, so that the magnitude of output voltage reference vector $\underline{V}^*_{dq}$ remains below the limit, while preserving the angle ψ_{dq}. The limitation is implemented as in **Fig. 2.18**. Sum voltage reference for converter arm capacitor string is set to [49]:

$$\overline{v^*_{C\Sigma\{p,n\}x}} = V_{DC} \tag{2.61}$$

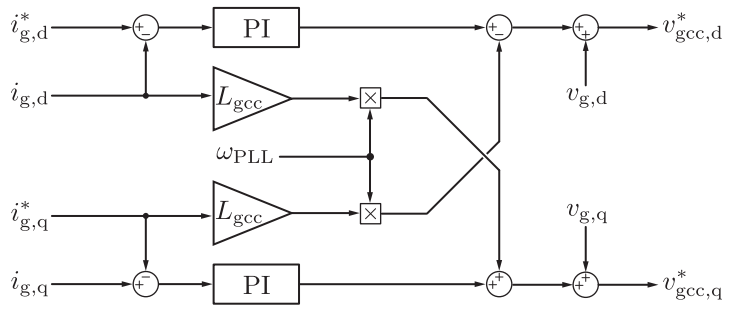


Fig. 2.17 GCC implementation in *dq* reference frame. L_{gcc} represents the equivalent inductance seen by the current controller.

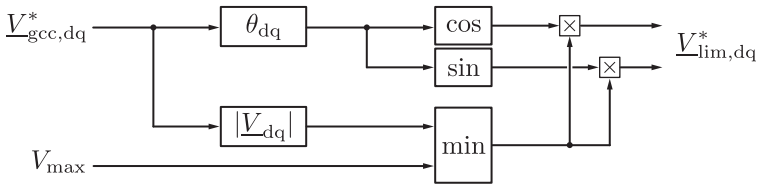


Fig. 2.18 GCC output voltage limitation.

to ensure $v_{cx} = V_{DC}$ (see (2.8)). If we neglect capacitor voltage ripple, it is clear from (2.9) that, in absolute terms,

$$V_{max} = v_{s,max} = \frac{V_{DC}}{2} \tag{2.62}$$

Once the voltage amplitude requirement reaches converter limit, $\underline{V}^*_{dq}$ is recreated with magnitude of V_{max}.

2.4.3 DC link voltage control

DC link voltage is controlled by the rectifier stage, indirectly through total energy control loop (**Sec. 2.3.5**). In contrast to low-level-count converter structures, MMC features distributed energy storage within SMs. The total amount of energy stored in six branches of one MMC conversion stage, under nominal conditions is given by (2.52). Active power reference of energy exchange with the 50 Hz grid is generated as output from total energy controller, and forwarded to *P*/*Q* control (**Fig. 2.10**). Equilibrium in energy exchange with 50 Hz grid on one side, and with inverter stage on the other, ensures stable DC voltage level.

2.4.4 Active and reactive power control

P/*Q* controller, realized as in **Fig. 2.19**, produces current references for inverter GCC based on power of exchange requirements. The operation is somewhat different for two conversion stages.

- *Rectifier MMC* – P^* is dictated by total energy controller, while Q^* can be arbitrarily set within converter operating range.
- *Inverter MMC* – both P^* and Q^* are set in accordance with requirements of energy exchange with 60 Hz grid.

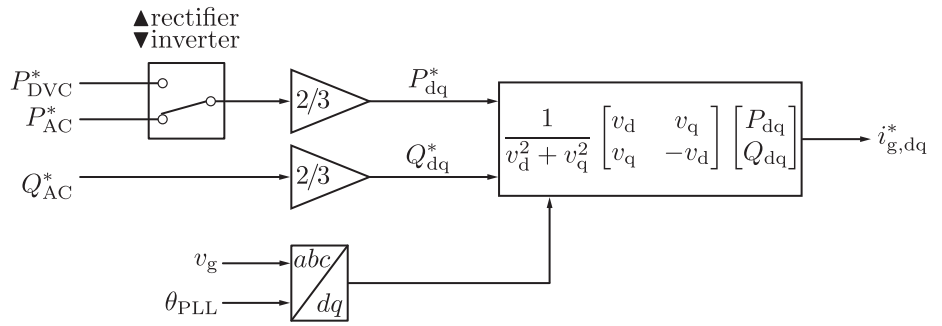


Fig. 2.19 Active and reactive power control for rectifier and inverter stages. Notice that rectifier stage can only arbitrarily control reactive power exchange, while active power is dictated by the load on inverter side. Reference power exchange direction is always from converter to the grid.

Current references are obtained according to instantaneous power theory [50]. In $\alpha\beta 0$ domain:

$$p_{\alpha\beta} = v_\alpha i_\alpha + v_\beta i_\beta \qquad \text{instantaneous P} \tag{2.63}$$

$$q_{\alpha\beta} = v_\alpha i_\beta - v_\beta i_\alpha \qquad \text{instantaneous Q} \tag{2.64}$$

$$p_0 = v_0 i_0 \qquad \text{instantaneous zero-sequence P} \tag{2.65}$$

or, written in matrix form:

$$\begin{bmatrix} p_{\alpha\beta} \\ q_{\alpha\beta} \\ p_0 \end{bmatrix} = \underbrace{\begin{bmatrix} v_\alpha & v_\beta & 0 \\ -v_\beta & v_\alpha & 0 \\ 0 & 0 & v_0 \end{bmatrix}}_{\left[M_{\alpha\beta 0}\right]} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \qquad \rightarrow \qquad \overrightarrow{i^*_{\alpha\beta 0}} = \left[M_{\alpha\beta 0}\right]^{-1} \begin{bmatrix} p^*_{\alpha\beta} \\ q^*_{\alpha\beta} \\ p^*_0 \end{bmatrix} \tag{2.66}$$

Assuming no zero-sequence power component, and keeping in mind that power references are invariant between $\alpha\beta$ and dq frames, current references fed to GCC are given by (2.67). Since transformations performed in the model are not power-invariant, i.e. $P_{\mathrm{dq}} = {}^2\!/_3 P_{\mathrm{abc}}$, the scaling factor of 2/3 is added. Implementation is presented in **Fig. 2.19**.

$$\begin{bmatrix} i^*_\mathrm{d} \\ i^*_\mathrm{q} \end{bmatrix} = \frac{2}{3}\frac{1}{v_\mathrm{d}^2 + v_\mathrm{q}^2}\begin{bmatrix} v_\mathrm{d} & -v_\mathrm{q} \\ v_\mathrm{q} & v_\mathrm{d} \end{bmatrix}\begin{bmatrix} p^*_{\mathrm{abc}} \\ q^*_{\mathrm{abc}} \end{bmatrix} \tag{2.67}$$

2.4.5 AC power grid

At this stage, both 50 Hz and 60 Hz grids are represented as ideal sinusoidal voltage sources behind equivalent R_g-L_g impedance, as depicted in **Fig. 2.20**. Voltage amplitude v_g, angular frequency ω_g and phase shift φ_g are varied to evaluate converter behavior under disturbances.

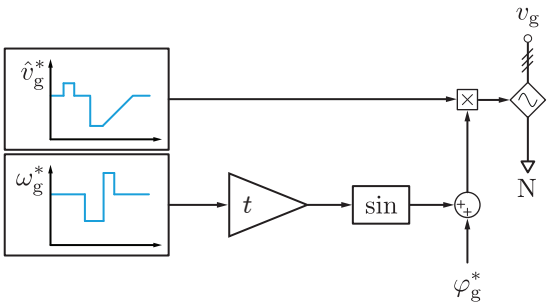


Fig. 2.20 Grid representation used for I-MMC model development. Voltage amplitude and frequency are altered to evaluate converter operation under disturbances.

2.5 SM modeling and ratings

The complexity of MMC topology, in terms of number of possible switching states, corresponds to the number of deployed SMs. Thus, the question of modeling approach naturally arises, with regards to level of adopted approximations (simplifications). Multiple options were considered (**Fig. 2.21**):

- *Arm-level averaged* model assumes a very simplified representation – each of the MMC arms is represented with a single SM of equivalent capacitance C_{br}. This level may be sufficient for system-level observations, as well as for higher-level control considerations (PLL, GCC). It has thus not been implemented in thee model.
- *SM-level averaged* model, unlike arm-level averaged, takes into account capacitance mismatch between SMs of a branch. Thus, SM balancing action may be implemented. However, switching action is not considered; rather, continuous insertion index value is used to control SM behavior.
- *SM-level fast switched* model represents each SM through capacitance C_{SM}, equivalent losses and auxiliary control circuit consumption represented by R_{SM}, and an idealized switch that "inserts" the SM into the branch according to the gating signal $G^{(i)}$. This approach is adequate for MMC-specific dynamics analysis, energy and circulating current controllers development.
- *SM-level switched* model may take into account non-ideal switching properties of SM semiconductors. It allows for thermal calculations.

The choice of using SM-level fast switched modeling approach is made, since it enables the study of all of the MMC control loops, takes into account the modulation scheme, and offers reasonable execution times. Vectorization feature of *PLECS* environment enables scaling of the model to the desired SM count without changes to the model layout or parameters other than N_{SM} (see **Fig. 2.21**).

2.5.1 PEL SM ratings

Even though modeling approach is unaffected by the number of SMs and their ratings, the simulation output will numerically correspond to the envisioned laboratory prototype. The SM developed in PEL is presented in **Fig. 2.22**, while the ratings are given in **Tab. 2.1**. Overall converter prototype ratings are given in **Tab. 2.2**.

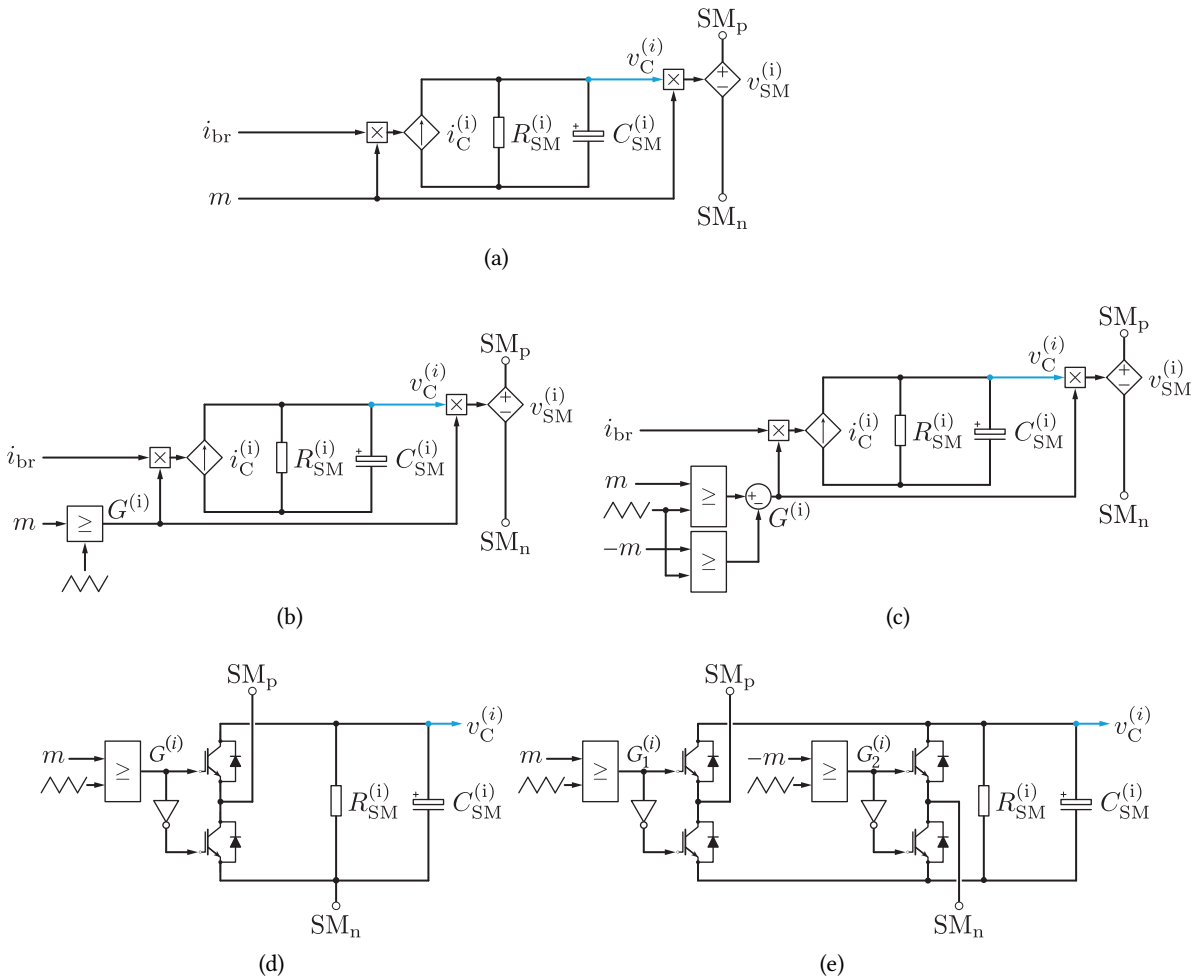


Fig. 2.21 Implemented SM models: averaged (a), fast switched HB with idealized switches (b), fast switched FB with idealized switches (c), switched HB (d), switched FB (e). Please notice that averaged model is fed with insertion index, while fast switched model receives gate switching signals.

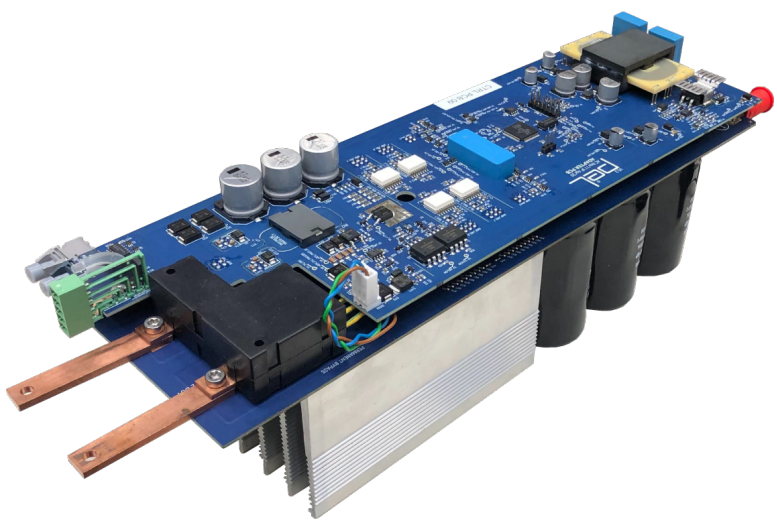


Fig. 2.22 MMC SM developed in PEL, for laboratory prototype converter.

Tab. 2.1 PEL SM ratings for the MMC prototype.

Rated voltage	V_{SM} =650 V
Maximum (trip) voltage	V_{SM} =800 V
Capacitance	C_{SM} =2.25 mF±10%
IGBT rated current	I_{IGBT} =70 A
IGBT rated voltage	V_{IGBT} =1200 V
IGBT switching frequency	f_{sw} =1 kHz

Tab. 2.2 PEL Three-Phase to Three-Phase (AC/AC) MMC prototype converter ratings, used as a reference for converter modeling within the thesis.

Line voltage	U_n =6 kV
Apparent power	S_n =500 kVA
Grid frequency	f_g =50 Hz
Number of SMs per branch	N_{SM} = 16
Branch inductance	L_{br} =2.5 mH
Branch inductance coupling coefficient	k_{br} = 0.3
Branch resistance	R_{br} =50 mΩ

It should be noted that PEL SM design is based on FB Semikron SKiiP 26GH12T4V11 IGBT module. The circuit is designed as a FB SM for research platform flexibility.

2.6 Model output evaluation

Modeling of MMC-specific, as well as higher-level control structures has been presented in the previous section. This section gives insight into model output in the same manner – from internal energy balancing structures towards grid-side controllers.

2.6.1 Internal MMC control

For internal energy balancing control evaluation, load power profile was set as in **Fig. 2.23**. All of the presented results are based on the inverter MMC stage.

2.6.1.1 Energy filtering

To properly assess MMC internal energy balancing, time-varying component of measured sum- and differential energy should be filtered-out, as shown in (2.34) and (2.35) and **Fig. 2.5**. Output of the filtering circuit (**Fig. 2.6**) is given in **Fig. 2.24**. Upper graph shows sum energy values – unfiltered, after first notch filter (ω_g), and after second notch filter ($2\omega_g$) in the cascade. Lower graph represents differential energy in the same manner. As sum energy oscillates with $2\omega_g$, the first filter has negligible effect, while the second significantly reduces oscillation amplitude. Naturally, phase is shifted as well, but this is tolerable as mean value is of interest. Looking at differential energy, oscillating with ω_g, the first filter reduces the amplitude and phase-shifts the signal, while the second filter has no significant effect.

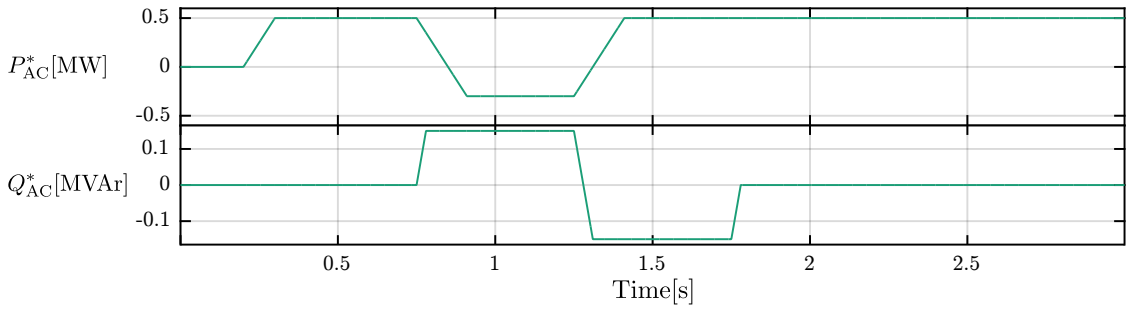


Fig. 2.23 Power profile used for balancing action validation.

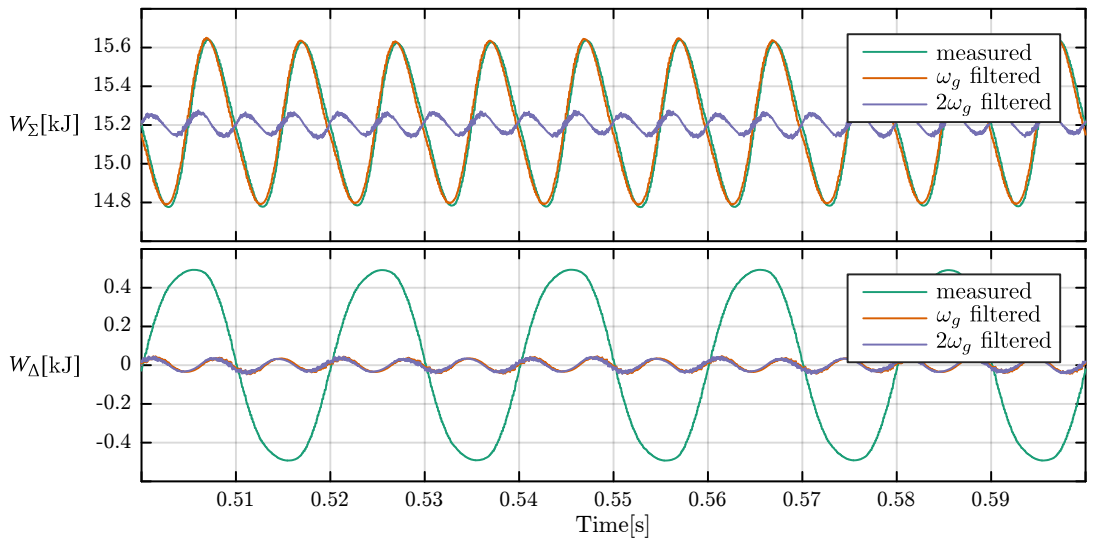


Fig. 2.24 Measured and filtered values of sum and differential energies of one MMC phase-leg are presented in the upper and lower graphs, respectively. As sum energy oscillates with $2\omega_g$, it is only affected by the second notch filter in the cascade (see **Fig. 2.6**). On the other hand, differential energy is oscillating at ω_g, and is thus affected by the first notch filter in the cascade.

2.6.1.2 Horizontal and vertical energy balancing

Internal MMC horizontal and vertical energy balancing actions must preserve equal energy share among converter phase-legs and among upper and lower phase branches, respectively. At the same time, balancing actions must not alter converter output at AC and DC terminals. **Fig. 2.25** presents the performance of the internal energy balancing controllers from **Secs. 2.3.3** and **2.3.4**. Converter is loaded with power profile from **Fig. 2.23**, while the energy controllers of interest are disabled during $T_{dis} \in [1.5\text{s}, 2.5\text{s})$. Looking at **Fig. 2.25**, the leftmost zoom-set presents balanced sum- and differential capacitor voltages. At time instant $t = 1.5$s, energy controllers are deactivated. Non-equal SM capacitance values (see **Tab. 2.1**) are taken into account by randomly assigning capacitance value to each SM at the start of each simulation. Without control over state of charge of branches and phase-legs, such non-equal capacitance values lead to divergence of sum- and differential voltages, i.e. energies. The second zoom-set depicts this divergence, however grid currents are balanced. At time instant $t = 2.5$s, balancing controllers are reactivated. Consequently, circulating current balancing action can be observed in third zoom-set, along with unaltered grid-side performance. Balancing is regained, as seen in the fourth zoom-set.

It should be noted that, although SM energy imbalance cannot be initially observed from the terminals, it would eventually lead to losing converter controlability, as some SMs overcharge and the others discharge outside of designed capacitor voltage band.

2.6.1.3 Total energy control

To evaluate model behavior, total energy reference test pattern from **Fig. 2.26** is used. Performance of total energy controller, implemented as in **Sec. 2.3.5**, can be seen in **Fig. 2.27**. MMC model is loaded with test power profile (**Fig. 2.23**). Total energy reference is based on rated SM capacitance and voltage level (**Tab. 2.1**), and calculated as in (2.52). It can, however, be altered during operation – to higher values for increase in available control action, or to lower values for decrease in losses.

Fig. 2.26 also confirms that total energy controller correctly tracks the reference value. Further, from **Fig. 2.27**, following the four zoom-sets from left to right, it can be observed that sum and differential capacitor voltages remain balanced, as well as that there is no distortion of grid-side quantities.

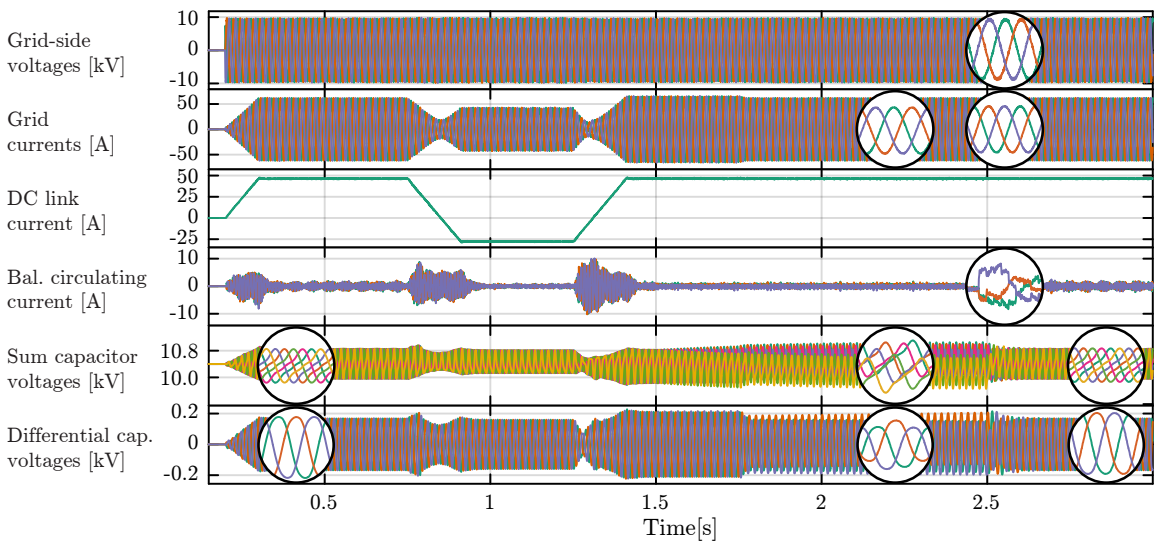


Fig. 2.25 Simulation sequence of the inverter stage MMC utilizing horizontal and vertical balancing circuits from **Secs. 2.3.3** and **2.3.4**. As can be seen, grid currents remain unaffected by the balancing control action at all times. During the period denoted by $T_{\text{dis}} \in [1.5\text{s}, 2.5\text{s})$, the energy balancing controller were disabled, which resulted in the SMs capacitor voltages divergence. Once the controllers were reactivated at time instant $t = 2.5\text{s}$, converter energies converged back to the nominal values.

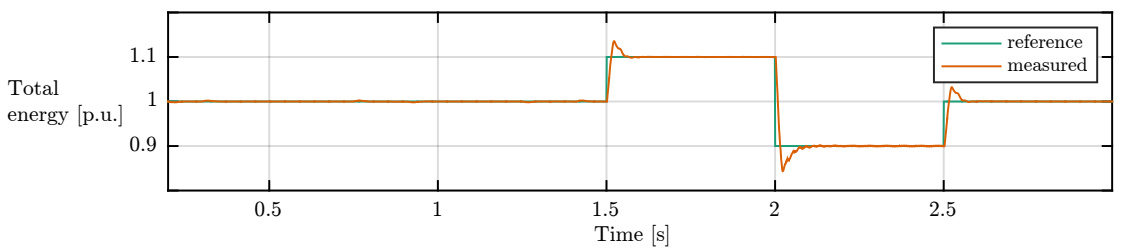


Fig. 2.26 Total energy reference and measured value, for a single MMC conversion stage. Values are per unit, with base given in (2.52).

It is clear from (2.52) that sum capacitor voltage envelope will follow the total energy reference, as seen in **Fig. 2.27**. Three positive and negative DC link current peaks, occurring at $t_1 = 1.5$s, $t_2 = 2$s and $t_3 = 2.5$s correspond to the additional charging or discharging of SMs' capacitors during transition to higher or lower total energy reference, respectively.

2.6.1.4 SM voltage balancing and modulation

Due to inevitable non-zero tolerance in SMs' capacitance values, balancing of SM voltage levels within each of the converter branches is performed as in **Sec. 2.3.7**. In the model, SM capacitance is set to a random value within the tolerance band of ±10%, as in **Tab. 2.1**. PSC-PWM modulation with min-max CM voltage injection is used, as discussed in **Sec. 2.3.8**. The output of the model is presented in **Fig. 2.28**. Eight phase-shifted carriers and a generated branch voltage reference can be seen in the topmost graph. SM gate signals are generated accordingly and seen in the next graph. The third graph validates proper balancing of SM capacitor voltages. The fourth graph presents multilevel branch voltage waveform, with $(N_{SM} + 1)$ levels.

2.6.2 Higher level control

Higher level controllers have been evaluated in back-to-back operation of both MMC stages. Exploited test power profile is presented in **Fig. 2.29**. As discussed in **Sec. 2.4.4**, active power can only be imposed on the inverter stage, while rectifier stage reference is calculated based on the load demand and eventual total energy variation requirements. Thus, active-power test profile is presented in the uppermost graph. Reactive power profiles of the rectifier and inverter can be independently set, and are chosen as in the middle and the lowermost graph, respectively.

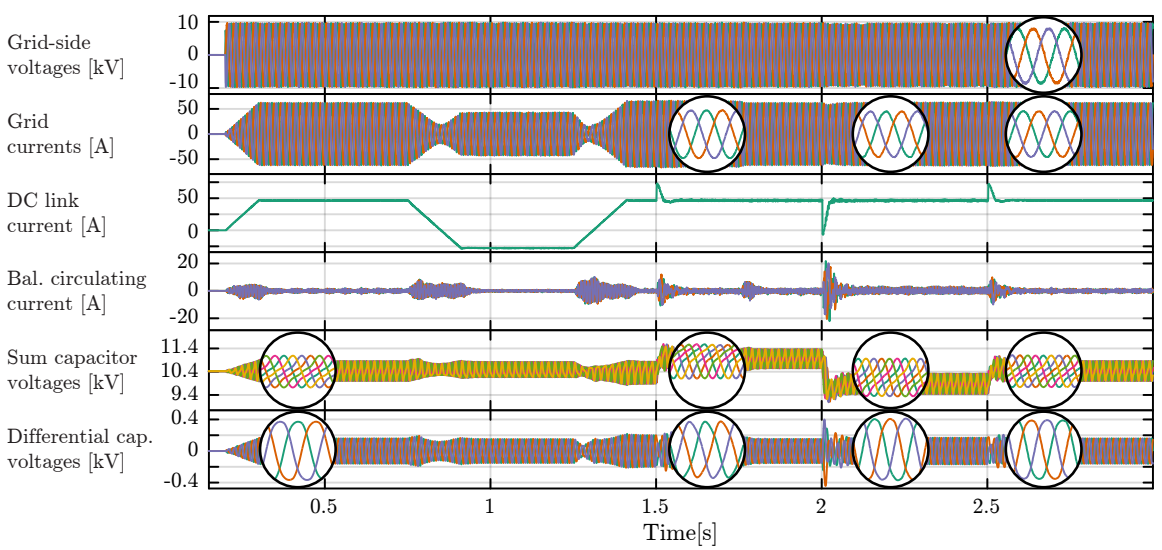


Fig. 2.27 Simulation sequence of the inverter stage MMC, which demonstrates proper operation of total energy controller. Stored energy reference is changed at time instants $t_1 = 1.5$s, $t_2 = 2$s and $t_3 = 2.5$s, according to **Fig. 2.26**. Looking from left to right, zoom-sets uncover decoupling of grid current from internal converter balancing action, confirming proper energy controller operation. Peaks in the DC link current correspond to charging and discharging of MMC capacitors during transition to new energy reference.

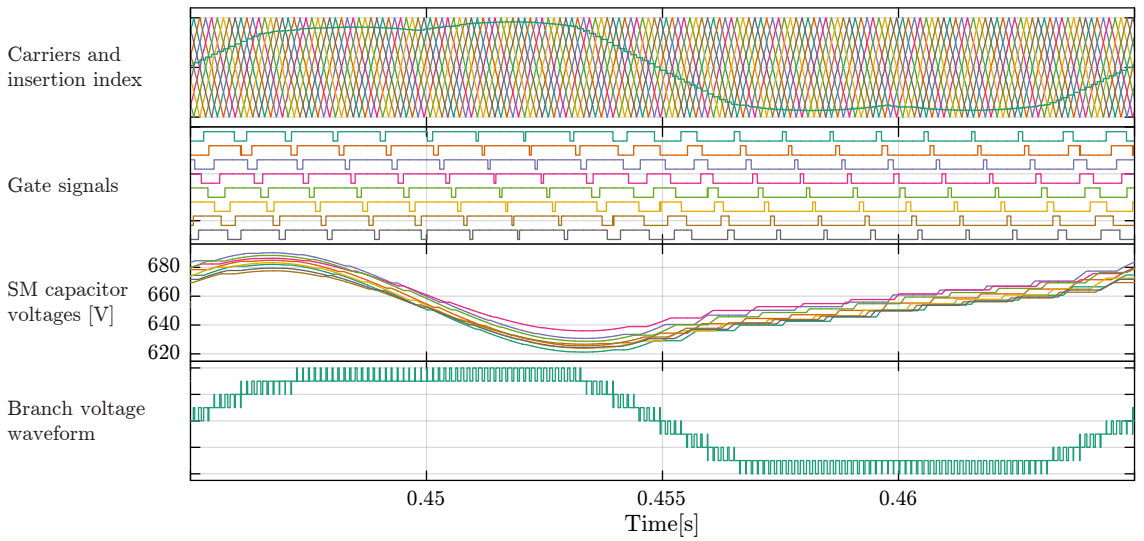


Fig. 2.28 Single 20 ms grid period simulation sequence of one MMC branch is displayed. Eight phase-shifted carriers, and a reference with CM voltage injection can be seen in the first graph. Generated branch gate signals are displayed in the second plot. The third plot confirms proper SM voltage balancing. The last plot depicts multilevel branch voltage waveform, with $(N_{SM} + 1)$ levels.

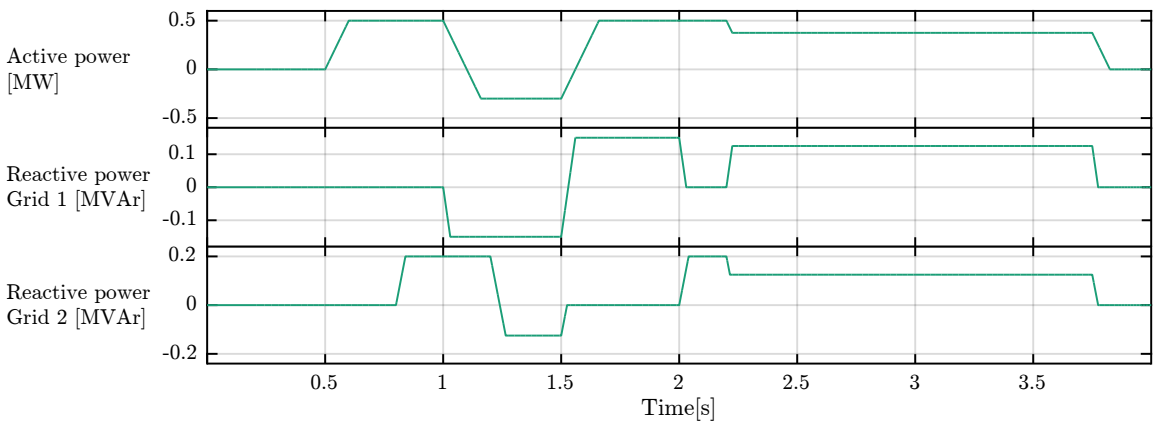


Fig. 2.29 Active and reactive power test profile for back-to-back operation of two MMC stages. Uppermost and lowermost graphs represent active and reactive power requirements of the Grid 2, respectively. Grid 1 active power reference is dependent on Grid 2 requirements, and thus cannot be set independently. In contrast, reactive power components of the two grids can be freely chosen within the operating area of the converters. The middle graph thus represents Grid 1 reactive power test profile.

2.6.2.1 PLL

PLL has been implemented as in **Sec. 2.4.1**. For the purpose of model verification, grid voltage is varied within ±10% of v_g, as seen in the uppermost graph of **Fig. 2.30**. Further, grid frequency is altered within ±3% around rated f_g, as in the lowermost graph. Grid voltage variation produces negligible response in the estimated frequency. Regarding grid frequency variation, PLL response settles within 100ms after the disturbance. The basic PLL suffices for symmetrical grid conditions.

2.6.2.2 GCC and PQ control

Two conversion stages of I-MMC are fed with power test profile from **Fig. 2.29**. Active and reactive power references are further converted to current references in *dq* reference frame and fed to GCC, as described in **Sec. 2.4.4**. GCC has been implemented as in **Sec. 2.4.2**. Output of the simulation model is presented in **Fig. 2.31**.

The topmost graph represents DC link current, which is proportional to the active power transferred between the two grids through the DC link.

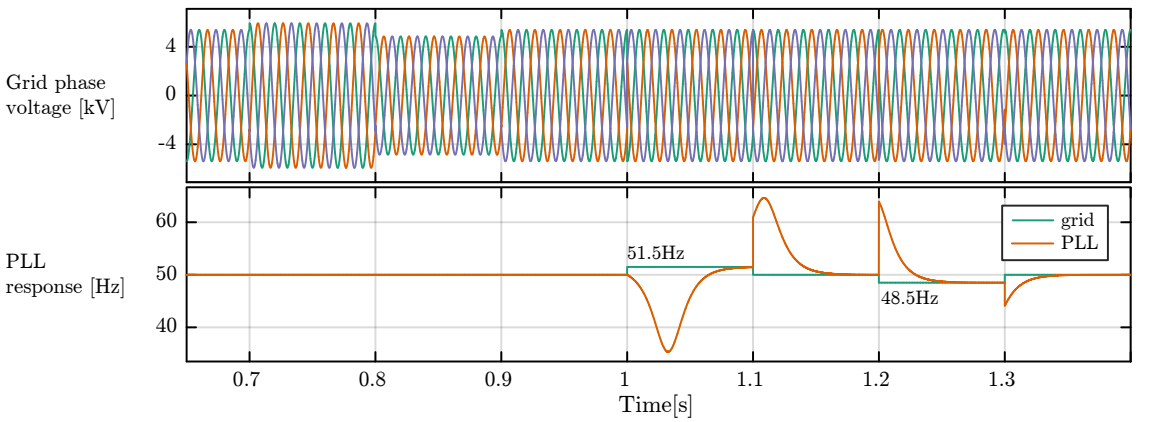


Fig. 2.30 Upper graph depicts grid voltage test pattern. At time instants $t_1 = 0.7$s, $t_2 = 0.8$s and $t_3 = 0.9$s amplitude is increased to $1.1v_g$, decreased to $0.9v_g$ and finally reset to rated value. Lowermost graph presents grid frequency test profile, and PLL response. Grid voltage disturbance produces insignificant frequency estimation error. PLL response to frequency variations settles within 100ms.

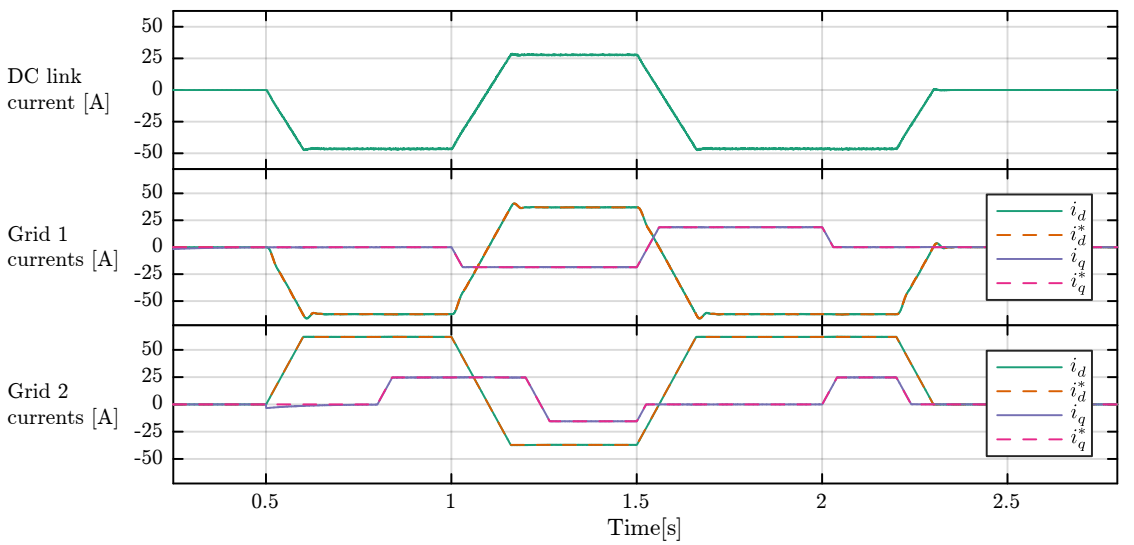


Fig. 2.31 Simulation sequence presenting GCC outputs in back-to-back operation of rectifier and inverter MMC stages. Lowermost graph confirms correct tracking of Grid 2 (inverter) current references, obtained from **Fig. 2.29**. Middle graph displays Grid 1 (rectifier) current components. Active power component tracks Grid 2 requirements, while reactive power component follows test profile reference. DC link current, presented in topmost graph, transfers active power among two grid terminals.

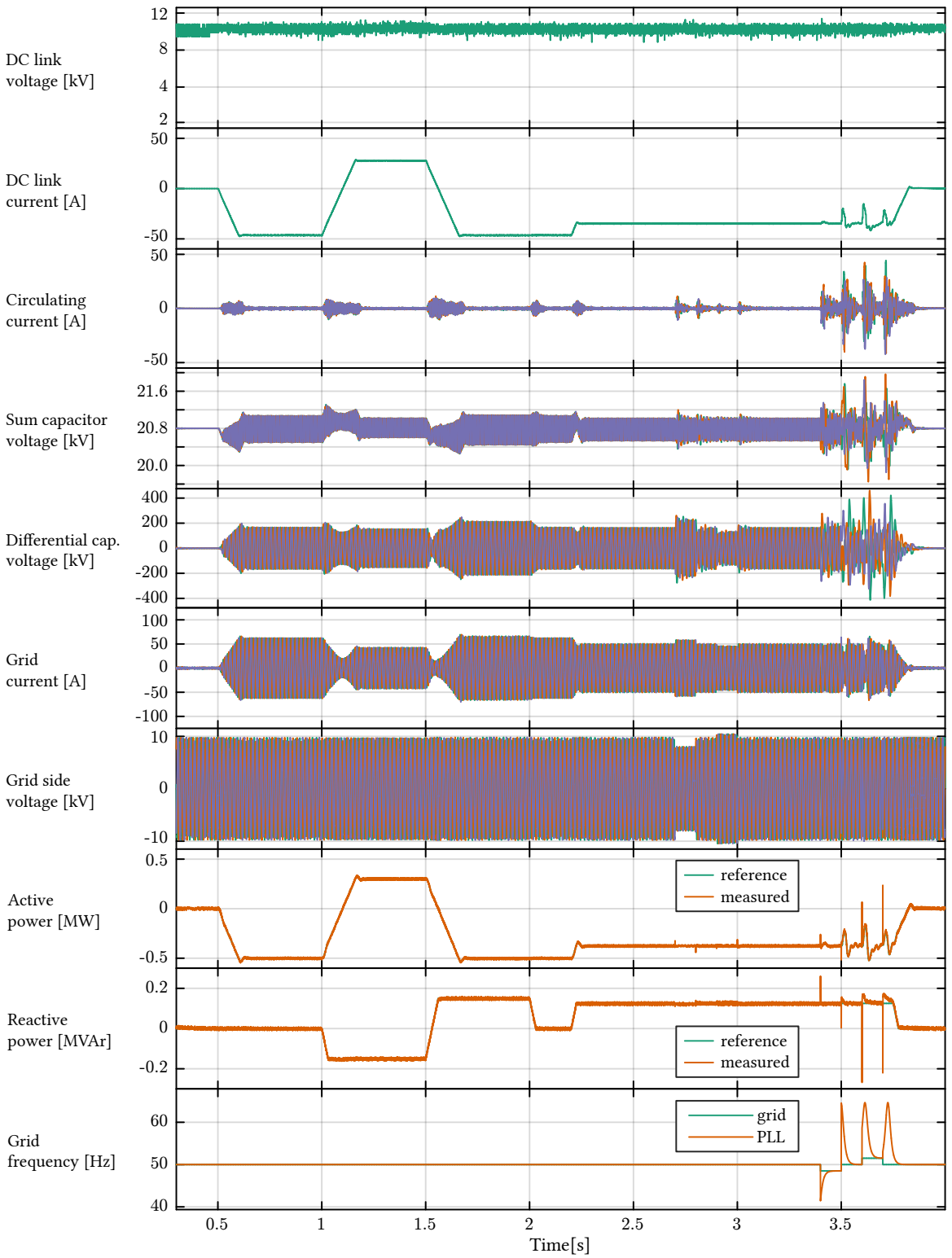


Fig. 2.32 Simulation results for MMC rectifier stage of the presented model, connected to 50 Hz grid. During time intervals $T_{f1} \in [3.0s, 3.1s)$ and $T_{f2} \in [3.2s, 3.3s)$, frequency diverges from rated by −3% and +3%, i.e. 48.5Hz and 51.5Hz, respectively. Voltage amplitude disturbance is present during $T_{v1} \in [2.3s, 2.4s)$ and $T_{v2} \in [2.5s, 2.6s)$, equaling $0.85v_{g1}$ and $1.1v_{g1}$, respectively.

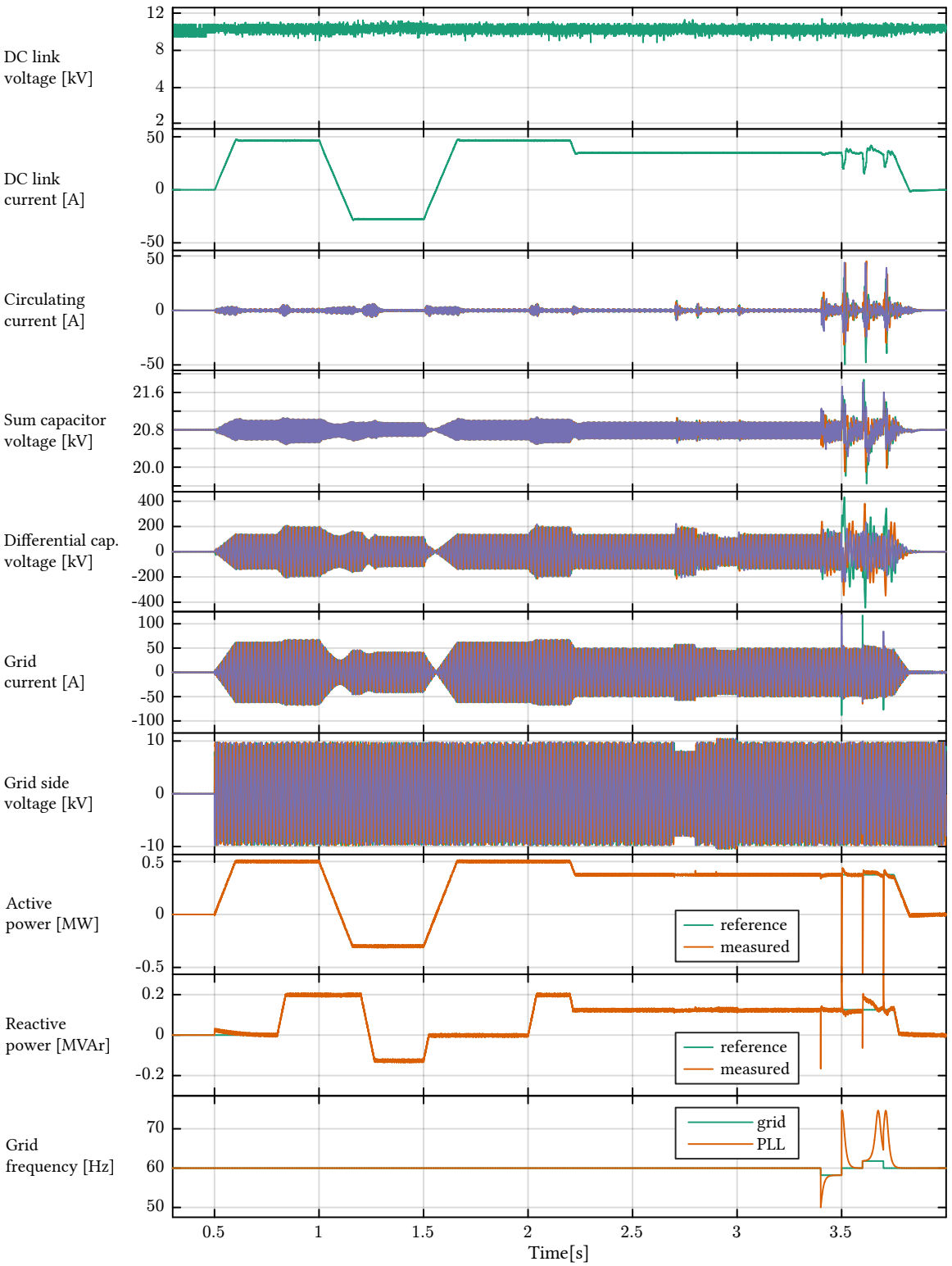


Fig. 2.33 Simulation results for MMC inverter stage of the presented model, connected to 60 Hz grid. During time intervals $T_{f3} \in [3.4s, 3.5s)$ and $T_{f4} \in [3.6s, 3.7s)$, frequency diverges from rated by -3% and $+3\%$, i.e. 58.2Hz and 61.8Hz, respectively. Voltage amplitude disturbance is present during $T_{v3} \in [2.7s, 2.8s)$ and $T_{v4} \in [2.9s, 3.0s)$, equaling $0.85v_{g2}$ and $1.1v_{g2}$, respectively.

The middle graph represents references and measured current components of rectifier stage's GCC. Active power demand of Grid 2, and the reactive power profile towards Grid 1, defined in **Fig. 2.29**, correspond to d and q current components, respectively.

The lowermost graph depicts inverter stage GCC references and measured currents. One can immediately see that d current component is of equal amplitude and opposite sign compared to the rectifier stage and the DC link current. Further, q current component complies with reactive power reference set towards Grid 2, as in **Fig. 2.29**.

2.6.3 Back-to-back operation behavior

Relevant output waveforms of rectifier and inverter conversion stages, for test load profile defined in **Fig. 2.29**, are given in **Figs. 2.32** and **2.33**, respectively. For test purposes, both conversion stages are subjected to grid-side disturbances in terms of voltage amplitude and frequency.

Grid 1 – during time intervals $T_{\mathrm{f1}} \in [3.0s, 3.1s)$ and $T_{\mathrm{f2}} \in [3.2s, 3.3s)$, frequency diverges from rated by -3% and $+3\%$, i.e. 48.5Hz and 51.5Hz, respectively. Voltage amplitude disturbance is present during $T_{\mathrm{v1}} \in [2.3s, 2.4s)$ and $T_{\mathrm{v2}} \in [2.5s, 2.6s)$, equaling $0.85v_{\mathrm{g1}}$ and $1.1v_{\mathrm{g1}}$, respectively.

Grid 2 – during time intervals $T_{\mathrm{f3}} \in [3.4s, 3.5s)$ and $T_{\mathrm{f4}} \in [3.6s, 3.7s)$, frequency diverges from rated by -3% and $+3\%$, i.e. 58.2Hz and 61.8Hz, respectively. Voltage amplitude disturbance is present during $T_{\mathrm{v3}} \in [2.7s, 2.8s)$ and $T_{\mathrm{v4}} \in [2.9s, 3.0s)$, equaling $0.85v_{\mathrm{g2}}$ and $1.1v_{\mathrm{g2}}$, respectively.

Concerning the internal MMC control, proper balancing- of sum and differential energies is achieved, while voltage ripple is lower than $\pm 10\%$. DC link voltage is kept constant throughout the rectifier-side grid voltage disturbances. Active and reactive power references are tracked correctly by the inverter stage. Active power of the rectifier stage is set by the inverter requirements, the converter losses and eventual total energy setpoint alterations, while reactive power follows the test profile. The converters are stable through voltage- and frequency amplitude disturbances in both grids. Frequency amplitude disturbances at T_{f1} to T_{f1} occur at time increments comparable to chosen PLL settling time.

2.7 Summary

This chapter presented MMC control loops and modeling of the converter implemented within the thesis. Starting from MMC governing equations, converter controllability is derived. Control outline of an I-MMC interfacing two fixed-frequency electrical grids has been presented as a starting point for assessing individual controllers. Internal converter energy control loops have been developed. Further, higher-level controllers are presented.

On the hardware side, SM models of various degree of fidelity, for higher- and lower-level of converter operation analysis, have been introduced. Model ratings, based on PEL prototype being developed, are listed and used throughout the rest of this thesis. Model output evaluation in back-to-back test scenario has been performed, as a verification of both internal and higher-level control loops.

Following the scope of the thesis, this chapter sets ground for the PHSP-specific control system alteration, presented and discussed in the following chapter. One fixed-frequency grid is replaced by a variable-speed Wound-Rotor Synchronous Machine (WRSM), while grid-code-compliant CM voltage injection based method is implemented and discussed.

3
Indirect MMC Control for PHSP Application

This chapter presents control structure of I-MMC for CFSM four-quadrant VSD. Starting from the model developed in ***Chap. 2****, grid on one side is replaced by a WRSM. Appropriate control actions, within so-called low-frequency mode, are added to allow for full output frequency range on machine side at rated torque. Grid-side control is extended for grid code compatibility. Upon detection of grid voltage- or frequency deviation, converter response complies with the grid code requirements. Grid support capabilities of PHSP in such events have been analyzed. Results of in-depth simulations are presented.*

3.1 Converter control outline

Outline of I-MMC control is presented in **Fig. 3.1**. Alterations to the previously introduced control layout for grid-to-grid operation (**Chap. 2**), are presented below.

- **Grid-side stage** operates in rectifier mode, performing DC-link voltage control. According to PHSP production schedule, active power reference is sent to the machine-side stage. Addi-

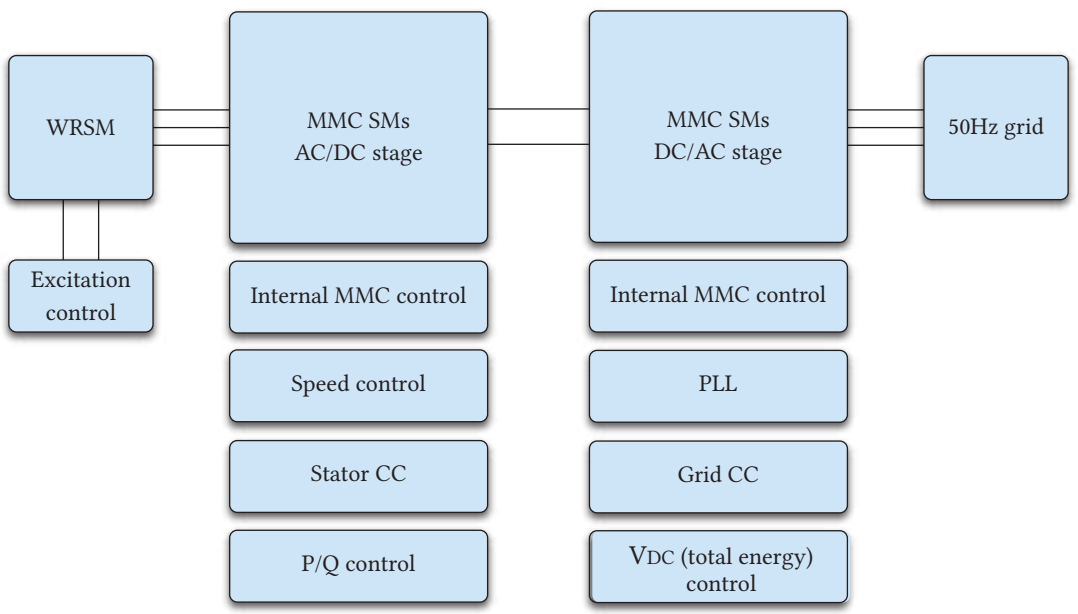


Fig. 3.1 Overview of the developed I-MMC model interfacing WRSM of a PHSP to a fixed-frequency AC grid. Rectifier and inverter stages are connected to 50 Hz grid and WRSM, respectively. Excitation current control is realized through a buck converter.

tionally, to comply with the grid code, grid-side control provides modifications to active power reference of the machine in case of grid-side faults or asymmetries.

- **Machine-side stage** operates in inverter mode, performing Field-Oriented Control (FOC) of a WRSM. Active power reference is obtained from the grid side. Reactive power reference is based on machine rated parameters, but can be kept as low as zero concerning the MMC control. Speed controller determines speed setpoint on the basis of the head level and the active power reference from the grid-side, to obtain maximal efficiency. Stator current control realizes the necessary shaft torque to control the machine speed. In pump mode, guide vane position is controlled to maximize efficiency and unit stability margin.

3.2 Internal MMC control for LF operation

As shown in **Chap. 1**, I-MMC is a promising solution for variable speed operation of high-power PHSPs. Inherently modular structure, redundancy, high-quality output voltage waveform, decoupling of machine from the grid, as well as provision of ancillary services can be achieved. This makes the I-MMC topology superior to well-established DFIM units, monolithic-converter-fed WRSM [13], as well as D-MMC-fed WRSM rated at grid frequency [23].

Chap. 2 presented I-MMC control system for interconnection of two AC systems, operating in a grid-code-defined narrow band around their rated frequencies. In PHSP, variable-speed machine, i.e. variable-frequency 3PH system is interfaced to a fixed-frequency 3PH electric grid **Fig. 3.2**.

Drive units in PHSP application should allow for multiple operating regimes:

- Controlled start from zero-speed in pump or turbine mode
- Variable speed operation around rated speed
- Switch-over from turbine to pump operating mode and vice versa
- Sufficient torque over the entire speed (frequency) range, to allow for operating mode change-over without dewatering

Consequently, control system of machine-side MMC stage must be appropriately modified to allow for LF operation occurring during machine start-up and pump/turbine operating mode change-over.

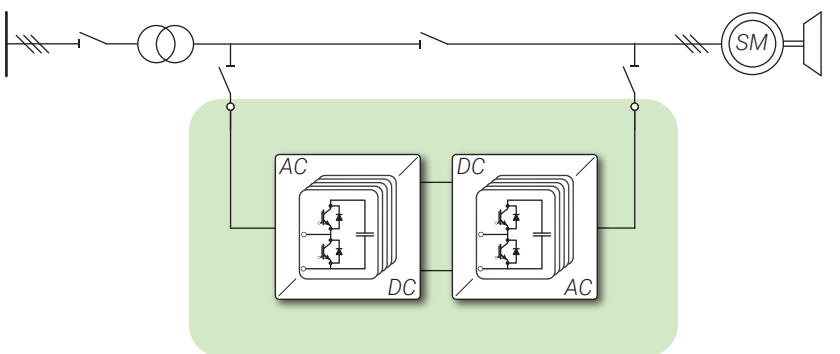


Fig. 3.2 I-MMC layout for PHSP application.

3.2.1 SM-level energy ripple in LF operation

Starting from branch-level current and inserted voltage expressions, instantaneous branch power can be expressed.

$$i_{\{p,n\}x} = i_{cx} \pm \frac{i_{sx}}{2} \tag{3.1}$$

$$v_{\{p,n\}x} = v_{cx} \mp v_{sx} \tag{3.2}$$

$$p_{\{p,n\}x} = v_{\{p,n\}x} i_{\{p,n\}x} \tag{3.3}$$

Assuming the converter is ideally balanced, i.e. no balancing components of circulating currents and CM voltage exist, components of (3.1) and (3.2) can be written. For simplicity, upper branch of phase a is observed. Under such presumptions, the following holds:

$$i_c = \frac{I_{dc}}{3} \tag{3.4}$$

$$i_s = \frac{\hat{i}s}{2}\cos(\omega_s t - \varphi) \tag{3.5}$$

$$v_c = \frac{V_{dc}}{2} \tag{3.6}$$

$$v_s = m_s \frac{V_{dc}}{2}\cos(\omega_s t) \tag{3.7}$$

where m_s represents AC-side modulation index. In an ideally balanced converter, total inserted branch voltage is equally shared among SMs. Instantaneous SM power is derived as:

$$p_{SM} = \frac{1}{N_{SM}}\left(\frac{V_{dc}}{2} - m_s\frac{V_{dc}}{2}\cos(\omega_s t)\right)\left(\frac{I_{dc}}{3} + \frac{I_s}{2}\cos(\omega_s t - \varphi)\right) \tag{3.8}$$

Average SM power, denoted $\overline{p_{SM}}$, must equal zero as the C_{SM} only buffers energy oscillations, while energy is exchanged at active power between AC and DC terminals.

$$\begin{aligned}\overline{p_{SM}} &= \frac{V_{dc}}{N_{SM}}\left\{\frac{I_{dc}}{6} - m_s\frac{\hat{i}_s}{8}\cos(\varphi) + \underbrace{\frac{\hat{i}_s}{4}\cos(\omega_s t - \varphi) - m_s\frac{I_{dc}}{6}\cos(\omega_s t) - m_s\frac{\hat{i}_s}{8}\cos(2\omega_s t - \varphi)}_{\text{zero average}}\right\} \\ &= 0\end{aligned} \tag{3.9}$$

Relationship between i_c and i_s from (3.4) and (3.5) can thus be determined, according to the zero-average condition (3.9).

$$I_{dc} = \frac{3m_s}{4}\hat{i}_s\cos(\varphi) \tag{3.10}$$

Time-varying zero-average components of p_{SM} can be rewritten.

$$\tilde{p}_{SM} = \frac{V_{dc}\hat{i}_s}{4N_{SM}}\left\{\cos(\omega_s t - \varphi) - \frac{m_s^2}{2}\cos(\varphi)\cos(\omega_s t) - \frac{m_s}{4}\cos(2\omega_s t - \varphi)\right\} \tag{3.11}$$

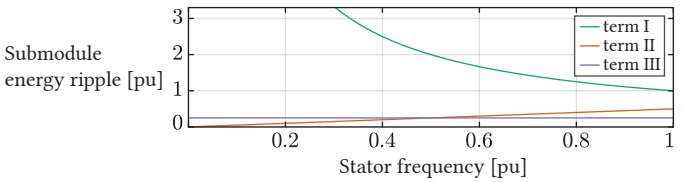


Fig. 3.3 Frequency dependence of SM energy ripple components (3.12). The first term is dominant in LF region.

Integrating instantaneous AC power of a SM, (3.11), AC component of SM energy is obtained.

$$\begin{aligned}\tilde{w}_{\mathrm{SM}} &= \int \tilde{p}_{\mathrm{SM}}\,\mathrm{d}t \\ &= \frac{V_{\mathrm{dc}}\hat{i}_s}{4N_{\mathrm{SM}}}\left\{\underbrace{\frac{1}{\omega_s}\sin(\omega_s t-\varphi)}_{\text{decreases with }\omega_s} - \underbrace{\frac{m_s^2}{2\omega_s}\cos(\varphi)\sin(\omega_s t)}_{\text{increases with }\omega_s} - \underbrace{\frac{m_s}{4\omega_s}\sin(2\omega_s t-\varphi)}_{\text{constant}}\right\}\end{aligned} \tag{3.12}$$

In CFSM constant-torque application, stator current amplitude is constant (3.13). Ratio of stator voltage amplitude and angular electrical frequency ω_s is approximately constant in range up to the rated speed $\left(0 \ldots \omega_{s,\mathrm{rated}}\right]$ (3.14).

$$\hat{i}_s \approx \text{const.} \tag{3.13}$$

$$\frac{\hat{v}_s}{\omega_s} \approx \text{const.} \tag{3.14}$$

Keeping in mind the output AC voltage expression (3.15), SM energy ripple behavior can be characterized within the entire operating speed range of the machine.

$$\hat{v}_s = \frac{m_s V_{\mathrm{dc}}}{2} \tag{3.15}$$

Three members of SM energy ripple equation (3.12) manifest different dependency on output frequency, as illustrated in **Fig. 3.3**.

- The first member is dominant in LF region, decreasing with higher output frequency.
- The second member increases with output frequency according to (3.14) and (3.15), and thus should not be considered in LF region.
- The third member is constant according to (3.14) and (3.15).

During LF operation, as well as during ride-though LF region while accelerating the machine, very high energy oscillations at low stator frequency are caused by the first member of (3.12) [30].

Capacitor voltage ripple can be derived.

$$\begin{aligned}\Delta\tilde{w}_{\mathrm{SM}} &= \frac{1}{2}C_{\mathrm{SM}}\left(v_{\mathrm{C,max}}^2 - v_{\mathrm{C,min}}^2\right) \\ &= \frac{1}{2}C_{\mathrm{SM}}\left((\bar{v}_C + \Delta v_C)^2 - (\bar{v}_C - \Delta v_C)^2\right) \\ &= 2C_{\mathrm{SM}}\bar{v}_C\Delta v_C\end{aligned} \tag{3.16}$$

Assuming average SM capacitor voltage is controlled to V_{SM}, capacitor voltage ripple can be rewritten.

$$\Delta v_{\mathrm{C}} = \frac{\Delta \tilde{w}_{\mathrm{SM}}}{2C_{\mathrm{SM}}\bar{v}_{C}} = \frac{\Delta \tilde{w}_{\mathrm{SM}}}{2C_{\mathrm{SM}}V_{\mathrm{SM}}} \tag{3.17}$$

SM capacitor voltage ripple dynamics is equal to SM energy ripple dynamics, in terms of dependency on MMC output frequency. Thus, according to (3.12) and (3.17), the dominant member of capacitor voltage ripple is identified.

$$\Delta v_{\mathrm{C,dom,lf}} = \frac{1}{2C_{\mathrm{SM}}V_{\mathrm{SM}}} \cdot \frac{V_{\mathrm{DC}}\hat{i}_{s}}{4N_{\mathrm{SM}}} \cdot \frac{1}{\omega_{s}} \sin(\omega_{s}t - \varphi) \tag{3.18}$$

Setting branch-level sum capacitor voltage reference $v_{C\Sigma p}$, $v_{C\Sigma n}$ to rated V_{DC} value [49], and introducing arbitrary DC-link voltage reference value, (3.18) can be rewritten.

$$v^{*}_{\mathrm{C}\Sigma} = V_{\mathrm{DC,n}} \tag{3.19}$$

$$V^{*}_{\mathrm{DC}} = k_{\mathrm{DC}}V_{\mathrm{DC,n}} \tag{3.20}$$

$$\Delta v_{\mathrm{C,dom,lf}} = \frac{k_{\mathrm{DC}}\hat{i}_{s}}{8C_{\mathrm{SM}}\omega_{s}} \sin(\omega_{s}t - \varphi) \tag{3.21}$$

Analyzing (3.21), multiple approaches to capacitor voltage ripple limitation during LF operation are possible.

- **CM voltage injection** – High frequency, e.g. $\omega_{\mathrm{s,rated}}$, CM voltage component is supplied to phase legs, to shift energy oscillation to higher frequencies, the domain SM capacitors are designed for [30], [51], [52]. In such a case, vertical energy balancing of the converter relies on such higher-frequency voltage instead of the LF AC voltage component. Industry-standard HB SM topology can be used, at the expense of CM voltage being present at machine neutral point and additional current stress to the machine-side converter stage.
- **DC-link voltage variation** – It is clear from (3.21) that, if the ratio of DC-link voltage reference to stator frequency is kept constant, SM voltage ripple will be constant [39]. Lowering DC-link voltage level, however, requires that all or part of the SMs are realized as FB units. CM voltage is not introduced to the machine, at the expense of higher initial cost of the converter, as well as higher losses in exploitation.

As CFSM can be designed with insulated bearings and appropriate insulation for operation under CM voltage presence, this section is based around CM voltage injection approach, taking the advantage of HB SM design. However, in retrofit applications, where older machines, designed for grid voltage waveform operation are used, further investment in variable DC-link voltage solution may be of interest.

3.2.2 Common-mode voltage injection

As shown in the literature [30], injection of CM voltage can shift SM energy oscillation to the higher-frequency domain, for which capacitors are designed in terms of the resulting ripple. Care should be taken, however, as supplied CM voltage interacts with branch currents, introducing additional non-zero power components that should be compensated.

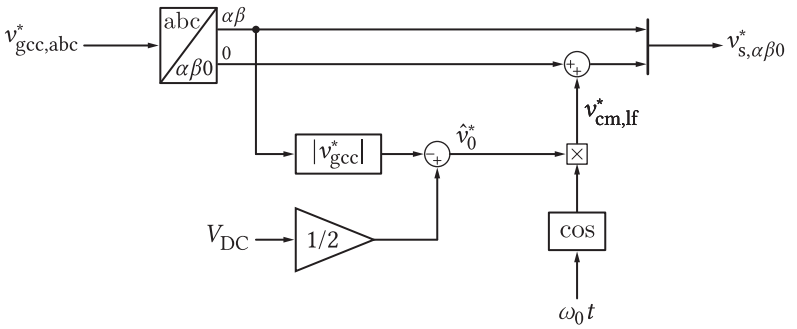


Fig. 3.4 CM voltage reference generation for LF mode energy balancing action. The highest available amplitude is used to minimize circulating current amplitude.

Injected CM voltage can be of arbitrary waveform and frequency, e.g. sine-wave [30], [31] or square [52]. This section considers sine-wave voltage of rated machine frequency.

$$v_0 = \hat{v}_0 \cos(\omega_0 t) \tag{3.22}$$

The amplitude is limited by the available DC-link voltage, and the applied stator voltage. Within LF range, output voltage amplitude is rather low, as shown in (3.14), thus considerable magnitude range is available for CM voltage.

$$\hat{v}_{0,\max} = \frac{V_{DC}}{2} - \hat{v}_s \tag{3.23}$$

For converter balancing within the LF region, higher voltage amplitude is desired, as it results in lower balancing circulating current requirement for the same balancing power of energy exchange. On the contrary, higher CM voltage amplitude introduces higher stress to the machine. CM voltage injection implementation is presented in **Fig. 3.4**.

To analyze the influence of CM voltage, equations (3.4) to (3.7) are rewritten.

$$i_c = I_{c,DC} + \hat{i}_{c,AC} \cos(\omega_c t) \tag{3.24}$$

$$i_s = \frac{\hat{i}s}{2} \cos(\omega_s t - \varphi_s) \tag{3.25}$$

$$v_c = \frac{V_{dc}}{2} \tag{3.26}$$

$$v_{s0} = \hat{v}_s \cos(\omega_s t) + \hat{v}_0 \cos(\omega_0 t) \tag{3.27}$$

Branch power equations can be written (3.1) to (3.3).

$$\begin{aligned} p_{\{p,n\}x} &= (v_{cx} \mp v_{sx}) \cdot \left(i_{cx} \pm \frac{i_{sx}}{2} \right) \\ &= \left(\frac{V_{DC}}{2} \mp \hat{v}_s \cos(\omega_s t) \mp \hat{v}_0 \cos(\omega_0 t) \right) \cdot \left(I_{c,DC} + \hat{i}_{c,AC} \cos(\omega_c t) \pm \frac{\hat{i}s}{2} \cos(\omega_s t - \varphi_s) \right) \\ &= \frac{V_{DC} I_{c,DC}}{2} + \frac{V_{DC} \hat{i}_{c,AC}}{2} \cos(\omega_c t) \pm \frac{V_{DC} \hat{i}_s}{4} \cos(\omega_s t - \varphi_s) \\ &\mp \hat{v}_s I_{c,DC} \cos(\omega_s t) \mp \hat{v}_s \hat{i}_{c,AC} \cos(\omega_s t) \cos(\omega_c t) - \frac{\hat{v}_s \hat{i}_s}{2} \cos(\omega_s t) \cos(\omega_s t - \varphi_s) \\ &\mp \hat{v}_0 I_{c,DC} \cos(\omega_0 t) \mp \hat{v}_0 \hat{i}_{c,AC} \cos(\omega_0 t) \cos(\omega_c t) - \frac{\hat{v}_0 \hat{i}_s}{2} \cos(\omega_0 t) \cos(\omega_s t - \varphi_s) \end{aligned} \tag{3.28}$$

Within LF mode, AC component of circulating current can be assigned the same frequency as CM voltage, to enable active power transfer between upper and lower branches of each phase-leg.

$$\omega_c = \omega_0 = \omega_{\text{s,rated}} \tag{3.29}$$

Equation (3.28) can be rewritten.

$$\begin{aligned} p_{\{\text{p,n}\}\text{x}} = {} & \frac{V_{\text{DC}} I_{\text{c,DC}}}{2} + \underbrace{\frac{V_{\text{DC}} \hat{i}_{\text{c,AC}}}{2} \cos(\omega_0 t)}_{\text{HF zero-mean}} \pm \frac{V_{\text{DC}} \hat{i}_s}{4} \cos(\omega_s t - \varphi_s) \\ & \mp \hat{v}_s I_{\text{c,DC}} \cos(\omega_s t) \mp \underbrace{\frac{\hat{v}_s \hat{i}_{\text{c,AC}}}{2} (\cos((\omega_0 - \omega_s)t)}_{\text{HF zero-mean}} \mp \underbrace{\frac{\hat{v}_s \hat{i}_{\text{c,AC}}}{2} (\cos((\omega_0 + \omega_s)t)}_{\text{HF zero-mean}} \\ & - \frac{\hat{v}_s \hat{i}_s}{4} \cos(\varphi_s) - \frac{\hat{v}_s \hat{i}_s}{4} \cos(2\omega_s t - \varphi_s) \\ & \mp \underbrace{\hat{v}_0 I_{\text{c,DC}} \cos(\omega_0 t)}_{\text{HF zero-mean}} \mp \frac{\hat{v}_0 \hat{i}_{\text{c,AC}}}{2} \mp \underbrace{\frac{\hat{v}_0 \hat{i}_{\text{c,AC}}}{2} \cos(2\omega_0 t)}_{\text{HF zero-mean}} \\ & - \underbrace{\frac{\hat{v}_0 \hat{i}_s}{4} \cos((\omega_0 - \omega_s)t + \varphi_s)}_{\text{HF zero-mean}} - \underbrace{\frac{\hat{v}_0 \hat{i}_s}{4} \cos((\omega_0 + \omega_s)t - \varphi_s)}_{\text{HF zero-mean}} \end{aligned} \tag{3.30}$$

High Frequency (HF) fluctuations of (3.30) are buffered by SM capacitors. Non-zero-mean members, as well as zero-mean LF members are of interest for LF balancing action. Sum- and differential leg-level power components are thus obtained, excluding HF zero-mean members.

$$\begin{aligned} p_{\Sigma\text{x,lf}} &= p_{\text{px,lf}} + p_{\text{nx,lf}} = 2 v_c i_c - v_s i_s \\ &= V_{\text{DC}} I_{\text{c,DC}} - \frac{\hat{v}_s \hat{i}_s}{2} \cos(\varphi_s) - \frac{\hat{v}_s \hat{i}_s}{2} \cos(2\omega_s t - \varphi_s) \end{aligned} \tag{3.31}$$

$$\begin{aligned} p_{\Delta\text{x,lf}} &= p_{\text{px,lf}} - p_{\text{nx,lf}} = v_c i_s - 2 v_s i_c \\ &= \frac{V_{\text{DC}} \hat{i}_s}{2} \cos(\omega_s t - \varphi_s) - 2 \hat{v}_s I_{\text{c,DC}} \cos(\omega_s t) - \hat{v}_0 \hat{i}_{\text{c,AC}} \end{aligned} \tag{3.32}$$

Feed-forward AC and DC components of circulating current are calculated for mitigation of LF components of sum- and differential leg-level power.

$$p_{\Sigma\text{x,lf}} = 0 \tag{3.33}$$

$$p_{\Delta\text{x,lf}} = 0 \tag{3.34}$$

Per-phase feed-forward circulating current components are calculated for LF operation.

$$I_{\text{c,DC,ff}} = \frac{\hat{v}_s \hat{i}_s}{2 V_{\text{DC}}} (\cos(\varphi_s) + \cos(2\omega_s t - \varphi_s)) = \frac{v_s i_s}{V_{\text{DC}}} \tag{3.35}$$

$$\hat{i}_{\text{c,AC,ff}} = \frac{1}{\hat{v}_0} \left\{ \underbrace{\frac{V_{\text{DC}} \hat{i}_s}{2} \cos(\omega_s t - \varphi_s)}_{\text{3-ph zero-sum}} - \underbrace{2 \hat{v}_s I_{\text{c,DC}} \cos(\omega_s t)}_{\text{3-ph zero-sum}} \right\} \tag{3.36}$$

DC components of (3.35) are simply equalization of AC and DC instantaneous active power flow values, per phase. AC components of (3.36) sum up to zero, consequently control action will not be visible from converter terminals.

3.2.3 Horizontal energy balancing

As presented, leg-level energy oscillations are shifted to HF values through the introduction of CM voltage. HF energy ripple is buffered in SM capacitors. Mean value of measured energy is controlled in the same manner as demonstrated for HF operation (**Sec. 2.3.3**).

However, non-zero-mean and LF components also exist in the spectrum (3.31). These are mitigated by feed-forward circulating current component (3.35). Horizontal energy balancing control for LF operation, including feed-forward member, is presented in **Fig. 3.5**.

3.2.4 Vertical energy balancing

Similar to the case of horizontal energy balancing, differential leg-level energy oscillation is shifted to higher frequency range. Control is performed taking filtered energy measurements into account, i.e. average energy is controlled. Contrary to HF mode, AC circulating current is not interacting with symmetrical 3PH output voltage, as output frequency reaches as low as zero value during machine LF operation. Instead, HF CM voltage component is used to exchange energy in vertical direction.

Consequently, HF control approach presented in **Fig. 2.9** is modified. Per-phase AC balancing power references are calculated. Current amplitudes are obtained for the actual amplitude of available CM voltage. There is no phase disposition among phase currents; following the adopted waveform (3.24), multiplication of amplitude reference with $\cos(\omega_0 t)$ is performed.

Non-zero-mean and LF components from (3.32) spectra are mitigated by means of feed-forward current injection. Values obtained in (3.36) are used. Vertical energy balancing control for LF operation, including feed-forward terms, is depicted in **Fig. 3.6**.

3.2.5 Start-up and switch-over between LF and HF mode

With the increase of MMC output frequency, energy balancing approach should be transitioned from LF to HF method due to the following effects:

- Increase of frequency implies decrease of SM capacitor voltage ripple, towards the region where ripple buffering can be performed within acceptable SM voltage ripple.

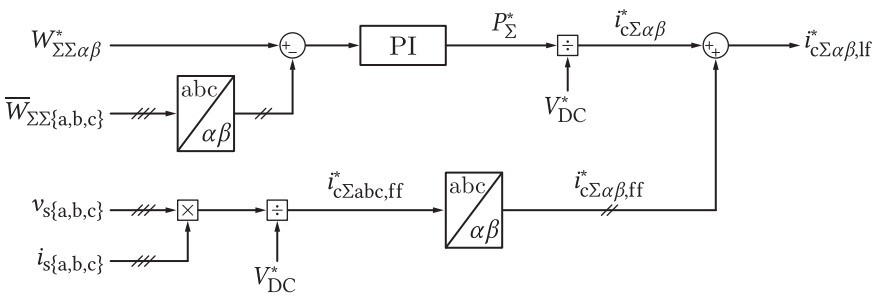


Fig. 3.5 Horizontal energy balancing implementation for one MMC stage operating in LF mode. Observed energy is a filtered value, as average components are of interest and HF oscillations are buffered by SM capacitors. To achieve even horizontal energy distribution, $\alpha\beta$ components are referenced to zero. Additional feed-forward component is injected to mitigate non-zero-mean and LF oscillations that cannot be buffered.

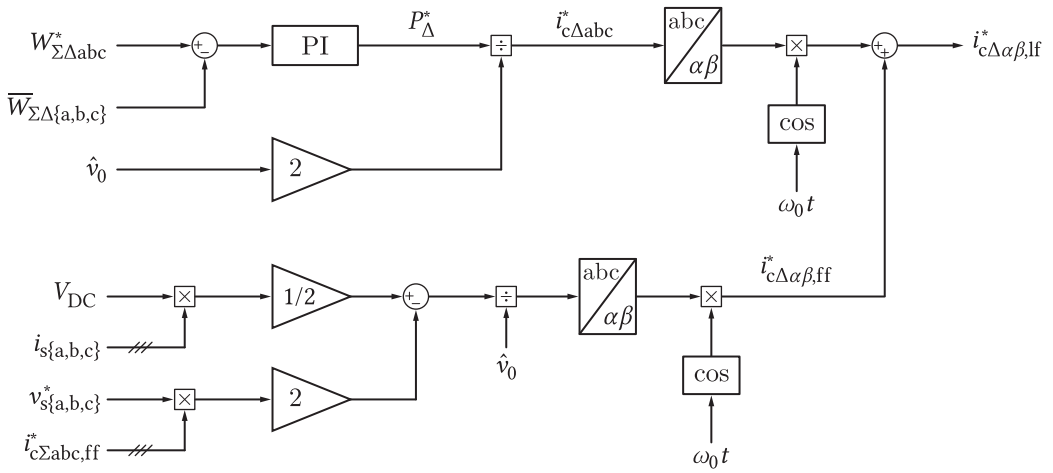


Fig. 3.6 Vertical energy balancing implementation for one MMC stage operating in LF mode. Observed energy is a filtered value, as average components are of interest and HF oscillations are buffered by SM capacitors. To achieve even vertical energy distribution, $\alpha\beta$ components are referenced to zero. Additional feed-forward component is injected to mitigate non-zero-mean and LF oscillations that cannot be buffered.

- Increase of stator voltage amplitude leads to decrease of available CM voltage amplitude, further implying higher circulating current amplitudes for balancing task (3.23).
- Frequency and amplitude of stator output voltage are high enough to switch to HF balancing.

Converter output frequency range can be split into three regions, regardless of the direction of rotation:

- LF – covering start-up, stopping, change of direction through zero-speed. Frequency range covers $(0 \dots \omega_{lf}]$.
- Switch-over – enabling smooth transition between the two balancing methods. Frequency range covers $(\omega_{lf} \dots \omega_{hf}]$.
- HF – covering variable-speed operation above switch-over area, i.e. $\left(\omega_{hf} \dots \omega_{s,rated}\right]$.

There is naturally a freedom in choice of region boundaries ω_{lf} and ω_{hf}. Choosing too low values results in high SM capacitor ripple upon switch-over to the HF region, as $1/\omega_s$ member after transition will still be very high. Choosing too high values imposes additional circulating current amplitude requirement, due to inverse proportionality of available CM voltage amplitude and output frequency (3.14) and (3.23). The following values are adopted.

$$f_{lf} = 15\,\text{Hz} \qquad \omega_{lf} = 30\pi\,\text{rad/s} \tag{3.37}$$

$$f_{hf} = 20\,\text{Hz} \qquad \omega_{hf} = 40\pi\,\text{rad/s} \tag{3.38}$$

Considering hydraulic pump application in PHSP, where pumping action requires operation above roughly 40 % of rated speed, MMC would dominantly operate in the HF region.

$$k_{hf} = \begin{Bmatrix} 0 & |\omega_s| \in (0 \dots \omega_{lf}] \\ \frac{|\omega_s| - \omega_{lf}}{\omega_{hf} - \omega_{lf}} & |\omega_s| \in (\omega_{lf} \dots \omega_{hf}] \\ 1 & |\omega_s| \in \left(\omega_{hf} \dots \omega_{s,rated}\right] \end{Bmatrix} \tag{3.39}$$

$$k_{\mathrm{lf}} = 1 - k_{\mathrm{hf}} \tag{3.40}$$

Transition is performed through the introduction of LF and HF coefficients – k_{lf} and k_{hf}, respectively [31]. In the switch-over frequency region, superposition of LF and HF balancing methods is active. Control switch-over implementation is presented in **Fig. 3.7**. CM voltage is injected without reduction throughout the transition process. HF circulating current components gradually take over control action from LF components during frequency increase; the opposite is true during frequency decrease.

CM voltage injection approach during machine start-up is presented in **Fig. 3.8**. LF to HF switch-over is performed from (3.37) to (3.38), within $T \in (1.3\,\mathrm{s} \ldots 1.4\,\mathrm{s}]$. After this interval, the converter operates in HF mode, where CM voltage is only introduced to improve DC-link utilization, as shown in **Sec. 2.3.8.1**.

Balancing components of internal MMC circulating currents differ for both horizontal and vertical energy balancing actions (**Secs. 3.2.3** and **3.2.4**). Switch-over is performed continuously during the switch-over interval $[\omega_{\mathrm{lf}} \ldots \omega_{\mathrm{hf}})$, as defined in **Fig. 3.7**. Circulating current components of machine-side MMC in $\alpha\beta$ reference frame, during frequency ramp-up sequence, under constant output current (torque) load, are presented in **Fig. 3.9**. Feed-forward AC and DC members are injected in LF mode only, to mitigate LF leg-level energy oscillations. Horizontal balancing DC current reference is calculated equally over the range. Vertical balancing AC current is interacting with HF CM voltage in LF range, followed by output frequency AC voltage in HF range. During the switch-over, both LF and HF current components proportionally contribute to the balancing action. It can be noted that high amplitude of AC feed-forward circulating currents, relative to output current, are necessary for balancing action.

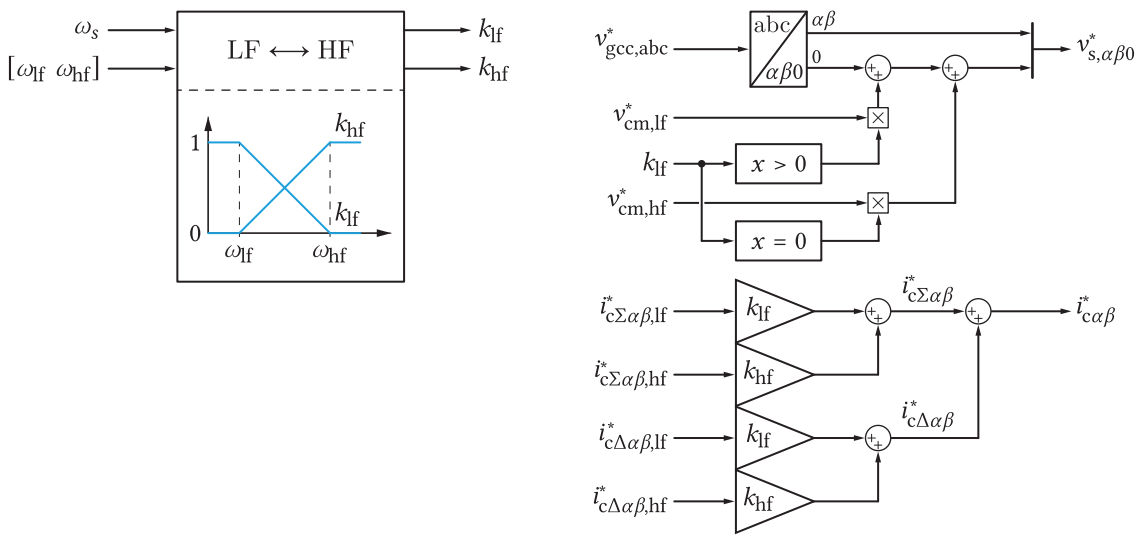


Fig. 3.7 Switch-over between LF and HF operating regions is presented. Current reference scaling coefficients are calculated according to (3.40). CM voltage is supplied without reduction throughout the transition process.

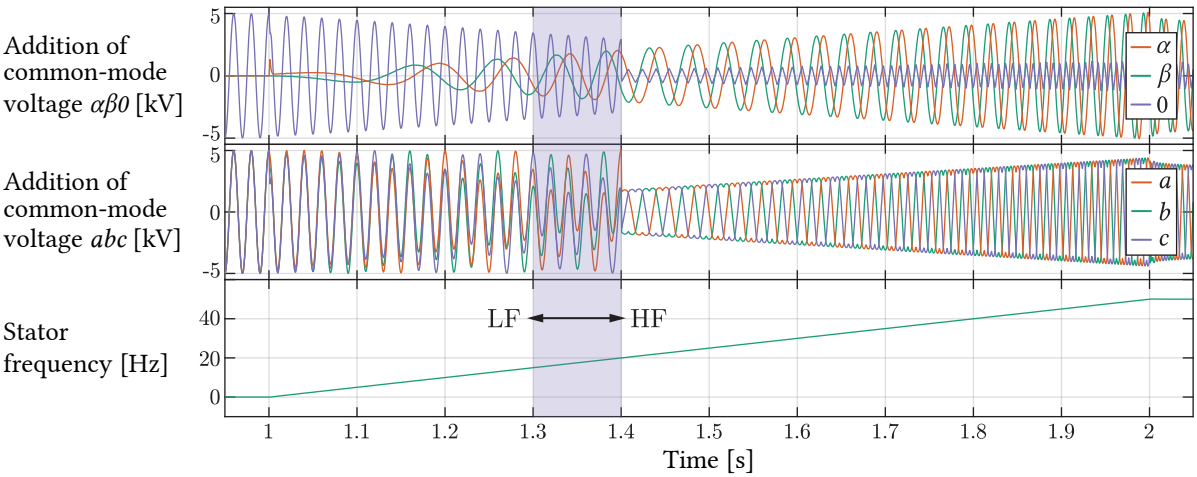


Fig. 3.8 Machine start-up sequence is presented, with two distinct CM voltage injection strategies. In LF and switch-over region, up to (3.38), or 1.4 s, maximum available amplitude of CM voltage is used for LF balancing action (3.23). Once in HF domain, CM voltage is introduced to increase utilization of DC link.

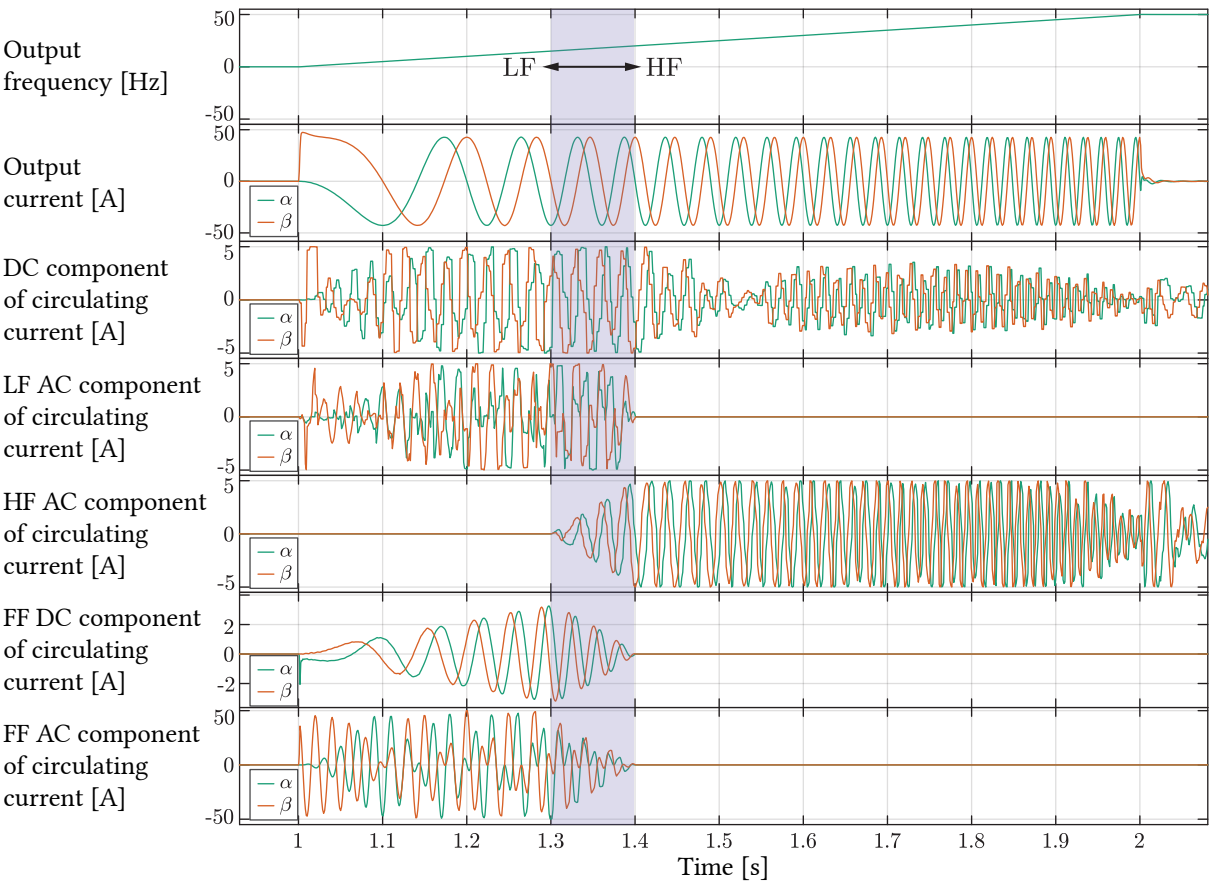


Fig. 3.9 Internal MMC balancing current components for frequency ramp-up from zero to nominal value, at constant output current amplitude, are presented. Switch-over between LF and HF modes of operation is clearly visible at $T \in [1.3\,\text{s} \ldots 1.4\,\text{s})$ interval.

Start-up sequence of machine-side MMC is presented in **Fig. 3.10**. DC link voltage is defined by prototype converter rating to 10.4 kV (**Tab. 2.2**). AC terminals voltage is limited by the machine rated voltage to 6 kV line-to-line. Output AC voltage and current are unaffected by the internal energy balancing action current. Both sum- and differential capacitor voltage ripple is within the ±10 % limits, presented by dashed lines. Observing the LF operating region, a significant reserve within the allowed capacitor voltage range is available. Thus, to reduce additional current stress in LF mode, further limitation can be imposed on circulating current balancing components of **Figs. 3.5** and **3.6**, resulting in higher but below-the-limit sum- and differential voltage fluctuations. Individual SM-level capacitor voltage ripple, for both positive and negative branch of one phase is given in **Fig. 3.11**. SM modeling parameters are given in **Tab. 3.1**. In the model, a ±10 % capacitance tolerance of C_{SM} is taken into account, with the assumption that all SMs are initially charged to the equal voltage level. Rated SM voltage is chosen at $V_{\mathrm{DC,rated}}/N_{\mathrm{SM}}$. The results demonstrate correct voltage balancing between the SMs.

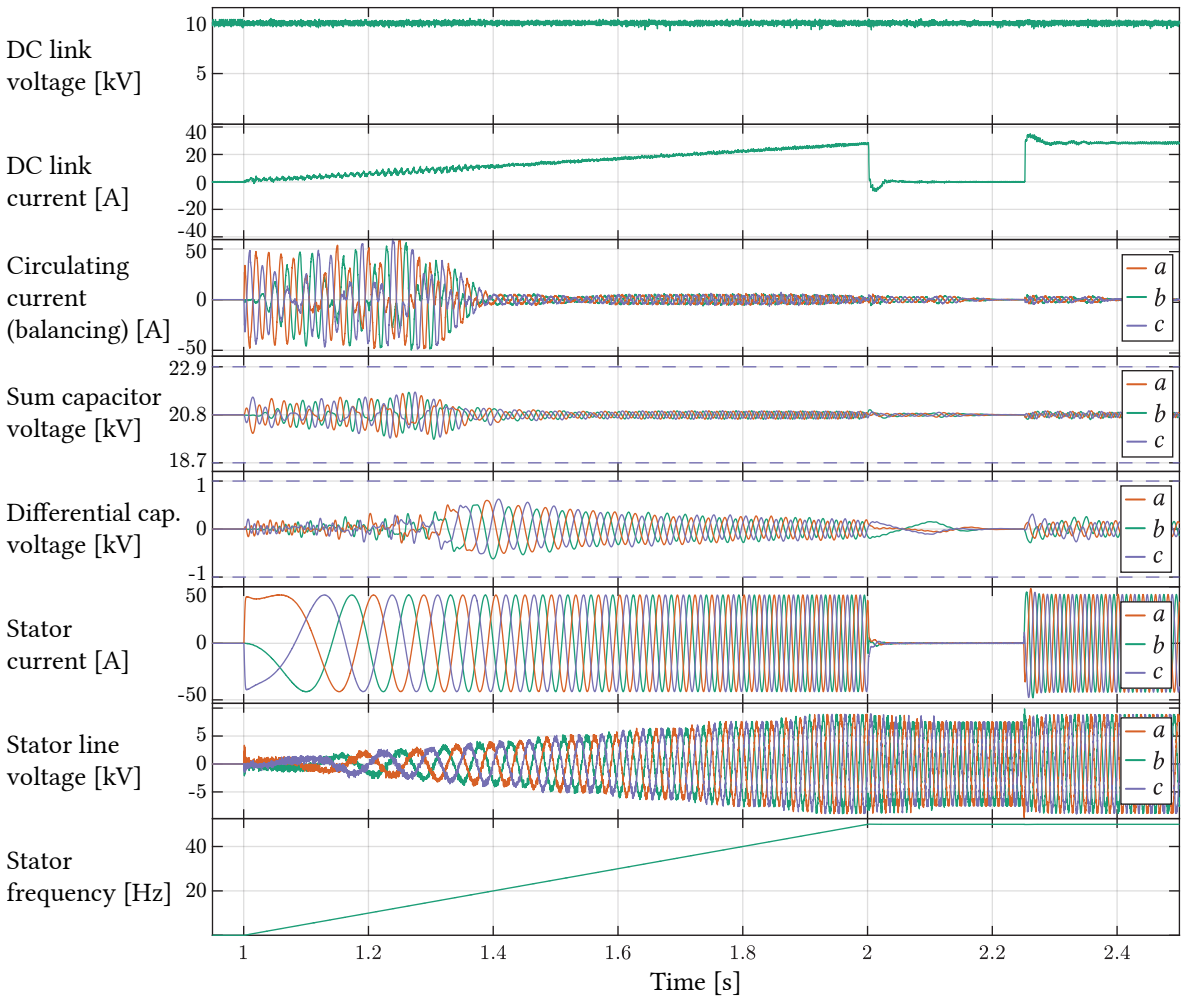


Fig. 3.10 Machine-side MMC terminal voltage and current values during frequency ramp-up. Balancing component of circulating current, as well as sum- and differential capacitor voltage ripple are presented. During frequency ramp-up, and transition from LF to HF, no distortion can be observed on converter terminals. Leg-level sum- and differential SM voltage ripple is within 10 % boundaries.

Tab. 3.1 PEL SM capacitor ratings for the machine-side MMC prototype

Rated voltage	V_{SM} =650 V
Maximum (trip) voltage	V_{SM} =800 V
Capacitance	C_{SM} =2.25 mF±10%

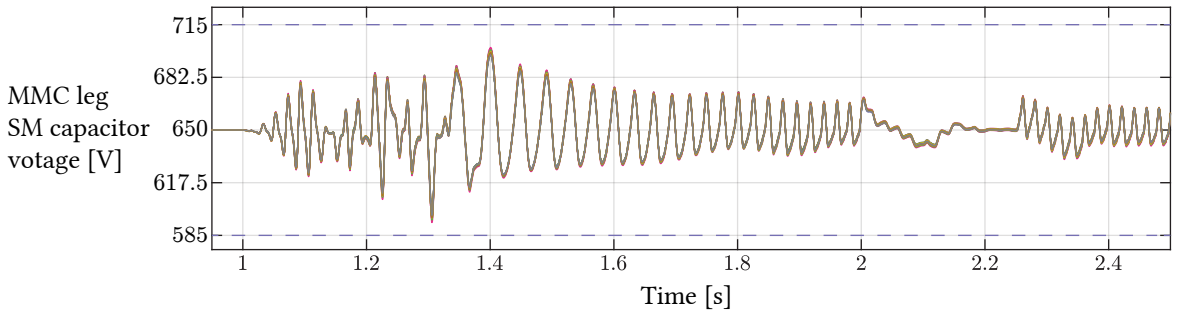


Fig. 3.11 Phase-leg SM-level capacitor voltage ripple during output frequency ramp-up sequence. Dashed lines represent 10 % voltage boundaries around the rated SM voltage of 650 V. Capacitor voltages are kept within the boundaries utilizing presented LF mode control system. LF to HF switch-over is performed within $T \in (1.3\,\text{s} \ldots 1.4\,\text{s}]$ time interval.

Certain reserve exists between maximal instantaneous C_{SM} voltage amplitude and the adopted limit. As discussed, this reserve can be used to partially relax the current stress during LF operation, by decreasing current amplitude limit at the expense of higher voltage ripple.

3.3 Machine-side control

3.3.1 Current control

3.3.1.1 Machine model and stator current control

Within this section, FOC is applied to the model of WRSM, using parameters of the machine available at PEL. The machine is of salient pole type. Main electrical and mechanical parameters are given in **Tab. 3.2**, while equivalent circuit parameters are provided in **Tab. 3.3**.

Tab. 3.2 Medium voltage WRSM rated parameters.

Machine type	SEVER RMSOT 6355 Lk-4
Apparent power	S_n =526 kV A
Active power	P_n =500 kW
Torque	M_n =3044 N m
Stator voltage	$V_{\text{s,n}}$ =6 kV (star)
Stator current	$I_{\text{s,n}}$ =48 A±10%
Speed/frequency	$n_{\text{n}}/f_{\text{n}}$ =1500/min/50 Hz
Excitation current	$I_{\text{f,max}}$ =16 A
Excitation voltage	$V_{\text{f,max}}$ =262 V

Tab. 3.3 Medium voltage WRSM equivalent circuit parameters.

Stator resistance	R_s =1.1 Ω
Stator leakage inductance	L_{ls} =23.16 mH
Unsaturated magnetic inductance	L_{md0} =361.81 mH, L_{mq0} =171.5 mH
Saturated magnetic inductance	L_{mdsat} =320.81 mH
Excitation resistance	R_f^s =0.291 Ω
Excitation leakage inductance	L_{lf}^s =30.5 mH
Damper resistance	R_{kd}^s =6.262 Ω, R_{kq}^s =2.256 Ω
Damper leakage inductance	L_{lkd}^s =67.48 mH, L_{lkq}^s =19.67 mH
Turns ratio	$N_s/N_f = 192/1952 = m_{fs}$
Inertia	J_m =11.2 kg m^2
Inertia time constant	H =1.11 s
Number of pole pairs	$p = 2$

Stator currents are controlled in dq reference frame, d-axis being aligned to the excitation flux. Equivalent circuit for stator current control is presented in **Fig. 3.12**, with all the units scaled to the stator side. The equivalent impedance seen by the current control is the sum of AC-side MMC impedance, stator resistance and leakage inductance.

To determine the dq back Electromotive Force (EMF) amplitudes in **Fig. 3.12**, flux linkages of salient pole machine are required. These are obtained in (3.41) and (3.42).

$$\Psi_d = L_{ls} i_d + L_{md}\left(i_d + i_f^s + i_{kd}^s\right) = L_d i_d + L_{md} i_f^s + \underbrace{L_{md} i_{kd}^s}_{\substack{\text{zero in} \\ \text{steady state}}} \tag{3.41}$$

$$\Psi_q = L_{ls} i_q + L_{mq}\left(i_q + i_{kq}^s\right) = L_q i_q + \underbrace{L_{mq} i_{kq}^s}_{\substack{\text{zero in} \\ \text{steady state}}} \tag{3.42}$$

With the knowledge of back EMF, decoupled stator current control is developed and presented in **Fig. 3.13**, utilizing the appropriate feed forward members for d and q axes. Assuming operation below saturation knee, decoupling gains and controller tuning equivalent inductances are as follows:

$$L_d = L_{ls} + L_{md0} \tag{3.43}$$

$$L_d = L_{ls} + L_{mq0} \tag{3.44}$$

On the other hand, equivalent MMC AC inductance is determined as follows.

$$L_{br,AC} = L_{br}\frac{1 + k_{br}}{2} \tag{3.45}$$

Where k_{br} denotes branch inductor coupling coefficient (**Sec. 2.1**). The positive value is used, i.e. same orientation of "dots", leading to AC flux addition. MMC branch impedance parameters are given in **Tab. 3.4**. Stator current control is tuned according to the equivalent circuit , where:

$$L_{cc} = L_{ls} + L_{br,AC} \tag{3.46}$$

$$R_{cc} = R_s + \frac{R_{br}}{2} \tag{3.47}$$

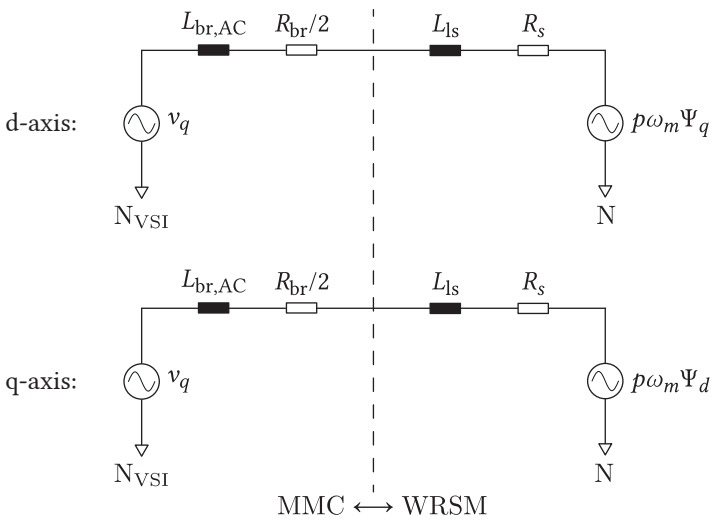


Fig. 3.12 Equivalent circuit for decoupled control of salient pole WRSM stator currents in *dq* reference frame is presented. Stator leakage inductance L_{ls} is an order of magnitude higher than equivalent MMC branch inductance. Both of these are, however, taken into account. Flux linkage expressions are given in (3.41) and (3.42).

Tab. 3.4 MMC branch impedance parameters.

Branch inductance	$L_{br} = 2.5\,\text{mH}$
Branch resistance	$R_{br} = 50\,\text{m}\Omega$
Coupling factor	$k_{br} = 0.3$

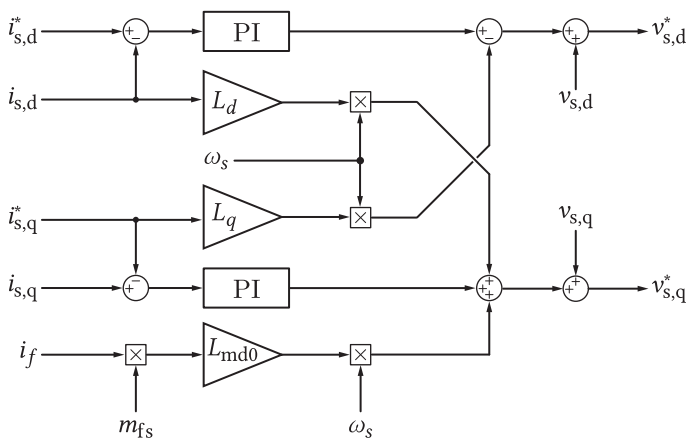


Fig. 3.13 Stator current control implementation in *dq* reference frame.

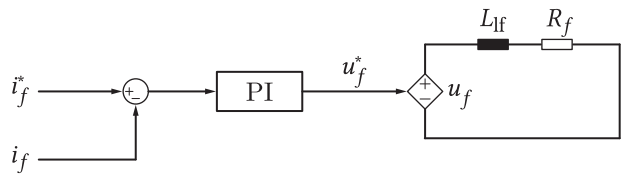


Fig. 3.14 Excitation (field) winding model and current control. Flux in *d*-axis of the machine is kept at constant value, as at this point field-weakening is not observed. Excitation winding supply is modeled by an ideal voltage source. Commercial excitation supply systems are a mature technology, and are not of interest for this research.

3.3.1.2 Excitation circuit model and current control

Synchronous machines in the order of 100 MV A are of WRSM type. Consequently, *d*-axis magnetizing flux is provided through control of excitation winding current. In case speeds above rated are required, the machine can be operated in field-weakening mode, through the reduction of excitation current. Time constant of excitation winding is higher than the one of stator winding, thus lower dynamics is obtained. To increase dynamic response, *d*-axis current injection from the stator side can provide faster magnetizing flux transient, allowing the excitation current to settle to the new value. After the transient, stator *d*-axis current reference can be set back to zero [53].

At this point, field-weakening mode of operation is not implemented, and variable speed operation is observed in the range $\left[-\omega_{\mathrm{m,rated}}, \omega_{\mathrm{m,rated}}\right]$. Additionally, unity power factor is set at the stator terminals, i.e. *d*-axis stator current reference is forced to zero. Excitation current control is implemented as depicted in **Fig. 3.14**. PI controller is tuned according to parameters from **Tab. 3.3**. Voltage actuator is modeled through an ideal controlled voltage source.

3.3.1.3 Current control verification

Verification of current control system, for both stator and excitation current, is presented in **Fig. 3.15**. Excitation current is referenced to a fixed value. The value is selected according to stator voltage in open-circuit test, at rated speed. A time delay of 1 s is introduced for excitation current transient.

Stator *d*-axis current is referenced to zero. *q*-axis stator current is step-changed twice per second, between positive- and negative rated amplitude values. The results demonstrate correct tracking of all three references.

3.3.2 Speed control

WRSM speed control is superimposed to current control. According to the motion equation (3.48), constant speed is achieved when electromagnetic torque produced by the machine equals the opposing load torque in terms of amplitude. Total load torque comprises load imposed on machine shaft externally, as well as torque caused by friction. A machine outputting torque higher or lower than the total load torque will accelerate or decelerate, respectively. The dynamics, i.e. the rate of acceleration, is determined by torque magnitude and machine inertia.

$$M_{\mathrm{em}} = M_{\mathrm{load}} + J_m \frac{2}{p} \frac{d\omega_s}{dt} \tag{3.48}$$

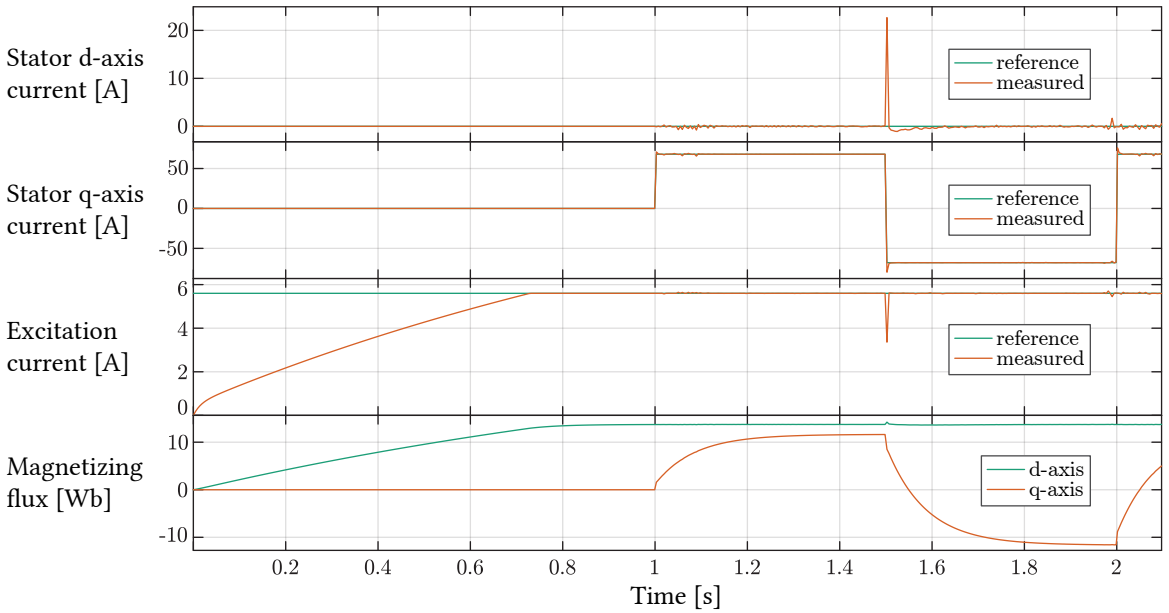


Fig. 3.15 Control system verification for *dq*-frame stator current control and excitation current control. Stator *d*-current reference is referenced to zero, while excitation current is set to constant value. Thus, field-weakening is not implemented at this point, constant *d*-axis flux originates from excitation winding. Stator *q*-axis current is step-changed at 1 Hz frequency. All references are correctly tracked by the control.

Speed control is tuned according to the mechanical inertia of the machine, and limited in reference output amplitude to rated torque increased by an overloading factor.

$$M_{\mathrm{em,max}} = k_{\mathrm{OL}} M_{\mathrm{em}} \tag{3.49}$$

Relationship between electromagnetic torque and machine current components, for salient-pole machine, is given in (3.50).

$$M_{\mathrm{em}} = \frac{3p}{2}\left(i_q \Psi_d - i_d \Psi_q\right) \tag{3.50}$$

Setting and controlling *d*-axis stator current component to zero (unity power factor), only one member of the equation (3.50) contributes to torque development. Combining (3.41) and (3.50), stator *q*-axis current reference is obtained. Obtained reference is scaled by a factor of K_{dq}, which is dependent on Clarke transformation coefficient, and in this case equals $K_{\mathrm{dq}} = 3/2$.

$$i_q^* = \frac{2}{3p} \cdot \frac{M_{\mathrm{em}}}{L_{\mathrm{md}} i_f m_{\mathrm{fa}}} K_{\mathrm{dq}} \tag{3.51}$$

Speed controller structure is presented in **Fig. 3.16**. Control verification is performed utilizing speed and load torque test profiles presented in the two topmost graphs of **Fig. 3.17**. Non-zero load torque is applied in steady state. Output torque and speed correctly track the references. Excitation current in constant in amplitude. Magnetizing flux of *d*-axis is kept constant.

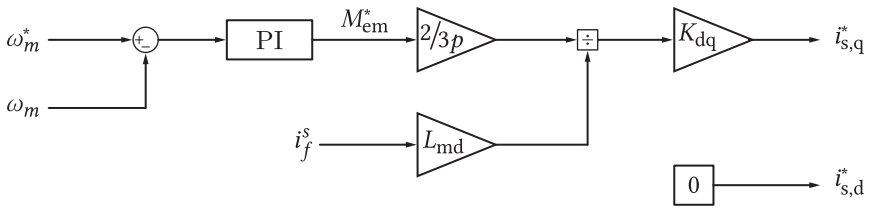


Fig. 3.16 WRSM speed control, assuming unity power factor, i.e. zero reference of *d*-axis current. Field current is used to control flux in steady-state. During transients, *d*-component of stator current can be used to alter the flux for faster dynamic response, while slower field winding current reaches new steady state. Coefficient K_{dq} is dependent on Clarke transformation coefficient. Invariant impedance approach was used, i.e. $K_{dq} = 3/2$.

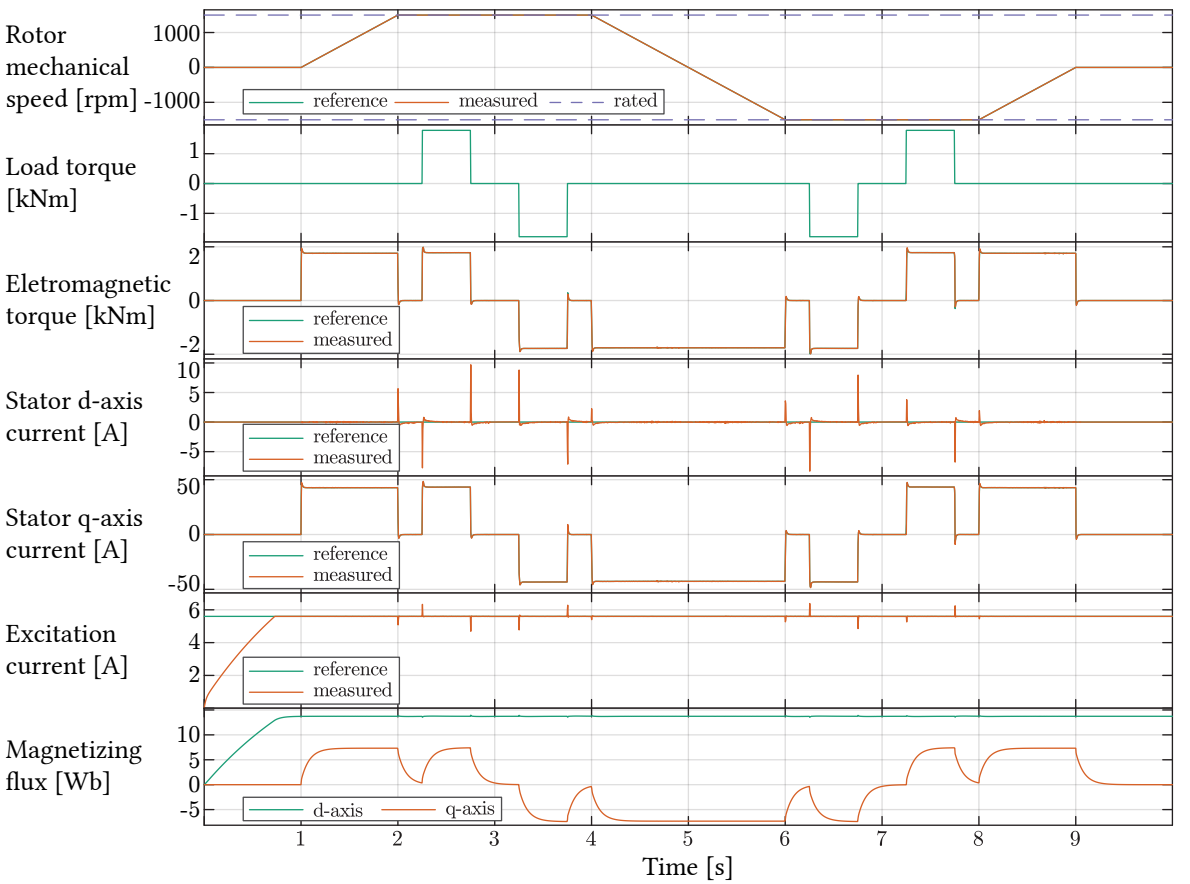


Fig. 3.17 WRSM speed control verification. Machine is started after excitation current build-up time delay. Speed and load torque references are given independently. Speed controller generates electromagnetic torque reference for speed reference maintenance, for arbitrary load torque. Stator current references in *dq*-system are generated and tracked. Excitation current is kept constant (constant flux). Cascaded control of WRSM correctly tracks the reference.

3.3.3 Test scenario model output

For the test profile of speed and rated torque, full operating sequence of machine-side MMC is presented in **Fig. 3.18**. For the full test operating sequence, internal MMC balancing currents are presented in **Fig. 3.19**. One cycle output line-to-line voltage waveform is presented in **Fig. 3.20**. Considering the applied PSC-PWM, the apparent switching frequency of $N_{SM} \cdot f_{sw} = 16\,\text{kHz}$ and voltage level count of $N_{SM} + 1 = 17$ produce high-quality multilevel waveform and low current ripple. It should be noted, however, that output power ratings in the range of 100 MV A at MV level are more likely to use lower SM count of higher individual voltage, based on currently available high-power PEBBs [35]. Switching frequency of 1 kHz may also be high in such a scenario.

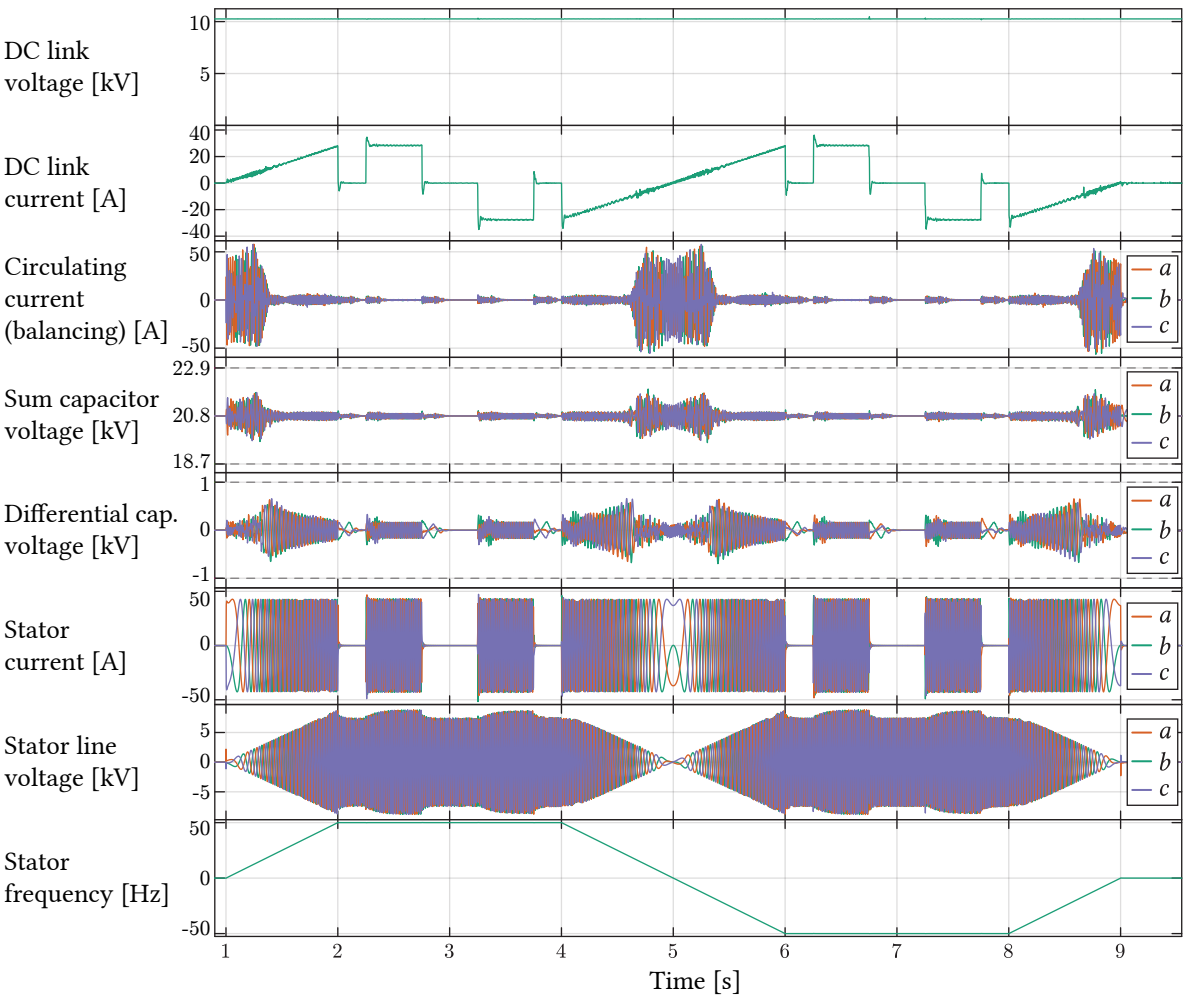


Fig. 3.18 Machine-side MMC terminal voltage and current waveforms are presented over the entire 10 s test pattern. Performance-wise, terminal values are unaffected by internal balancing circulating current component.

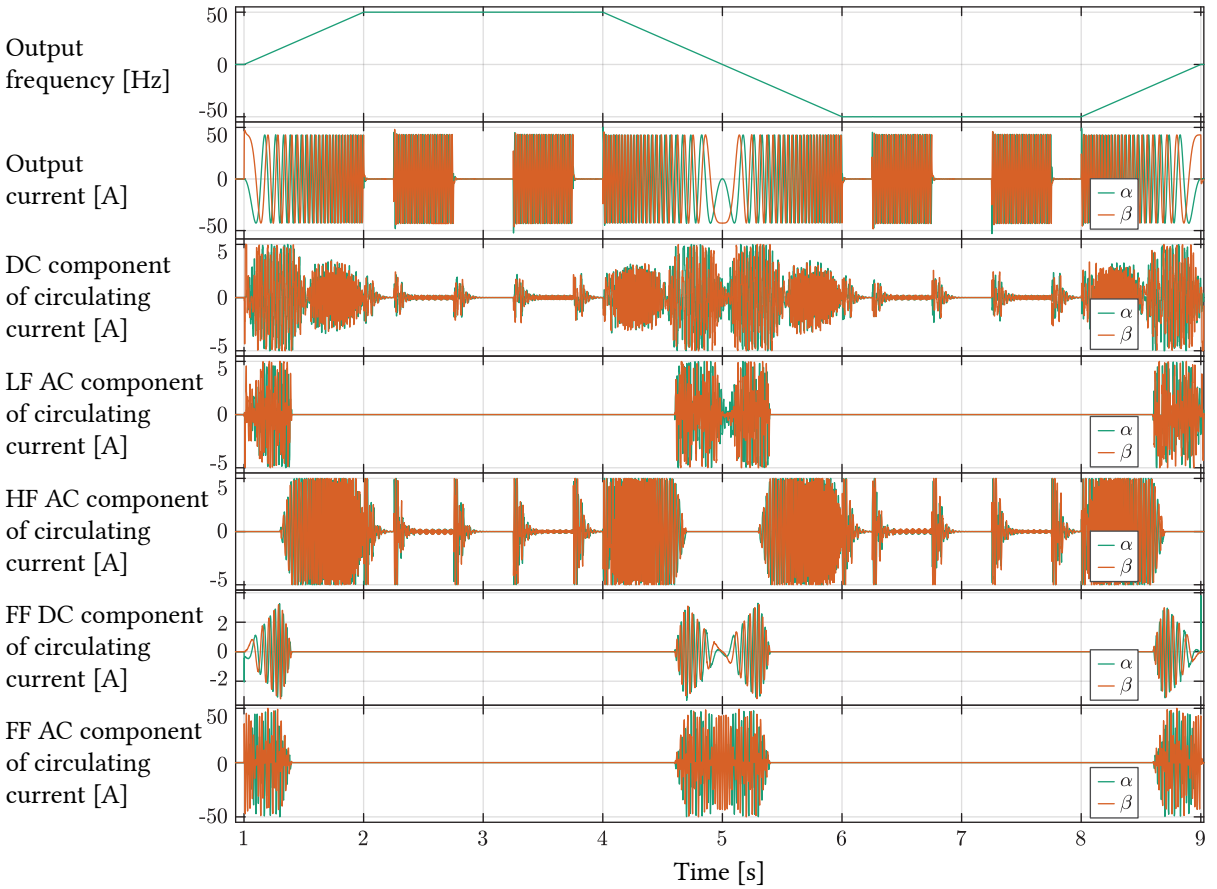


Fig. 3.19 Internal MMC balancing current components for full test-sequence, comprising ramp-up to rated frequency, direction of rotation changeover, and load torque variation response (visible indirectly through output current values).

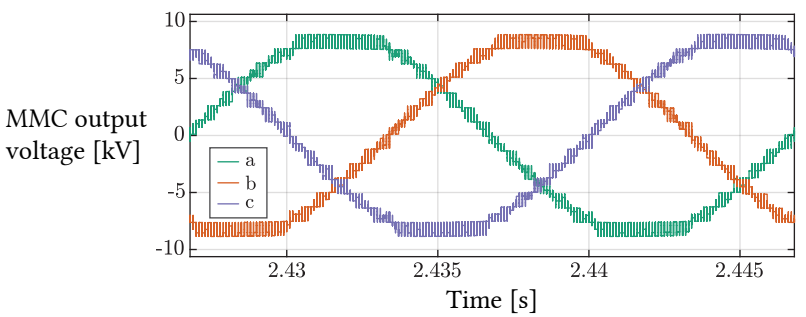


Fig. 3.20 Line-to-line output voltage of machine-side MMC, at rated frequency. With PEL prototype MMC parameters – $N = 16$ SMs per branch and SM switching frequency of 1 kHz, voltage waveform is of very high quality. Apparent switching frequency equals 16 kHz, with 16 + 1 voltage levels. In high-power MV applications, however, lower SM count, as well as lower switching frequency can be expected.

3.4 Grid-side control

3.4.1 Grid code requirements

A set of minimal technical requirements for grid connection of generating units, *grid code*, is provided by the TSO responsible for the observed power system. These requirements are defined for operation within allowed voltage and frequency deviations, as well as for operation under various grid disturbances, e.g. short circuit conditions. Within this section, requirements from German VDE transmission code are adopted [54]. Requirements comprise the following:

- Active power output and frequency control
- Reactive power supply
- Behavior in the event of grid disturbances

3.4.1.1 Active power output

Active power delivery to the grid, as a function of instantaneous frequency, is illustrated in **Fig. 3.21**. Four operating regions can be identified in the figure, corresponding to active power reference scaling as presented in (3.52).

$$P^*_{\mathrm{GC}} = \begin{cases} 0 & f_g \in [0 \ldots 47.5\,\mathrm{Hz}) \\ P^*_{\mathrm{TSO}} & f_g \in [47.5\,\mathrm{Hz} \ldots 50.2\,\mathrm{Hz}) \\ P^*_{\mathrm{TSO}} - 0.4 \cdot \left(f_g - 50.2\,\mathrm{Hz}\right) & f_g \in [50.2\,\mathrm{Hz} \ldots 51.5\,\mathrm{Hz}) \\ 0 & f_g \in [51.5\,\mathrm{Hz} \cdots + \infty) \end{cases} \tag{3.52}$$

As a PHSP is a renewable energy source, the grid code refers to *available power*, rather than rated power, as the actual output capability may depend on momentary conditions of plant's water reservoirs. In principle, however, PHSP is a dispatchable source. Assuming operation at active power output level P^*_{TSO}, agreed with the corresponding TSO, any deviation in frequency within the band of 47.5 Hz to 50.2 Hz foresees no change in reference amplitude. If a PHSP participates in primary control, the active power setpoint in adjusted in case of frequency deviation.

Above 50.2 Hz, a 40 % down-slope is used to de-rate the reference. With the frequency exceeding 51.5 Hz, active power reference is driven to zero, and the plant is allowed to disconnect from the grid [54]. In the test scenario, however, PHSP will be always connected to the grid, which enables the supply of reactive power support, if needed, even in the case of simultaneous frequency deviation.

3.4.1.2 Reactive power supply

Since PHSPs of considered power rating in 100 MV A range are connected to 110 kV or higher grid voltages, continuous reactive power support may be required, i.e. dead band $0.9U_n \ldots 1.1U_n$ may not be considered. At this point, continuous reactive power support of 2 % per 1 % of voltage deviation from the rated is realized outside of the dead band, while original reactive power reference is used within the dead band (**Fig. 3.22**).

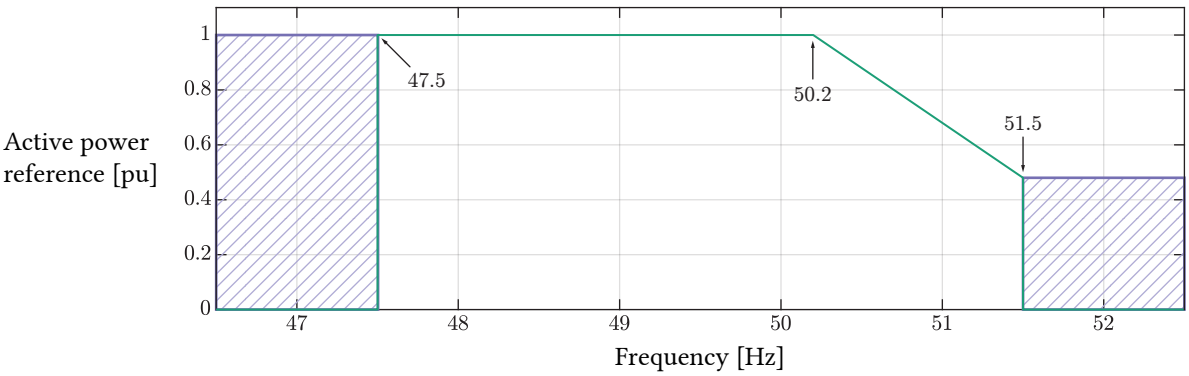


Fig. 3.21 Active power output scaling as a function of grid frequency, according to the grid code. Below 47.5 Hz and above 51.5 Hz it is permitted to disconnect from the grid. Within the operating region of 47.5 Hz to 50.2 Hz, rated active power can be delivered. In the following region of 50.2 Hz to 51.5 Hz, active power amplitude must be lowered at the slope of $k_P = -0.4/\text{Hz}$.

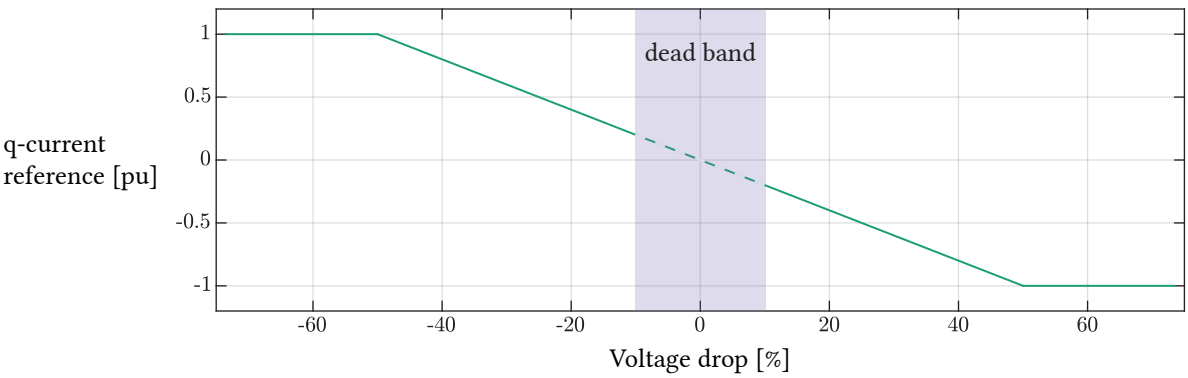


Fig. 3.22 Reactive power supply requirements are presented for under- and over-voltage grid conditions, with the aim of providing voltage support. In the normal operating voltage range of $\pm 10\,\% \hat{v}_{\text{g,n}}$ the values are not specified. Once outside of these limits, reactive current component must be injected, with $k_Q = -2$ slope.

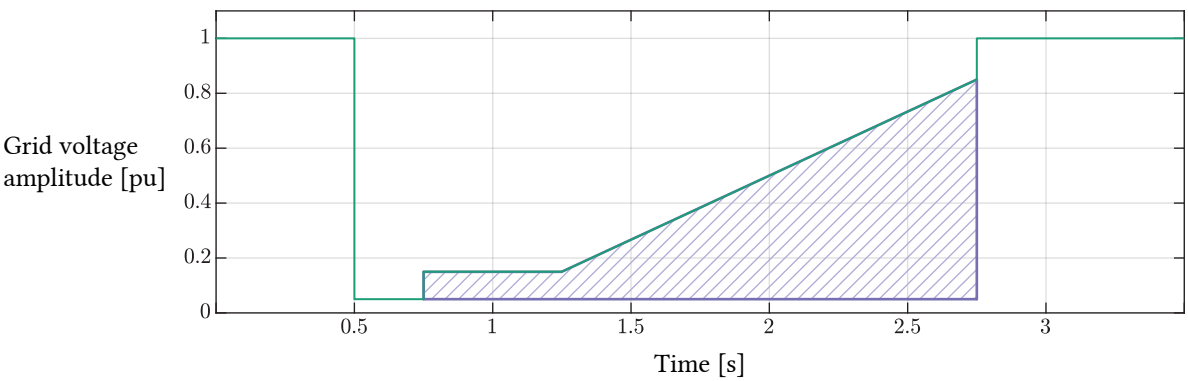


Fig. 3.23 Grid-code-defined limiting curves for a generating facility of Type 2, adapted from [55]. Largest value of the three line voltages is considered. Generating units must ride through the fault without disconnection for all the cases above the solid line. In the shaded area, short-time disconnection of generating units is permitted.

3.4.1.3 Behavior under grid disturbances

Every power system is prone to periodic abnormal conditions, such as unbalances and short circuits. In case these occur in one of the generating facilities, protection can be triggered and the unit shut down. For disturbances in the proximity of the plant, but outside of its control reach, i.e. in the power transmission, distribution and consumption system, the generating units must support the clearance of the disturbance by acting in compliance with the grid requirements, dependent on the unit type. Generating units are diversified in two types [54].

- **Type 1** – synchronous generators connected directly to the grid. Fixed-speed PHSPs belong to this group.
- **Type 2** – all the generating units not fulfilling the condition of Type 1. This group is referred to as *power parks* in the European Union legislative [55]. The CFSM-based PHSPs fall within this category.

Symmetrical grid disturbance behavior comprises LVRT in three-phase short circuit events, as well as symmetrical voltage dips. These two types of events can be mutually represented by the depth of voltage dip and the corresponding duration. A profile representing an extreme case scenario in terms of depth of voltage dip and duration is defined for both Type 1 and Type 2 categories in [55]. Limiting curves for both Type 1 and Type 2 facilities, provided in [55], are adapted and presented in **Fig. 3.23**. As more severe conditions are envisioned for Type 2 units, these values are adopted as a test scenario for the I-MMC-based PHSP drive model. The range of per-unit voltage dip amplitudes and duration is given in **Tab. 3.5**, highest being chosen for the test scenario.

Tab. 3.5 Fault-ride-through capability voltage and time parameters for Type 1 and Type 2 generating units.

Voltage parameters [pu]			Time parameters [s]		
	Type 1	**Type 2**		**Type 1**	**Type 2**
U_{ret}	0.05 pu to 0.3 pu	0.05 pu to 0.15 pu	t_{clear}	0.14 s to 0.25 s	0.14 s to 0.25 s
U_{clear}	0.7 pu to 0.9 pu	$U_{\text{ret}} - 0.15$ pu	t_{rec1}	t_{clear}	t_{clear}
U_{rec1}	U_{clear}	U_{clear}	t_{rec2}	$t_{\text{rec1}} - 0.7$ s	t_{rec1}
U_{rec2}	0.85 pu to 0.9 pu and $\geq U_{\text{clear}}$	0.85 pu	t_{rec3}	$t_{\text{rec2}} - 1.5$ s	1.5 s to 3 s

Tab. 3.6 Per-phase voltage values during disturbances presented in **Fig. 3.24**, adapted from [56]. Coefficient k represents depth of voltage dip, having values in the range $[0 \dots 1]$ for none to maximum voltage dip, respectively. Type A represents symmetrical fault and can be used to describe LVRT. The remaining cases are various scenarios of unsymmetrical grid conditions.

Disturbance type	$v_{\text{a,dist}}$	$v_{\text{b,dist}}$	$v_{\text{c,dist}}$
A	$(1-k)v_a$	$(1-k)v_b$	$(1-k)v_c$
B	$(1-k)v_a$	v_b	v_c
C	v_a	$v_b - (k/2)(v_b - v_c)$	$v_c + (k/2)(v_b - v_c)$
D	$(1-k)v_a$	$v_b + (k/2)v_a$	$v_c + (k/2)v_a$
E	v_a	$(1-k)v_b$	$(1-k)v_c$
F	$(1-k)v_a$	$v_b + (k/3)(v_a - v_b)$	$v_c + (k/3)(v_a - v_c)$
G	$(1-k/3)v_a$	$(1-k)v_b - (k/3)v_a$	$(1-k)v_c - (k/3)v_a$

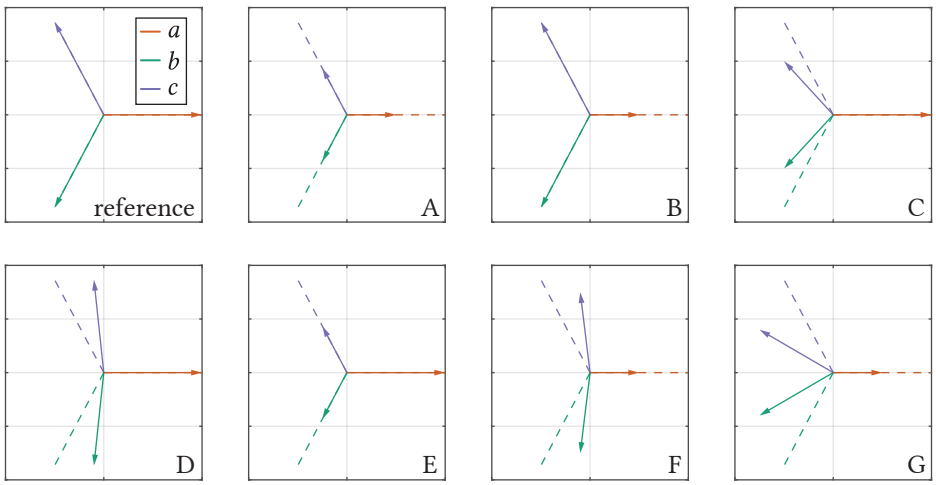


Fig. 3.24 Graphical representation of observed grid disturbances, adapted from [57]. The first graph depicts nominal grid voltages. *Type A* disturbance is of symmetrical nature. It can be used to represent either 3PH LVRT profile, or a less severe voltage dip. Scenarios *B* to *G* represent various unsymmetrical grid voltage disturbances, where both positive and negative voltage sequence exist. Critical cases for converter control verification can be taken as *Type A* with highest foreseen voltage dip, and one of the unsymmetrical cases that can verify grid synchronization and current control under the presence of positive and negative voltage sequence. *Type B* has been considered in this work.

Unsymmetrical grid disturbance behavior comprises single phase or two-phase short circuits and voltage dips. Again, these two can be represented mutually through depth of voltage dip in the affected phase(s) and duration of the dip. Looking back at **Fig. 3.23**, grid code does not necessarily assume symmetrical fault [55]. The depth of voltage dip refers to the phase of the highest voltage amplitude, so the possibility of unsymmetrical fault is covered. As no specific information is given on these cases, a multitude of unsymmetrical scenarios can be observed [58], as presented analytically in **Tab. 3.6** and graphically in **Fig. 3.24**. These types of faults are significant to be covered, as they result in appearance of negative voltage sequence, which requires modification in PLL realization, to be able to extract the two sequences and correctly reconstruct the information on grid voltage conditions. Additionally, a degree of freedom in current control approach arises, as both positive and negative sequence can be used.

3.4.2 Grid synchronization for unbalanced conditions

In a power system, grid-connected converter is exposed to both symmetrical and unsymmetrical voltage deviations, originating from different types of faults. Statistics has shown that symmetrical faults, i.e. three-phase short circuits and symmetrical voltage dips, are the most rare in a power system [59]. In the event of an unsymmetrical grid disturbance form, illustrated in **Fig. 3.24**, both positive and negative sequence voltage amplitudes exist. As GCC used in this study is realized in *dq* frame, aligned to positive-sequence voltage vector, proper extraction of positive-sequence angle and voltage amplitude is necessary.

Synchronous reference frame PLL is not sufficient for proper grid angle and voltage amplitude tracking, in the event of both positive- and negative-sequence voltage existence. Thus, an advanced PLL structure, named Double Decoupled Synchronous Reference Frame (DDSRF) PLL is implemented

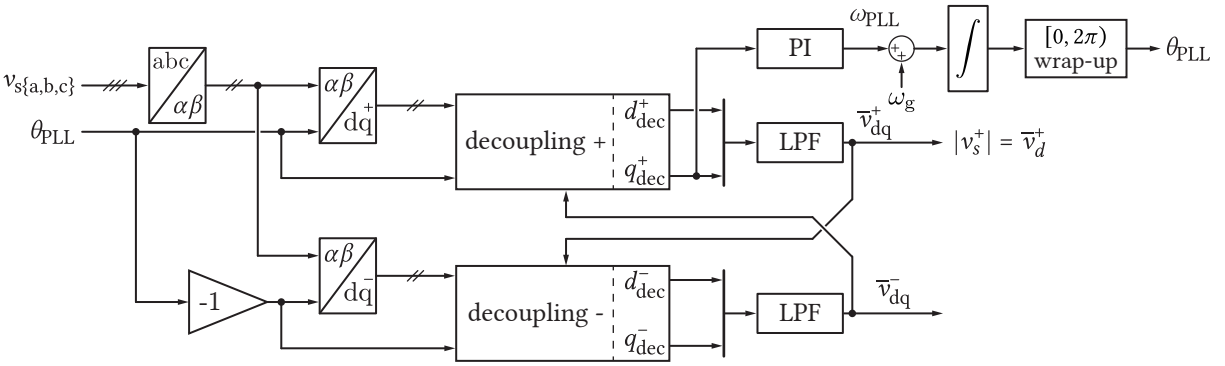


Fig. 3.25 The implementation of DDSRF PLL is presented. To perform correct reconstruction of positive-sequence voltage component in an event of unsymmetrical voltage deviation in the grid, both positive and negative voltage sequence are obtained. Decoupling between *d* and *q* axes is performed, followed by voltage angle tracking in *q* axis, and positive-sequence grid voltage extraction from the *d*-axis of the positive sequence DDSRF output.

for grid synchronization. Introduced in [60], and implemented as depicted in **Fig. 3.25**, DDSRF tracks both positive- and negative-sequence voltage in *dq* reference frame. Extracted *d*- and *q*-axis amplitudes of positive frame are fed back to decoupling block of negative frame, and vice-versa, to mitigate the cross-influence of the two sequences. Further, as in the case of elementary Synchronous Reference Frame (SRF) PLL, positive-sequence *q*-axis voltage is tracked to zero, and positive-sequence voltage angle is obtained. Corresponding voltage amplitude is thus equal to *d*-axis voltage amplitude. DDSRF PLL finally provides grid voltage angle, positive- and negative-sequence voltage amplitudes.

3.4.3 Power reference scaling for grid-code compliance

As a grid-connected generating and storage facility, a PHSP participates in the electrical energy markets. For the power levels considered within this work, i.e. in the order of 100 MV A, power plants are connected to High Voltage (HV) transmission network. All the transactions in terms of energy delivery and energy consumption (storage), are communicated in advanced to the corresponding TSO, which then issues dispatching plan, followed by the PHSP. During normal operation, under rated electrical parameters of the network, active and reactive power of exchange are within the limits of the production capacity of the plant.

In case of deviations in either grid frequency or grid voltage, the generating facility is obliged to at least follow grid-code requirements. Active power at which the energy is delivered to the grid must be reduced at the sign of increasing grid frequency, and maintained at the constant value for decreasing grid frequency, as shown in **Fig. 3.21**. At the same time, however, in case of a voltage deviation event, the reactive power reference of the PHSP must be linearly increased for the decreased voltage level, or decreased for increased voltage level, to support the grid, as described in **Fig. 3.22**.

The two events, i.e. frequency and voltage deviation, can occur simultaneously in the network. As the grid code refers to the rated active power for frequency control, and to the rated generating unit current for voltage support, operating limit of the converter would hit the current limit, resulting in scaled-down actual power levels, violating both of the grid-code requirements. A proper power references scaling is thus introduced. Either active or reactive power can be given a priority. In this work, reactive power, i.e. voltage support, is given priority over the frequency support. The

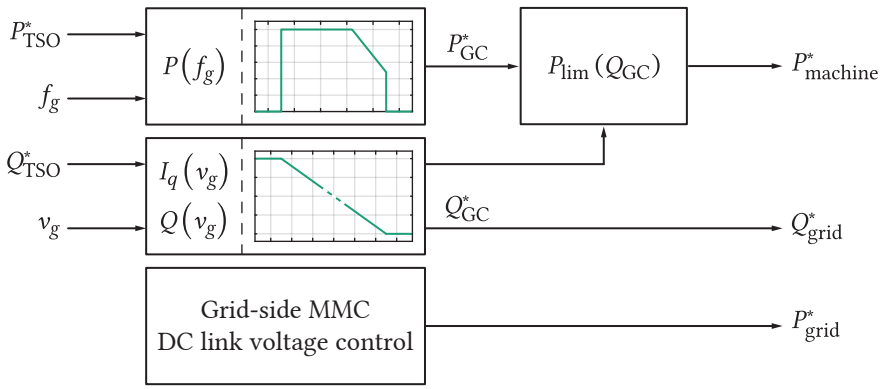


Fig. 3.26 PQ references scaling for grid-code compliance is presented. Active and reactive power references, P^*_{TSO} and Q^*_{TSO}, are obtained from the corresponding TSO, as the production schedule assuming normal network conditions. In case of frequency- or voltage deviation, appropriate scaling is performed to comply with the grid code. Since both frequency and voltage disturbance can exist simultaneously, priority must be given to one of the requirements. In this work, priority is given to the reactive power support, thus the active power reference passed to the electrical machine control is de-rated in case of reactive power augmentation need. Grid-side active power reference is obtained from total energy control stage, which is equal in amplitude to $P^*_{machine}$, augmented by the losses of the converter.

realization of power reference scaling is presented in **Fig. 3.26**. Starting from active and reactive power references dispatched by the corresponding TSO, both references are independently scaled up or down. In case both frequency and voltage deviations occur simultaneously, grid voltage support is prioritized and, if necessary, active power reference is scaled down to fit within the operating range of the converter. The limited power reference is then supplied to the machine-side converter. Active power reference for the grid-side stage is generated independently within the total energy (DC-link voltage) control loop.

$$P^*_{grid} = P^*_{machine} + P_{loss} \tag{3.53}$$

Neglecting converter losses, grid-side stage total energy control power reference is equal in amplitude and opposite in sign to the machine power reference. Taking into account the I-MMC losses that must be provided by this stage, there is a slight deviation between $P^*_{machine}$ and P^*_{grid} presented in **Fig. 3.26**. Losses are, however, typically in the order of one percent of the rated power and are neglected in this study, as they do not affect the analysis of the system dynamics and performance.

3.4.4 GCC reference saturation

Adaptation of power references to deviated grid conditions is ensured by proper scaling technique, as presented in **Sec. 3.4.3**. However, for the active and reactive power references existing just before the fault, grid current reference generator will recalculate current references taking into account now lower available voltage amplitudes. Thus, in transient conditions, right after the voltage dip, current reference in either d or q axis of GCC will immediately increase in proportion to the depth of voltage dip, almost certainly violating the current limit of the converter ratings. This scenario leads to deviation of the ratio between active and reactive power references, and the distortion of output current waveform.

The need for reference saturation calculation within the GCC can be met in numerous ways. The authors of [61] propose either the Proportional Saturator (PS) method, implying equalized scale-down

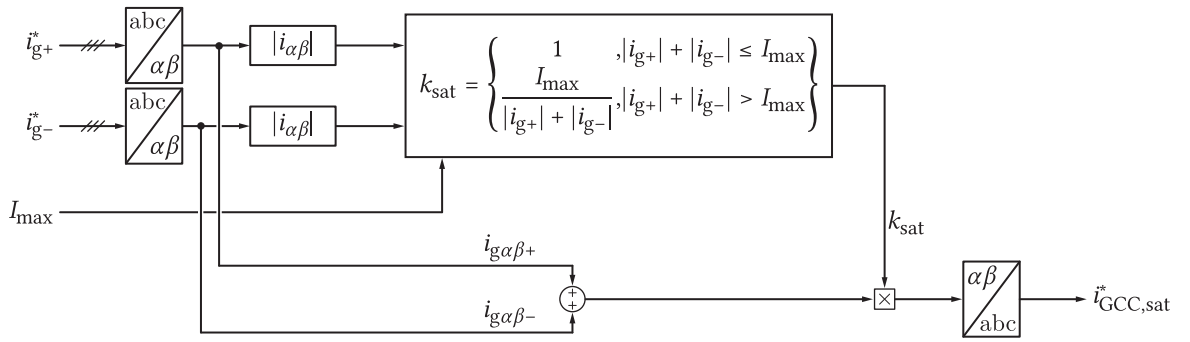


Fig. 3.27 Grid current reference saturation block, comprising both positive- and negative sequence monitoring, is presented. Amplitudes of positive- and negative sequence current references are summed up and compared to current limit of the converter. In case of current limit violation, saturation coefficient becomes $k_{sat} < 1$, limiting the total output current reference.

of both *d* and *q*-axis current references, or the Maximum Area Saturator (MAS), a technique that applies non-equal scaling coefficients to the two SRF axes, to maximize converter utilization. Even though the latter technique utilizes the full current carrying capacity of the converter, the straightforward PS has been chosen for implementation. As in reality these saturators are only active from the occurrence of the grid fault to the proper reaction of the scaling control from **Fig. 3.26**, it is satisfactory for this study to simply not violate converter current limit, at the expense of sub-optimal usage of converter capacity within the short transient period.

The implemented saturation block measures the positive- and negative-sequence of grid current references, and calculates the mutual scaling coefficient k_{sat}, taking into account the maximum allowed current of the converter, I_{max}. In case of the implemented grid current reference calculation, only the positive sequence of current is present. Saturation scaling coefficient takes the values as in (3.54), in function of current reference amplitudes and converter current limit. Index terms + and - represent positive and negative sequence, respectively.

$$k_{sat} = \left\{ \begin{matrix} 1 & |i_{g+}| + |i_{g-}| \le I_{max} \\ \frac{I_{max}}{|i_{g+}|+|i_{g-}|} & |i_{g+}| + |i_{g-}| > I_{max} \end{matrix} \right\} \tag{3.54}$$

3.4.5 Test scenarios

Three test scenarios are performed, covering the most representative cases of control system response:

- **Frequency deviation**, as presented in **Fig. 3.22**, as a frequency support requirement
- **Type A** voltage disturbance from **Fig. 3.24**, as a symmetrical fault challenging LVRT capability of the converter
- **Type B** voltage disturbance from **Fig. 3.24**, as an exemplary unsymmetrical fault, examining control system response to the presence of both positive- and negative-sequence voltage

For all the three scenarios, the machine is accelerated to rated speed within the period $T_{accel} \in [1\,s, 2\,s]$. In the steady state, active power reference to the machine and reactive power reference to the grid, are set according to **Fig. 3.28**

Tab. 3.7 Active and reactive power references used for grid-disturbance-response verification of PHSP.

Generating active power reference	$P_{\text{TSO}} = 430\,\text{kW}$
Grid-side reactive power reference	$Q_{\text{TSO}} = 100\,\text{kvar}$

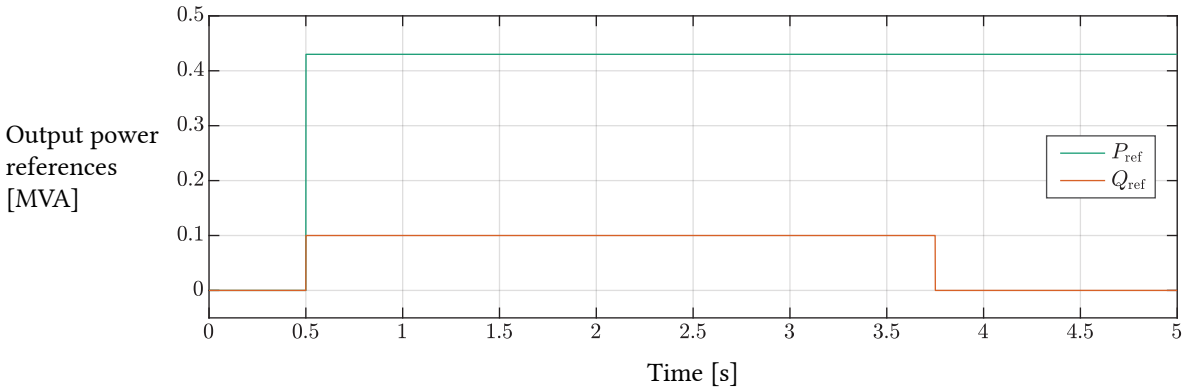


Fig. 3.28 Active and reactive power reference values prior to and during the observed grid disturbance events, used for verification of PHSP response.

3.4.5.1 Frequency deviation

The first test scenario comprises grid frequency variation, following the pattern depicted in **Fig. 3.29**. Starting from the rated frequency of 50 Hz, a step transition to 51 Hz occurs at $t = 2.2$ s. In accordance with the grid-code requirements, active power reference is de-rated linearly with the frequency deviation up to 51.5 Hz and $t = 2.525$ s. At this point, it is allowed to disconnect generating facility from the grid. In the test scenario, however, only the active power reference is forced to zero, keeping the plant online, able to deliver reactive power.

Fig. 3.30 presents higher-level control I-MMC response to grid frequency variations. The topmost graph presents PLL-obtained frequency, as well as upper and lower operation limits, according to **Fig. 3.21**. The next graph presents grid disconnection allowance signal, which is active in the period $t \in [2.565\,\text{s}, 2.7\,\text{s})$. Even though frequency deviation above the permitted range is already detected at $t = 2.525$ s, an anti-disturbance time delay of 40 ms is introduced to allow for PLL transient settling. The third graph presents the following:

- Active power reference obtained from the TSO, which is constant and set according to **Tab. 3.7**.
- Scaled active power reference, according to **Fig. 3.21**, which starts being de-rated at $t = 2.21$ s, with the rise of grid frequency above 50.2 Hz detected.
- Active power limit calculated based on converter current carrying capacity and instantaneous reactive power demand, which is given priority, as presented in **Sec. 3.4.3**.
- Active power reference communicated to the machine-side converter, P^*_{machine}. In this case, as there is no grid voltage deviation and the associated increase in reactive power demand, active power reference is not additionally de-rated by the second scaling block presented in **Fig. 3.26**.

The lowermost graph presents reactive power reference and obtained value, equal to the reference set in **Tab. 3.7**.

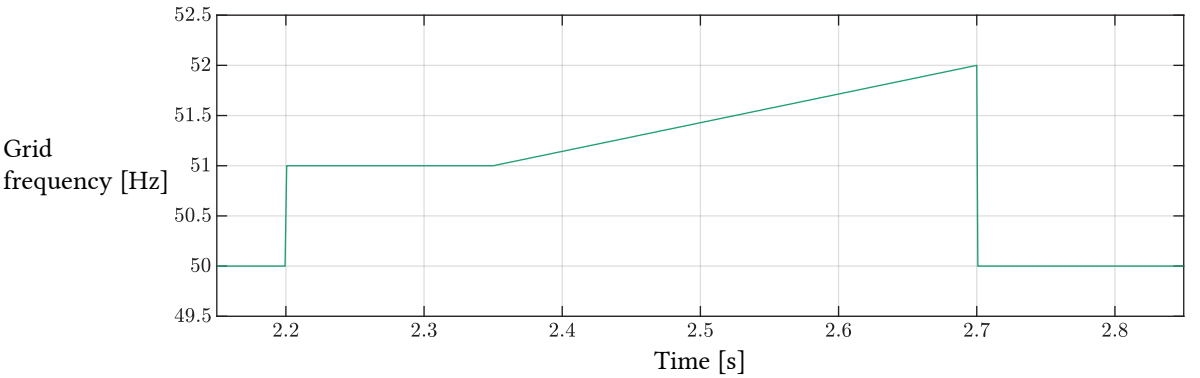


Fig. 3.29 Grid frequency variation test profile is presented. According to grid-code requirements from **Fig. 3.21**, a reduction of output frequency should occur linearly starting from $t = 2.2$ s, up to $t = 2.525$ s. Once the frequency exceeds 51.5 Hz, converter output is referenced to zero. Converter is not disconnected from the grid, but exchanges no active power.

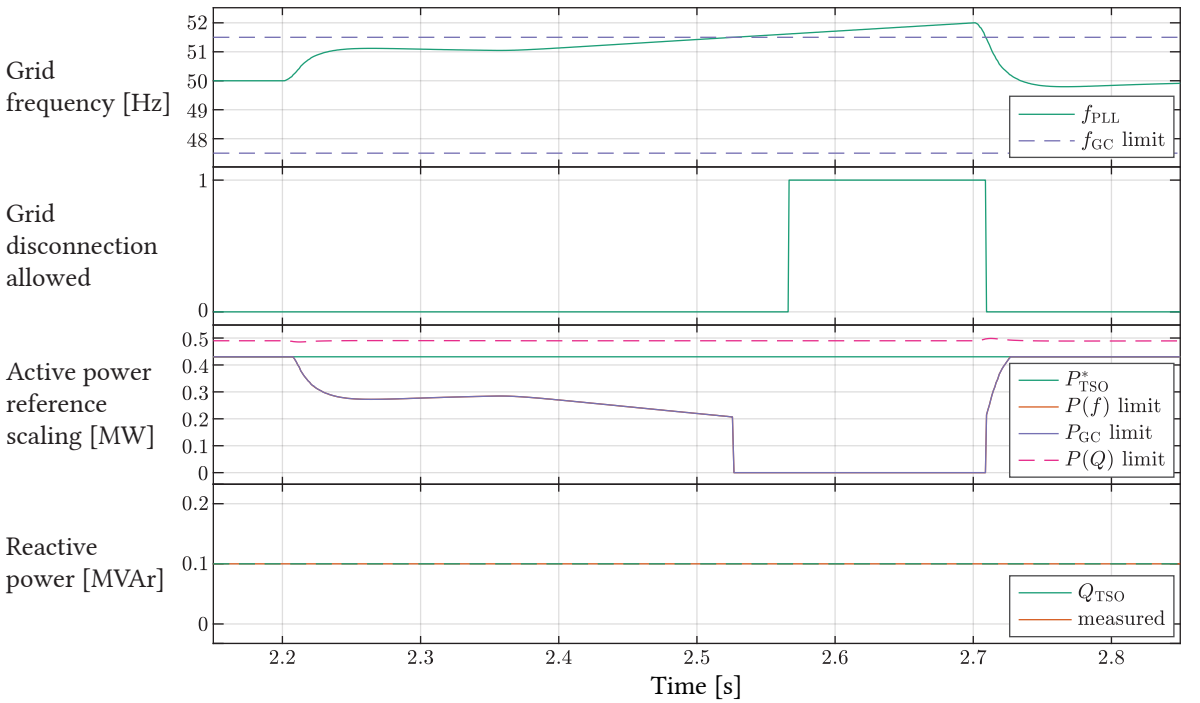


Fig. 3.30 Grid frequency variation test profile is presented. According to grid-code requirements from **Fig. 3.21**, a reduction of output frequency should occur linearly starting from $t = 2.2$ s, up to $t = 2.525$ s. Once the frequency exceeds 51.5 Hz, converter output is referenced to zero. Converter is not disconnected from the grid, but exchanges no active power.

Grid-side MMC operation sequence corresponding to **Fig. 3.30** test scenario is presented in **Fig. 3.31**. DC-link voltage is controlled correctly throughout the transient. Sum- and differential capacitor voltage ripple are within ±10 % limits (dashed lines). Grid-side output voltage is symmetrical and of constant amplitude, according to the test scenario. Grid current is sinusoidal, correctly tracking the reference.

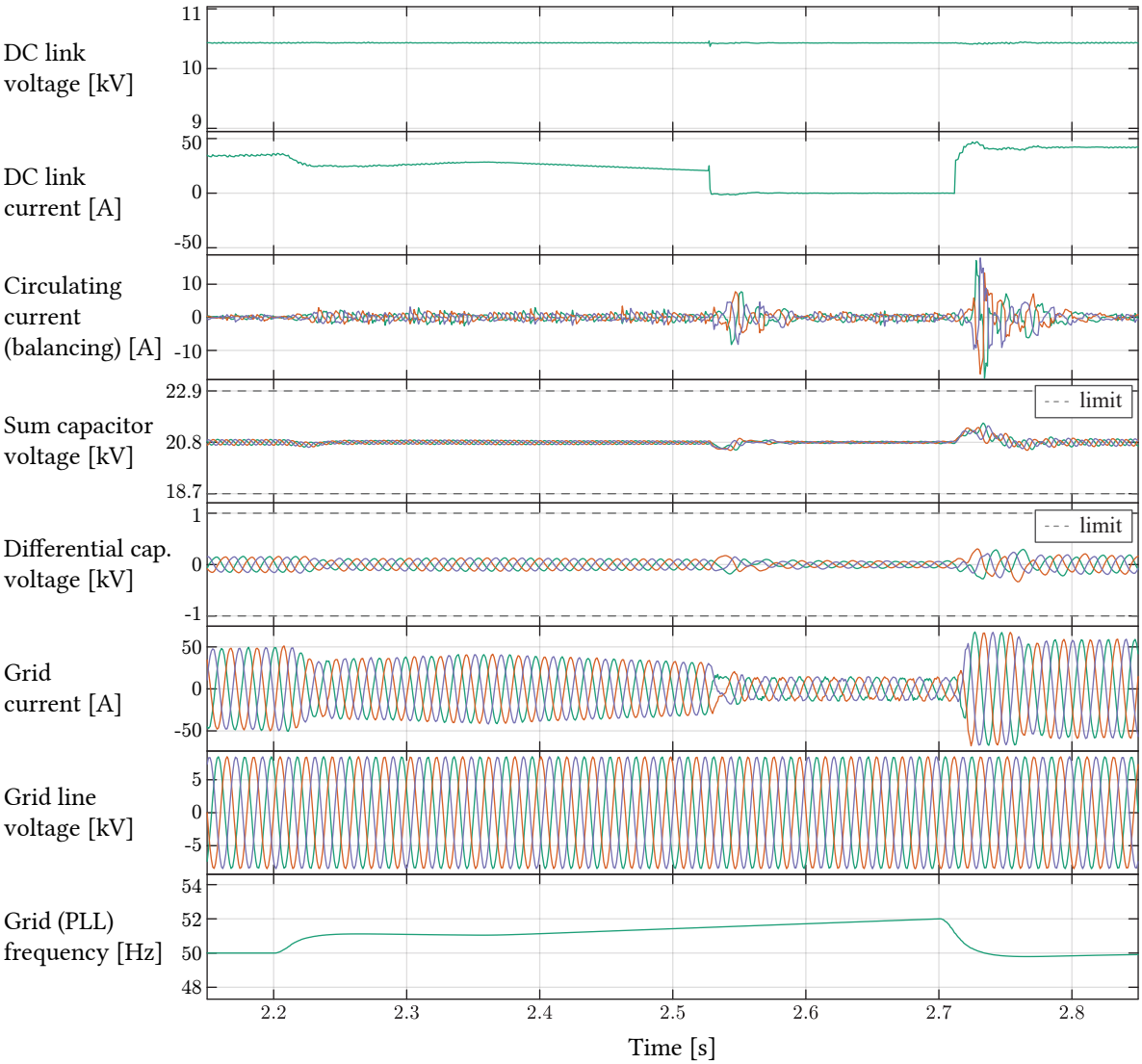


Fig. 3.31 Grid-side MMC operating sequence, corresponding to the frequency deviation test scenario from **Fig. 3.30** is presented. DC-link voltage control performed by this stage maintains the constant voltage amplitude. Sum- and differential capacitor voltages are contained within the ±10 % boundaries, presented by the dashed lines. Grid-side current is of sinusoidal waveform. Active and reactive power amplitudes correspond to the values calculated in the scaling block **Fig. 3.26**.

Machine-side MMC operation sequence corresponding to **Fig. 3.30** test scenario is presented in **Fig. 3.32**. Machine is operated at constant speed (rated) and constant torque equal to 90 % of rated value, equaling to power output determined in **Tab. 3.7**. Speed is controlled by the turbine circuit, by means of guide vanes control, as this is an established control approach in generating (turbine) mode of PHSP operation [62]. Synchronous machine can change loading torque setpoint with high gradient, limited only by the current controller dynamics. In such a case, if the turbine circuit speed controller cannot match the dynamics of machine loading torque change, rotor shaft speed deviation shall occur. However, as the machine and the grid are decoupled, this speed deviation is acceptable, and in fact represents the exploitation of the high inertia of rotating mass, that is typically a characteristic of

hydro generators. After such a transient in loading torque, turbine speed controller can compensate for the speed deviation over time and finally drive the error to zero, without the disturbance being visible from the grid terminals. Being decoupled from the grid, machine inertia can also be used as a flywheel, to support the grid with fast active power injection. Concerning the machine-side MMC internal control, sum- and differential capacitor voltages are within the predefined ±10 % boundaries.

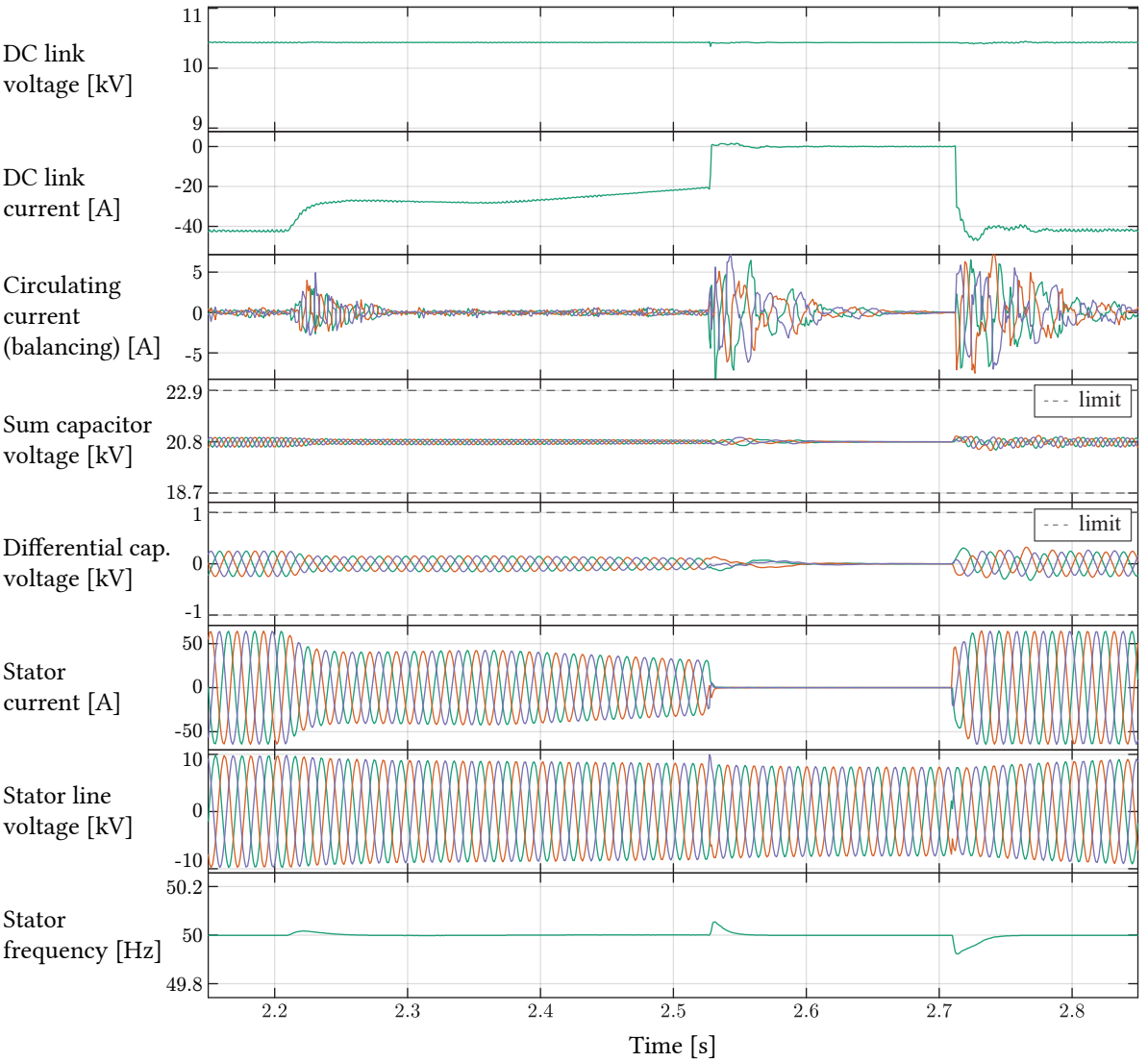


Fig. 3.32 Machine-side MMC operating sequence, corresponding to the frequency deviation test scenario from **Fig. 3.30** is presented. Machine is operated at fixed (rated) speed, extracting the energy from the hydraulic circuit at constant loading torque of 90 % of rated value. Speed control is performed by means of guide vane openings control, as accustomed in PHSP applications. Sum- and differential capacitor voltage ripple is contained within the ±10 % boundaries, presented by the dashed lines. Grid-side current is of sinusoidal waveform. Active and reactive power amplitudes correspond to the values calculated in the scaling block **Fig. 3.26**.

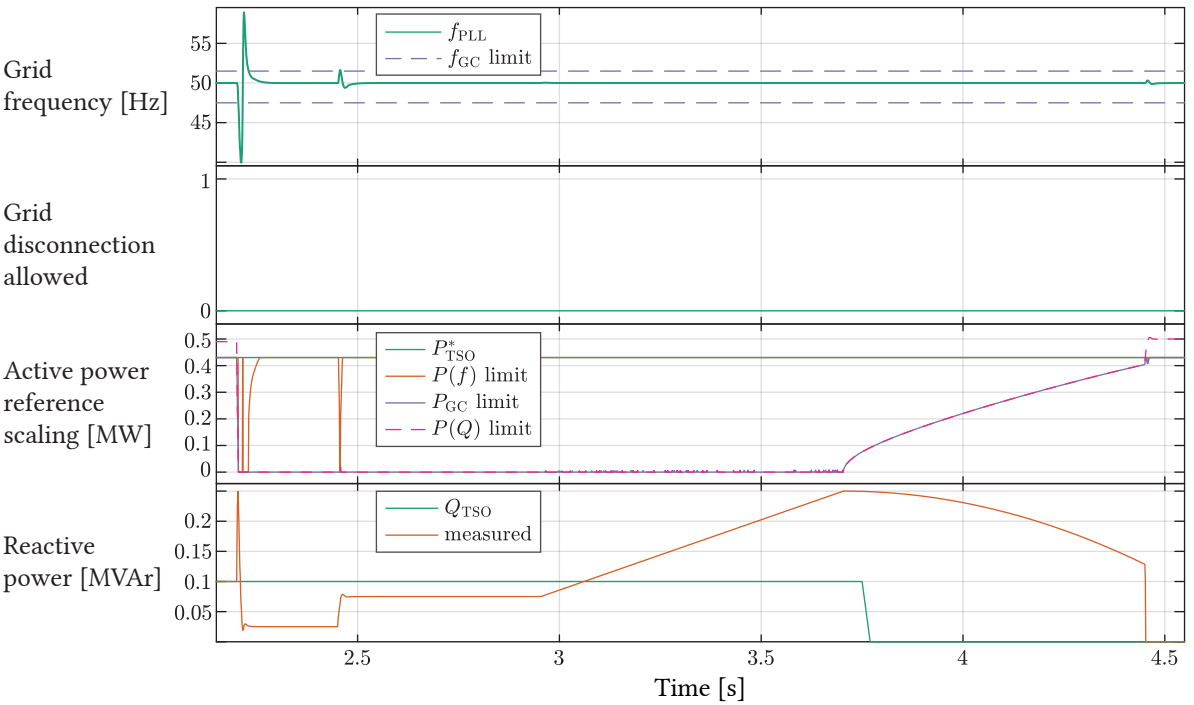


Fig. 3.33 Higher-level active and reactive power reference scaling for the symmetrical voltage dip test scenario, Type A of the **Fig. 3.24**. For this worst-case voltage dip profile (**Fig. 3.23**), the entire converter current carrying capacity is used for reactive current support. Active power delivery is gradually reestablished with voltage recovery during LVRT.

3.4.5.2 Symmetrical disturbance

The second test scenario comprises the LVRT sequence following the worst-case symmetrical voltage dip, Type A, presented in **Fig. 3.24**. Voltage recovery profile is taken for the most severe grid-code-defined case (**Tab. 3.6**) for Type 2 generating facilities, which is relevant for CFSM PHSPs.

For the voltage profile presented in **Fig. 3.23**, following voltage support requirement in **Fig. 3.22**, a varying degree of converter current carrying capacity must be allocated to reactive current provision to the grid. In turn, but also since the available AC voltage is decreased, active power reference is de-rated through the LVRT sequence.

Fig. 3.33 presents higher-level control I-MMC response to Type A LVRT sequence. The topmost graph presents PLL-obtained frequency, as well as upper and lower operation limits, according to **Fig. 3.21**. The next plot presents grid disconnection allowance signal, which is never active during this test scenario, as there is no transit into the shaded area of **Fig. 3.23**. Even though frequency deviation above the permitted range is already detected at the voltage dip instant, anti-disturbance time delay (40 ms) allows for PLL transient settling. The third plot presents the following:

- Active power reference obtained from the TSO, which is constant and set according to **Tab. 3.7**.
- Scaled active power reference, according to **Fig. 3.21**, which introduces no de-rating in this scenario due to rated frequency operation.
- Active power limit calculated based on converter current carrying capacity and instantaneous

reactive power demand, which is given priority, as presented in **Sec. 3.4.3**.

- Active power reference communicated to the machine-side converter, P^*_{machine}. During high voltage dip, the entire current capacity is reserved for reactive current support, thus active power allowance increases only with grid voltage amplitude increase.

The lowermost graph presents TSO reactive power reference and modified value according to **Fig. 3.22**.

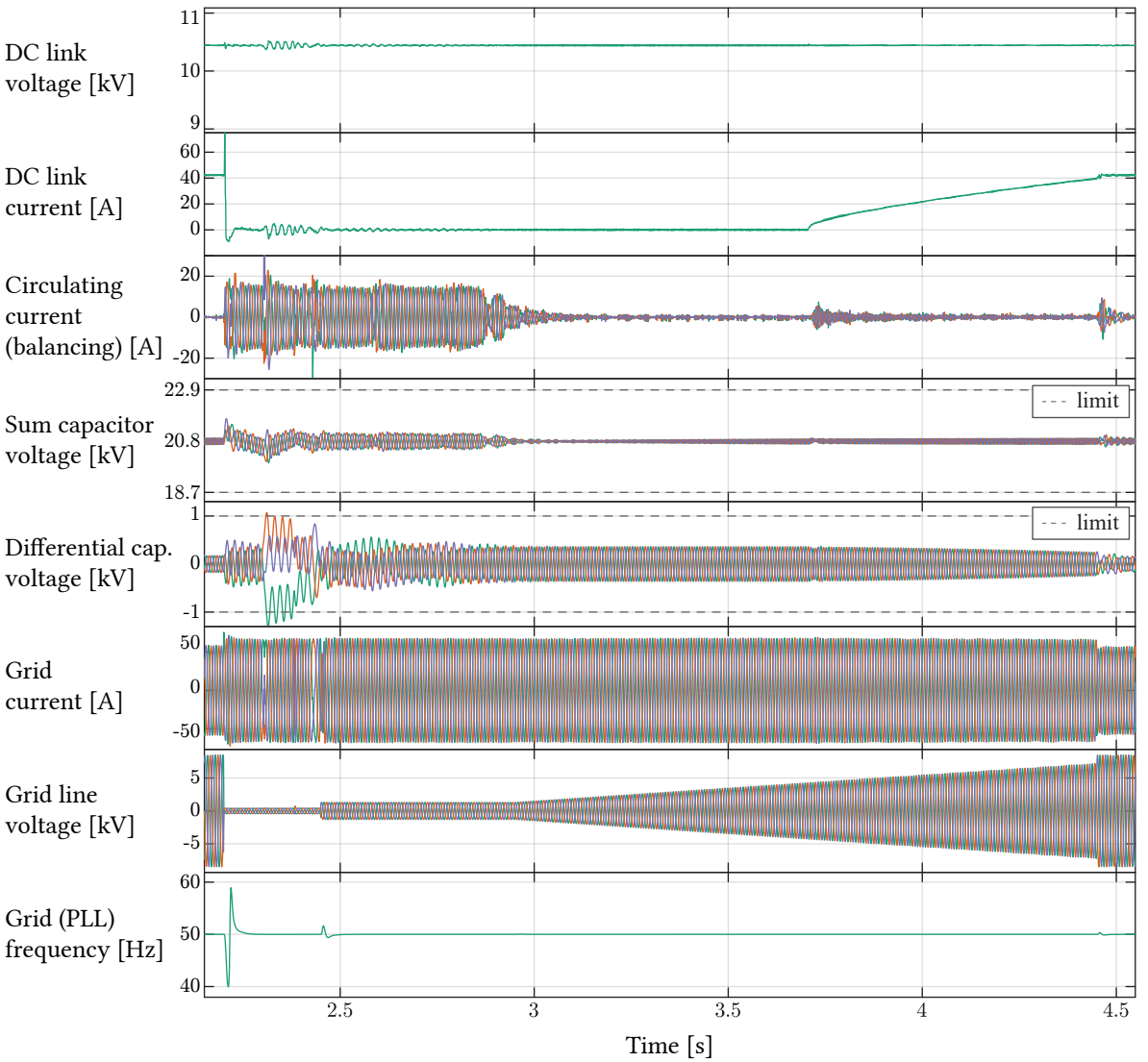


Fig. 3.34 Grid-side MMC operating sequence, corresponding to the worst-case LVRT test scenario from **Fig. 3.23** is presented. DC-link voltage control performed by this stage maintains the constant voltage amplitude. Sum- and differential capacitor voltages are contained within the ±10 % boundaries, with slight overshoot in differential voltage levels. Reactive current support to the grid is prioritized throughout the recovery (**Fig. 3.22**), with active power transfer being gradually reestablished during the fault clearance.

Grid-side MMC operation sequence corresponding to **Fig. 3.23** test scenario is presented in **Fig. 3.34**. DC-link voltage is controlled correctly throughout the transient. Sum- and differential capacitor voltages are within ±10 % limits, with slight overshoot in differential energy control during the most severe voltage dip. Grid-side output voltage is symmetrical and follows the LVRT recovery profile. Full grid current capacity is used for reactive current support, while active power transfer is gradually reestablished at the final stages of recovery. The effect is visible in DC link current amplitude, which is the image of active power transferred from- or to the machine-side.

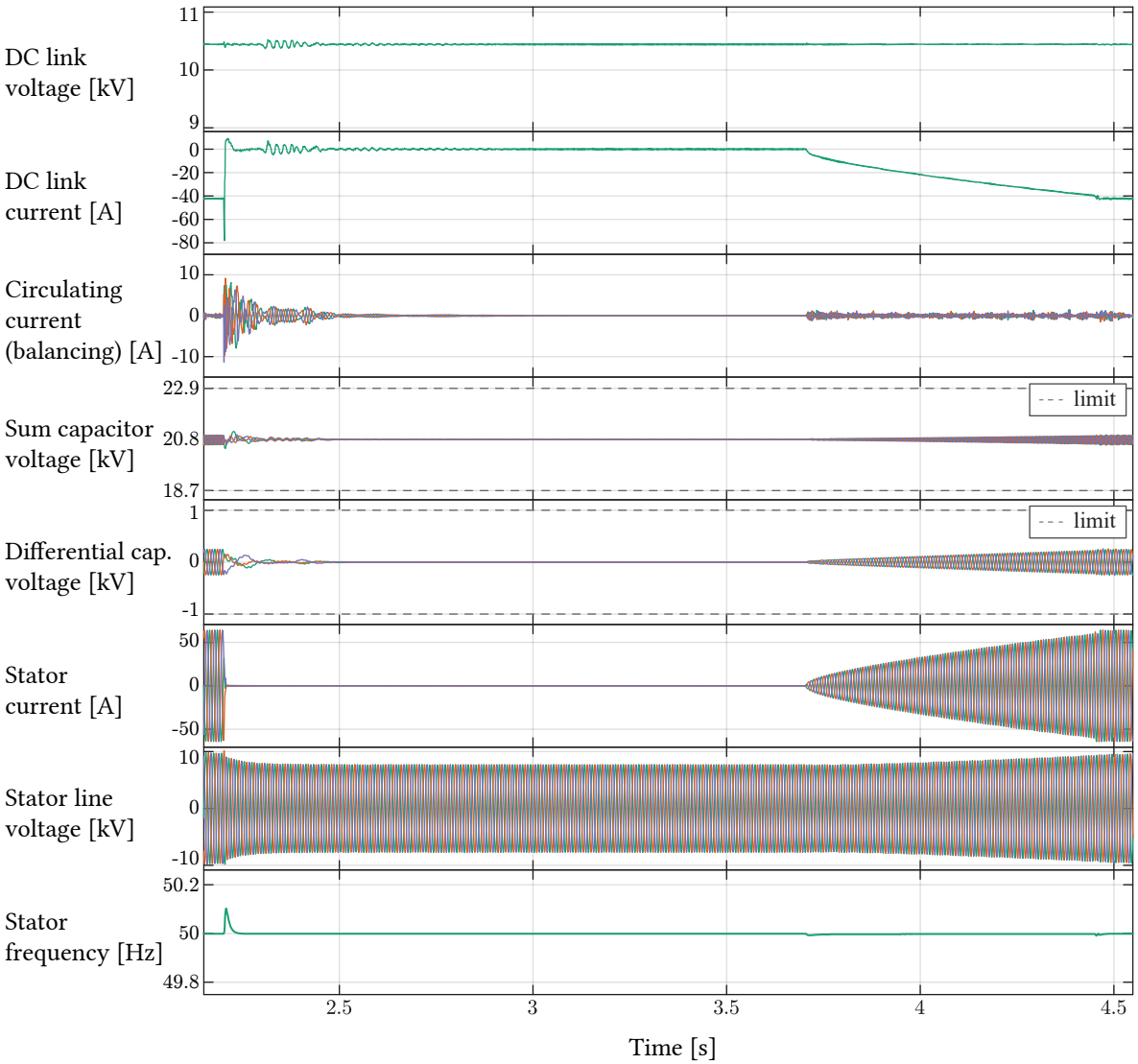


Fig. 3.35 Machine-side MMC operating sequence, corresponding to the worst-case LVRT test scenario from **Fig. 3.23** is presented. Machine is operated at fixed (rated) speed, extracting the energy from the hydraulic circuit at constant loading torque of 90 % of rated value. Speed control is performed by means of guide vane openings control, as accustomed in PHSP applications. Upon grid voltage dip, machine torque reference is immediately driven to zero, and active power transfer to the grid interrupted. A slight deviation in machine speed is visible through stator frequency plot; the prominence of this phenomena depends on the machine and hydraulic system inertia, however it does not affect the grid due to decoupling through the I-MMC.

Machine-side stage operating sequence corresponding to the worst-case symmetrical disturbance, i.e. LVRT test scenario **Fig. 3.23** is presented in **Fig. 3.35**. Machine is operated at constant speed (rated) and constant torque equal to 90 % of rated value, equaling to power output determined in **Tab. 3.7**. Speed is controlled by the turbine circuit, by means of guide vanes control, as this is an established control approach in generating (turbine) mode of PHSP operation [62]. At the occurrence of severe grid voltage dip, machine torque reference is immediately driven to zero. Due to inertia, machine speed and stator electrical frequency do show a transient (lowermost graph), which is rather small for the modeled 0.5 MVA machine (**Tab. 3.2**). As the machine is operated at unity power factor, interruption of active power transfer results in practically zero stator current amplitude. With the gradual grid fault clearance and voltage recovery, active power transfer is reestablished. Very low sum- and differential capacitor voltage ripple is present due to low current, while the average values are properly controlled.

3.4.5.3 Unsymmetrical disturbance

The third test scenario comprises the single-phase voltage dip of Type B, presented in **Fig. 3.24**. Voltage recovery profile is taken for the most severe grid-code-defined case (**Tab. 3.6**) for Type 2 generating facilities, which is relevant for CFSM PHSPs. The voltage dip is applied to phase *a* only.

Similarly to the symmetrical voltage disturbance (**Fig. 3.23**), a varying degree of converter current carrying capacity is reserved for reactive current provision to the grid. More active power can be delivered, however, as two phases are still unaffected by the fault.

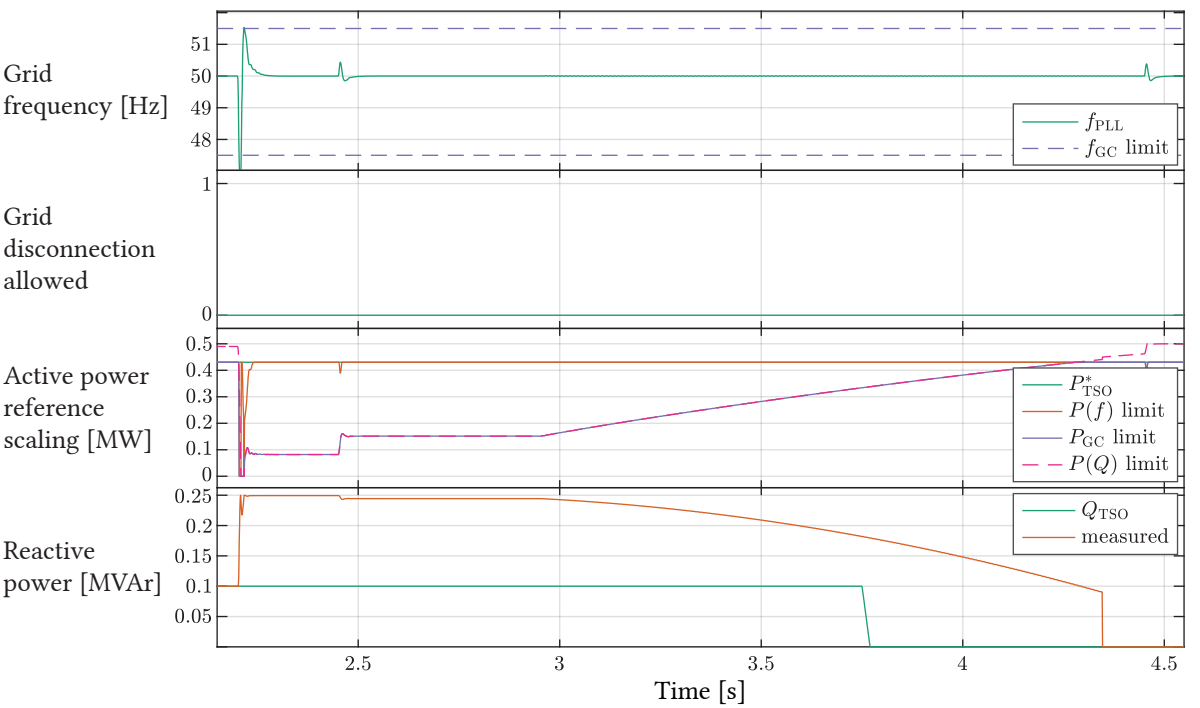


Fig. 3.36 Higher-level active and reactive power reference scaling for the Type B unsymmetrical voltage dip test scenario (**Fig. 3.24**). Worst-case voltage dip profile (**Fig. 3.23**) is applied to phase *a*, thus high share of converter current carrying capacity is initially used for reactive current support. Active power delivery is gradually reestablished with phase *a* voltage recovery.

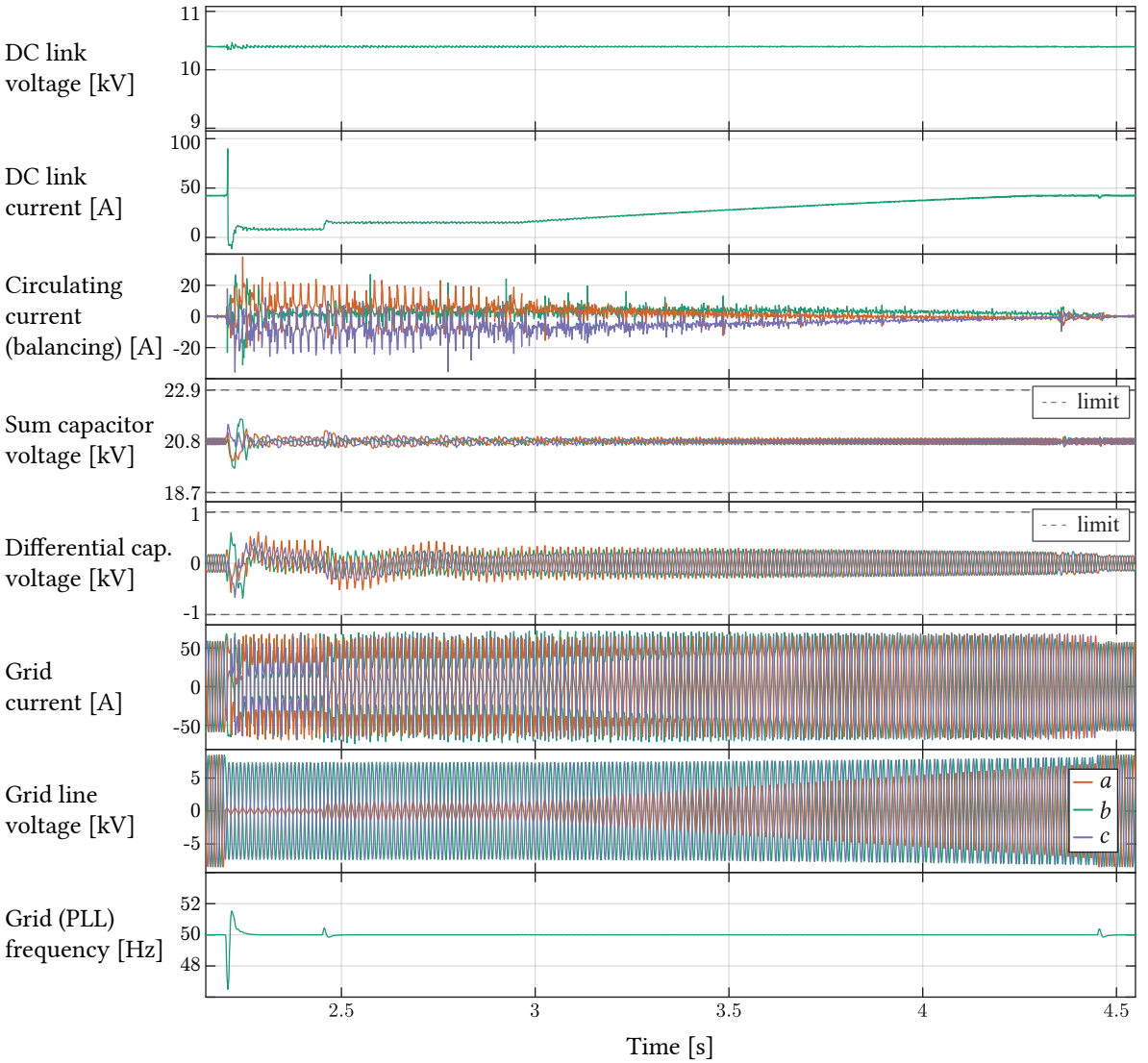


Fig. 3.37 Grid-side MMC operating sequence, corresponding to the Type B unsymmetrical grid voltage disturbance; Worst-case voltage dip profile of **Fig. 3.23** is applied to phase *a*. DC-link voltage control performed by this stage maintains the constant voltage amplitude. Sum- and differential capacitor voltages are contained within the ±10 % boundaries. Reactive current support to the grid is prioritized throughout the recovery (**Fig. 3.22**), with reduced active power transfer during the fault clearance. Unsymmetrical grid current is the consequence of forcing correct power reference tracking regardless of the unsymmetrical grid voltage conditions.

Fig. 3.36 presents higher-level control I-MMC response to Type B sequence, where **Fig. 3.23** profile is applied to phase *a*. The topmost graph presents PLL-obtained frequency, as well as upper and lower operation limits, according to **Fig. 3.21**. The next plot presents grid disconnection allowance signal, which is never active during this test scenario, as there is no transit into the shaded area of **Fig. 3.23**. Anti-disturbance time delay of the allows for PLL transient settling, thus no grid disconnection is performed during the initial voltage dip transient. The third plot presents the following:

- Active power reference obtained from the TSO, which is constant and set according to **Tab. 3.7**.

- Scaled active power reference, according to **Fig. 3.21**, which introduces no de-rating for the rated frequency operation.
- Active power limit calculated based on converter current carrying capacity and instantaneous reactive power demand, which is given priority, as presented in **Sec. 3.4.3**.
- Active power reference communicated to the machine-side converter, P^*_{machine}. During high voltage dip, a significant current capacity is reserved for reactive current support, with active power transfer capacity being gradually increased.

The lowermost graph presents TSO reactive power reference and modified value according to **Fig. 3.22**.

Grid-side MMC operation sequence corresponding to Type B test scenario (**Fig. 3.24**) is presented in **Fig. 3.37**. DC-link voltage is controlled correctly throughout the transient. Sum- and differential capacitor voltages are within ±10 % limits. Grid-side output voltage is unsymmetrical and follows the voltage recovery profile of each phase. Full grid current capacity is used, initially predominantly for reactive current support, while active power transfer is gradually reestablished.

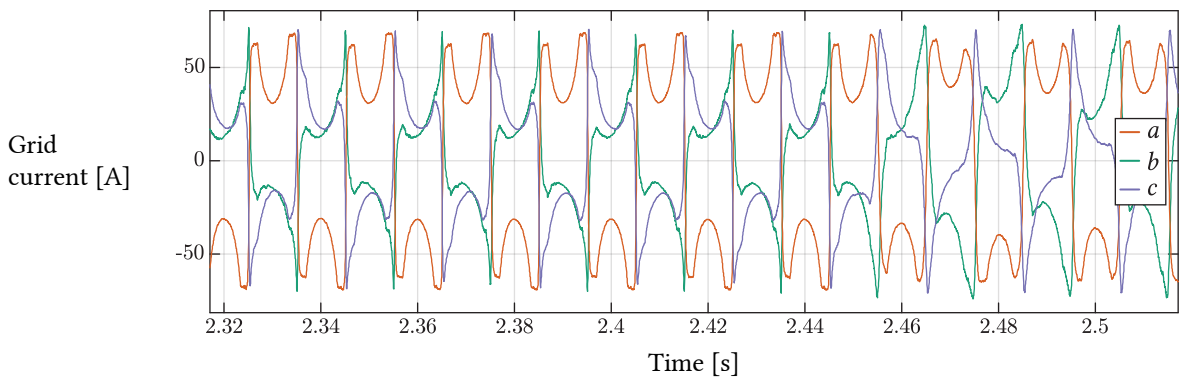


Fig. 3.38 Grid current waveform over the highest voltage dip of the Type B fault (**Fig. 3.24**), with phase *a* affected, as presented in the third test scenario. Instantaneous power theory is used to calculate grid current voltage references, leading to excellent tracking of active and reactive power references, at the expense of highly distorted current. Grid current spectrum is presented in **Fig. 3.39**.

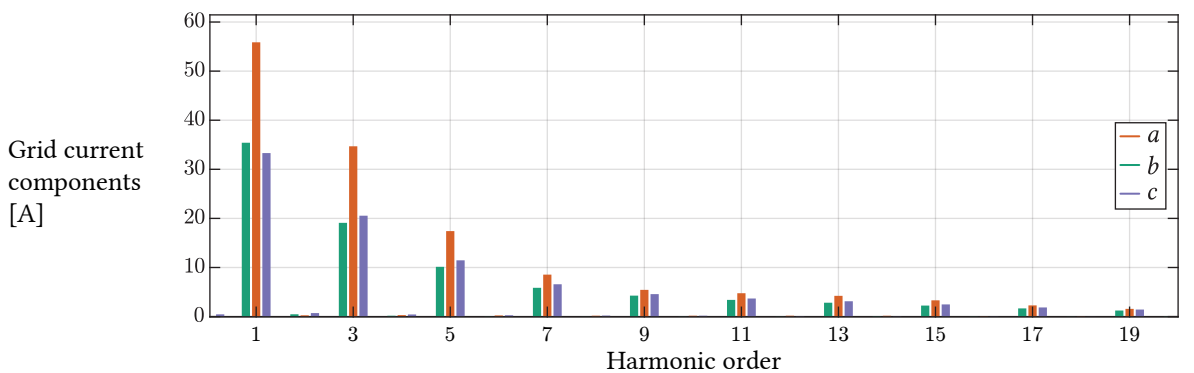


Fig. 3.39 Grid current spectrum is presented, for the current sequence presented in **Fig. 3.38**. Significant distortion originates in favoring power reference tracking under unbalanced grid voltage conditions, in this case Type B voltage imbalance (**Fig. 3.24**).

The effect is visible in DC link current amplitude, which is the image of active power transferred from- or to the machine-side. Grid current distortions are visible, as power references tracking is prioritized, regardless of the unsymmetrical voltage amplitudes.

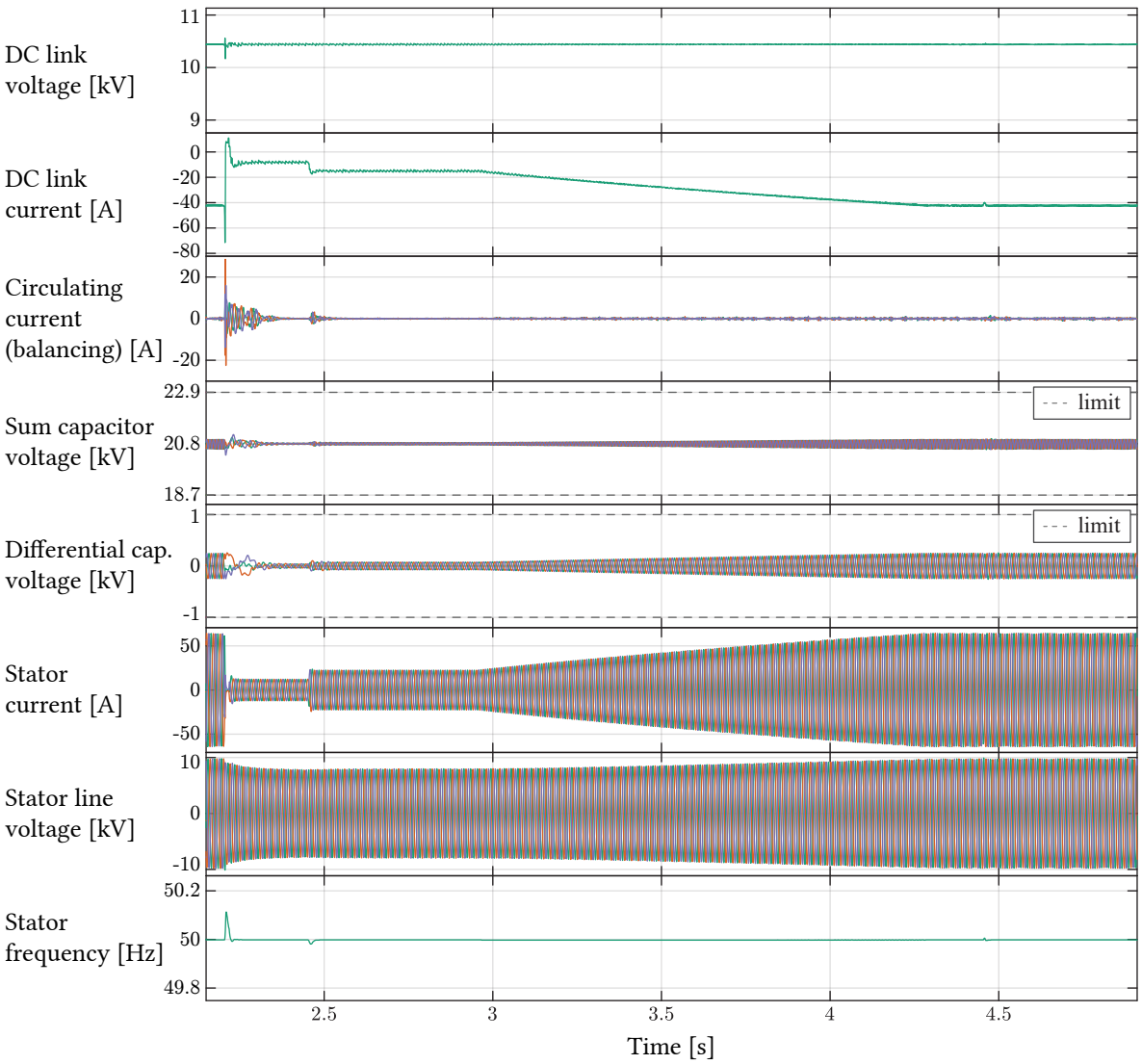


Fig. 3.40 Machine-side MMC operating sequence, corresponding to the worst-case Type B (**Fig. 3.24**) grid voltage imbalance affecting phase *a*, with voltage profile as in **Fig. 3.23**. Machine is operated at fixed (rated) speed, extracting the energy from the hydraulic circuit at constant loading torque of 90 % of rated value. Speed control is performed by means of guide vane openings control, as accustomed in PHSP applications. Upon phase *a* grid voltage dip, machine torque reference is immediately reduced, and active power transfer to the grid adapted to the maximal available capacity allowed by the reactive current grid support priority (**Fig. 3.22**). Sum- and differential capacitor voltage levels are kept within the ±10% limits. A slight deviation in machine speed is visible through stator frequency plot; the prominence of this phenomena depends on the machine and hydraulic system inertia, however it does not affect the grid due to decoupling through the I-MMC.

Grid current waveform during the initial voltage dip is presented in more details in **Fig. 3.38**. Highly distorted waveform is a consequence of utilization of instantaneous power theory for calculation of GCC references, thus favoring correct tracking of active and reactive power references under unbalanced grid voltage conditions. Spectral composition of grid current for the same time window is presented in **Fig. 3.39**.

Machine-side stage operating sequence corresponding to the worst-case Type B unsymmetrical disturbance (**Fig. 3.24**), i.e. LVRT test scenario **Fig. 3.23** is presented in **Fig. 3.40**. Machine is operated at constant speed (rated) and constant torque equal to 90 % of rated value, equaling to power output determined in **Tab. 3.7**. Speed is controlled by the turbine circuit, by means of guide vanes control, as this is an established control approach in generating (turbine) mode of PHSP operation [62]. At the occurrence of severe grid-side phase *a* voltage dip, machine torque reference is reduced to the newly available active power transfer capacity, dictated by the reactive current grid support (**Fig. 3.22**). Due to the hydraulic inertia, machine speed and stator electrical frequency do show a transient, which is rather small for the modeled 0.5 MVA machine (**Tab. 3.2**). With the gradual grid fault clearance and voltage recovery, active power transfer is reset to the initial value. Sum- and differential capacitor voltages are controlled within the adopted limits.

3.4.6 GCC reference calculation for unbalanced grid operation

So far, instantaneous *PQ* theory [50] has been used to calculate GCC current references, in both symmetrical and unsymmetrical grid disturbance scenarios. While results for normal operation and symmetrical disturbances are very good, it is under unsymmetrical voltage disturbances that this method indicates room for improvement.

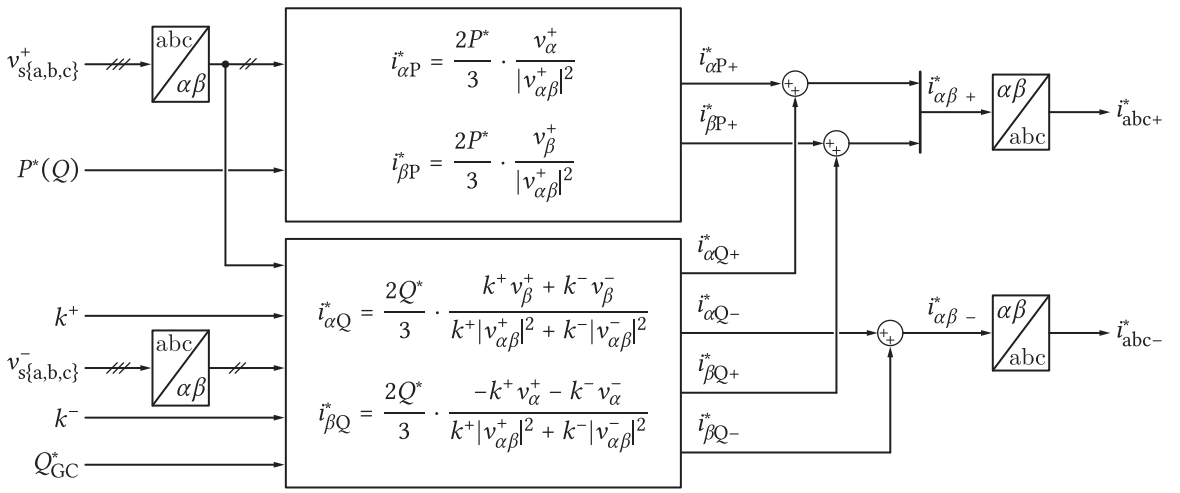


Fig. 3.41 Flexible voltage support control is presented. Positive and negative voltage sequence are decoupled. Consequently, grid current distortion during unsymmetrical grid disturbances is driven to a minimum, and traded for the active and reactive power ripple. Arbitrary choice of k^+ and k^- coefficients allows for additional voltage equalization support through the k^- factor. In two extreme cases, either maximum reactive power support in case of $k^+ = 1$, or maximum grid voltage equalization support in case of $k^- = 1$. In test scenario comprising Type B fault, factors were chosen at $k^+ = 1$, $k^- = 0$.

During voltage asymmetries, both positive- and negative voltage sequence occur. As GCC calculation is performed using power references and measured grid voltage, the total amplitude of both voltage sequences enters the calculation, providing distorted current references, i.e. components at higher harmonics. This is on one side presented in [63], but also visible in **Figs. 3.38** and **3.39**. The method correctly tracks active and reactive power references, at the expense of highly distorted current waveform.

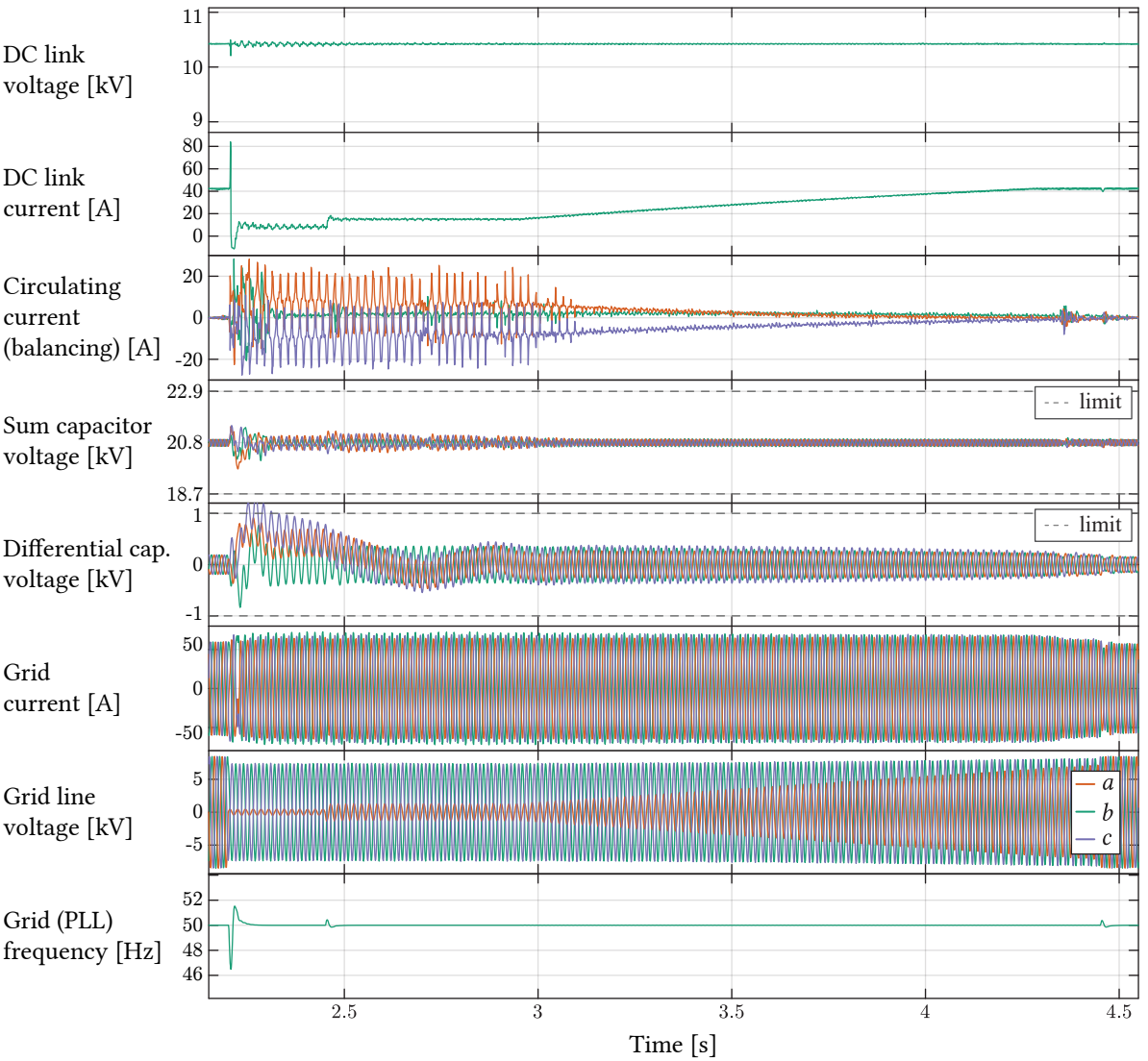


Fig. 3.42 Grid-side MMC operating sequence, corresponding to the Type B unsymmetrical grid voltage disturbance, with Flexible Voltage Support Control (FVSC) implemented; Worst-case voltage dip profile of **Fig. 3.23** is applied to phase *a*. DC-link voltage control performed by this stage maintains the constant voltage amplitude. Sum- and differential capacitor voltages are contained within the ±10 % boundaries, with an exception in differential voltage following the initial voltage dip. Reactive current support to the grid is prioritized throughout the recovery (**Fig. 3.22**), with reduced active power transfer during the fault clearance. Symmetrical grid current is favored over the correct power reference tracking, which in this case exhibits significant ripple.

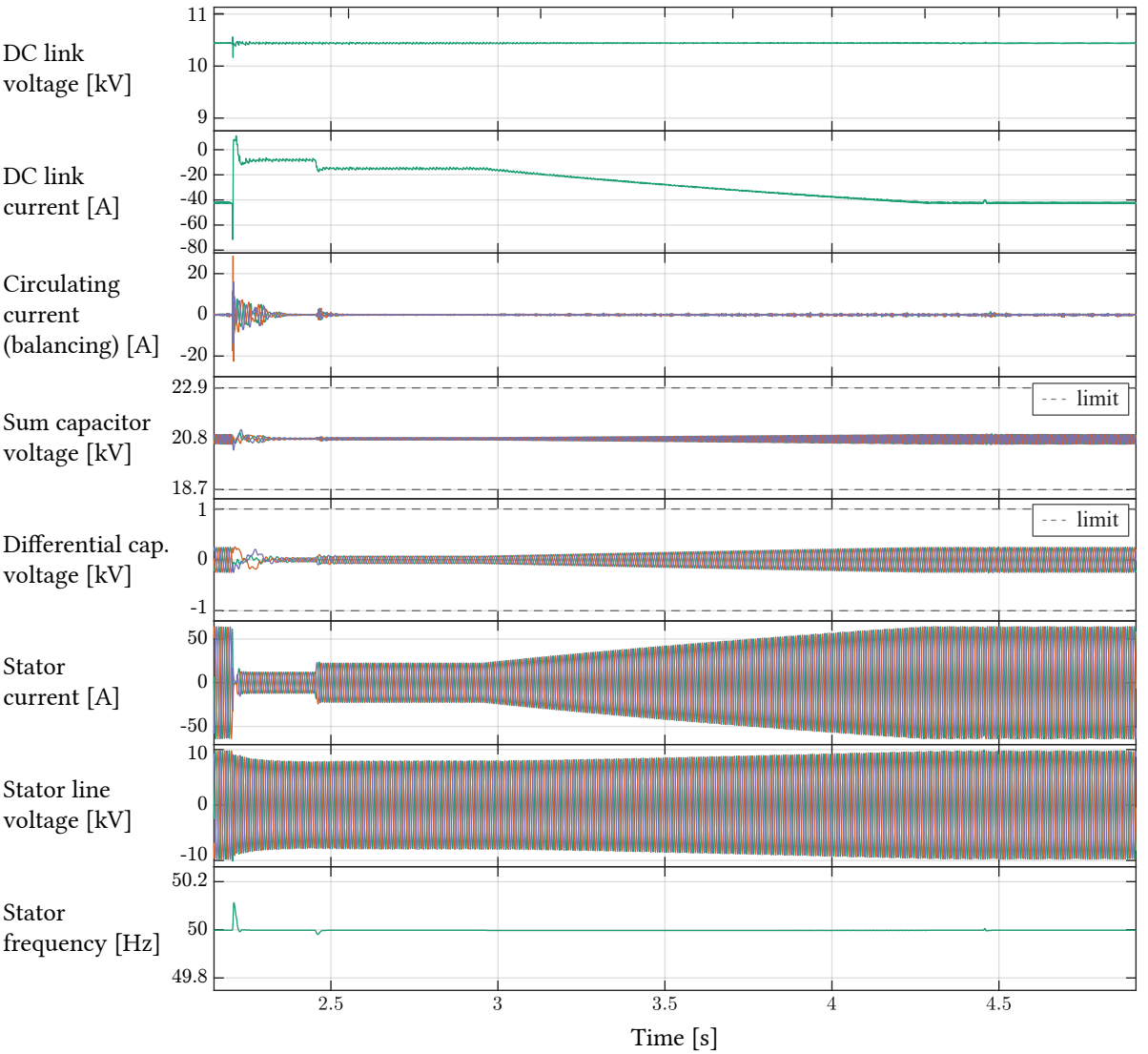


Fig. 3.43 Machine-side MMC operating sequence, corresponding to the worst-case Type B (**Fig. 3.24**) grid voltage imbalance affecting phase *a*, with voltage profile as in **Fig. 3.23**, with FVSC implemented on the grid side. Machine is operated at fixed (rated) speed, extracting the energy from the hydraulic circuit at constant loading torque of 90 % of rated value. Speed control is performed by means of guide vane openings control, as accustomed in PHSP applications. Upon phase *a* grid voltage dip, machine torque reference is immediately reduced, and active power transfer to the grid adapted to the maximal available capacity allowed by the reactive current grid support priority (**Fig. 3.22**). Sum- and differential capacitor voltage levels are kept within the ±10% limits. A slight deviation in machine speed is visible through stator frequency plot; the prominence of this phenomena depends on the machine and hydraulic system inertia, however it does not affect the grid due to decoupling through the I-MMC.

To mitigate this issue, an alternative form of GCC reference calculation method, namely FVSC, introduced in [63], has been implemented as an approach specifically developed to respond to grid requirements during unsymmetrical disturbance conditions. Within this control block, presented in **Fig. 3.41**, a decoupling of positive and negative voltage sequence amplitudes has been performed in such a way that grid current waveforms are practically free of distortion. FVSC current refer-

ence calculations are performed as follows [63], + and − denoting positive- and negative sequence, respectively.

$$i^*_{\alpha P} = \frac{2P^*}{3} \cdot \frac{v^+_\alpha}{|v^+_{\alpha\beta}|^2} \tag{3.55}$$

$$i^*_{\beta P} = \frac{2P^*}{3} \cdot \frac{v^+_\beta}{|v^+_{\alpha\beta}|^2} \tag{3.56}$$

$$i^*_{\alpha Q} = \frac{2Q^*}{3} \cdot \frac{k^+ v^+_\beta + k^- v^-_\beta}{k^+|v^+_{\alpha\beta}|^2 + k^-|v^-_{\alpha\beta}|^2} \tag{3.57}$$

$$i^*_{\beta Q} = \frac{2Q^*}{3} \cdot \frac{-k^+ v^+_\alpha - k^- v^-_\alpha}{k^+|v^+_{\alpha\beta}|^2 + k^-|v^-_{\alpha\beta}|^2} \tag{3.58}$$

Active power reference is translated to positive-sequence current reference. Reactive power reference can be realized through interaction with both positive and negative voltage systems, at an arbitrary proportion, defined by coefficients k^+ and k^-. Coefficient have been chosen to favor positive sequence system, as it would be the case with instantaneous *PQ* approach.

$$k^+ = 1 \qquad\qquad k^- = 0 \tag{3.59}$$

3.4.6.1 Unsymmetrical disturbance

The method was verified for the case of Type B voltage disturbance, as in the third test scenario (**Sec. 3.4.5.3**). Active and reactive power scaling are identical to the **Fig. 3.36**, as the choice of different grid current calculation block does not affect power scaling. The grid- and machine-side MMC stages' waveforms are presented in **Fig. 3.42** and **Fig. 3.43**, respectively. Compared to the test scenario of **Sec. 3.4.5.3** where instantaneous power theory was used for current reference calculation, grid-side MMC stage results (**Fig. 3.42**) demonstrate significantly lower grid current distortion. Sum- and differential capacitor voltages are kept within the predesignated boundaries, with an exception in differential voltage values just after the initial voltage dip.

Machine-side stage operating sequence corresponding to the worst-case Type B unsymmetrical disturbance (**Fig. 3.24**), while utilizing FVSC for the grid-side current reference calculations, is presented in **Fig. 3.43**. The test sequence is in no way different to the one presented under the test scenario **Sec. 3.4.5.3** utilizing instantaneous power theory for GCC calculation. Machine is operated at unity power factor; active power delivery profile corresponds to stator current. Sum- and differential capacitor voltages are well within the imposed limits.

The resulting grid current waveform and spectral content are presented in **Fig. 3.44** and **Fig. 3.45**, respectively. This is achieved, however, at the price of high ripple in active and reactive power values. From **Fig. 3.44**, grid current waveform appears distortion-free, as also confirmed in the spectral image of the current in **Fig. 3.45**.

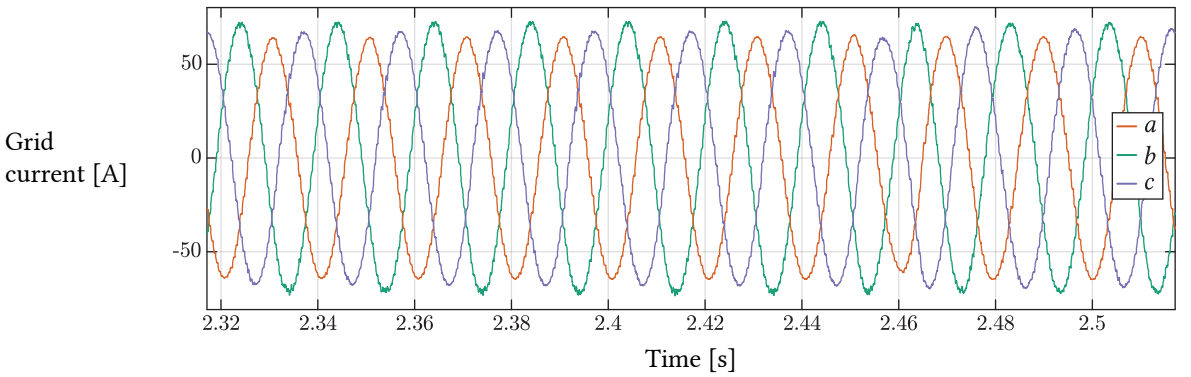


Fig. 3.44 Grid current waveform over the highest voltage dip of the Type B fault (**Fig. 3.24**), with phase *a* affected, as presented in the third test scenario. FVSC is used to calculate grid current voltage references, leading to low distortion of the grid current, at the expense of high ripples in active and reactive power reference tracking. Grid current spectrum is presented in **Fig. 3.45**.

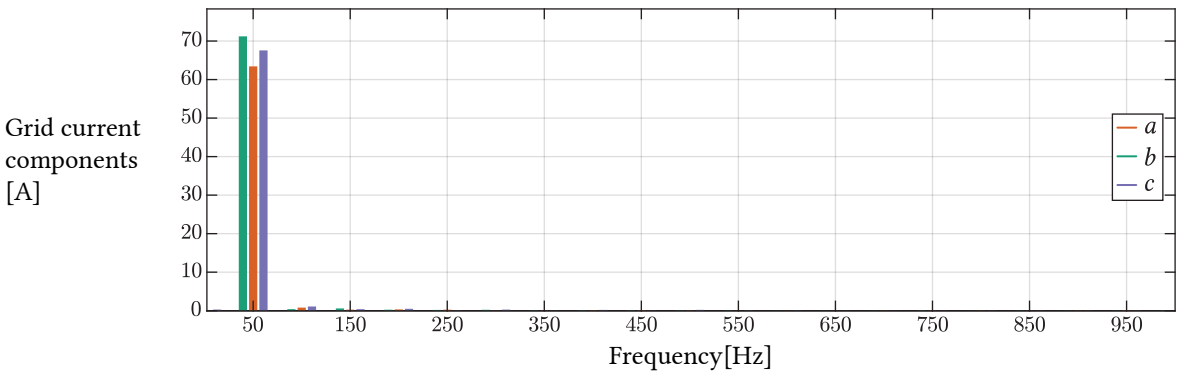


Fig. 3.45 Grid current spectrum is presented, for the current sequence presented in **Fig. 3.44**. Very low distortion is achieved through the use of FVSC under unbalanced grid voltage conditions, in this case Type B voltage imbalance (**Fig. 3.24**.

3.5 Summary

Relying on the converter control loops and ratings presented in the previous chapter, this chapter tackles PHSP-specific MMC operation requirements and control approaches to meet them. These comprise operation at rated machine torque over the complete frequency range, and grid-code compliance under grid disturbances.

LF operation of I-MMC under rated machine torque has been analyzed. Relation between high SM energy oscillation within this region, leading to prohibitively high capacitor voltage oscillations, is put in relation to converter operating variables. Two methods for full frequency range operation are identified – CM-voltage-based balancing action, and variable DC link voltage operation possibility. Machine-side control is modified to accommodate CM-voltage-based control action, and results are presented.

Grid-side control is modified to meet the grid-code-imposed requirements applicable to PHSP connected to the grid through a full-size converter. PLL has been modified to enable detection of unsymmetrical grid faults, which are the most common in the power system.

Three test scenarios were performed, covering normal operation, symmetrical grid disturbance and unsymmetrical grid disturbance, both under worst-case grid-code-defined LVRT voltage dip. The fourth test scenario proposes alternative grid current reference calculation, suitable to unsymmetrical abnormal grid states.

As the CM-voltage-based control strategy comprises high amplitude CM voltage stress to the machine, the next chapter proposed a variable DC link voltage method, enabling CM-voltage-free operation, while maintaining grid-code-compliance over the entire machine speed range.

4

Variable DC Link Voltage Operation for PHSP Retrofit

This chapter presents grid-code-compliant, CM-voltage-free machine operation over the entire PHSP operating range through the introduction of variable DC link voltage operation. AFE stage is replaced by a FB MMC to enable zero-to-rated DC link voltage variation. DC voltage control has been modified to ensure CM-voltage-free operation without additional energy balancing actions. Machine start-up sequence, pumping/turbine switch-over, as well as LVRT sequence have been demonstrated.

4.1 Low frequency CM-voltage-free operation

As shown in the literature [30] and discussed in the previous chapter, topology-specific requirements exist when supplying Variable Speed (VS) electric machines from MMC. Two methods for machine operation at rated torque, over the entire frequency range, have been identified in **Chap. 3**: CM-voltage-based [30], [31] and variable-DC-voltage-based [39]. The first relies on CM voltage injection with additional LF-range energy balancing action through additional circulating current components. The method introduces additional CM voltage stress to the machine ans is thus not suitable for retrofit applications.

The second method is based on variable DC link voltage operation of the I-MMC. Operation over the entire frequency range, at rated machine torque, without CM-voltage stress is achieved [39]. Starting from (3.18), dominant SM energy oscillating component in the LF region can be maintained constant by varying the DC link voltage reference.

As DC link voltage in I-MMC is a purely internal quantity, arbitrary value is allowed, as long as energy can be transferred between the grid- and machine-side stages within the DC current rating of the converter. Setting $V_{\mathrm{DC}} \neq V_{\mathrm{DC,n}}$, such that:

$$V_{\mathrm{DC}} = k_{\mathrm{DC}} V_{\mathrm{DC,n}} \qquad k_{\mathrm{DC}}/\omega_s = \text{const.} \tag{4.1}$$

SM voltage ripple (3.21) is constant irrespective of the operating frequency, without augmentation of C_{SM} and without the introduction of CM voltage injection as in [30].

Care must be taken, however, concerning SM insertion voltage requirements when varying DC link voltage reference. The effect of DC link voltage reference reduction differs in grid- and machine-side MMC stage. Under normal circumstances, grid voltage is in a narrow band around the rated value, defined by the grid code [55], regardless of the machine operating point. On the other hand, machine-side MMC AC output voltage amplitude is dependent on the output frequency.

Recalling (2.8), (2.9) and (4.1), if the DC link voltage is to be reduced, modified branch voltage reference is obtained. In an ideally balanced MMC conversion stage, without balancing circulating current components, while assuming branch insertion voltage reference can be expressed as:

$$v_{\{\mathrm{p,n}\}} = \frac{V_{\mathrm{DC,n}}}{2}\left(k_{\mathrm{DC}} \mp m_{\mathrm{s}} \cos\left(\omega_s t + \theta_s\right)\right) \tag{4.2}$$

where θ_s denotes AC voltage phase shift. Under operation at rated DC link voltage, where $k_{\mathrm{DC}} = 1$, insertion voltage reference is always positive, thus HB SMs can be utilized for low cost and losses. Conversely, it is straightforward to conclude that any DC voltage component reference lower than AC voltage component amplitude will lead to negative value of branch insertion voltage, disqualifying an all-HB MMC solution.

4.1.1 Machine-side stage

Branch insertion voltage reference of the machine-side MMC can be written as follows, based on (4.2), assuming $\theta_s = 0$.

$$v_{\{\mathrm{p,n}\}\mathrm{SM}} = \frac{V_{\mathrm{DC,n}}}{2}\left(k_{\mathrm{DC}} \mp m_{\mathrm{s,SM}} \cos\left(\omega_{\mathrm{s,SM}} t\right)\right) \tag{4.3}$$

Following the LF SM energy oscillation analysis performed in **Chap. 3**, DC link voltage reference, and thus k_{DC}, should be tied to stator supply frequency $\omega_{\mathrm{s,SM}}$, as in (4.1), to ensure constant value of the LF-dominant SM voltage ripple term derived in (3.21). At the same time, ensuring non-negative branch insertion voltage reference (4.3) would allow for the use of HB-based machine-side MMC. It is thus important to not oversee LF non-linearity in converter output voltage requirement when supplying machine in constant-torque mode.

As full machine speed range is required, approximation (3.14) leading to (4.1) cannot guarantee non-negative insertion voltage requirement. When operating the machine in the LF region, assuming rated torque and unity power factor, rated stator current is required. Under such circumstances, i.e. very low machine back-EMF, voltage drop over the stator resistance at rated current flow is not negligible, and must be compensated by the stator current controller. Thus, k_{DC} can be determined (4.4) to always satisfy FOC-generated stator voltage reference without driving (4.3) negative, assuming $m_{\mathrm{s,SM}} \in [0, 1]$.

$$k_{\mathrm{DC}} = m_{\mathrm{s,SM}} \tag{4.4}$$

Consequently, machine-side MMC can be operated for CM-voltage-free rated-torque machine supply, at variable DC link voltage reference, over the entire frequency range, with non-negative branch insertion voltage references. The machine-side stage can thus be realized utilizing HB SMs. According to (3.14), dominant LF SM capacitor voltage ripple component will consequently not be strictly constant over the LF range, as $k_{\mathrm{DC}}/\omega_{\mathrm{s,SM}} \approx$ const.. However, the presented results demonstrate that this effect can be ignored, as the ripple is well below the imposed limits.

4.1.2 Grid-side stage

In contrast to the machine-side stage, where non-negative branch insertion voltage reference can be achieved thanks to the nearly-linear linkage between stator supply frequency and voltage amplitude (V/f), grid-side stage must be controlled for the equal k_{DC} value at constant grid voltage amplitude.

Analogously to (4.3), grid-side branch voltage reference is obtained.

$$v_{\{\mathrm{p,n}\}\mathrm{grid}} = \frac{V_{\mathrm{DC,n}}}{2}\left(k_{\mathrm{DC}} \mp m_{\mathrm{s,grid}} \cos\left(\omega_{\mathrm{s,grid}} t\right)\right) \tag{4.5}$$

Depending on the active and reactive power references, as well as on the small grid-code-allowed deviations of grid voltage amplitude, AC voltage reference of the grid-side MMC stage is found in a narrow band around the rated value. This, for the normal operating conditions, translates to modulation index value, $m_{\mathrm{s,grid}}$, around unity value. It is clear from (4.5) that, neglecting a couple-of-percent band around rated value, practically any machine frequency below rated results in $k_{\mathrm{DC}} < m_{\mathrm{s,grid}}$, leading to the negative branch insertion voltage reference requirement at the grid-side.

In an all-HB I-MMC, as presented in **Chap. 3**, the lowest attainable DC link voltage is limited by the grid voltage amplitude, allowing only for slight reduction below $V_{\mathrm{DC,n}}$ value, achieved by voltage boosting action defined by desired control voltage reserve in the converter.

Variable DC link voltage operation, over the entire $V_{\mathrm{DC}} \in [0, V_{\mathrm{DC,n}}]$ range of (4.4), is in this chapter enabled through the use of bipolar FB SMs in the grid-side MMC stage [39], as presented in **Fig. 4.1**. Since an all-FB MMC stage can provide any DC link voltage value in the range of $V_{\mathrm{DC}} \in [-V_{\mathrm{DC,n}}, V_{\mathrm{DC,n}}]$, the use of all-FB design is clearly an over-engineered solution for the VSD application requiring only half of that range. However, **Fig. 4.1** and the control method presented in this chapter have no limitations in terms of grid-code requirements and no penalties in terms of CM-voltage machine stress. The presented solution will serve as a reference design for the novel control- and design methods developed presented in the upcoming chapters, specifically for PHSP applications, with the aim to reduce the number of FB SMs in the converter while introducing as few trade-offs compared to an all-FB AFE reference design.

While definitely being a more costly solution compared to an all-HB I-MMC where machine-stage is operated as [30], the proposed topology (**Fig. 4.1**) offers sine-wave-alike supply to the machine,

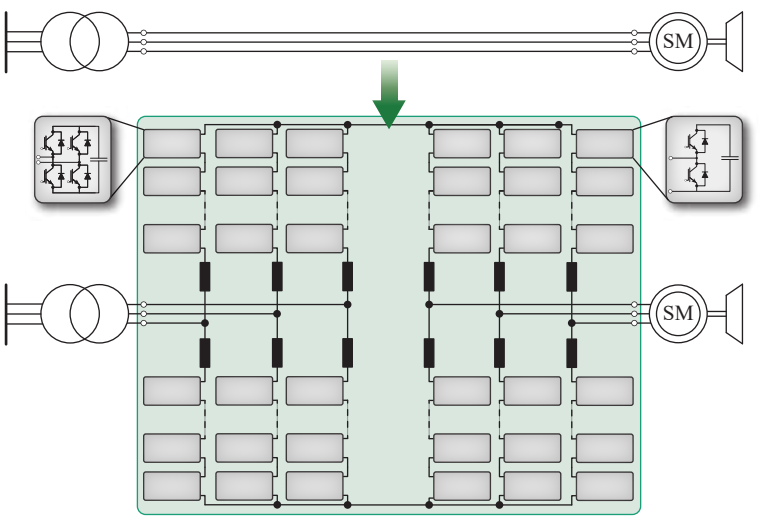


Fig. 4.1 Retrofit of an existing PHSP with I-MMC for conversion to VS operation, without machine modifications. Grid-side stage is realized as a FB MMC, while a HB MMC is utilized for the machine-side stage. An optional converter bypass is omitted.

without prohibitively-high-amplitude CM voltage, over the entire frequency range. Further, no additional circulating balancing currents are imposed in the LF region. Grid-code compatibility is also preserved, as the operating area of FB-based AFE towards the grid is independent on the actual DC link voltage reference. Existing machines can thus be kept in operation with no modifications.

4.2 Converter control

Grid-code-compliant higher-level control system is equal to the one developed in **Sec. 3.1**. Control schemes utilized in the existing VS PHSPs [62] are respected. The control system is outlined in **Fig. 4.2**. TSO-scheduled active and reactive power references are, if necessary, scaled by grid-code-defined frequency- and voltage-support functions $P(f_g)$ and $I_Q(v_g)$ [55]. If both support actions are simultaneously required, advantage can be given to either of them, by scaling of the lower-priority one according to converter current limit (**Sec. 3.4.3**). Reactive power is prioritized in the simulations hereafter.

4.2.1 Grid-side higher-level control

AFE stage has dual role. Firstly, exchange of reactive energy with the grid is performed according to TSO schedule, grid code, or contracted ancillary service, regardless of the WRSM operating state. Grid-code-scaled reactive power reference Q^*_{grid} is fed to the GCC.

Secondly, DC link voltage is controlled through active energy exchange with the grid, at reference P^*_{grid}, equal to grid-code-scaled P^*_{SM}, slightly augmented to supply converter losses.

4.2.2 Machine-side higher-level control

Inverter Unit (INU) stage exchanges active energy with the hydraulic system at grid-code-scaled reference P^*_{SM} – pumping or generating, at arbitrary power factor (unity in this case), as it is decoupled from the grid. P^*_{SM} and water head H are fed to an algorithm that outputs optimal machine speed for highest hydraulic system efficiency. Turbine controller operates guide vanes following ω^*_{opt}. Based on P^*_{SM} and instantaneous WRSM speed, FOC performs machine torque control. Dynamics of response to the P^*_{SM} change is thus determined by fast machine current control. As in **Chap. 3**,

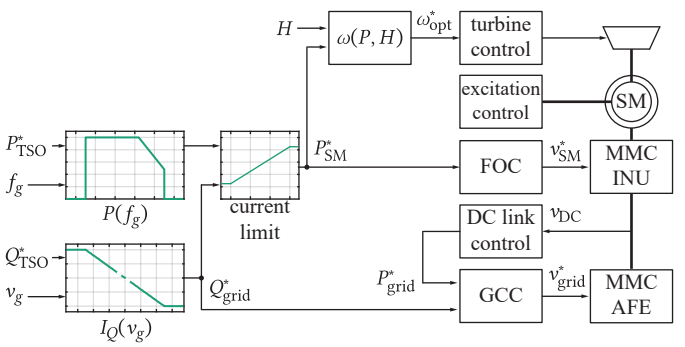


Fig. 4.2 Overview of the complete control system structure of the proposed converter. Active and reactive power references are fed to the machine- and grid-side conversion stages, respectively. FOC operates the machine at unity power factor and constant excitation current, while shaft speed is controlled for optimal hydraulic efficiency by the turbine controller. DC link voltage is controlled by the grid-side stage.

WRSM excitation controller is operated in the constant flux mode up to the rated speed, with the possibility of field-weakening operation should the speed above rated be required.

4.2.3 Internal MMC control

Energy balancing control loops are implemented equally in both INU and AFE stage, the only difference being in total energy control – while INU is supplied from the DC link, AFE is supplied from the grid. Internal control loops are derived in **Chaps. 2** and **3**.

4.3 Test scenario

Two test scenarios have been defined, aiming to cover the typical PHSP operating sequences under normal grid conditions and LVRT during worst-case grid-code-defined symmetrical voltage dip. SM voltage deviation limit of ±10 % is adopted, at total energy of 84.4 J/kVA per MMC stage (**Tab. 2.2**). This is in accordance with the analysis in [30], where voltage deviation limit just below ±20 % was obtained at 42 J/kVA of stored energy per stage.

4.3.1 VS PHSP operation

Test scenario sequence is presented in **Fig. 4.3**. Machine torque is kept constant at 90 % of rated value. Speed reference is varied from standstill, to positive rated, followed by change of direction (i.e. operating mode) under constant torque. WRSM is operated at unity power factor, while grid-side reactive power reference is varied in the range of −20 % to 20 % of apparent power (**Tab. 2.2**).

4.3.2 LVRT evaluation

LVRT capability of the proposed design has been evaluated for the worst case grid-code-defined scenario [55], for Type 2 generating facility, i.e. plant connected to the grid trough a converter, presented in **Fig. 3.23**. Highest voltage dip of 95 % is thus considered.

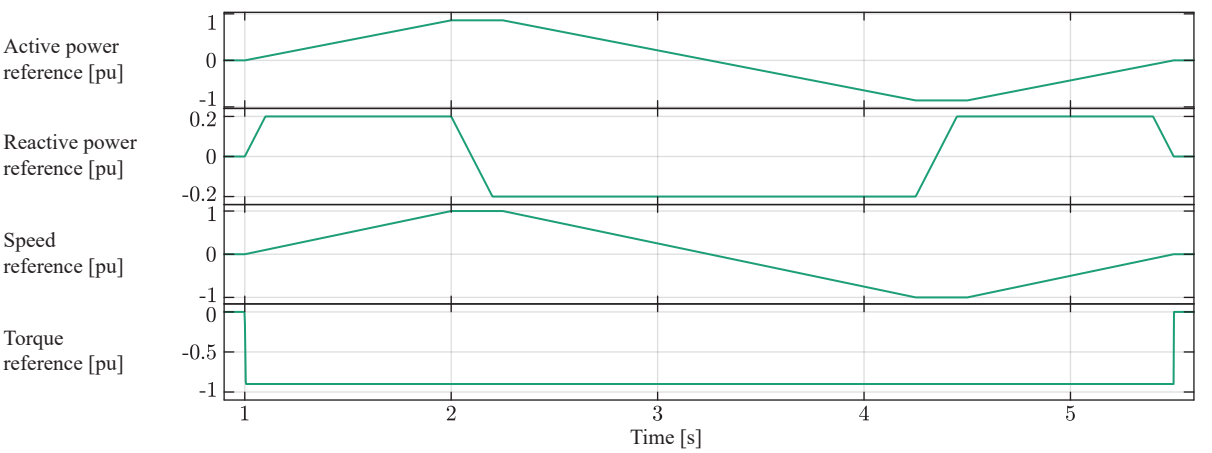


Fig. 4.3 Test scenario reference values, top to bottom: grid-side active power (0.9 pu), grid-side reactive power (0.2 pu), PHSP speed reference (−1 pu to 1 pu), WRSM torque (−0.9 pu).

4.4 Simulation results

4.4.1 Machine-side VS PHSP operation

Machine-side stage sequence of operation, corresponding to **Fig. 4.3** test scenario, is presented in **Fig. 4.4**. Constant torque reference is correctly tracked over the entire speed range, including zero-crossing. As DC link voltage is now varied proportional to speed, DC current is constant. Significant transients expectedly occur during step-change in i_{DC} reference, caused by step change in torque reference at $t \in \{1\,\mathrm{s}, 5.5\,\mathrm{s}\}$ and by P^*_{SM} sign change-over at zero speed crossing, causing step change of sign in i_{DC} at $t \approx 3.25\,\mathrm{s}$. Both sum and differential capacitor voltage ripple are constant over the entire frequency range, with the exception of an overshoot occurring at zero crossing, around $t = 3.25\,\mathrm{s}$. This, however, stays within the imposed boundaries.

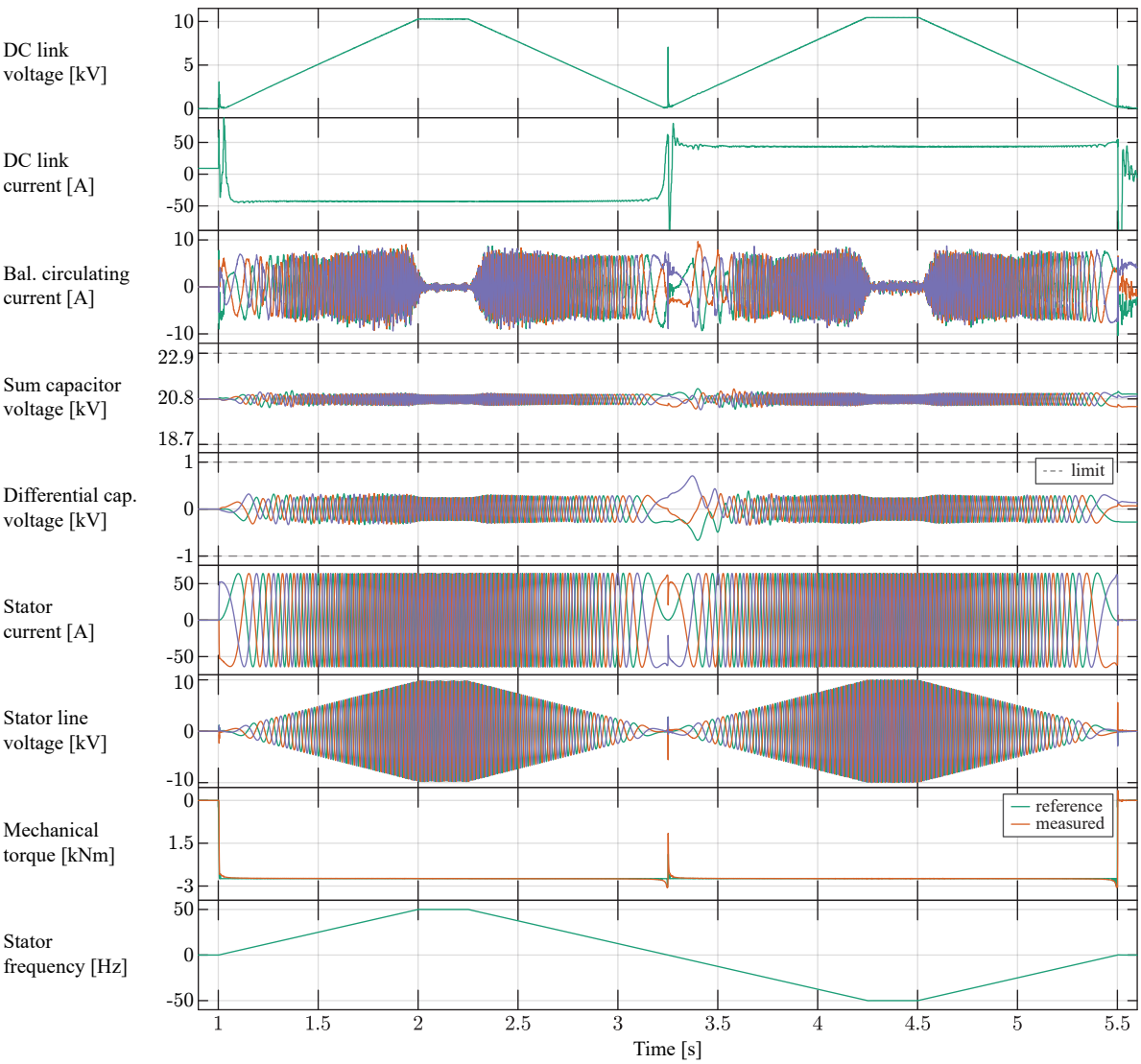


Fig. 4.4 Machine-side MMC full cycle of operation according to the test scenario of **Fig. 4.3**.

4.4.2 Zero-crossing capacitor ripple

As the simulation results confirm, machine-side SM capacitor ripple is indeed constant at frequencies down to zero. However, right after frequency zero-crossing, **Fig. 4.5** shows a significant rise in capacitor voltage of the upper branches of phases a and c occurs at $t = 3.35\,\mathrm{s}$. This transient cannot be evaluated assuming sinusoidal waveform of (3.12), but rather by observing instantaneous voltage and current state of a SM, given for phase a in **Fig. 4.6**.

Approaching zero-speed at sinusoidal voltage and current waveforms, Δv_{SM} is constant, according to (3.21). During $t \in [3.25\,\mathrm{s}, 3.35\,\mathrm{s})$, upper branch inserted voltage equals zero, i.e. all SMs are disconnected, consequently there is no change of SM charge, voltage remains constant. During approximately $t \in [3.35\,\mathrm{s}, 3.4\,\mathrm{s})$, inserted voltage is rising, while upper branch current is positive, charging upper SMs, leading to positive Δv_{SM} and rise in SM voltage. Control action cannot discharge the HB SM under these conditions. At $t = 3.4\,\mathrm{s}$, branch current crosses zero becoming negative. As instantaneous branch power (3.3) is negative, SMs are being discharged until $t = 3.44\,\mathrm{s}$. Lower branch can be analyzed in the same manner.

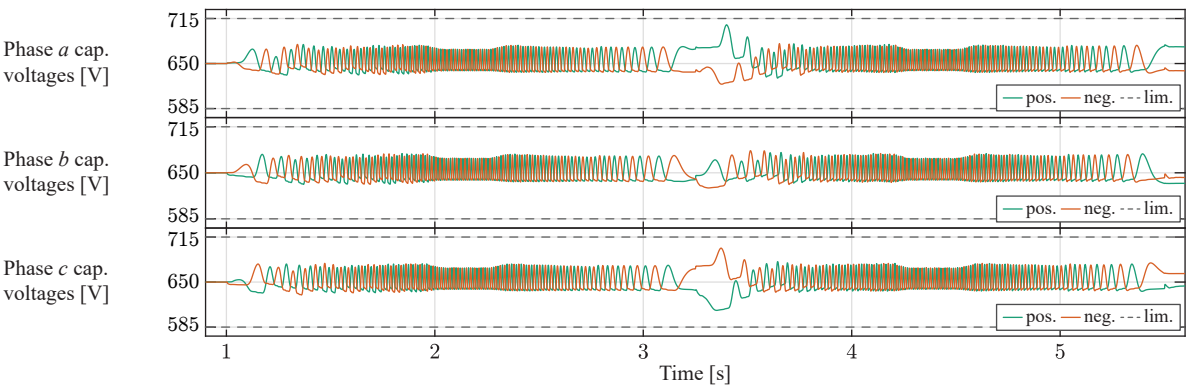


Fig. 4.5 Per-phase capacitor voltage ripple of the machine-side MMC stage, for **Fig. 4.3** test profile.

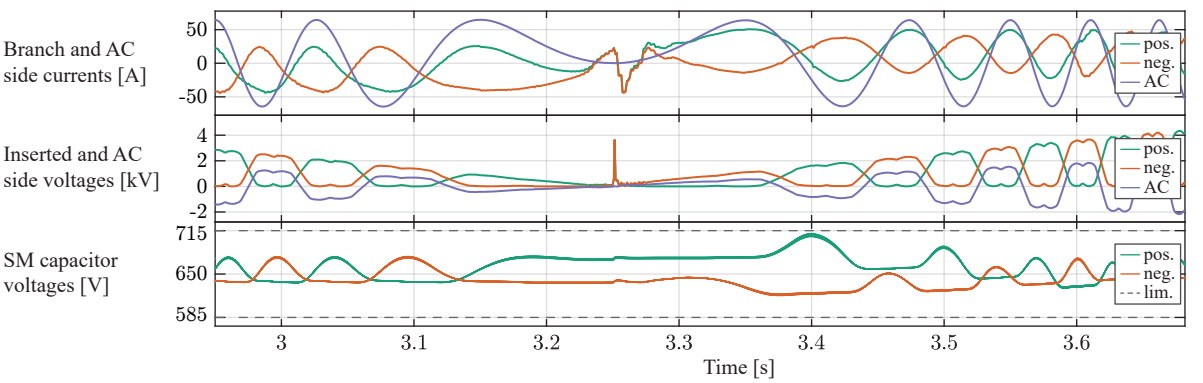


Fig. 4.6 Phase a transient is presented, for zero-speed crossing under constant torque. A low-amplitude third harmonic voltage is injected for better DC link utilization. Lowermost graph presents an envelope of all SM capacitors' voltage, color-coded to upper and lower branch.

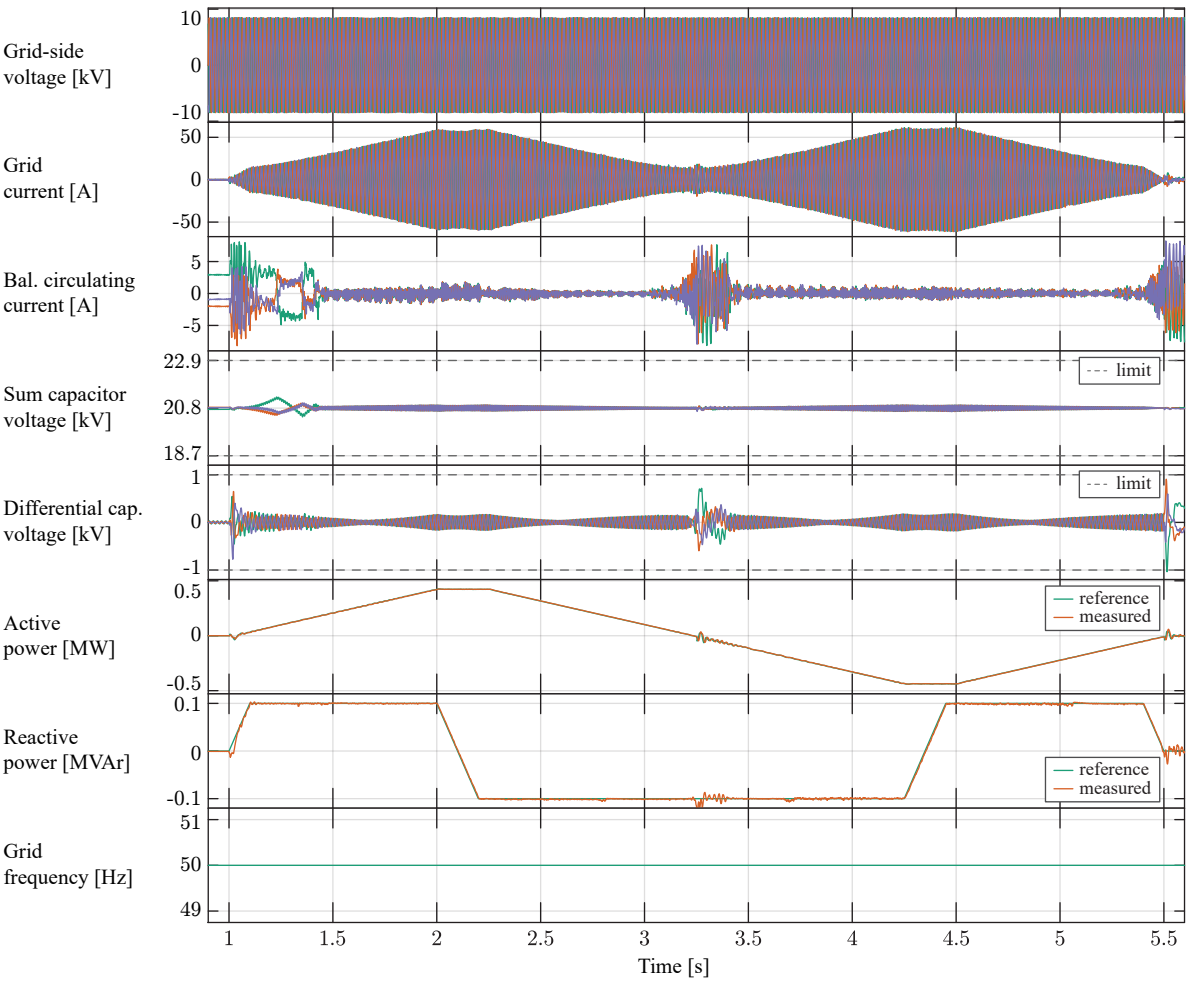


Fig. 4.7 Grid-side MMC full cycle of operation according to the test scenario of **Fig. 4.3**.

4.4.3 Grid-side variable-speed PHSP operation

AFE MMC stage operation sequence, following test scenario **Fig. 4.3**, is presented in **Fig. 4.7**. Correct active and reactive power tracking is performed. DC link voltage is correctly controlled (**Fig. 4.4**). Capacitor voltage is stable across the operating range, with transients at DC current step change. By that, it can be concluded that the both grid and machine side are successfully decoupled.

4.4.4 LVRT

PHSP response to the most severe LVRT profile defined for Type 2 generating facility in [55], is presented in **Fig. 4.8**. Immediately upon fault occurrence, WRSM torque reference is driven to zero. Machine torque control reduces torque output from 0.9 pu to 0 pu in 5 ms. For converter parameters in **Tab. 2.2**, as PSC-PWM is used, apparent switching frequency of $f_{\text{app}} = N_{\text{SM}} f_{\text{sw}} \approx 16\,\text{kHz}$ leads to theoretical current, i.e. torque, control bandwidth of $10T_{\text{app}} = 625\,\mu\text{s}$. A speed deviation (acceleration) from reference is observed upon removal of WRSM torque. In higher-inertia systems, this deviation can be less significant. As hydraulic system dynamics is decoupled from the grid, these mismatches are acceptable. On the grid side, AFE stage utilizes full current capacity for reactive current support

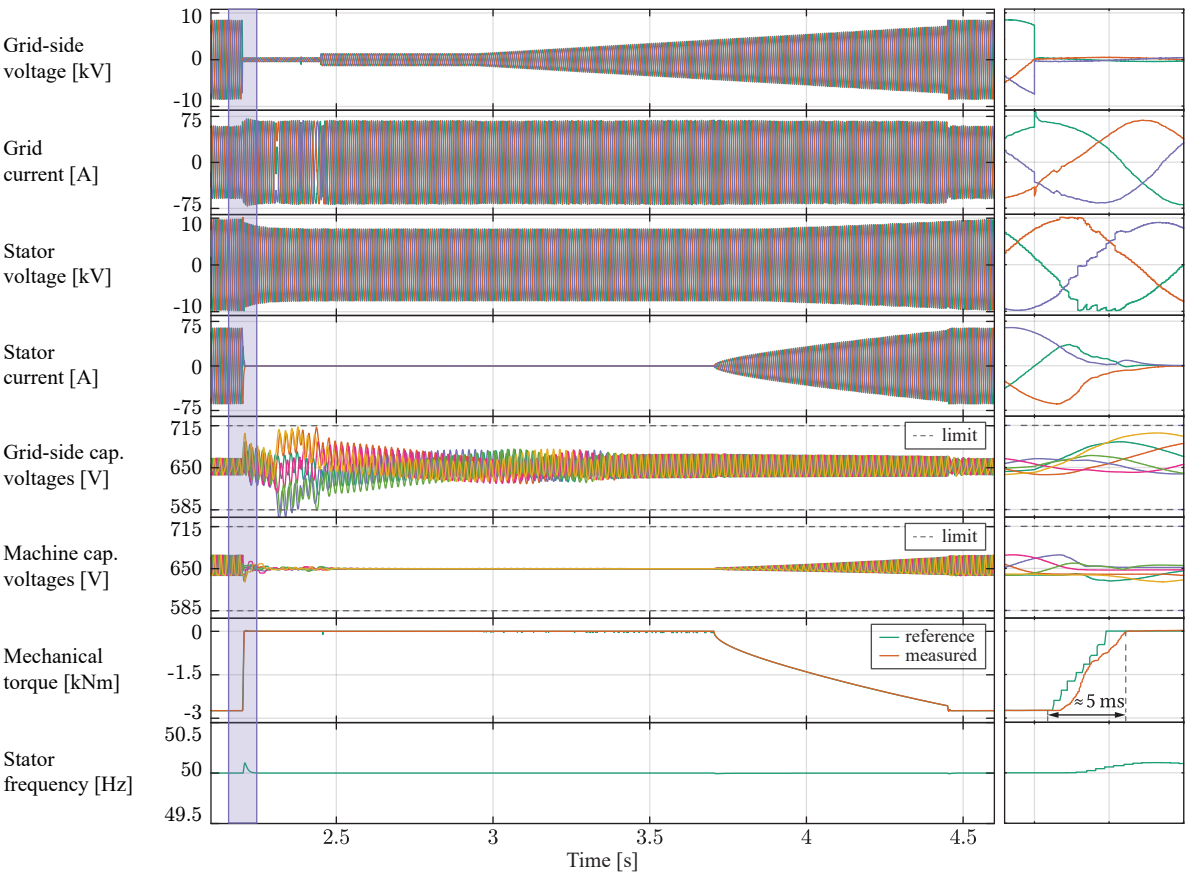


Fig. 4.8 LVRT sequence of operation according to worst-case scenario defined in [55] (see **Fig. 3.23**). Highlighted section is zoomed in.

to the grid. As grid voltage gradually recovers, active energy delivery is resumed.

4.5 Summary

Relying on the SM energy fluctuation analysis over LF operating region, presented in **Chap. 3**, CM-voltage-free solution for PHSP I-MMC operation has been introduced in this chapter. Unlike CM-voltage injection method, variation of DC link voltage reference with machine frequency has been performed. In this way, CM-voltage-free operation is achieved over the entire PHSP operating range, at no additional balancing action in the LF operating region.

Two representative test scenarios have been presented, namely operation under normal grid conditions at variable power factor, and worst-case symmetrical grid fault behavior. Full PHSP operating range, under rated torque, including zero-crossing in turbine/pump operation mode switch-over was analyzed. Grid-side fault behavior is also addressed in terms of PHSP response.

Concerning SM capacitance dimensioning, simulation results show that, starting from stored energy requirement of rated-frequency MMC operating point, varying the DC link voltage, the converter can be operated over the entire frequency range, at rated machine torque, while keeping SM voltage deviations within the same design limits.

CM-voltage-free operation of the PHSP has been demonstrated on a reference design I-MMC, comprising HB-based INU and FB-based AFE, allowing for unrestricted grid-side operation, while varying the DC link voltage in the range of zero-to-rated, according to the machine operating point. While the presented topology complies with the grid-code requirements and enables machine-friendly operation, it is clear that the FB-based AFE offers wider operating range than required.

In the following two chapters, an I-MMC solution with a mix of FB and HB SMs in each branch of the AFE stage is introduced and analyzed. Such a mixed-SM AFE stage is named H-MMC. The aim of H-MMC utilization if the reduction of FB SM share in the AFE stage and, consequently, introduction of cheaper and more efficient PHSP-oriented I-MMC solution compared to the above presented reference design.

Firstly, a grid-code-compliant H-MMC control- and design method is presented, with reduced, albeit non-zero, CM-voltage stress to the machine. Secondly, a CM-voltage-free control- and design method is introduced, with a design-selectable trade-off between FB SM share and attainable power factor range at the grid-side. Both of the solutions will be compared to the reference design presented in this chapter in terms of trade-offs on the grid- and the machine-side.

5

Hybrid MMC With Reduced CM-Voltage-Stress for PHSP Retrofit

This chapter presents a novel control- and design method for PHSP-oriented I-MMC. The converter is based on H-MMC grid-side stage, having a mix of FB and HB SMs in the branches, and a HB-based machine-side stage. In contrast to the all-HB converter presented in ***Chap. 3****, the proposed solution offers reduced CM voltage stress on the machine. Compared to the CM-voltage-free I-MMC design presented in* ***Chap. 4****, based on FB grid-side MMC and a HB machine-side stage, the introduced H-MMC design offers reduced FB SM share in the grid-side stage. At the same time, grid-code compatibility has been maintained. A design trade-off between CM voltage reduction and FB SM share has been analyzed and presented in details.*

5.1 Reduced DC link voltage operation

Research community has recognized the potential of variable DC link voltage operation of I-MMC, as machine-friendly CM-voltage-free operation can be performed by varying the intermediate DC link voltage with output machine frequency, in the range $(0, V_{\mathrm{DC,n}}]$, where $V_{\mathrm{DC,n}}$ denotes the rated DC link voltage. Variable DC link voltage operation of the I-MMC has been analyzed in **Chap. 4** as an alternative to the CM voltage injection method. The efficient all-HB I-MMC, however, can only operate in a narrow band around $V_{\mathrm{DC,n}}$, due to fixed AC-side grid voltage amplitude, as presented in **Chap. 3**. The use of all-FB grid-side MMC stage, able to generate full range of DC voltage from positive- to negative rated value, is thus discussed in **Chap. 4**, following [39], as the most extreme alternative in terms of additional power losses and cost.

Alternative methods for reduced DC link voltage operation are proposed in the literature. In [64], a switch is introduced to the DC link, and constant voltage of an ideal DC source which could be replaced by HB-based MMC, is chopped to achieve appropriate average V_{DC}. The entire converter reliability, however, relies on the newly introduced switch, thus redundancy is compromised. A two-quadrant solution is proposed in [65], utilizing cascaded H-bridge as the grid-side stage. Such a solution is clearly not a candidate for four-quadrant-operation requirement of a PHSP.

For the inherent MMC redundancy and scalability to be preserved, a method of reduced DC link voltage operation not reliant on either additional DC link devices [64] or less-scalable AFE topology [65] should be foreseen. A conventional MMC AFE based on FB SMs has been shown to be an over-engineered solution for this application, as it enables $[-V_{\mathrm{DC,n}}, V_{\mathrm{DC,n}}]$ DC voltage operating range, where only positive half of this domain is required by the PHSP control method presented in **Chap. 4**.

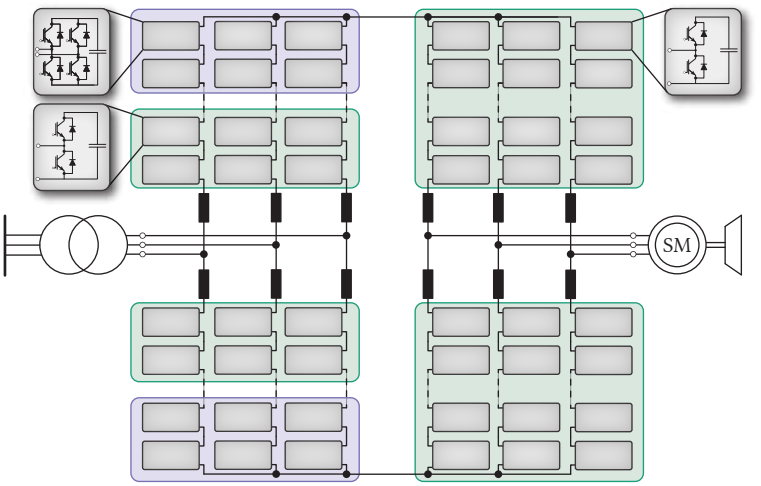


Fig. 5.1 H-MMC topology, presented as grid-side stage of an I-MMC solution to retrofit of an existing PHSP with H-MMC for conversion to VS operation, without machine modifications. Machine-side MMC is a standard HB SM based unit, as presented in **Chap. 3**, while grid-side stage is a H-MMC based on mix of FB and HB SMs; its design and operating principles are presented in this chapter.

Starting from an all-FB AFE stage, replacement of a fraction of FB SMs in each branch by the HB units yields reduced overall converter losses and cost, but also to a certain reduction in attainable operating area. This type of converter, named H-MMC, is discussed in this and the following chapter.

Reduced DC link voltage operation of H-MMC has been well studied in high-voltage DC applications, where boosted AC-side modulation index, which to good extent may be equalized with reduced DC voltage operation, is considered. Likewise, DC fault handling and DC link voltage reduction under certain operating conditions attract significant researchers' interest in the domain of DC power distribution networks. Design of an H-MMC enabling both reduction of DC link voltage down to zero and DC fault handling capability, comprising 2/3 of FB SMs per branch, has been presented in [66], along with a control approach relying on a capacitor sorting algorithm. Starting from operation at rated DC voltage and unity modulation index, the converter can be operated at unity power factor down to $0.5V_{\mathrm{DC,n}}$, while further voltage reduction requires a linear decrease of power factor down to zero. A thorough high-voltage-DC-optimized design approach has been carried out in [67]. The proposed method also relies on capacitor sorting algorithm, and offers reduction of DC link voltage down to $0.5V_{\mathrm{DC,n}}$ at theoretical FB/HB SM ratio of 1/4. However, further reduction down to zero, discussed for unity power factor, requires approximately 80% of installed SMs being FB. While also offering negative DC voltage operation, this feature is not of interest in MMC VSD applications. Variable DC link voltage operation of H-MMC fed from a line-commutated converter is assessed in [68], for DC link power flow control. SM energy balancing is performed through modified sorting algorithm, where FB SM voltage measurements are added a calculated offset to alter insertion preference and ensure energy balance. Operation down to $0.4V_{\mathrm{DC,n}}$ at unity power factor is achieved, with 50 % FB SM share, and without additional circulating current injection. Further control actions to achieve down-to-zero DC link voltage range have not been addressed. Starting from H-MMC with FB/HB ratio of 2/3, with branches SMs charged to a total of $1.5V_{\mathrm{DC,n}}$ each, and operating at boosted AC modulation index, an energy balancing method based on additional fundamental frequency reactive circulating current injection is introduced in [69], [70]. Capacitor

voltage balancing at boosted modulation index has been assessed in [71] utilizing a coupling of additional second-order SM-level voltage component and second-order circulating current for energy transfer. Influence of modulation index, power factor and FB/HB ratio on converter operation have been addressed. H-MMC balancing at reduced DC link voltage operation has been performed utilizing additional second-order circulating current injection in [72]. Additional current component ensures bipolar branch current in all operating areas and, in turn, proper balancing of HB even at reduced DC link voltage and high power factor values. Asymmetric H-MMC for variable DC link voltage operation has been presented in [73] for high-voltage DC power flow control. However, no details on capacitor voltage balancing at unequal upper- and lower-branch inserted DC voltage component were provided. H-MMC operation at boosted AC modulation index has as well been studied for medium-voltage DC applications. In such domain, due to lower SM-count and inadequacy of nearest-level modulation typically found in high-voltage DC [46], a form of Phase-Shifted Carrier (PSC) modulation with reference modification has been proposed in [47], along with an additional capacitor sorting algorithm.

Operation at variable DC link voltage has also been studied specifically with VSD application in mind. An extreme case utilizing a FB MMC as AFE, introduced as a reference scenario in **Chap. 4** is presented in [39],[40], enabling $[-V_{\mathrm{DC,n}}, V_{\mathrm{DC,n}}]$ operating range while doubling AFE stage losses. In [64], constant DC voltage is chopped by a DC link switch, to achieve desired average V_{DC}, while in [74] further SM capacitance reduction through decreased SM average voltage operation has been studied. As converter operation relies on the newly introduced switch, high reliability based on MMC redundancy is compromised. H-MMC AFE with all-FB upper branches and all-HB lower branches is presented in [41], demonstrating DC link voltage reduction down to practically zero. Non-equal insertion voltage references of FB- and HB-based branches call for non-equal AC current component share among the branches, where at certain operating frequencies, sum of AC current component in branches is a couple of times higher than the grid (output) current. At unity power factor there is little current overload in certain operating points, due to grid current being proportional to machine frequency. However, provision of reactive energy at lower-than-rated machine frequency, e.g. at 80% as a possible lower range for PHSP operation, would drive some of the converter SMs into a more prominent over-current state.

This chapter focuses on the design and control of H-MMC-based AFE for variable DC link voltage operation. AFE stage comprises branches with a mix of HB and FB SMs, grouped into Submodule Clusters (SMCs) (see **Fig. 5.1**). The control method proposed in this chapter enables CM voltage stress reduction, while allowing for an arbitrary grid-side power factor, including unity, over the entire designed DC operating voltage range, at equal loading of upper- and lower converter branches. A design method for optimal FB to HB SM ratio selection for the desired DC voltage operating range is derived. The next chapter will present an alternative control method, and an appropriate design method, for CM-voltage-free machine operation, with a design trade-off in grid-code compatibility at lower machine frequencies.

5.1.1 Partial DC link voltage reduction

Chap. 4 has introduced CM-voltage-free operation of PHSP assuming zero-to-rated DC link voltage reduction capability. Even at partial reduction of DC link voltage, advantages can be obtained, either in conjunction with CM voltage LF operation strategy [31], or through reduction of SM reference voltage level that allows for higher SM voltage oscillation margin [75]. Partially reduced DC link

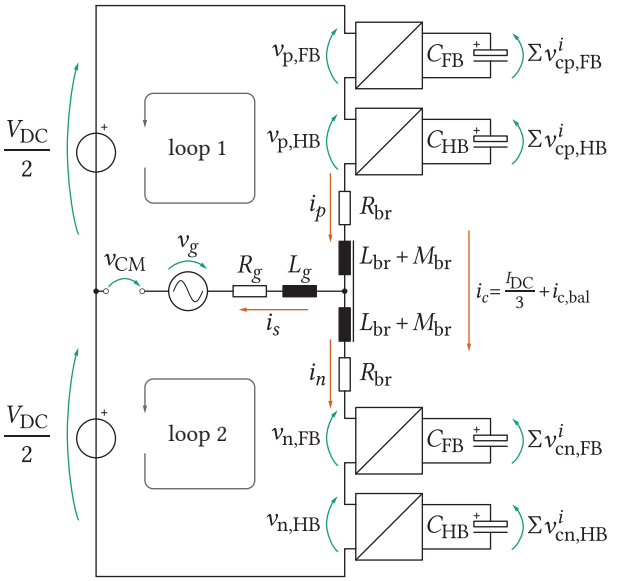


Fig. 5.2 Equivalent circuit of one phase of a hybrid MMC, where all the SMs are presented as two units, being equivalent to the SMCs of FB and HB SM installed. The following notation is applied: C_{FB}, C_{HB} – equivalent capacitance, $\Sigma v^i_{c\{p,n\},FB}$, $\Sigma v^i_{c\{p,n\},HB}$ – total voltage of the corresponding SMC, $v_{\{p,n\},FB}$, $v_{\{p,n\},HB}$ – total inserted voltage of the corresponding SMC.

voltage leads to lower required machine-side CM voltage amplitude for energy oscillation suppression, without further increase in LF circulating current amplitude. Thereby, CM voltage amplitude is kept below (existing) machine limitations. In case only partial reduction of DC link voltage is sufficient, which can be achieved replacing a fraction of AFE MMC's HB SMs with FB units, this is an attractive field to consider as a compromise between PHSP I-MMC-based VSD with all-FB and all-HB AFE.

5.2 H-MMC equivalent circuit and energy dynamics

Following **Fig. 5.1**, all the SMs of H-MMC branch can be presented as two equivalent SMCs, corresponding to N_{FB} and N_{HB} individual SMs, as in **Fig. 5.2**. At the moment, the actual number of FB and HB SMs is irrelevant, and will be discussed later. If the full potential of FB units is used for negative voltage insertion, reference waveforms of the FB (5.1) and the HB (5.2) SMCs are derived from (4.2), assuming $\theta_s = 0$. While the analysis is performed for the grid-side stage, subscript *grid* has been omitted for easier readability.

$$v^*_{\{p,n\},FB} = \mp \frac{m_s V_{DC,n}}{2}(1 - k_{DC})\cos(\omega_s t) \tag{5.1}$$

$$v^*_{\{p,n\},HB} = \mp \frac{m_s V_{DC,n}}{2} k_{DC}\cos(\omega_s t) + \frac{k_{DC} V_{DC,n}}{2} \tag{5.2}$$

Branch current can be written based on (3.1), assuming no balancing circulating currents.

$$i_{\{p,n\}} = \frac{I_{DC}}{3} \pm \frac{\hat{i}_s}{2}\cos(\omega_s t + \varphi_s) \tag{5.3}$$

Average FB (5.4) and HB (5.5) SMC energies within one branch reveal that, even though total branch energy averages to zero, i.e. $\overline{w}_{\{p,n\},FB} + \overline{w}_{\{p,n\},HB} = 0$, SMC energies are diverging (**Fig. 5.3**), as HB

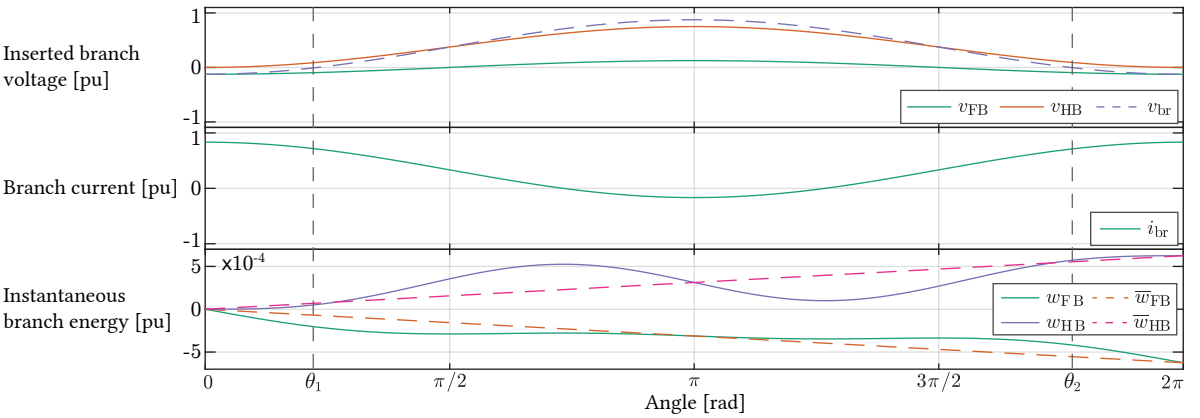


Fig. 5.3 Per unit branch-level waveforms over one fundamental cycle of H-MMC AFE stage, for the following parameters: $m_s = 1$, $\hat{i}_s = 1$, $\cos(\varphi_s) = 1$, $k_{DC} = 0.75$. From top to bottom: inserted branch voltage of FB-, HB-string, and total inserted voltage; branch current; instantaneous and average power of FB and HB strings, instantaneous and average energy of FB and HB strings. Angles θ_1 and θ_2 denote zero-crossing of inserted branch voltage.

SMC has positive bias in exchange with DC link, while FB SMC only exchanges energy with AC terminals. Note that DC current amplitude is presented as a function of AC-side current, derived from the AC and DC active power equality requirement (3.10). Thus, insertion references modification is necessary to ensure zero-average energy of individual SMCs.

$$\overline{w}_{\{p,n\},FB} = \underbrace{-\frac{m_s V_{DC,n} \hat{i}_s \cos(\varphi_s)}{8}(1 - k_{DC})t}_{\overline{w}_{AC} \text{ non-zero average}} \tag{5.4}$$

$$\overline{w}_{\{p,n\},HB} = \underbrace{-\frac{m_s V_{DC,n} \hat{i}_s \cos(\varphi_s)}{8} k_{DC} t}_{\overline{w}_{AC} \text{ non-zero average}} + \underbrace{\frac{m_s V_{DC,n} \hat{i}_s \cos(\varphi_s)}{8} t}_{\overline{w}_{DC} \text{ non-zero average}} \tag{5.5}$$

It is evident that only FB SMs can be used to insert negative portion of the branch voltage during the corresponding part of the cycle, which can be defined as $\omega_s t \in [\theta_1, \theta_2]$ (see **Fig. 5.3**). The duration of branch-level negative voltage insertion requirement can be determined from zero-crossing of (4.2), as an interval $\theta \in (\theta_2, \theta_1)$, $\theta_{\{1,2\}} = \pm(\arccos(k_{DC}/m_s) - \theta_s)$.

Once the branch-level inserted voltage reference is positive, i.e. in $\theta \in (\theta_1, \theta_2)$ interval, insertion references of FB (5.1) and HB (5.2) SMCs can be altered, to achieve zero-average power and energy, consequently equal loading of the two SMCs over the fundamental period.

$$\overline{w}_{\{p,n\},FB} = \overline{w}_{\{p,n\},HB} = 0 \tag{5.6}$$

As the zero-crossing instants of the inserted branch-level voltage (4.2) differ when varying either k_{DC} or m_s, FB SM insertion reference alteration can as well be performed at zero-crossing of AC component of (5.1) and (5.2), which is always equal to $\theta_{\{1,2\}} = \{\pi/2 - \theta_s, 3\pi/2 - \theta_s\}$. Branch-level insertion voltage is always positive for the given range, thus insertion references can be altered in a way presented in **Fig. 5.4**. During negative AC-side voltage reference value, all the SMs of the FB SMC are inserting AC-only voltage (5.1), while all the SMs of the HB SMC are inserting AC voltage

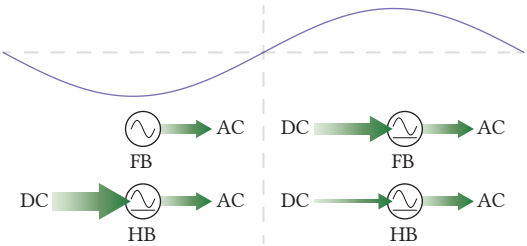


Fig. 5.4 Insertion strategy of the FB and HB SMs. During negative value of AC component of inserted branch voltage (left), FB SMC inserts AC-only voltage (5.1), while HB SMC inserts AC components with DC offset (5.2). Energy imbalance between SMCs is caused by non-equal energy share. During positive value of AC component of inserted branch voltage (right), FB SMC is inserting AC voltage with DC offset. In this way, FB SMs are charged from DC side to compensate for the unequal loading. HB SMC DC voltage insertion component is proportionally reduced.

Tab. 5.1 Average energy exchange share between FB and HB SMC of one converter branch, over the negative AC voltage half-cycle, for insertion references (5.1) and (5.2).

Terminals	HB SMC	FB SMC
AC	k_{DC}	$1-k_{\mathrm{DC}}$
DC	1	0

with DC offset (5.2). During this half-period, FB SMC only exchanges energy with AC-side, thus SMs are discharged, while HB SMC exchanges a portion of AC-side energy and all DC-side energy, causing corresponding SMs to charge. Once the branch-level AC voltage component is positive, FB SMC insertion reference must be added a certain DC component, such that energy can be exchanged with DC link as well, and satisfy (5.6).

Starting from (5.4) and (5.5), keeping in mind that voltage insertion reference is to be altered once per half-cycle, it is straightforward to derive required SMCs' inserted DC voltage component reference modification. Energy exchange share over the negative AC voltage half-cycle is given in **Tab. 5.1**.

Each SMC must exchange equal energy with DC and AC terminals to ensure equilibrium. The required FB and HB average energy over the positive AC voltage half-cycle is defined by the DC voltage insertion compensation factors, k_{cFB} and k_{cHB} (5.7), where $T_{\mathrm{fund}} = 2\pi/\omega_s$.

$$\frac{k_{\mathrm{DC}}}{1-k_{\mathrm{DC}}} = \frac{k_{\mathrm{DC}}+k_{\mathrm{cHB}}}{0+k_{\mathrm{cFB}}} \cdot \frac{T_{\mathrm{fund}}}{2} \tag{5.7}$$

Compensation factors are chosen to not alter the total inserted DC voltage amplitude, $k_{\mathrm{DC}} = k_{\mathrm{cHB}} + k_{\mathrm{cFB}}$.

$$k_{\mathrm{cHB}} = k_{\mathrm{DC}}(2k_{\mathrm{DC}}-1) \tag{5.8}$$

$$k_{\mathrm{cFB}} = 2k_{\mathrm{DC}}(1-k_{\mathrm{DC}}) \tag{5.9}$$

Positive AC voltage half-cycle SMC references are obtained.

$$v^*_{\{\mathrm{p,n}\},\mathrm{FB,pos}} = \mp\frac{m_s V_{\mathrm{DC,n}}}{2}(1-k_{\mathrm{DC}})\cos(\omega_s t) + V_{\mathrm{DC,n}}k_{\mathrm{DC}}(1-k_{\mathrm{DC}}) \tag{5.10}$$

$$v^*_{\{\mathrm{p,n}\},\mathrm{HB,pos}} = \mp\frac{m_s V_{\mathrm{DC,n}}}{2}k_{\mathrm{DC}}\cos(\omega_s t) + \frac{V_{\mathrm{DC,n}}}{2}k_{\mathrm{DC}}(2k_{\mathrm{DC}}-1) \tag{5.11}$$

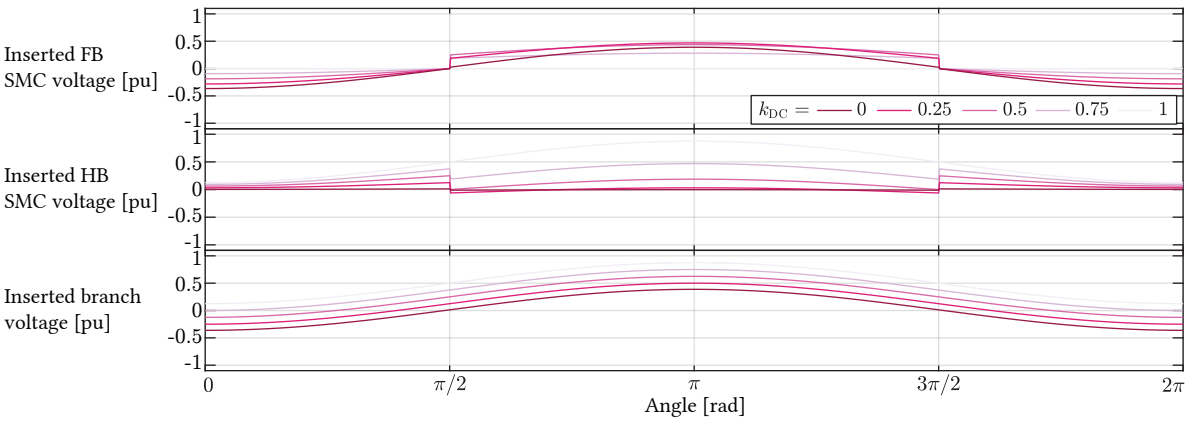


Fig. 5.5 Modified insertion references for FB and HB SMCs, compensating for discrepancies in constant power delivered from the two SMCs of a branch.

Due to HB SMs being limited to positive insertion voltage operation, presented compensation method is applicable to the DC link voltage reduction range of (5.12), as illustrated in **Fig. 5.5**.

$$V_{DC} \in [k_{DC,min}, 1] V_{DC,n} \tag{5.12}$$

$$k_{DC,min} = 1/2 \tag{5.13}$$

Average SMC energies are integrated starting from (5.3), (5.10) and (5.11).

$$\overline{w}_{\{p,n\},FB,pos} = \underbrace{\frac{m_s V_{DC,n} \hat{i}_s \cos(\varphi_s)}{4}(1-k_{DC})t}_{\overline{w}_{DC}\text{ non-zero average}} - \underbrace{\frac{m_s V_{DC,n} \hat{i}_s \cos(\varphi_s)}{8}(1-k_{DC})t}_{\overline{w}_{AC}\text{ non-zero average}} \tag{5.14}$$

$$\overline{w}_{\{p,n\},HB,pos} = \underbrace{\frac{m_s V_{DC,n} \hat{i}_s \cos(\varphi_s)}{8}(2k_{DC}-1)t}_{\overline{w}_{DC}\text{ non-zero average}} - \underbrace{\frac{m_s V_{DC,n} \hat{i}_s \cos(\varphi_s)}{8}k_{DC}t}_{\overline{w}_{AC}\text{ non-zero average}} \tag{5.15}$$

Energy imbalance of the FB and HB SMCs over one fundamental cycle is further obtained (5.16) and (5.17).

$$\Delta w_{FB,cycle} = \int_{-\pi/2}^{\pi/2} p_{\{p,n\},FB,neg}\, dt + \int_{\pi/2}^{3\pi/2} p_{\{p,n\},FB,pos}\, dt = -\frac{V_{dc,n} \hat{i}_s \cos(\varphi_s)}{\omega_s} k_{DC}(1-k_{DC}) \tag{5.16}$$

$$\Delta w_{HB,cycle} = \int_{-\pi/2}^{\pi/2} p_{\{p,n\},HB,neg}\, dt + \int_{\pi/2}^{3\pi/2} p_{\{p,n\},HB,pos}\, dt = \frac{V_{dc,n} \hat{i}_s \cos(\varphi_s)}{\omega_s} k_{DC}(1-k_{DC}) \tag{5.17}$$

$$\Delta w_{br,cycle} = \Delta w_{FB,cycle} + \Delta w_{HB,cycle} = 0 \tag{5.18}$$

Even though non-oscillatory instantaneous power components of the negative AC voltage half-cycle have been identified and compensated for in the positive AC voltage half-cycle (**Fig. 5.5**), the fact that oscillatory members of instantaneous power equations are now also being altered twice per cycle results in non-zero-average energy originating from such oscillatory components. Following (5.16) and (5.17), additional active power of exchange between FB and HB SMCs must equal (5.19) over the

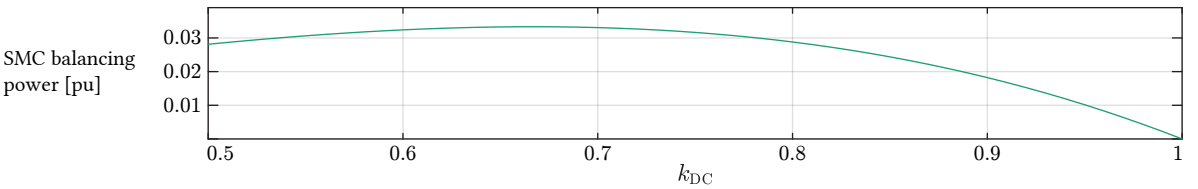


Fig. 5.6 SMC balancing power amplitude requirement over the operating range of variable DC link voltage. If the converter supplies constant-torque machine, i.e. active power is proportional to angular frequency, maximal value is seen at $k_{DC} = 2/3$ (5.19).

fundamental period. In constant-torque VSD application, active power is proportional to machine angular frequency. At unity grid-side power factor, grid current amplitude, $\hat{i}_s$, is proportional to k_{DC}, thus maximal SMC balancing power value is seen at $k_{DC} = 2/3$.

$$P_{\Delta SMC} = \frac{V_{DC,n}\hat{i}_s \cos(\varphi_s)}{2\pi} k_{DC}(1 - k_{DC}) \tag{5.19}$$

The power amplitude requirement of newly introduced balancing component (5.19) is presented over the operating range (5.12) in **Fig. 5.6**, for $m_s = 1$.

5.3 H-MMC energy balancing

The concept adopted is to preserve internal control of a conventional MMC presented in **Chap. 2**, i.e. horizontal, vertical and total energy control, while adding a control layer to balance FB and HB SMCs at the branch level.

5.3.1 Branch-level energy balancing

From the branch-level up, H-MMC topology control is identical to conventional MMC, as presented in **Chap. 2** and highlighted in green on **Fig. 5.7**. Higher-level control comprises active (P^*_{AC}) and reactive (Q^*) power reference tracking, followed by reference scaling with respect to converter current capacity and grid-code-imposed requirements. AC-side voltage references are generated by phase-locked loop-enabled grid current control.

Horizontal, vertical and total energy balancing is performed as derived in **Chap. 2**. Horizontal and vertical balancing actions are purely internal to the MMC. Current references are passed to CCC, and the action is not visible from either AC or DC terminals. Total energy controller has a different role for rectifier and inverter operation. In the first case, grid-side power reference is generated (P^*_{DCV}) to match DC-side power demand, keeping the total converter state-of-charge constant. In the second case, DC link current is controller to supply AC-side reference power of the converter.

5.3.2 Inter-SMC energy balancing

Within converter branches, an additional control layer is required to compensate for unequal DC-side energy exchange of the SMCs (5.19), highlighted in violet in **Fig. 5.7**. To establish active power transfer between FB and HB SMCs within the same converter branch, without altering AC and DC terminal values of the converter, additional circulating current and voltage components are used, ensuring these will only produce non-zero-average active power transfer between themselves. Such

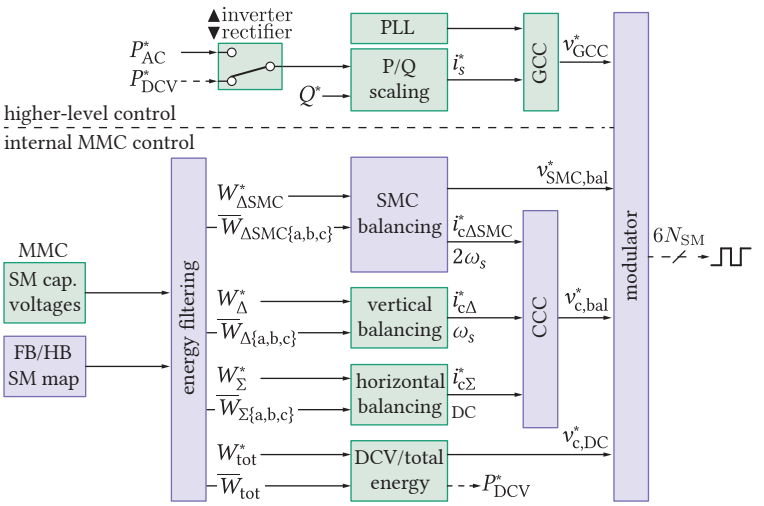


Fig. 5.7 H-MMC control outline is presented. Starting from standard MMC control (green), SMC balancing layer is added to the internal control. A FB/HB SM map is required for proper SMC energy measurement and control. Modulator is presented in more details in **Fig. 5.10**. Upper-level control is unaffected, comprising grid-code-compliant scaling of active (P) and reactive (Q) power references, followed by grid current controller (GCC), synchronized to the grid through phase-locked loop (PLL).

components must not interfere with DC and fundamental frequency AC components, thus multiples of two of fundamental frequency can be considered. AC circulating current at $2\omega_s$ is employed (5.20), along with additional FB and HB SMC voltage references at $2\omega_s$ (5.21).

$$i_{c\Delta SMC} = \hat{i}_{c\Delta SMC} \cos(2\omega_s t) \tag{5.20}$$

$$v^*_{SMC,bal,\{FB,HB\}} = \pm\hat{v}_{SMC,bal} \cos(2\omega_s t) \tag{5.21}$$

To satisfy zero-sum current at DC terminals, a symmetrical three-phase system is introduced, satisfying (5.22).

$$\sum \vec{i}_{c2\omega\{a,b,c\}} = 0 \tag{5.22}$$

This current component flows through both upper and lower branch of a phase leg, interacting with AC and DC components of the inserted FB and HB SMCs.

- **Interaction with DC voltage components** introduces zero-average oscillating power at $2\omega_s$.
- **Interaction with AC voltage components** at ω_s introduces zero-average oscillating power components at ω_s and $3\omega_s$, as AC voltage insertion reference is kept unchanged over the fundamental cycle (5.1),(5.2),(5.10),(5.11).
- **Interaction with balancing AC voltage component** at $2\omega_s$ introduces non-zero-average active power and a zero-average oscillating component at $4\omega_s$.

Due to opposing phase of (5.21), exchange of energy between the SMCs of the same branch is compensating the energy imbalance over the fundamental cycle (5.16) and (5.17).

As the number of SMs within FB and HB SMCs can be non-equal, SMC differential energy reference is defined by the FB to HB ratio (5.23). Note that differential energy reference (5.23) shall be multiplied

by two in the corresponding controller, as phase-leg-level circulating current controls SMC energy balancing in both upper and lower branch.

$$W^*_{\Delta\mathrm{SMC}} = \frac{1}{2}\left(\frac{(\Sigma V_{\mathrm{SM,HB}})^2}{N_{\mathrm{HB}}} - \frac{(\Sigma V_{\mathrm{SM,FB}})^2}{N_{\mathrm{FB}}}\right) C_{\mathrm{SM}} = \frac{C_{\mathrm{SM}} V^*_{\mathrm{SM}}}{2}(N_{\mathrm{HB}} - N_{\mathrm{FB}}) \tag{5.23}$$

Compared to the phase-leg-level vertical balancing, SMC energy balancing shares the same control approach, however on a branch-level. Thus, the same control structure can be used [44], as implemented in **Sec. 2.3.4**. Firstly, balancing current components are calculated per-phase. Further, for each phase current component, reactive components are injected into the remaining two phases, to satisfy (5.22).

As in the other energy balancing actions, SMC controller feedback is a filtered-out differential energy, determined from capacitor voltage measurements based on (5.23). Thus, SM mapping, i.e. disposition of FB and HB SMs within a branch is fed to the energy controller (**Fig. 5.7**).

5.4 H-MMC design

With the control concept defined, the first step in H-MMC design assumes deciding on minimal required DC link voltage, i.e. selecting $k_{\mathrm{DC,min}}$ from the available range (5.13). This determines the amplitude of negative insertion voltage needed for an ideally balanced converter (5.1), which still does not lead to the correct selection of FB/HB SM ratio. As presented in **Sec. 5.3**, additional SMC balancing voltage and current requirements must be taken into account, which affect the insertion voltage amplitude requirement of FB and HB SMCs. Relying on these results, and adding energy balancing requirements of a uniform-SM MMC, insertion voltage budget has been calculated for each of the control loops. As a design example, values corresponding to the medium-voltage MMC unit introduced in **Tab. 2.2** are used. **Tab. 5.2** provides absolute and per unit values for easier analysis, with converter line voltage and three-phase apparent power chosen as base units. These ratings are used in test scenarios later on. Please note that, since inductance and capacitance represent frequency-dependent impedances, these are given for fundamental 50 Hz frequency in per unit system. Scaling to another frequency, e.g. for second harmonic impedance, is straightforward.

Tab. 5.2 H-MMC parameters used in the test scenarios, given in both absolute and per unit values, with line voltage and three-phase apparent power being base values.

Line voltage	U_n =6 kV	1 pu
Apparent power	S_n =500 kVA	1 pu
Grid frequency	f_g =50 Hz	-
Number of SMs per branch	N_{SM} = 16	-
SM voltage	V_{SM} =650 V	0.108 pu
SM capacitance (tol. ±10%)	C_{SM} =2.25 mF	0.020 pu
Branch inductance	L_{br} =2.5 mH	0.011 pu
Branch inductance coupling coefficient	k_{br} = 0.3	-
Branch resistance	R_{br} =50 mΩ	7×10^{-4} pu
Switching frequency	f_{sw} =1 kHz	-

5.4.1 SMC insertion voltage waveform

The next step in converter design assumes defining FB and HB SMC insertion voltage waveforms. Insertion references are derived for the two AC-side voltage half cycles of **Fig. 5.4** – negative in (5.1) and (5.2) and positive in (5.10) and (5.11). A generalized expression over the fundamental cycle is given (5.24) and (5.25), expanding the above equations to comprise converter control voltage components: $\hat{v}_{\mathrm{c,bal}}$ – circulating current control, $\hat{v}_{\mathrm{c,bal},2\omega_s}$ – SMC-balancing current control, $\hat{v}_{\mathrm{c,bal,SMC}}$ – SMC-balancing voltage component.

$$v^*_{\{\mathrm{p,n}\},\mathrm{FB,cycle}} = \mp\frac{m_s V_{\mathrm{DC,n}}}{2}(1-k_{\mathrm{DC}})\cos(\omega_s t)+\frac{N_{\mathrm{FB}}}{N_{\mathrm{SM}}}\left[\hat{v}^*_{\mathrm{c,bal}}\cos(\omega_s t+\pi/2)+\hat{v}^*_{\mathrm{c,bal},2\omega_s}\cos(2\omega_s t+\pi/2)\right] + \hat{v}^*_{\mathrm{c,bal,SMC}}\cos(2\omega_s t)+\begin{cases}V_{\mathrm{DC,n}}k_{\mathrm{DC}}(1-k_{\mathrm{DC}})(v_s\le 0) & \{\mathrm{p,n}\}=\mathrm{p}\\ V_{\mathrm{DC,n}}k_{\mathrm{DC}}(1-k_{\mathrm{DC}})(v_s\ge 0) & \{\mathrm{p,n}\}=\mathrm{n}\end{cases} \quad (5.24)$$

$$v^*_{\{\mathrm{p,n}\},\mathrm{HB,cycle}} = \mp\frac{m_s V_{\mathrm{DC,n}}}{2}k_{\mathrm{DC}}\cos(\omega_s t)+\frac{N_{\mathrm{HB}}}{N_{\mathrm{SM}}}\left[\hat{v}^*_{\mathrm{c,bal}}\cos(\omega_s t+\pi/2)+\hat{v}^*_{\mathrm{c,bal},2\omega_s}\cos(2\omega_s t+\pi/2)\right] + \hat{v}^*_{\mathrm{c,bal,SMC}}\cos(2\omega_s t+\pi)+\begin{cases}(k_{\mathrm{DC}}V_{\mathrm{DC,n}}/2)\left[(v_s\ge 0)+(2k_{\mathrm{DC}}-1)(v_s\le 0)\right] & \{\mathrm{p,n}\}=\mathrm{p}\\ (k_{\mathrm{DC}}V_{\mathrm{DC,n}}/2)\left[(v_s\le 0)+(2k_{\mathrm{DC}}-1)(v_s\ge 0)\right] & \{\mathrm{p,n}\}=\mathrm{n}\end{cases} \quad (5.25)$$

Analogously to improvement in DC link utilization through injection of CM voltages to AC-side phase voltage waveforms, third harmonic of SMC balancing voltage is introduced. Waveforms (5.24) and (5.25) are graphically presented in **Fig. 5.8**, for required modulation index of $m_{\mathrm{s,req}} = 2\hat{v}_{\mathrm{ph}}/(1.15V_{\mathrm{DC,n}}) = 0.821$. Minimal voltage of HB SMCs over the cycle, for attainable DC voltage reduction factor range $k_{\mathrm{DC}} \in [0.5, 1]$ equals 0.029 pu, meaning the converter can be realized with selected design choices without violation of HB electrical limit.

5.4.2 Determination of the required FB/HB share

Due to higher device count and consequently higher losses of FB SMs compared to HB alternative, their number is selected as the minimal value that satisfies voltage insertion requirement (5.24). For the case of arbitrary k_{DC}, with CM voltage injection for both AC-side voltage and SMC balancing voltage, maximum FB SMC voltage requirement is obtained from (5.24) and **Fig. 5.8**. In the worst-case scenario of the minimal DC link voltage attainable by this method (5.13), maximal FB insertion voltage reference leads to FB SM count (5.26). The same can be determined for an arbitrary DC link voltage

Tab. 5.3 H-MMC FB SMs requirement for various degrees of DC link voltage reduction, and the number of required FB SMs for the exemplary design.

k_{DC}	1	0.95	0.9	0.85	0.8	0.75	0.7	0.65	0.6	0.55	0.5
$\max(\hat{v}_{\mathrm{ins,FB}})$ [pu]	0	0.196	0.32	0.434	0.537	0.63	0.711	0.782	0.843	0.893	0.933
$N_{\mathrm{FB,min}}$[%]	0.0%	11.3%	18.5%	25.1%	31.0%	36.3%	41.0%	45.1%	48.6%	51.5%	53.8%
N_{FB}	0	2	3	5	5	6	7	8	8	9	9

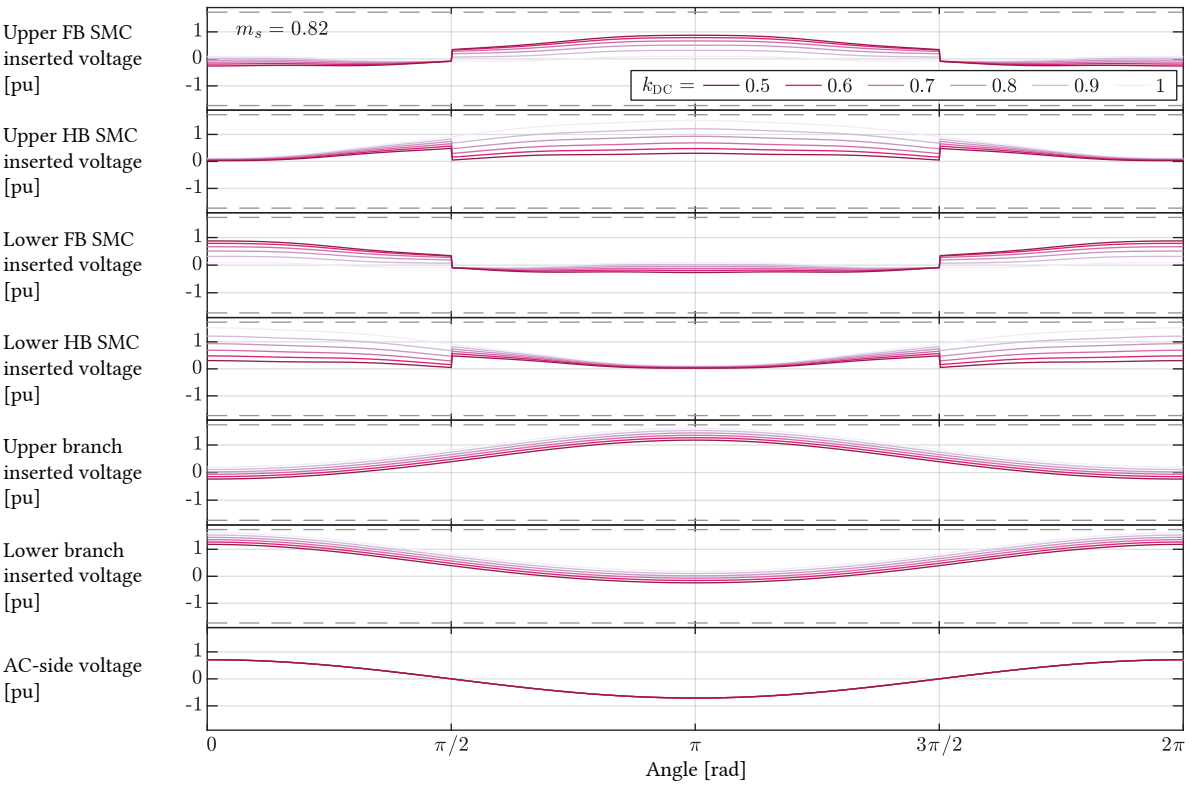


Fig. 5.8 Branch insertion indexes of phase a are presented, comprising all the voltage components (5.24) and (5.25), of the amplitudes calculated within the voltage budget section. Voltage budget utilization is improved through third harmonic injection for SMC balancing voltage, at $6\omega_s$. The minimal voltage of HB SMC reference equals 0.029 pu at $k_{DC} = 0.5$. Dashed lines represent available branch voltage.

reduction ratio, as in **Tab. 5.3**.

$$\max_{k_{DC}=0.5}\left(\hat{v}_{ins,FB,\{p,n\}}\right) = 0.878\,\text{pu} \longrightarrow N_{FB} = \left\lceil \frac{\max_{k_{DC}=0.5}\left(\hat{v}_{ins,FB,\{p,n\}}\right) V_b}{V_{SM}} \right\rceil = 9(56\,\%) \tag{5.26}$$

5.5 Virtual SM at variable DC voltage operation

A number of FB SMs $N_{FB,sel}$ selected for a certain $k_{DC,sel}$ will also enable operation at any higher DC link voltage value up to the rated, i.e. $k_{DC} \geq k_{DC,sel}$, through appropriate control actions.

5.5.1 Virtual SM concept

For converter operation at the lowest designed level of DC link voltage, e.g. $k_{DC,sel} = 0.5$, the required number of FB and HB SMs corresponds to the actual number of installed SMs, (5.26). PSC pulse-width modulation is implemented, thus SMs of individual SMCs are provided with a set of PSCs, as presented in the leftmost part of **Fig. 5.9**. As the operating point is shifted towards higher DC voltage values, $k_{DC} > k_{DC,sel}$, the minimal required share of FB SMs reduces (**Tab. 5.3**). For an example of $k_{DC} = 0.8$ (center part of **Fig. 5.9**), the minimal number of FB SMs are assigned (mapped) to FB SMC, and

quantified as N_{FBv}. The remaining number on installed FB units, $N_{\mathrm{FB}} - N_{\mathrm{FBv}}$, is mapped to the HB SMC, and operate as virtual HB SMs. The new number of SMs operating as HB thus increases to $N_{\mathrm{HBv}} = N_{\mathrm{SM}} - N_{\mathrm{FBv}}$. The corresponding PSCs are assigned to N_{FBv} and N_{HBv}, as in the middle section of **Fig. 5.9**. Further increase in DC voltage leads to the other extreme – for $k_{\mathrm{DC}} = 1$, all the FB SMs operate as virtual HB SMs, as in the rightmost section of **Fig. 5.9**.

5.5.2 H-MMC modulation

Modulation is performed as illustrated in **Fig. 5.10**. In case $N_{\mathrm{FB}} = N_{\mathrm{FBv}}$, insertion voltage references (5.24) and (5.25) are compared to the available voltages of FB and HB SMCs, thus insertion indexes are obtained, as presented in the leftmost part of **Fig. 5.10**. These are fed to two sets of PSCs, determined as in **Fig. 5.9**, to generate gate pulses for individual SMs of the SMCs. With further rise in DC voltage reference, e.g. $k_{\mathrm{DC}} = 0.8$, some FB SMs are assigned to HB SMC (**Fig. 5.9**, middle).

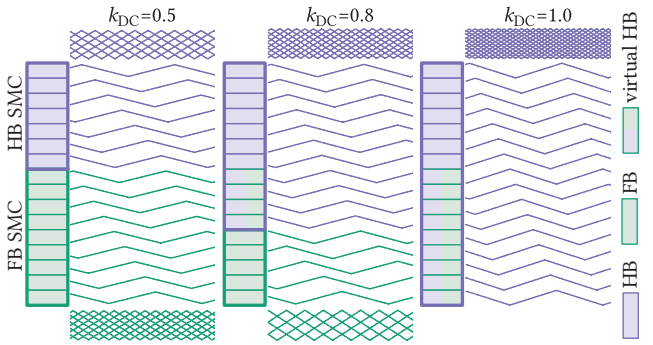


Fig. 5.9 PSC generation strategy is presented. The leftmost column presents operation at lowest k_{DC} value. Increasing DC link voltage value, a certain number of FB SMs must be operated as HB, denoted *virtual HB*, following **Tab. 5.3**. Note that actual switching frequency of unipolar-modulated FB operated with positive-only reference is 50 % lower compared to FB operation.

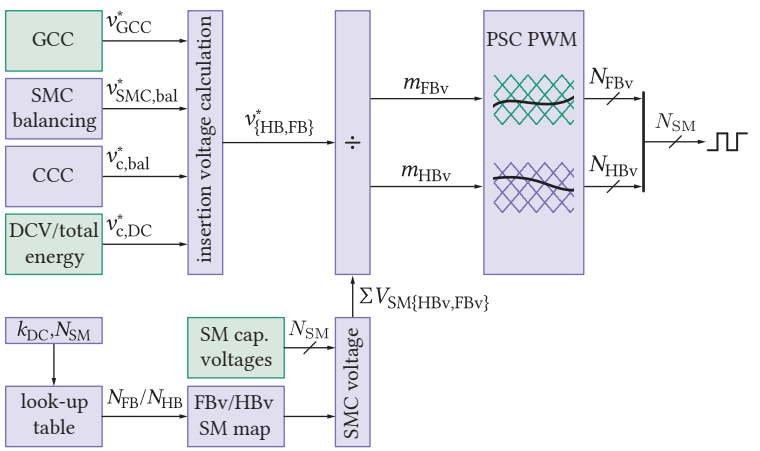


Fig. 5.10 Modulation scheme of H-MMC is presented, with conventional MMC control blocks in green and newly-introduced blocks in violet. Required FB/HB ratio for operating point (k_{DC}) and SM count (N_{SM}) is determined from the look-up **Tab. 5.3**. As k_{DC} rises, a part of FB SMs is being assigned to the HB SMC and operated as *virtual HB SMs*. The resulting SM mapping is used to correctly sum available SMC voltages, and calculate insertion indexes. Two sets of PSCs are generated, as illustrated in **Fig. 5.9**.

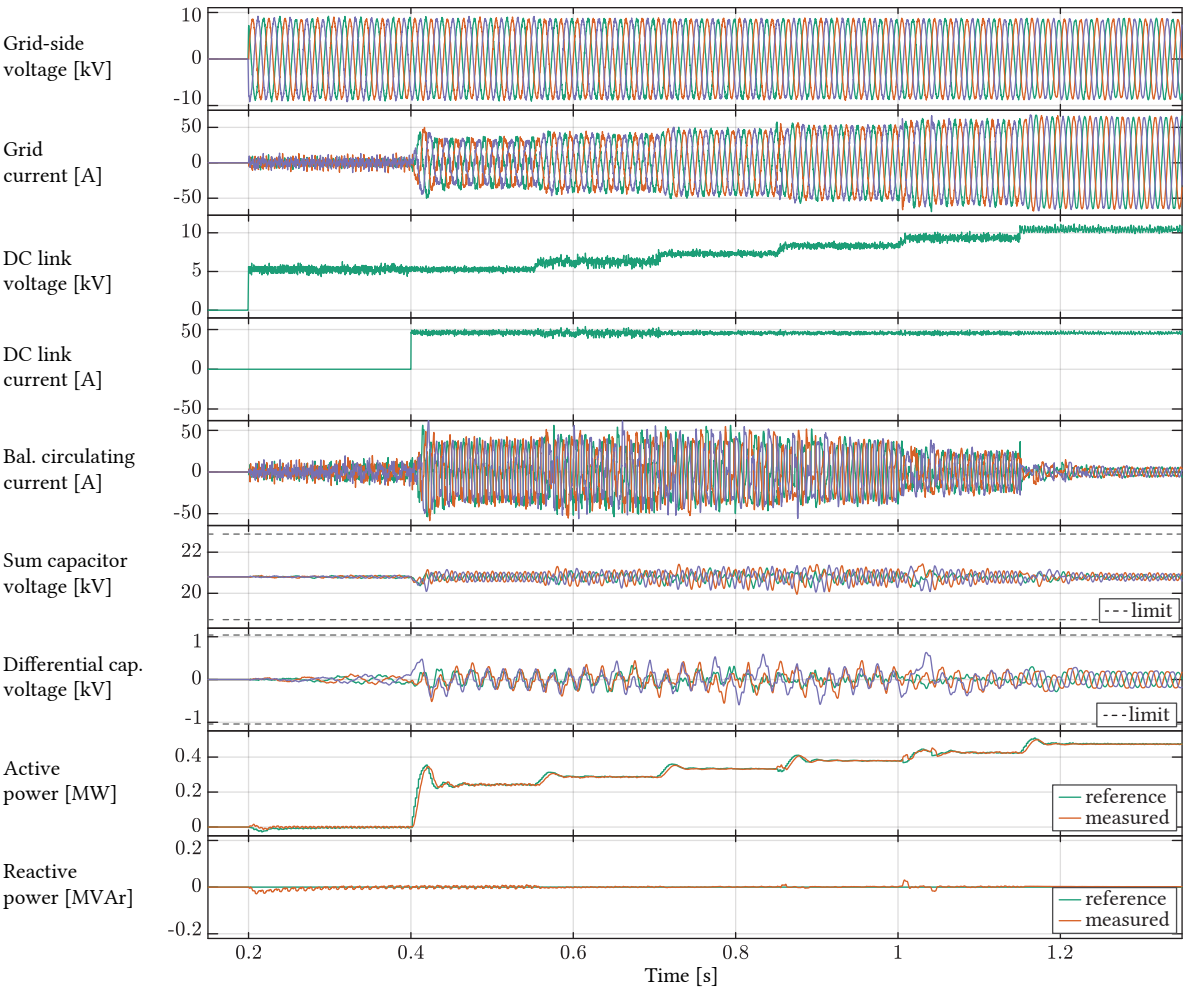


Fig. 5.11 H-MMC operation sequence at variable DC link voltage and rated DC link current operation over the complete operating range and unity power factor. Active and reactive power references are correctly tracked, while sum- and differential capacitor voltages ripple is driven well below marked 10 % limit.

Starting from the actual number of installed SMs, N_{FB} and N_{HB} and their disposition within the converter branches, all the SMs are reassigned to virtual N_{FBv} and N_{HBv} SMC strings and mapped to corresponding SMCs. Measured SM capacitor voltages are then added-up to determine available SMC voltages, denoted $\Sigma V_{\mathrm{SM}\{\mathrm{HBv,FBv}\}}$. Closed-loop control is performed, where insertion voltage references (5.24) and (5.25) are divided by available measured voltages, to generate modulation indexes for SMs of the two SMCs – m_{FBv} and m_{HBv}. Two sets of PSCs are used, assigned to individual SMs as in **Fig. 5.9**. Gate signals are fed to corresponding SMs using the determined FBv/HBv SM map. SMC energy balancing described in **Sec. 5.3.2** is now used with the FBv/HBv SM map of **Fig. 5.10**.

5.6 Test scenario and results

H-MMC-based AFE converter performance have been verified through high-fidelity switched-model simulations of the medium-voltage ratings converter (**Tab. 5.2**). Three test scenarios were observed – in the first and the second case, unity- and variable power factor operation of the AFE are observed,

respectively, at the rated DC current value being the worst-case. In the third scenario, constant-torque machine start-up sequence at variable DC link voltage has been tested, with H-MMC serving as AFE and a HB MMC acting as machine-side stage.

5.6.1 Unity power factor operation

The ability to operate the converter at unity power factor is demonstrated in test scenario of **Fig. 5.11**. DC link voltage reference is gradually increased from $k_{\mathrm{DC}} = 0.5$ in 0.1 steps up to the rated (unity) value. DC load is controlled to maintain the rated DC current value. Operating at unity power factor, active- and reactive (zero) power references are correctly tracked, while sum- and differential capacitor voltages are kept well below the acquired ±10 % limit.

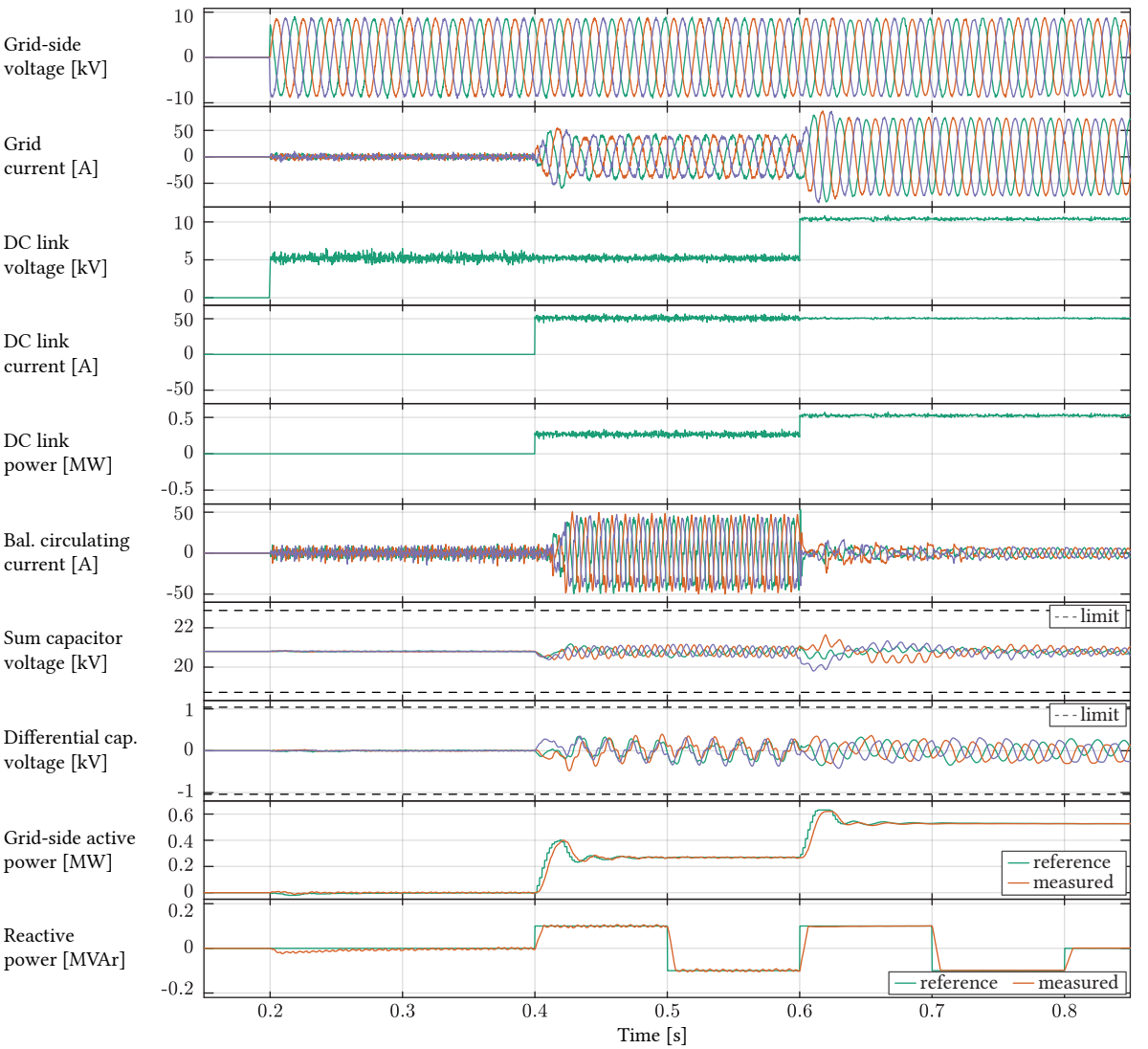


Fig. 5.12 H-MMC converter operation for two extreme DC link voltage setpoints, under varying power factor, is presented. Branch-level sum- and differential capacitor voltages are kept under balance, while active and reactive power references are correctly tracked. DC link current is kept at rated value throughout the test.

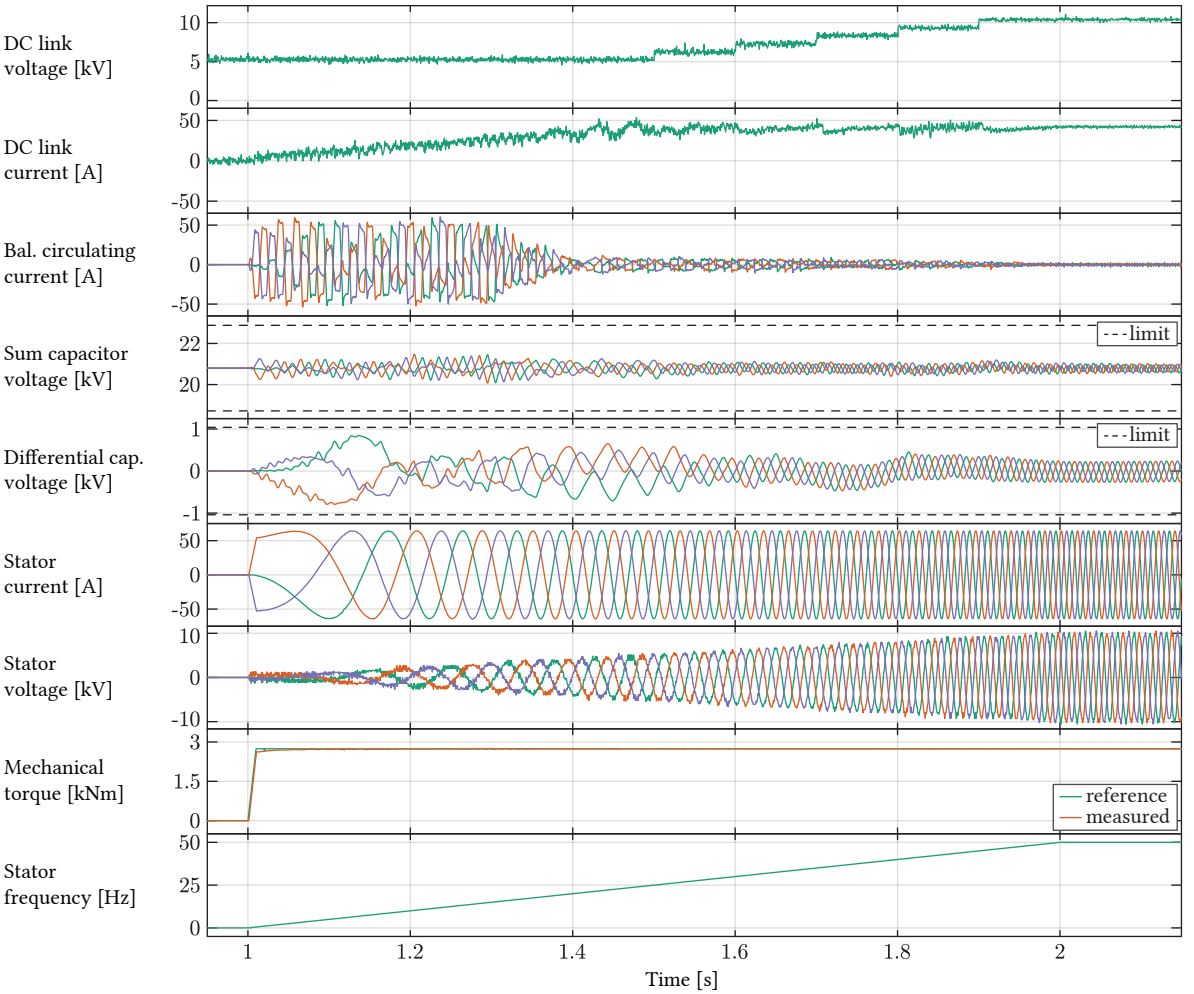


Fig. 5.13 Machine-side MMC operation during constant-torque machine start-up is presented. Below 50 % of rated frequency, DC link voltage is kept at the minimal value ($V_{\mathrm{DC,n}}/2$), resulting in 50 % lower CM voltage amplitude requirement for capacitor ripple limitation [30]. Further, above 50 % of rated frequency, DC voltage amplitude is incremented in proportion to output frequency, in steps of $0.1V_{\mathrm{DC,n}}$. In this way, SM capacitor ripple is kept well below the limits over the entire operating range.

5.6.2 Variable power factor operation

Converter operation is tested at variable reactive power demand, for two DC link voltage operating points – the lowest ($k_{\mathrm{DC}} = 0.5$) and the highest, i.e. rated value, as presented in **Fig. 5.12**. DC link current has been kept at the rated value throughout the test, while reactive power reference has been varied in $\pm 0.2 S_n$ range. Both active and reactive power references are tracked correctly by the AFE control, while sum- and differential branch-level capacitor voltages are kept below ±10 %.

5.6.3 Constant-torque machine start-up

While presented variable DC voltage H-MMC operation is clearly not limited to supplying VSDs, the thesis is focused on PHSP applications. Thus, the third test-scenario (**Fig. 5.13**) presents constant-torque machine start-up sequence of a 6 kV, 0.5 MVA synchronous unit, of the ratings given in **Tab. 3.2**.

Machine-side MMC is HB-based (**Fig. 5.1**, right), supplied from a H-MMC AFE stage. Following the machine-side MMC energy ripple expression (3.12), we can conclude that the energy oscillation of the dominant (first) term will be constant if ratio of DC link voltage to output frequency is constant. Thus, for this specific application, we will aim to maintain $k_{\mathrm{DC}}V_{\mathrm{DC,n}}/\omega_{\mathrm{sm}} = \mathrm{const}$, where w_{sm} denotes electrical angular frequency of the machine. As the presented H-MMC control method has a maximal DC link voltage range of $[0.5, 1]V_{\mathrm{DC,n}}$, DC voltage reference when supplying a machine is obtained:

$$V_{\mathrm{DC}} = \begin{cases} V_{\mathrm{DC,n}}/2 & |\omega_{\mathrm{sm}}| \in (0 \dots 0.5]\,\omega_{\mathrm{sm,rated}} \\ k_{\mathrm{DC}}V_{\mathrm{DC,n}} & |\omega_{\mathrm{sm}}| \in (0.5 \dots 1]\,\omega_{\mathrm{sm,rated}} \end{cases} \tag{5.27}$$

In the LF operating region, below half the rated speed, where $k_{\mathrm{DC}}V_{\mathrm{DC,n}}/\omega_{\mathrm{sm}} \neq \mathrm{const}$, capacitor voltage balancing is performed utilizing CM voltage and appropriate circulating current components as in [30]. Following (3.12) and aforementioned DC voltage limit, DC link voltage reference is kept at the lowest level up to 50 % of rated machine frequency. Further, it is set in proportion to the output frequency, in steps of $0.1V_{\mathrm{DC,n}}$. This strategy decreases CM voltage amplitude by 50 % in the lowest machine frequency region, compared to [30], keeping the same circulating balancing current amplitude limit and allowed capacitor voltage deviation. Being less severe load to the H-MMC compared to the **Sec. 5.6.1** scenario, only the machine-side MMC performance has been presented here.

5.6.4 Spectral analysis of the grid-side current

According to the recommended practice and requirements, published under [76], harmonic current distortion limits are defined in percent of the maximal-demand load current, while Total Harmonic Distortion (THD) is normally related to the ratio of all harmonics to the fundamental component of the observed operating point. Firstly, THD of the grid current for unity power factor test scenario, presented under **Sec. 5.6.1**, is calculated for each of the operating points.

Tab. 5.4 H-MMC grid current THD and TDD for various k_{DC} values at constant DC current. I_1 represents fundamental AC current component amplitude, which is used to calculate TDD at partial loads [76].

k_{DC}	0.5	0.6	0.7	0.8	0.9	1.0
I_1 [A]	37.0	43.2	50.3	57.4	64.3	71.6
$\mathrm{THD_i}$ [%]	11.8	7.0	4.5	3.9	5.1	1.7
$\mathrm{TDD_i}$ [%]	6.1	4.2	3.2	3.1	4.6	1.7

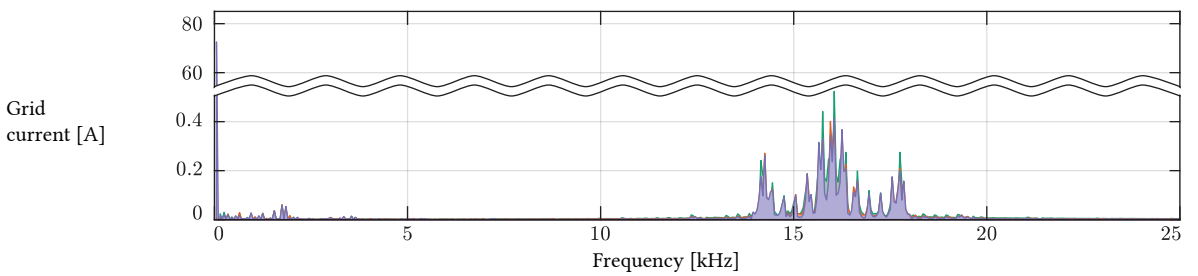


Fig. 5.14 Grid-current spectra for rated DC link voltage and rated load. Please note the y-axis is cut for easier readout of both sub-ampere harmonic components and the dominant fundamental 50 Hz component. Higher harmonic amplitudes are dominant around apparent switching frequency of $N_{\mathrm{SM}}f_{\mathrm{sw}} = 16\,\mathrm{kHz}$.

Further, Total Demand Distortion (TDD) is calculated by scaling the obtained partial load THD values to the rated value of fundamental grid current component, to comply with IEEE 519-2014 [77]. Maximal demand current rating was taken as the fundamental current component at the rated DC link voltage, $I_{1,\mathrm{n}} = 71.6\,\mathrm{A}$, following **Tab. 5.4**. TDD is calculated as $\mathrm{TDD_i} = \mathrm{THD_i} I_1 / I_{1,\mathrm{n}}$.

Both sets of values are presented in **Tab. 5.4**. While IEEE 519-2014 proposes TDD limit of 5 % for connection voltage up to 69 kV, the presented H-MMC approach surpasses this limit only at the lower end of the operating range ($k_{\mathrm{DC}} = 0.5$), having a maximal value of 6.1 %. Please note, however, that grid-code compatibility in terms of TDD was not of primary concern when choosing converter ratings. A slightly higher insertion voltage reserve would eliminate the risk of overmodulation that was observed at the lowest DC link operating voltage reference, leading to the observed TDD violation. Finally, a grid current spectrum has been presented at the rated operating DC voltage, in **Fig. 5.14**. Higher-order harmonics are present around the apparent switching frequency, i.e. $N_{\mathrm{SM}} f_{\mathrm{sw}} = 16\,\mathrm{kHz}$, while lower-order harmonics are of significantly lower amplitudes.

5.6.5 SMC energy control

SMC energy balancing controller action is presented in more details in **Fig. 5.15**, for test scenario of **Sec. 5.6.1**. Based on k_{DC} value, FB/HB ratio is determined from **Tab. 5.3**. Further, SMC balancing current limit is dynamically calculated and set, based on the required balancing power at the operating point (5.19) and applied SMC balancing voltage component $\hat{v}_{\mathrm{c,bal,SMC}}$ (5.24) and (5.25), as seen in the third subplot of **Fig. 5.15**. Differential SMC energy reference of (5.23) is correctly tracked in all the phase-legs, as presented on the lowermost graph.

Capacitor voltages of individual SMs grouped in FB and HB SMCs of upper and lower branch of a phase-leg, are presented in **Fig. 5.16**. Capacitance tolerance of ±10 % is introduced in the converter model. Results confirm correct SM-level capacitor voltage control, as all units converge to the reference value of 650 V, over all the values of k_{DC}, including transition between operating points.

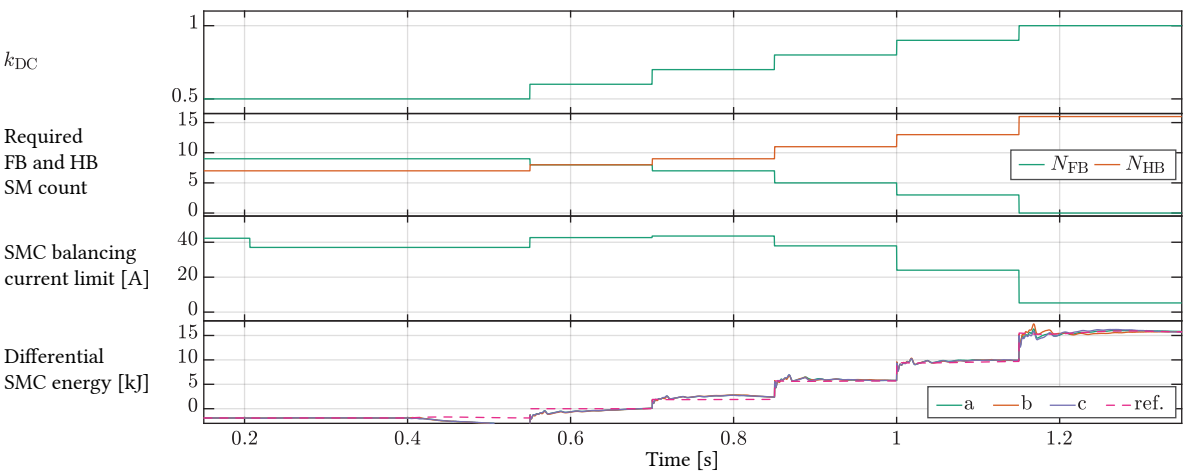


Fig. 5.15 SMC differential energy controller operation for test scenario of **Fig. 5.11**. For the instantaneous ratio of $N_{\mathrm{FB}}/N_{\mathrm{HB}}$ SMs, differential energy reference is calculated using (5.23). Control action is limited as a function of AC-side output current, at constant value of SMC balancing voltage (5.21). Differential SMC controller tracks the reference correctly.

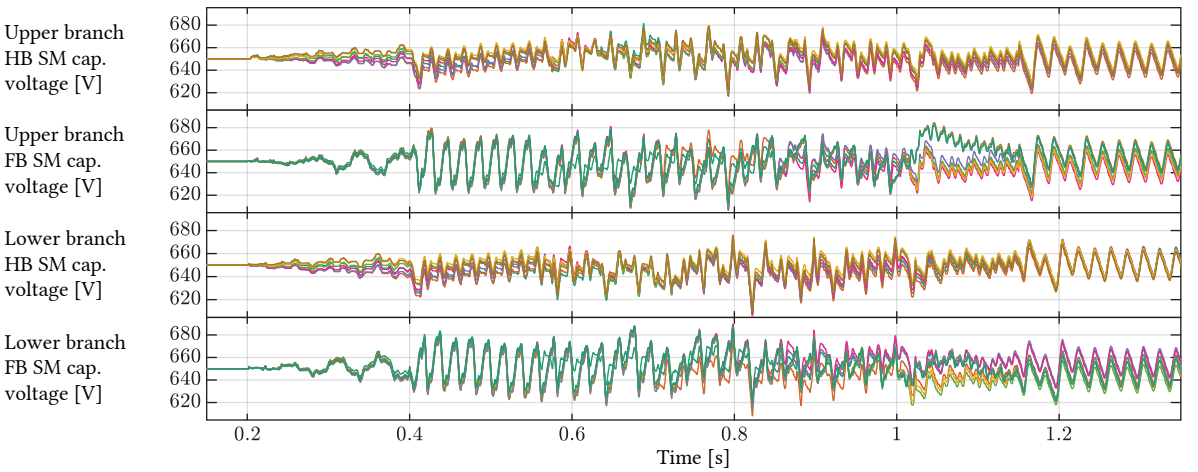


Fig. 5.16 HB and FB SMC capacitor voltage for test sequence is presented, for both upper and lower branch of a phase-leg. Voltage deviation is below ±7 %, i.e. 606 V to 692 V, at variable DC link voltage and rated DC link current operation over the complete operating range at $\cos \varphi_s = 1$.

5.6.6 Current capacity requirements of the H-MMC

As elaborated in **Sec. 5.3.2**, an additional control layer is introduced to H-MMC to enable energy equilibrium of FB and HB SMCs. As certain power of exchange between the two SMCs needs to be established through dedicated voltage and current components' interaction, there is a degree of freedom in favoring either lower voltage or lower current amplitudes for the task. Naturally, to keep the losses low, lower current is a preferred choice. On the other hand, converter branch voltage budget is limited, thus there is a limitation in SMC balancing voltage component increase. In the simulations, SMC balancing voltage amplitude is set to a fixed amplitude of $\hat{v}_{\mathrm{c,bal,SMC}} = 0.132\,\mathrm{pu}$, excluding rated DC link voltage operation, where SMC balancing is obsolete, following zero power demand (5.19).

Peak current budget of a conventional MMC with either all-HB or all-FB SMs can be obtained neglecting SMC balancing demands. At the branch-level, the peak current budget is determined by per-branch AC- and DC-side current components, levied by the balancing circulating current budget, chosen at $\hat{i}_{\mathrm{c,bal,lim}} = 0.25\,\mathrm{pu}$.

$$\hat{i}_{\mathrm{br,lim}} = \hat{i}_{\mathrm{c,bal,lim}} + i_{\mathrm{DC,n}}/3 + \hat{i}_{\mathrm{s,n}}/2 = 0.852\,\mathrm{pu} = 71\,\mathrm{A} \tag{5.28}$$

Converter current components are presented in more details in **Fig. 5.17**. Three topmost graphs depict conventional horizontal and vertical MMC balancing components, as well as H-MMC-specific SMC balancing current. These references are summed up, and controlled by a single circulating current controller as in **Fig. 5.7**, realized through a PIR controller, i.e. proportional, integral and resonant action, as it should control both AC and DC circulating current components. Total balancing circulating current reference and actual value are presented in the fourth subplot. Further, constant DC link current, and increasing AC-side current are presented. The lowermost graph plots the six branch currents and compares them to the peak current limit of the conventional MMC design approach (5.28). The maximal amplitude reached by the branch current of H-MMC in the test pattern of **Sec. 5.6.1** equals 82.5 A, or 16.2 % above the conventional design peak limit.

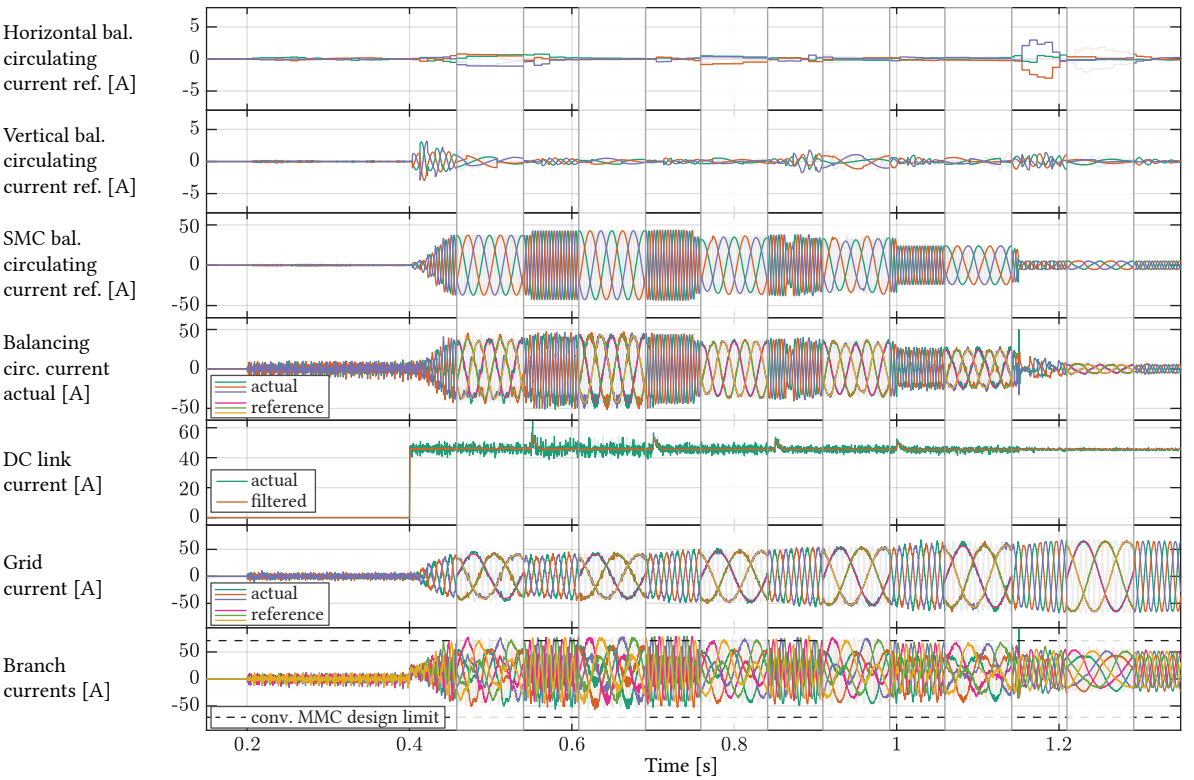


Fig. 5.17 Current components contributing to the converter branch stress are presented for the first test scenario, i.e. unity power factor operation at the variable DC link voltage reference. MMC-internal circulating currents are already presented per-branch. DC link current contributes as $i_{DC}/3$ while AC-side current contributes with half of its amplitude. Lowermost graph presents the six branch currents and the peak branch current limit of conventional MMC design (71 A). In terms of peak current carrying capability, the maximal overload compared to the conventional MMC is 82.5 A, or 16.2 %. For each operating point, i.e. for each DC link voltage value from $0.5V_{DC,n}$ to the rated, a zoomed-in semi-transparent area has been added to the graph, which represents waveforms in more details.

The obtained value represents the peak current over the entire operating range, at the worst-case scenario of rated DC current, corresponding to constant-torque machine operation in PHSP application (**Fig. 5.1**). Following (5.19), **Fig. 5.15** and **Fig. 5.17**, SMC balancing current depends on both active power being transferred and DC link voltage reduction. While this result definitely calls for SM peak current over-sizing compared to a HB- or FB-based MMC, the observed PHSP application should be kept in mind. Low DC link voltage value corresponds to the low output machine frequency (3.12). In steady-state operation, machine output frequency is in a certain band around rated, typically up to 10 % below [78], where additional current stress is only slightly above the design limit (**Fig. 5.17**).

As low speeds are used during pump/turbine change-over of the operating regimes, the over-current scenario is likely to only happen in these transients. Moreover, if the machine is not operated in constant-torque, but rather towards natural quadratic torque pump characteristics, i.e. if active power is not linearly proportional to the frequency, overload level can be additionally decreased. Further, the obtained current limit (5.28) can be decreased if voltage budget allows for an increase in SMC balancing voltage component (5.21).

Tab. 5.5 Switching and conducting devices count of H-MMC in three operating points, compared to an all-FB AFE MMC. All numbers are given relative to the total SM count, while diodes are neglected.

k_{DC}	N_{FB}	N_{HB}	FB_V	HB_V	switching	conducting
$[-1, 1]$	1	0	1	0	2	2
0.5	0.56	0.44	0.56	0.44	1.56	1.56
0.8	0.56	0.44	0.31	0.69	1.31	1.56
1	0.56	0.44	0	1	1	1.56

5.7 Discussion of the results

At reduced DC link voltage operation, additional H-MMC SMC balancing control layer introduces certain additional current stress to the semiconductors, compared to an all-FB based AFE MMC presented in **Chap. 4** (5.17). A question of H-MMC benefit thus arises, taking into account higher SM current rating that translates into higher initial converter cost and potentially higher losses. Starting from the presented H-MMC design (**Tab. 5.2**), a comparison to its FB counterpart is made in **Tab. 5.5**, for three values of k_{DC}. At the lowest attainable value of $k_{DC} = 0.5$, active semiconductor count is lower in H-MMC, however higher current stresses reduce this advantage. Further increase in DC link voltage amplitude causes an increasing fraction of FB SMs to operate as virtual HB units. Considering unipolar modulation, such a FB SM will only receive non-negative reference, upper switches will change state, while only one of the lower two will permanently conduct within the cycle. The closer to rated DC voltage the operating point is, the more pronounced this effect is. Finally, at $k_{DC} = 1$, the same number of semiconductors is actively switching as in a HB MMC.

Considering VS PHSP application, where low DC link voltage values occur only during transients, and operating range is in a certain region around the rated frequency, the initially higher current requirements are compensated through the exploitation benefits.

5.8 Summary

Variable DC link voltage operation of the H-MMC-based AFE converter is a promising enabling technology for retrofit of high number of large PHSPs to VS operation.

A H-MMC realized using a mix of FB and HB SMs is presented. Converter design, in terms of minimal FB SM share for a desired DC link voltage operating range is derived. Additional control layers required for correct energy balancing of FB and HB SMCs are developed and verified.

Operation at unity power factor, as well as at an arbitrary non-unity power factor is enabled over the entire attainable operating range. Both upper- and lower branch of each phase-leg are equally loaded in terms of current and voltage requirement, leading to the uniform SM devices selection and thermal design. While somewhat higher SM current rating is required compared to a FB-based AFE MMC, the lower total number of switching actions, especially at higher DC link voltage amplitudes, compensates for this downside.

Redundancy inherent to the conventional MMC topology has not been compromised in H-MMC. Design- and control approach have been verified through an extensive set of high-fidelity switched-

model simulations. Grid-code-compatibility in terms of an arbitrary power factor, and thus the ability to support the grid under abnormal conditions, is retained.

The following chapter provides yet another alternative to a FB-based AFE for variable DC link voltage operation of an I-MMC for PHSP. Unlike the solution presented in this chapter, a control- and design method offering down-to-zero DC link voltage control is presented. Instead of partial reduction of CM voltage stress to the machine, a CM-voltage-free operation possibility is achieved. This, however, will be done at the expense of limited attainable power factor range on the grid side, depending on the current machine operating point.

Similarly to this chapter, a design method is derived, offering a trade-off between FB SM share, attainable DC link voltage range, and the degree of reduction of available grid-side power factor range.

6

Hybrid MMC With Zero CM-Voltage-Stress for PHSP Retrofit

*This chapter presents a novel control- and design method for an I-MMC for PHSP applications. As in **Chap. 5**, the grid-side stage is an H-MMC with a mix of HB and FB SMs in each branch, while the machine-side stage is realized as an HB MMC. Unlike **Chap. 5**, where grid-code compatibility retention was of primary concern, this chapter presents an alternative H-MMC control- and design method, with the primary goal of enabling CM-voltage-free machine operation. This is performed at the expense of reduction in attainable grid-side power factor during operation below the machine rated speed. A design trade-off offers further expansion of the converter operating area through selection of higher-than-minimal FB SM share in the H-MMC stage. Control system and the limits of operation are verified through switched-model simulations.*

6.1 CM-voltage-free machine operation

As discussed thoroughly in **Chap. 3** and **Sec. 5.1**, variable DC link voltage operation of the machine-side MMC stage, such that ratio of DC voltage reference and the machine output frequency is kept constant, overcomes the main shortcoming of the conventional HB-based I-MMC: high CM voltage machine stress. Starting from the reference design of **Chap. 4**, offering unnecessarily wide DC voltage operating area, a reduction in FB SM share has been realized in **Chap. 5** through the introduction of H-MMC grid-side stage. Appropriate control method ensures retention of grid-code compatibility at reduced, albeit non-zero CM-voltage stress to the machine.

Within this chapter, starting from the same reference design, and deploying H-MMC topology in the grid-side stage, the overall converter structure remains unchanged, as in **Fig. 5.1**. However, the novel control method for H-MMC AFE presented in this chapter enables CM-voltage-free machine operation through down-to-zero variable DC link voltage operation, at equal upper- and lower branches loading, using a standard PSC modulation method, without sorting algorithms. For the novel control method, a design approach for selection of the required FB/HB SM ratio for an arbitrary DC voltage reduction range is developed. A design trade-off between attainable DC link voltage reduction, available grid-side power factor range and FB SM share is presented.

6.2 H-MMC operating principles and design

Analogously to the **Chap. 5**, starting from an all-HB MMC designed for fixed DC link voltage operation, comprising N_{SM} SMs per branch, charged to $V_{\mathrm{SM}} = V_{\mathrm{DC,n}}/N_{\mathrm{SM}}$, a portion of the SMs can be replaced by FB units, to achieve sufficient negative voltage insertion capability required by the

variable DC link voltage operation (4.2), as presented in **Fig. 5.1**. This section presents the newly proposed operating principles in terms of insertion voltage reference share between FB and HB SMCs, as well as minimal FB count, that yield inherently balanced converter at an arbitrary DC link voltage value, without the need to employ any sorting algorithm.

6.2.1 Equivalent circuit

H-MMC equivalent circuit is depicted in **Fig. 5.2**. All the SMs of a branch are represented by two equivalent clusters, corresponding to N_{FB} and N_{HB} individual SMs. As the analysis of the two branches within a phase of **Fig. 5.2** is equivalent, upper branch is observed. Starting from the same notation as in **Chap. 5**, the problem is discussed for a certain operating point, defined by the following:

- **DC-side** voltage reference, determined through k_{DC}.
- **AC-side** (grid) voltage reference $\hat{v}_{\mathrm{s}}$, corresponding modulation index – m_{s}, power factor – $\cos(\varphi_{\mathrm{s}})$ and output voltage displacement angle – θ_{s}, as well as current amplitude – $\hat{i}_{\mathrm{s}}$.

Following the convention defined in **Fig. 6.1**, grid-side voltage phasor is aligned to the reference axis. Converter AC-side terminal voltage v_{s} is displaced with respect to the reference axis by the angle θ_{s}. Assuming purely inductive equivalent AC-side impedance, grid current is in quadrature with $\underline{V}_{\mathrm{s}} - \underline{V}_{\mathrm{g}}$. Grid current to converter AC-side voltage displacement angle is defined as $\varphi_{\mathrm{s}} = \theta_{\mathrm{s}} - \Psi_{\mathrm{s}}$.

In general, insertion voltage references of HB (6.1) and FB (6.2) SMCs can have arbitrary AC voltage amplitudes ($\hat{v}_{\mathrm{HBAC}}$, $\hat{v}_{\mathrm{FBAC}}$), AC voltage displacement angles (φ_{HB}, φ_{FB}) and DC voltage amplitudes (V_{HBDC}, V_{FBDC}), as long as the MMC operating constraints are satisfied, as discussed later in **Sec. 6.2.2**. Following the notation of **Fig. 6.1**, SMC AC displacement angles are referenced with respect to the total branch AC insertion voltage amplitude, in this example v_{p}, defined by the phasor magnitude $\underline{V}_{\mathrm{p}}$ and displacement angle $\theta_{\mathrm{s}} + \pi$ with respect to the reference axis.

Please note that equations (6.1) and (6.2) for the upper branch are written in general form and are always valid if the convention of **Fig. 6.1** is respected. In the given example, angle φ_{FB} is negative with respect to **Fig. 6.1** convention, and its amplitude will thus appear with a minus sign in (6.2).

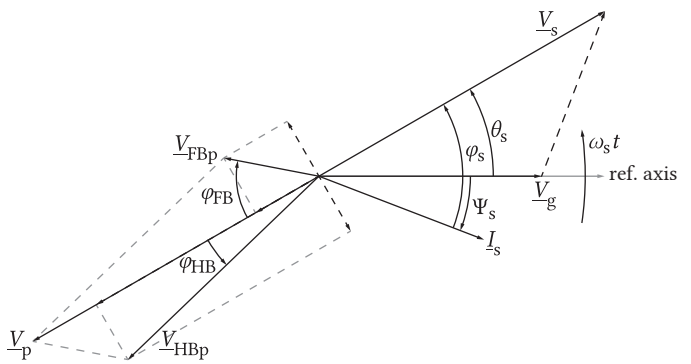


Fig. 6.1 Phasors of grid- and converter-side relevant voltage and current values, with corresponding angles defined. Upper-branch inserted SMC AC voltage phasors, as well as resulting branch-level AC voltage phasor, are presented. Please note that angle sign is defined by an arrow with respect to mathematically positive direction, e.g. φ_{FB} is negative, while φ_{HB} is positive in the given example.

$$v_{\mathrm{HB}} = V_{\mathrm{HBDC}} - \hat{v}_{\mathrm{HBAC}} \cos(\omega t + \theta_{\mathrm{s}} + \varphi_{\mathrm{HB}}) \tag{6.1}$$

$$v_{\mathrm{FB}} = V_{\mathrm{FBDC}} - \hat{v}_{\mathrm{FBAC}} \cos(\omega t + \theta_{\mathrm{s}} + \varphi_{\mathrm{FB}}) \tag{6.2}$$

6.2.2 Operating constraints

SMC insertion voltage waveforms can be arbitrarily chosen as long as the operating constraints, discussed in the following subsections, are met. These form the basis for FB/HB SMC voltage sharing method presented in **Sec. 6.2.3**.

6.2.2.1 Terminal voltage constraints

DC- and AC-side, i.e. sum- and differential voltages must sum up to the DC voltage reference and grid current controller reference, respectively (see (4.2)), as in (6.3) and (6.4). Following (4.2), the relation between the DC terminal (6.3), AC terminal (6.4) and SMC voltages (6.1) and (6.2) can be derived.

$$\text{DC: } k_{\mathrm{DC}} V_{\mathrm{DC,n}}/2 = V_{\mathrm{FBDC}} + V_{\mathrm{HBDC}} \tag{6.3}$$

$$\begin{aligned}
\text{AC: } & m_s V_{\mathrm{DC,n}} \cos(\omega_{\mathrm{s}} + \theta_{\mathrm{s}})/2 \\
&= \hat{v}_{\mathrm{FBAC}} \cos(\omega t + \theta_{\mathrm{s}} + \varphi_{\mathrm{FB}}) \\
&+ \hat{v}_{\mathrm{HBAC}} \cos(\omega t + \theta_{\mathrm{s}} + \varphi_{\mathrm{HB}}) \\
&= \underbrace{\left[\hat{v}_{\mathrm{FBAC}} \cos(\varphi_{\mathrm{FB}}) + \hat{v}_{\mathrm{HBAC}} \cos(\varphi_{\mathrm{HB}})\right]}_{=m_s V_{\mathrm{DC,n}}/2} \cos(\omega_s t + \theta_{\mathrm{s}}) \\
&- \underbrace{\left[\hat{v}_{\mathrm{FBAC}} \sin(\varphi_{\mathrm{FB}}) + \hat{v}_{\mathrm{HBAC}} \sin(\varphi_{\mathrm{HB}})\right]}_{=0} \sin(\omega_s t + \theta_{\mathrm{s}})
\end{aligned} \tag{6.4}$$

A multitude of AC voltage sharing options can be seen from (6.4), as the AC voltage reference at the terminals can be synthesized through various combinations of HB and FB insertion voltage amplitudes ($\hat{v}_{\mathrm{HBAC}}$,$\hat{v}_{\mathrm{FBAC}}$) and displacement angles (φ_{HB},φ_{FB}). One can observe from **Fig. 6.1** that it is favorable to minimize displacement angles amplitudes, as this will in turn require lower SMC AC voltage amplitudes for the same terminal voltage reference.

6.2.2.2 Terminal and SMC energy constraints

Energy exchange in an MMC must be matched between AC and DC terminals, otherwise SM capacitors may be discharged or overcharged. In case of H-MMC, this is true at both branch-terminal-level (6.5) and SMC-level (6.6) and (6.7). Zero-average values of (6.5) to (6.7) must be maintained.

$$\overline{p}_{\mathrm{DC}} + \overline{p}_{\mathrm{AC}} = \frac{k_{\mathrm{DC}} V_{\mathrm{DC,n}} i_{\mathrm{DC}}}{6} - \frac{m_s V_{\mathrm{DC,n}} \hat{i}_s}{8} \cos(\varphi_{\mathrm{s}}) \tag{6.5}$$

$$\overline{p}_{\mathrm{FB,SMC}} = \frac{V_{\mathrm{FBDC}} i_{\mathrm{DC}}}{3} - \frac{\hat{v}_{\mathrm{FBAC}} \hat{i}_s}{4} \cos(\varphi_{\mathrm{s}} + \varphi_{\mathrm{FB}}) \tag{6.6}$$

$$\overline{p}_{\mathrm{HB,SMC}} = \frac{V_{\mathrm{HBDC}} i_{\mathrm{DC}}}{3} - \frac{\hat{v}_{\mathrm{HBAC}} \hat{i}_s}{4} \cos(\varphi_{\mathrm{s}} + \varphi_{\mathrm{HB}}) \tag{6.7}$$

Among (6.5) to (6.7), only two equations are independent, as $\overline{p}_{\mathrm{FB,SMC}} + \overline{p}_{\mathrm{HB,SMC}} = \overline{p}_{\mathrm{AC}} + \overline{p}_{\mathrm{DC}}$. Thus, (6.5) and either (6.6) or (6.7) can be considered as the system of two equations fully defining terminal

and SMC energy constraints of a H-MMC. As (6.5) is a terminal constraint unrelated to intra-branch control, i.e. contains only converter-level operating point variables, it will not contribute the system of internal H-MMC variables. Relationship between the AC and DC current components is derived from (6.5).

$$i_{\mathrm{DC}} = \frac{3m_{\mathrm{s}}\hat{i}_{\mathrm{s}}}{4k_{\mathrm{DC}}}\cos(\varphi_{\mathrm{s}}) = \frac{3\hat{v}_{\mathrm{s}}\hat{i}_{\mathrm{s}}}{2k_{\mathrm{DC}}V_{\mathrm{DC,n}}}\cos(\varphi_{\mathrm{s}}) \tag{6.8}$$

6.2.2.3 SM voltage constraints

At the SM- and SMC-level, limitations to the design space are introduced, imposed by the electrical ratings of SMs and number of SMs per SMC. HB insertion voltage reference must always be non-negative (6.9), while maximal available insertion voltage of HB (6.10) and FB (6.11) SMCs are determined by their corresponding number.

$$V_{\mathrm{HBDC}} + \hat{v}_{\mathrm{HBAC}} \geq 0 \tag{6.9}$$
$$V_{\mathrm{HBDC}} + \hat{v}_{\mathrm{HBAC}} \leq (1 - N_{\mathrm{FB}}/N_{\mathrm{SM}})\, V_{\mathrm{DC,n}} \tag{6.10}$$
$$|V_{\mathrm{FBDC}} + \hat{v}_{\mathrm{FBAC}}| \leq (N_{\mathrm{FB}}/N_{\mathrm{SM}})\, V_{\mathrm{DC,n}} \tag{6.11}$$

6.2.3 SMC insertion voltage determination

In the H-MMC, we can differentiate three sets of variables.

1. **System-level:** AC-side voltage amplitude (through m_{s}), grid current – i_{s} and power factor – $\cos(\varphi_{\mathrm{s}})$.
2. **Converter-level:** DC-side rated voltage and reduction factor – $V_{\mathrm{DC,n}}$, k_{DC}; total number of SMs, share of FB and HB units – N_{SM}, N_{FB}, N_{HB}.
3. **Branch-level SMC:** AC voltage amplitudes – $\hat{v}_{\mathrm{FBAC}}$, $\hat{v}_{\mathrm{HBAC}}$; AC voltage displacement angles – φ_{FB}, φ_{HB}; DC voltage amplitudes – V_{FBDC}, V_{HBDC}.

System-level variables can be set to their rated values, while converter-level variables, with the exception of k_{DC}, are defined by the converter design. This leads to the branch-level variables. The six intra-branch variables are defined by a total of four equations (6.3) and (6.12) to (6.14), obtained as follows.

- DC insertion branch voltage constraint (6.3).
- AC insertion branch voltage constraints, starting from (6.4).

$$\hat{v}_{\mathrm{FBAC}}\cos(\varphi_{\mathrm{FB}}) + \hat{v}_{\mathrm{HBAC}}\cos(\varphi_{\mathrm{HB}}) = \hat{v}_{\mathrm{s}} \tag{6.12}$$
$$\hat{v}_{\mathrm{FBAC}}\sin(\varphi_{\mathrm{FB}}) + \hat{v}_{\mathrm{HBAC}}\sin(\varphi_{\mathrm{HB}}) = 0 \tag{6.13}$$

- SMC energy balance constraint, from either (6.7) or (6.6), utilizing DC- to AC-terminal current relationship $i_{\mathrm{DC}} = f(\hat{i}_{\mathrm{s}})$ (6.8). In this case, equation (6.7) is chosen.

$$\frac{\hat{v}_{\mathrm{HBAC}}}{V_{\mathrm{HBDC}}} \cdot \frac{k_{\mathrm{DC}}}{m_{\mathrm{s}}}\cos(\varphi_{\mathrm{s}} + \varphi_{\mathrm{HB}}) = \cos(\varphi_{\mathrm{s}}) \tag{6.14}$$

Since there are four equations and six variables, two among them are to be chosen freely. The selection is made to set V_{HBDC} (6.15) and $\hat{v}_{\mathrm{HBAC}}$ (6.16) voltage amplitudes in a way to maximally utilize insertion voltage potential of installed HB SMs, respecting (electrical) SM voltage constraints (6.9) and (6.10). This leads to the design with the minimal number of lossier and more expensive FB SMs, in favor of more efficient and cheaper HB units. As certain control voltage reserve must be accounted for, AC voltage component of HB SMC should not exceed (6.16), where k_{res} determines AC voltage control reserve. Factor k_{res} is defined as a fraction of maximal available AC voltage, and is taken as 5 % in this work, i.e. $k_{\mathrm{res}} = 0.05$.

$$V_{\mathrm{HBDC}} = \frac{N_{\mathrm{HB}}}{N_{\mathrm{SM}}} \cdot \frac{V_{\mathrm{DC,n}}}{2} \tag{6.15}$$

$$\hat{v}_{\mathrm{HBAC}} = (1 - k_{\mathrm{res}}) V_{\mathrm{HBDC}} \tag{6.16}$$

FB SMC DC insertion voltage component is defined from (6.3).

$$V_{\mathrm{FBDC}} = \frac{V_{\mathrm{DC,n}}}{2} \left(k_{\mathrm{DC}} - \frac{N_{\mathrm{HB}}}{N_{\mathrm{SM}}} \right) \tag{6.17}$$

Furthermore, observing (6.14), m_{s} is constant for a grid-connected application, while k_{DC} can be in the range of $k_{\mathrm{DC}} \in [0, 1]$. Likewise, the ratio of AC to DC insertion voltage components of HB SMC can be in the range of $\hat{v}_{\mathrm{HBAC}}/V_{\mathrm{HBDC}} \in [0, 1]$, following (6.9). Thus, for minimal alteration of φ_{HB}, and consequently minimal additional SMC AC voltage amplitude required to synthesize required branch-level voltage (refer to $\underline{V}_{\mathrm{p}}$ of **Fig. 6.1**), the maximal value of $\hat{v}_{\mathrm{HBAC}}/V_{\mathrm{HBDC}} = 1 - k_{\mathrm{res}} = 1$ should be selected (6.14), (6.16), which proves the validity of choices (6.15) and (6.16). For the purpose of control voltage reserve, this ratio should be kept below unity, as aforementioned.

Finally, four equations with four variables are left, and the system can be solved. HB displacement angle is calculated from (6.14) and (6.16).

$$\varphi_{\mathrm{HB}} = \arccos\left(\frac{m_{\mathrm{s}} \cos(\varphi_{\mathrm{s}})}{k_{\mathrm{DC}}(1 - k_{\mathrm{res}})} \right) - \varphi_{\mathrm{s}} \tag{6.18}$$

Amplitude of FB SMC AC insertion voltage is obtained from (6.12) and (6.13), following phasor representation of AC voltages given in **Fig. 6.1**. Knowing that $\hat{v}_{\mathrm{p}} = \hat{v}_{\mathrm{n}} = \hat{v}_{\mathrm{s}}$, d- and q-axis components of $\underline{V}_{\mathrm{FB\{p,n\}}}$ can be determined.

$$\hat{v}_{\mathrm{FBAC}} \cos(\varphi_{\mathrm{FB}}) = \hat{v}_{\mathrm{s}} - \hat{v}_{\mathrm{HBAC}} \cos(\varphi_{\mathrm{HB}}) \tag{6.19}$$

$$\hat{v}_{\mathrm{FBAC}} \sin(\varphi_{\mathrm{FB}}) = -\hat{v}_{\mathrm{HBAC}} \sin(\varphi_{\mathrm{HB}}) \tag{6.20}$$

Further, FB SMC AC insertion voltage amplitude and displacement angle are derived.

$$\hat{v}_{\mathrm{FBAC}} = \sqrt{\hat{v}_{\mathrm{s}}^2 - 2\hat{v}_{\mathrm{s}}\hat{v}_{\mathrm{HBAC}} \cos(\varphi_{\mathrm{HB}}) + \hat{v}_{\mathrm{HBAC}}^2} \tag{6.21}$$

$$\varphi_{\mathrm{FB}} = \arctan \frac{-\hat{v}_{\mathrm{HBAC}} \sin(\varphi_{\mathrm{HB}})}{\hat{v}_{\mathrm{s}} - \hat{v}_{\mathrm{HBAC}} \cos(\varphi_{\mathrm{HB}})} \tag{6.22}$$

In this way, SMC insertion voltage references are fully defined. AC voltage amplitude (6.21) and displacement angle (6.22) are the last to be determined. The values are dependent on HB SM insertion voltage amplitude and displacement angle, which are determined to maximally utilize HB SMs' voltage capacity and to ensure SMC-level energy balance, respectively.

6.2.4 Power factor limitation

Assuming constant-voltage-amplitude grid-connected operation of the converter, which is the case in PHSP under normal grid conditions, the modulation index is nearly constant. Power factor limitation is derived from (6.14) and (6.16), keeping in mind that HB SMC AC voltage displacement angle is calculated to satisfy SMC energy equilibrium (6.14). Without affecting the generality, we can observe positive value of cosine functions. In this case, maximal value of $\cos(\varphi_s + \varphi_{HB})$ equals one, and defines the limiting component of attainable AFE power factor.

$$\cos(\varphi_s) = \underbrace{(k_{DC}(1-k_{res})/m_s)}_{\leq 1 \text{ for } m_s=1} \underbrace{\cos(\varphi_s + \varphi_{HB})}_{\max=1} \tag{6.23}$$

Power factor limitation is derived (6.24). Thus, at unity modulation index, power factor is limited by DC voltage reduction factor and AC voltage control reserve.

$$\cos(\varphi_s) \leq k_{DC}(1-k_{res})/m_s \tag{6.24}$$

6.2.5 Design for an arbitrary DC voltage range

Previously formulated relations can be used to aid the design of H-MMC. For a desired DC voltage reduction and known input power factor, one could determine optimal ratio of FB and HB SMs. However, to explore all the combinations, while allowing comparison to the reference design and the previously introduced H-MMC control- and design approach (**Chap. 5**, the design flow example presented hereafter is related to the converter parameters used throughout this thesis (**Tab. 5.2**).

A minimal number of FB SMs should be determined, so as not to violate the available SM insertion voltage limitation (6.11), for a given total number of SMs and desired DC voltage operating range, i.e. k_{DC} range. Determination process is iterative, as follows, and demonstrated on medium voltage MMC with parameters given in **Tab. 5.2**, where $m_{s,n} = 0.95$ and $k_{res} = 0.05$.

- Starting from an all-HB MMC, one HB SM per branch is replaced by a FB SM.
- DC voltage reference is swept over the desired operating range, i.e. $k_{DC} \in [k_{DC,min}, 1]$.
- Power factor is swept from maximal value (6.24) to zero.
- For each operating point defined by N_{FB}, k_{DC} and $\cos(\varphi_s)$, SMC-level variables are calculated according to (6.3) and (6.15) and (6.22).
- Voltage insertion capability of the selected number of FB and HB SMs is compared against the calculated insertion voltage references. If assumed SM configuration cannot synthesize the required references, one more HB SM is replaced by a FB unit and the entire process is repeated.
- The highest-HB-share solution, not violating insertion voltage capability (6.11), is adopted.

Following the generalized derivation of **Secs. 6.2.2** to **6.2.4**, the presented iterative design approach will always produce optimal design in terms of the lowest share of FB SMs for the required DC link voltage range and AC-side power factor range.

6.2.6 Design selection for PHSP application

For CM-free PHSP operation, value of $k_{\mathrm{DC,min}} = 0$ is required. Attainable DC voltage reduction and power factor range are presented in **Fig. 6.2**, for the converter ratings given in **Tab. 5.2**.

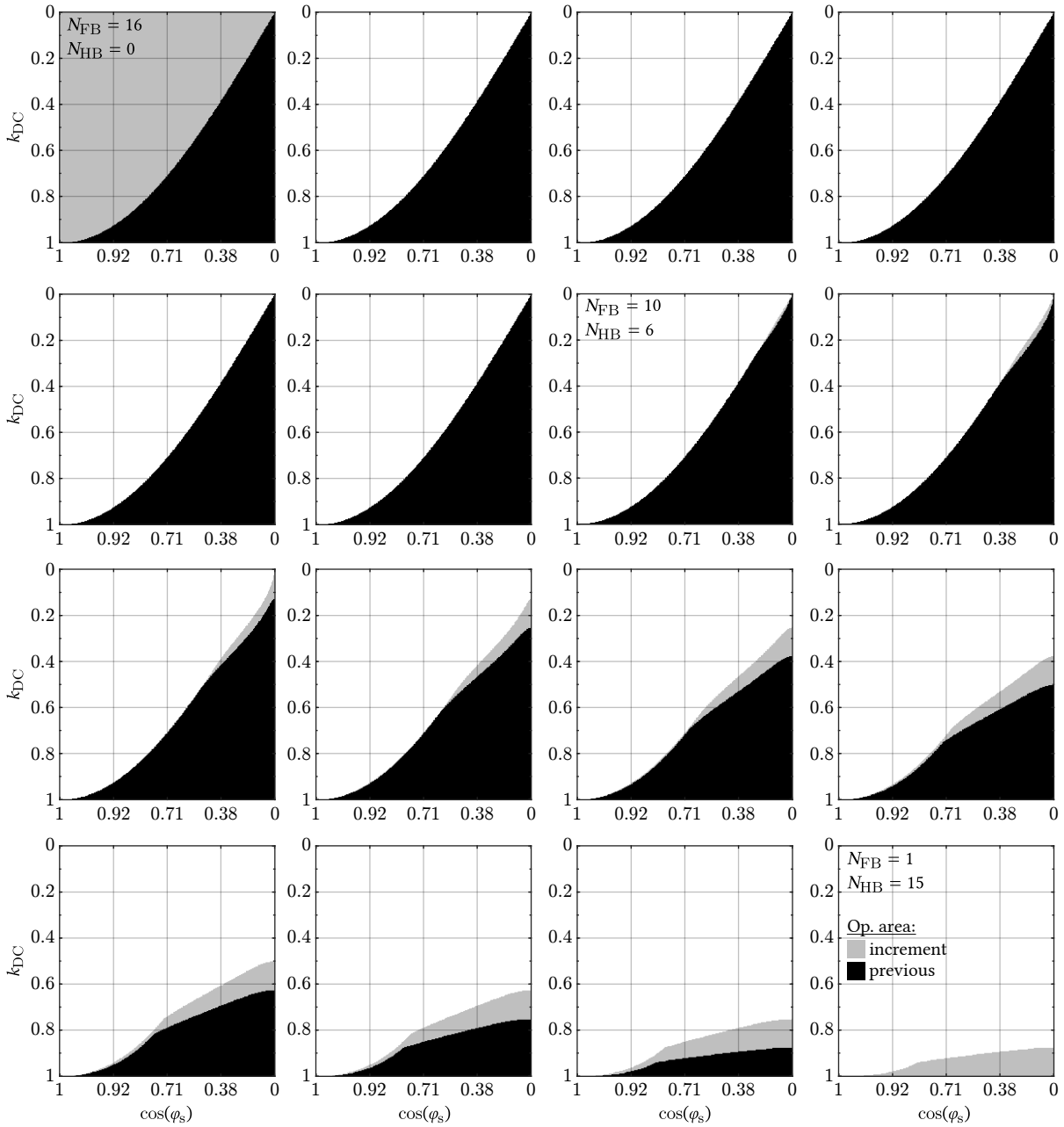


Fig. 6.2 Attainable operating region for varying share of FB SMs, starting from **Tab. 5.2** converter parameters for $m_{\mathrm{s}} = 0.95$ and $1 - k_{\mathrm{res}} = 0.95$. For each $N_{\mathrm{HB}}/N_{\mathrm{FB}}$ ratio, the grey area in graphs shows the achieved increment in converter operating range compared to the configuration with one FB SM less, which is marked by the black area. It can be noticed that an increase in FB count above $N_{\mathrm{FB}} = 10$ doesn't provide further operating range extension for the presented method. FB-only solution achieves full DC voltage range at arbitrary power factor, whereas HB-only setup operates at arbitrary power factor in a narrow band around the rated DC voltage.

For each N_{HB}/N_{FB} ratio, the grey area in graphs shows the achieved increment in converter operating range compared to the configuration with one FB SM less, which is marked by the black area. In an all-HB MMC case, operation at arbitrary power factor in a narrow band around rated DC voltage is possible. Introduction of FB SMs in place of HB units gradually increases operating range towards lower DC voltage values. Surpassing $N_{FB} = 10$, there is no further yield in increased FB share for the presented method.

Following this analysis, minimal FB share that enables DC link operating range down to zero for the used MMC ratings, is $N_{FB} = 10$. This hardware configuration is henceforth used in test scenarios. Naturally, if one only has a need for partial DC voltage reduction, lower FB count and thus cheaper and more efficient configuration can be chosen. The optimization criteria of the presented method is to obtain the lowest FB SM share, starting from a converter of arbitrary ratings and SM count. This has been demonstrated for arbitrary DC link voltage range and AC-side power factor.

6.3 H-MMC energy balancing

Zero-average energy exchange is ensured both at the branch level through AC and DC terminal constraints, and at the SMC level, through novel insertion voltage and displacement angles strategy.

At SM level, PSC modulation establishes energy balance. However, as in a conventional MMC with uniform SMs, limited corrective energy balancing actions are required. Four principal balancing actions are inherited from the conventional MMC, while an additional SMC balancing layer is added, as presented in **Fig. 6.3**.

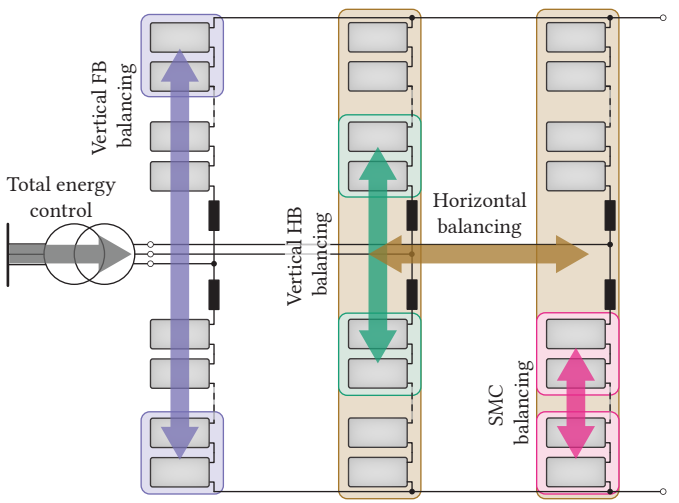


Fig. 6.3 Energy control and balancing loops of H-MMC operating as AFE are presented. While total energy control and inter-phase horizontal energy balancing are performed equally as in a conventional MMC (**Chap. 2**, inter-branch vertical energy balancing is altered. Due to displacement angles in inserted AC voltages of SMCs (6.18), (6.22), independent balancing control loops are established for HB and FB SMCs. An additional intra-branch balancing layer has been added to compensate for imbalance between same-branch SMCs.

6.3.1 Conventional energy balancing loops

Three out of four conventional energy balancing actions are implemented identically to a MMC with uniform SMs, as presented in **Chap. 2**.

Total energy is controlled in the same manner as for a conventional MMC [51], [79]. In the case of AFE, this loop is supplied from the grid side ($P^*_{\mathrm{AC,rec}}$ in **Fig. 6.4**).

Horizontal energy balancing is performed in the same manner as with a conventional MMC [44], [79]. DC circulating current $i_{\mathrm{c}\Sigma}$ is fed to the circulating current controller (**Fig. 6.4**), and balancing action is performed in conjunction with inserted DC voltage component (6.3).

Local SM energy balancing is performed as in [80], through correction of SM insertion voltage reference.

6.3.2 Vertical energy balancing

Vertical energy balancing approach equally relies on [44], [79], where inserted AC voltage component (6.4) is used in conjunction with a balancing current component for the control action. However, AC insertion voltage components of HB and FB SMCs differ (6.16), (6.21), thus a unique circulating current reference cannot be generated for both SMCs due to differing AC voltage displacement angles, φ_{HB} and φ_{FB}. Thus, two vertical energy controller are generating two independent circulating current references, $i^*_{\mathrm{c}\Delta\mathrm{HB}}$ and $i^*_{\mathrm{c}\Delta\mathrm{FB}}$ (**Fig. 6.4**) for control of the appropriate SMCs, with respect to their AC insertion voltages. Differential energy references are naturally set to zero, while feedback values $\overline{W}_{\Delta\mathrm{HB}\{\mathrm{a,b,c}\}}$ and $\overline{W}_{\Delta\mathrm{FB}\{\mathrm{a,b,c}\}}$ are obtained from filtered-out SM capacitor voltage measurements.

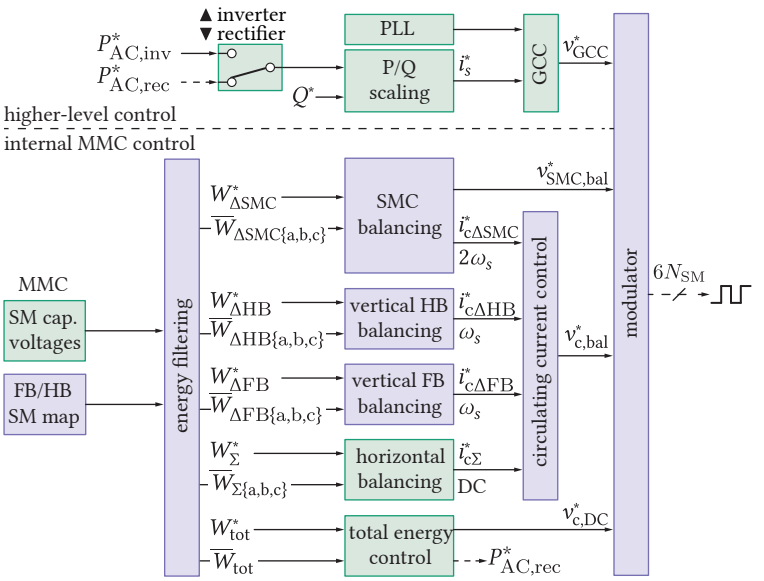


Fig. 6.4 H-MMC control outline is presented. Starting from conventional MMC control (green), vertical balancing is performed independently for FB and HB SMCs, while SMC balancing layer is added to the internal control. A FB/HB SM map is required for proper SMC energy measurement and control. Upper-level control is unaffected, comprising grid-code-compliant scaling of active (P) and reactive (Q) power references, followed by grid current controller (GCC), synchronized to the grid through phase-locked loop (PLL).

6.3.3 Inter-SMC energy balancing

In the presented control method, SMC balancing is inherently guaranteed under the steady-state conditions, as demonstrated in **Sec. 6.2**. However, as in horizontal and vertical balancing actions, a small corrective balancing capacity is required to re-balance SMCs after transient events.

Inter-SMC energy exchange is achieved utilizing additional circulating current and voltage components, which will not interact with terminal voltages and currents. Thus, an AC circulating current at $2\omega_s$ (6.25), along with an additional SMC voltage at $2\omega_s$ (6.26), is introduced to produce this corrective action, where $x \in \{a, b, c\}$ and $\theta_x \in \{0, -2\pi/3, 2\pi/3\}$. Zero-sum DC terminal circulating current condition must be satisfied (6.27), determining balancing current per-phase amplitudes $\hat{i}_{c\Delta SMCx}$ and displacement angles Ψ_x.

$$i_{c\Delta SMCx} = \hat{i}_{c\Delta SMCx} \cos(2\omega_s t + \Psi_x) \tag{6.25}$$

$$v^*_{SMC,bal\{HB,FB\}x} = \pm\hat{v}_{SMC,bal} \cos(2\omega_s t + \theta_x) \tag{6.26}$$

$$\sum i_{c\Delta SMCx} = 0 \tag{6.27}$$

Energy flow between SMCs of the same branch by means of (6.25) and phase-opposing voltages (6.26) is thus compensating the energy imbalances.

SMC differential energy reference is defined by FB to HB ratio, i.e. the difference in rated energy levels of the corresponding SMCs (6.28).

$$W^*_{\Delta SMC} = \frac{1}{2}\left(\frac{(\Sigma V_{SM,HB})^2}{N_{HB}} - \frac{(\Sigma V_{SM,FB})^2}{N_{FB}}\right) C_{SM} = \frac{C_{SM} V^*_{SM}}{2}(N_{HB} - N_{FB}) \tag{6.28}$$

SMC energy balancing relies on a dedicated energy controller, outputting per-phase balancing current components (6.25), further modified to guarantee zero-sum amplitude at DC converter terminals (6.27). As the same mapping principle is used in conventional inter-branch vertical MMC balancing, the same control structure can be used [44]. One can notice that the same method was used in **Chap. 5**. Unlike here, where inter-SMC action of corrective nature, the previously proposed H-MMC control method utilizes it as the dominant balancing path between the SMCs, requiring higher balancing voltage or current amplitudes.

6.3.4 Modulation

In high-SM-count MMC applications, e.g. high-voltage DC inter-ties, the use of nearest-level modulation is common due to high output voltage resolution [46], [47]. Medium-voltage applications, however, comprise far fewer SMs. Inheriting modulation of high-voltage DC installations would result in poor output voltage waveform quality, further followed by significant current harmonic distortion [46].

A method to adapt modulation approach to medium-voltage installations, by combining nearest-level and pulse-width modulation, is presented in [46]. Another approach can naturally be the use of PSC modulation, introduced for multilevel converters in [48]. In such a case, N_{SM}-times higher apparent switching frequency at the converter branch terminals, with respect to SM switching frequency, ensures high-quality output voltage waveform, i.e. low total harmonic distortion.

In conventional MMC with either all-HB or all-FB layout, PSC modulation can be implemented as in [48]. So far presented PSC-based medium-voltage H-MMC solutions with reduced DC voltage

(boosted AC modulation index) operation capability, with a mix of HB and FB SMs within branches, require capacitor sorting algorithms and modulation reference alterations for proper operation [47]. In the method proposed in this chapter, HB and FB SMCs within each converter phase leg act as two independent voltage sources (**Fig. 5.2**), with a separate layer controlling energy balancing between the two. Thus, classical PSC modulation with two sets of carriers for FB and HB SMCs has been implemented, requiring no capacitor sorting algorithm.

Following the developed control structure (**Fig. 6.4**), the modulator is presented in more details in **Fig. 6.5**. Starting from voltage references of the grid current control, SMC balancing and balancing current control, circulating current control and total energy control, insertion voltages of HB and FB SMCs are generated. Individual SM capacitor voltages are measured, filtered, and summed-up based on SM map, to obtain HB and FB SMC available insertion voltages for closed-loop control. Two sets of PSCs are used to generate gating signals for SMs of corresponding SMCs. Effectively, the modulation scheme is simpler than in the control method of **Chap. 5**, as the *virtual SM* concept is not in use here, thus there is no need for carrier- and SM map modifications.

6.3.5 System-level control

Higher-level control system of H-MMC is developed in compliance with the control schemes utilized in the existing variable speed PHSPs [62], as presented in the reference design of **Sec. 4.2**. Since the internal MMC control should be decoupled from the terminals, the same grid- and machine-side control loops are valid, the only adaptation being in the attainable operating area range, as discussed in **Sec. 6.2.4**.

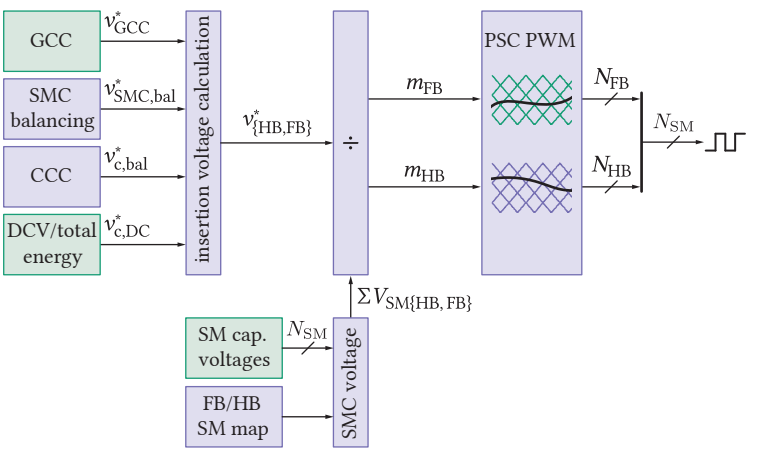


Fig. 6.5 Modulation scheme of H-MMC is presented, with conventional MMC control blocks in green and newly-introduced blocks in violet. SM mapping stores information on FB/HB SM position in the branches and is used to correctly sum available insertion voltages of FB/HB SM clusters. In contrast to a conventional MMC, SM cluster balancing voltage components $v^*_{SMC,bal}$, and circulating current controller additional SM cluster balancing currents are added. Insertion voltage references $v^*_{\{HB,FB\}}$ are obtained by the voltage sharing algorithm presented in **Sec. 6.2.3**. FB/HB clusters' insertion indices are then obtained, based on available insertion voltages $\Sigma V_{SM\{HB,FB\}}$. Two sets of phase-shifted carriers are used to generate SM gating signals.

6.4 Test scenarios and results

A total of three test scenarios have been performed – AFE stage supplying a passive DC load, AFE operation under alteration of power factor beyond attainable operating area, and finally synchronous machine start-up sequence of the H-MMC-based converter. The presented results are obtained from switched-model simulations. Exceptionally, system-level test scenario (**Sec. 6.4.3**) has been simulated utilizing an averaged model, since the converter operation and limits have been demonstrated in details in test scenarios of **Sec. 6.4.1** and **Sec. 6.4.2**.

6.4.1 H-MMC AFE supplying passive load

In the first scenario, presented in **Fig. 6.6**, H-MMC AFE operation is observed over the entire DC link voltage operating range, at 90 % of the rated DC link current. DC voltage reference is increased from zero to rated value in steps of $0.1V_{\mathrm{DC,n}}$, while load is varied to maintain constant DC current amplitude. This resembles a VSD operation, where DC current is a reflection of the machine-side AC current, which is approximately constant in the PHSP application of interest. On the grid side, reactive power reference is determined from the maximal power factor expression (see (6.24)), reaching unity at the rated DC voltage.

Active and reactive power references are correctly tracked. Sum- and differential average capacitor voltages are correctly controlled within the predefined limits. Zoomed-in areas at $t = 2\,\mathrm{s}$ and $t = 8\,\mathrm{s}$ reveal sinusoidal waveforms of both grid current and voltage before and after DC voltage change transients.

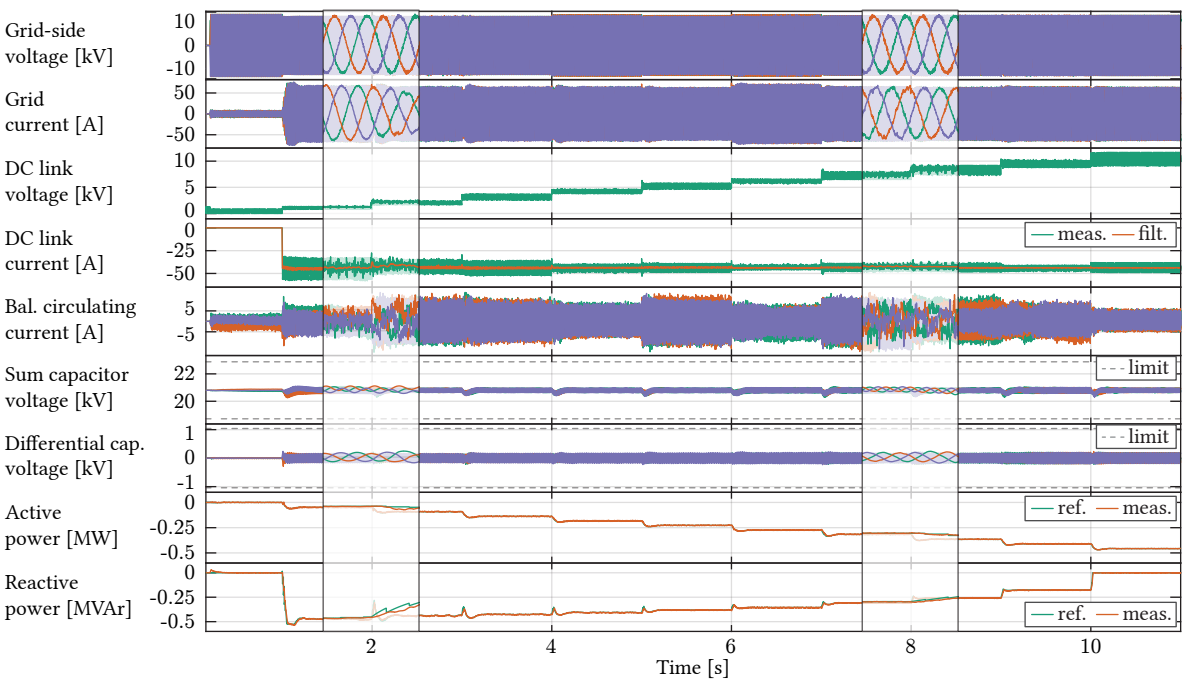


Fig. 6.6 H-MMC test sequence presenting variable DC voltage operation in the entire range from zero to the rated value. Power factor is set at the limit of the safe operating range (6.24). Zoomed-in areas at $t = 2\,\mathrm{s}$ and $t = 8\,\mathrm{s}$ confirm that AC voltage and current are virtually unaffected by the k_{DC} transients.

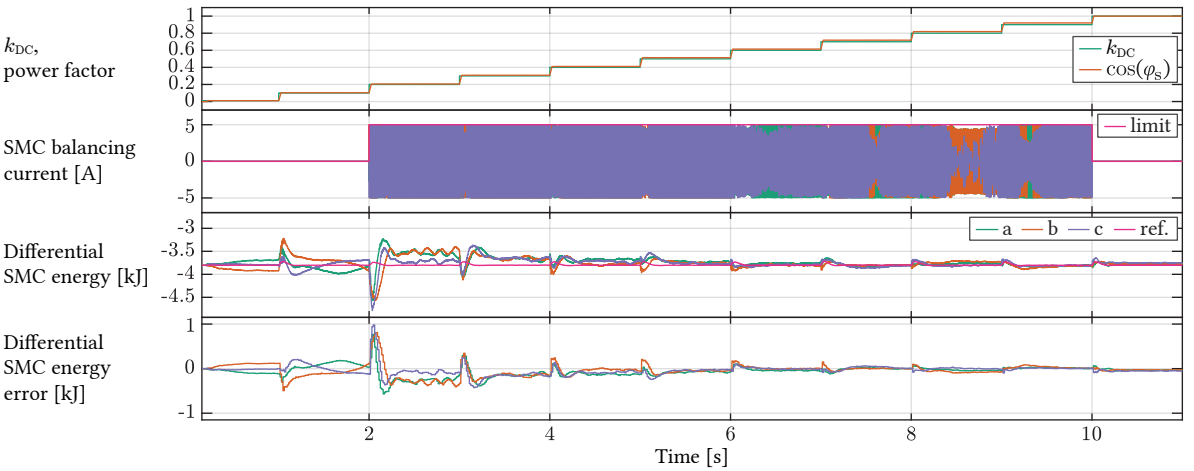


Fig. 6.7 SMC energy balancing action is presented in more details for variable DC voltage operation scenario, at highest attainable power factor. Differential energy between SMCs of each phase converges to the reference value. Balancing action is unnecessary at very low DC voltage value, when converter operates using only FB SMs, as well as at the rated DC voltage, when conventional MMC operation is possible.

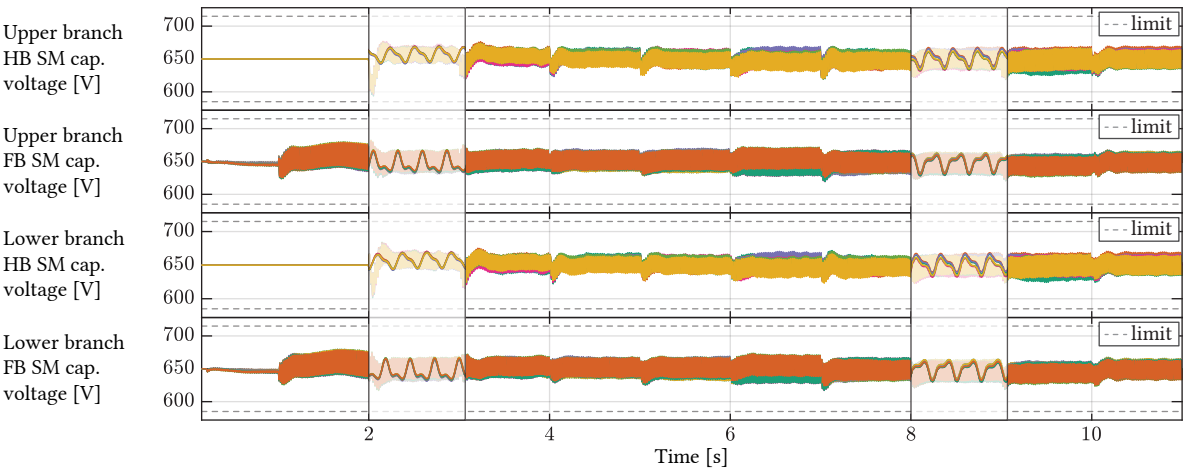


Fig. 6.8 Capacitor voltages of individual SMs of one converter phase-leg, grouped in the SMCs. Zoomed-in areas at $t = 2.5$ s ($k_{DC} = 0.2$) and $t = 8.5$ s ($k_{DC} = 0.8$) reveal capacitor voltage waveforms in more details, when both HB and FB SMs are utilized.

Inter-SMC balancing action, specific to the presented H-MMC control approach, is presented in more details in **Fig. 6.7**. Topmost plot presents variation of power factor $\cos(\varphi_s)$ as a function of DC voltage reference (6.24), taking the maximal value attainable for the given operating point. Dedicated balancing current (6.25) is limited in amplitude, and presented in the next subplot. Further, differential energy reference (6.28) and measured per-phase values are seen. The last subplot presents the controller error, which converges to zero after each transient. In this work, inter-SMC balancing current limit is set to 5 A, i.e. approximately 10 % of branch current amplitude.

At the rated DC voltage value, when there is no negative insertion voltage requirement, the converter can operate as a conventional MMC with equal insertion voltage references for both FB and HB SMs (4.2). In case of very low DC link voltages, in this design $k_{DC} < 0.2$, voltage insertion capability of FB

SMs is sufficient for both DC and AC voltage component amplitudes (see (4.2)), thus converter can operate as conventional FB MMC. In both cases, SMC balancing action is not required and is thus disabled through zero current and voltage limit (6.25), (6.26).

As branch-level sum- and differential capacitor voltages (**Fig. 6.6**) only reflect horizontal, vertical and total balancing actions, **Fig. 6.8** presents individual capacitor voltage values of one phase-leg, grouped to FB and HB SMCs of upper and lower branch. Following the test scenario in the topmost graph of **Fig. 6.7**, three operating segments can be identified.

In the range $(0, 2)$s, while $k_{\mathrm{DC}} < 0.2$, only FB SMs are switched, while HB SMs are bypassed. This operating region coincides with FB-only operating area in **Fig. 6.9**, for the selected hardware configuration ($N_{\mathrm{FB}} = 10$). Zero-current flows through the HB SM capacitors, thus constant voltage and no ripple are observed. Auxiliary SM power supply is fed internally from the SM capacitor, and its power consumption is typically very low compared to the rated SM power. Using the SM presented in [81] as an example similar to simulated converter parameters (**Tab. 5.2**), total internal power consumption of 20 W leads to the discharge time constant in the order of a minute during bypass.

Further, in the range of $[2, 10)$s, the converter is operated as presented in Sec. 6.3. Both HB and FB SMs contribute to the output voltage, however different references are fed to the SMCs, as derived in the previous sections. It can be seen that inter-SMC balancing action ensures average SMC voltages are equal to the reference values, while local SM balancing compensates for capacitance tolerance taken into account in the model (**Tab. 5.2**). Lastly, in the range of $[10, 11)$s, DC link voltage reference is at the rated value. As there is no need for negative branch voltage insertion, all SMs operate with equal insertion voltage references, as in a conventional MMC.

6.4.2 H-MMC limit of operation

Limit of H-MMC operation for the derived control method is presented for multiple hardware configurations in **Fig. 6.9**. For the chosen configuration ($N_{\mathrm{FB}} = 10$), operation in the entire DC voltage range is tested with $0.1V_{\mathrm{DC,n}}$ increments, at the border of attainable operating area, as marked by the green dots.

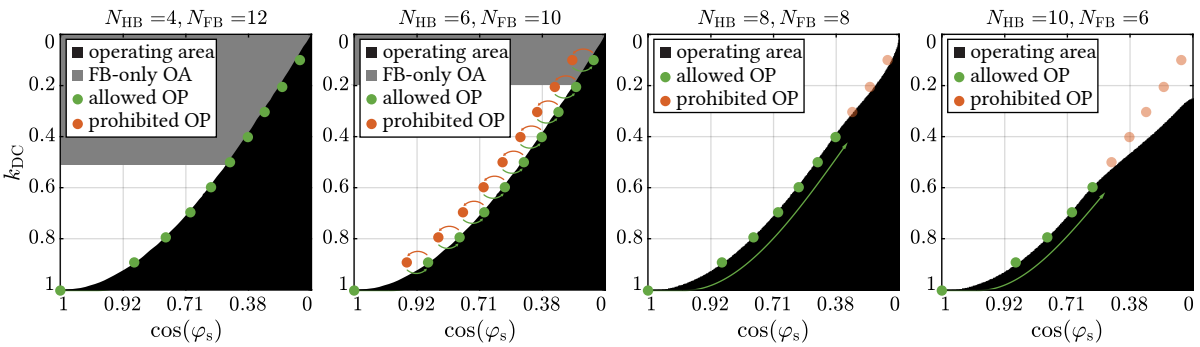


Fig. 6.9 Limit of the H-MMC operating area in terms of DC voltage and power factor range is presented for different hardware configurations. For the selected configuration of $N_{\mathrm{FB}} = 10$, operation in both allowed and prohibited operating area is presented, by deliberately increasing power factor 10 % above the limit at each operating point, for a short time interval. Below $k_{\mathrm{DC}} = 0.2$, available FB insertion voltage is sufficient for AC and DC side insertion voltage requirements (see (4.2)), thus converter can operate as conventional FB unit at any power factor.

In this test scenario, for each of the DC voltage operating points, power factor is set for a short time to 10 % above the limit (6.24), to the operating point marked by a red dot. Under such conditions, SMCs cannot be balanced through any choice of inserted voltages or displacement angles, inter-SMC differential energies diverge and cannot be re-balanced through a limited corrective inter-SMC balancing action. After return to the safe operating area, SMC energy controller gradually reestablishes balance.

Results are depicted in **Fig. 6.10**. For each DC voltage reference, a short alteration of power factor to restricted area is visible in reactive power subplot, while terminal voltage and current waveforms remain unaffected by the short power factor alterations.

At the SMC level (**Fig. 6.11**), however, after expected transient on k_{DC} change, a sharp deviation of SMC differential energies is visible at each prohibited power factor alteration. At such a rate of change, prolonged operation in the prohibited area leads to very high SMC energy deviations, ultimately leading to overcharge of FB and full discharge of HB SMs, or vice versa, and failure of the converter in either case.

Individual capacitor voltages of one phase-leg are presented in **Fig. 6.12**. Short duration of deviations to prohibited operating area and consequent SMC balancing action have ensured average capacitor voltages remain within the predefined limits.

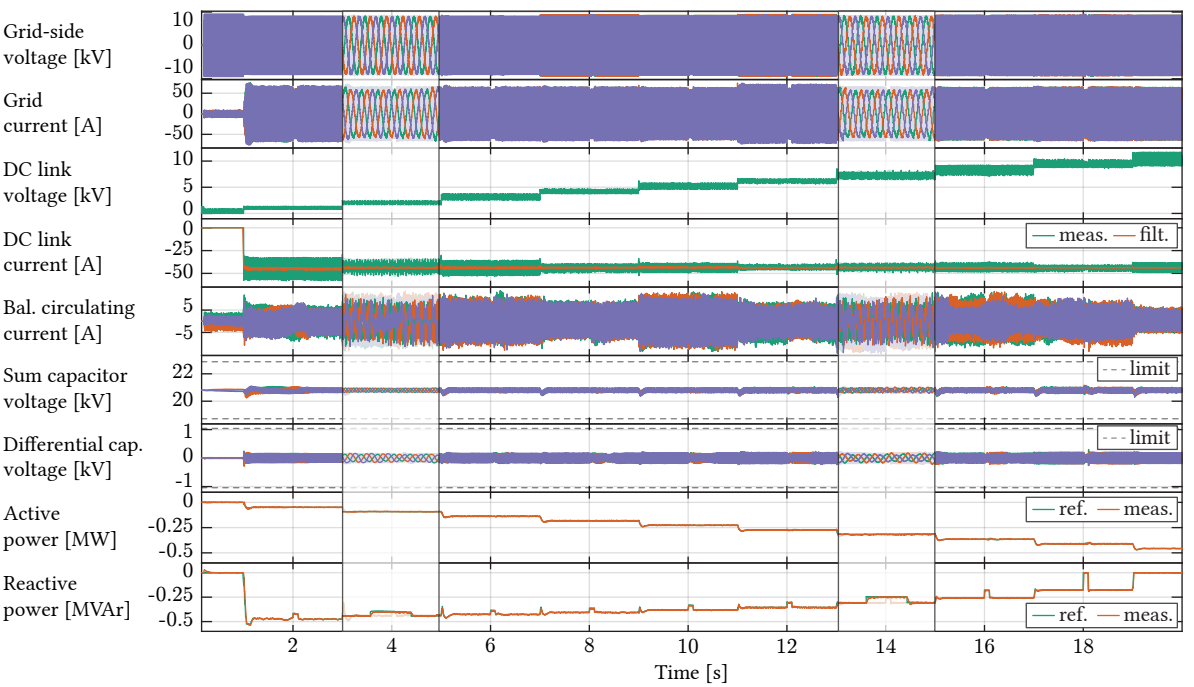


Fig. 6.10 Operating sequence of H-MMC at constant DC current load, over the entire DC voltage operating range. For each applied k_{DC}, operation at 10% higher-than-allowed power factor is tested by applying power factor step-changes at $t \in \{4\,\mathrm{s}, 6\,\mathrm{s}, \ldots, 18\,\mathrm{s}\}$ instants. Consequently, short-term alterations in reactive power amplitude are seen. While AC terminal current and voltage waveforms are unaffected, as seen in the zoomed-in areas, converter cannot operate permanently in these points. At over-the-limit power factor (see (6.24)), differential SMC energy cannot be balanced anymore, leading to capacitor voltage divergence between FB and HB SMs and ultimately converter failure.

Fig. 6.13 illustrates H-MMC operation limit in more details, for a single operating point, arbitrarily chosen as $k_{DC} = 0.5$. Power factor $\cos(\varphi_s)$ increase above the maximally permitted value $\cos(\varphi_s)_{max}$ violates constraint (6.24), meaning the converter is not inherently balanced anymore. This results in an immediate deviation in SMC differential energies, which is of permanent character, as we have not returned to the safe operating area (see **Fig. 6.9**).

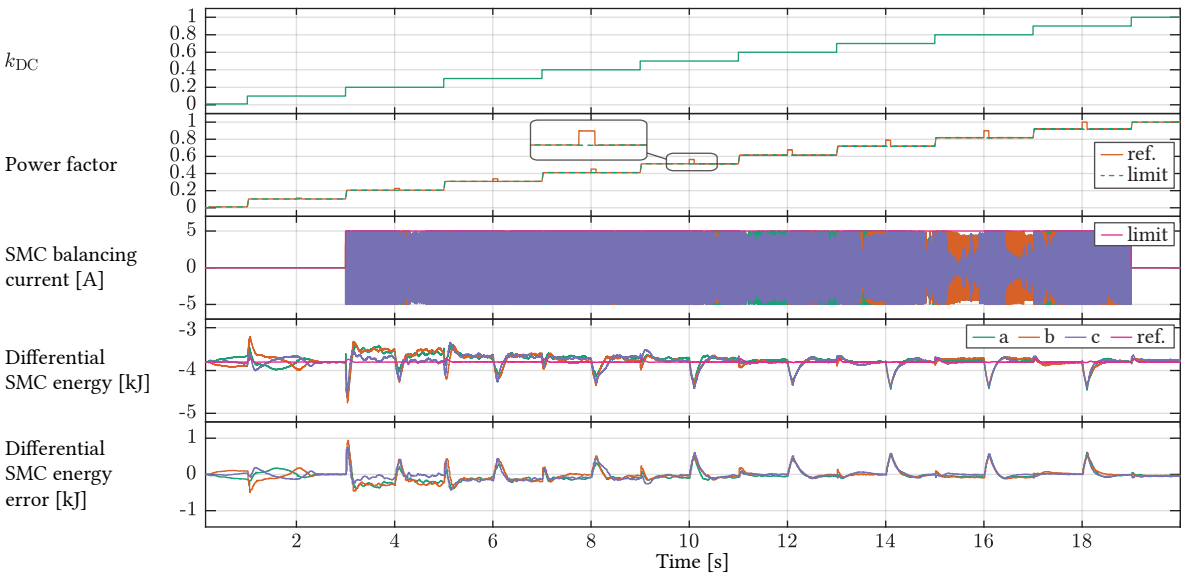


Fig. 6.11 SMC balancing action for the second test scenario. Differential energy divergence is seen successfully controlled after each k_{DC} step. However, power factor alteration above the limit causes sharp SMC energy deviation, at $t \in \{4\,s, 6\,s, \dots, 18\,s\}$ instants. Operation in prohibited area would thus quickly drive the converter out of operation by overcharging FB- and fully discharging HB SMs, or vice versa. One can notice power factor deviation at $k_{DC} = 0.1$ has no impact, as this is the area of FB-only operation capability (see **Fig. 6.9**).

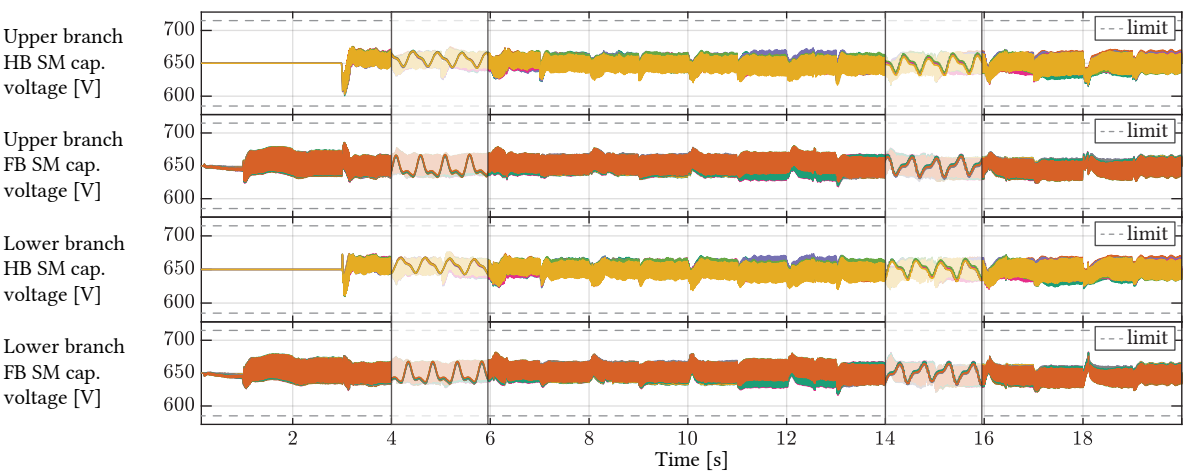


Fig. 6.12 Instantaneous voltage of individual capacitors belonging to one phase-leg is presented. Effects of the short-term alterations of power factor beyond the limit, at $t \in \{4\,s, 6\,s, \dots, 18\,s\}$ instants, are compensated by the SMC controller, as shown in **Fig. 6.11**. This figure demonstrates that the SM voltages remain mutually balanced under all scenarios.

Inter-SMC balancing corrective action cannot handle such a permanent imbalance, thus average capacitor voltages of HB and FB SMCs quickly deviate out of normal operation limits. Gradual discharge of HB SMs and overcharge of FB SMs follows, ultimately leading to converter control failure.

6.4.3 Constant-torque machine start-up

As converter limits of operation have been presented and verified, the last test scenario presents H-MMC in its intended application – variable speed PHSP. Synchronous machine start-up sequence, according to the PHSP control presented in **Sec. 4.2** is tested under the rated torque, from standstill to the rated speed. Operation sequences of the grid- and machine-side stages are provided in **Fig. 6.14** and **Fig. 6.17**, respectively.

DC link voltage reference is kept in proportion to the machine stator frequency, ensuring constant amplitude of the dominant SM capacitor energy ripple, as derived in **Sec. 3.2.1**. Both machine torque and DC current are kept at constant, rated, values. Sum- and differential capacitor voltage ripples are kept well within the limits, at approximately constant amplitudes over the entire speed range. Machine is operated at unity power factor, while grid-side reactive power reference follows H-MMC demand during the reduced DC voltage operation. Both active and reactive power references are tracked correctly. It can be noted that reactive power demand of the presented control method does not require higher-than-rated apparent converter power, thus no current overload exists.

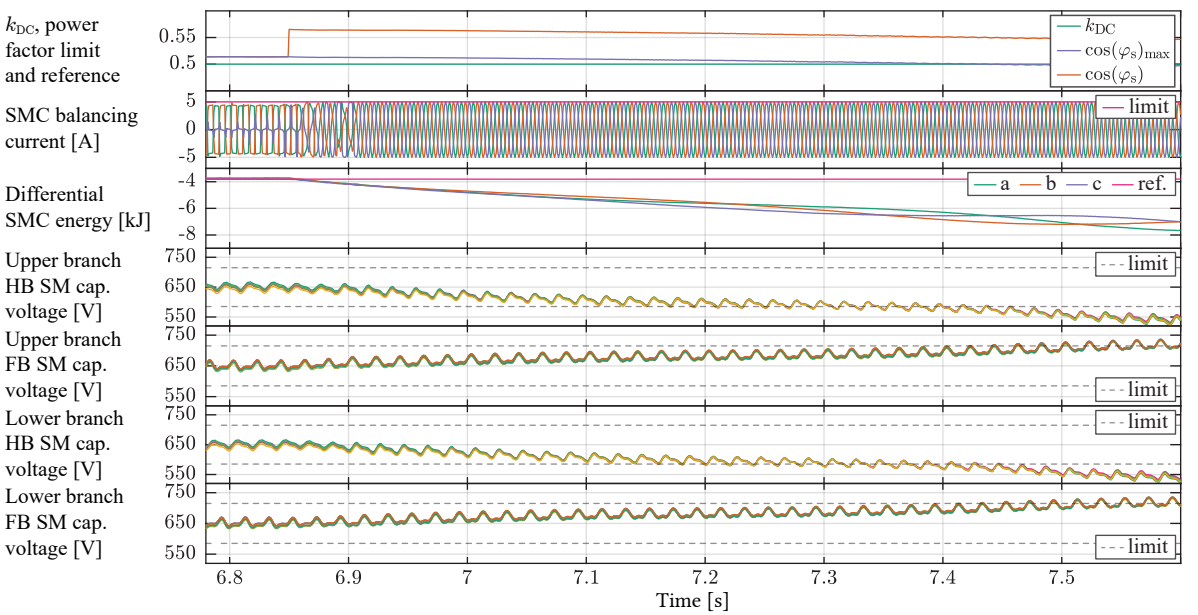


Fig. 6.13 A more severe case of the second test scenario is presented, for $k_{DC} = 0.5$. In this case, power factor $\cos(\varphi_s)$ is augmented 10 % above the maximally allowed value $\cos(\varphi_s)_{max}$ for the operating point, violating (6.24) and resulting in continuous deviation of SMC energies beyond balancing action corrective capacity. Average capacitor voltages of HB and FB SMs cannot be controlled, ultimately resulting in converter operation failure.

The capacitor voltage deviation in the machine-side MMC remains well withing the limit of ±10% regardless of the machine operating frequency. This confirms theoretical considerations presented in **Sec. 3.2.1**, and demonstrates the ability of the proposed converter configuration to enable CM voltage-free variable speed operation of the PHSP, along with other ancillary services.

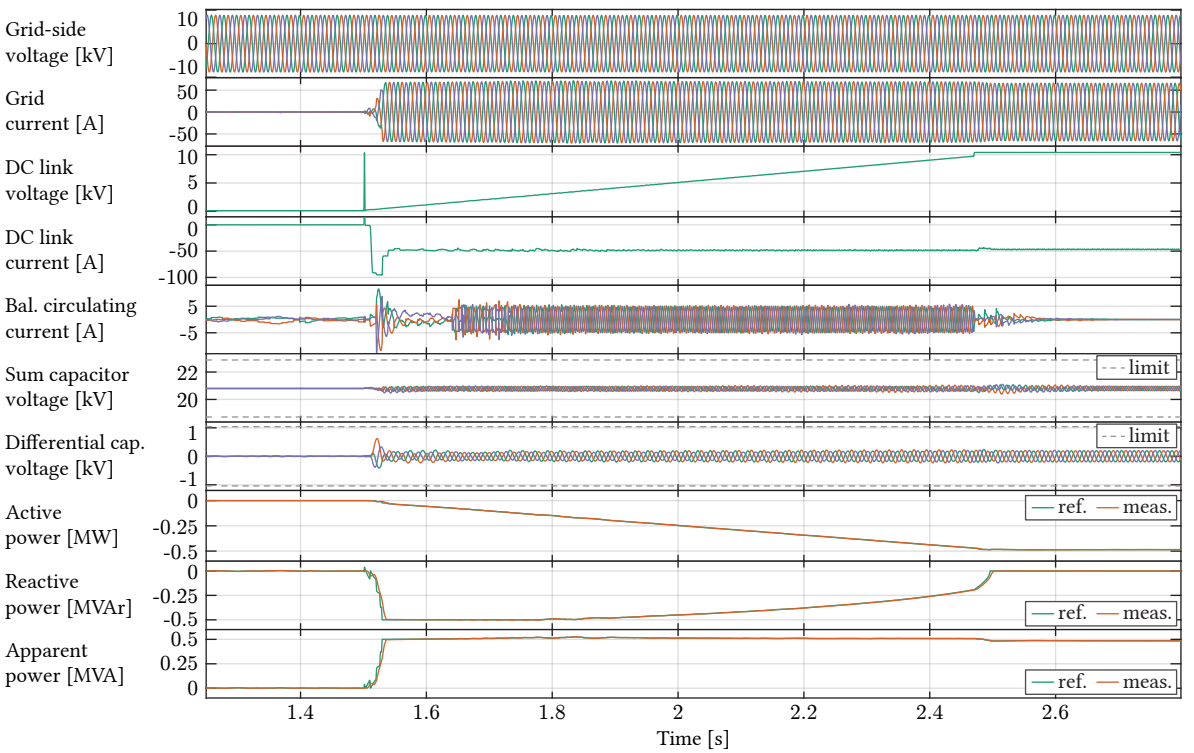


Fig. 6.14 Grid-side operating sequence of H-MMC in a PHSP application is presented, for machine start-up sequence. DC voltage reference is changed in proportion to the machine stator frequency, while under such conditions DC current is constant due to the constant machine torque.

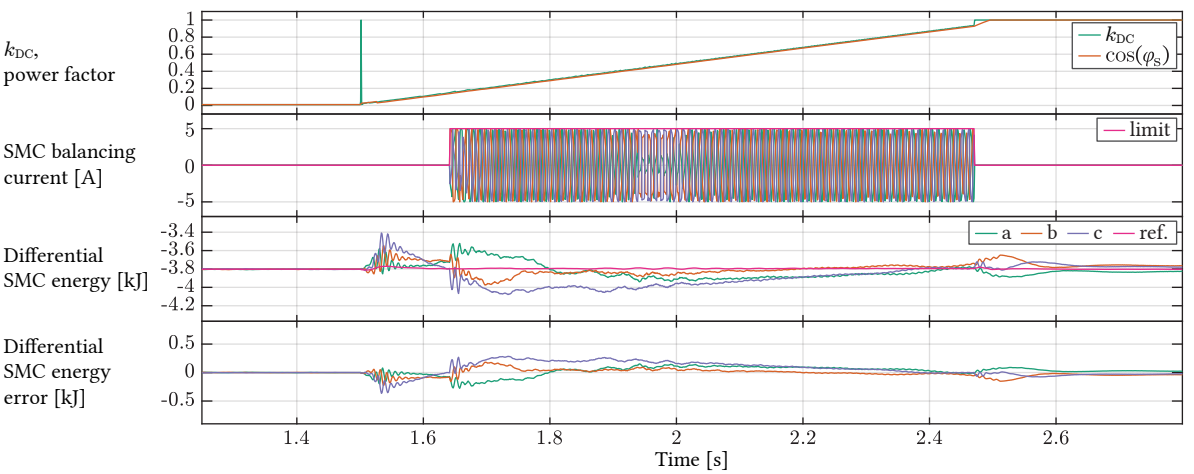


Fig. 6.15 SMC balancing action for machine start-up test sequence is presented. Differential SMC energy deviation is even lower due to linear rise in k_{DC}, unlike step changes seen in the previous test scenarios. Controller error converges to zero.

SMC balancing action is presented in **Fig. 6.15**. Compared to step-change in k_{DC} of the previous scenarios, here the energy deviation is even lower, thus capacitor voltage deviations between FB and HB SMCs are even smaller. Individual capacitor voltage levels are well within ±10% limit, seen in **Fig. 6.16**.

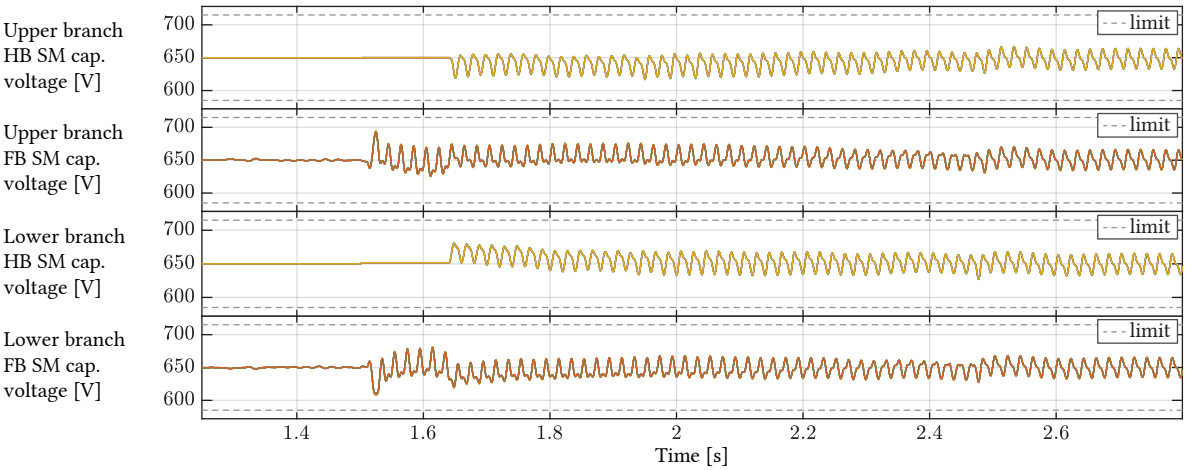


Fig. 6.16 H-MMC capacitor voltage ripple of individual SMs during rated-torque machine start-up sequence. As in previous test scenarios, values are kept well within the ±10% limit.

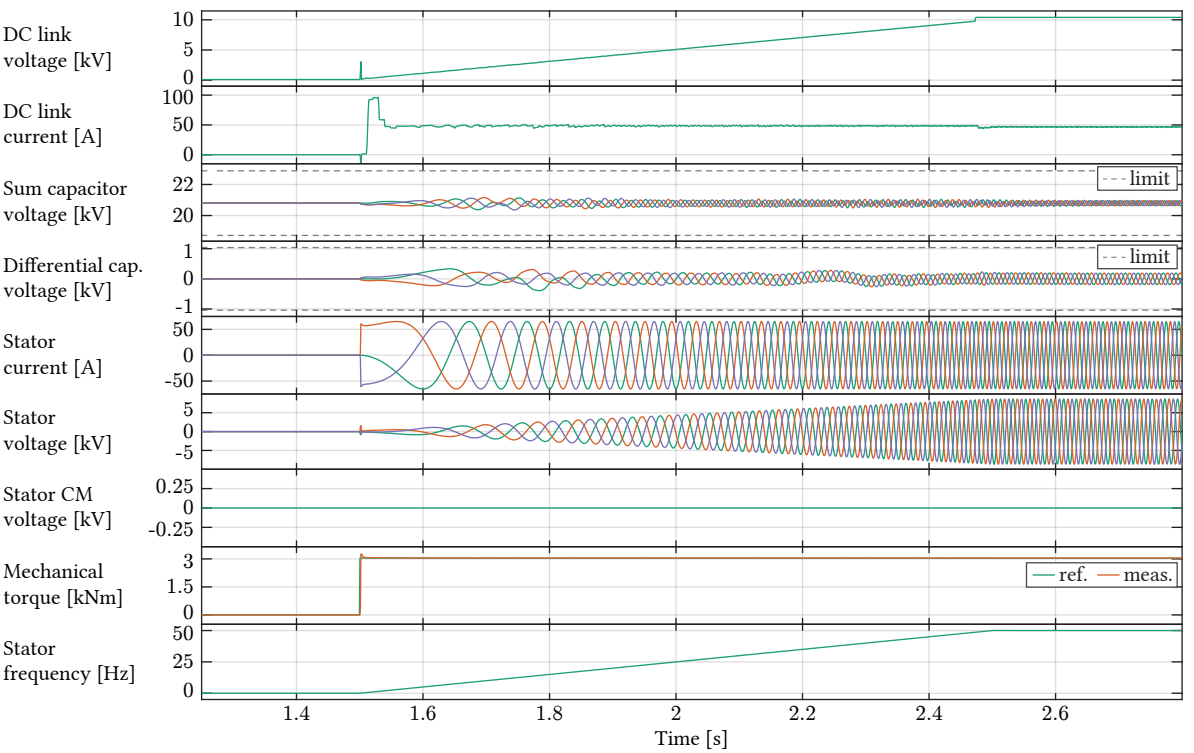


Fig. 6.17 Machine-side MMC operating sequence during machine start-up at rated torque. DC voltage is changed in proportion with the output (stator) frequency, thus approximately constant voltage ripple is ensured throughout the entire frequency range, without additional control action involving CM voltage injection.

6.5 Discussion of the results

The developed H-MMC control method relies on HB and FB SMC insertion voltage determination that yields inherent energy balance among the SMCs within each branch, while inheriting conventional MMC energy balancing loops. An additional inter-SMC energy balancing path ensures transient stability. Certain current capacity is required for such a control action, which was limited to 10 % of rated branch current in test scenarios.

Trade-offs of the method can be evaluated through comparison to relevant published methods. Lower FB/HB share for zero-to-rated DC voltage operating range is achieved compared to [67], at the price of higher power factor reduction towards the grid. Higher FB/HB share (62 % against 50 %) is required compared to [41]. Unlike [41], grid can be supported by reactive power under reduced DC link voltage without branch current overload, as grid current component is equally shared between the branches.

Compared to the method presented in **Chap. 5** [82], where 56 % FB share enables down to 50 % DC link voltage reduction at unity power factor, the alternative method proposed within this chapter achieves down-to-zero DC voltage reduction with only slightly higher FB share (62 %), but with obligatory grid-side power factor reduction, thus compromising the grid-code compatibility. At slightly lower FB share (50 %), method of [68] enables the advantage unity power factor operation down to 40 % of rated DC link voltage. However, method for further reduction is not offered.

With respect to some relevant high-voltage-DC-oriented methods [69], [71], it is not possible to form a fair comparison, as they assume operation under boosted AC modulation index, which is not of interest in the observed PHSP application. The two methods,[69] and [71], utilize additional first- and second-order circulating current components, respectively, as the primary means of energy balancing among the FB and HB SMs, while the second-order circulating current is only used as a corrective measure in the newly proposed solution. The method published in [72] imposes lower FB SM share (50 %) for the same down-to-zero DC link voltage range, at higher power factor compared to the method presented here. The method, in turn, requires additional second-order circulating current injection for proper balancing. The amplitude of additional circulating current is the highest for high power factor operation at low DC link voltages.

6.6 Summary

Utilizing the same hardware setup as in the method of **Chap. 5**, CM-voltage-free machine-friendly I-MMC is presented, operating at variable DC link voltage thanks to H-MMC AFE stage. The resulting PHSP variable-speed-retrofit solution thus requires no additional work on the machine, mechanical and hydraulic systems.

A novel H-MMC design and control method has been presented and demonstrated on the reference medium voltage MMC used throughout the thesis (**Tab. 5.2**), with 16 SMs per branch. The attainable operating region in terms of DC voltage reduction and maximal power factor in each of the operating points have been presented for each possible share of FB and HB SMs. Further analysis was performed with $N_{\mathrm{FB}} = 10$, $N_{\mathrm{HB}} = 6$ hardware configuration, as it can achieve zero-to-rated DC voltage operating range, with minimal FB count. The developed generalized iterative design approach is based around optimization criteria of minimal FB SM share, and is valid for arbitrary converter ratings and SM count.

Building on conventional MMC control, additional inter-SMC balancing layer has been added and discussed in details. Newly introduced control layers have been verified through a set of high-fidelity simulations of representative test scenarios. Firstly, normal operation of AFE stage has been presented. Further, theoretical limits of operating area were verified. Finally, start-up sequence of the reference 6 kV, 0.5 MVA synchronous machine has been presented, under rated torque operation. CM voltage-free machine supply is demonstrated over the entire operating range, ensuring full compatibility of the proposed solution with the existing fixed-speed PHSP units considered for retrofit.

The developed method offers reduced DC link voltage operation in an arbitrary range, with minimal share of FB SMs, and low additional balancing current requirement. H-MMC-based back-to-back drive does suffer from higher losses compared to the standard HB-based MMC, but offers CM-voltage-free machine operation in return.

Compared to the other relevant methods, including the method presented in **Chap. 5**, reduced FB SM count and very low additional balancing current requirement come at the price of reduced grid-side power factor range at lower-than-rated machine speed. A design trade-off between FB/HB share and power factor range can be chosen within the provided design stage.

7

Summary, Overall Conclusions and Future Works

The closing chapter aims to provide an overview of the thesis scope and motivations, followed by a discussion of the main contributions to the scientific community. Finally, opportunities for future research activities based on the presented work are proposed.

7.1 Summary and contributions

This thesis is focused on high-power medium-voltage AC-AC power conversion employing I-MMC topology, with a specific motivation to offer scalable, machine-friendly solutions for retrofit of existing fixed-speed PHSPs to highly-flexible variable-speed operation.

The work is motivated by a steady shift that can be observed in the power systems – an ever-increasing share of RES, combined with the stochastic nature of their power output, is altering the well-known typical daily load curve of the power system. On the other hand, power systems were historically developed as a balanced mix of the constant-power-output base generating units, energy storage facilities in the form of large PHSPs, typically in the range of 100 MVA to 1 GVA, and the various fast balancing plants, e.g. gas or hydro. Large variations in power demand between the daytime and the nighttime periods were balanced against constant generation power output through nighttime absorption and daytime generation of electrical energy by the large PHSPs units. Smaller energy balance deviations were, in turn, handled by the various fast balancing units. The profitability of a PHSP relied on this fact, which became an important aspect during the electricity market deregulation some decades ago.

Higher flexibility in terms of ancillary services offered to the grid, as well as faster response to the transients, can be achieved through variable speed operation of the PHSPs. This results in higher profitability of such plants, and was one of the incentives for the first variable speed units, based exclusively on DFIMs. Variable-speed-operated PHSPs units could thus offer a way forward for both the plant owners, in terms of high-enough profitability under today's power system and the electricity market circumstances, and to the power systems, through provision of the faster-response energy storage facilities, reducing the required share of spinning reserve in the system.

Regardless of the benefits to variable speed operation of the PHSPs, the vast majority of the installed units are still being operated as fixed-speed WRSMs directly connected to the grid. The work within this thesis provides a multitude of solutions to the retrofit of these existing fixed-speed units into the variable-speed-operated ones, without modification to the existing electrical machines, by inserting an I-MMC between the machine and the grid-side transformer. In such retrofit applications, where

the machine is originally designed for rated frequency equal to that of the grid, there is so far only one installed unit in operation, utilizing limited-scalability topology and consequently additional voltage-matching transformers.

I-MMC is identified as a highly-scalable topology that can decouple two equal-frequencies AC systems. Voltage amplitude of the machines found in large PHSPs, operating in the range of 6 kV to 20 kV, can be easily offered by the MMC. Regarding the power (current) amplitude scalability, analysis of industrially used SM ratings, performed in **Chap. 1** reveals that higher-current-rated SMs, or the parallel connection of lower-current units, is necessary to cover the power range of interest, i.e. 80 MVA to 400 MVA. I-MMC decouples the machine from the grid, thus hydraulic- and electrical systems' dynamics are decoupled in transient conditions as well. Plant reaction time to steps in active or reactive power demand are in such a way no longer dependent on the reaction times of the hydraulic circuit; rather, inertia of the machine can be utilized as a flywheel to provide fast transient response.

Machine operation at rated torque, over the entire frequency range, enables fast transients between pumping and generating operating modes, without de-watering. However, LF MMC operation at rated machine torque, without significant oversizing of the SM capacitors, requires topology-specific control system modifications of the machine-side MMC stage. This in general requires either an additional CM voltage component for converter energy balancing over the LF region, or operating the converter with DC link voltage reference varying from zero to the rated value as a function of the output frequency. The widely-adopted solution for the low-loss HB-SM-based MMCs is the CM-voltage-based technique. Such a solution has been implemented and validated for grid-code compatibility in **Chap. 3**.

While the newly-built machines can be designed specifically for VSD operation, retrofit applications are limited by the design of the existing units, intended for sine-wave grid voltage operation. Presence of CM voltages with amplitudes up to half the rated DC link voltage proves to be prohibitively high when supplying such machines. Starting from the same converter ratings and SM count as in the CM-voltage-injection-based solution (**Chap. 3**), a CM-voltage-free reference design and control system have been implemented in **Chap. 4**. To supply the machine-side stage with zero-to-rated DC link voltage amplitude, without violation of the grid code under both normal and faulty operating scenarios, AFE stage is realized as a FB-based MMC. While being both machine-friendly and grid-code-compliant, this solution comprises 50 % of FB SMs in the entire converter, resulting in higher initial cost and converter losses.

The main contributions of this thesis are the two control- and design methods, proposed in **Chaps. 5** and **6**, aiming at the reduction of FB SM share in the AFE stage of the I-MMC designed for PHSP application. In both of the approaches, the reference design of **Chap. 4** serves as the starting point. Replacement of a portion of FB SMs by the HB units, with modifications to the control system, leads to different trade-offs in the performance of the resulting design. In both cases, AFE stage is realized with a mix of HB and FB SMs in each branch, and thus named H-MMC.

The newly proposed control- and design methods are constrained to PSC-PWM modulation, suitable even for the low SM count; such a result can be seen in designs with relatively high SM voltage with respect to the machine rated voltage. Further, equal upper- and lower-branch current stress is assured in the methods.

Without violating the grid-code constrains for any operating point, the first proposed control- and

design method is presented in **Chap. 5**. Branch-level AC and DC insertion voltage references are split between the HB and FB SMCs, and altered twice per fundamental period, to equalize to the extent possible active power of energy exchange between the AC and the DC terminals for both of the SMCs. However, the method still introduces a certain inherent imbalance in energy exchange with AC and DC terminals of both HB and FB SMCs. The energy balance is achieved through additional second-harmonic voltage- and circulating current components. These produce zero-average energy exchange in interaction to the existing voltage and current components within the branch. However, they enable energy exchange between the HB and FB SMCs within each branch, while their effect is not visible at the terminals. DC link voltage reduction down to 50 % of the rated value is achieved, leading to 50 % reduction in CM-voltage stress to the machine in the LF region. The corresponding design method is valid for arbitrary DC link voltage reduction ratio.

Relying on the same topology as in **Chap. 5**, another novel H-MMC AFE control- and design method has been developed, prioritizing zero-CM-voltage-stress to the machine over the grid-code compatibility. Starting from branch-level AC and DC insertion voltage reference, HB and FB SMC references are generated, such that the desired branch-terminal voltage is synthesized, while SMC energy balance is inherently guaranteed. Maximal utilization of the HB SMs, without the violation of the electrical limits is firstly ensured. Unlike in the previously presented method, AC voltage reference phasors of the SMCs within each branch are phase-shifted, and the amplitudes modified, such that a certain power of energy exchange is achieved between the SMCs. The AC voltage components' angle- and amplitude modifications are performed in such a way to not alter terminal values. Since the converter is inherently balanced in this way, only a corrective energy balancing action is required between the SMCs. The same second-harmonic method is used as presented in **Chap. 5**, however at significantly lower required power amplitudes.

This method (**Chap. 6**) enables down-to-zero DC link voltage reduction and consequently CM-voltage-free operation of the machine. Full compatibility to the existing machines in fixed-speed PHSPs is achieved at the similar share of FB SMs compared to the method of **Chap. 5**. While the grid-code-compatibility is not retained in lower-than-rated frequency range, the developed design method offers a trade-off between the grid-side power factor range and the FB SM share. In the light of the nature of PHSP operation, the plant is operated at or just below the rated speed most of the time. As grid-side power factor limitation is the smallest around the rated frequency, this could be a tolerable trade-off.

7.2 Overall conclusions

The transition to RES-dominated power systems of tomorrow must be backed by an equally sharp increase in the share of highly-flexible grid-scale energy storage systems. While we are witnessing the advancements in migration of the historically smaller-scale energy storage systems, like batteries, to the grid-scale levels, existing PHSPs are currently offering by far the highest volume of energy storage capacity. A highly-scalable I-MMC, with H-MMC-based AFE stage for reduced cost and losses, offers a plug-and-play retrofit solution for conversion of the existing fixed-speed PHSP units to variable-speed operation, and support the power system evolution in a sustainable manner. This thesis provides novel design- and control methods aimed at addressing this issue, but the findings are also applicable to the other applications of medium-voltage high-power conversion.

In parallel to the efforts of converting the existing fixed speed PHSPs to the variable speed operation, new plants are also being built. In a design process of PHSP initially considered for variable speed

operation, there is naturally a liberty to arbitrarily choose both machine and converter characteristics. Designing a PHSP with different machine- and grid rated frequencies enables the use of D-MMC for interface to the grid, as a more efficient solution than I-MMC in such a scenario. The first such project is currently under way in Austria (**Sec. 1.2.3**). The use of D-MMC in retrofit applications, however, would require a redesign of the machine. Thus, either the D-MMC or the novel H-MMC-based solutions presented in this thesis can prove more beneficial, depending on the application.

7.3 Future works

The presented work has covered converter scalability estimation, design and control method development stages of a H-MMC for PHSP retrofit applications. Thereby, some opportunities for future work on the topics can be explored, as outlined here.

7.3.1 Switching frequency reduction

The control methods presented in the thesis comprise PSC-PWM, and the SMs switch at 1 kHz, ensuring a high-quality waveform at the terminals, even at lower SM-count. Such a choice is made to ensure compatibility of the models within the thesis with the industrial control system used for the medium voltage converter prototype being developed in the PEL, consisting of low-voltage SMs. In high-power applications, such a switching frequency can be prohibitively high. The use of different modulation schemes, e.g. optimized pulse patterns, may yield better results in terms of overall efficiency, while still satisfying the grid-code-imposed limits. Thus, the use of H-MMC for PHSP, with alternative modulation schemes, or PSC with reduced switching frequency, can be addressed.

7.3.2 Reduced SM reference voltage operation

As some studies propose, instead of addressing the cause of prohibitively high SM capacitor voltage ripple in the LF region, an alternative approach may be to ensure that the maximal instantaneous capacitor voltage ripple does not exceed the electrical design limit. In the LF region, since the insertion voltage amplitude requirement is lower, this can be performed through reduction of SM reference voltage amplitude, leaving more headroom for increased capacitor voltage ripple, as published by other researchers. As the grid-code-compliant H-MMC-based method presented in **Chap. 5** employs reduced-CM-voltage injection for reduction in SM capacitor voltage ripple, thus still stressing the machine to some extent, the method could be modified by further reducing the CM voltage action, while implementing reduction in SM reference voltage value.

7.3.3 Real-life efficiency comparison

The novel H-MMC-based solutions have been studied from the control- and design perspectives. A study on efficiency of these methods against the reference FB AFE-based solution, for a real-world daily- or weekly operating sequence of a variable-speed PHSP could contribute to a more fair comparison of the methods.

7.3.4 De-rated operation in case of SM loss

As an inherently scalable topology, an MMC can typically be designed with certain redundancy in case of SM loss due to fault. While such an approach invariably increases the initial price of the

converter, it can reduce down-times, and in turn increase the income of the plant. With an estimation of SM reliability and losses in case of unplanned maintenance downtime, a choice on the level of redundancy can be made. In case of no redundancy provided by design, or in a situation where more SMs fail, strategies for continued operation under de-rated performance can be assessed.

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