EPFL

Thèse n° 9042

Hard and Soft Switching Losses in Power Converters: Role of Transistor Output Capacitance

Présentée le 28 mars 2022

Faculté des sciences et techniques de l'ingénieur
Laboratoire de dispositifs semiconducteurs de puissance
Programme doctoral en génie électrique

pour l'obtention du grade de Docteur ès Sciences

par

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École polytechnique fédérale de Lausanne

2022

Truth is the daughter of time.

To my mother…

Acknowledgements

My journey towards getting a PhD degree has not been an easy task. It has been challenging, both mentally and physically. The five years at EPFL has taught me that the journey, ultimately, is a test of your willpower and the support you get along the way, nothing else.

First, I would like to thank my thesis supervisor, Professor Elison Matioli, for giving me the opportunity to carry out my doctoral studies at EPFL and putting his trust in me. Thank you for your support and guidance throughout my studies. I'm grateful to the jury members of my doctoral examination for their time in assessing my doctoral work, and their valuable insights and recommendations. The appreciation I received for my thesis from you is very important to me, and I regard it very highly. I thank the president of the jury, Professor Farhad Rachidi-Haeri from EPFL, the external experts Professor Marian Kazimierczuk from Wright State University, Ohio, U.S.A, and Dr Thiwanka Wijekoon from Huawei Technologies, Germany, and the internal expert Professor Drazen Dujic. I'm thankful to EPFL for supporting me throughout my studies and financing my research work. I also thank the Swiss Office of Energy (SFOE) for providing important financial support for my research work as well as for the betterment of our research lab.

Muriel, I'm deeply indebted to you for all the support you gave me during my initial settlement in Switzerland; and your support did not stop there. You helped me with matters even outside of EPFL till the very end. I thank all the Powerlab members for their support during various stages of my studies.

I must mention a few additional words about the jury members of my doctoral examination. I'm grateful to Professor Drazen Dujic for his support during my stay at EPFL. Every time I had a question, whether technical or about my career, you were very quick to meet with me and provide guidance. I'm also lucky to get to know Professor Farhad Rachidi-Haeri. Not only you were the president of my doctoral examination but you also helped me with several technical questions I had during my third year of studies. Prof. Kazimierczuk, I'm grateful to you for the detailed comments and corrections on my thesis; they helped me to improve my thesis before its final publication. And Dr Wijekoon, thank you for the encouragement and all the advice.

I'm also grateful to Professor Mario Paolone for being the president of my candidacy exam as well as for his wonderful and cheerful engagement as the advisor of the EPFL hyperloop team.

I'm thankful to Dr André Hodder, Sylvain Robert, and Dr Stéphane Burri for their kind technical advice and support during various stages of my studies. I especially thank Pietro Bianco for his invaluable technical support. Pietro, your level of service and kindness are such a rarity. I would also like to thank my students Jessy Ançay, Linda Ösmon, Nicolas Bollier, Enea Figini, Bruno Kola, and Simon Aquarone. Thank you all for giving me a chance to work on my teaching and supervising skills.

I'm forever grateful to my colleague and friend Georgios Kampitsis. You helped me through a

very challenging time when I was doubting myself. You believed in me and your moral support was instrumental to pass those hurdles. The same goes for my friend Armin Jafari. Your company was invaluable to me to get through the final stages of my PhD. I would also like to thank my friends Giovani and Ilaria for all the good times we had together and for always getting us exceptionally good food. Luca, thank you for all the technical and non-technical discussions we had together. I'm also thankful to Remco, Katya, and Jun for their cheerful support during various stages of my work.

One of the best things that happened to me during my stay at EPFL was being part of the EPFL Hyperloop team (2017–2018). I will never forget the time we spent together, both in Lausanne and Los Angeles. I would like to thank the whole team, with special thanks to Simone, Milena, Linda, and João. Simone, whenever I needed help, you were there; your friendship made my life in Switzerland much easier. Milena, thank you for being a really good friend and helping me to preserve my sanity. Linda and João, thank you for all the good memories and your support.

I would also like to acknowledge my lifelong friends Kasun, Hiranya, and Amali. Your constant communication, although you live in three different countries, has helped me more than you can imagine. I'm grateful to my good friends Kamalaruban Parameswaran and Nuwan Liyanage for their continuous support and advice, especially during the final year of my studies.

I'm also grateful to my first power electronics teacher Professor Sunil Abeyratne and my second power electronics teacher Professor John Salmon.

Finally, I would like to thank my mother, my father, my sister, and my brother-in-law. I cannot thank you enough for everything you have done for me.

*Lausanne, 21.03.2*022 Nirmana Perera

Preface

Since the industrial revolution, a myriad of machines were invented, commercialized, and then used to do one task, which can be put under the following umbrella ideology: the betterment of human society and creation of solutions that make everyday life easier. Electric power, and consequently, modern-day power processing has been an integral part of this ideology, shaping the technical advancements in many fields.

At the time of writing this thesis (the year 2022), the world has faced a far bigger challenge than this ideology. The EU-wide existing ambition for 'The 2030 climate and energy framework' is the following [1] (verbatim from the source):

- At least 40% cuts in greenhouse gas emissions (from 1990 levels)
- At least 32% share for renewable energy
- At least 32.5% improvement in energy efficiency

To make this a reality, power processing now has a very timely task ahead. Consequently, *power electronic converters* need to see a significant increase in their performance within a very short amount of time.

This thesis work was not initially undertaken with this as an ideology. The work was undertaken purely on its scientific merit. But I hope it aids, in some way, to achieve this important goal as the thesis presents important insights on the energy losses in power converters.

Nirmana Perera,

Lausanne, Switzerland.

(March 2022)

Abstract

Hard and Soft Switching Losses in Power Converters:

Role of Transistor Output Capacitance

by

Nirmana Perera

To best utilize power converters, a sound understanding of the relationship between the circuit topology and the power-semiconductor-device characteristics is required. This is especially important in high-frequency switching, where device parasitics start to largely interfere with the circuit. In this regard, the parasitic-output-capacitance of power devices plays a vital role in the losses of the system, which affect both the efficiency of the circuit and the system volume. This thesis studies the characterization of output capacitance as well as its interaction with power electronic topologies at a fundamental level and presents important insights, underlining limitations in the conventional knowledge on the subject.

The thesis shows that the analysis of output-capacitance-related losses should be treated based on the type of switching employed, as the circuit-level effect of the output capacitance is different in soft- and hard-switching topologies. For both cases, it is highlighted that the charge-versus-voltage curve of device output capacitance provides the most complete information of its behaviour. First, the correct measurement methods to identify output capacitance losses for soft-switching operations are analysed and validated. Then, it is shown how a fundamentally different charge–discharge mechanism in device output capacitance takes place in hard-switching operation (in contrast to soft-switching), and a new measurement approach is devised to quantify the related loss. These measurement methods are then used to evaluate output-capacitance losses of commercially available Si, SiC, and GaN power transistors. The developed concepts are taken a step further and utilized to separately evaluate gate- and driver-related losses in driving a transistor undergoing zero-voltage-switching. The technique is then used to identify the performance limitations of HF and VHF gate-driver ICs. Finally, consolidating the ideas developed throughout the thesis, an experimental case study is provided for a soft-switching converter.

We conclude that output capacitance is a critical device feature that should be considered in high-frequency converter design and be given the same level of attention as device on-resistance

in the design stage of a device. We believe this is instrumental to the progress of modern power converters—especially, ones based on emerging wide-bandgap devices—towards their fullest potential.

Keywords: calorimetry, charging, class-E inverter, co-energy, discharging, energy loss, electrical measurements, gallium nitride (GaN), gate driving, gate loss, hard switching, hysteresis, no-load circuit, no-load loss, output capacitance, silicon (Si), silicon carbide (SiC), soft switching, power converters, power loss, resonant converters, switching, switching energy, switching loss, wide-bandgap (WBG) devices.

Résumé

Pertes de commutation dure et douce dans les convertisseurs de puissance:

Rôle de la capacité de sortie du transistor

par

Nirmana Perera

Afin de mieux utiliser les convertisseurs de puissance, une compréhension approfondie de la relation entre la topologie du circuit et les caractéristiques de composant à semi-conducteur de puissance est nécessaire. Celle-ci est particulièrement pertinente dans les cas de commutation à haute fréquence, où les effets parasites provenant du composant commencent à interférer de manière conséquente avec le circuit. A cet égard, la capacité de sortie parasite des composants de puissance joue un rôle crucial dans les pertes du système, en affectant à la fois l'efficacité et le volume du circuit. Cette thèse étudie la caractérisation de la capacité de sortie aussi bien que son interaction avec les topologies d'électronique de puissance à un niveau fondamental et présente des informations importantes mettant en avant les limites des connaissances conventionnelles sur le sujet.

Cette étude montre que l'analyse des pertes liées à la capacité de sortie doit être traitée en fonction du type de commutation utilisé, car l'effet de la capacité de sortir au niveau du circuit est différent dans les topologies à commutation douce et dure. Dans les deux cas, il est mis en évidence que la courbe charge-tension de la capacité de sortie du composant fournit les informations les plus complètes sur son comportement. Tout d'abord, les méthodes de mesure correctes pour identifier les pertes de capacité de sortie pour les opérations de commutation douce sont analysées et validées. Ensuite, il est montré comment un mécanisme de charge–décharge fondamentalement différent dans la capacité de sortie du composant se présente lors d'une opération de commutation dure (contrairement à la commutation douce), et une nouvelle approche de mesure est conçue pour quantifier la perte associée. Ces méthodes de mesure sont ensuite utilisées pour évaluer les pertes de capacité de sortie des transistors de puissance Si, SiC et GaN disponibles dans le commerce. Les concepts développés sont ensuite approfondis et utilisés pour évaluer séparément les pertes liées à la grille et au driver lors du fonctionnement d'un transistor subissant une commutation à tension nulle. La technique est également utilisée pour identifier les limitations de performances des circuits intégrés de driver pour la grille à HF et VHF. Enfin, consolidant les idées développées tout au long de la thèse, une étude de cas expérimentale est fournie pour un convertisseur à commutation douce.

Nous concluons que la capacité de sortie est une caractéristique essentielle du composant qui doit être prise en compte dans la conception du convertisseur de haute fréquence et doit recevoir le même niveau d'attention que la résistance à l'état passant du composant lors de la phase de conception. Nous pensons que cela joue un rôle déterminant dans la progression des convertisseurs de puissance modernes, en particulier ceux basés sur des composants émergents à large bande interdite, vers leur plein potentiel.

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Part I

1 Introduction

1.1 New Challenges in Power Conversion

Power processing, or *power conversion*, is ubiquitous in modern-day tasks. This is facilitated by *power electronic converters*. Some classic applications are ac/dc adapters for portable devices, computer and telecom power supplies, uninterruptible power supplies, 400-Hz power systems in aircraft, audio amplifiers, and industrial motor drives.

During the past two decades, the power electronics industry has gone through a substantial change. The automotive industry has seen significant use of power electronics with the introduction of electric vehicles (EV), invigorated by Tesla Motors [2]. At the same time, motivated by the timely need for renewable energy sources, photovoltaic and wind energy power conversions have been moving forward with increased participation from both academia and the industry [3]. The trend is finally fuelled by the emergence of wide-bandgap (WBG) semiconductor devices,[1] paving the way for increased efficiency in existing power converters as well as for new solutions that were not possible with silicon (Si) power devices [4–6].

The early predictions with the adoption of WBG devices for power converters saw silicon carbide (SiC) devices contributing to the high-power and high-voltage (650 V to 3.3 kV) applications, such as photovoltaic systems, transportation, EV charging and heavy machine drives [7]. Gallium nitride (GaN) devices, on the other hand, were understood to spread into applications below 600 V, targeting

[1] We will not go into the details of the impressive material properties of WBG devices as they have been discussed extensively in modern literature. One good starting reference would be the book 'GaN transistors for efficient power conversion' by Alex Lidow et al. [4].

medium-power applications, but achieving significantly higher switching frequencies—approaching, and going beyond, 1 MHz. Some original focus applications of GaN were in the markets of portable adapters, telecom, and wireless charging [7]. As GaN devices have seen unprecedented growth in the past few years, they are now also being aimed at applications such as audio amplifiers, energy storage, solar inverters, on-board chargers (OBC), and dc-dc converters for data centres [7, 8]. For example, in 2021, several commercial mobile-phone manufacturers such as Baseus, Anchor, Aukey, and Belikin had made available mobile-phone-chargers incorporating GaN devices. Furthermore, it is believed that the latest 140-W USB-C power adapter from Apple used GaN power devices.[2]

The modern power electronics industry, propelled by new applications and rapid growth of WBG devices, face a timely and very important challenge in moving towards greener electronics and sustainable power industry. This means that the energy efficiency limits are and should not only be limited by the monetary factors, but also by the timely need of sustainability goals. Several important challenges need to be overcome in this regard.

1. WBG devices are still in the early development phase in comparison with their theoretical performance limits. Pushing them to their theoretical limits requires solving existing limitations in the device technologies and the performance of passive components.
2. Si power devices have asymptotically reached their theoretical limits [4], and further improvements in them are quite limited. However, WBG devices are still in the acceptance stage for many other applications. To see a commercially viable adoption with sustainability goals in target, power converters based on WBG devices need to be extremely energy efficient.
3. In terms of power electronic topologies, it is unlikely a disruptive topology would come forth with unprecedented energy gains. Since the basic topologies, as well as modulation techniques, had been invented alongside the advancement of Si devices, the general trend so far has been the incremental improvement of existing topologies. It is an open question if these improvements can answer the above-mentioned challenge.
4. One side of the energy optimization has been severely impeded by the magnetics [9], which are an integral part of the temporary energy storage in many commonly used converter topologies. The energy efficiency improvement in this aspect is heavily dependent on advancements in magnetic materials.

Finding answers to these questions is a global challenge. In this thesis, we discuss several important aspects in the switching process of modern power converters that could shed light on finding answers to some of the above-mentioned challenges. We do this by focusing on the interactions between the main constituents of a power electronics solution.

1.2 Power Electronic Circuits and Power Semiconductor Devices

Figure 1.1 shows an example of a simple power electronics solution. At the system level, a converter (such as the shown buck converter) or a collection of converters work in unison to achieve a given power processing task. A single converter can be considered from a component level approach: generally, this is the level at which a power electronics engineer carries out a converter design. Two approaches for active-device utilization can be observed: use of discrete devices (separate power devices and separate

[2] Based on online details on the breakdown of the device carried out by third parties.

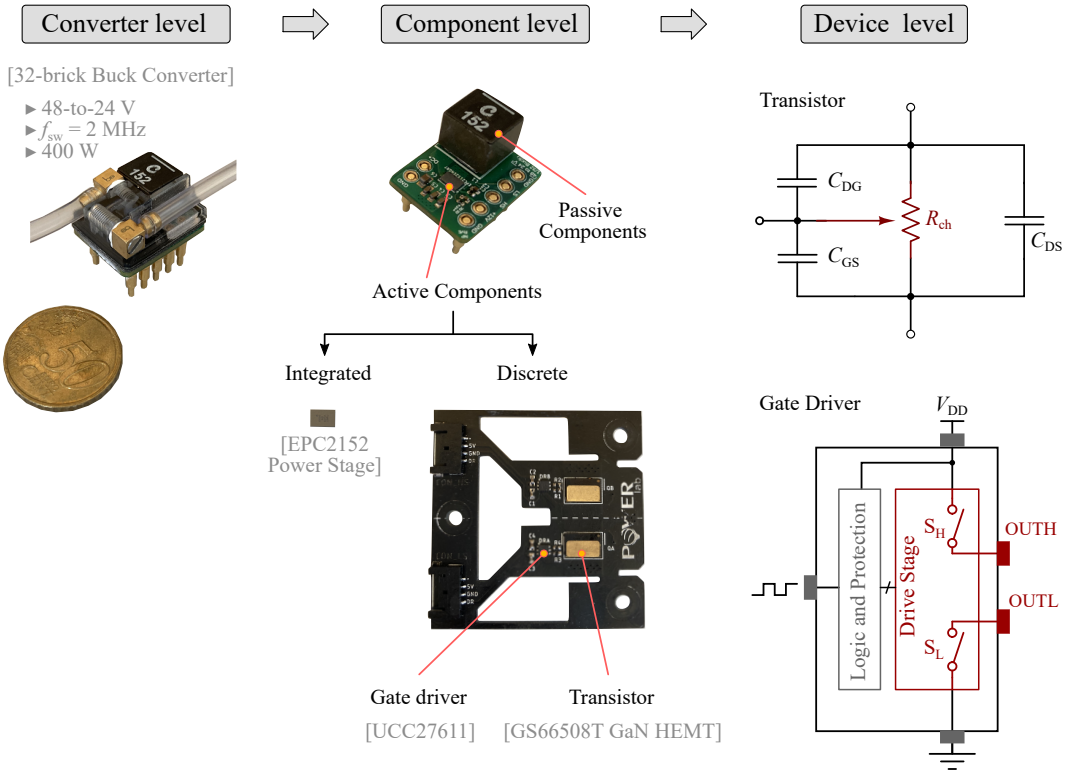


Figure 1.1: A power electronics system can be described from three different levels: converter level, component level and device level.

gate drivers) or use of integrated power modules (power device and the gate-driver integrated to a single chip, or even a half-bridge with integrated drivers, such as the shown EPC2152 module). Finally, the components can be looked at from a device level, to identify their individual performances and limitations.

For primary design purposes, in general, a power electronic converter can be described as a collective interaction of three main constituents: topology, switches (active devices), energy-storage components (passive devices). Control and modulation can be included in the category of topology. Then, there are three secondary constituents, which need to be considered for the practical operation of the converter: packaging, thermal management, and electromagnetic interference and compatibility (EMI and EMC) considerations [4].[3] These secondary constituents, in essence, can be considered as remedies to undesirable by-products of the original solution.

As illustrated in Figure 1.2, the interaction between the main constituents can be simply expressed as topology being linked to the active and passive devices with the switching frequency. An improvement in the main constituents will yield fundamental and high-value benefits, which will, in turn, minimize requirements for certain secondary constituents. The emergence of WBG devices, and the consequential shift of the switching frequency into the MHz range, has resulted in a breakthrough advancement in the active devices and has caused a disruptive shift in the converter technology. Therefore, the nature, the rules, and the limitations of the interaction between the main constituents have changed; and they need to be fully understood and explored to achieve the full potential of converters

[3] The ideas were given in the Foreword done by Dr Fred C. Lee on the referenced book.

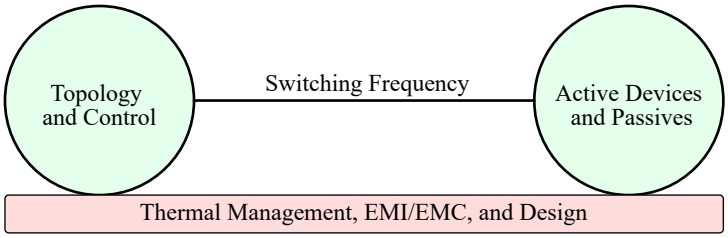


Figure 1.2: A power electronic converter can be identified as an interaction between devices (active and passive) and the topology (and its control) linked by the switching frequency. The final converter solution is supported by cooling and EMI/EMC solutions based on application requirements.

based on WBG devices.

Figure 1.3 shows how much power (y-axis) is lost due to the energy loss (x-axis) in a switch during a single switching cycle, for different switching frequencies. The energy loss could be due to the conduction or switching of the power device; it could also represent the total gate-driving energy loss. For example, the switching-energy losses range between a few nanojoules up to several hundreds of microjoules for 30-A 650-V power devices [10]. For Si devices with the same ratings, the corresponding gate-driving energy losses could easily go beyond five hundred nanojoules. The important point to note here is that the active device is not solely responsible for these losses; the loss is a combination of three factors:

1. Characteristics of the active device (e.g., ON-state resistance and parasitic capacitances of a power device)
2. Circuit (e.g., topology, control, and modulation)
3. Operational conditions (e.g., load current, temperature)

The final loss is the result of the interaction of the above three factors; this is the measured loss. In our early efforts, to address one or a few of the main challenges outlined in Section 1.1, we have identified

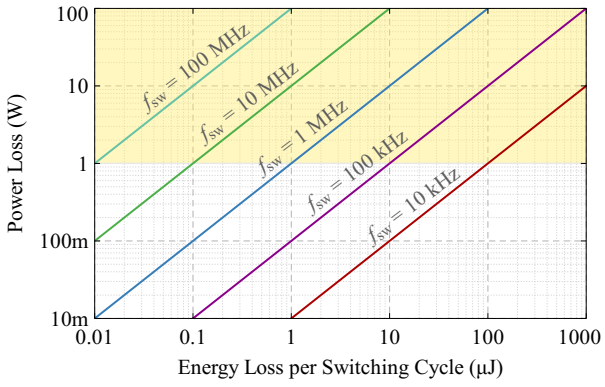


Figure 1.3: How an energy loss related to a single switching cycle translates to a power loss at different switching frequencies (f_{sw}). The area shaded in yellow corresponds to a power loss greater than 1 W. In practical operating conditions, switching losses in a power device range between a few tens of nanojoules to several hundreds of microjoules. For hard-switching converters operating at 100 kHz, losses could easily go beyond 10 W when the switching energy is several hundreds of microjoules. The same can be stated about soft-switching converters operating beyond 10 MHz when their OFF-state loss (discussed in Chapter 4) is around 1 microjoule.

the parasitic output capacitance (C_o) of a power semiconductor device and its relation to the switching circuits as an important and timely scientific endeavour. We outline the general reasoning for this as follows.

- WBG devices have the potential to push both hard- and soft-switching frequencies to unprecedentedly high levels. However, this will yield substantial power losses if the switching energy is not controlled. As switching events are tightly coupled with the output capacitances of power devices, a better understanding of them is required to make WBG solutions energy-efficient in high-frequency (HF) and very-high-frequency (VHF) operations.
- Topology and control have an important role in controlling the energy losses in active devices. Understanding the relationship between the topology and active devices from a fundamental level will help derive better energy-efficient solutions.
- Magnetic-less topologies [11, 12] are one possible solution to the hindrance caused by the losses in power magnetics. In these topologies, ceramic capacitors, as well as device capacitances, are utilized for temporary energy storage purposes, with the least involvement from magnetics. In the switching process, the device capacitances are charged and discharged, resulting in energy losses, which are functions of both the topology and the power device.

1.3 Motivations

In line with the general challenges outlined previously, here, we introduce the specific scientific problems that motivated the research work in this thesis. The points introduced below are discussed in each chapter of Part 2 of this thesis, with a detailed background review.

Recent interest in the device output capacitance of power FETs was triggered by the observation of certain unexpected losses in soft-switching converters by Fedison, Fornage, Harrison and Zimmanck in 2014 [13]. The target devices were silicon super-junction (Si-SJ) devices. This work was followed by an additional work in 2016 by Fedison and Harrison [14], where these losses were understood to be from a *hysteresis loss* related to the *large-signal behaviour* of the output capacitance of a power field-effect transistor (FET). The authors utilized a technique called the *Sawyer–Tower* circuit to measure these large-signal losses. The claims by the authors were further strengthened by the findings of Roig and Bauwens in 2015, where a device-level analysis showed similar non-idealities in the output capacitance of Si-SJ devices [15]. Our initial investigations were motivated by these findings. At this juncture, it should also be mentioned that, during the thesis work, we have come to notice research efforts by other groups,[4] motivated by the same findings. We appreciate these efforts as they were helpful to cross-check our results and progress, as well as to generate additional insights.

For soft-switching operation, the above-mentioned initial research works focused only on a few select Si-SJ devices and their performance. But no useful categorization or discussion of similarities and dissimilarities between different device technologies were present.[5] Moreover, the voltage dependence of output-charge versus voltage (QV) curves were not investigated broadly.[6] We believe this will provide

[4] For example, the works by the Stanford University group [16–18], by Bura et al. [19], and by Miftakhutdinov [20].

[5] The recent works by Zulauf et al. [17], Bura et al. [19], and Guacci et al. [21], which were published in 2018, conducted experiments on GaN and SiC devices. But the results were limited to only a few devices, and no comparisons within the technologies were given.

[6] The later work by Zulauf et al. [22] analysed additional devices of different device technologies with quantitative details on hysteresis losses. However, our focus was on identifying important qualitative relationships between different device technologies and families [23].

useful insights in identifying the root causes of output-capacitance hysteresis losses. By looking at *QV* patterns we aim to answer the following questions. During which voltage range does the hysteresis pattern emerge? Or does the hysteresis loop have a linear relationship with voltage? And how do patterns change between different semiconductor technologies?

In the highly-cited 2009 work by Perreault et al., a small-signal parameter R_{oss} was mentioned as a displacement loss mechanism in the device output-capacitance branch. Then, in the 2014 publication by Fedison et al. [13], it is mentioned that R_{oss} is not suitable to characterize large-signal hysteresis losses. However, to the best of our knowledge, there had been no comprehensive evaluation of this parameter and its limitations to be used as a figure-of-merit for large-signal hysteresis losses. We also aim to shed light upon this.

After the discoveries by Fedison et al. in 2014 (discussed earlier), the initial focus was mainly on the soft-switching performance of devices. No special attention was given in follow-up studies to the effects the circuit topology has on the charge–discharge process of device output capacitance. Especially, the hard-switching performance was not given attention. On the one hand, with the emergence of WBG devices, the hard-switching operation has moved into the regime of several hundreds of kilohertz, and even, a few megahertz [24]. On the other hand, the role of output capacitance in hard-switching operation is not understood comprehensively in the literature: the existing analytical equations on switching losses are either misleading [25] or quite complex, and hence fail to provide a simple understanding. Furthermore, it is not clear if the large-signal *QV* curves related to hard-switching operation would be similar to the ones obtained under soft-switching conditions. These points mark some of the most important problems addressed in this thesis.

In hard-switching circuits and most of the soft-switching circuits, the gate-driving circuit operates in hard-switching conditions: this is termed as 'hard-gating'.[7] This process involves charging and discharging the output and input capacitances of driver transistors, while the gate of the external power device is turned ON and OFF. These driver transistors are expected to sink and source peak-currents of several amperes at each switching event. Furthermore, to best utilize WBG power FETs in high-power-density applications, these switching events need to be repeated at very high frequencies [26], which could incur non-negligible power losses related to gate driving. So far, there has been no conclusive investigation on the driver switching losses. Moreover, the value of the utilized gate charge ($Q_{\text{G-ZVS}}$) in zero-voltage-switching (ZVS) operation[8] of a power FET is different to its counterpart in hard-switching ($Q_{\text{G-HS}}$). Although some reports mention $Q_{\text{G-ZVS}}$ [27], no details are provided as to the means of its determination. It is important to note that $Q_{\text{G-ZVS}}$ is not given in datasheets, and the use of the $Q_{\text{G-HS}}$ is simply erroneous for ZVS operation. While trying to answer these questions, we also aim to provide additional insights on selecting a suitable combination of the gate-driver and power FET for MHZ-range ZVS circuits.

In our efforts to address the above-mentioned problems, several technical challenges were faced in the domains of analysis and experimental measurements. These challenges motivated additional investigations and resulted in further contributions. These are discussed appropriately in the corresponding chapters.

[7] Please see Section 6.2.5 for more details.
[8] Please see Section 3.2 for the definition and more details.

1.4 Thesis Contributions

The main contributions of the thesis are listed below.

- Analysis of large-signal behaviour of transistor output capacitance for soft-switching operation.
  - A detailed technical investigation on the Sawyer–Tower technique is carried out: important usage recommendations and the limitations of the technique are discussed.
  - Characterization of the output-capacitance losses of Si, SiC, and GaN power FET families using the Sawyer–Tower technique.
  - Based on *QV* patterns, it is shown that different device structures (even for the same semiconductor technology) exhibit different dependencies on excitation voltage levels, resulting in diverse C_{o}-hysteresis patterns.
  - Identifying the usability of the small-signal parameter R_{oss}.
- Identifying the fundamental role of device output capacitance in creating hard-switching losses.
  - The fundamental topological difference between hard-switching and soft-switching is highlighted.
  - Introducing the capacitive co-energy concept and its relation to the charging process of a capacitor.
  - Presenting an energy-based approach to describe the contribution of the device output-capacitance in hard-switching topologies. It is shown that when a device is fully hard switched during its turn-ON process, a fixed energy loss is incurred in the device channel equal to $Q_{\mathrm{o}} \cdot V_{\mathrm{dc}}$.
  - Development of a straightforward measurement technique to obtain large-signal *QV* curves for FETs under hard switching.
  - Demonstrating that, for a given device, neither the small-signal values nor the large-signal behaviour in soft-switching operation does not necessarily correspond to the large-signal behaviour in hard switching.
- Revisiting gate-driving losses: separate evaluation of the switching losses related to the output-stage of the gate-driving circuit and the gate capacitance of a power FET.
  - Analytical presentation of the important difference between the gate charge values related to a FET subjected to hard-switching and zero-voltage-switching conditions.
  - Distinguishing between two independent loss components in gate-driving: gate-loss related to a power FET and the switching loss the chosen gate-driver, where the latter is related to the output and input capacitances of the two transistors in the output stage of the driver. An experimental technique is developed to evaluate these two loss components for a given driver-transistor combination.
  - Performance evaluation of state-of-the-art gate-driver ICs and experimental calculation of $Q_{\mathrm{G\text{-}ZVS}}$ of commercial power FETs (for Si, SiC, and GaN technologies).
  - It is shown that for GaN devices with small current ratings, the switching loss of the gate-driver can dominate the total gate-driving loss. It is suggested that additional loss optimizations should focus on the driver's output stage rather than the power device.

- Experimental evaluation and accurate breakdown of active-device losses in a resonant power converter.
  - First in-circuit demonstration and measurement of output-capacitance hysteresis losses in a converter under actual operation.
  - Development of an experimental method with mW-level precision to perform an accurate breakdown of active-device losses in a converter. Four components are evaluated: transistor ON-state loss, transistor OFF-state loss, transistor gate loss, and charge–discharge losses related to the internal capacitances of the gate-driver.

1.5 Thesis Organization

The thesis material is organized as follows.

Part 1 serves as a general introduction to this thesis, providing background information on the main content provided in Part 2. Part 1 consists of three chapters.

Chapter 1 details the problem definition followed by the motivations and thesis contributions. **Chapter 2** provides a detailed review of the concepts related to device output capacitance. In relation, the chapter also establishes important terminology and definitions related to device output capacitance, providing clarification on certain concepts that are either loosely defined or overlooked in the technical literature. **Chapter 3** introduces important concepts and terminology related to the switching process in power electronic converters.

Part 2 consists of five chapters, where the first four chapters present the main contribution of this thesis. The final chapter concludes the thesis.

Chapter 4 discusses the hysteresis loss in the output capacitance of field-effect transistors and its adverse effects on the performance of soft-switching converters. **Chapter 5** explores the relationship between device output capacitance and hard-switching losses. **Chapter 6** studies the gate-driving process of power FETs, with an especial focus on the losses in the output stage of gate driver ICs. **Chapter 7** provides an important case study with a class- E inverter, incorporating the material presented in the previous chapters. **Chapter 8** concludes the thesis by summarizing the presented work and giving insights on possible future directions.

2 Thematic Overview: Output Capacitance, Charge, and Energy

THIS chapter serves as a prelude to the main content of this thesis. First, a general background on the output capacitance of a field-effect transistor is given. Relevant definitions and terminology are also presented, with added discussions where necessary. We also introduce charge- and energy-based definitions related to the output capacitance of a power transistor. We conclude by emphasising why the interaction between the output capacitance and the power electronic topology is an important event in switching power circuits.

2.1 Basic Concepts and Terminology

In this subsection, we introduce basic concepts related to the output capacitance of a field-effect transistor. This aids the analysis of subsequent circuits with much clarity. We also aim to establish proper and meaningful terminology to avoid any confusion that might arise from different terminology found in the technical literature on the subject.

2.1.1 Device Parasitic Capacitances

The standard representation of the parasitic capacitances of a field-effect transistor is given in Figure 2.1. The three terminals of the device are marked as the gate (G), drain (D) and source (S). Three main parasitic capacitances are defined concerning the three terminals of the device [28–30]:

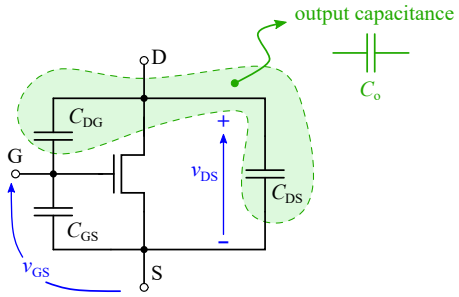


Figure 2.1: A model of a field-effect transistor (FET) with its parasitic capacitances: gate–source capacitance (C_{GS}), drain–gate capacitance (C_{DG}), and drain–source capacitance (C_{DS}). The output capacitance is defined as $C_o = C_{DG} + C_{DS}$ (i.e., the parallel combination of C_{DG} and C_{DS}): generally, C_o is defined for a shorted gate–source connection.

1. C_{GS}: gate–source capacitance.

2. C_{DS}: drain–source capacitance.

3. C_{DG}: drain–gate capacitance.

All the three symbols (C_{GS}, C_{DS}, C_{DG}) used here are generic notations that refer to actual physical capacitances, irrespective of the type of excitation used to measure them.

2.1.2 Input, Output, and Reverse-Transfer Capacitances

In actual circuit operation, the three parasitic capacitances mentioned above, generally, operate in combination. In this regard, a meaningful representation of device parasitic capacitances is given as follows [29].

1. Input capacitance (C_i): the parallel combination of C_{GS} and C_{DG}.

$$C_i = C_{GS} + C_{DG} \tag{2.1}$$

2. Output capacitance (C_o): the parallel combination of C_{DS} and C_{DG}.

$$C_o = C_{DG} + C_{DS} \tag{2.2}$$

3. Reverse-Transfer capacitance (C_r): equal to C_{DG}

$$C_r = C_{DG} \tag{2.3}$$

As with the previous set of definitions, C_i, C_o, and C_r used here are generic notations which refer to actual capacitances, irrespective of the type of excitation used to measure it. In most technical literature and device datasheets, these parameters are notated as C_{iss}, C_{oss}, and C_{rss}, with reference to a small-signal measurement method. We will discuss more on this and the meaning of using the additional subscript letters 'ss' in Section 2.2.1.

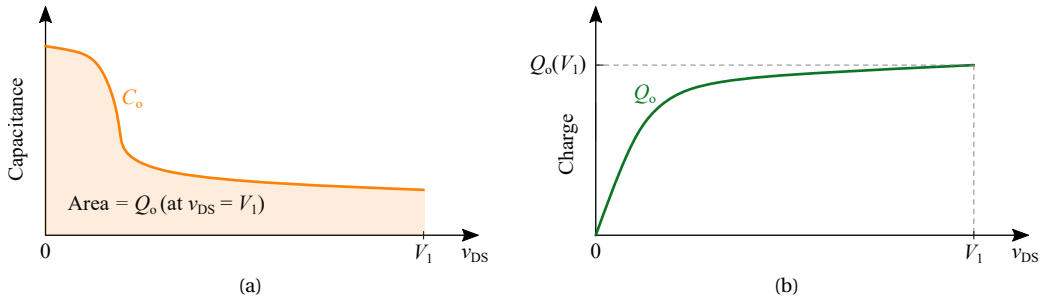


Figure 2.2: The main features of device output capacitance are characterized by its *CV* and *QV* curves. (a) Output capacitance C_o is a monotonically decreasing function of the transistor's drain–source voltage, v_{DS}. This is represented as a capacitance versus voltage (*CV*) curve. (b) The charge stored in C_o is referred to as the output charge (Q_o) of the device. For example, for $v_{DS} = V_1$, the stored charge is marked as $Q_o(V_1)$ or simply Q_o.

2.1.3 Output Capacitance and *CV* Curves

The output capacitance of a field-effect transistor is a *monotonically decreasing* function of the device's drain–source voltage, v_{DS}. This dependence can be noted as $C_o(v_{DS})$. However, for simplicity, we will only use C_o to denote output capacitance, where the dependence of v_{DS} is always implied.

The typical variation of C_o with v_{DS} for a FET is graphically illustrated in Figure 2.2(a). Such a plot is referred to as a *capacitance(C)-versus-voltage(V) curve,* or simply, a *CV curve.*

2.1.4 Output Charge and *QV* Curves

The output charge (Q_0) is defined as the charge stored in C_o for a given v_{DS} value V_1. This is calculated by taking the area under the *CV* curve up to V_1: this is marked as the area shaded in orange in Figure 2.2(a). Mathematically, Q_o can be expressed as

$$Q_o = \int_0^{V_1} C_o \, d v_{DS}. \tag{2.4}$$

The output charge is a *monotonically increasing* function of v_{DS}. A typical Q_o characteristic is then given by a *charge(Q)-versus-voltage(V) curve,* or in the abbreviated notation, a *QV curve.* A typical *QV* curve for a power FET is plotted in Figure 2.2(b). The value of Q_o at $v_{DS} = V_1$ is marked as $Q_o(V_1)$ or simply as Q_o.

2.1.5 Drain–Source Voltage

For our purposes in this work, the drain–source voltage of a FET is expressed as follows:

$$v_{DS} = V_{DS} + v_{ds}. \tag{2.5}$$

Here v_{DS}, V_{DS}, and v_{ds} refer to total instantaneous, dc, and ac components of the voltage across the drain–source terminals of the device, respectively. Concerning small-signal measurements,[1] V_{DS}

[1] Discussed in Section 2.2.

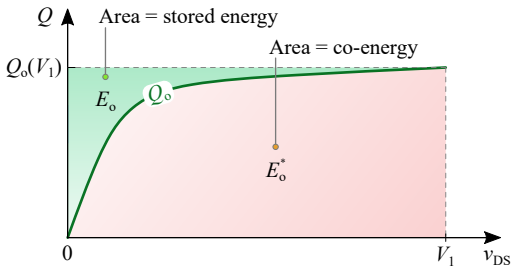


Figure 2.3: Definition of energy components related to output capacitance on a *QV* curve.

is used as the x-axis to denote the bias voltage when plotting capacitance or charge values against drain–source voltage. In large-signal excitations,[2] we use v_{DS} to convey the large and instantaneous nature of the excitation. In general, we will use v_{DS} as the x-axis for *CV* and *QV* curves.

It is important to note that output charge (Q_o) is generally given for a particular *maximum* value of drain–source voltage. When the circuit configuration is not specified, we will denote this maximum voltage as V_1 in this thesis—see Figure 2.2(b). For different circuit topologies, V_1 can be replaced as follows.

1. $V_1 = V_p$ is used to denote the peak voltage related to sinusoidal-type excitations with a dc offset. For example, in circuits like the Sawyer–Tower and class-E inverter.
2. $V_1 = V_{dc}$ is used when the maximum voltage is determined by a dc-link voltage, V_{dc}. For example, traditional PWM converters and resonant-transition converters (see Section 5.2.2 for additional discussions).

2.1.6 Stored Energy and co-Energy

A measure of the utility (or the non-utility) of output capacitance is the energy that can be stored in it for a given drain–source voltage. The *stored energy* of C_o is denoted as E_o and is marked by the area between the *charge* (Q)-axis and the curve of Q_o: with our definition for a *QV* plot, the *charge*-axis is the y-axis. The area under consideration is marked by the green-shaded-area in Figure 2.3 and is mathematically given as

$$E_o = \int_0^{Q_o} v_{DS}\, dQ, \tag{2.6}$$

Like both Q_o and C_o, the stored energy is a function of v_{DS}.

Another energy component can be identified in Figure 2.3 (area shaded in light orange): the area between the curve of Q_o and the *voltage(V)*-axis.[3] This is defined as the *co-energy* (E_o^*) of C_o and is expressed as

$$E_o^* = \int_0^{V_1} Q\, dv_{DS}. \tag{2.7}$$

A detailed discussion on the co-energy component is carried out in chapter 5.

[2] Discussed in Section 2.2.
[3] In our case, the *voltage* axis is the x-axis.

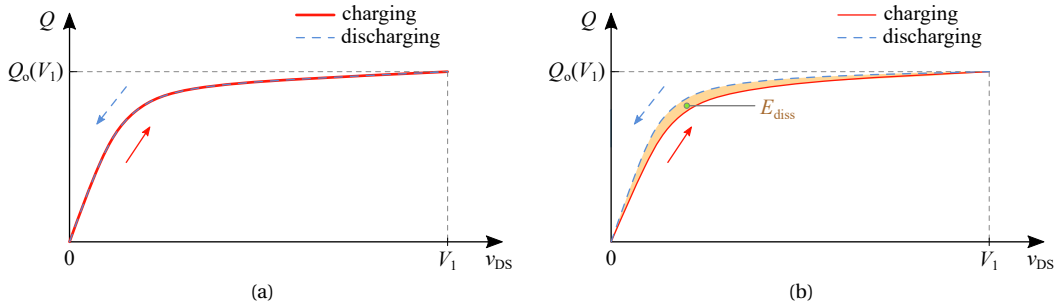


Figure 2.4: Charge and discharge paths in a *QV* plot. (a) Ideal charge–discharge behaviour of C_o, where paths coincide. (b) Non-ideal behaviour of C_o, with different charge–discharge paths resulting in a hysteresis energy loss, E_{diss}.

2.1.7 Hysteresis Energy Loss

One major topic of this thesis is the *non-ideal hysteresis-energy-loss* related to the output capacitance of a FET. In a switching power circuit, the device output capacitance is charged and discharged to a maximum voltage V_1 cyclically.[4] This *charge–discharge* process can be summarized on a *QV* plot. Figure 2.4(a) shows an ideal case where the charge (marked by solid red curve) and discharge (marked by the dashed blue curve) paths coincide. A non-ideal charge–discharge process is characterized by the non-coincidental paths as shown by Figure 2.4(b). The area between the two curves (marked by the area shaded in yellow) is representative of an energy loss related to the process and is termed *hysteresis energy loss*. We use the notation E_{diss} to represent this loss, where the subscript 'diss' refers to *dissipation*.

The hysteresis-energy-loss in C_o is a function of the maximum voltage (V_1) across the device's drain–source terminals and is expressed as

$$E_{diss} = \int_0^{Q_o} v_{DS}\, dQ - \int_{Q_o}^{0} v_{DS}\, dQ, \tag{2.8}$$

where Q_o is the charge stored in C_o at $v_{DS} = V_1$. As mentioned in Section 2.1.5, V_1 will be replaced by the symbols V_p or V_{dc} in the following chapters, based on the circuit topology. The related power loss for a given frequency f is expressed as

$$P_{diss} = f \cdot E_{diss}. \tag{2.9}$$

Also note that the main implications of E_{diss} concern soft-switching circuits (see Chapter 4); for hard-switching circuits, the energy losses are conveniently described by using stored and co-energy components (see Chapter 5).

2.2 Small- versus Large-Signal Excitation

Two distinct approaches could be used to measure parameters related to device output capacitance:

1. Conventional *small-signal* excitation approach that measures C_{oss}.

[4] The specific nature of this process is topology dependent. We will discuss these aspects as we progress through the content of this work.

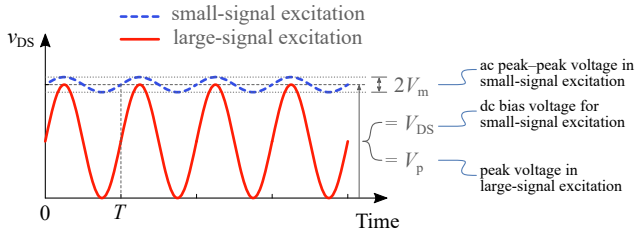


Figure 2.5: Small-signal versus large-signal excitations.

Table 2.1: Notation used in Device Datasheets for Small-Signal Quantities

Quantity	Notation related to small-signal methods
C_o	C_{oss}
Q_o	Q_{oss}
E_o	E_{oss}

2. Recently utilized *large-signal* excitation approach, which is used to evaluate Q_o, E_o, and E_{diss}.[5]

The difference between the two methods is summarized in Figure 2.5. We discuss the technical details of these two approaches in Section 2.3.

In device datasheets, the parameters related to device parasitic capacitances are given by what is known as *small-signal* values. In other words, the values are measured under (or derived based on) small-signal conditions. The quantities (related to output capacitance) introduced so far, and their respective small-signal quantities, (if applicable) are listed in Table 2.1.

2.2.1 Notation of Output Capacitance

At this juncture, we emphasize the importance of having a clear notation for the measured parameters. It is very important not to confuse the meaning of the subscript 'ss' in C_{oss} with the term 'small signal'.[6] In certain technical literature, the subscript 'ss' is sometimes understood as '**s**mall-**s**ignal'. This could be because datasheets report small-signal values for output capacitance, and the related values are denoted as C_{oss}.[7] To clarify this, here we provide the correct meaning of this subscript, with reference to the document ***International Standard Part 8: Field Effect Transistors (IEC 60747-8)*** by the *International Electrotechnical Commission (IEC)*[31].[8] [9]

1. C_{iss}: common **s**ource **s**hort-circuit input capacitance
2. C_{oss}: common **s**ource **s**hort-circuit output capacitance
3. C_{rss}: common **s**ource **s**hort-circuit reverse transfer capacitance

In all three cases above, the subscript 'ss' means '**s**ource **s**hort'.[10] However, it should be noted that all the measurements methods given for these three quantities in the document IEC 60747-8 are, in fact, small-signal approaches.

Based on these details, we use the following convention to avoid any confusion. Output capacitance is generally denoted as C_o when the measurement method (or the excitation type) is either

[5] For example, the Sawyer–Tower technique measures Q_o: then, based on the QV curve, E_o, E_o^*, and E_{diss} can be evaluated.
[6] Equally valid for Q_{oss} and E_{oss}.
[7] Alongside C_{iss} and C_{rss}.
[8] IEC 60747-8 ed 3.0 "Copyright © 2010 IEC Geneva, Switzerland. www.iec.ch". Pages 54–57. The content is reproduced here with permission from IEC.
[9] The author would also like to thank senior field application engineer Mr Bernd Riemann from Alpha and Omega Semiconductor (Europe) for guidance in finding this information.
[10] In addition, a parameter C_{ods} is defined as the common drain short-circuit output capacitance in the document, where the subscript 'ds' means '**d**rain **s**hort'.

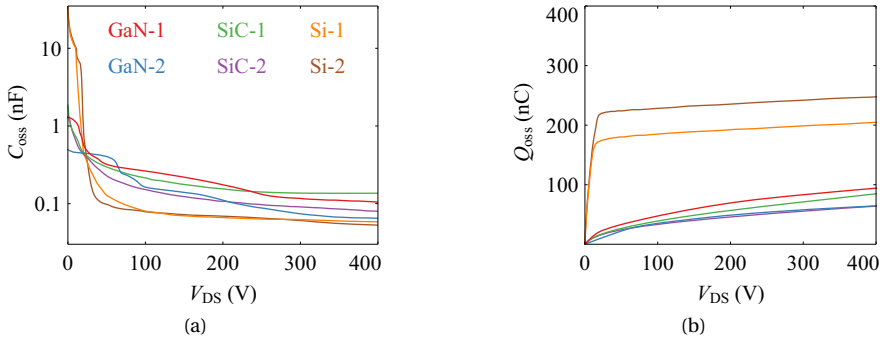


Figure 2.6: (a) C_{oss} and (b) Q_{oss} curves of several commercial power FETs (rated voltages and currents are between 650–900 V and 27–39 A, respectively). Note: the C_{oss} curves are extracted from the datasheet curves using a digitizer tool. The Q_{oss} curves were obtained by using Eq. (2.4) on the C_{oss} data.

not important or not mentioned. C_o is also used to denote the values measured under large-signal conditions. When the measurement is specifically done under small-signal conditions, we use the notation 'C_{oss}' to follow the convention used by the datasheets.[11] The same arguments apply to other relevant parameters.

2.2.2 Small-Signal *CV* and *QV* Characteristics

Figure 2.6 shows C_{oss} and Q_{oss} curves reported in the datasheets of several commercial power FETs: two examples, each from GaN, SiC, and Si technologies, are shown.

Generally, datasheets tend to provide a specific C_{oss} value at a large v_{DS} value, for example, at 400 V. This value is significantly small compared to C_{oss} values at lower voltages, such as 50 V and below. Therefore, a better approach is to utilize the complete C_{oss} curve to get a better estimate of its small-signal behaviour. It should also be noted that datasheets do not generally provide Q_{oss} curves, although, in recent years more manufacturers tend to include this plot as well.

An example is considered in Figure 2.7(a) where the small-signal *CV* curve for a GS66508T GaN HEMT is given. The values of C_{oss} at 0, 200, and 400 V are 493, 111, and 65 pF, respectively. This 65-pF value (at 400 V) is the one given in the electrical characteristics table in the datasheet. The value of Q_{oss} can be evaluated by taking the area under the C_{oss} curve up to 200 V as marked by the area shaded in orange. The Q_{oss} curve is plotted up to 400 V in Figure 2.7(b): the value at 200 V is 59 nC. The value of E_{oss} at 200 V is also marked in Figure 2.7(b) (equal to the area shaded in green).

The exact values of C_{oss} and the nature of *CV* curves are highly dependent on device structure and geometry [29]. Once a device is fabricated, C_{oss} is generally considered to be dependent only on v_{DS} for all practical purposes.[12] All three device parasitic capacitances also show negligible dependence on temperature [32].[13]

[11] With the acknowledgement that the subscript 'oss' refers to 'output', 'source', and 'short', respectively.

[12] The non-idealities that will be introduced later in Chapters 4 and 5 are generally discussed in relation to an output-capacitance *branch*, rather than just a capacitance. Under different excitation types and frequencies, the behaviour of the branch could vary, where we assume the capacitance itself stays unchanged. For example, the non-idealities can be lumped to a series inductance and a highly-nonlinear resistance (to account for *real* losses), which is dependent on both the frequency and the drain–source voltage.

[13] Measured under small-signal excitations.

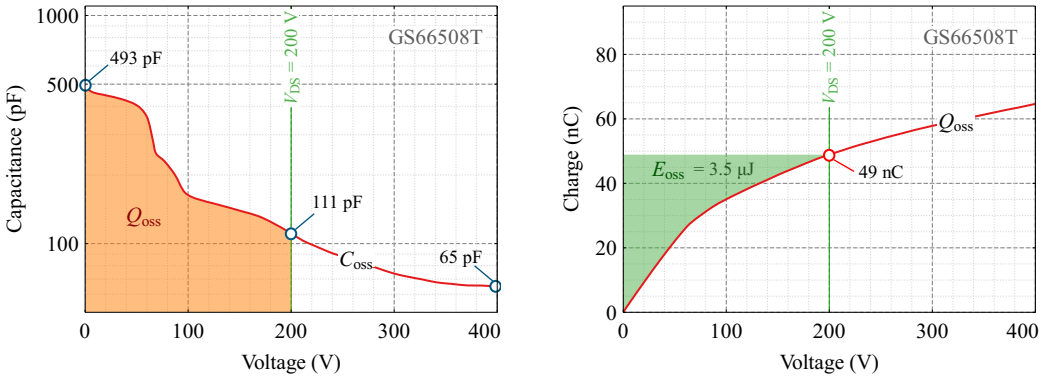


Figure 2.7: Calculation of the small-signal parameters Q_{oss} and E_{oss} from datasheet-based C_{oss} curves for a given V_{DS} value. A GS66508T (650-V and 30-A) GaN HEMT is considered (datasheet version: Rev 200402). (a) The area under the *CV* curve (area shaded in orange), up to a certain dc bias voltage on drain–source terminals, for example, V_{DS} = 200 V, gives the Q_{oss} for that voltage. (b) E_{oss} for a given V_{DS} is calculated by taking the area between the Q_{oss} curve and the y-axis (area shaded in green).

2.3 *CV* and *QV* Measurements

Here we briefly discuss the practical aspects of *CV* and *QV* measurements.

2.3.1 Small-Signal *CV* Measurements

As mentioned previously, the device data sheets provide a small-signal output capacitance, C_{oss}. Figure 2.8 provides a simple block diagram of the measurement process. In practice, generally, an impedance analyser or a power-device curve tracer is utilized for this measurement.

A small ac-perturbation-voltage, generally around 10–250 mV (RMS), over a dc bias voltage ($V_{DS,x}$) on the device under test (DUT). [33]. An excitation frequency (f) is selected: datasheets usually provide this for either 100 kHz or 1 MHz.[14] The gate–source terminals of the DUT are kept shorted (i.e., v_{GS} =0). The bias voltage is then swept from 0 V to a specified maximum V_{dc}. For example, if V_{dc} = 400 V and the step size is 2 V, the measurement will involve 200 steps. For each step, the measurement equipment calculates the impedance, from which the value of capacitance is extracted based on a specified capacitance model for each bias voltage. Then a C-versus-V_{DS} plot is obtained. A detailed discussion on the practical aspects of small-signal measurements will be given in Section 4.4.2.

2.3.2 Large-Signal *QV* Measurements

In contrast to small-signal measurements, large-signal measurements generally estimate C_o (or more often, Q_o) of a power transistor by subjecting the device to large excitation voltages, for instance, between 0 V and V_p = 400 V. This is graphically presented in Figure 2.9.[15] It can be noted that the ac variation 0–V_p is much larger than the ac variation $2 \cdot V_m$ in small-signal excitation (see Figure 2.8), for the same excitation frequency. As will be seen in chapter 4, such large excitations bring forth a

[14] We believe the reason for the choice is to minimize the effect of parasitic inductance on the measured value. We have also contacted some manufacturers to question this choice. Some informed us that this has been a convention and that the choice of one frequency, for example, 1 MHz, allows comparing their products with competitors.

[15] More details on this and the Sawyer–Tower circuit are given in Chapter 4.

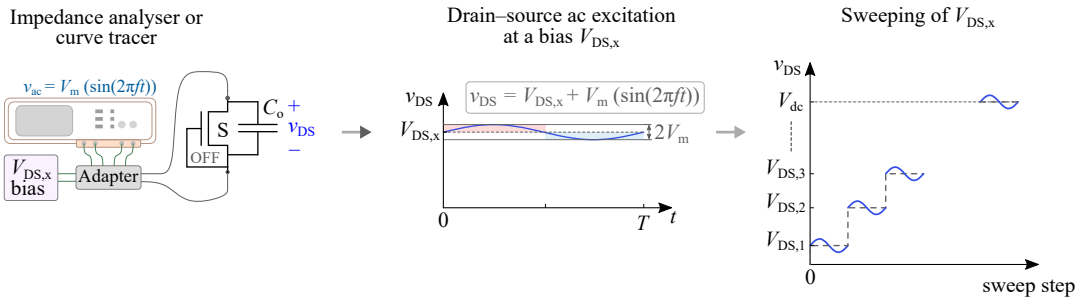


Figure 2.8: Performing *small-signal CV* measurements with an impedance analyser or a power device curve tracer.

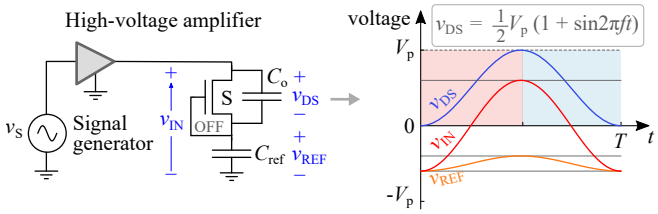


Figure 2.9: *Large-signal* excitation with the Sawyer–Tower circuit.

different behaviour for the output capacitance of certain power devices, which are not observable under small-signal excitations.

In the large-signal methods discussed in this work, the first result is usually a Q_o-versus-V_{DS} curve. Then the related large-signal output capacitance can be derived based on the standard equation for a capacitance C as follows:

$$i = C \cdot \frac{dv}{dt} \tag{2.10}$$

$$\frac{dq}{dt} = C \cdot \frac{dv}{dt} \tag{2.11}$$

$$C = \frac{dq}{dv}. \tag{2.12}$$

Changing the notation for output capacitance and drain–source voltage, we obtain

$$C_o(v_{DS}) = \frac{dQ_o(v_{DS})}{dv_{DS}}. \tag{2.13}$$

Eq. (2.13) means that C_o is simply the gradient of the Q_o-versus-v_{DS} curve. The definition in Eq. (2.13) should be used to avoid a common confusion where a non-linear capacitance is defined by the linear equation $C_o(v_{DS}) = Q_o(v_{DS})/v_{DS}$ that fails to capture the device's large-signal variation of its charges [14, 34]. Acknowledging the fact that both large-signal charge and capacitance are functions of v_{DS}, for the rest of this thesis, we use the simple notations $C_o(v_{DS}) = C_o$ and $Q_o(v_{DS}) = Q_o$.

2.4 Charge- and Energy-Equivalent Parameters

Certain device datasheets define additional equivalent (or effective) capacitances related device output capacitance. These definitions are summarized in Table 2.2, where the main definition refers to our convention and the alternative definition refers to the names given in certain datasheets for the same parameter. We summarize the meaning of these parameters as follows.

1. **Charge-equivalent linear capacitance ($C_{o(Q,eq)}$):** is linear (or fixed) capacitance value that would store the same amount of charge as C_o when it is charged from 0 V to a v_{DS} value equal to V_1. This can be expressed as

$$C_{o(Q,eq)} = \frac{\int_0^{V_1} C_o \, dv_{DS}}{V_1} = \frac{Q_o}{V_1}. \tag{2.14}$$

   An example for $V_1 = 200$ V is considered for a C_{oss} curve of a GS66508T GaN HEMT in Figure 2.10(a). In device datasheets, this parameter is usually expressed as 'Effective Output Capacitance (Time Related), $C_{o(TR)}$'. In other words, it means the value of fixed capacitance that would take the same amount of time to charge from 0 V to V_1. It should be noted that the actual charging time depends on the excitation type and the path resistances. Therefore, this alternative definition should be used for the condition where the charging is achieved through a constant current source, as suggested by the Application Note AN90005 by Nexperia [35].

2. **Energy-equivalent linear capacitance ($C_{o(E,eq)}$):** is linear (or fixed) capacitance value that would store the same amount of energy as C_o when is charged from 0 V to a v_{DS} value equal to V_1. This

Main Definition	Symbol	Alternative Definition	Symbol
Charge-equivalent linear capacitance	$C_{o(Q,eq)}$	Time-related effective output capacitance	$C_{o(TR)}$
Energy-equivalent linear capacitance	$C_{o(E,eq)}$	Energy-related effective output capacitance	$C_{o(ER)}$
RMS value of capacitance	$C_{o(RMS)}$	-	-

Table 2.2: Summary of Equivalent Capacitances Related to Device Output Capacitances

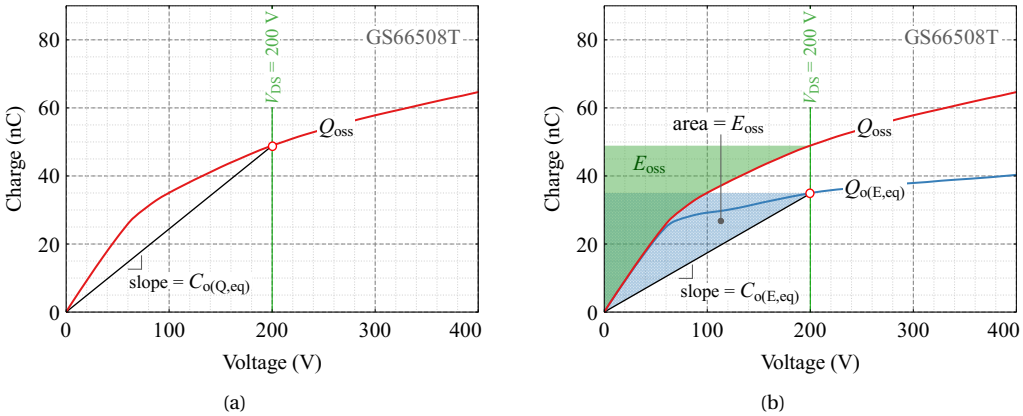


Figure 2.10: Definition of charge- and energy-equivalent capacitances based on small-signal capacitance, C_{oss}. An example for a GS66508T GaN HEMT at 200 V is considered. For a given drain–source voltage, (a) the charge-equivalent capacitance is defined as a linear capacitance, $C_{o\,(Q,eq)}$, that gives a stored charge equal to Q_{oss}, whereas (b) the energy-equivalent capacitance is defined as a linear capacitance, $C_{o\,(E,eq)}$, that stores an amount of energy equal to E_{oss}.

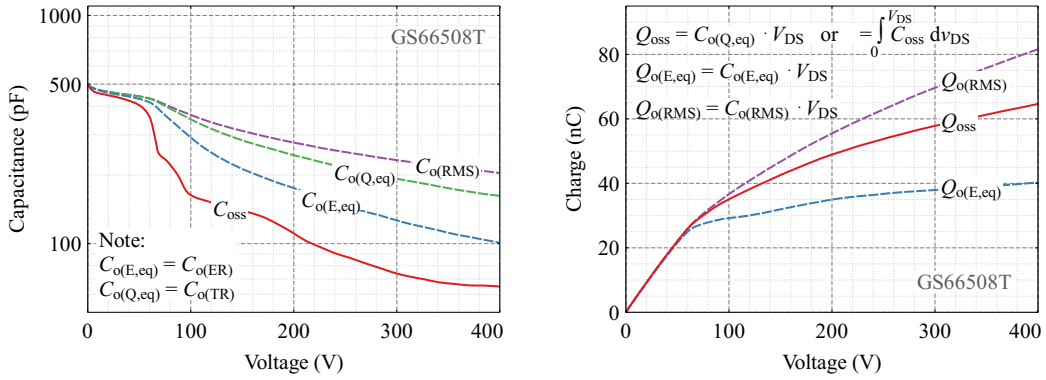


Figure 2.11: A summary of different representations of C_{oss} found on device datasheets. A GS66508T GaN HEMT is considered. (a) Representation of the quantities $C_{o(ER)} = C_{o(E,eq)}$, $C_{o(TR)} = C_{o(Q,eq)}$, and $C_{o(RMS)}$, alongside C_{oss} on a *CV* plot. (b) Representation of the quantities $Q_{o(E,eq)}$ and $Q_{o(RMS)}$, alongside Q_{oss} on a *QV* plot.

can be expressed as

$$E_o = \frac{1}{2} C_{o(E,eq)} V_1^2. \tag{2.15}$$

Eq. (2.15) can be rearranged to get,

$$C_{o(E,eq)} = \frac{2E_o}{V_1^2}. \tag{2.16}$$

Device datasheets usually express this parameter as 'Effective Output Capacitance (Energy Related), $C_{o(ER)}$'. An example for $V_1 = 200$ V is considered in Figure 2.10(b). Here, an energy-equivalent charge ($Q_{o(E,eq)}$) can also be defined such that

$$Q_{o(E,eq)} = C_{o(E,eq)} \cdot V_1.$$

$Q_{o(E,eq)}$ is also plotted in Figure 2.10(b), where the shaded area in blue is equal to E_{oss}.

3. **RMS value of output capacitance ($C_{o(RMS)}$):** a root-mean-square (RMS) value for C_o can be defined as given by Eq. (2.17) when it is charged from 0 V to a v_{DS} value equal to V_1.

$$C_{o(RMS)} = \sqrt{\frac{\int_0^{V_1} C_o^2 \, dv_{DS}}{V_1}} \tag{2.17}$$

Here, a related charge value can be as

$$Q_{o(RMS)} = C_{o(RMS)} \cdot V_1. \tag{2.18}$$

Figure 2.11 provides a summary of the parameters discussed here in relation to the small-signal values of a GS66508T GaN HEMT.

2.5 Non-Linear Nature of Device Output Capacitance

As mentioned earlier, device output capacitance is a nonlinear function of v_{DS}. The nature and severity of the nonlinearity depend on the technology and structure of a device. For instance, certain Si-SJ

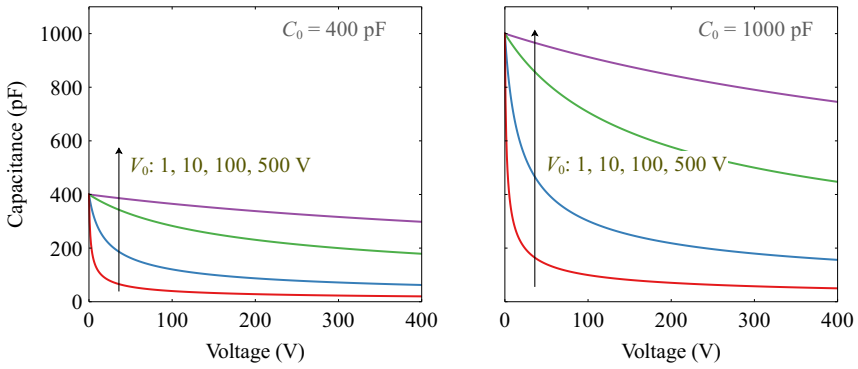


Figure 2.12: CV curves obtained using Eq. (2.19) for $m = 1/2$, and $C_0 = 400$ pF and 100 pF. Four different values for V_0 are considered for the two cases of C_0.

devices show orders of magnitude change in their C_o when v_{DS} changes from 0 V to a few volts (or a few tens of volts). For instance, consider Figure 2.6(a): C_{oss} value of super-junction device Si-1 change from 33 nF to 80 pF, when v_{DS} changes from 100 V, which corresponds to a reduction by more than 400 times. On the other hand, the change is not profound, for some devices, such as device SiC-2, where the C_{oss} value change from 1.3 nF to 150 pF for the same voltage change (a reduction of approximately 9 times).

Such complexity of the non-linearity of C_o on v_{DS} makes it difficult to formulate a generalized analytical equation for C_o for power transistors. In the SPICE models provided by device manufacturers, output capacitance is modelled by two or more complex equations that provide a good estimate of the experimental observed C_{oss} curve.[16] However, for simple analytical purposes, an equation such as given by Eq. (2.19) can be used to describe the change of C_o with v_{DS} [33].

$$C_o = \frac{C_0}{\left(1 + \dfrac{v_{DS}}{V_0}\right)^m} \tag{2.19}$$

A commonly used value for m is 1/2. The value output capacitance at $v_{DS} = 0$ V is determined by the parameter C_0. Figure 2.12 shows two examples of the use of Eq. (2.19) with $C_0 = 400$ pF and 1000 pF. For each case, four different values of V_0 is considered. Additional details on the analytical and SPICE modelling of C_o can be found in the work by Costinett et al. [33].

2.6 Output Capacitance and Circuit Topology

In this chapter, we have introduced basic concepts related to the output capacitance and output charge of field-effect transistors. Our discussions were carried out from the perspective of C_o of a power FET, without any particular reference to the power electronic circuit, or the topology, on which the power device is utilized on. This is an extremely important consideration as we will see in Chapter 4 (concerns the interaction of C_o with soft-switching topologies) and Chapter 5 (concerns the interaction of C_o with hard-switching topologies). Two simple examples, accompanied with explanatory text, are shown in Figure 2.13 to elucidate this point.

[16] The methods and equations used to model C_o vary depending on the manufacturer. And some models are encrypted, and therefore, exact equations are not possible to be read on the model file.

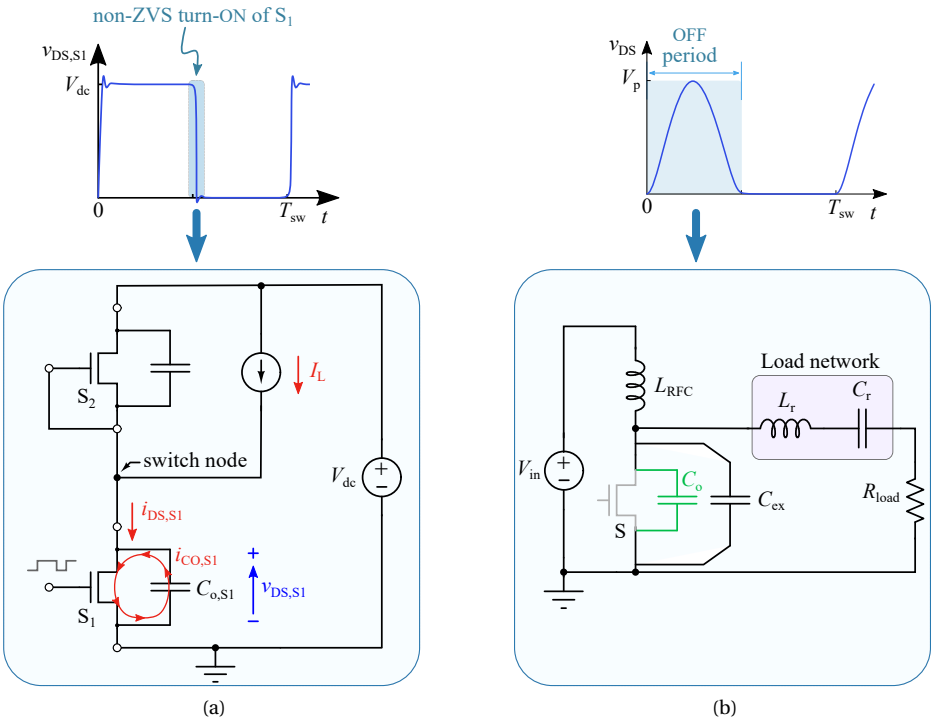


Figure 2.13: The relationship between the output capacitance of a power FET and a power electronics circuit is not a straightforward one. Their interaction, as well as the usefulness of C_o to the circuit, depends on the topology of the circuit. Two examples are considered. (a) In a double-pulse-test circuit, the output capacitance of the test device (S_1) is self-discharged through the channel of S_1 during its turn-ON. Here, C_o is not considered to be a useful parameter for the circuit as it creates an energy loss that scales with switching frequency. (b) In a class-E inverter circuit, C_o of the switching device S is utilized to achieve ZVS. If the value of C_o is too small, an external shunt capacitance C_{ex} is added to achieve ZVS. If C_o is too large, then other parameters of the circuit need to be changed/tuned.

In the next chapter, we look into the basics of switching processes and related terminology to provide background on power electronic topologies, which is the second important consideration of the interaction mentioned above.

3 Thematic Overview: Switching Circuits and Switching Process

THIS chapter reviews basic concepts related to switching events in a power converter. We review different operating modes in standard hard- and soft-switching circuits and highlight the specific modes which are responsible for the charge–discharge process of device output capacitance. We specifically distinguish between the OFF-state, ON- and OFF-transients, and dead-time. Important ideas related to currents in a device are also reviewed, emphasizing the need to distinguish between the drain and channel currents. Finally, the concept of zero-voltage-switching is revisited to highlight its presence in both hard- and soft-switching techniques.

3.1 Basic Concepts

Switching (or switch-mode) power circuits can have very simple arrangements such as a single inverter-leg (half-bridge) configuration, or they can have complex topologies such as switched-capacitor circuits or multi-level converters. In general, each complex circuit can be represented as a collection of unit blocks or equivalent circuits, whose steady-state operation can be described with a few operating modes. Some examples can be identified as follows.

- Generally, multi-level converters can be described as a combination of unit blocks (half-bridges or full-bridges) [36].

- Switched-capacitor converters are also analysed with unit cells [37] or equivalent circuits [38].

These approaches not only allow the analysis of a complex circuit easier, but they also provide important insights into the development of measurement and characterization tools to investigate particular features of a complex circuit or the behaviour of circuit elements under certain operating conditions. Such thinking resulted in the no-load techniques presented in Chapters 5 and 6. Therefore, here we review important ideas related to two elemental unit blocks that are common in power electronic topologies, which are also the main circuit configurations exploited in this thesis work to study the behaviour of C_o.

3.1.1 ON Resistance and Channel Resistance

The ON-resistance (or ON-state resistance) of a transistor, denoted as $R_{DS(on)}$, is the sum of all the resistances (contact, channel, etc.) in the conduction path[1] when the device is in ON state[2] [26]. Therefore, the ON resistance is higher than the channel resistance. To simplify our analysis in Chapter 5, we neglect the contact resistances; any other resistances within the structure are lumped into the channel resistance, which would be then equal to $R_{DS(on)}$ at fully-ON condition of the device.

3.1.2 Operating modes in a Hard-Switching Circuit

Figure 3.1 illustrates the typical waveforms (qualitative) and operating modes in an inverter leg (or a cell) operating in hard switching. We specifically focus on S_1, which is the bottom device in leg configuration. The related operating modes and the state of the output capacitance of S_1, $C_{o,S1}$, can be summarized as follows.

- OFF state: v_{DS} is held fixed at V_{dc} by the dc-link voltage (generally by a large dc-link capacitance). Therefore, the voltage across $C_{o,S1}$ is fixed, and $C_{o,S1}$ does not experience any charge or discharge event: $C_{o,\,S1}$ is inactive (but fully charged) in this mode.
- ON state: the device channel is fully enhanced (i.e., $R_{ch} = R_{DS(on)}$) and conducts current. The voltage across $C_{o,S1}$ is equal to the ON-state voltage across the device, which we can be considered to be zero as far as charging or discharging of $C_{o,S1}$ is considered. Thus, $C_{o,\,S1}$ is inactive (and fully discharged) in this mode.
- turn-OFF transition: v_{DS} of S_1 changes from ON-state voltage to V_{dc}. $C_{o,S1}$ goes through its charging process, and therefore, it is active in this mode.
- turn-ON transition: v_{DS} of S_1 changes from V_{dc} to its ON-state voltage. $C_{o,S1}$ goes through its discharging process, and therefore, it is active in this mode.
- dead-times: during the dead times, the device channels are cut-off. However, depending on the topology, a v_{DS}-transition mode may or may not coincide with a specific dead-time. For example, in Figure 3.1, the OFF-transition of S_1 coincides with dead-time.

Note that we define *fully enhanced* as the condition $v_{GS} = V_{drive}$, where V_{drive} is the drive-voltage value for which the typical $R_{DS(on)}$ value for a device is given.[26]. Additional details on these operating modes, alongside the losses relevant to each mode, are discussed in Section 5.2.3.

[1] The ends of the path are defined by the drain and source terminal contacts.
[2] For a given V_{GS} value beyond $V_{(GS)th}$.

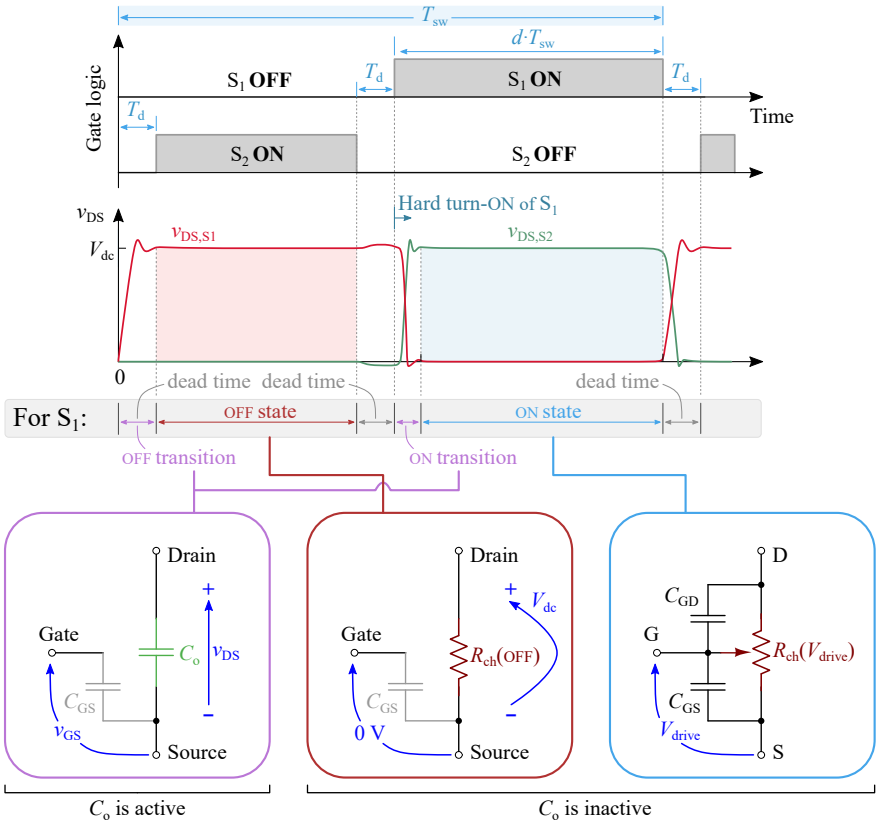


Figure 3.1: Operating modes in a standard hard-switching circuit. The device under test is S_1.

3.1.3 Operating modes in a Soft-Switching Circuit

Here, we focus specifically on the operating modes in a class-E circuit [see Figure 2.13(b)], one of the simplest soft-switching topologies. The operating modes are illustrated in Figure 3.2, where the output capacitance of the switching device is denoted as C_o.

- OFF state: v_{DS} changes from ON-state voltage to the peak-voltage V_p and then back to ON-state voltage. Therefore, C_o goes through a complete charge and discharge cycle: C_o is active in this mode.
- ON state: the device channel is fully enhanced and conducts current. The voltage across C_o is equal to the ON-state voltage across the device. Thus, $C_{o,\,S1}$ is inactive in this mode.

In contrast to the hard-switching conditions discussed earlier (Section 3.1.2), one important distinction here is that there is no distinctive ON or OFF transition: both transitions are spread through the OFF state. In other words, the charge and discharge of C_o is a continuous process, which is not the case for hard switching.

It should also be mentioned that there are variants of soft-switching topologies that do not offer such a charge–discharge profile for C_o. In certain cases, distinct ON or OFF transitions exist, which are, however, much smoother and prolonged in contrast to hard-switching transitions: an example is briefly discussed in Section 5.2.2.

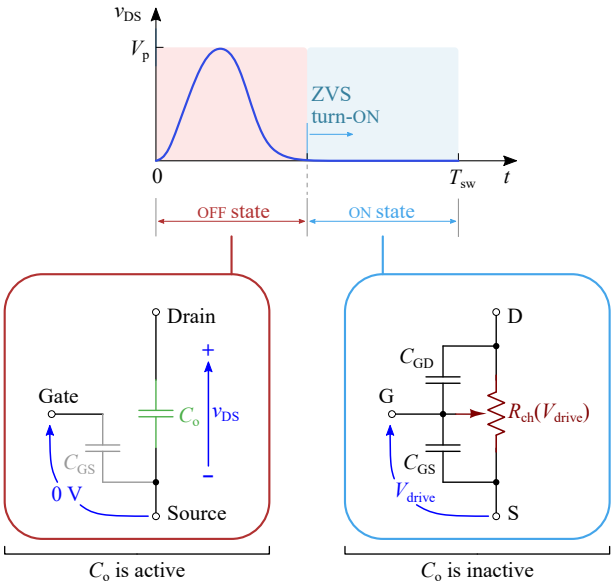


Figure 3.2: Operating modes in a standard class-E circuit.

3.1.4 Currents in a Switching Transistor

Using a double-pulse test (DPT) circuit as an example, different current components in a switching power transistor are marked in Figure 3.3 and listed in Table 3.1. A summary of important current components is given below.

- **drain–source current** (i_{DS}): the total instantaneous current that is flowing into the drain terminal of the device (equal to the current coming out of the source terminal when gate current is neglected). This can also be simply referred to as the *drain current*.
- **channel current** (i_{CH}): the total instantaneous current that is flowing through the *channel* of the device.
- **output capacitance current** (i_{CO}): the total instantaneous current that is flowing into (or out of) the output capacitance of the device. The direction of the current can be marked based on the particular topology under consideration for convenience. This current is equal to $i_{C_{DG}} + i_{C_{DS}}$. Therefore, in Figure 3.3, a positive value for i_{CO} is considered (current going into C_o from the drain terminal).

A very important point to note here is the distinction between the channel and the drain–source current. The former can be measured using standard electrical measurements,[3] while the latter cannot be measured by electrical means in practice. Nevertheless, this distinction is paramount and serves an important role in the several analyses carried out in this thesis work. One example is considered in Section 3.1.5 about switching energy.

On another practical note, it should be mentioned that it is possible to measure the channel current in certain simulation software. For example, this is possible in LTspice (by Analog Devices) by allowing

[3] Subjected to bandwidth limitations.

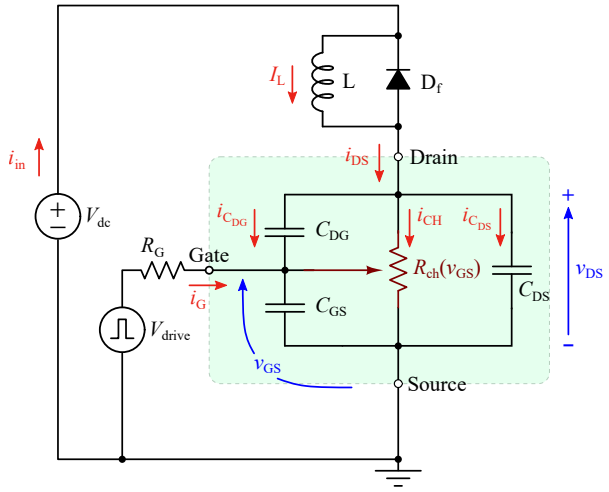


Figure 3.3: Currents in a switching transistor.

Table 3.1: Currents in a Switching Transistor

Symbol	Description
i_{DS}	drain–source current
i_{CH}	channel current
$i_{C_{DS}}$	current through C_{DS}
$i_{C_{DG}}$	current through C_{DG}
i_{C_o}	current through C_o
i_G	gate current

access to subcircuit currents.[4] Care should be taken, when identifying the correct current component as different manufacturers use different naming conventions for the channel.[5] For example, GaN manufacturers GaN Systems and EPC use the name ***bswitch*** to define the channel current in their SPICE models.

3.1.5 Switching Energy

Switching energy is the energy lost (in the channel of the power device) due to the overlap of voltage and current (*VI*-overlap) during a switching event—see Figure 3.4. More specifically, for a power transistor, the voltage and the current in concern are the device drain–source voltage, v_{DS}, and the channel current, i_{CH}, respectively.

Consider a hard-switched device. Let us define the *VI* overlap times for the turn-ON and turn-OFF transitions as $t_{ov\text{-}ON}$ and $t_{ov\text{-}OFF}$, respectively. Then turn-ON switching energy can be given as

$$E_{on} = \int^{t_{ov\text{-}ON}} i_{CH}\, v_{DS}\, dt, \tag{3.1}$$

while the turn-OFF switching energy can be given as

$$E_{off} = \int^{t_{ov\text{-}OFF}} i_{CH}\, v_{DS}\, dt. \tag{3.2}$$

Finally, the total energy loss in switching for a single switching cycle can be given as

$$E_{sw} = E_{on} + E_{off}. \tag{3.3}$$

[4] Go to **Tools → Control Panel**. Then select the **Save Defaults** tab. Tick the option that says **Save Subcircuit Device Currents [*].**

[5] In addition, depending on the complexity of the device model, several current components need to be added in the waveform window to get the correct value for channel current.

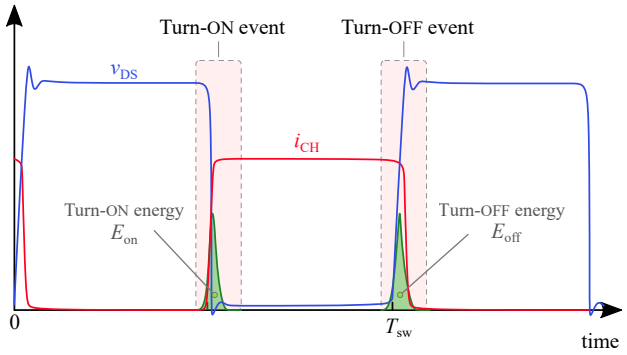


Figure 3.4: Representation of switching energy.

Under steady-state operation, the corresponding power loss is then given as

$$P_{sw} = f_{sw} E_{sw}, \tag{3.4}$$

where f_{sw} is the switching frequency.

There have been certain discrepancies in conventional loss analysis concerning measured and theoretical switching energies due to the use of drain–source current instead of the channel current. For the turn ON transition, the externally measured $i_{DS} \cdot v_{DS}$ underestimated the turn-ON switching energy for hard-switching circuits; for the turn OFF transition, it overestimates the turn-OFF switching energy [39]. This was eventually clarified in several works by distinguishing between channel and drain currents [25, 39–41]. We emphasize that the channel current should be considered to evaluate switching energy.

3.2 Soft-Switching Operation

The idea behind soft-switching operation is to minimize (and ideally make zero) reduce the switching power loss (P_{sw}) in power electronic converters[26, 28, 29]. While the traditional hard-switching converters result in *hard* switching transitions, these converters offer much *softer* (or smoother) ON or OFF events.

For a given switching frequency, as amply clear from Eq. (3.4), the only possible course of action to reduce P_{sw} is to reduce E_{sw}. This can be achieved by minimizing (or making zero) either E_{on} or E_{off} and in the ideal case by minimizing both. Based on these two possibilities, two main categories in soft switching are identified:

1. **zero-voltage-switching (ZVS)**[6]**:** E_{on} is ideally made zero by making (or allowing) $v_{DS} = 0$ V, before the turn-ON event. And for the entire duration of $t_{ov\text{-}ON}$, v_{DS} is kept at 0 V. This essentially makes the integral in Eq. (3.1), and hence E_{on}, equal to zero. Such a turn-ON event is generally termed a *ZVS-turn-ON event.*

2. **zero-current-switching (ZCS):** E_{off} is ideally made zero by making (or allowing) $i_{CH} = 0$ A, before the turn-OFF event. And for the entire duration of $t_{ov\text{-}OFF}$, i_{DS} is kept at 0 A. This makes the integral in Eq. (3.2), and hence E_{off}, equal to zero.

[6] In this thesis, we use the initialism ZVS to refer to both 'zero-voltage switching' and 'zero-voltage switched'.

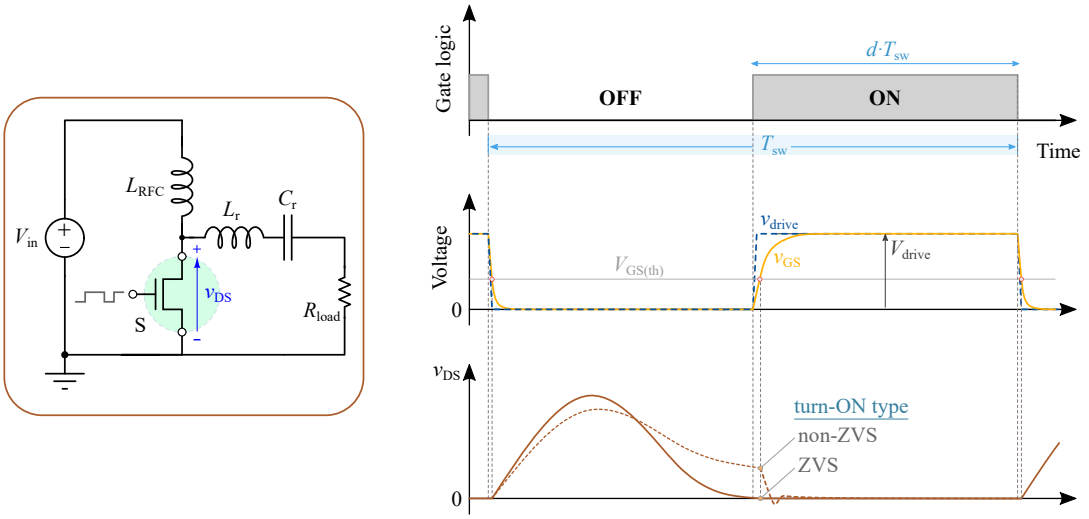


Figure 3.5: ZVS and non-ZVS turn-ON events of the switching device in a class-E inverter.

It should also be mentioned that for fast devices, the turn-OFF loss can be reduced to very small values having a good gate control with no ZCS implemented [25, 41]. This is because the speed at which the channel current is cut off during the turn-OFF event is predominantly controlled by the gate-driver circuit. With a strong drive circuit, therefore, it is possible to reduce $t_{\text{ov-OFF}}$ to a small value in driving modern power FETs, especially WBG devices [41]. In practice, such gate control is achievable with a driver circuit with very-low loop inductance, low gate resistance and large-enough sink current capability. Furthermore, E_{sw} can ideally be made zero when such an approach is used in a circuit with ZVS [41].

Figure 3.5 shows an example of a class-E inverter [28, 42, 43], which is a soft-switching converter. The circuit, by design, operates such that the switching device (S) is turned ON under ZVS conditions as shown by the waveforms. Ideally, $v_{\text{GS}} = V_{\text{GS(th)}}$ is approached when $v_{\text{DS}} = 0$ V and $\frac{dv_{\text{DS}}}{dt} = 0$ [44].[7] In Figure 3.5, an example case where ZVS is not achieved is also shown (denoted as a non-ZVS turn-ON). It is also important to note that the circuit is not designed to achieve ZCS (see the non-zero channel current at the turn-OFF in Figure 7.4). However, as mentioned earlier, E_{off} can be minimized by using a fast turn-OFF process.

Another important aspect about ZVS is that it is not necessarily limited to soft-switching converters, which are specifically designed to achieve zero E_{on}. In certain hard-switching topologies—and under certain operating conditions—some of the devices in the circuit inherently undergo a ZVS turn-ON.[8] An example is a synchronous buck converter—see Figure 3.6. In the topology, the turn-ON event of S_2 is a fully hard-switched one. However, the turn-ON event of the synchronous device can achieve ZVS: this depends on the duration of the dead time (T_{d}), the magnitude of the load current I_{L}, and E_{o} of the used power FET. In Figure 3.6, consider the dead-time that occurs after the turn-OFF event of S_2. A ZVS turn-ON is achieved for S_1 during this period when I_{L} is large enough to discharge all the electric charge that was stored in the output capacitance of S_1. When I_{L} is not large enough, a partial-ZVS condition is

[7] The condition $\frac{dv_{\text{DS}}}{dt} = 0$ is a requirement specific to the class-E circuit [42, 45].

[8] Whether the energy stored in the device output capacitance is recovered or not is a different matter. This is not discussed here as it involves additional analyses on circuit topologies and is beyond the scope of this thesis. A good starting point on such a work would be the work by Kasper et al. [46].

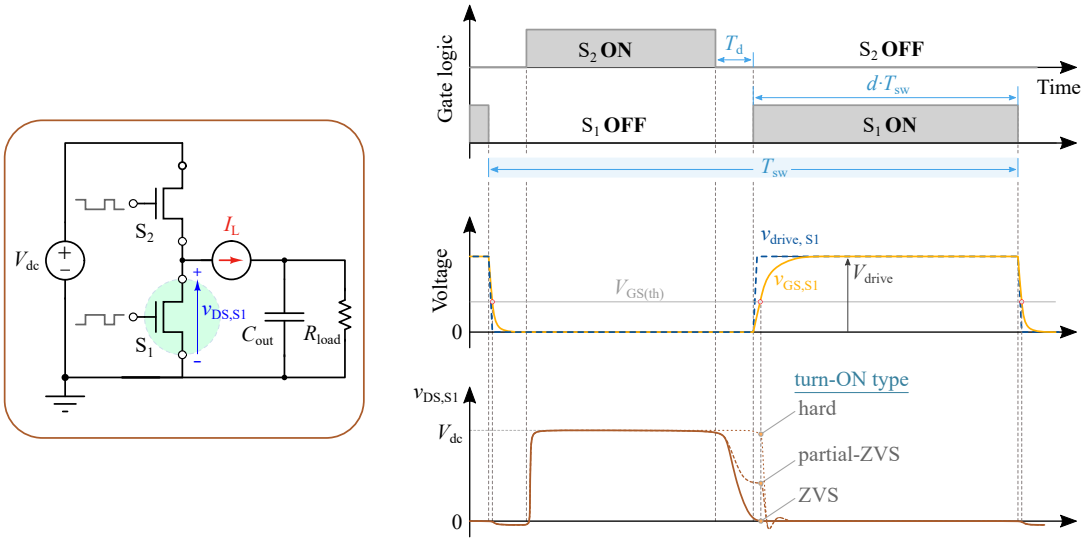


Figure 3.6: ZVS, partial-ZVS, and hard turn-ON events of the synchronous device in a buck converter. Note: S_1 is the synchronous device and S_2 is the main switching device.

achieved as shown: a partial-ZVS event is also possible if the dead-time is not long enough for a given value of I_L. In the extreme case, where I_L or dead-time is too small, the turn-ON of S_2 undergoes a fully hard-switched event.

A final remark should be given on the charge and discharge process of device output capacitance in soft-switching power circuits. In circuits like the class-E inverter (see Figure 3.5), the charge and discharge processes of C_o take place as a resonant process [17], while the device is in its OFF state. Therefore, this process can be considered as an excitation of C_o, where the transfer of energy is facilitated through an inductance. And ideally, this process is assumed to be lossless [17, 47].[9] In the next chapter, we discuss the validity of this. We will show that, in real devices, this charge–discharge process of C_o in soft-switching operation is, in fact, lossy.

[9] The same arguments are valid for other soft-switching circuits, such as resonant-transition type converters (see Section 5.2.2), where the charge and/or discharge of C_o is also achieved as part of a resonant event.

Part II

4 Output Capacitance and Soft-Switching Circuits

THE advent of WBG semiconductor devices is shifting the upper-frequency limit for both hard- and soft-switching. At the same time, Si super-junction technology, with its commandingly lower on-state resistance, was still moving forward, pushing the operating frequencies for power converters. The evidence of an unexpected loss mechanism in Si-SJ devices that were used in soft-switching converters initiated an important investigation into the large-signal behaviour of the output capacitance of field-effect transistors. This served as the basis for this chapter as well as for this thesis work. We focus on the following topics in this chapter.

We start with establishing the background of output-capacitance hysteresis losses, and the concepts of small-signal and large-signal measurements. Then we provide an in-depth analysis on the Sawyer–Tower technique, which is a powerful tool for analysing the large-signal behaviour of C_o. The technique is then used to characterize commercial FET technologies: we investigate both frequency and voltage dependency of the output-capacitance losses. The possibilities of using small-signal measurements to identify these losses are also discussed. A brief discussion on the origins of C_o-hysteresis losses from a device perspective is also given. Finally, based on the experimental results, we provide a useful categorization of output-capacitance hysteresis loss for the soft-switching operation.

It should also be mentioned that the power MOSFETs (of Si, Si-SJ, and SiC technologies) studied in this chapter are vertical devices, while the GaN devices are *lateral devices*.[1]

This chapter is partly based on the material published in the following articles:

[1] Commonly known as lateral heterojunction field-effect transistors (HFETs) or high electron mobility transistors (HEMTs) [6].

C1. **N. Perera**, A. Jafari, L. Nela, G. Kampitsis, M. S. Nikoo, and E. Matioli, 'Output-Capacitance Hysteresis Losses of Field-Effect Transistors', in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, Nov. 2020, pp. 1–8.

J1. **N. Perera** et al., 'Analysis of Large-Signal Output Capacitance of Transistors Using Sawyer–Tower Circuit', *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 3, pp. 3647–3656, Jun. 2021.

J2. **N. Perera**, M. S. Nikoo, A. Jafari, L. Nela, and E. Matioli, 'Coss Loss Tangent of Field-Effect Transistors: Generalizing High-Frequency Soft-Switching Losses', *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12585–12589, Dec. 2020.

4.1 Background: Output-Capacitance Hysteresis Loss

With the growth of power MOSFET technology, HF soft-switching converters have been widely researched to push existing power density limits [3], [8], [9]. For instance, resonant-type power converters are an attractive solution to achieving large power densities at high frequencies due to their soft-switching behaviour [17, 29, 48]. Their applications include, among others, computer power supplies [49], radio-frequency (RF) power amplifiers in communication systems [42, 50, 51], and wireless power transfer systems[26]. During a single switching cycle in these converters, the output capacitance, C_o,[2] of the switching device is charged and discharged in a resonant manner dictated by the specificities of the topology, as means of achieving soft-switching conditions [29]. Since the device is in the OFF state during the charging–discharging process of C_o, this ideally yields zero losses [17, 47] in contrast to hard-switching conditions [52]—see Figure 4.1

In doing so, Fedison et al. found an unexpected loss mechanism related to the output capacitance of silicon super-junction (Si- SJ) MOSFETS [9], which could not be explained with the capacitance versus voltage (*CV*) curves from datasheets. It was reported that transition losses still exist due to dynamic

[2] Please refer to Section 2.2.1 for details on the notation.

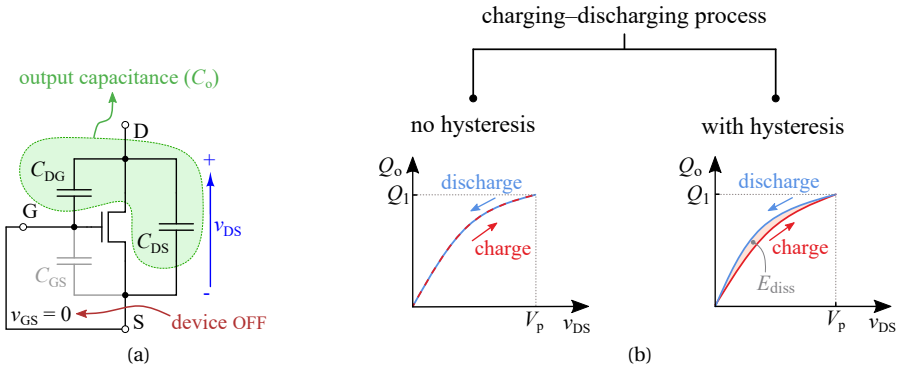


Figure 4.1: (a) In resonant-type converters such as the class-E inverter, the charging–discharging process of the output capacitance ($C_o = C_{DG} + C_{DS}$) of a transistor occurs while it is in OFF state (i.e., $v_{GS} = 0$ V). (b) The related variation of the accumulated charge (Q_o) versus device drain–source voltage, v_{DS}, is represented by a *QV* curve. Two cases can be considered for a *QV* curve: (1) without hysteresis; and (2) with hysteresis, where different charging (red line) and discharging (blue line) paths result in a hysteresis energy loss, E_{diss}, which is specified for a given maximum voltage V_p of v_{DS}.

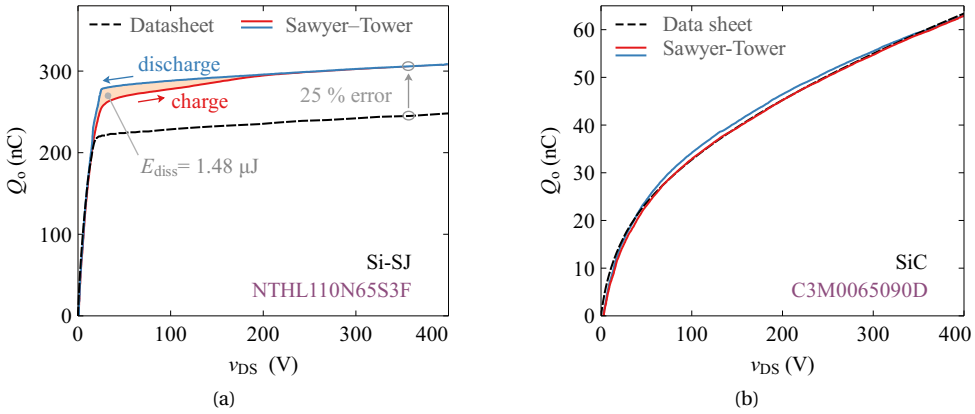


Figure 4.2: Large-signal Q_o versus v_{DS} curves obtained from the Sawyer–Tower circuit at 100 kHz for two devices, where the dashed black lines show the small-signal Q_{oss} calculated using datasheet C_{oss} values. (a) The Si-SJ device exhibits a large difference in small and large-signal curves, with Q_o at 400 V showing a 25% increase in the large-signal results. With distinct charge/discharge paths (solid red and blue lines respectively), the Si-SJ device shows a considerable hysteresis loss of E_{diss} = 1.48 μJ. (b) A 900-V SiC device with similar small and large-signal curves, and with some hysteresis in the charge–discharge curves; here, as $Q_o$values at 400-V are much smaller, the related E_{diss} (= 0.36 μJ) is also lower.

charging and discharging of the power device's output capacitance under soft-switching conditions [13–15, 17, 19, 21]. The corresponding energy loss is attributed to a hysteresis loss [47], which is observed in large-signal charge versus voltage (QV) curves as shown in Figure 4.1(b). Numerous works have reported such losses pertaining to different device structures: in Si Super-Junction (Si-SJ) transistors [14, 18, 53]; and wide-band-gap (WBG) SiC transistors [19, 22] and GaN high-electron-mobility transistors (HEMTs) [17, 19, 21, 54, 55].

4.1.1 Small- versus Large-Signal Behaviour of Device Output Capacitance

The operation of power electronics in the MHz range is influenced by the power losses associated with device output capacitance, C_o. The observation of hysteresis losses in charging/discharging C_o of Si-SJ MOSFETs and WBG devices initiated an increased focus on device C_o and its large-signal behaviour, as the datasheet-provided small-signal capacitance, C_{oss}, is incapable of explaining such behaviour.[3]

Unlike the real operating conditions in power electronic circuits, small-signal CV measurements never subject C_o to a large voltage swing. Recent research shows that datasheet based C_{oss} curves fail to accurately estimate losses related to C_o [14, 20]. On the other hand, large-signal-measurement techniques better emulates the charge–discharge behaviour of C_o in the actual circuit [14, 17, 56].

The difference between large and small-signal curves, and hence the severity of the error in actual Q_o (or C_o) and related losses, varies based on the device type. The implications of this in real converter applications are twofold, depending on if the device is hard switched or soft switched. If the device is hard-switched, the total C_o-related losses occur first in charging C_o through the available circuit path and then in discharging the charge stored in C_o through the device channel itself (see Chapter 5 for details). The resulting loss is given by the product $Q_o|_{V_{dc}} \cdot V_{dc}$, where V_{dc} is the dc-link voltage (or the bus voltage). Therefore, the error in the losses is directly related to the estimated Q_o value at a given V_{dc} value. Figure 4.2(a) shows an example for a Si-SJ transistor, where the small-signal Q_{oss} value varies

[3] Please see Section 2.2 for more details.

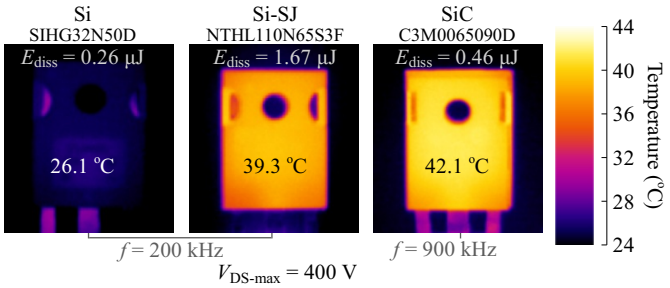


Figure 4.3: Thermal images showing the temperature rise of three devices (Si, Si-SJ and SiC) with different E_{diss} values (estimated using the Sawyer–Tower circuit). The devices (with v_{GS} = 0 V) have the same hardware package (TO-247) and were excited sinusoidally in the Sawyer–Tower circuit arrangement at 400 V. The observed losses are not possible to be calculated based on datasheets, and ideally, these devices should not dissipate any power as charging/discharging C_o is assumed to be lossless. The observed power dissipation reveals the need for a proper characterization of device C_o.

by 25% in comparison with the large-signal value, resulting in a significant error in hard-switching losses. On the other hand, Figure 4.2(b) shows a case for a SiC device, where the large-signal Q_o curve shows less deviation from the datasheet curve, with negligible hysteresis at 100 kHz. The large-signal behaviour in hard-switching circuits is separately addressed in Chapter 5, and hence, not addressed in this chapter.

If the device output capacitance is resonantly charged/discharged under soft-switching conditions, based on the datasheet curves, no C_o-related loss should occur [17]. However, the Q_o *vs* v_{DS} curve of the Si-SJ device in Figure 4.2(a) reveals a difference in the charge/discharge paths, resulting in a hysteresis loss, E_{diss} [14, 22, 23]. Figure 4.3 shows three devices with similar hardware packages that were excited with a large-signal sinusoidal signal with a 400-V peak voltage. The Si and Si-SJ devices were excited at 200 kHz. The Si-SJ device exhibits a significant temperature rise, hence much larger power dissipation ($P_{diss} = E_{diss} \cdot f$) compared to the Si device. This is due to relatively large (1.67 µJ > 0.26 µJ) E_{diss} of the Si-SJ device. Although the SiC device is switched at a much higher frequency (4.5 times higher), compared to the other two devices, it only shows a temperature 3 °C higher compared to the Si-SJ device: this is due to the SiC device's lower E_{diss} value of (0.46 µJ < 1.67 µJ). These results show the importance of large-signal Q_o *vs* v_{DS} measurements in predicting both hard and soft-switching losses, which are not possible to be calculated based on datasheet-based small-signal C_{oss} (or Q_{oss}) curves.

4.1.2 Adaption of the Sawyer–Tower Technique

One of the main techniques adapted to observe the large-signal behaviour of C_o is the Sawyer–Tower circuit [14, 17, 22, 53, 57]. The circuit consists of a signal generator, a high-voltage amplifier, a fixed linear reference capacitor, C_{ref}, and the device under test (DUT).

The Sawyer–Tower technique has traditionally been used for ferroelectric dielectric material characterization [57]; and now has been adapted to characterize large-signal C_o of Si, Si-SJ, SiC and GaN power transistors [14, 17, 53], and very recently of SiC power diodes[58]. It initially obtains the device's output charge characteristic (Q_o *vs* v_{DS}) by applying a large excitation voltage, and subsequently, C_o is obtained by taking the derivative of Q_o with respect to v_{DS}.

The Sawyer–Tower technique provides several distinct advantages for C_o characterization. The DUT (gate and source shorted) and a reference capacitor are the only two electronic devices involved:

no external components such as inductors, active switches, gate drivers or control circuitry. Only two voltage measurements are involved (v_{IN} and v_{REF}): this allows the method to be very accurate even at lower VHF levels as there are no current measurements involved, which are prone to higher inaccuracies. The losses in the circuit are only due to Q_o hysteresis losses: no conduction or any other external losses exist, allowing direct evaluation of E_{diss} by thermal measurements. A large range of voltage-swings across v_{DS} can be achieved: if the voltage is limited due to the amplifier's output voltage rating, a simple high-frequency transformer can be used to boost the voltage output, provided that the amplifier's output power capability is not exceeded for the given f. In addition, the results are recorded in continuous operation, which is closer to actual operating conditions as opposed to single-cycle-measurement methods, such as the nonlinear resonance approach [56]. Continuous excitation is also a good indicator of hysteresis loss as the devices with large E_{diss} values heat up and this can be observed using a thermal camera, as we have shown in Figure 4.3. Moreover, the Sawyer–Tower circuit can easily perform frequency sweeps by changing the signal-generator output frequency (f).

However, the Sawyer–Tower method has some technical limitations. The maximum-voltage swing for a given f (even with a high-frequency transformer) is confined by the voltage amplifier [22, 56] because the gain of the amplifier degrades with increasing f as the power output capability of the amplifier is limited. The response due to different types of excitation signals offers additional details about a device's C_o [17]: for instance, triangular waveforms allow to observe the response due to a constant dv/dt excitation, whereas pulsed excitation creates a very high dv/dt condition. Although near sinusoidal waveforms could be applied at higher frequencies, the application of pulsed waveforms is limited by the bandwidth of the voltage amplifier and the value of the equivalent load capacitance, C_{eq}.

Several alternative methods exist for large-signal Q_o (or C_o) estimation. A nonlinear-resonance method [56], relies upon the resonance between a pre-calibrated inductor and the device C_o. The method only requires a low-voltage dc source as the input, and therefore, eliminates the need for a high-voltage high-bandwidth amplifier. Since the DUT is switched to generate the resonance pulse, the method requires gate driving circuitry and external control signals. Furthermore, it is necessary to use different inductors for frequency sweeps. A modified version of the Sawyer–Tower circuit with improved bandwidth capabilities [19], involves a switched half-bridge arrangement as a large-signal trapezoidal source and an external *LC* component. Pure thermal/calorimetric measurements provide another way of large-signal C_o loss measurement. However, this only gives an estimation for losses at different v_{DS} values, and therefore, fails to deliver *CV* or *QV* patterns, which are instrumental in understanding large-signal C_o or Q_o dependence on voltage. In addition, at lower power dissipation levels, the accuracy of this method is compromised [22]. In another method, a soft-switched H-bridge configuration is used [21], with a DC voltage source, two DC chokes and a load inductance, and three dc capacitors. The total losses are estimated with a calorimetric approach, where the separation of C_o losses from the total losses is prone to measurement inaccuracies in several stages. Also, the method does not deliver any large-signal *CV* or *QV* patterns.

Although the Sawyer–Tower technique is based on a simple circuit, many factors could affect its valid operating range and subsequent measurements. And discourse on its proper implementation is limited in the technical literature. Recent research on the topic employs the Sawyer–Tower technique [14, 17, 53], and its variations [19], to demonstrate the difference between large and small-signal C_{oss} curves, however, an in-depth explanation of the circuit operation and its limitations is not given. The recent work in [22] addresses some details of the circuit such as the reference capacitor C_{ref} selection and the body-diode to a certain extent. Nevertheless, to the best of our knowledge, an in-depth analysis of the Sawyer–Tower technique for C_o measurement is not available in the literature.

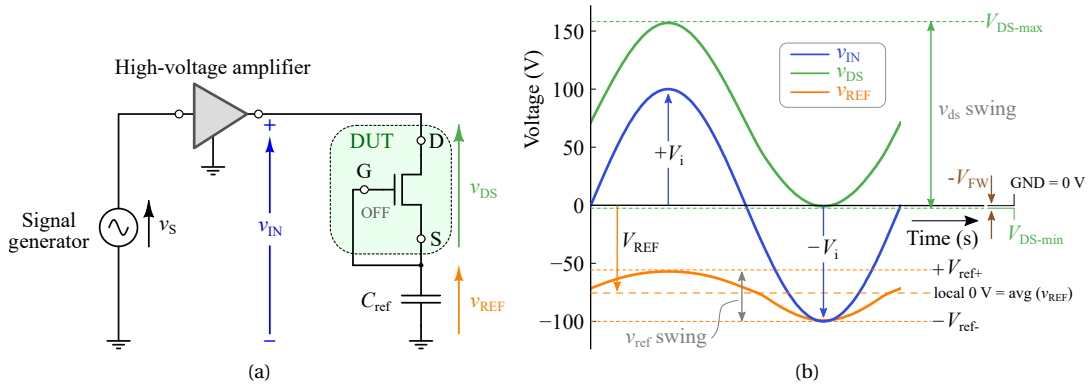


Figure 4.4: (a) Sawyer–Tower circuit and (b) distribution of voltage waveforms under steady-state operation.

Table 4.1: Summary of Voltage Definitions and Steady-State Voltage Values

Voltage	Total instantaneous	dc component		ac component		
	Symbol	Symbol	Value	Symbol	Value	Peak–Peak
Signal-generator output	v_S	V_S	0	v_s	$V_s \sin(\omega t)$	$\pm V_s$
Voltage-amplifier output	v_A	V_A	0	v_a	$V_a \sin(\omega t)$	$\pm V_a$
					$= G \cdot V_s \sin(\omega t)$	
Input to the load	v_{IN}	V_{IN}	0	v_{in}	$V_i \sin(\omega t)$	$\pm V_i$
DUT drain–source	v_{DS}	V_{DS}	$\neq 0$	v_{ds}	-	$-V_{SD}$ to $V_{DS\text{-}max}$
Across C_{ref}	v_{REF}	V_{REF}	$\neq 0$	v_{ref}	-	$-V_{ref\text{-}}$ to $+V_{ref+}$

In the next subsection, we present a detailed discussion on the Sawyer–Tower technique for large-signal output capacitance characterization addressing key factors affecting the accuracy and the range of measurements. It is proved that the Sawyer–Tower circuit, under certain conditions in steady-state operation could make the DUT enter reverse conduction at the negative peak of the input signal, which could compromise the basic assumptions of the method.

4.2 Analysis of the Sawyer–Tower Technique

The operation of the circuit is heavily dependent on all its parameters. For instance, the output resistance and the current limit of the high-voltage amplifier could distort the excitation signal applied on the DUT. The characteristics of C_{ref} depend on the dc-bias voltage and the excitation frequency, f, applied, and therefore, could compromise the measurement accuracy. DUTs with large C_{oss} could result in a low-impedance load, that could exceed the amplifier's loading capabilities. Neglecting the effects of these parameters on the circuit inevitably lead to measurement inaccuracies and false conclusions. Therefore, a thorough investigation of the technical aspects of the method is essential.

4.2.1 Basic Steady-State Operation

The Sawyer–Tower circuit, shown in Figure 4.4(a), results in the steady-state voltage waveforms shown in Figure 4.4(b) and listed in Table 4.1. The fundamental result of this method is a Q_o *vs* v_{DS} curve extracted from measured v_{REF} and v_{DS} data.

We consider a generic field-effect power transistor as the DUT whose gate and source terminals are

shorted to remove the effects of gate capacitance, C_{GS}, from the circuit. Therefore, the only active part of the DUT is its C_o. The drain–source leakage path (generally represented by a large resistance, R_p, in parallel to C_o) is assumed to be of infinite resistance for this part of the analysis. The DUT is connected in series to a linear capacitor C_{ref} to form an equivalent load capacitance

$$C_{eq} = C_o \cdot C_{ref}/(C_o + C_{ref}). \tag{4.1}$$

The capacitance C_{eq} is subjected to an input voltage v_{IN} created by amplifying a low-voltage signal v_S with an excitation frequency of f. Under a steady-state operation, a dc-bias (V_{REF}) is built across C_{ref}, which corresponds to a dc charge, Q_{REF}. Therefore, v_{IN} results only in an ac charge variation on C_{ref},

$$q_{ref} = C_{ref} \cdot v_{ref}. \tag{4.2}$$

Since the DUT and C_{ref} are in series, the same current flows through them (under a steady-state operation), leading to equal charge variations. Thus, we get

$$Q_o \propto C_{ref} \cdot v_{ref}. \tag{4.3}$$

Therefore, the charge variation in C_o is translated to an easy-to-measure ac voltage across C_{ref}: this is the fundamental concept behind the Sawyer–Tower circuit.

4.2.2 Start-up of the Circuit

During the first negative half-cycle, the ac input voltage forces the reference capacitor to be charged in the negative direction through the reverse conduction path of the DUT (a body-diode for Si and SiC MOSFETs and reverse-conduction mode for GaN HEMTs). This results in the dc bias V_{REF}, and hence the dc charge component Q_{REF} in C_{ref}, which in turn makes the reverse conduction path inactive in ideal operation.[4] Note that it could take a few cycles to fully reach this state depending on the circuit design values.

4.2.3 Measurements

The experimental setup that was used in our measurements is shown in Figure 4.5, where the details of the equipment are listed in Table 4.2.

The two voltages v_{REF} and v_{IN} are measured (under steady-state operating conditions) with a Tektronix MDO3104 oscilloscope (1 GHz), accompanied by TPP1000 passive voltage probes (1 GHz).[5] Then v_{DS} is calculated as = $v_{IN} - v_{REF}$. The final QV curves are obtained by mapping Q_o *to* v_{DS} in the time domain, using a computer program such as MATLAB® or Origin. The hysteresis loss can also be calculated using the same programs: a simple subtraction between the areas under two curves (charging–discharging) yields the hysteresis loss.[6]

Note that the direct use of the expressions $Q_o = C_{ref} \cdot v_{ref}$ and $Q_o = C_{ref} \cdot v_{REF}$, found in the literature

[4] In reality, steady-state reverse conduction exists. The reasons are discussed in Section 4.2.7.

[5] The probe-end uses the MMCX square-pin adapter 131-9717-xx.

[6] In our experience, although the Sawyer–Tower circuit is capable of measuring 10 to 20 nanojoules of differences in E_{diss}, our preferred choice for the lower measurement limit is 50 nJ.

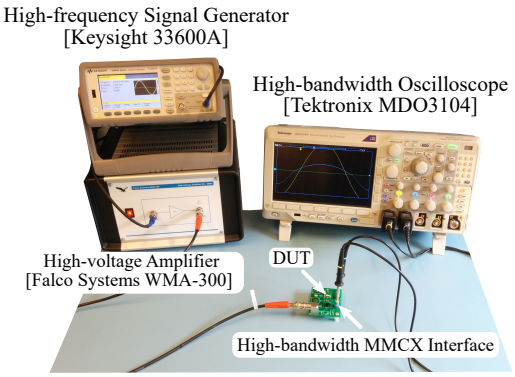


Figure 4.5: Experimental test setup of the Sawyer–Tower measurement technique used to analyse large-signal output capacitance.

Table 4.2: List of Equipment Used for Experimental Analysis

Name	Manufacturer	Description
B1505A	Keysight	Power device analyser / Curve tracer
E4990A	Keysight	50 MHz impedance analyser
33600A	Keysight	Trueform waveform generator
WMA-300	Falco Systems	5 MHz high-voltage amplifier
MDO3104	Tektronix	Mixed domain 1GHz 5GS/s oscilloscope

[13, 17] could lead to inaccurate estimations, as they do not provide the complete behaviour of Q_o *vs* v_{DS} variation. The first does not take into account the zero base-lined variation for Q_o, while the latter incorporates the dc-charge within C_{ref}. To address this problem, we introduce Eq. (4.4):

$$Q_o|_{v_{DS}} = C_{ref}\,(v_{ref} - v_{ref}|_{v_{DS}=0}). \tag{4.4}$$

Eq. (4.4) takes into account the finite reverse voltage of the DUT: the term $v_{ref}|_{v_{DS}=0}$ ensures that $Q_o = 0$ when $v_{DS} = 0$—see Section 4.2.6 for certain practical aspects.

To provide some practical perspective, experimental waveforms of v_{IN}, v_{REF}, and v_{DS} (steady-state) obtained for a GaN device and a Si-SJ device are shown in Figures 4.6(a) and 4.6(b), respectively. For different C_{ref} values, the input voltage must be changed to keep $V_{DS\text{-}max}$ fixed (in our example, we keep this at 400 V). The higher the value of C_{ref}, the smaller the peak–peak variation in v_{ref}. An extensive discussion on the selection of C_{ref} will be given in Section 4.2.5. We also observe that v_{IN} in Figure 4.6(b) is distorted to a certain degree, although it resembles a sinusoid in Figure 4.6(a). The underlying reason is discussed in Section 4.2.4.

In our preliminary experiments, we have realized that the Sawyer–Tower setup is a sensitive circuit that can be affected by several parameters of the equipment used and system parasitics. In addition, no consideration is given in the literature on how the range and behaviour of C_o affect the operation of the entire circuit. These factors are analysed and explained in Sections 4.2.4–4.2.7 with the aid of the detailed circuit in Figure 4.7.

4.2.4 High-Voltage Amplifier and Equivalent Load

A high-voltage amplifier is required to boost the excitation signal (from a signal generator) to test the devices up to their rated voltages (e.g., 650 V). These amplifiers have two important characteristics that

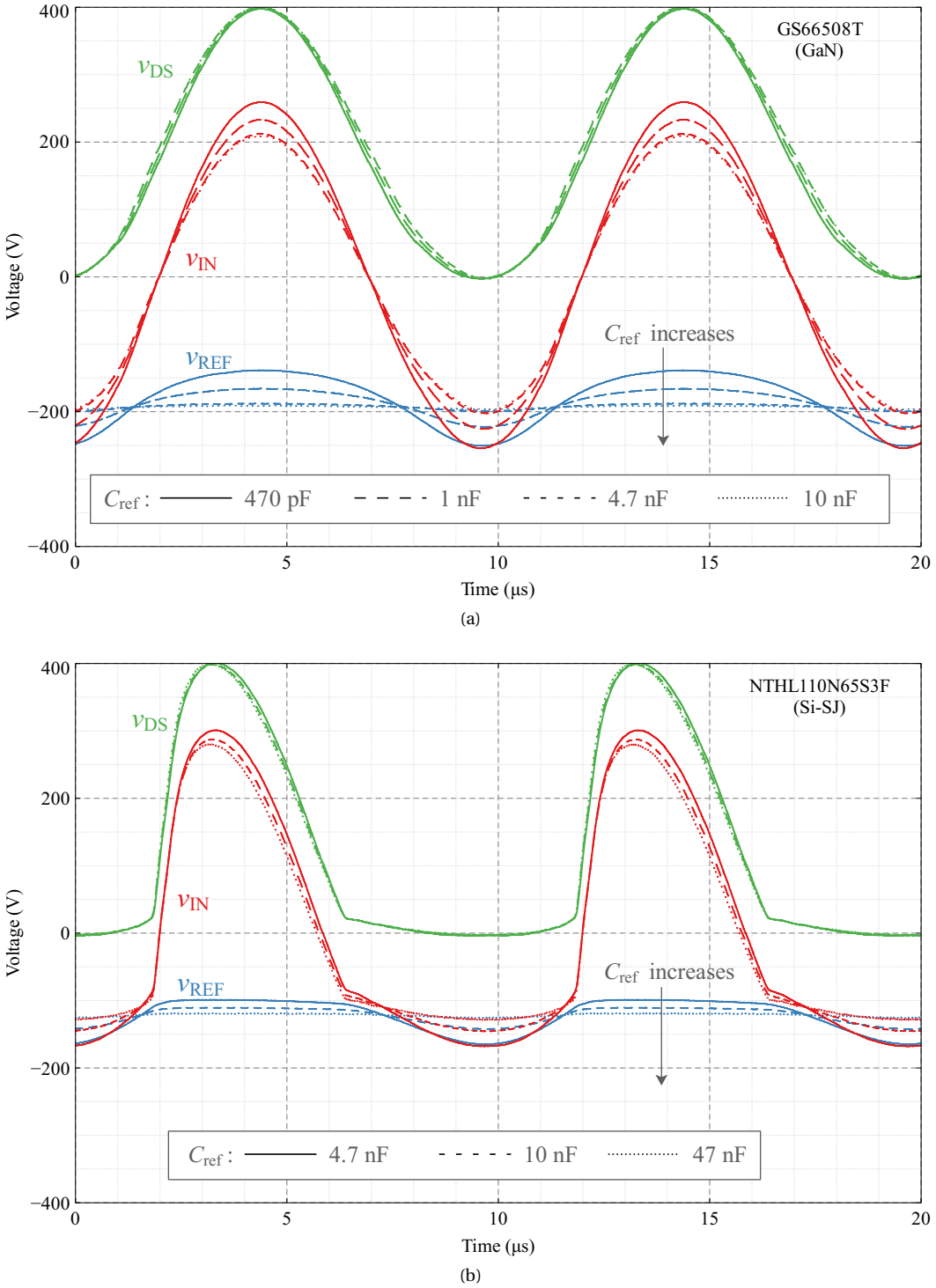


Figure 4.6: Experimental waveforms showing the variation of the voltages v_{IN}, v_{REF} and v_{DS} for different C_{ref} values in the Sawyer–Tower circuit, where the DUT is (a) GS66508T GaN HEMT (650-V and 30-A) and (b) an NTHL110N65S3F Si-SJ MOSFET (650-V and 30-A). All reference capacitors were of C0G type. Conditions: $V_{DS\text{-}max}$ = 400 V and 100 kHz.

could affect the proper operation of the Sawyer–Tower circuit:

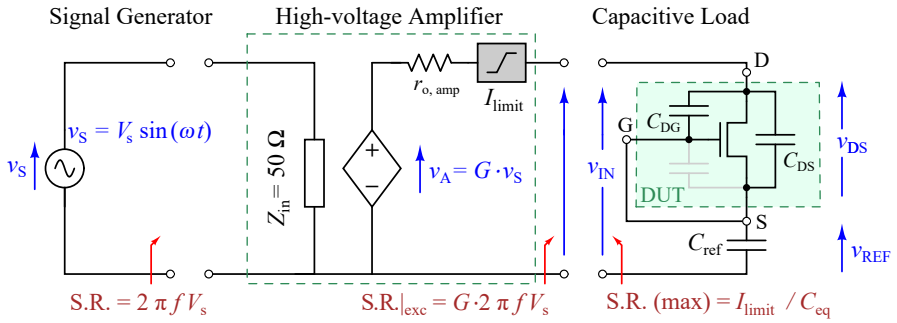


Figure 4.7: Detailed Sawyer–Tower circuit. The following are highlighted: slew-rates at each interface; amplifier output resistance, $r_{o,\,amp}$ and current limit, I_{limit}; and DUT, where $C_o = C_{DG} + C_{DS}$.

1. *Current Limit*, I_{limit}.
2. Finite *Output Resistance*, $r_{o,\,amp}$.

To study these effects independently, we assume the following conditions:

- A sinusoidal excitation signal v_S.
- Ideal C_{eq} with infinite parallel resistance.
- Output slew-rate of the amplifier (hardware-limited), $S.R.|_{amp}$, is larger than the slew-rate of the amplified v_S, $S.R.|_{exc} = G \cdot 2\pi f V_s$. (see Figure 4.7).

$$S.R.|_{amp} \geq S.R.|_{exc} \tag{4.5}$$

These two factors are directly related to the rate of change of load voltage, and therefore, could result in voltage distortions if overlooked. I_{limit} is a practical limit in commercial amplifiers and defines the maximum current through the load. Then the change in the rate of voltage across C_{eq} is limited as given in Eq. (4.6).

$$\text{rate}_1 = \frac{dv}{dt} = \frac{I_{limit}}{C_{eq}} \tag{4.6}$$

The amplifier's $r_{o,\,amp}$ determines the RC time constant for the load and results in the following relation:

$$\text{rate}_2 = \frac{V_i}{4 r_{o,\,amp} C_{eq}}. \tag{4.7}$$

where V_i is the peak of the ac signal v_{in} applied to the load. Here, we have considered four time-constants to reach the maximum load voltage.

Both rates can limit the full propagation of the amplifier output (v_A) to the load.

- if $\text{rate}_2 > \text{rate}_1$, rate_1 becomes dominant and the maximum load slew-rate is determined by I_{limit} and C_{eq}. At the same time, if $S.R.|_{exc} > \text{rate}_1$, the load can't follow the input: v_{IN} becomes distorted as I_{limit} introduces a non-linearity to the circuit.
- if $\text{rate}_1 > \text{rate}_2$, the resultant load slew-rate is limited by $r_{o,\,amp}$, V_i and C_{eq}. If $S.R.|_{exc} > \text{rate}_2$, the load will follow the input voltage shape, but with a gain reduction due to RC limitations.

These distortions are more pronounced when DUTs with large C_{oss} values are tested.

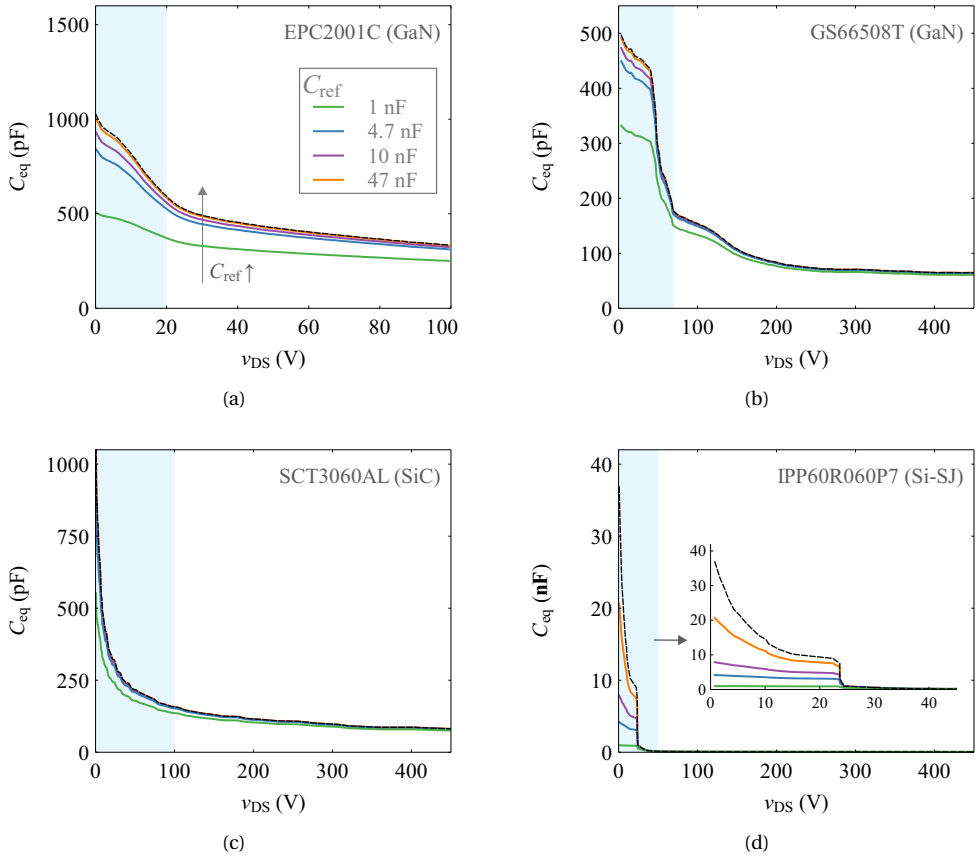


Figure 4.8: C_{eq} versus v_{DS} for (a) EPC2001C(GaN), (b) GS66508T(GaN), (c) SCT3060AL(SiC), and (d) IPP60R060P7(Si-SJ) transistors, for different C_{ref} values. The dashed black lines show the datasheet C_{oss} value. The shaded blue area highlights the "*low* v_{DS} *region*".

4.2.4.1 Effects of C_{oss} and C_{ref}

We base the following analysis on the small-signal output capacitance C_{oss}. For all commercial power transistors, C_{oss} is a monotonically decreasing function of the applied v_{DS}. Especially, in the "*low* v_{DS} *range*" (see Figure 4.8), it is significantly larger (even an order of magnitude) than in the large v_{DS} range. Thus, the load impedance ($Z_{load} = 1/j\omega C_{eq}$) reduces greatly in the low v_{DS} range and results in the following implications:

1. v_{IN} gets distorted at the bottom of its negative half cycle (where the low v_{DS} range occurs) as a higher voltage drops across $r_{o,\,amp}$, clearly depicted in Figure 4.9.

2. the load current can surpass I_{limit} and alter v_{IN}.

3. exceeding the amplifier's power capability at large f values, due to increased load current.

To prevent any signal distortion, a proper C_{ref} value should be selected. As can be seen from Figure 4.9, the lower the value of C_{ref}, the lower the distortion. However, excessive reduction of C_{ref} reduces the available share for the v_{DS} swing (as the ac voltage drop across C_{ref} increases), for a fixed V_i.

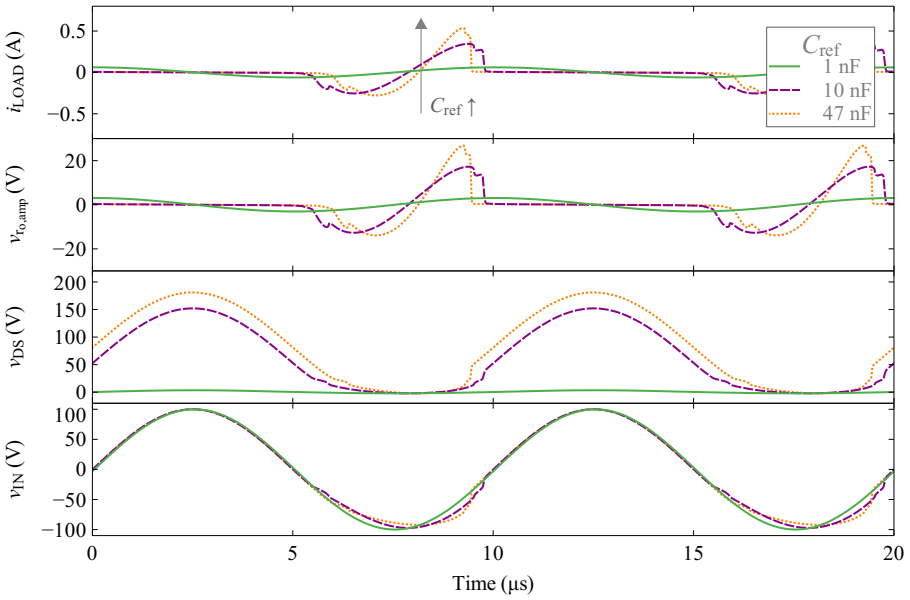


Figure 4.9: LTspice simulation results showing the effects of having a large C_{oss} value in the low v_{DS} range, for f = 100 kHz. The DUT is a Si-SJ MOSFET (IPP60R060P7) with $C_{oss}|_{v_{DS}=0} \approx 40$ nF. The distortion in v_{IN} is intensified with increasing C_{ref} as Z_{load} further decreases.

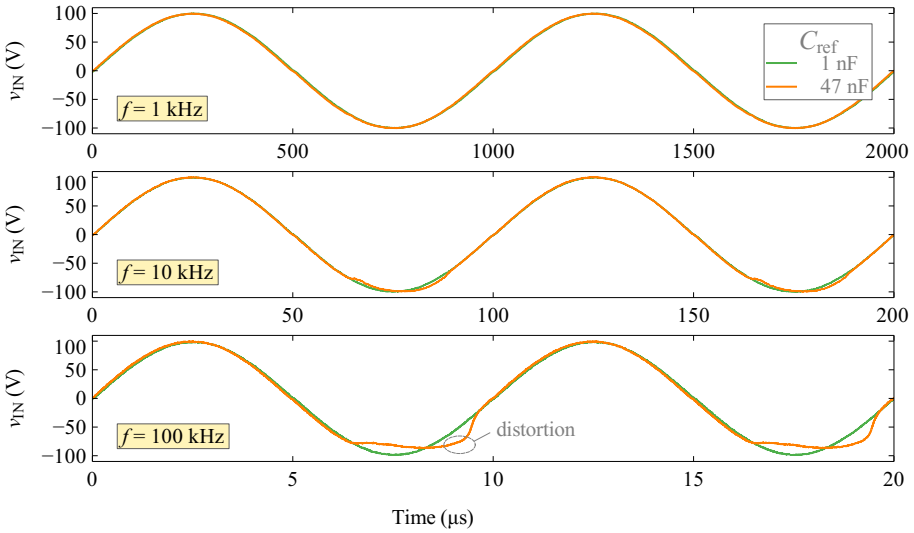


Figure 4.10: Experimental waveforms of v_{IN} for the IPP60R060P7 Si-SJ MOSFET for different excitation frequencies. v_{IN} distorts when C_{ref} is large.

To experimentally support this analysis, Figure 4.10 shows v_{IN} for a Si-SJ MOSFET for different C_{ref} and f values. For the case of C_{ref} = 1 nF ($\approx 0.025 \times C_{oss}|_{v_{DS}=0}$), no distortion occurs as expected; while a clear distortion in v_{IN} appears for the case of C_{ref} = 47 nF ($\approx 1 \times C_{oss}|_{v_{DS}=0}$).

The distortion increases with increasing f as the load impedance gets further lowered. Therefore, for a DUT with large C_{oss}, f should be chosen adequately low so that the amplifier's output-power-capability is respected. In other words, one needs to be aware of the power versus frequency trade-off of voltage amplifiers.

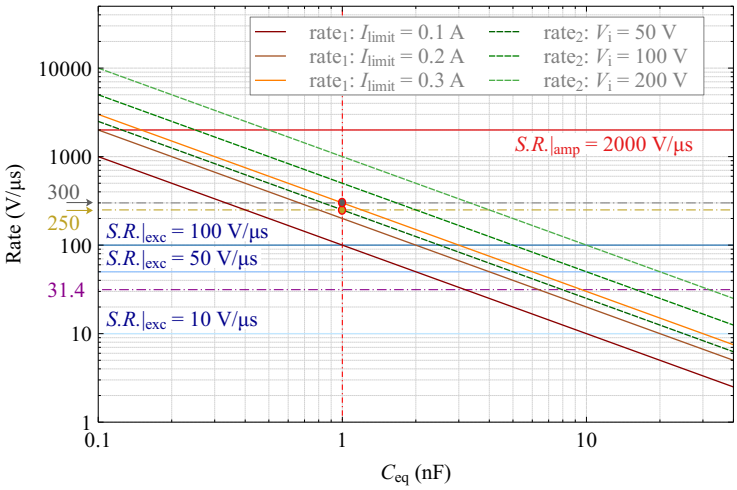


Figure 4.11: Variation of rate$_1$ (in solid diagonal lines for different I_{limit}), and rate$_2$ (in dashed diagonal lines for different V_i with $r_{o,\,amp}$ fixed at 50 Ω) with C_{eq}. Solid blue lines show practical $S.R.|_{exc}$ values while the solid red line shows $S.R.|_{amp}$ for the WMA-300 amplifier.

4.2.4.2 Voltage Amplifier Selection and Slew-Rate Limitations

For the correct implementation of the Sawyer–Tower circuit, the amplifier slew-rate should satisfy Eq. (4.5). At the same time, the circuit parameters should be chosen such that the dominant load slew-rate, $S.R.|_{dominant}$, is higher than $S.R.|_{exc}$.

$$S.R.|_{exc} < S.R.|_{dominant} < S.R.|_{amp} \tag{4.8}$$

Figure 4.11 provides a quick reference chart to evaluate whether the circuit satisfies the slew-rate conditions of Eq. (4.8) for a given C_{eq} value. An example of a good selection is given for an EPC2001C transistor, tested with a WMA-300 amplifier of $S.R.|_{amp}$ = 2000 V/μs and I_{limit} = 300 mA, shown as solid red and orange lines in Figure 4.11, respectively. Consider a sinusoidal excitation of f = 100 kHz, V_s = 1 V, G = 50, $r_{o,\,amp}$ = 50 Ω, and C_{ref} = 47 nF. Then $S.R.|_{exc}$ is calculated to be 31.4 V/μs < $S.R.|_{amp}$. According to Figure 4.8(a), C_{eq} in the low v_{DS} range is 1 nF. Then, rate$_1$ and rate$_2$ are calculated as 300 and 250 V/μs, respectively (equations given in Figure 4.11). Thus, $S.R.|_{dominant}$ = 250 V/μs, and thus, Eq. (4.8) is satisfied. On the other hand, if f is increased to 1 MHz, with everything else unchanged, then $S.R.|_{exc}$ = 314 V/μs, and Eq. (4.8) is no longer satisfied.

4.2.5 Reference Capacitor, C_{ref}

The selection of C_{ref} is of vital importance for the correct operation of the Sawyer–Tower circuit [14, 22, 53]. First, we derive a useful new equation to calculate C_{ref} based on design requirements. We assume that there is no distortion in v_{IN} due to the slew-rate limitations and that C_{ref} is ideal and linear.

To derive an equation for the value of C_{ref}, consider C_o characterization of a DUT for a v_{DS} swing of $V_{DS\text{-}min} = -V_{FW}$ to $V_{DS\text{-}max}$, and an input voltage swing of $\pm V_i$. Considering the load-side circuit; and

at $v_{DS} = V_{DS\text{-}max}$, the following holds:

$$+ V_i = V_{BIAS} + V_{ref+} + V_{DS\text{-}max}. \tag{4.9}$$

This equation can be solved further by realising that for steady-state, $V_{BIAS} = V_{REF} = (-V_i + V_{FW}) + V_{ref\text{-}}$, where $-V_{FW}$ is the device's dc voltage drop during reverse conduction (see Section 4.2.7). Substituting this into Eq. (4.9) gives,

$$2\,V_i = V_{FW} + V_{DS\text{-}max} + V_{ref\text{-}} + V_{ref+}. \tag{4.10}$$

The term "$V_{ref\text{-}} + V_{ref+}$" can be substituted by using Eq. (4.11) and Eq. (4.12), which are easily derived from Eq. (4.4). Simplifying, we get an essential equation in Eq. (4.13) to calculate the value of C_{ref} required for a given v_{DS} swing of $V_{DS\text{-}max}$.

$$Q_{o\text{-}max} = C_{ref}\,(V_{ref+} - v_{ref}|_{v_{DS}=0}) \tag{4.11}$$

$$Q_{o\text{-}min} = C_{ref}\,(-V_{ref\text{-}} - v_{ref}|_{v_{DS}=0}) \tag{4.12}$$

$$C_{ref} = \frac{Q_{o\text{-}max} - Q_{o\text{-}min}}{2\,V_i - V_{DS\text{-}max} - V_{FW}} \tag{4.13}$$

Here, $Q_{o\text{-}max}$ is the minimum charge stored in the DUT, while $Q_{o\text{-}min}$ is the minimum. For practical cases, $Q_{o\text{-}min}$ can be assumed to be negligible compared to $Q_{o\text{-}max}$: the small-signal $Q_{oss\text{-}max}$, which can be easily estimated from datasheet-based C_{oss} curves, is a good first approximation for $Q_{o\text{-}max}$.

For example, consider an EPC 2001C that should be subjected to $V_{DS\text{-}max} = 50$ V where V_i is limited to 50 V. The device has $Q_{o\text{-}max} \approx 30$ nC at 50 V, and therefore, C_{ref} should be higher than 600 pF according to Eq. (4.13). For this DUT, calculated voltage swings in C_{ref} for six different C_{ref} values are graphically illustrated in Figure 4.12. It is observed that larger C_{ref} allows for a larger v_{DS} swing. And as the value of C_{ref} is decreased and approaches $C_{oss}|_{V_{DS\text{-}max}}$ (this is between 450 to 350 pF for swings above 40 V), the available v_{DS} swing significantly reduces.

4.2.5.1 Selecting the Type of C_{ref}

There are mainly two commonly used multi-layer ceramic capacitor (MLCC) types available in the market that are classified upon their dielectric class (of EIA standard): Class I and Class II.

Class I dielectric based capacitors, also known as C0G/NP0 temperature compensating capacitors, are based on non-ferroelectric material and exhibit a fixed capacitance with the bias-voltage: measured characteristics for this type of capacitor is shown in Figure 4.13(a). On the other hand, the capacitance of Class II capacitors (e.g. X7R, X7T and X5R types) decrease with the bias-voltage as shown in Figure 4.13(a).

Figure 4.13(b) shows experimental Q_o curves for an EPC2001C transistor using both types of capacitors with a nominal value of 47 nF (small-signal curve for Q_{oss} is shown with a dashed black line). The curve for the X7T type shows a clear deviation from the C0G/NP0 type: an 8% error is observed in Q_o where the deviation reaches up to 3.7 nC for $v_{DS} = 100$ V. C0G/NP0 (Class I) is, thus, the preferred type because C_{ref} should be independent of V_{BIAS} throughout the whole v_{DS} range.

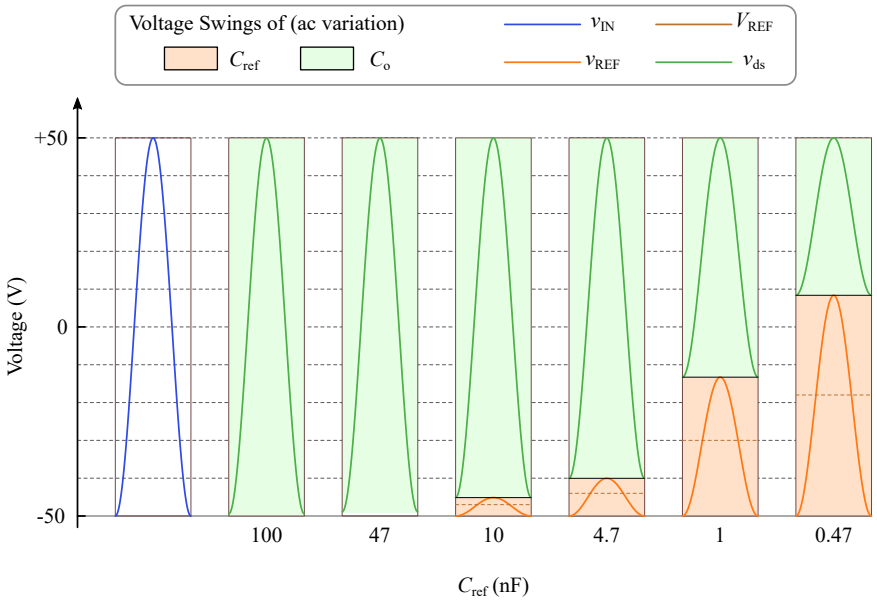


Figure 4.12: The distribution of the available voltage swing for the DUT (shaded area in green) and the reference capacitor (shaded area in orange) upon the selection of C_{ref} values of 100, 47, 10, 4.7, 1, and 0.47 in nF. The baseline of v_{ds} is placed on top of the peak of v_{REF} to show how the input voltage to the load, v_{IN}, is shared between the two swings: v_{IN} with a swing of 50 V is considered. The DUT is an EPC2001C transistor and results are based on LTspice simulations. When the value of C_{ref} is decreased, the ac swing (v_{ref}) across it increases and the dc bias V_{REF} shifts upwards, and consequently, the swing available for v_{DS} reduces.

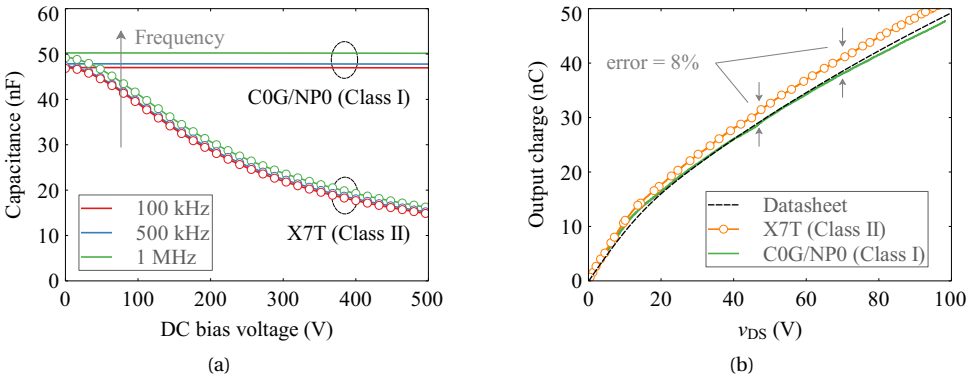


Figure 4.13: (a) Capacitance *vs* bias-voltage of C_{ref}, measured with a Keysight B1505A curve tracer, and (b) experimental Q_o curves for an EPC2001C transistor at f = 100 kHz using same the C_{ref}. A Class I NP0/C0G capacitor (TDK CGA8R4NP02J473J320KA) and a Class II X7T capacitor (TDK CGA5L1X7T2J473K160AC) with nominal values of 47 nF are compared.

4.2.5.2 Frequency Dependence of C_{ref}

Although C0G/NP0 type has a fixed capacitance throughout the voltage range, related frequency effects should be considered. On the one hand, the effective capacitance seen from the external circuit increases as f approaches the self-resonant frequency (SRF) of the capacitor (due to parasitic inductance in the package of the capacitor)—see Figure 4.14. On the other hand, the equivalent series resistance, R_{ESR}, of the capacitor increases with f. Due to these two reasons, f has an upper limit for a given C_{ref} value and type.

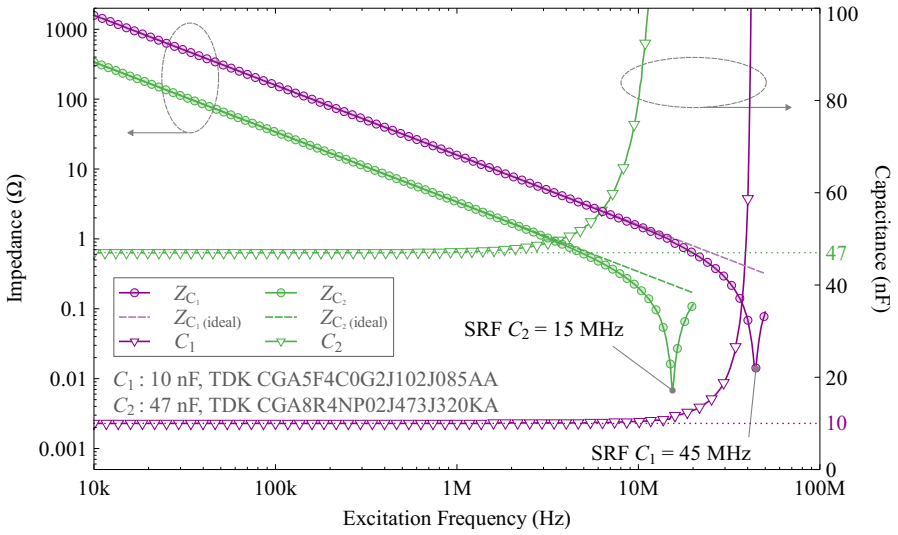


Figure 4.14: Variation of impedance and capacitance of two C0G/NP0 capacitors (C_1 of 10 nF and C_2 of 47 nF) measured with a Keysight E4990A Impedance Analyser. The actual impedance values (Z_{C_1} and Z_{C_2}) starts to deviate from their ideal ones (indicated by dashed lines) when approaching their SRFs.

Measured impedance and capacitance values of two different NP0/C0G capacitors (C_1 and C_2) are shown in Figure 4.14. The impedances of C_1 and C_2 decrease significantly as f approaches SRF; this is a result of the overall effect of the increase of both measured capacitance (dominant) and R_{ESR} with f (up to SRF). The decreasing impedance results in an overall increase in the load current and, hence, an increase in the voltage drop across R_{ESR}. The measured v_{ref}, under steady-state conditions, is now given by Eq. (4.14).

$$v_{\text{ref}}\big|_{\text{measured}} = v_{\text{ref}}\big|_{\text{actual}} + i_{\text{LOAD}} R_{\text{ESR}} \tag{4.14}$$

The product $i_{\text{LOAD}} R_{\text{ESR}}$ adds an error to the calculated Q_{o} value that gets higher as f approaches SRF. Operation close to the SRF also introduces a deviation of C_{ref} from its nominal value, adding further to the Q_{o} estimation error. The optimal f range is discussed in Section 4.2.5.3, showing the upper bound for f when selecting a commercial capacitor.

4.2.5.3 Selecting the Value of C_{ref}

A map of possible selections for C_{ref} based on Eq. (4.13), for a given V_{i}, is shown in Figure 4.15. Four different families of curves for V_{i} are chosen between 100 V to 600 V. Additionally, five $Q_{\text{o-max}}$ values between 5-120 nC that corresponds to commercial MOSFETs and GaN HEMTs are considered. For instance, consider V_{i} = 100 V and a 50% voltage swing across a DUT with $Q_{\text{o-max}}$ = 50 nC at $V_{\text{DS-max}}$ = 100 V: the optimum C_{ref} is then calculated as 500 pF (assume $V_{\text{FW}} \approx 0$).

For a given C0G/NP0 MLC capacitor, f should be chosen in the flat part of the C *vs* f curve. This range normally extends up to SRF/10. The acceptable range of f values for a selection of commercial capacitors is shown in Figure 4.16.

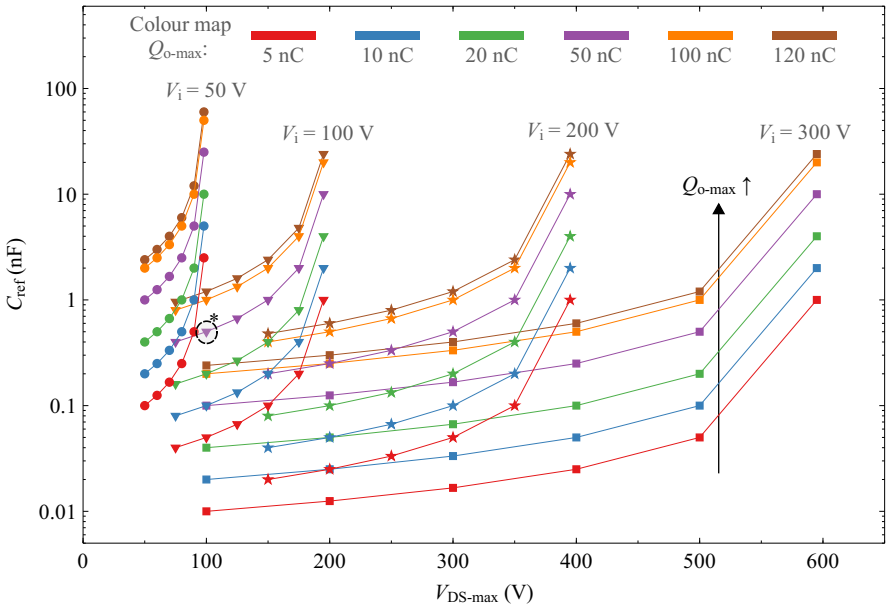


Figure 4.15: Selection chart of C_{ref} value for a required $V_{DS\text{-}max}$ based on the input voltage range V_i and device's $Q_{o\text{-}max}$. $Q_{o\text{-}min} \approx 0$ for practical cases.

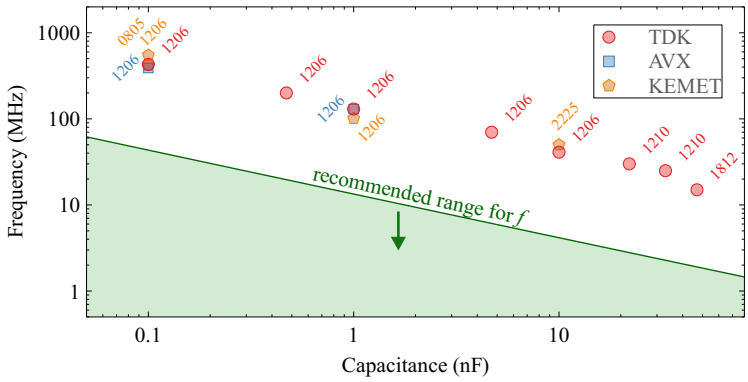


Figure 4.16: Self-resonant frequency versus capacitance for commercial C0G/NP0 MLC capacitors (500/630 V): marked by three different symbols for three different manufacturers. The labels indicate the package.

4.2.6 Experimental Evaluation of the Effects of C_{ref}

After following the above-mentioned basic principles in selecting C_{ref}, here we carry out additional experimental investigations on the use of different C_{ref} values for a given device, while $V_{DS\text{-}max}$ is fixed. We specifically study if (and how) the *QV* curves and the resulting E_{diss} values change when the value of C_{ref} is altered.

Figure 4.17 plots large-signal *QV* curves of the output capacitance of six different devices (two each from Si, SiC, and GaN devices that will be studied in Section 4.3). For the GaN and SiC devices, we have considered five different C_{ref} values, whereas for the Si devices we have considered three different C_{ref} values in the nF range. All the devices exhibit identical patterns for the C_{ref} values from 4.7–47 nF: the value of Q_o at 400 V also does not show any variation. The same conclusions can be made for the C_{ref} values from 470 pF and 1 nF with relation to devices GS66508T [Figure 4.17(a)] and C3M0065090D

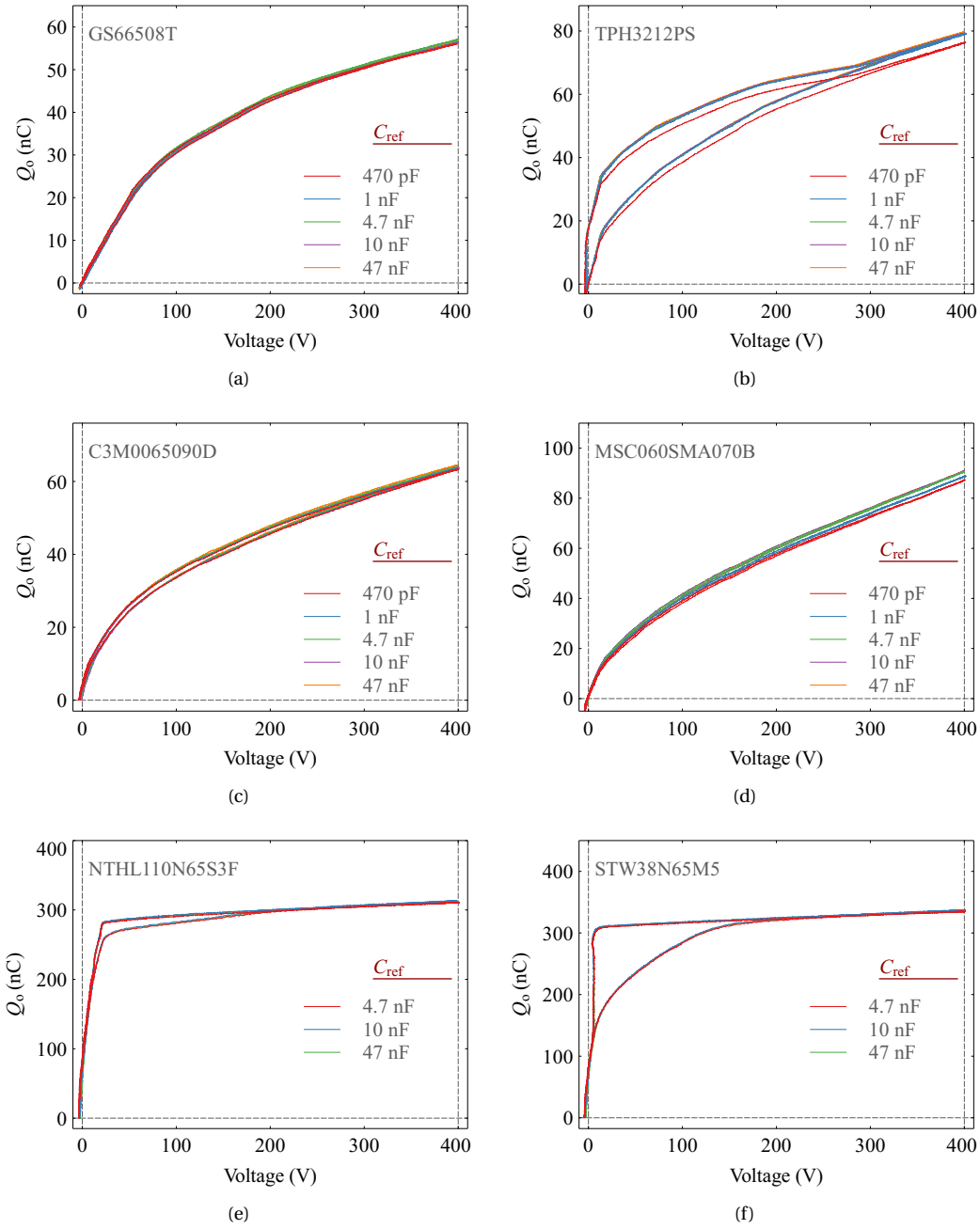


Figure 4.17: *QV* patterns obtained using the Sawyer–Tower circuit for different C_{ref} values. Six different devices are considered as the DUTs (please see Table 4.3 in Section 4.3 for the specifications of the devices): (a)–(b) GaN devices; (c)–(d) SiC devices; and (e)–(f) Si-SJ devices. Conditions: $V_{DS\text{-}max}$ = 400 V and 100 kHz.

[Figure 4.17(c)]. A slight decrease in the Q_o at 400 V is observed for device MSC060SMA070B for two lowermost C_{ref} values. A similar decrease in Q_o can be observed for device TPH3212PS [Figure 4.17(b)], however only for the case where C_{ref} = 470 pF.

On the one hand, we saw in Section 4.2.4.1 that a low C_{ref} value will avoid any distortions in v_{IN}. On the other hand, the aforementioned shift (negative offset in the direction of the y-axis) in Q_o, for

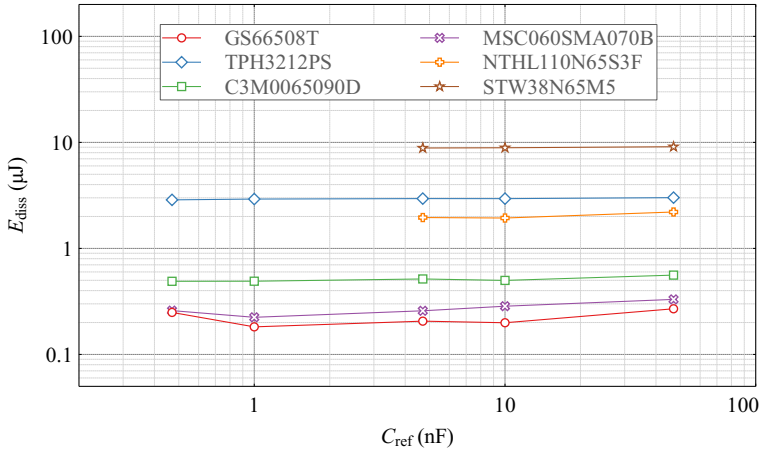


Figure 4.18: Variation of E_{diss} with C_{ref} for the devices considered in Figure 4.17. Conditions: 400 V and 100 kHz.

C_{ref} values lower than 1 nF, indicates that there is a lower limit for C_{ref} as well. This shift in Q_o could be related to a limitation of Eq. (4.4) for test cases with low C_{ref} and certain device structures. We believe this requires additional investigations. It should also be noted that the shift in Q_o is not related to any hysteresis related effects. As Figure 4.18 indicates, the resulting E_{diss} values related to all six devices do not show considerable variations throughout the whole range of C_{ref} values. The slight variations in E_{diss} for the devices GS66508T and MSC090SMA070B are also not significant and expected as E_{diss} values are around 100–200 nJ, which are close to the lower end of the measurement limits.

In summary, Figure 4.18 shows that E_{diss} is independent of the value of C_{ref} for the practical operation of the circuit. However, the value of Q_o could start to show slight offsets for small C_{ref} values, and therefore, it is advisable to test several values of C_{ref} [higher than the value determined by Eq. (4.13)] to confirm the coincidence of the QV curves.

4.2.7 The Reverse Conduction of the DUT

The Sawyer–Tower circuit is based on the fundamental assumption that the current through C_{ref} and the device's C_o are always equal when the circuit is operating under steady-state conditions, meaning that there is no reverse conduction (third-quadrant operation) of the DUT [22, 59]. Our investigations show that this assumption does not hold for certain design/operating conditions.

To elucidate, we consider that the device has reached steady-state conditions, where the dc bias of C_{ref} is given in Eq. (4.15), in which V_{FW} is assumed to be a fixed dc voltage drop independent of the level of reverse current.

$$V_{BIAS} = V_{REF} = (-V_i + V_{FW}) + V_{ref\text{-}}. \tag{4.15}$$

The corresponding circuit is given in Figure 4.19(a), where we get,

$$v_{DS} = v_{IN} - v_{ref} - V_{BIAS}. \tag{4.16}$$

Applying Eq. (4.16) for the negative peak of v_{IN}, and substituting V_{BIAS} from Eq. (4.15), we get $v_{DS} = -V_{FW}$. This shows that the reverse conduction is inhibited as long as $v_{DS} \geq -V_{FW}$.

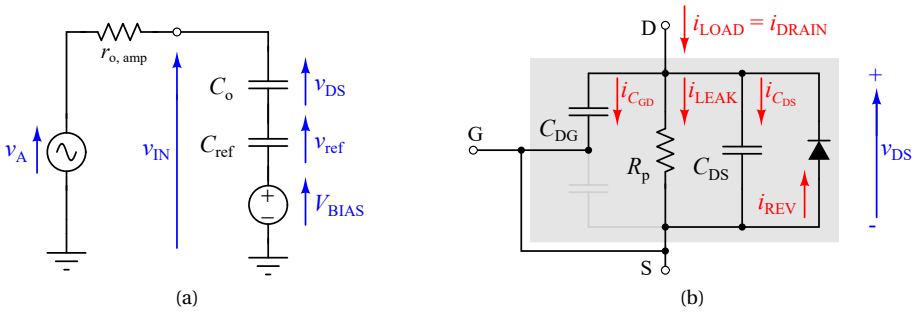


Figure 4.19: (a) Sawyer–Tower circuit under steady-state operation where $v_{REF} = v_{ref} + V_{BIAS}$, and (b) a model of the DUT showing the leakage current i_{LEAK}.

4.2.7.1 Experimental Observation of Reverse Conduction

In our experiments, however, clipping of v_{DS} at $-V_{FW}$ level was observed, indicating steady-state reverse conduction of the DUT. This effect is shown in Figure 4.20 for several transistors. The three GaN HEMTs show clipped v_{DS} values of -1.1 V, -1.8 V, and -1.2 V respectively for $f = 1$ kHz, while the SiC device shows clipping at -0.9 V. The clipping period increases with decreasing f as seen in Figure 4.20 for $f = 1$ and 10 kHz.

The effect of steady-state reverse conduction on the Sawyer–Tower technique can be directly observed in Figure 4.21, which shows the resulting v_{DS} *vs* Q_o curves. For both transistors, Q_o curves show a flat region at the bottom of the discharge path; this indicates that C_o stops discharging and the DUT starts to conduct in reverse mode. During this period the assumption $Q_o \propto C_{ref} \cdot v_{ref}$ is no longer valid, leading to false conclusions on the existence of hysteresis for Q_o. For example, for the GaN device in Figure 4.21(b), an E_{diss} of 51 nJ is observed at 10 kHz. It increases up to a significant 325 nJ at 1 kHz, where the underlying reasons are discussed in Section 4.2.7.3. These losses should not be considered as due to C_o.

4.2.7.2 Identification of Underlying Reasons

This reverse conduction happens because C_{ref} accumulates some positive dc charge, ΔQ_+, that results in a slight positive addition to its steady-state dc bias. The new bias can be written as $V_{BIAS} + \Delta Q_+ / C_{ref}$, which results in

$$v_{DS} = -V_{FW} - \Delta Q_+ / C_{ref} < -V_{FW}, \tag{4.17}$$

allowing reverse conduction to take place. The small reverse currents, indicated by the small reverse voltages, lead to the conclusion that the slight dc bias $\Delta Q_+ / C_{ref}$ is related to the OFF-state drain-source leakage of the DUT.

To support this theory, a simulation was carried out in which the leakage was modelled by a resistance R_p, placed across the device's drain and source, as shown in Figure 4.19(b). Results for an EPC2001C device are shown in Figure 4.22, where R_p is changed from 100 kΩ to 10 MΩ to model devices with high-leakage currents (1 mA) and low-leakage currents (50 μA). For low R_p values, the leakage current ($i_{LEAK} = i_{R_p}$) is large enough to cause a clipping of v_{DS} at -1.1 V, as shown in the zoomed inset. The reverse conduction is also confirmed by the flattening of C_o current, i_{C_o}, during this period.

Therefore, the reverse conduction due to device leakage causes additional DUT loss that could be

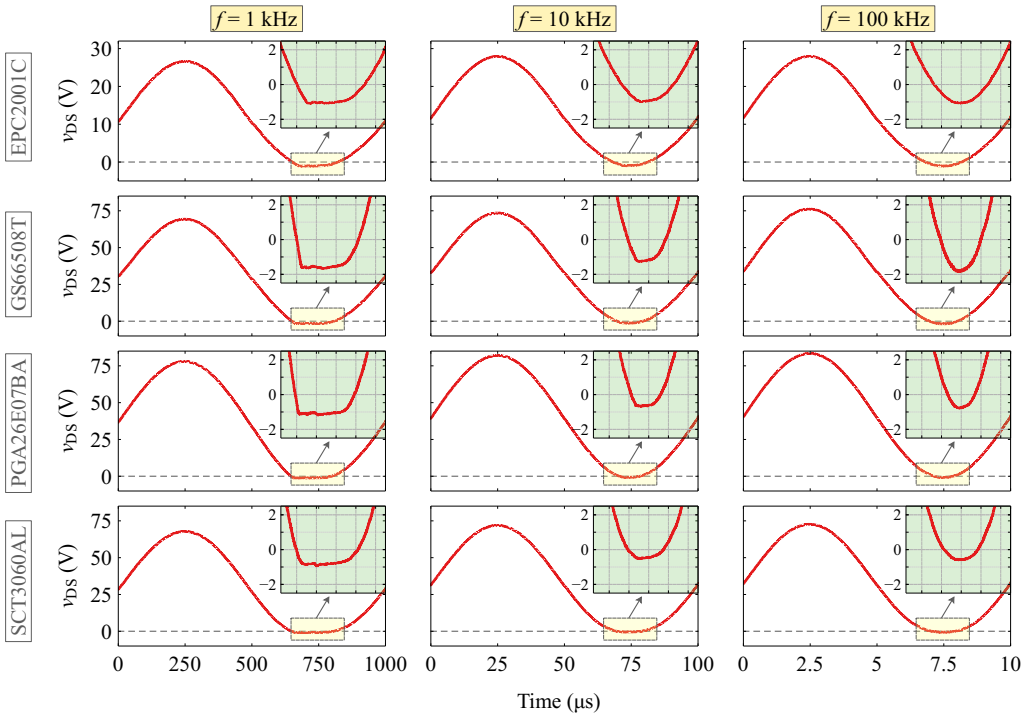


Figure 4.20: Experimental waveforms of v_{DS} showing steady-state reverse conduction for DUTs: GaN HEMTs; EPC2001C, GS66508T, PGA26E07BA; and SiC device SCT3060AL. Negative clipping of v_{DS} is seen in all the cases for f = 1 kHz and 10 kHz. C_{ref} of 1 nF was used.

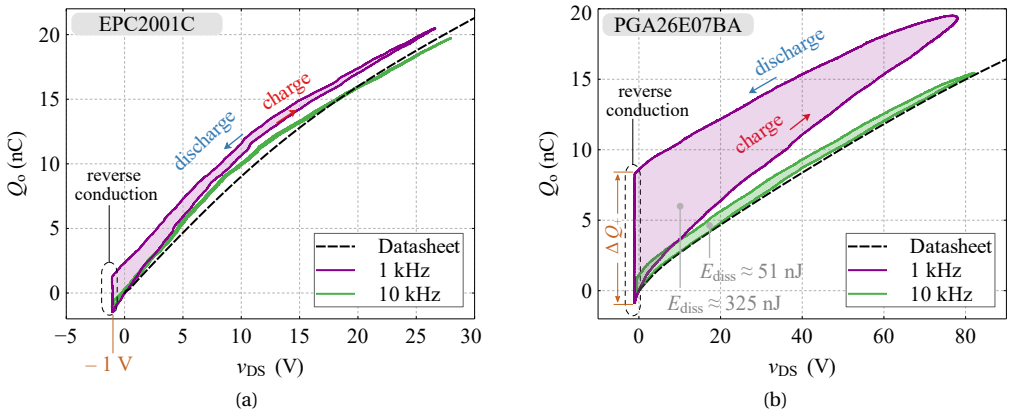


Figure 4.21: Experimental v_{DS} *vs* Q_o curves for (a) EPC 2001C, and (b) PGA26E07BA transistors, showing hysteresis paths and E_{diss} losses that are not due to C_o, but due to an artefact of the steady-state reverse conduction of the DUT. For the PGA26E07BA device, at 10 kHz, this creates an E_{diss} loss of 51 nJ, while it increases up to 325 nJ at 1 kHz. Note that, here we have used Q_o as the x-axis and v_{DS} as the y-axis.

misinterpreted as Q_o hysteresis loss, thus, compromising the use of the Sawyer–Tower technique. This problem can be mitigated by correctly choosing the range of f as discussed in Section 4.2.7.3.

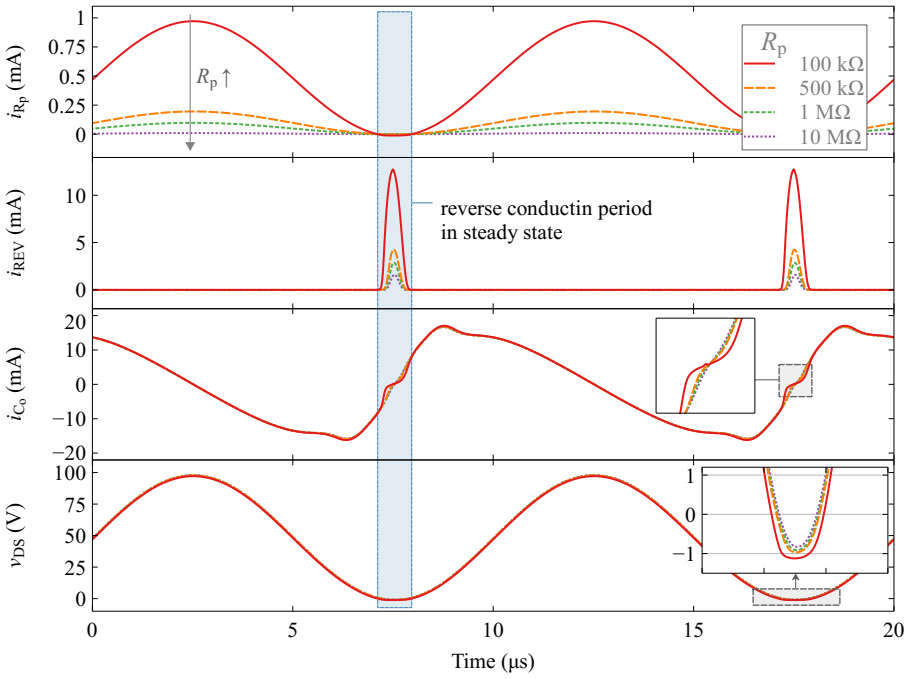


Figure 4.22: LTspice simulation results showing the effect of device leakage (by changing R_p) in creating a reverse conduction period during the steady-state operation of the Sawyer–Tower circuit. v_{DS} clipping at -1.2 V shows clear reverse conduction. The DUT consists of an EPC 2001C device model and an external resistance R_p, placed across the device's drain and source, to create different leakage levels. f = 100 kHz, v_A = ±50 V, C_{ref} = 47 nF and $r_{o,\,amp}$ = 50 Ω.

4.2.7.3 Minimizing Steady-State Reverse Conduction of the DUT

To minimize the effects of the steady-state reverse conduction, f should be chosen such that the resulting extra positive dc charge, ΔQ_+, due to leakage is at least two orders of magnitudes lower compared to the device's reported Q_o range to have an error less than 1%.

For the worst case, where the leakage current is at maximum ($I_{LEAK\text{-}max}$), the charge ΔQ_+ is written as in Eq. (4.18), where $T = 1/f$ and T_{rev} is the duration of the reverse conduction.

$$\Delta Q_+ = I_{LEAK\text{-}max} \cdot (T - T_{rev}) \tag{4.18}$$

For all practical purposes, we can assume $T \gg T_{rev}$, and thus,

$$\Delta Q_+ \propto \frac{I_{LEAK\text{-}max}}{f}. \tag{4.19}$$

This reveals that ΔQ_+ increases with decreasing f. At low-enough frequencies, ΔQ_+ becomes comparable to devices' Q_o values and could cause significant errors in estimated Q_o. This is illustrated in Figure 4.23, where $\Delta Q_+ \approx I_{LEAK\text{-}max}/f$ is used with practical device leakage currents. For example, if a device with $I_{LEAK\text{-}max}$ = 100 μA is subjected to a Q_o swing of 100 nC (dashed orange line), the error changes from 1% to 10% when f changes from 100 kHz to 10 kHz.

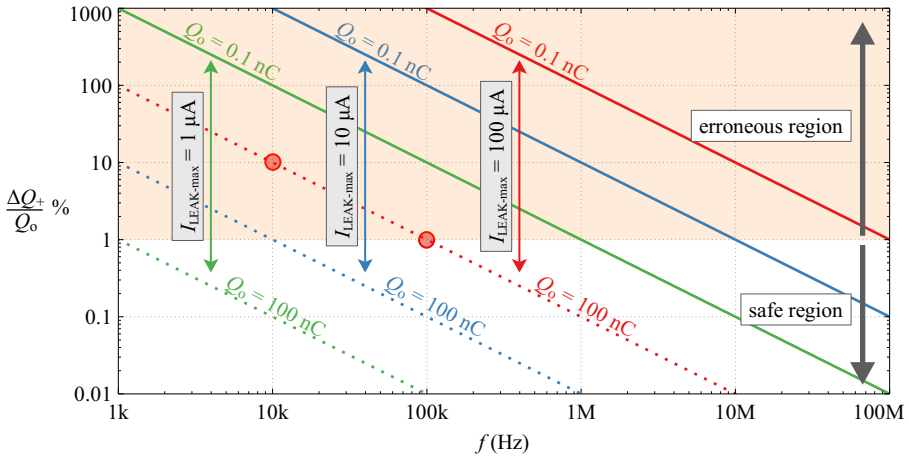


Figure 4.23: Variation of the ratio between ΔQ_+ and device Q_o values, with f. For each case of $I_{\text{LEAK-max}}$, the dashed and solid lines correspond to a change of Q_o from 100 to 0.1 nC, respectively.

4.3 Output-Capacitance Loss in Soft-Switching Circuits

In Chapter 2, the hysteresis energy loss in C_o in large-signal operation was introduced as a function of the maximum (or peak) voltage, V_p, across the device's drain–source terminals. We repeat the equation here for convenience:

$$E_{\text{diss}} = \int_0^{Q_1} v_{\text{DS}}\, dQ - \int_{Q_1}^0 v_{\text{DS}}\, dQ, \tag{4.20}$$

where Q_1 is the output charge for a given V_p (i.e., $Q_1 = Q_o|_{v_{\text{DS}}=V_p}$). To be precise, Eq. (4.20) should be considered for a given excitation type on C_o.[7]

Here, we investigate the practicality of this equation under the excitation[8] in a Sawyer–Tower circuit: for example, we ask the question does E_{diss} stay constant with V_p for some devices. On the other hand, it is important to identify device types where E_{diss} shows significant variation with V_p. In this case, E_{diss} adds an extra constraint on deciding the maximum voltage across a switching device for a given HF or VHF application. This is especially important in resonant converters, for example, in the classical class-E inverter where the device voltage stress could be quite high [42]. Even for converters with low voltage stresses, such as the class-ϕ_2 inverter [50], the circuit components are selected and tuned to achieve a given V_p value. Prior knowledge on the dependence of hysteresis energy losses with V_p for the available devices would allow selecting the most suitable operational voltage range for the circuit. In light of this, the quantitative variation of the E_{diss} value with V_p has been published for some commercial devices [17, 19, 22]. Although this provides means of selecting a suitable device with lower losses, the understanding of how QV patterns vary with V_p for different device technologies is important in identifying the root cause for E_{diss}, and consequently, improving device performance. Such an understanding will also aid in developing more realistic SPICE models to account for hysteresis losses.

Using the Sawyer–Tower technique, here we examine four prominent field-effect transistor technologies in detail for their output-capacitance hysteresis loss. Especially, we will observe how their QV patterns change with V_p. This allows the identification of voltage ranges upon where the hysteresis

[7] The importance of this point is largely discussed in Chapter 5.
[8] We consider the case where the signal generator outputs a pure sinusoid.

patterns emerge. The frequency dependencies are also studied. In our experiments, we concern ourselves with the soft-switching losses in the frequency range of 10 kHz to 1 MHz. The operation in higher frequencies is discussed in Section 4.6.1, with an experimental demonstration in Chapter 7.

Based on the results of this section, an overview of the *QV* hysteresis patterns between different device structures is provided in Section 4.6.1.

4.3.1 Measurement Approach and Basic *QV* Patterns

The test circuit operates such that the excitation voltage across the device drain–source terminals is sinusoidal,[9] while the gate–source terminals are shorted (i.e., $v_{GS} = 0$ V). Si, Si-SJ, SiC and GaN devices (in the range of 500 to 900 V_{DSS}) are tested up to a V_p of 400 V. To make a comparative study, twelve FETs are selected such that they have a current rating of around 30 A. The part numbers, device technologies and other important details from the datasheets of the selected FETs are tabulated in Table 4.3.

[9] This is the ideal situation. Although the output of the signal generator is sinusoidal, v_{DS} could deviate from the ideal form due to the reasons discussed in Section 4.2.4.1.

Table 4.3: Devices Evaluated in the Study (Section 4.3)

Index	Technology	Voltage (V)	Part Number	Manufacturer	Current Rating (A) @ T_C = 25 ˚C	$R_{DS(on)}$ (mΩ) typical	Package
Si-1	Si (planar/conventional)	500	SiHG32N50D	Vishay Siliconix	30	125	TO-247
Si-2	Si-SJ	650	NTHL110N65S3F	ON Semiconductor	30	98	TO-247
Si-3	Si-SJ	650	IPW65R110CFD	Infineon	31	99	TO-247
Si-4	Si-SJ	650	STW38N65M5	STMicroelectronics	30	73	TO-247
SiC-1	SiC	700	MSC090SMA070S	Microsemi	25	90	D3PAK
SiC-2	SiC	650	SCT3080AL	ROHM Semiconductor	30	80	TO-247
SiC-3	SiC	900	C3M0065090D	Cree	36	65	TO-247
SiC-4	SiC (cascode)	650	UF3C065080K3S	UnitedSiC	31	80	TO-247
GaN-1	GaN	650	GS66508T	GaN Systems	30	50	GaN*PX*
GaN-2	GaN	600	IGOT60R070D1	Infineon	31	55	PG-DSO-20-87
GaN-3	GaN	600	PGA26E07BA	Panasonic	31	56	DFN 8X8
GaN-4	GaN (cascode)	650	TPH3212PS	Transphorm	27	72	TO-220

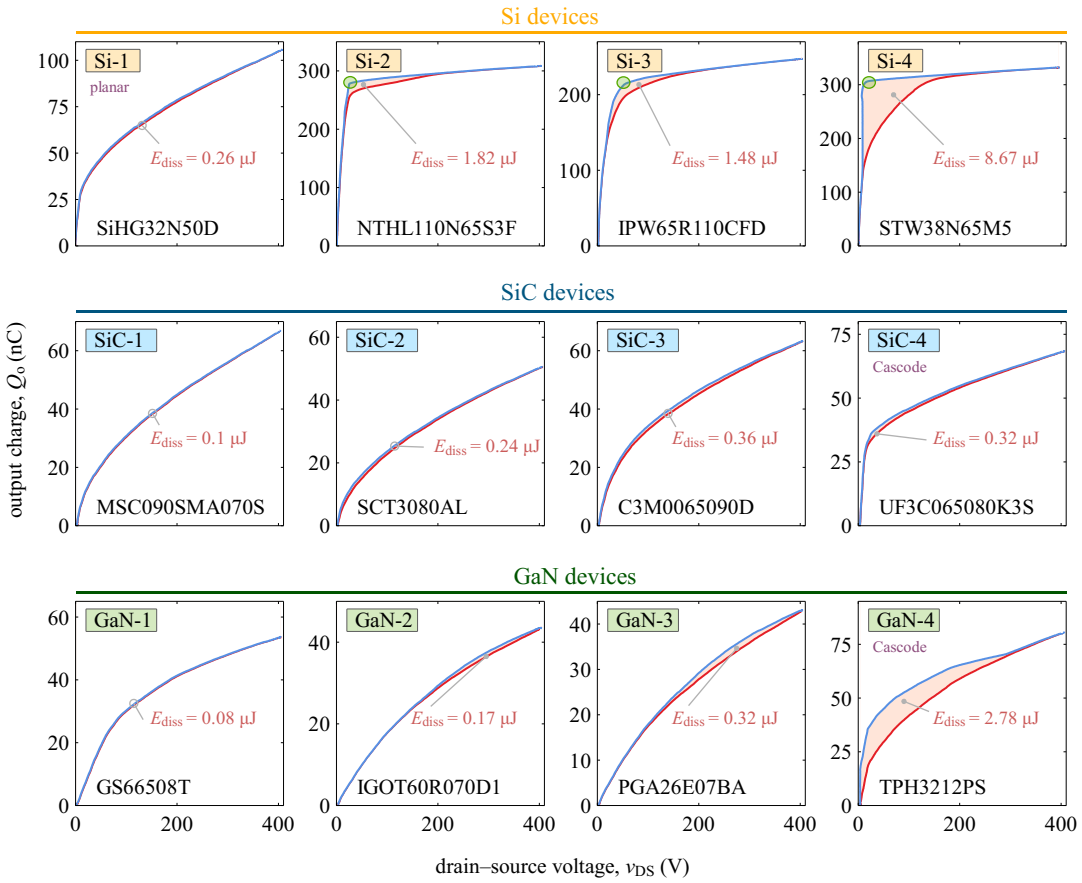


Figure 4.24: Experimental QV (Q_o versus v_{DS}) curves of twelve different power transistors (voltage rating between 500–900 V and current rating around 30 A): planar/conventional Si device Si-1, Si-SJ devices Si-2 to Si-4, SiC devices SiC-1 to SiC-4 and GaN devices GaN-1 to GaN-4. The details of the devices are listed in Table 4.3. The solid red and blue lines correspond to charging and discharging paths, respectively; the hysteresis energy loss E_{diss} is indicated by the area between the two curves (shaded in orange colour). The measurements were performed using the Sawyer–Tower technique at V_p = 400 V. The excitation signal is a sinusoid of f = 100 kHz. A C_{ref} of 1 nF was used for all the measurements, except for the Si devices 2–4, where a C_{ref} of 47 nF was used.

Figure 4.24 plots experimental QV curves of the selected devices for V_p = 400 V and f = 100 kHz. The resulting E_{diss} is calculated by taking the area (shaded in orange in each subfigure) between the charging (solid red line) and discharging (solid blue line) paths. As the peak output voltage of the high-voltage amplifier was limited to ± 150 V (this limits V_p to 300 V), a high-frequency transformer was utilized at the output of the amplifier to boost the voltage, so that V_p = 400 V was achievable. A C_{ref} of 1 nF was employed for all the devices, except for the Si devices 2–4, where a C_{ref} of 47 nF was used. This is because the large Q_o values (≥ 250 nC) of these three devices cause too large a variation in v_{ref} for C_{ref} = 1 nF, and hence a drop in the available v_{DS} swing.

4.3.2 Hysteresis Losses Observed with the Sawyer–Tower Circuit

Figure 4.24 also indicates that the DUTs exhibit diverse QV patterns, even within the same semiconductor types. In the Si family, the planar/conventional Si structure shows negligible hysteresis while the super-junction (SJ) counterparts exhibit significant hysteresis with E_{diss} values greater than 1 μJ. The SJ devices show a distinct knee-type behaviour in their discharging paths (indicated by a green

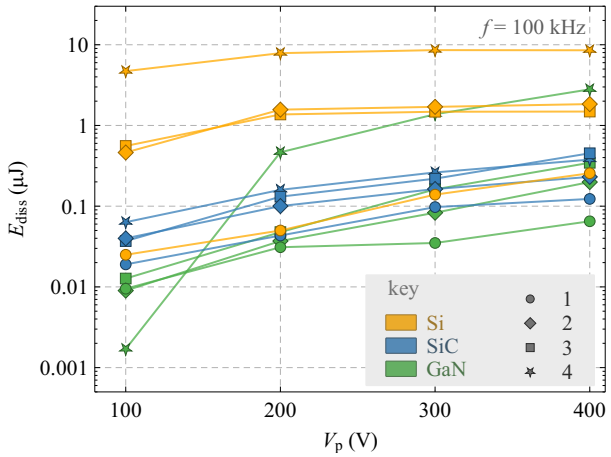


Figure 4.25: Variation of E_{diss} with different V_{p} values for the twelve tested devices. V_{p} is varied between 100 and 400 V at 100 V steps. The results are obtained with the Sawyer–Tower circuit at 100 kHz.

circle), about which the region corresponding to E_{diss} is much larger; the respective charging paths show much smoother transitions. The hysteretic area ceases around 200 V, beyond which the two paths coincide. SJ devices show much larger Q_{o} values (≥ 250 nC), while other devices—with comparable or lower values of ON-state resistance, $R_{\text{DS(on)}}$—show much lower Q_{o} values (≤ 100 nC) at 400 V.

The WBG devices SiC-1 and GaN-1 hardly show any hysteresis. The barely visible area between the charge–discharge curves of these two devices and the devices Si-1 and SiC-3, is symmetrically distributed within the whole v_{DS} range (i.e., the widening in the hysteretic area is symmetrical about $\approx V_{\text{p}}/2$). An interesting observation is that the patterns of the cascode structures of the WBG devices (SiC-4 and GaN-4) deviate from their non-cascode counterparts, showing the knee-type behaviour characteristic to SJ structures. Furthermore, the cascode GaN device shows significant hysteresis compared to other GaN devices.

These observations are only indicative of the soft-switching performance of these devices at $V_{\text{p}} =$ 400 V and $f = 100$ kHz. A complete understanding requires investigation into their behaviour at different V_{p} and f values, which is the subject of the next two subsections.

4.3.3 Voltage Dependence of *QV* Patterns

The dependence of *QV* patterns on voltage amplitude is investigated in this section. The aim is to identify if the hysteresis patterns emerge only within a certain voltage range, and if so, how they compare with different devices and semiconductor technologies. First, to provide a general view of the selected devices, Figure 4.25 compares the variation E_{diss} with V_{p} for all the devices. Then, to explain the dependence of E_{diss} on V_{p}, the *QV* patterns of each device is individually presented in Figures 4.26, 4.27 and 4.28, for Si, SiC and GaN devices, respectively. The excitation frequency is kept fixed at 100 kHz.

A clear observation in Figure 4.25 is that the Si-SJ devices show a saturation of their E_{diss} values as V_{p} passes 200 V. This can be explained by observing Figures 4.26(b), 4.26(c), and 4.26(d). The hysteresis patterns exist even at 100 V and continue to grow up to 200 V. However, after 200 V, the charging and discharging paths coincide resulting in no hysteretic area. This suggests that the Si-SJ hysteresis is

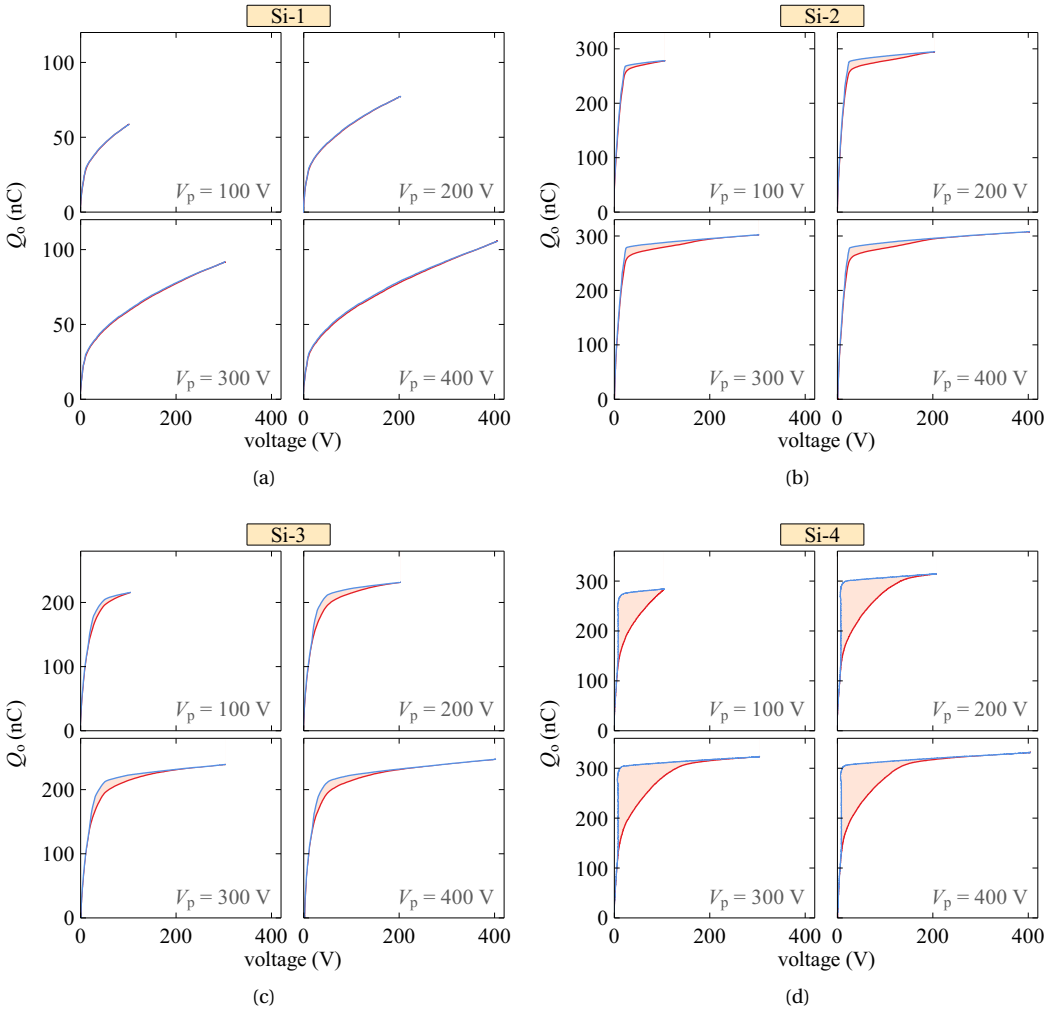


Figure 4.26: Experimental results showing how the *QV* hysteresis patterns vary with V_p (100, 200, 300 and 400 V) for the tested Si devices. Device 1 is a planar (conventional) Si device, while the others are super-junction Si devices. The excitation frequency was set at 100 kHz.

a low-voltage phenomenon, and that operation beyond a certain voltage, for example, 200 V in the studied cases, does not result in additional hysteresis energy losses. This could also be related to their significantly large C_o values (usually 10–100 nF) in the low v_{DS} range, which can be up to three orders-of-magnitude larger compared to the values at 400 V.

The devices Si-1, SiC-1 and GaN-1, as expected from their 400-V results, exhibit no appreciable hysteresis even at low voltages—see Figure 4.26(a), 4.27(a) and 4.28(a). Only a barely-visible and symmetrically-spread hysteresis is present. However, Figure 4.25 indicates that these devices show, although lower in value, an increasing E_{diss} with V_p. A possible reason for this is discussed in Section 4.5.

The importance of the graphical observation of hysteresis patterns becomes apparent by looking into the GaN devices 1 to 3, which are from three different manufacturers. According to Figure 4.25, the three devices (marked by circle, diamond and square symbols in green) show similar increasing

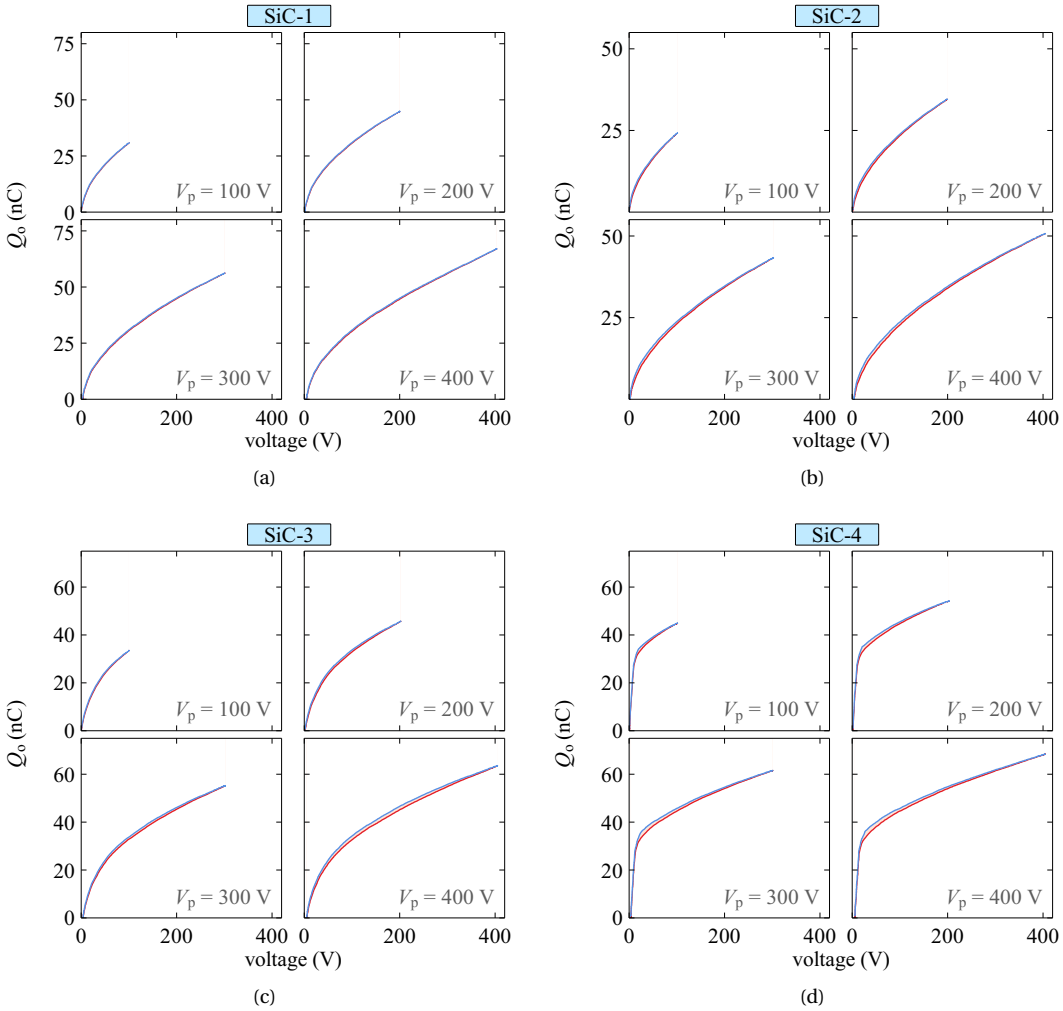


Figure 4.27: Experimental results showing how the *QV* hysteresis patterns vary with V_p (100, 200, 300 and 400 V) for the tested SiC devices. The first three devices are standard SiC MOSFETS while device 4 has a cascode structure. The excitation frequency was set at 100 kHz.

trends in their E_{diss} values with V_p. However, a major anomaly is observed in devices GaN-2 and GaN-3 when their *QV* patterns are looked into—see Figure 4.28(b) and 4.28(c). The hysteresis area of the two devices widens in the high v_{DS} range (above 200 V), unlike in device GaN-1, which shows no such swelling. The hysteresis appears only for cases with $V_p \gtrsim 100$ V, and the hysteresis pattern widens with increasing V_p. On the other hand, there is no visible hysteresis present at voltages below 100 V for these two devices (V_p values of 20 and 50 V were also tested, and results showed no hysteresis); in this case, they act similar to device GaN-1, but in stark contrast to SJ devices, which clearly show a low-voltage hysteresis. This suggests that for these two GaN structures, C_o hysteresis is a phenomenon that occurs only in the high v_{DS} range. In addition, as Figure 4.25 shows, device GaN-3 exhibits much larger E_{diss} values compared to device GaN-2, which is also verified by the relatively larger hysteresis patterns of the former.

The superimposition of *QV* patterns corresponding to different V_p values on the same plot yields additional details between technology-specific differences in hysteresis losses. Figure 4.29(a) shows

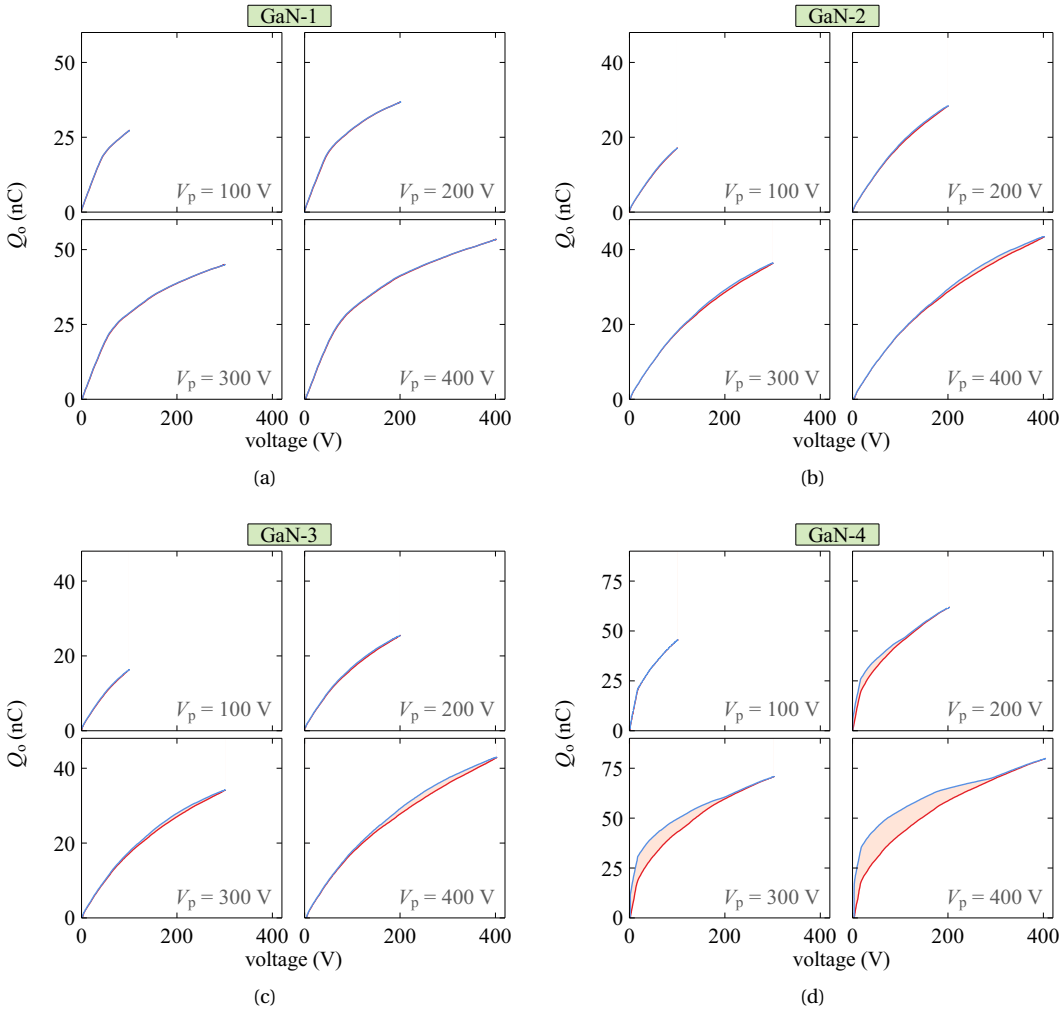


Figure 4.28: Experimental results showing how the *QV* hysteresis patterns vary with V_p (100, 200, 300 and 400 V) for the tested GaN devices. The devices1–3 are e-mode devices, whereas device 4 is a cascode device. The excitation frequency was set at 100 kHz.

that for device Si-3, the charge paths coincide for 100- and 400-V cases. However, for the cascode GaN device, as Figure 4.29(b) shows, neither the charging nor the discharging paths show any coincidence for the considered voltages (100, 200 and 400 V), suggesting a non-uniform dependence of the *QV* patterns with V_p. The device also shows a large increase of its E_{diss} value from 100 V to 200 V in Figure 4.25. This is explained by its *QV* hysteresis patterns that appear to take place only if V_p is above 100 V, as Figure 4.28(d) indicates. Even above 200 V, the shapes of the hysteresis areas are quite different to other GaN devices. The shapes are more similar to that of Si-SJ devices.

4.3.4 Frequency Dependence of Hysteresis Loss and *QV* Patterns

In this section, the frequency dependence of E_{diss} is investigated, while keeping the excitation voltage fixed. Figure 4.30 plots experimental results for different device structures up to 1 MHz. None of the devices exhibits significant dependence on frequency in the considered range. This becomes also

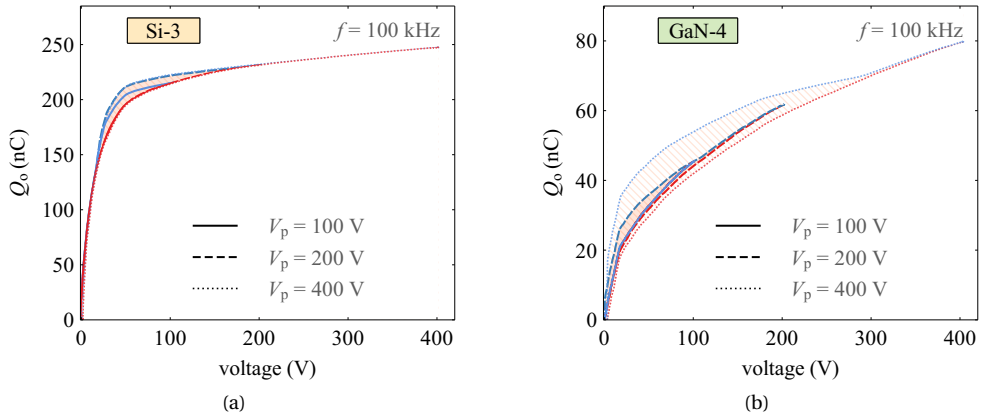


Figure 4.29: Superimposition of *QV* hysteresis patterns of the devices (a) Si-3 and (b) GaN-4. The hysteresis pattern of device Si-3 at 400 V is a clear extension of the pattern at 100 V, with coincidental charging paths at each voltage. Device GaN-4 shows no hysteresis at 100 V; at 200 and 400 V, it shows hysteresis, but unlike device Si-3, the charging paths for each case of peak voltage are non-coincidental.

apparent by looking at the hysteresis patterns of the devices. Figure 4.31(a) shows that the *QV* patterns are almost identical for the SJ device Si-2 when excited at three different frequencies (50, 100 and 200 kHz), explaining the non-existence of any significant frequency dependence; the same can be observed for device Si-4 in Figure 4.31(b), although with a slight increase in the hysteresis area at 200 kHz, and hence the value of E_{diss}, which can be also noticed in Figure 4.30.

Frequency independence can also be seen in the *QV* patterns of the WBG devices SiC-3, GaN-1 and Gan-4, up to 1 MHz—see Figures 4.31(c)–4.31(e), which are in accordance with the results from Figure 4.30. It should be noted here that some works in the literature indicate a frequency dependence for E_{diss} in certain WBG families; however, these effects become prominent only above 5-10 MHz. This aspect is discussed in Section 4.6.1.

The impact of hysteresis energy loss is extremely important at high operating frequencies, as the

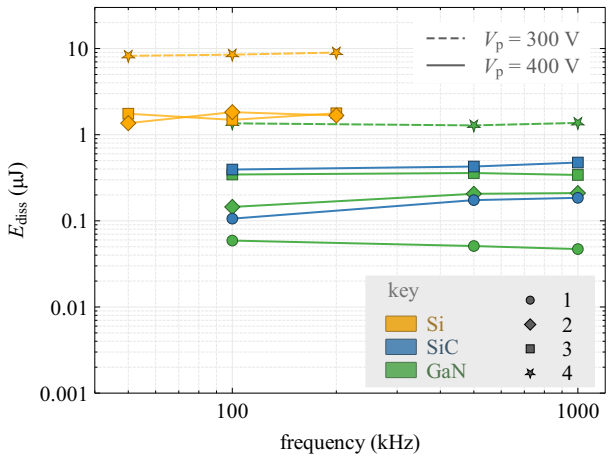


Figure 4.30: Variation of E_{diss} versus f for selected devices. The results are obtained using the Sawyer–Tower circuit with a variable frequency sinusoidal excitation signal. As the Si devices have a large output capacitance value at the low v_{DS} range, they could only be tested up to 200 kHz due to increased distortion of v_{IN} (see Section 4.2.4 for the underlying reasons).

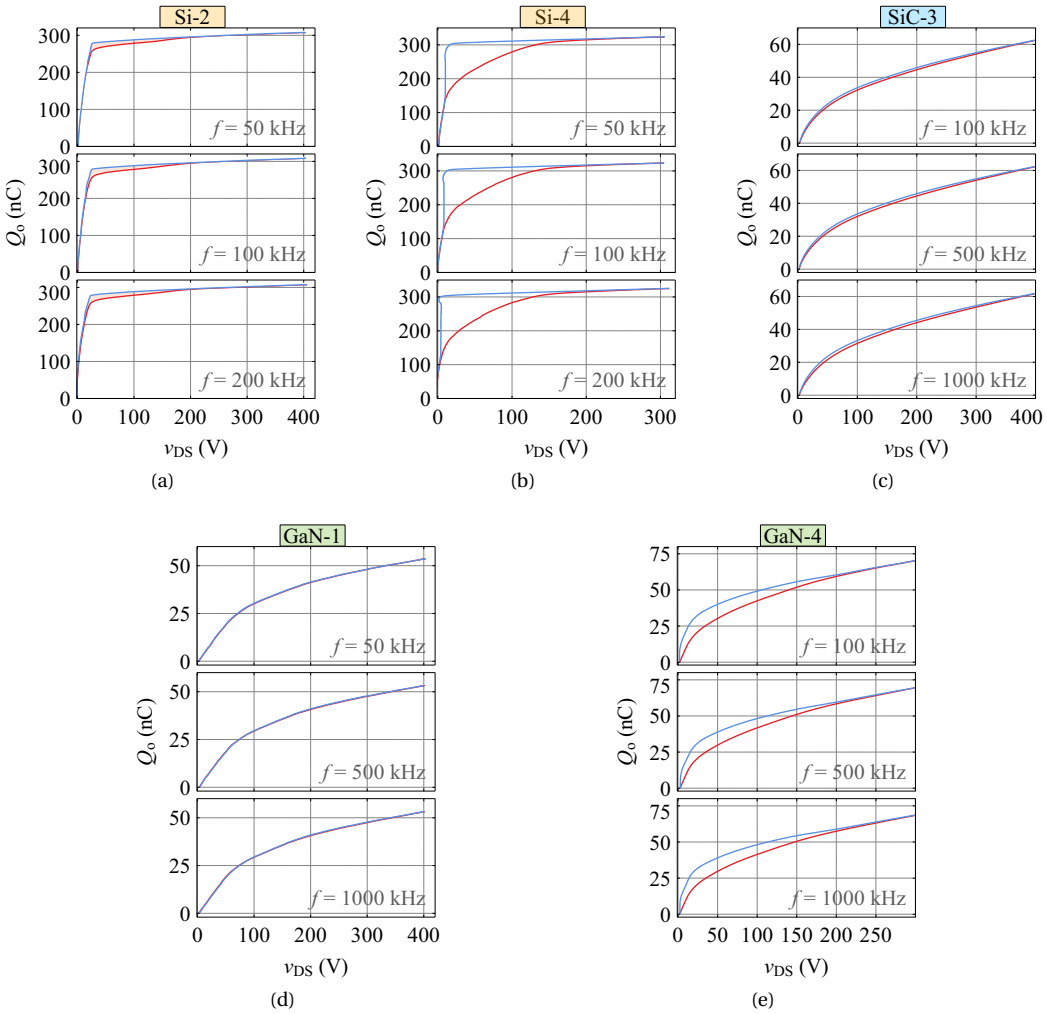


Figure 4.31: Experimental QV patterns for different f values. The considered devices, in general, maintain a QV pattern that is independent of the considered frequency range.

resulting power loss, P_{diss}, scales with f:

$$P_{\text{diss}} = f \cdot E_{\text{diss}}. \tag{4.21}$$

For a given P_{diss} value, the maximum operating frequency of a certain device is limited by its E_{diss} value. For instance, at 400 V and 1 MHz, device GaN-4 would result in a power loss greater than 1 W, while device GaN-1 would cause a loss much less than 0.1 W. If a device has a frequency-dependent hysteresis loss, the details of its E_{diss} as a function of f is required up to the test frequency to estimate P_{diss}. For such cases, Eq. (4.21) can be modified to show the frequency dependence of E_{diss} as

$$P_{\text{diss}} = f \cdot E_{\text{diss}}(f). \tag{4.22}$$

Therefore, if a device has an increasing E_{diss} with f, then it greatly reduces the device's usability, especially at VHF frequencies. However, for the considered devices and up to 1 MHz, as Figure 4.30 suggests, Eq. (4.21) can be utilized to obtain a good estimate of P_{diss} by using an E_{diss} value measured

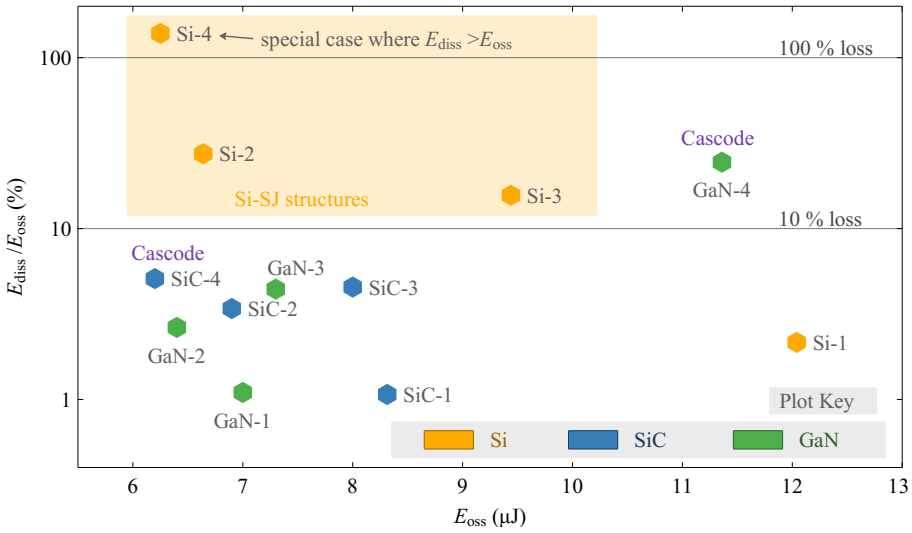


Figure 4.32: E_{diss} values of the devices listed in Table 4.3 plotted as a percentage loss of their E_{oss} values. The E_{diss} values are evaluated at 400 V and 100 kHz, while the E_{oss} values are calculated using datasheet-provided C_{oss} curves for 400 V.

at a much lower frequency, such as 100 kHz. A practical demonstration of this is presented in chapter 7 for device GaN-4.

4.3.5 Hysteresis Losses versus Hard-Switching Losses

As an important remark on the large-signal hysteresis losses of C_o, here, some perspective into the levels of energy that correspond to hard-switching and soft-switching loss mechanisms is given.[10]

Figure 4.32 plots E_{diss} values (at 100 kHz) normalized by the corresponding small-signal E_{oss},[11] for all the devices tested listed in Table 4.3. As can be observed, E_{diss} values are generally small (< 10%) in comparison with the respective E_{oss} values. However, the Si-SJ structures and the GaN cascode show more than 10% of normalized losses. The SJ device Si-4 shows an anomaly giving an E_{diss} value greater than its E_{oss} value. The devices GaN-1 and SiC-1 offer the lowest normalized loss for E_{oss} values up to 9 μJ, suggesting the best soft-switching performance up to 1-5 MHz. Beyond this frequency range, the frequency dependence of E_{diss} should be taken into account.

4.3.6 Family Comparison

So far in Section 4.3, we have investigated twelve different power FETs with a current rating of around 30 A, which belonged to twelve different manufacturers (see Table 4.3). This allowed us to identify differences in the C_o-hysteresis losses and *QV* patterns between the respective semiconductor technologies. This subsection focuses on a single power FET *family* (or *series*) of a given manufacturer and examines how *QV* patterns behave for different devices in each family.

We will limit our focus to 500–700 V devices. We consider three families each from Si, SiC and GaN semiconductor technologies. Each family corresponds to a fixed voltage rating and has devices with

[10] Hard-switching losses are discussed in chapter 5.

[11] In device datasheets, output-capacitance-related parameters are given as small-signal quantities: capacitance, C_{oss}; charge, Q_{oss}; and stored energy, E_{oss}. For more details see Section 2.2.2.

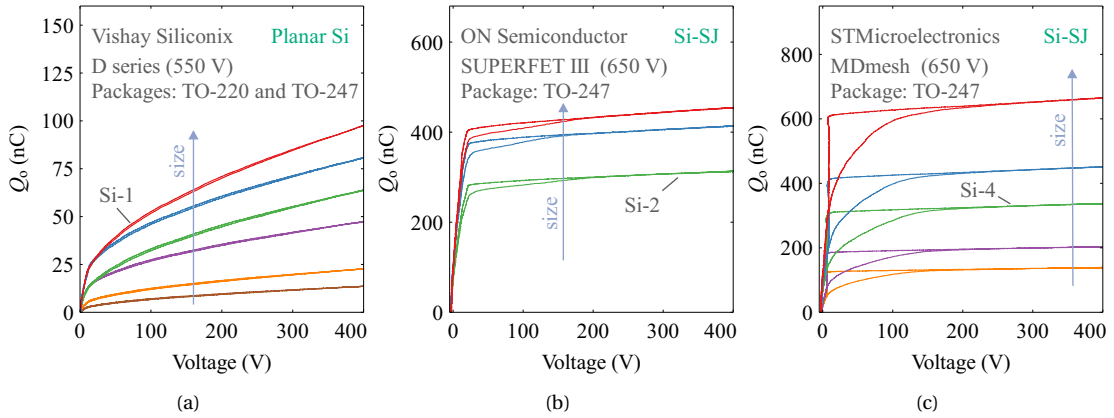


Figure 4.33: Variation of *QV* patterns within a particular Si-device-family of a given rated voltage. Within a family, the size of a device is scaled up as the current rating is increased. Three families/manufacturers are considered: (a) planar D-series Si family from *Vishay Siliconix*; (b) superfet III Si-SJ family from *ON Semiconductor*, with the series ID NTHL; (c) MDmesh Si-SJ family from *STMicroelectronics*, with the series ID STW. Sawyer–Tower circuit at an excitation frequency of 100 kHz was used for the measurements. A C_{ref} value of 1 nF was used for the planar-Si family, whereas the value of C_{ref} was set at 10 nF for the two Si-SJ families.

different current ratings: a higher current rating means a higher die size,[12] and hence, a large device capacitance. We have utilized the Sawyer–Tower circuit at 100 kHz for these measurements and set $V_{\text{DS-max}}$ to 400 V.

Figure 4.33 plots the results for the three selected Si families: for all three families, the value of Q_o at 400 V increases with the size of the device as expected by the increased device capacitance. For the planar series, as was with device Si-1 in Figure 4.24 [also marked here in Figure 4.33(a)], there is no appreciable hysteresis for all the devices. Although the SUPERFET III series shows hysteresis [device Si-2 from Figure 4.33(a) is also marked in Figure 4.33(b)], there is no significant variation of the hysteresis-loop areas among the devices. MDmesh series, on the other hand, does show appreciable increments in the loop areas as the device size becomes larger.

In Figure 4.34, three SiC families are considered. The MSC series does not exhibit hysteresis at the considered frequency of 100 kHz. The SCT and UF3C series show hysteresis, and moderate levels of increments can be observed in the hysteresis-loop area as the device size increases. For the series UF3C, which is a cascode SiC structure, it can also be noted that the hysteresis pattern concentrates on the knee-point of the *QV* curves of all the devices, as was observed with Si-SJ structures.

Finally, the results for the GaN families are presented in Figure 4.35. No appreciable hysteresis can be observed for all the devices in the GS665 series, which could be foreseen from the results for device GaN-1 in Sections 4.3.2 and 4.3.3 [(device GaN-1 from Figure 4.24 is also marked here in Figure 4.35(a) for comparison)]. A significant difference in the hysteresis area can be observed for the two devices in the X-GaN series: the smaller device has a current rating of 15 A ($R_{\text{DS(on)}}$ = 140 mΩ), while the larger, which is device GaN-3 from Table 4.3, is rated for 31 A ($R_{\text{DS(on)}}$ = 56 mΩ). All the devices in the TPH series exhibit hysteresis, with considerable increments in the hysteresis area, as was observed for the MDmesh Si-SJ series.

[12] For the considered Si and SiC families, the package size is generally fixed at TO-247 (or TO-247), for all the current ratings. In contrast, this is not the case for some GaN families, for example, GaN systems and EPC: the package size changes with device size as there is no external packaging involved like in Si devices. However, since the years 2020 and 2021, it can be observed that GaN manufacturers also try to incorporate standard package sizes.

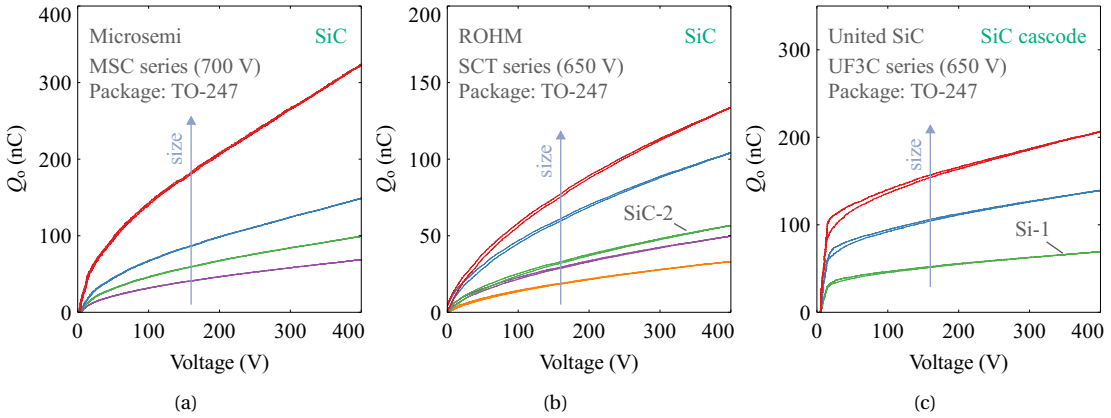


Figure 4.34: Variation of *QV* patterns within a particular SiC-device-family of a given rated voltage. Three families/manufacturers are considered: (a) SiC family from *Microsemi*, with the series ID 'MSC'; (b) SiC family from *ROHM*, with the series ID 'SCT'; (c) cascode SiC-family from *UnitedSiC*, with the series ID 'UF3C'. Sawyer–Tower circuit at an excitation frequency of 100 kHz was used for the measurements. A C_{ref} value of 1 nF was used for all three families.

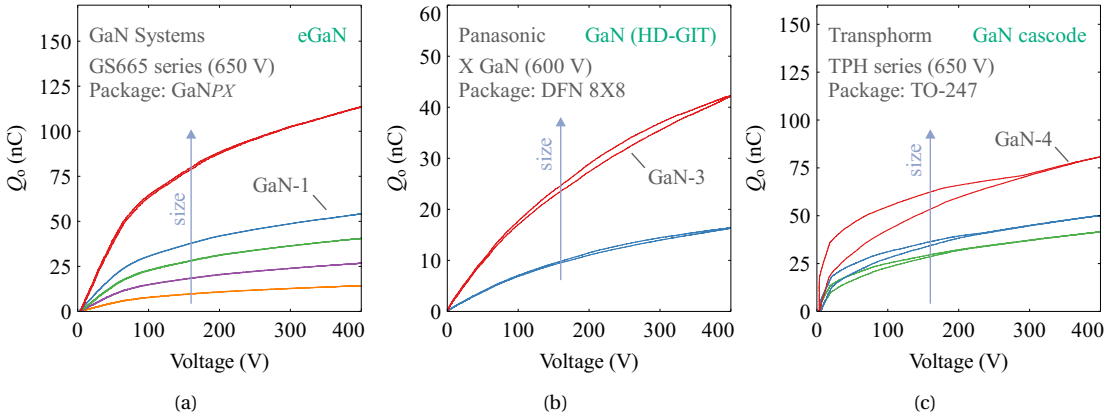


Figure 4.35: Variation of *QV* patterns within a particular GaN-device-family of a given rated voltage. Three families/manufacturers are considered: (a) an e-mode GaN family from *GaN Systems*, with the series ID GS665; (b) the e-mode GaN family from *Panasonic*, with the series ID PGA; (c) a cascode GaN-family from *Transphorm*, with the series ID TPH. The excitation frequency was set at 100 kHz. Sawyer–Tower circuit at an excitation frequency of 100 kHz was used for the measurements. A C_{ref} value of 1 nF was used for all three families.

In all the device families considered here, we can find the following common observations for devices in each series:

- For device families that do not show hysteresis, their *QV* patterns (in terms of appearance) show a simple scale up as the device size increases.

- If a device in a selected family exhibits hysteresis, then all the devices in the family exhibit hysteresis. This is expected, as all the devices in a family, in general, have the same basic structure. And the root cause for hysteresis will exist in all the devices in that family. However, as the device scales up, the hysteresis loop may or may not scale up in a simple linear fashion [see the difference in Figures 4.33(b) and 4.33(c)].

4.4 Possibilities of Small-Signal Measurements

In our discussions so far, we have highlighted the limitations of small-signal measurements of output capacitance. It should also be noted that the measurements specifically referred to the capacitance value obtained using impedance measurements (see Section 2.2 and Section 4.1.1), based on the imaginary part of the complex impedance. However, these impedance measurements also provide a real part that is representative of a resistive loss, which has not been widely discussed so far. In this section, we look specifically into this resistive component, R_o, its measurement, and its capabilities to provide qualitative estimates of C_o-related large-signal energy losses. We start by looking into its origins.

4.4.1 Background

In 2014, when Fedison et al. reported output-capacitance-related energy losses in ZVS circuits based on Si MOSFETS [13], one of the main messages conveyed was the requirement of a better model for C_o that could capture the observed losses. The following is a direct extract from the abstract of the related publication [13]:

> *It is shown that a simple model using C_{oss} in series with a resistance R_{oss} is inadequate for describing the observed energy loss and a different model is needed.*

At this point, it should be emphasized that the small-signal series resistance (denoted as R_{oss}) is not a parameter that is given on device datasheets[13] of power FETs or Application Notes by manufacturers. Furthermore, it is not widely discussed in the technical literature related to the C_o of power devices. Therefore, a natural curiosity arises as to the origin of the concept of R_{oss} in power FETs as well as its implications and limitations in predicting C_o-related energy losses. This serves as the main motivation for the content in this section.

Although Fedison et al. mention R_{oss} in the said publication [13], no additional information on R_{oss} is given in the main content of the article. With some extensive literature survey, we were able to trace back the origins of the measurement of R_{oss} to a few research works by an MIT group (headed by Prof. David Perreault) between 2007 and 2009. In 2007, the master's thesis of Robert Pilawa-Podgurski presents measurement results of R_{oss} for 65–70 V LDMOS devices used for a resonant boost converter [61]: the measurements were given for a frequency of 110 MHz using an Agilent 4395A impedance analyser. The reported values ranged from 0.1 to 1.3 Ω. Some other works by the group also present additional measurements of R_{oss} [62–64]. The concepts are summarized in the 2009 publication by the same group, which highlights a *displacement loss* created by R_{oss} as an important loss mechanism in VHF devices [63]. The device model presented in the said work is shown in Figure 4.36.

Before this thesis work, a few pieces of subsequent literature [21, 65] have also mentioned R_{oss}, but with very limited information on the implications on power devices and any related prior references. The 2018 application note by ST Microelectronics, identifies R_{oss} as an EMI suppression mechanism: a measured R_{oss} versus V_{DS} plot for two 100-V devices were also given, but no additional details were provided regarding the measurements. Furthermore, related to EMI suppression, a 2011 journal article by Bhargava treats the role of R_{oss} as a loss mechanism that attenuates ringing in dc-dc synchronous

[13] This is the case for power FETs. In all of the devices (100–900 V devices) that we have used in our studies, we have not come across any reference to this parameter. However, we have come across this parameter in the datasheets of certain RF power FETs (e.g., device NTE221 [60]).

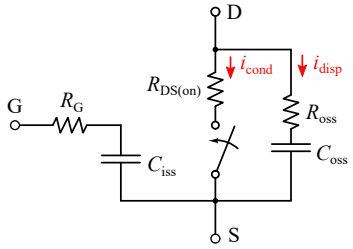


Figure 4.36: Device model that was presented in the work by Perreault et al. [63]. The authors highlight a *Displacement Loss* caused by the output-capacitance branch that consists of the capacitance C_{oss} and resistance R_{oss}.

buck converters [66]. The work also refers to prior works, one by the above-mentioned MIT group [62], and another by Kam et al. [67]. The 2011 work by Kam et al. also discusses the implication of R_{oss} in minimizing ringing in switching power supplies and claims to provide a novel method to quantify attenuation losses by measuring R_{oss} through impedance and voltage measurements.[14]

These works have mainly focused on certain aspects of R_{oss} for VHF (30–300 MHz) applications. In addition, the measurement methods were not discussed in detail. And more importantly, any implications of R_{oss} for power FETs used in medium-frequency (MF: 300 kHz to 3 MHz) or high-frequency (HF: 3 MHz to 30 MHz) applications were not discussed. Furthermore, the studies were mostly centred on devices that were rated for below 100-V operation.

One recent work in 2020 used small-signal measurements to quantify C_o-hysteresis losses of WBG devices [68]. A model of the C_o branch was represented as follows: a nonlinear (voltage-dependent) effective small-signal capacitance, denoted as $C_{oss}^{eff} = \sqrt{\frac{1}{V_p}\int_0^{V_p} C_{oss}^2\, d\,v_{DS}}$ that encompasses the total variation of C_{oss} for a given peak voltage V_p; R_o was referred to as R_s,[15] whose value is frequency-dependent. Note that C_{oss}^{eff} is simply the RMS definition $C_{oss(RMS)}$ of C_{oss} as was explained in Section 2.4. The energy dissipated in resonantly charging/discharging the C_{oss} branch, in a full cycle, was attributed to R_s. Subsequently, we have carried out additional experiments and discovered that R_s is not fully capable of accurately *quantifying* the hysteresis losses for some of the tested devices.[16] One reason for this, we believe, is the following. Due to the limitations of the measurement equipment, the value of R_s was measured up to a maximum bias voltage of 40 V. And it was assumed in the aforementioned work that R_s stays constant beyond 40 V based on its flat nature between 20–40 V. Any observation of the behaviour of R_s at higher voltages, for example at 400 V, requires complicated biasing techniques with high accuracy. The existing measurement tools available to us were incapable of performing such measurements.[17]

Nevertheless, as we will demonstrate, R_o values—measured at relatively lower bias voltages (up to 100 V, for example)—could still provide valuable *qualitative* information on the expected hysteresis losses in certain types of WBG devices. This is especially useful when information on the large-signal behaviour of a WBG device is not available. With this motivation, here, we report important findings on R_o for commercially available normally-OFF device families and investigate its implications in a broader sense to provide a qualitative prediction on high-frequency soft-switching losses.

[14] A transmission line structure with a vector network analyser was utilized.
[15] The subscript 's' stands for 'series'.
[16] The E_{diss} values calculated with the Sawyer–Tower results and predicted with R_s differed.
[17] Additional details on this are discussed in Section 4.4.2.

4.4.2 Measurements on the Output-Capacitance Branch

Keeping with our convention used in denoting output capacitance as C_o, we will denote the resistive component in series with C_o as R_o. Since our measurements here concern small-signal excitations, we denote the measured value of R_o as R_{oss}, going with the convention used by some of the prior works mentioned above.

In all the experimental impedance measurements presented here, a Keysight E4990A impedance analyser with a 16047E test fixture (50 MHz) was used. Using this unit as a reference, Figure 4.37 gives a graphical representation of an impedance measurement process related to a standard high-frequency impedance analyser. The excitation signal is a sinusoidal voltage with a magnitude V_m and a frequency $\omega = 2\pi f$. It is important to note that the excitation voltage magnitude is typically set in the equipment as an RMS value (i.e., not as a peak value).[18] The impedance measured at ω is given as

$$Z = R + \mathrm{j}X \tag{4.23}$$

where R and X are the resistive and reactive components, respectively. The equivalent circuit for a capacitor is also shown in Figure 4.37 [69]. The real and imaginary parts related to the impedance of this equivalent circuit,[19] are calculated as follows:

$$R = R_l + \frac{R_p}{1+\omega^2 R_p^2 C^2} \tag{4.24}$$

$$X = \mathrm{j}\,\frac{\omega L - \omega R_p^2 C + \omega^3 R_p^2 L C^2}{1+\omega^2 R_p^2 C^2} \tag{4.25}$$

In a standard impedance analyser, we can directly record the measured impedance value in either polar form or Cartesian form as given by Equations 4.24 and 4.25. However, for most cases, we could utilize built-in simplified modes, depending on the nature of the DUT. For instance, we could use the 'C_sR_s *mode*',[20] if our DUT can be represented as a simple resistance and capacitance in series, which is indeed our requirement here. Then, in reality, when the impedance analyser displays C_s and R_s, they encompass all other parasitics in the equivalent circuit as follows:

$$R_s = R_l + \frac{R_p}{1+\omega^2 R_p^2 C^2} \tag{4.26}$$

$$C_s = \frac{C + \dfrac{1}{\omega^2 C R_p^2}}{1 - \dfrac{L}{C R_p^2} - \omega L C} \tag{4.27}$$

Below, we provide some important practical considerations based on the reference *Impedance Measurement Handbook* by Keysight Technologies. Certain simplifications for Equations 4.26 and 4.26 can be found as follows.

- For sufficiently large R_p (i.e., $R_p \gg 1/\omega C$), we get $R_s \approx R_l$.

[18] For example, if the excitation voltage is set to be 100 mV, it is the RMS value corresponding to a perfect sinusoid. Then, $V_m = 100 \cdot \sqrt{2}$ mV.

[19] Between points A and B.

[20] The subscript 's' refers to series.

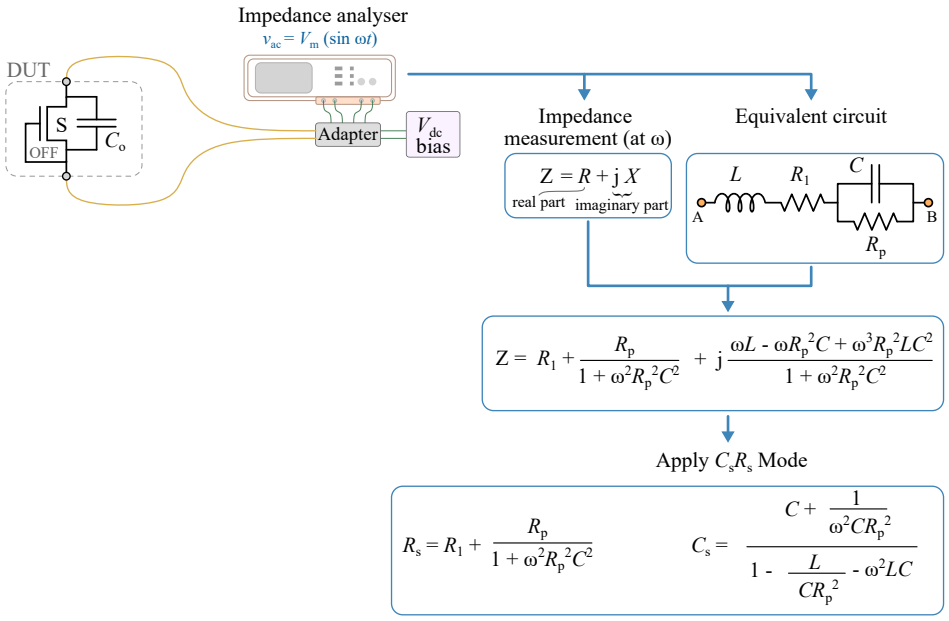


Figure 4.37: The process of getting C_s and R_s values from impedance measurements using an impedance analyser. Here, we consider a Keysight E4990A unit. The details are based on the material presented in the document *Impedance Measurement Handbook* by Keysight Technologies. [69].

- For sufficiently large R_p (i.e., $R_p \gg 1/\omega C$) and small L (i.e., $\omega L \ll 1/\omega C$), we get $C_s \approx C$.
  - For large capacitance values, $R_p \gg 1/\omega C$ is satisfied due to large C.
  - For small capacitances, R_p practically has a very large value; and again, the condition $R_p \gg 1/\omega C$ will be satisfied.
  - This means that, in general, a capacitor model can be simplified into a series connection of a resistor, a capacitor, and an inductor.[21]

Furthermore, to measure C up to several tens of megahertz, the test leads should be as short as possible. In our experiments, we placed the DUTs directly across the 16047E test fixture, with the leads (or the soldered wires) from the drain–source terminals clipped to a minimum length. With these measurement considerations taken into account, we performed impedance measurements on our DUTs, whose model is shown in Figure 4.38(a). Then, R_{oss} is simply calculated as

$$R_{oss} = R_s. \tag{4.28}$$

We focus on excitation frequencies in the range of 100 kHz to 50 MHz. As was mentioned previously, the dc bias voltage in our system was limited to 40 V.

It should also be noted that the output capacitance model in Figure 4.38(a) can be applied for any type of excitation on the device's drain-source voltage, v_{DS}. However, the calculated E_{diss} value depends on the type and magnitude of the excitation signal. Figure 4.38(b) shows the dependence of R_{oss} with the frequency of excitation, f, for two WBG devices. Figure 4.39(a) and Figure 4.39(b) highlight the nonlinear variation of C_{oss} and $C_{oss(RMS)}$ with v_{DS} for the same two devices. For the considered devices, we can also observe that R_{oss} is not a strong function of voltage (up to 40 V).

[21] The value of ω at which the requirement $R_p \gg 1/\omega C$ is no longer satisfied can be identified by observing the resonant point in the impedance versus frequency or capacitance versus frequency curve.

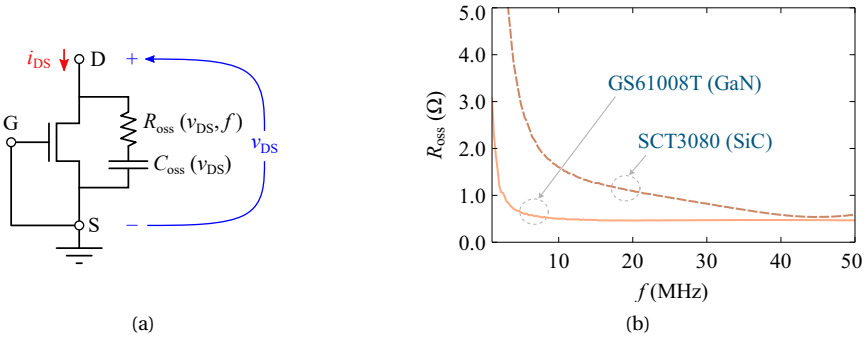


Figure 4.38: (a) The output capacitance of a FET modelled as a branch consisting of the series combination of a capacitance C_{oss} and a resistance R_{oss}, which are evaluated with small-signal measurements. We consider that C_{oss} depends only on v_{DS} and that R_{oss} depends on both v_{DS} and excitation frequency, f. (b) Variation of R_{oss} with excitation frequency for a 100-V GaN device and a 650-V SiC device. A Keysight E4990A impedance analyser with a 16047E test fixture (50 MHz) was used with an excitation voltage of 100 mV. The gate and source terminals of the transistors were shorted (i.e., $v_{GS} = 0$ V).

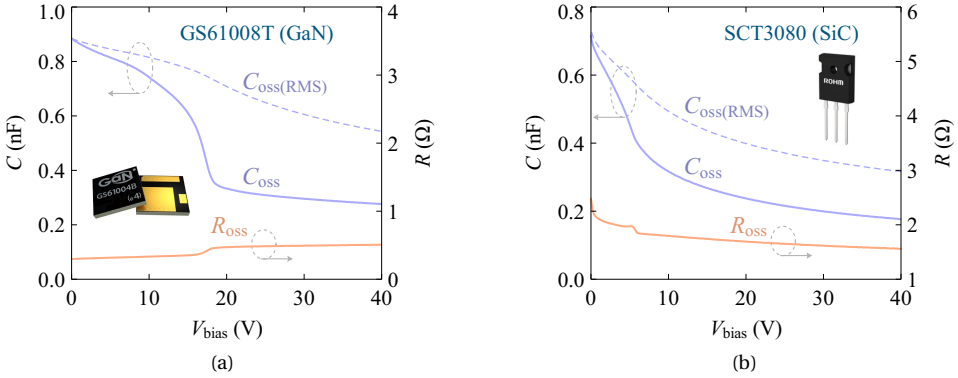


Figure 4.39: Variation of C_{oss}, $C_{oss(RMS)}$ and R_{oss} with bias voltage for the same devices considered in Figure 4.38(b). An excitation voltage of 100 mV at a frequency of 10 MHz was used.

4.4.3 Results for Commercial Power FETs

Our first endeavour was to study the behaviour of R_{oss} in commercially available state-of-the-art power FETs. More specifically, the devices rated at 500–700 V, which are generally used for 400-V applications. Figure 4.40 plots R_{oss} *vs* device on-resistance, $R_{DS(on)}$, for five device families (A to E). The details of these families are tabulated in Table 4.4. The R_{oss} values were measured at a bias voltage of 40 V and an excitation frequency of 10 MHz. All families generally show a linear relationship between R_{oss} and $R_{DS(on)}$. SiC families show a higher $R_{oss}/R_{DS(on)}$ ratio (> 10), while Si family A shows the lowest ratio (≈ 1). These results suggest that R_{oss} is fundamentally related to the sizing of a device in a linear manner, which can be represented as

$$R_{oss} \propto R_{DS(on)} \propto 1/I_{D(rated)}, \tag{4.29}$$

where $I_{D(rated)}$ is the current rating of the device.

To further investigate the implications, we consider what is known as the *sizing* of a device family. This is commonly referred to as the *scaling-up of a device* in device-engineer terminology. Scaling-up decreases the on-resistance, or equivalently increases the current rating, $I_{D(rated)}$, by increasing the physical *width* of a device. This can be modelled as a distribution of unit cells as depicted in Figure

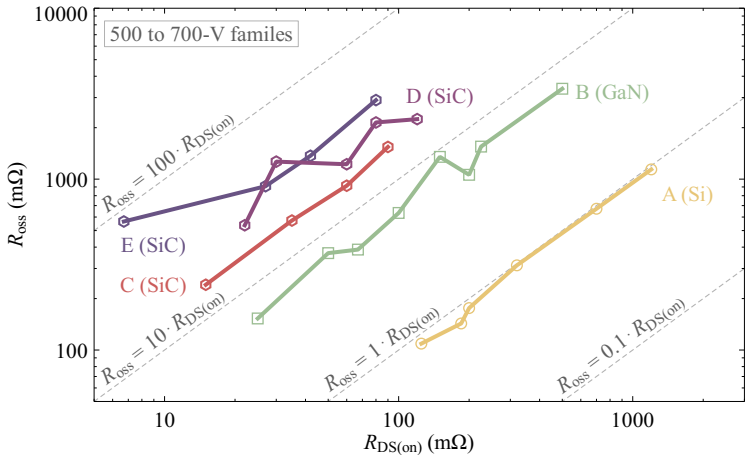


Figure 4.40: Variation of R_{oss} (at $v_{DS} = 40$ V and $v_{GS} = 0$ V) with $R_{DS(on)}$ for 500-700 V normally-off device families. The excitation signal has $f = 10$ MHz and a peak of 100 mV.

Table 4.4: Selected Device Families

Family	Voltage	Technology	Manufacturer
A	500	Si (planar/conventional)	Vishay
B	650	GaN	Gan Systems
C	700	SiC	Microsemi
D	650	SiC	ROHM
E	650	SiC (Cascode)	United SiC

4.41. Each cell has a current rating of I_{D0} and an output capacitance with the parameters $R_{oss\text{-}0}$ and capacitance $C_{oss\text{-}0}$.[22]

A device sized with n number of cells has $I_{D(rated)} = n \cdot I_{D0}$, $C_{oss} = nC_{oss\text{-}0}$ and $R_{oss} = R_{oss\text{-}0}/n$. This entails that the product $C_{oss} \cdot R_{oss}$ is independent of the sizing of the device (illustrated in Figure 4.41).

$$C \cdot R_{oss} = C_{oss\text{-}0} \cdot R_{oss\text{-}0}. \tag{4.30}$$

It should also be noted that Eq. (4.30) can be rewritten considering $C_{oss(RMS)}$ as given by Eq. (4.31). As this product inherently represents a time constant related to device output capacitance, we denote it by the symbol the τ_0.

$$\tau_0 = C_{oss(RMS)\text{-}0} \cdot R_{oss\text{-}0} = C_{oss(RMS)} \cdot R_{oss}. \tag{4.31}$$

Using the result $R_{oss} \propto R_{DS(on)}$ and Equations 4.30 and 4.31, we get

$$R_{oss} \propto R_{DS(on)} \propto \frac{1}{C_{oss}} \propto \frac{1}{C_{oss(RMS)}} \propto \frac{1}{I_{D(rated)}}. \tag{4.32}$$

The product $C_{oss}R_{oss}$ (or equivalently $\tau_0 = C_{oss(RMS)}R_{oss}$) can be considered a unique feature of a device structure/family that is independent of its current rating.

[22] Note that $C_{oss\text{-}0}$ is a function of v_{DS} and that $R_{oss\text{-}0}$ is a function of both v_{DS} and f.

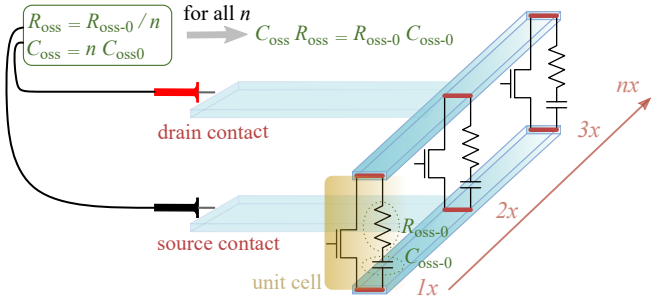


Figure 4.41: Sizing of a large device of a current rating $I_{D(rated)}$ can be imagined by a distribution of n unit cells, where each has a current rating of I_{D0}.

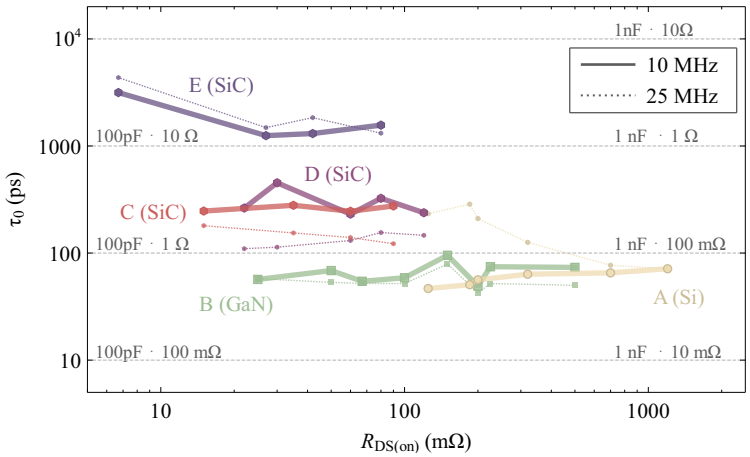


Figure 4.42: Variation of $\tau_0 = C_{oss(RMS)} \cdot R_{oss}$ (at v_{DS} = 40 V and v_{GS} = 0 V) with $R_{DS(on)}$ for the device families considered in Figure 4.40 and Table 4.4.

For the same devices families considered in Figure 4.40, we have plotted τ_0 versus $R_{DS(on)}$ in Figure 4.42 for two different frequencies: at 10 MHz (shown by solid lines) and at 25 MHz (shown by dotted lines). In general, it can be observed that all the families exhibit a τ_0 that is independent of $R_{DS(on)}$.[23] The observable offset in the direction of the y-axis when the frequency is changed from 10 to 25 MHz is due to the frequency dependence of R_{oss}. The GaN family shows the lowest values for τ_0 (below 100 ps), owing to the excellent properties of GaN semiconductor technology. The Si family perform similar to the GaN family at 10 MHz; however, it should be noted that the Si family does not offer $R_{DS(on)}$ values below 100 mΩ, while the GaN family does. SiC families C and D show similar levels of performance with τ_0 values between 300–400 ps at 10 MHz: the values decrease when going up to 25 MHz. For both excitation frequencies, the SiC family E shows τ_0 values above 1 ns.

Next, we investigate possible relationships between R_{oss} and large-signal hysteresis losses of C_o.

4.4.4 Implications of R_{oss} on Large-Signal Hysteresis Losses

Here, we consider the possibility of establishing a relationship between the small-signal parameter R_{oss} and the large-signal loss related C_o-hysteresis. We assume that the small-signal parameters are equally

[23] Although there are some changes as $R_{DS(on)}$ varies, there are no order-of-magnitude changes.

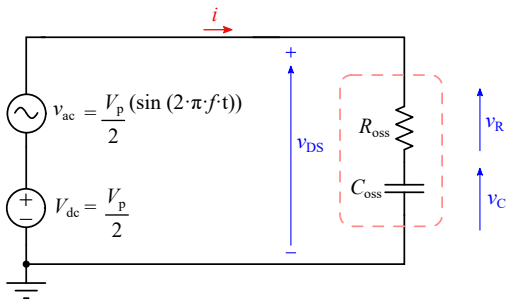


Figure 4.43: A simple *RC* circuit.

valid to represent the operation of the C_o-branch under both small- and large-signal excitations. We start with an analytical approach with the output-capacitance branch modelled as shown in Figure 4.43: the C_o-branch is excited with a large-signal voltage given by

$$v_{DS} = V_{dc} + v_{ac} \tag{4.33}$$

$$v_{DS} = \frac{V_p}{2}\left(1 + \sin(2\pi f t)\right). \tag{4.34}$$

Under steady-state conditions, only the ac excitation causes a loss in the circuit (there are no dc currents in the circuit). The energy dissipated in the C_o-branch during a single cycle, for a given f, can be written as

$$E_{diss} = \int_0^T v_{DS} \cdot i \, dt, \tag{4.35}$$

where $T = \frac{1}{f}$ is the excitation period. As this loss is caused by the resistive element R_{oss}, assuming R_{oss} to be a parameter independent of v_{DS}, we can also write

$$E_{diss} = \int_0^T i^2 \cdot R_{oss} \, dt. \tag{4.36}$$

The impedance of the C_{oss} branch can be written as a function of v_{DS}:

$$Z = R_{oss} + \frac{1}{j\omega C_{oss}(v_{DS})}. \tag{4.37}$$

Then, the magnitude of the impedance is calculated as

$$|Z| = \frac{1}{\omega C_{oss}(v_{DS})}\sqrt{1 + \omega^2 C_{oss}^2(v_{DS}) R_{oss}^2}. \tag{4.38}$$

Now, if we introduce an additional restriction to the operation, such that $\omega C_{oss} R_{oss} \ll 1$ for all C_{oss} values for v_{DS} values up to V_p, the impedance becomes a function of only C_{oss} and ω:

$$|Z| \approx \frac{1}{\omega C_{oss}(v_{DS})}. \tag{4.39}$$

Therefore, the current in the circuit is determined by C_{oss} for all practical purposes. This allows us to consider R_{oss} as a perturbation element. In other words, the voltage across R_{oss} can be neglected (i.e.,

$v_R \approxeq 0$ in Figure 4.43). The current in the capacitor is given as

$$i = C_{oss} \cdot dv_C/dt. \tag{4.40}$$

Since $v_R \approxeq 0$, we get $v_C = v_{DS}$. Then Eq. (4.40) can be written as

$$i = C_{oss} \cdot dv_{DS}/dt. \tag{4.41}$$

Using Equations 4.36 and 4.41, we can write

$$E_{diss} = \int_0^T (C_{oss} \cdot dv_{DS}/dt)^2 \cdot R_{oss}\, dt. \tag{4.42}$$

At this juncture, we realize that the symbolic calculation of the integral on the RHS of Eq. (4.42) is not straightforward. This is because the value of dv_{DS}/dt changes with v_{DS} (or equivalently, with time) for sinusoidal excitations. In fact, it depends on the excitation voltage pattern.

To simplify the analysis and arrive at a qualitative solution, we consider a triangular waveform as the excitation pattern,[24] where there is a linear increase of voltage from 0 to a maximum of V_p, during a time equal to $T/2$. Then we get $dv_{DS}/dt = \dfrac{V_p}{T/2}$: a time equal to $T/2$ is required for v_{DS} to change from 0 to V_p (the same amount of time is required to change from V_p to 0). For such an excitation type, we can simplify Eq. (4.42) as

$$E_{diss} = R_{oss} \cdot \frac{V_p}{T/2} \int_0^T C^2\, dv_{DS}. \tag{4.43}$$

We can rewrite the integral on the RHS as $2\cdot(\int_0^{V_p} C^2\, dv_{DS})$, where we also identify that $\int_0^{V_p} C^2\, dv_{DS} = V_p \cdot C^2_{oss(RMS)}$. Finally, we get

$$E_{diss} = 4f \cdot V_p^2\, C^2_{oss(RMS)} R_{oss}. \tag{4.44}$$

In general, for large-signal excitations on device drain–source terminals (from 0 to V_p), E_{diss} can be given by Eq. (4.45), as long as

1. the consequences of the excitation pattern can be effectively represented by the parameter k.
2. R_{oss} can be considered fixed for the considered voltage swing (0 to V_p).

$$E_{diss} = kfV_p^2 C^2_{oss(RMS)} R_{oss} \tag{4.45}$$

4.4.4.1 The Practicality of Eq. (4.45)

For sinusoidal excitations, the integral in Eq. (4.42) has no analytical solution in closed form due to the non-linear nature of C_{oss} and should be solved numerically. However, a simplified answer can be estimated assuming a linear C_{oss} value. To show this, first consider a non-linear capacitance that can

[24] This was the assumption used in the analysis given in the work by Mohammad et al. [68].

be represented as given by Eq. (2.19), which we rewrite here for convenience with $m = 1/2$:

$$C_{\text{oss}} = \frac{C_0}{\left(1 + \frac{v_{\text{DS}}}{V_0}\right)^{\frac{1}{2}}}. \tag{4.46}$$

Here, C_0 is the capacitance at $v_{\text{DS}} = 0$, and V_0 ($> v_{\text{DS}}$) is a device-specific constant.

Using Eq. (4.42), for a linear capacitance of C_0 and sinusoidal excitation, it can be shown that $k = \pi^2/2 \approx 4.9$. This suggests that for the non-linear capacitance given by Eq. (4.46), the integral in Eq. (4.42) would result in an effective value for k that is less than 4.9, suggesting a lower E_{diss}. Experimental confirmation of this can be found in the work by Zulauf et al. [17] that presents E_{diss} values for a selected GaN device. The experiments were carried out for both sinusoidal and square-wave (resembling a trapezoidal excitation) excitations at 10 MHz. The results showed that the losses for the sinusoidal excitation were always lower compared to the square-wave excitation.

4.4.4.2 Use of a Loss Tangent

To develop a unified loss-parameter that includes frequency dependence, a C_{oss}-loss-tangent can be defined as

$$\tan(\delta) = \frac{R_{\text{oss}}}{|X_{\text{c}}|} = \frac{R_{\text{oss}}}{1/(\omega C_{\text{oss(RMS)}})} = \omega C_{\text{oss(RMS)}} R_{\text{oss}} = \omega \tau_0. \tag{4.47}$$

By using Eq. (4.45) and 4.47, a normalized E_{diss} is defined with respect to an effective stored energy ($= \frac{1}{2} C_{\text{oss(RMS)}} \cdot V_{\text{p}}^2$) of device C_{oss}:

$$\overline{E_{\text{diss}}} = \frac{E_{\text{diss}}}{\frac{1}{2} C_{\text{oss(RMS)}} \cdot V_{\text{p}}^2} = \frac{k}{\pi} \tan(\delta). \tag{4.48}$$

It should be noted that $\tan(\delta)$ normalizes E_{diss} and encompasses $C_{\text{oss(RMS)}}$, R_{oss} and f in a single parameter for loss evaluation. Equations 4.30 and 4.47 show that $\tan(\delta)$ is constant for a given family and is independent of the current rating. Also, Eq. (4.48) shows that scaling up increases (as $C_{\text{oss(RMS)}}$ increases) the absolute E_{diss} within a device family.

For different device families, the family with the lowest $\tan(\delta)$ offers the lowest E_{diss} for a given value of stored energy (or equivalently, for a given current capability).

It should be noted that the parameter k is a factor that depends on the large-signal excitation[25] and is independent of the device structure. On the other hand, $\tan(\delta)$ is a device-specific parameter and is independent of k. Thus $\tan(\delta)$ allows comparing the soft-switching performance of different device families independently of the excitation signal.

[25] Since $v_{\text{GS}} = 0$ V, the large-signal excitation on the device, and hence, the voltage-transient time of v_{DS}, is determined by the external load and C_{o}.

4.4.5 Qualitative Results

In this section, we provide further insights on the implications of R_{oss} and $\tan(\delta)$ for the output-capacitance hysteresis losses in commercial power FETs.

As was mentioned previously in Section 4.4.1, it was not possible to measure the value R_{oss} at higher voltages due to technical limitations. In Figure 4.39 (see Section 4.4.2), we also observed that R_{oss} is not a strong function of voltage (up to 40 V) for the two devices considered. Most of the devices used in this study (belonging to the families given in Table 4.4) exhibit such behaviour. Based on this, for the following qualitative analysis, we assume that the value of R_{oss} at higher voltages, for example at 400 V, does not offer significant deviations (i.e., no order-of-magnitude changes). We also present experimental confirmation of the predictions based on $\tan(\delta)$.

The loss tangents and the related percentage losses (with respect to an effective stored energy $\frac{1}{2}C_{\text{oss(RMS)}} \cdot V_{\text{p}}^2$) with the excitation frequency (up to 50 MHz) are plotted in Figure 4.44(a) for different device structures: Si, SiC, and GaN power devices with similar current ratings—and rated voltage between 500–900 V—are considered. Note that, since R_{oss} is a frequency-dependent parameter, as illustrated in the example-cases shown in Figure 4.38(b), the value of $\tan(\delta)$ changes non-linearly with f. For frequencies below 15 MHz, the Si MOSFET (planar/conventional) and two GaN devices show $\tan(\delta)$ values well below 0.01, with less than 1% of losses. However, above 15 MHz, GaN devices show the lowest $\tan(\delta)$ values, generally below 3% of losses. The lower rate of increase of $\tan(\delta)$ towards the large frequencies of the GaN devices is attributed to the general decrease of R_{oss} with frequency. The significant increase of $\tan(\delta)$ of the Si device up to 25 MHz, leading up to $\approx$ 8% losses is due to the large increase of its R_{oss} in this frequency region. The SiC devices show negligible variation in their $\tan(\delta)$ values between 5 to 30 MHz. This agrees well with the conclusions by Zulauf et al. in their work [22], where the measured E_{diss} for the tested SiC devices show little change within the considered frequency range. All the SiC devices generally show higher losses for the whole frequency range.

Figure 4.44(b) plots $\tan(\delta)$ value with $R_{\text{DS(on)}}$ for different devices within a family at 10 MHz (solid lines) and at 25 MHz (dotted lines): the same five families (A to E) that were used in 4.4.3 are considered here. For all the device families it is observed that $\tan(\delta)$ stays fairly constant for 10 MHz, irrespective of the value of $R_{\text{DS(on)}}$, hence with the device current rating. This is in agreement with Eq. (4.32) and is expected based on the linear behaviour observed between R_{oss} and $R_{\text{DS(on)}}$ at 10 MHz from Figure 4.40. A similar trend can be seen at 25 MHz, except for the Si family that shows a deviated behaviour with much higher $\tan(\delta)$ values at lower $R_{\text{DS(on)}}$ values. The families A (Si) and B (GaN) offer the best performance at 10 MHz, with $\tan(\delta) \approx 0.005$; however, the GaN family B offers much lower $R_{\text{DS(on)}}$, allowing the same level of soft-switching performance at a much higher current rating.

Based on our analysis and results so far, next, we try to evaluate the utilization of the concept of $\tan(\delta)$, on the actual large-signal operation. Since it can generally be assumed that $E_{\text{oss}} \propto C_{\text{oss(RMS)}}$, and based on Eq. (4.48), the device family with the lowest $\tan(\delta)$ should be selected as the preferred choice to minimize E_{diss} for a given E_{oss}. To corroborate this experimentally, two Si and SiC devices were excited with the Sawyer–Tower circuit at a peak voltage of 400 V and a frequency of 900 kHz. The devices have similar E_{oss} values (around 10 μJ) and the same hardware package (TO-247); also, similar environmental conditions were maintained during the test. Figure 4.45 shows the impedance-plane measurements of the two devices, whose $|X_{\text{c}}|$ values lie in the same range, indicating E_{oss} values that are in close range. Steady-state thermal images of the two devices are also shown in Figure 4.45. The SiC device exhibits much higher power dissipation compared to the Si device. This is due to its much larger $\tan(\delta)$ value ($\approx$ 0.013) which is more than an order of magnitude larger compared to the Si device.

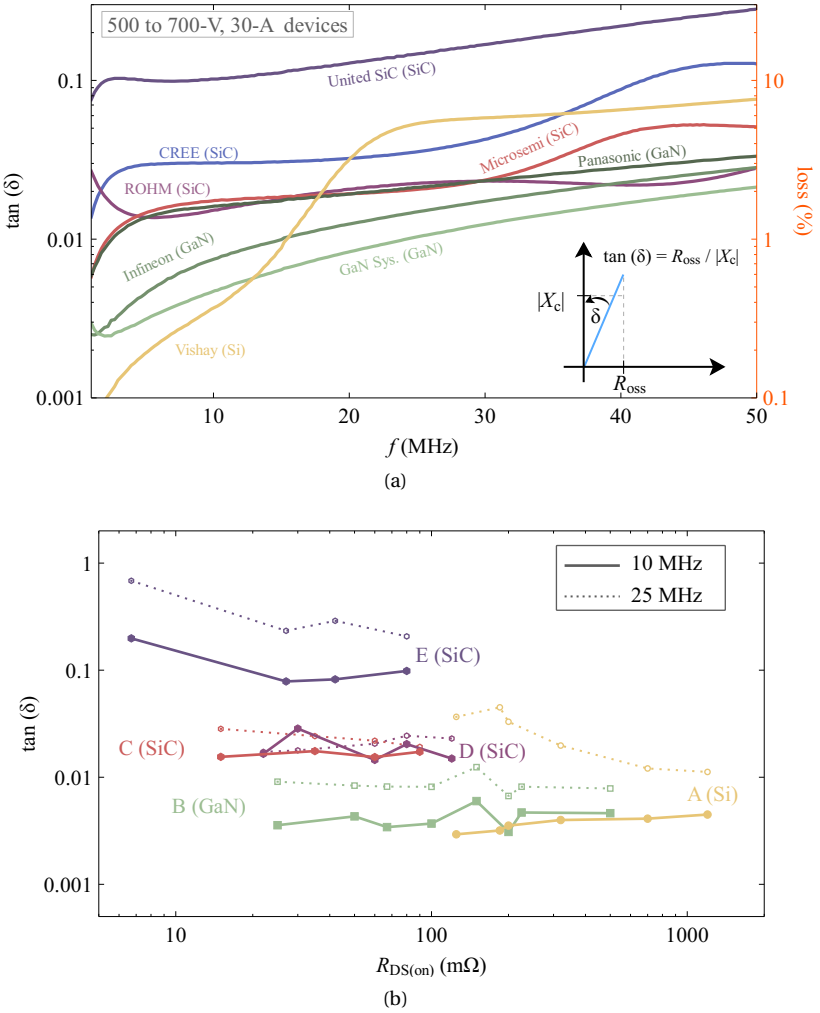


Figure 4.44: (a) Variation of tan (δ) *vs* f for 30-A 500–900-V devices from different manufacturers. The percentage losses are also given with respect to their effective stored energies, where the factor k/pi from Eq. (4.48) is not considered. A sinusoidal excitation signal with a peak of 100 mV was employed. (b) Variation of tan(δ) with $R_{DS(on)}$ for the device families A-E (tabulated in Table 4.4), measured at f = 10 MHz (solid lines) and f = 25 MHz (dotted lines), with $C_{oss(RMS)}$ values estimated at v_{DS} = 400 V.

It should be important to note that the loss-tangent method should only be considered for frequency-dependent energy losses, which can be characterized by the small-signal parameter R_{oss}. This is the case observed in most WBG devices [68]. For such devices, tan(δ) can be used as a qualitative measure of the large-signal hysteresis losses. On the other hand, the frequency-independent energy losses related to C_o [68], which can be observed mostly in Si-SJ devices, should be estimated using large-signal measurement methods, like the Sawyer–Tower method.[26] Since these losses are observed at much lower frequencies, such as 10-50 kHz [70], at which the value of tan(δ) is negligible, the extracted frequency-independent loss is a good measure of the C_o losses. It should be noted that such a device could exhibit a frequency-dependent energy loss component, which could become dominant and surpasses the frequency-independent portion at larger frequencies.

[26] The *QV* hysteresis patterns observed in Si-SJ devices cannot be modelled by a simple resistive parameter. See Section 4.4.7 and Section 4.6 for more details.

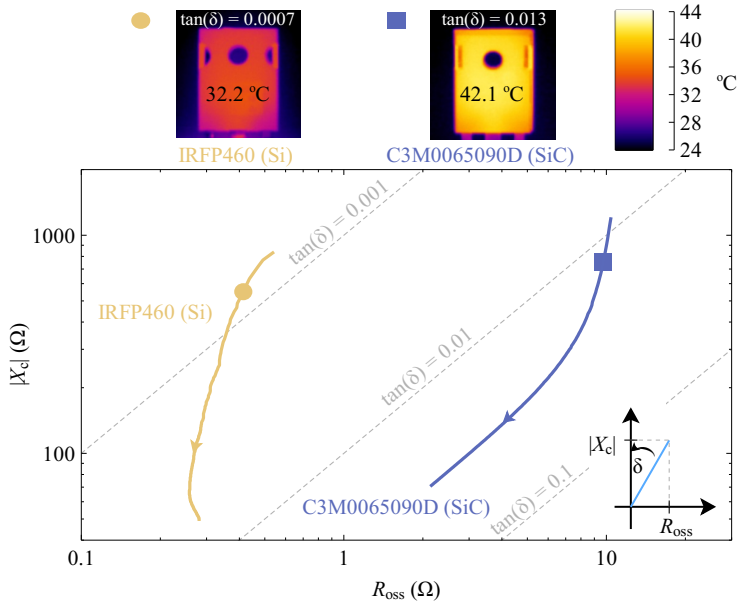


Figure 4.45: Temperature rise observed in two devices that have approximately equal E_{oss} values ($\approx 10\ \mu J$) at 400V, but different tan(δ) values. The devices are excited using the Sawyer–Tower circuit with a v_{DS} swing of 0–400 V and $f = 900$ kHz. Note: the arrows in $|X_c|$ curves show the direction of increasing frequency.

4.4.6 Discussion

Based on the concepts introduced related to R_{oss} and tan(δ), in this subsection, we discuss the selection of devices for high-frequency soft-switching applications. The conduction power loss (P_{con}) and soft-switching power loss (P_{diss}) of a device can be expressed as given in Equations 4.49 and 4.50, respectively. P_{con} is evaluated for a 50% duty cycle, where I_{load} is defined as a sinusoidal RMS current that is equal to 50% of the rated current of the device.

$$P_{con} = 0.5\, I_{load}^2\, R_{DS(on)} \tag{4.49}$$

$$P_{diss} = f \cdot E_{diss} = f \cdot \frac{k}{\pi} \tan(\delta) \cdot \frac{1}{2} C_{oss}^{eff}\, V_p^2 \tag{4.50}$$

To minimize the total losses in a soft-switching device, the total loss $P_{con} + P_{diss}$ should be minimized. To provide a perspective to this requirement, the relative distributions of P_{con} and P_{diss} of the commercial device families A-C are plotted in Figure 4.46. The solid lines show the maximum possible P_{con} for a given family. The P_{diss} values (at $V_p = 400$ V) for all the considered devices are shown at two frequencies, 1 MHz (dots) and 40 MHz (stars). A general guide for the selection of devices for soft-switching applications can be presented as follows.

At low frequencies (typically below 1 MHz), P_{con} dominates the losses,[27] thus one needs to minimize the losses by selecting the device with the lowest $R_{DS(on)}$. At high frequencies (which we consider as frequencies above 5-10 MHz), P_{diss} dominates the losses, and therefore, should be minimized. This can be achieved in two ways based on the design problem.

[27] Not considering lightly-loaded conditions.

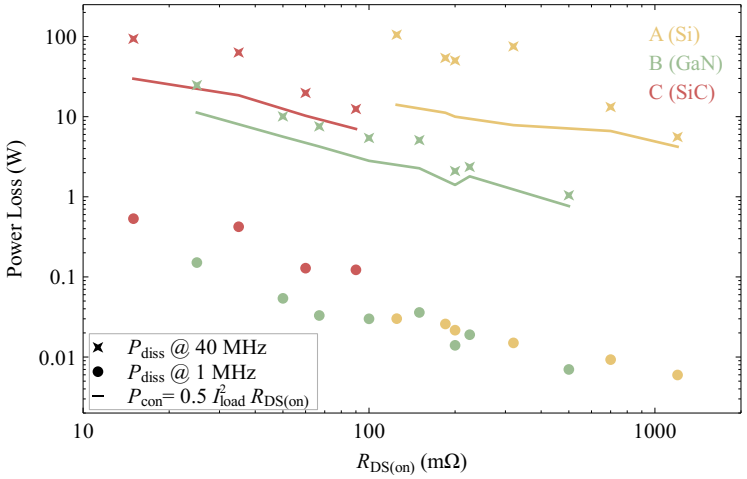


Figure 4.46: Comparison of power-loss levels with $R_{DS(on)}$ for three device families, where yellow, green, and red colours correspond to the device families A-C (tabulated in Table 4.4), respectively. The solid lines show the maximum possible conduction loss (P_{con}) for a given family for 50% of the rated current. Soft-switching power loss (P_{diss}) values of each considered device (for a V_p of 400 V) are shown at 1 MHz (dots) and 40 MHz (stars).

1. On the one hand, if the selection is within a given family, the device with the lowest E_{oss} (or $C_{oss(RMS)}$) should be selected. This is because tan(δ) is fixed for a family and the losses scale with $C_{oss(RMS)}$. Based on Eq. (4.32), this means selecting the device with the highest $R_{DS(on)}$, which is an approach contrary to the conventional belief. This can be understood from Figure 4.46, where all families tend to show lower P_{diss} with higher $R_{DS(on)}$.

2. On the other hand, if the E_{oss} value is given, similar to the case study in Figure 4.45, the device with the lowest tan(δ) value should be selected.

Figure 4.46 also highlights some important aspects of the selected commercial device families. The Si and the GaN families offer lower P_{diss} values (< 100 mW) at 1 MHz, while at 40 MHz, the GaN family (B) offers the lowest losses (< 10 W). At very-high frequencies, such as 40 MHz, the soft-switching losses dominate in comparison with the conduction losses and result in significant power losses. As the conduction losses could be well below their maximum possible value for a certain application (i.e., much below the solid lines indicated in Figure 4.46), optimization of P_{diss} for switching frequencies of tens of MHz is extremely important.

4.4.7 Recent Research and Limitations of the Approach

Although the concepts related to R_{oss} aid in providing a qualitative representation of large-signal hysteresis losses, there are certain limitations with the approach, especially when R_{oss} is considered to be voltage-independent.

Referring to Figure 4.43, we consider an excitation of the circuit such that V_p = 400 V and f = 1 MHz. We consider two cases:

1. C_{oss} is a linear capacitor of 470 pF.

2. C_{oss} is a nonlinear output capacitance (based on the SPICE model of the transistor GS66508T).

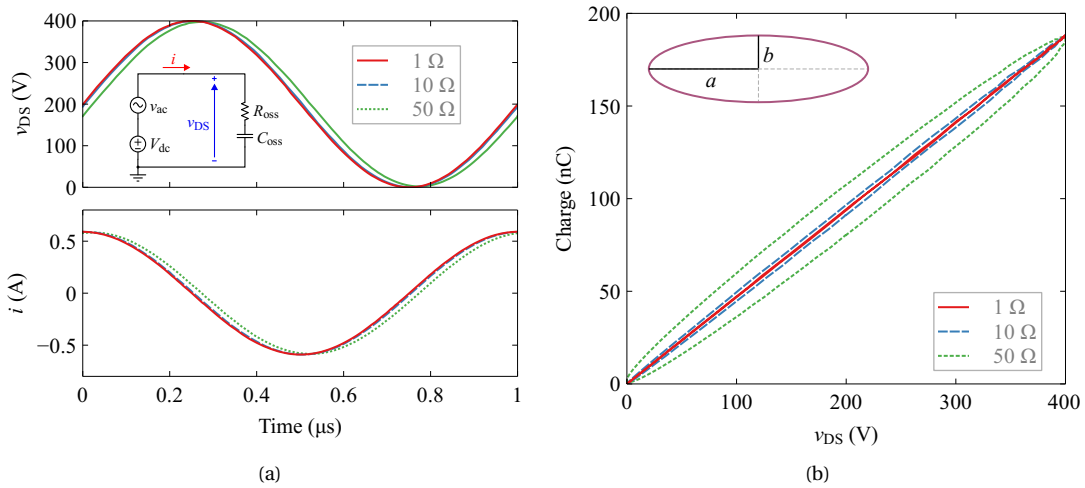


Figure 4.47: Large-signal excitation of the output-capacitance branch, which is modelled with the small-signal quantities C_{oss} and R_{oss} (also see Figure 4.43). A linear capacitance of value 470 pF is used for C_{oss} and three fixed values are considered for R_{oss}: 1, 10 and 50 Ω. (a) voltage and current waveforms. (b) QV curves. Conditions: $V_{dc} = \frac{V_p}{2}$ and $v_{ac} = \frac{V_p}{2}\left(1+\sin(2\pi f t)\right)$, where $V_p = 400$ V and $f = 1$ MHz.

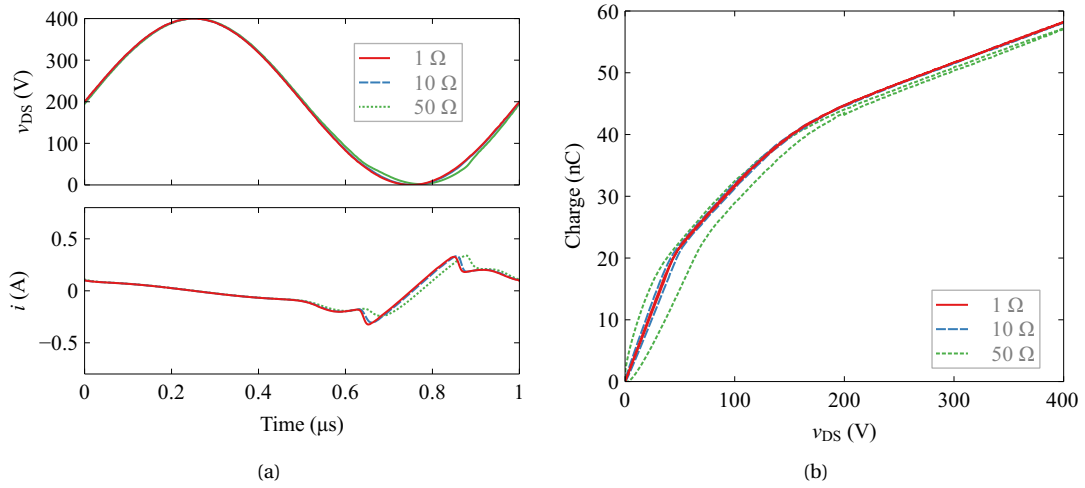


Figure 4.48: Large-signal excitation of the output-capacitance branch, which is modelled with the small-signal quantities C_{oss} and R_{oss} (also see Figure 4.43). The non-linear output capacitance of a GaN HEMT (GS66508T) is used for C_{oss}. Three fixed values are considered for R_{oss}: 1, 10 and 50 Ω. (a) voltage and current waveforms. (b) QV curves. Conditions: $V_{dc} = \frac{V_p}{2}$ and $v_{ac} = \frac{V_p}{2}\left(1+\sin(2\pi f t)\right)$, where $V_p = 400$ V and $f = 1$ MHz.

For both cases, we consider three fixed values for R_{oss}: 1, 10 and 50 Ω. LTspice simulation results for the two scenarios are shown in Figures 4.47 and 4.48. For the first case, it can be observed that the hysteresis pattern is elliptical, where increasing values of R_{oss} causes the semi-minor axis [the distance b of the ellipse shown at the top left corner in Figure 4.47(b)] of the ellipse to increase. For the non-linear case of C_{oss}, Figure 4.48 shows that the outwardly-curved portion of the hysteresis loop concentrates towards the lower range of v_{DS}: this is because of the much larger value of C_{oss} at low v_{DS} values that significantly increase the value of RC product. Referring back to the QV patterns that

were observed with the Sawyer–Tower circuit in Section 4.3, it is clear that a simple fixed-R_{oss} cannot completely recreate the experimentally observed large-signal hysteresis patterns, especially for the Si-SJ devices. This is the main reason for the claims by Fedison et al. on the limitations of the R_{oss} [13]—see Section 4.4.1.

At the time of writing, recent work by an Australian research group has shed light on these limitations in more detail [71]. The work specifically addresses the issue of a voltage-independent R_{oss} and proposes a voltage-dependent R_{oss} model that better represents QV-hysteresis curves for a Panasonic PGA26E19BA device. However, any experimental measurement of R_{oss} at high v_{DS} values was not reported. Another recent work has investigated the origins of soft-switching losses concerning SiC devices [72]. The authors have used an RC model (consisting of C_{oss} and a fixed resistance termed R_{oss}) to model C_o-hysteresis losses when a device is excited using Sawyer–Tower circuit. But, the work does not present any discussion on the experimental measurement of R_{oss}. The 2021 work by Escudero et al. discusses the practical evaluation of soft-switching losses in the secondary-side low-voltage rectifiers, in relation to an LLC converter [73]. Although the authors report hysteresis losses for several MOSFETS and refer to R_{oss} as an equivalent series resistance, to which the hysteresis losses can be attributed, no additional discussion on R_{oss} or its measurement is given.

We believe that the unavailability of R_{oss} values at high voltages is a critical limitation and identify it as an important direction for additional research. Based on our observations of QV patterns with Sawyer–Tower circuit, a voltage-dependent R_{oss} render itself a more realistic approach than a voltage-independent one, especially when the quantitative evaluation of hysteresis losses and SPICE modelling are concerned.

4.5 Origins of Output-Capacitance Hysteresis Losses

A brief discussion on the existing knowledge on the origins of C_o hysteresis losses is given in this section.[28]

Since the report of hysteresis losses observed in Si-SJ FETs [13], several research works have investigated and modelled the origin of these losses with a certain level of experimental validation. A first investigation was presented by Roig et al. for Si-SJ structures [15]. The authors associated C_o hysteresis with trapped stranded charges (Q_{STR}), using mixed-mode simulations. They studied both multi-epitaxy multi-implant (MEMI) and trench-filled epitaxial growth (TFEG) SJ structures and reported that the former is more prone to E_{diss} losses. The claims were further studied and confirmed by Zulauf et al. [18]. The more recent work by Lin further studied TFEG structures with numerical simulations and reported that the finite velocities of the carriers in the semiconductor are the root cause for C_o hysteresis in those devices [74].

Some initial studies on the origin of C_o hysteresis losses in GaN-on-Si HEMTs have also been reported [21, 75]. Guacci et al. investigated a 600-V device with a p-GaN ohmic gate (device GaN-2 studied in our work) [21]. The study proposed that the cause for the observed hysteresis loss is linked to the non-ideal insulating properties of the GaN carbon-doped buffer, which result in a parasitic resistive behaviour for the drain–substrate capacitance. Such a hypothesis was confirmed by the introduction of an improved GaN buffer design, which resulted in a reduced hysteresis loss. Zhuang et al. modelled and analysed a depletion-mode (D-mode) GaN-on-Si device, and consequently, identified additional

[28] Detailed device-level investigations and modelling was not a part of this thesis work but could serve as an interesting platform for future work.

C_o loss mechanisms [75]: 1) resistive losses in the GaN stack; 2) resistive losses in the Si substrate, related to the doping concentration; and 3) losses in the GaN stack due to traps.

The GaN devices studied in Section 4.3 of this thesis, to the best of our knowledge, belong to three different device architectures: device GaN-1 is a true e-mode device based on a Schottky *p*-GaN gate structure; devices GaN-2 and GaN-3 are true e-mode devices featuring an ohmic *p*-GaN gate contact [6]; and, GaN-4 is a cascode device.[29] Interestingly, the *QV* patterns observed in Section 4.3.3 also show three different variations for these devices: device GaN-1 shows no hysteresis, devices GaN-2 and GaN-3 show hysteresis only above 100 V, and the cascode structure shows a significantly–large hysteresis loss. These observations suggest that additional investigations from device manufacturers are required as complete knowledge of device structures are proprietary.

As for SiC devices, Bura et al. suspected that the trapping in the dielectric interface states could be the reason for related hysteresis losses [19]. The work by Zulauf et al. confirms this suspicion and states that the loss mechanism should be different to GaN-on-Si HEMTs [22]. At the time of writing this thesis, a subsequent publication by Tong et al. has attributed C_o-hysteresis losses in SiC power MOSFETS and diodes to a resistive loss in the termination region of the device[72].[30] They further claim that frequency-dependence of E_{diss} and related *QV*-behaviour is defined by incomplete ionizations.

In summary, the C_o-hysteresis losses in Si-SJ devices appear to be understood better in comparison with that in WBG devices. On the other hand, it could be argued that, since WBG devices are still emerging, unlike the Si technology, the original reasons for these losses could also vary, as researchers and manufacturers try new, and if not ambitious, device designs. Nevertheless, it is recommended that the manufacturers acknowledge these losses, with the basic information on quantitative values. The knowledge of these losses (with voltage and frequency) is imperative for the design of high-frequency power converters, from the circuit engineer's perspective.

4.5.1 On the Cascode Configuration and C_o-Hysteresis Losses

This subsection presents some preliminary investigations we have carried out on the cascode configuration. We believe these findings will provide further clarifications on C_o-hysteresis losses and create an interesting avenue for future research work.

An important observation in Figure 4.24 is that the hysteresis pattern observed for the cascode GaN device is drastically different compared with the other three GaN devices. A simple schematic of the cascode configuration is shown in Figure 4.49(a). Since all the considered GaN devices are lateral devices, and, in general, share a common structure apart from the gate design, it was of great interest to identify if the hysteresis pattern is an undesired consequence of the cascode configuration/arrangement itself. To find an answer, we carried out a simulation-level investigation. Figure 4.49(b) plots the *QV* curves obtained using the Sawyer–Tower technique for the cascode device: both simulation (dashed green lines) and experimental (red and blue solid lines) results are shown, alongside the datasheet curve (solid black line). For the simulation, the manufacturer-provided device SPICE model was used. In Figure 4.49(b), it can be observed that the simulation model exhibits C_o-hysteresis, although not as large as the experimental result; the bulging of the pattern at lower voltages and the coincidence of charge–discharge curves beyond 250 V can be observed in both the simulation and the experimental result. It should be noted that a typical NMOS SPICE model does not result in such a hysteresis pattern.

[29] See Section 4.5.1 for additional discussion on this structure.

[30] The authors have supported their main claims by TCAD simulations and experimental results based on the Sawyer–Tower method.

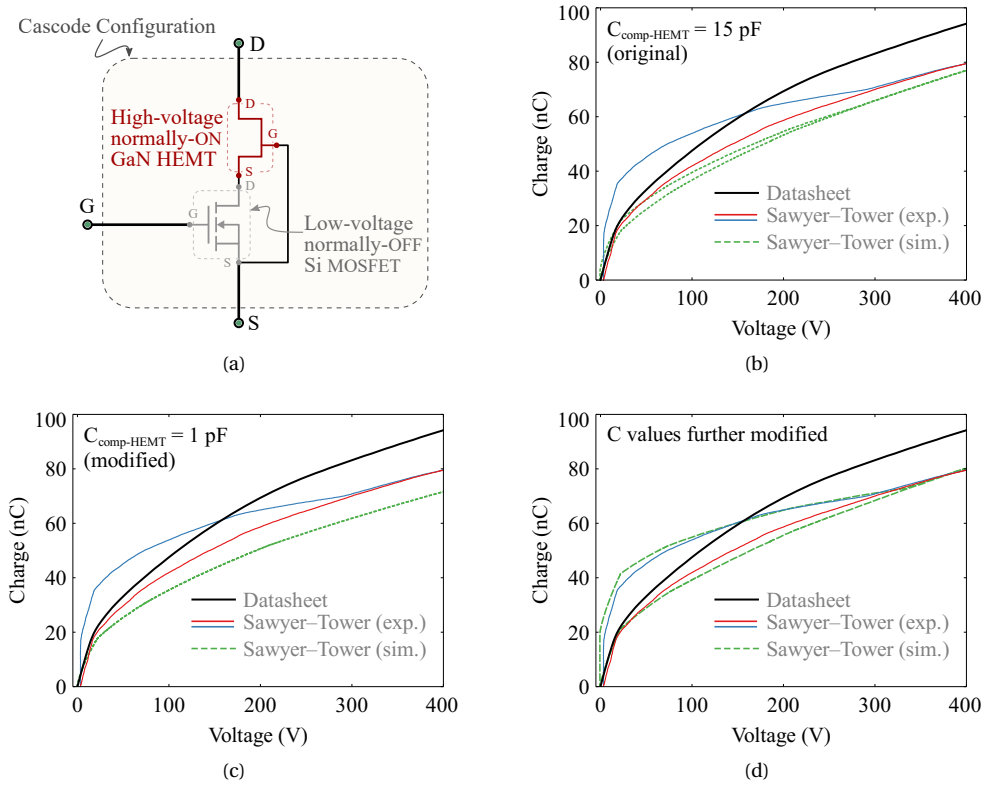


Figure 4.49: (a) Schematic of GaN-cascode configuration, where a low-voltage enhancement-mode (normally-OFF) Si MOSFET is connected in series with a depletion-mode (normally-ON) GaN HEMT [4]. The subfigures (b)–(c) consider device GaN-1 (TPH3212PS) studied in Section 4.3. Datasheet-based *QV* curve as well as experimental Sawyer–Tower results are also indicated. For the Sawyer–Tower circuit-based simulation results (dashed green lines), however, we consider three different cases of SPICE-model variations: (b) original SPICE model from the manufacturer (ver 2.0, 2016); (c) the capacitance component defined as $C_{comp\text{-}HEMT}$ in the SPICE model is changed from 15 pF to 1 pF; (d) a particular combination of the values of the capacitances $C_{comp\text{-}HEMT}$, $C_{comp\text{-}NMOS}$, and $C_{GD\text{-}HEMT}$ (in the SPICE model, there exist three capacitance values that define $C_{GD\text{-}HEMT}$) that could explain the experimentally-observed pattern. Note: the Sawyer–tower circuit is operated with f = 100 kHz, C_{ref} = 1 nF, and $V_{DS\text{-}max}$ = 400 V.

Furthermore, introducing a fixed R_{oss} component in series with device C_{oss} also cannot develop this particular result (see our analysis in Section 4.4.7); even the use of a nonlinear and monotonic R_{oss} is highly unlikely to create the behaviour observed in Figure 4.49(b).[31]

Next, we examined the particular SPICE model. A modification of the value of a parasitic capacitance[32] related to the HEMT from 15 pF to 1 pF, as shown by Figure 4.49(c), completely removes the hysteresis pattern.[33] Moreover, a certain combination of the values of the parasitic capacitances in the SPICE model of the cascode configuration,[34] in fact, can explain the experimentally-observed hysteresis, while maintaining the same $Q_o$value at 400 V—see Figure 4.49(d). Moreover, for the SPICE model used in Figure 4.49(d), we have carried out simulations where V_p is less than 100 V; agreeing

[31] See also the work by Mahajan et al., where the effects of a nonlinear R_{oss} are analysed [71].

[32] Defined under the term *HEMT_A Cap Compensation,* which we found to be effectively connected between drain–source terminals of the HEMT. This is denoted as $C_{comp\text{-}HEMT}$ in Figures 4.49(b) and 4.49(c). However, it is not clear why this capacitance is termed as a compensating capacitance.

[33] It can also be observed that this slightly reduces the $Q_o$value (for a given voltage). This is expected as part of the drain–source parasitic capacitance of the HEMT is now reduced.

[34] The values of the capacitances $C_{comp\text{-}HEMT}$, $C_{comp\text{-}NMOS}$, and $C_{GD\text{-}HEMT}$ in the SPICE model were modified.

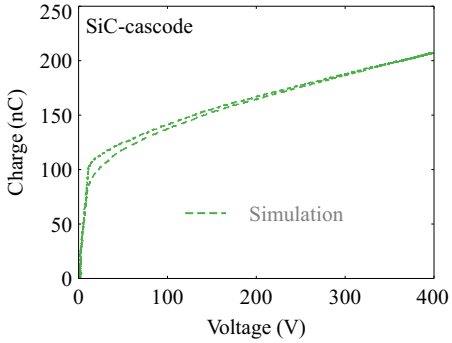


Figure 4.50: Simulation results of the *QV* curves of the SiC cascode device UJC1210K (1200 V, 100 mΩ, 20 A) obtained using the Sawyer–Tower circuit. Similar to the GaN-cascode device considered in Figure 4.49, the cascode configuration presents a hysteresis pattern in the simulations, that a simple R_{oss} component cannot produce. The simulation used the original SPICE model from the device manufacturer. The Sawyer–tower circuit is operated with f = 100 kHz, C_{ref} = 1 nF, and $V_{DS\text{-}max}$ = 400 V.

with experimental results in Figure 4.29(b), the simulation showed no hysteresis in this case.

In addition, Figure 4.50 plots *QV* curves (simulation results) for a SiC cascode device. We can observe that the particular SPICE model creates a hysteresis pattern that is similar to the experimental hysteresis pattern observed for device SiC-4, which is a cascode device from the same manufacturer. This further verifies that the hysteresis is enabled by the interaction between nonlinear parasitic capacitances and the cascode configuration.

These observations mean that the circuit-level operation of the cascode arrangement itself is responsible for a large-hysteresis pattern (above 100-V operation), which is unrelated to any device-level phenomenon. We believe additional investigations on the circuit-level performance of cascode structure could yield important information on its performance and limitations.

4.6 Categorization of Hysteresis Losses

Here, we present a general overview of our observations related to C_o-hysteresis losses and large-signal *QV* patterns.

4.6.1 Output-Capacitance Hysteresis Losses Beyond 1 MHz

Our observations in Section 4.3 indicated that E_{diss} show negligible frequency dependence below 1 MHz. Other research works have also shown that there is indeed a frequency dependence, whose effects become prominent only above 5–10 MHz [22, 55, 72]: for example, the non-cascode GaN devices [17, 68] and certain SiC families [55, 72].

Moreover, as seen for some SiC devices in the works by Zulauf et al. [22] and Bura et al. [19], the *QV* patterns exhibit symmetrically distributed hysteresis patterns at high frequencies; for SiC-3 device in Figure 4.24, a glimpse of this can be observed even at 100 kHz. It should also be noted that the SiC devices tested in the work by Zulauf et al. did not exhibit any appreciable frequency-dependence at high frequencies (up to 35 MHz). However, for some SiC devices, frequency-dependence has been predicted at high frequencies [54, 55].[35]

[35] The recent work by Tong et al. provided additional verification on this [72].

Certain Si-SJ devices have reported two hysteresis components: a low-frequency hysteresis component with negligible frequency dependence (agreeing with results in Figure 4.30), and a high-frequency component with frequency-dependence [22]. The GaN cascode family (used in Section 4.3) could be expected to behave similarly: 1) our work shows a frequency-independent, but large, hysteresis loss at low frequencies for device GaN-4; and 2) the work by Zulauf et al. shows frequency-dependent hysteresis losses at high frequencies for a device from the same family.

4.6.2 Categorization based on *QV* Patterns

The output-capacitance-related energy losses in a switching circuit can be broadly categorized into two main components as Figure 4.51 shows: hard-switching losses and soft-switching losses. In hard switching, the energy (E_o) stored in C_o is lost when the device is turned ON, as shown by the area shaded in green. There is another loss component called the *co-energy loss* in hard-switching circuits, which will be discussed in chapter 5.

In relation to soft-switching, two basic scenarios in C_o hysteresis losses can be identified depending on their frequency dependence: 1) a frequency-independent energy loss (i.e., a form of dc energy loss), which is significant at very low frequencies such as 10–100 kHz; and 2) a frequency-dependent energy loss that becomes prominent above 5–10 MHz, but insignificant at low frequencies. Based on our observations and the discussion in Section 4.6.1, commercial FETs can potentially be classified into two categories based on *QV* hysteresis patterns as shown in Figure 4.51.

1. Type 1: devices that show a large frequency-independent energy loss at low frequencies and an additional frequency-dependent energy loss at high frequencies.
   e.g.,: devices Si-2, Si-3, Si-4, GaN-4 studied in Section 4.3

2. Type 2: devices that show only frequency-dependent energy losses. They show very small and quite fixed hysteresis losses at frequencies below 1 MHz but increasing losses above 5-10 MHz.
   e.g.,: devices Si-1, SiC-1, GaN-1 studied in Section 4.3

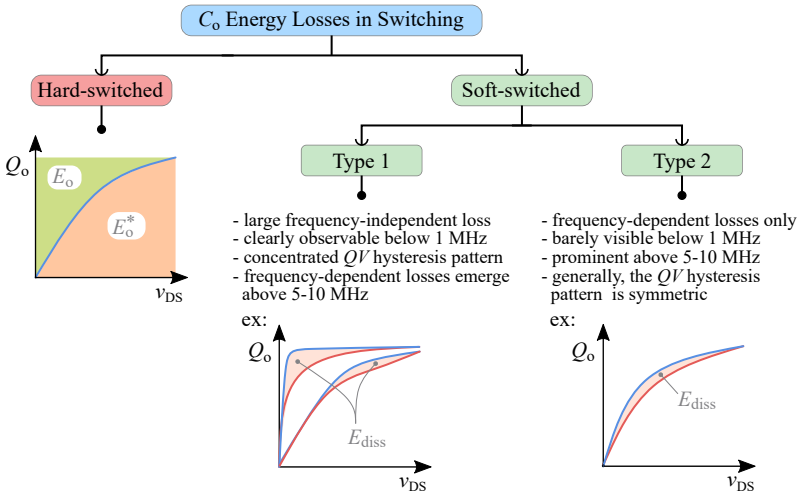


Figure 4.51: Categorization of C_o-related energy losses in hard-switching and soft-switching power electronic topologies. Energy losses in a soft-switched device can be further categorized into two types based on the shape of its *QV* hysteresis pattern as shown. Note: E_o^* is the co-energy component related to hard-switching circuits, which will be discussed in Chapter 5.

Considering the predictions based on R_{oss} in Section 4.4 and results of the work by Zulauf et al. [22] devices that fall under Type 2, exhibit a nearly-quadratic variation with V_p. This also could explain why the E_{diss} values of devices Si-1, SiC-1 and GaN-1 in Figure 4.25 increased with V_p.

4.7 Summary

We started this chapter by providing the background and the motivation for the presented content. Our preliminary investigations were driven by the hysteresis losses observed in the output capacitance of Si-SJ devices, reported by Fedison et al. in 2014. We started our analysis by highlighting the difference in small-signal and large-signal excitations and how the latter is important in identifying C_o-hysteresis losses.

Next, a thorough investigation of the Sawyer–Tower technique was given. Using this technique, then we investigated all four prominent power FET categories (planar-Si, Si-SJ, SiC and GaN) for their output-capacitance-related QV hysteresis patterns and related energy losses. We have shown that different structures exhibit different dependencies on excitation voltage levels, resulting in diverse hysteresis patterns. For instance, some structures show no hysteresis below 100 V, whereas, for another group, hysteresis is a phenomenon above 150–200 V. These observations are essential in identifying the underlying physical phenomena in output-capacitance-related losses.

The possibilities of using small-signal measurements to characterize C_o-hysteresis losses were also discussed. A detailed discussion on the small-signal parameter R_{oss} was given, highlighting its measurement, implication to hysteresis losses, and limitations. Then a brief discussion on the origins of C_o-hysteresis losses from a device perspective was given. Finally, based on experimental results, we provided a useful categorization of output-capacitance hysteresis losses related to soft-switching operation; this aids the power electronics designer to form a qualitative picture of the large-signal C_o-losses existing in commercial power FETs.

5 Output Capacitance and Hard-Switching Circuits

As Chapter 4 discussed in detail, device output capacitance plays a far more important role than device on-resistance in soft-switching circuits. In this chapter, we move into the next logical investigation: the large-signal behaviour of output capacitance in hard-switching circuits.

Here we discuss and analyse in great depth the role of output capacitance in hard-switching circuits and deliver important findings. First, we provide important background knowledge and highlight the main motivations behind this chapter. Then we present the main idea upon which the subsequent analytical work is based: hard-switching presents a fundamentally different charge–discharge mechanism for device output capacitance. Based on this notion, we present the concepts of co-energy loss and discharge-energy loss to establish a clear and simple theory to explain the contribution of C_{o} in a hard-switched turn-ON process, which is shown to be equal to the product $Q_{\mathrm{o}}V_{\mathrm{dc}}$.

With the developed theory, the unique behaviour of the no-load inverter leg configuration is analysed, highlighting its different operating modes. Based on the developed concepts, an experimental technique relying on average electrical measurements is developed to obtain output charge versus voltage (QV) curve for a given FET, which is true to the charge capacity of C_{o} in actual hard switching. This is followed by a comprehensive comparison of the QV behaviour of Si, SiC and GaN devices in small-signal, soft-switching and hard-switching conditions. An extensive discussion on practical and measurement considerations on the measurement method is also given.

As was the case with Chapter 4, the power MOSFETs (of Si, Si-SJ, and SiC technologies) studied in

this chapter are vertical devices, while the GaN devices are *lateral devices*.

This chapter is partly based on the material published in the following articles:

C2. **N. Perera** et al., 'Analysis of Output Capacitance Co-Energy and Discharge Losses in Hard-Switched FETs', in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, Nov. 2020, pp. 52–59.

J3. **N. Perera**, A. Jafari, R. Soleiman Zadeh Ardebili, N. Bollier, S. G. Abeyratne, and E. Matioli, 'Hard-Switching Losses in Power FETs: the Role of Output Capacitance', *IEEE Transactions on Power Electronics*, pp. 1–1, 2021, doi: 10.1109/TPEL.2021.3130831.

5.1 Background and Motivation.

High-frequency (HF) power converters utilizing FETs play an important role in high-power-density applications [6, 22, 26]. The recent years have seen increased interest in the behaviour of FET output capacitance, with new research groups initiating additional investigations [71, 76]. As the initial interest was mainly focused on the large-signal behaviour of C_o in soft-switching operation,[1] any discrepancies in hard-switching operation were often overlooked. This is reasonable as C_o-hysteresis energy losses were mainly observed at high-frequencies and the related power loss becomes appreciable in the MHz range—a range beyond the operational frequency of traditional hard-switching circuits. However, with the advent of WBG devices, the limits of hard-switching frequencies have already been pushed to the MHz range [24].

As we detailed in Chapter 4, the large-signal C_o-hysteresis losses is a major hindrance for soft-switching circuits operating in such frequencies [21–23]. In 30-A devices, for example, these losses vary from a few tens of nanojoules to a few microjoules at 400-V operation, in frequencies below 1 MHz [23]. In contrast, hard-switching energy losses, dominated by the turn-ON loss [41], are typically around 50–500 μJ at 400 V for the same devices. But more importantly—as we will see in this chapter—the role of C_o is fundamentally different in hard-switching converters as opposed to soft-switching operation. Therefore, the effects of any large-signal anomaly in C_o for hard-switching operation—for instance, a change in output charge—first need to be understood from a topological perspective. For example, an error in the estimation of Q_o could translate to a considerable change in power loss at f_sw of several hundreds of kilohertz.

Additional research has shown that the QV curves of certain device types, obtained with small-signal methods at different frequencies, and with the Sawyer–Tower circuit, exhibit a large offset in Q_o in comparison with datasheet curves [18, 22]. This is an important sign that C_o-related losses in hard switching could also be different in actual large-signal operations.

5.2 Basic Concepts

In this section, we discuss the fundamental differences in hard- and soft-switching, which are in general, imposed by the circuit. These distinctions are what determine the eventual energy loss related to switching from a topological perspective for a chosen device.

[1] Please see Section 2.2.1 for important notes on the notation of output capacitance.

5.2.1 Hard-Switching versus Soft-Switching: Current Scenario

In a hard-switched device, the loss distributions of turn-ON and turn-OFF transitions are directly related to C_o. The early insights in separating the turn-ON (E_{on}) and turn-OFF (E_{off}) losses came with the discussion on the differences in the drain and channel currents of a transistor, i_{DS} and i_{CH}, respectively [25, 39, 41]—see also Section 3.1.4. Especially, an E_{qoss} *loss mechanism* was discussed in recent literature [40, 77], highlighting its effects on E_{on}. It was presented as an additional loss in a transistor (during its turn-ON voltage commutation) due to the charging current of the complementary transistor's output capacitance.

In soft-switching circuits, C_o plays a different role but heavily influences the soft-switching process. The charge (Q_o) stored in C_o at a given voltage determines the condition for zero-voltage-switched (ZVS) operation [46]. With a more fundamental view on capacitance-related energy mechanisms, the capacitive co-energy, E_o^*, was utilized by Elferich in 2012 to model switch-node capacitance, C_{sw}, in ZVS circuits [78]. It was shown that the ratio $n_{co} = E_o^* / E_o$ is an important design factor in ZVS circuits; n_{co} increases the energy requirement for the ZVS transition for a given stored energy, E_o. Further insightful analyses on the relation between C_o and ZVS process were carried out by Oeder et al. [79], and Roig et al. [80].

5.2.2 Importance of Topological Distinction

A better perspective on the role of output capacitance in creating losses could be gained by realizing that the charging and discharging processes of C_o are topology-dictated, as illustrated in Figure 5.1. In conventional PWM switching, the charging and discharging of C_o are confined to the switching transitions [marked by blue and red highlights in Figure 5.1(d)]. For example in the double-pulse-test (DPT) circuit, $C_{o,S2}$ gets charged by the dc voltage source during the turn-ON transition of S_1 where the channel of S_1 acts as a resistance in series, $R_{ch,S1}$; this creates an additional energy loss in $R_{ch,S1}$ known as the co-energy loss [52], which is discussed in Section 5.4. We analyse these concepts in Section 5.4.

In contrast, the charging of $C_{o,S1}$ is dictated by the inductor L which does not create the same co-energy loss situation. In the class-E inverter [Figure 5.1(e)], which is a load-resonant soft-switching converter [28], the complete charge–discharge cycle of C_o is spread through the OFF state, unlike in conventional PWM converters. here the process is dictated by the resonant load-inductance, and not the dc voltage source. Thus, any resulting losses are purely due to the hysteretic behaviour of C_o. In resonant-transition switching [Figure 5.1(f)], the charge–discharge process is again dictated by an inductance used to achieve zero-voltage-switching (ZVS) [81], although this process happens only during switching transitions; and any resulting loss related to C_o is purely hysteretic [46].

This analysis shows that a generic measurement technique would not correctly capture the loss related to C_o, as the loss depends on how C_o is being treated in a topology. On the one hand, methods like the Sawyer–Tower technique and its variations [47], do not recreate the actual hard-switching process, and hence, are unsuitable to characterize hard-switching losses. In the Sawyer–Tower circuit, device drain–source terminals experience an excitation similar to what is shown in Figure 5.1(e), and a basic operational difference exists as an ac voltage source is used to charge and discharge C_o. On the other hand, the standard methods used for hard-switching tests cannot separate the individual contribution of C_o from the total switching loss; this is due to the existence of a load current that complicates the analysis as well as any measurement process [25, 39]. To find a comprehensive solution, first, we investigate the fundamental concepts related to the charging process of C_o in hard

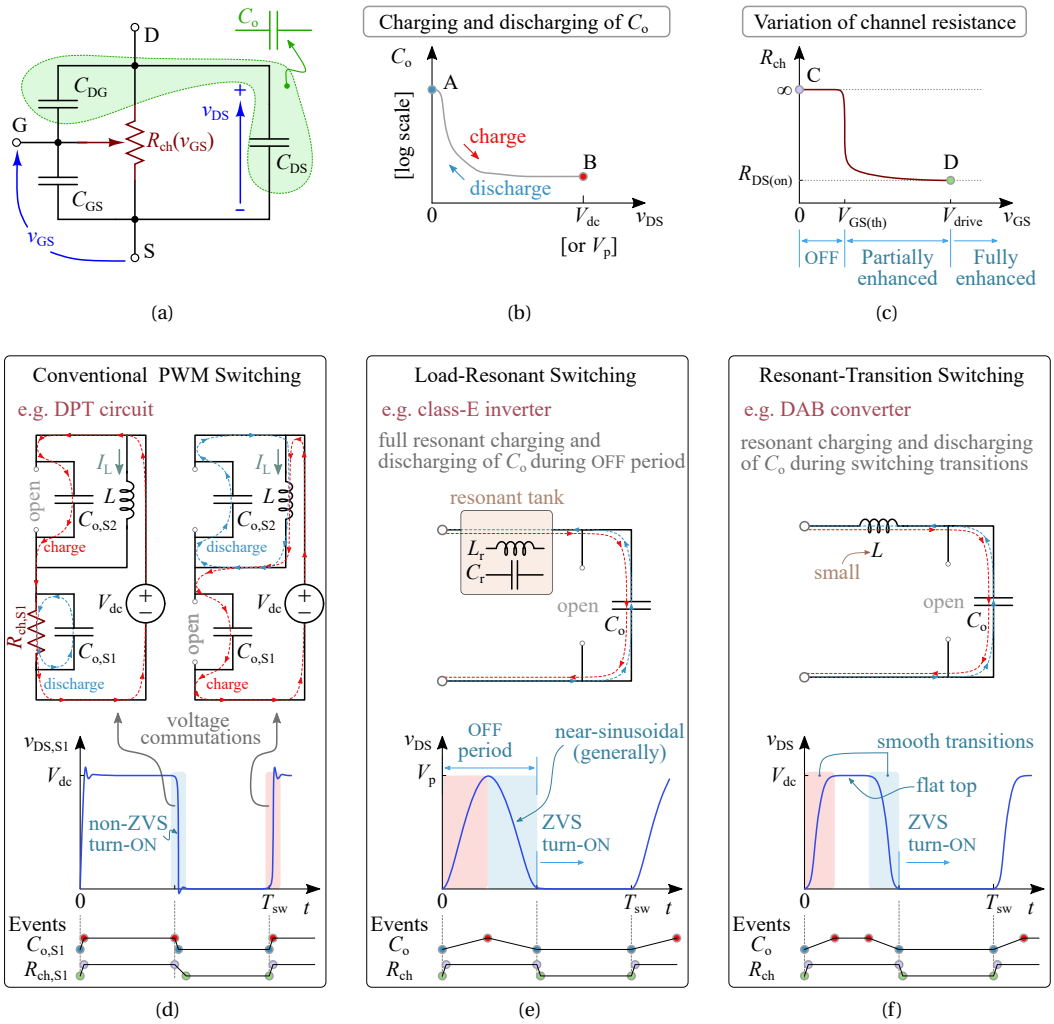


Figure 5.1: Overview of the behaviour of device output capacitance in different topologies. (a) The output capacitance of a FET is defined as $C_o = C_{DG} + C_{DS}$; the channel of the FET can be represented as a variable resistance $R_{ch}(v_{GS})$ dependent on the gate–source voltage v_{GS}. (b) During the charging and discharging processes, C_o traverses the paths A–B and B–A, respectively. (c) The channel resistance (R_{ch}) of the device takes the paths C–D and D–C during its ON and OFF transitions, respectively. The coincidence or non-coincidence of the paths of C_o and R_{ch}, and their nature, are topology dependent. This is highlighted by the events indicated in sub-figures (d), (e) and (f). For a given device, the output-capacitance losses are dependent on how the charge–discharge process is dictated by the circuit (i.e., the voltage waveform across C_o is determined by the topology and energy source). In this regard, and generally speaking, three different scenarios can be found: (d) conventional PWM switching (note: $C_{o,S1}$ and $C_{o,S2}$ are bottom and top device output capacitances, respectively); (e) load-resonant switching; and (f) resonant-transition switching.

switching (Sections 5.3 and 5.4) and then extend the developed concepts (Section 5.5) to devise a simple measurement technique (Section 5.6).

5.2.3 Hard-Switching-Transitions and Related Losses

Before moving into the main analysis, here we introduce and clarify some important terminology related to hard switching (and related losses). Consider Figure 5.2, which illustrates the gate-logic and v_{DS} waveforms for the two devices in a DPT circuit: S_1 is the switching device (bottom device) and as

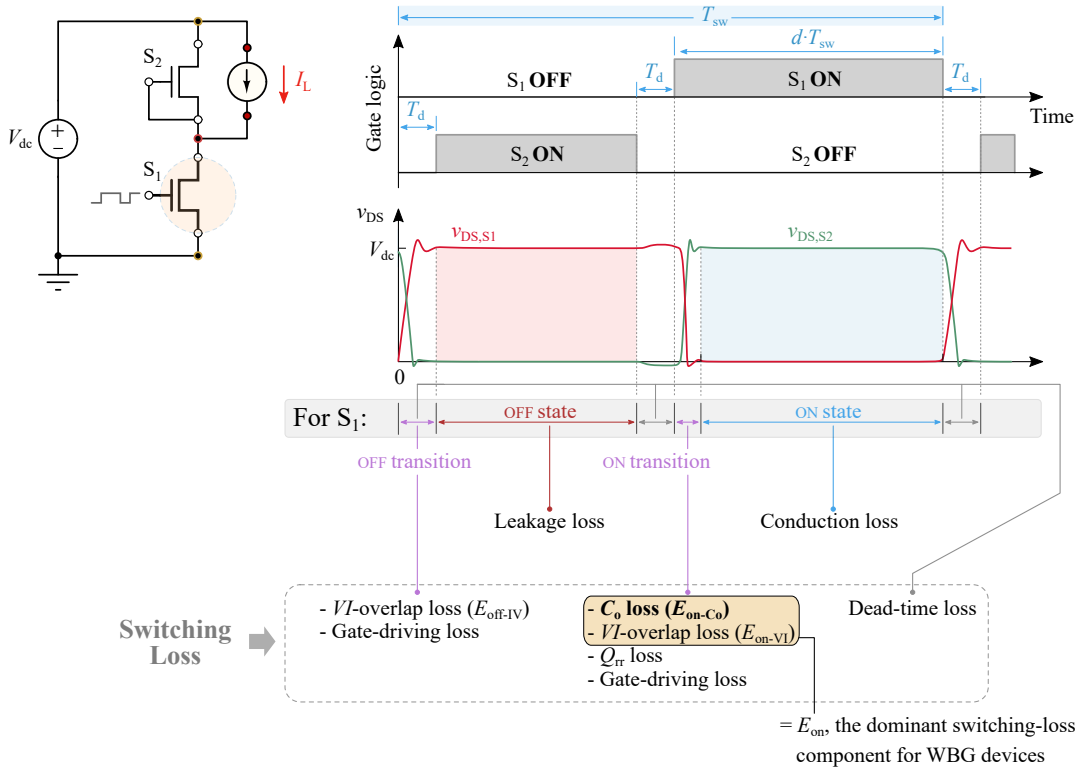


Figure 5.2: Qualitative representation detailing how hard-switching losses occur in a DPT circuit. S_1 is the switching device (bottom device), whereas S_2 (top device) operates in the third quadrant with its G–S terminals shorted (thus, behaves as a diode). All the loss components related to each state or transition are also presented. In general, for FETs, the turn-ON transition incurs the dominant switching-loss component (E_{on}); this, in turn, is dominated by the output-capacitance-related loss, $E_{on\text{-}Co}$, and the *VI* overlap loss, $E_{on\text{-}VI}$, respectively. In this particular topology, the output capacitance of S_1, $C_{o,S1}$, gets charged during the OFF-transition of S_1; and it gets discharged during the ON-transition, while the discharging of the output capacitance of S_2, $C_{o,S2}$, also takes place.

S_2 serves as a reverse conducting FET (top device). The following distinct operating periods can be identified for S_1. We make our distinctions based on the drain–source voltage waveform of the device as its variation indicates charging or discharging of device output capacitance.

- OFF state: v_{DS} is fixed at V_{dc} and the only existing loss in S_1 is related to the device drain–source leakage current (I_{DSS}). This loss is generally negligible. For instance, an I_{DSS} of 1 μA will only result in 0.2 mW at V_{dc} = 400 V for a 0.5 duty ratio.

- ON state: the device channel is fully enhanced (i.e., $R_{ch} = R_{DS(on)}$)[2], and the load current results in the typical conduction loss in the channel.

- turn-OFF transition: v_{DS} of S_1 changes from ON-state voltage to V_{dc}, while the opposite happens to S_2. The output capacitance of S_1, $C_{o,S1}$, gets charged, while the output capacitance of S_2, $C_{o,S2}$, gets discharged. Concerning the channel of S_1, the only related loss is the *VI*-overlap loss, which is denoted as $E_{off\text{-}VI}$. For WBG devices, this loss is not significant [41].

- turn-ON transition: v_{DS} of S_1 changes from V_{dc} to its ON-state voltage. The output capacitance of S_1 gets discharged, while at the same time the charging of the output capacitance of S_2 takes

[2] Also see Section 3.1.1.

place. These two processes incur a considerable loss in the channel of S_1, which we denote as $E_{\text{on-Co}}$. At the same time, a *VI*-overlap loss $E_{\text{on-VI}}$ also occurs in the channel of S_1.

- dead-times: During the dead times, the device channels are cut-off. Depending upon the topology, the dead times could overlap with a switching transition. For example, in this example, the OFF-transition overlaps with the dead-time but the ON-transition occurs after the dead-time. In addition, in this topology, only S_2 operates in the third quadrant, resulting in a dead-time loss.

5.3 Energy Components Related to Charging and Discharging of Capacitors

Typical charge versus voltage curves for a linear and nonlinear capacitor are shown in Figures 5.3(a) and 5.3(b), respectively. We denote both capacitors as C. For the charging process from 0 to Q_1, the *energy stored* in the capacitors is given as

$$E_{\text{C}} = \int_0^{Q_1} v\, dQ, \tag{5.1}$$

where v is the voltage across C. Q is the charge stored in C for a given voltage. Note that E_{C} is also equal to the *discharge loss* when C is discharged.

The integral given in Eq. (5.2) defines the *co-energy* component (discussed in the next Section) related to the output capacitance [52, 78].

$$E_{\text{C}}^{*} = \int_0^{V_1} Q\, dv \tag{5.2}$$

Figure 5.3 also shows that the addition of E_{C} and E_{C}^{*} results in

$$E_{\text{C}} + E_{\text{C}}^{*} = Q_1 V_1. \tag{5.3}$$

The Equations 5.1, 5.2, and 5.3 are valid for both linear and nonlinear capacitors.

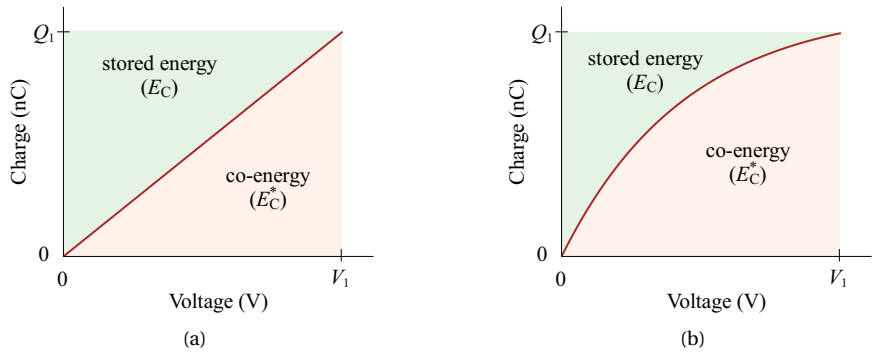


Figure 5.3: The distribution of stored energy (E_{C}) and co-energy (E_{C}^{*}) components in a charge versus voltage (QV) plot related to (a) a linear capacitor, and (b) a nonlinear capacitance.

5.4 Concept of co-energy in a Capacitor

In this section, we introduce the co-energy concept and carry out an extensive analysis of its relation to hard switching. The co-energy is an active loss component that occurs when a capacitor is charged by a *dc voltage source* [82, 83].

5.4.1 Mathematical Analysis

Figure 5.4 shows a circuit where a capacitance C (either linear or non-linear) is being charged by an ideal dc voltage source V_{dc}, in series with a resistance R. The current (i) and charge (Q) delivered from the supply are both functions of time t. The charging process starts at $t = 0$ and ends at $t \to \infty$. The following analysis shows that the final energy components in the process are functions of only V_{dc} and the charge capacity of C, which we denote as Q_1.

The total energy supplied by the dc voltage source at the end of charging is,

$$E_{\text{in}} = \int_0^{\infty} V_{\text{dc}} \cdot i \, dt = V_{\text{dc}} \int_0^{\infty} i \, dt. \tag{5.4}$$

Realizing that $\int_0^{\infty} i \, dt$ is equal to the total charge (Q_1) supplied by the source at the end of the charging process, we get

$$E_{\text{in}} = Q_1 V_{\text{dc}}. \tag{5.5}$$

This indicates that the energy supplied by the source is independent of R and depends only on V_{dc} and Q_1. Next, the energy stored in the capacitance is calculated as

$$E_{\text{C}} = \int_0^{\infty} v_{\text{C}} \cdot i \, dt. \tag{5.6}$$

Using the definition of current (i.e., $i = dQ/dt$), a variable change is applied to the above integral as $i\,dt = dQ$, where $Q = 0$ at $t = 0$, and $Q = Q_1$ at $t = \infty$. This gives

$$E_{\text{C}} = \int_0^{Q_1} v_{\text{C}} \cdot dQ. \tag{5.7}$$

Finally, the energy lost in R is calculated as

$$\begin{aligned} E_{\text{R}} &= \int_0^{\infty} v_{\text{R}} \cdot i \, dt = \int_0^{\infty} (V_{\text{dc}} - v_{\text{C}}) \cdot i \, dt \\ E_{\text{R}} &= \int_0^{\infty} V_{\text{dc}} \cdot i \, dt - \int_0^{\infty} v_{\text{C}} \cdot i \, dt. \end{aligned} \tag{5.8}$$

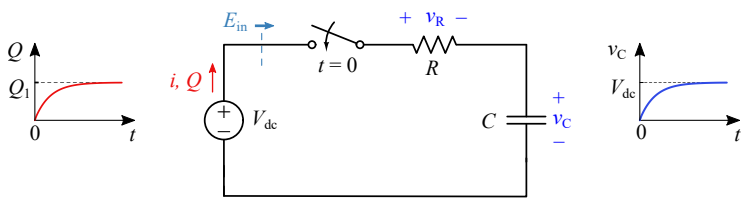


Figure 5.4: An ideal dc voltage source, V_{dc}, charges a capacitance C in series with a resistance R. The circuit is turned ON at $t = 0$. At $t \gg RC$, the charging process is completed with $v_{\text{C}} = V_{\text{dc}}$, and a total charge equal to Q_1 has been supplied by the source that is stored in C.

Identifying that the two integrals on the RHS of Eq. (5.8) are given by Eq. (5.4) and Eq. (5.6), we get

$$E_R = E_{in} - E_C = Q_1 V_{dc} - E_C \tag{5.9}$$

Since $Q_1 V_{dc}$ is the total area in a QV plot, according to Eq. (5.9), E_R can be expressed as

$$E_R = \int_0^{V_{dc}} Q dv_C. \tag{5.10}$$

The integral on the RHS in Eq. (5.10) is defined as the co-energy of C. This shows that the energy loss in R is independent of the value of R and depends only on the QV curve of C.

5.4.2 Simulation Results

Figure 5.5(a) shows a simple circuit where a linear capacitor, C, of 1 nF is charged with a dc voltage source, V_{dc}, in series with a resistor R. At the end of the charging process, C is charged up to a voltage $v_C = V_{dc} = 10$ V, while storing a charge equal to Q. Figure 5.5(b) shows simulation results for the energy distributions in this circuit for the charging process for different values of R. It is observed that irrespective of the value of R, the energy loss in R, E_R, converges to $0.5QV_{dc} = 0.5CV_{dc}^2$. According to Figure 5.3(a), the stored energy and co-energy are each equal to $0.5CV_{dc}^2 = 0.5 \times 1\text{nF} \times 10^2\text{V} = 50$ nJ for this linear capacitor. This shows that E_R is the co-energy loss [see Eq. (5.11)] and that it is independent of the value of R.

$$E_R = E_C^* \tag{5.11}$$

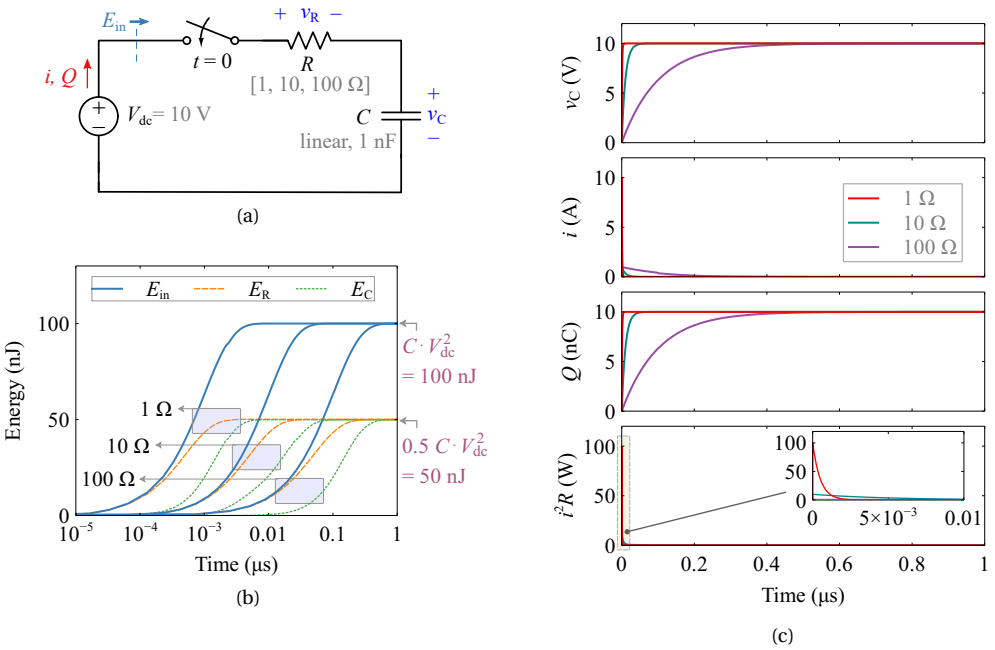


Figure 5.5: (a) Linear capacitor $C = 1$ nF (in series with a resistor, R) is charged by an ideal dc voltage source $V_{dc} = 10$ V. The circuit is simulated in LTspice. The switch is turned ON at $t = 0$. Three cases where $R = 1$, 10 and 100 Ω are considered. (b) Related energy distributions with time. The energy stored in C, lost in R, and supplied by the voltage source are denoted as E_C, E_R, and E_{in}, respectively. (c) Additional time-domain waveforms showing the voltage across the capacitor, v_C; current i that decays down to zero as $t \to \infty$; charge Q flowing through the circuit; and the i^2R loss in the resistance R.

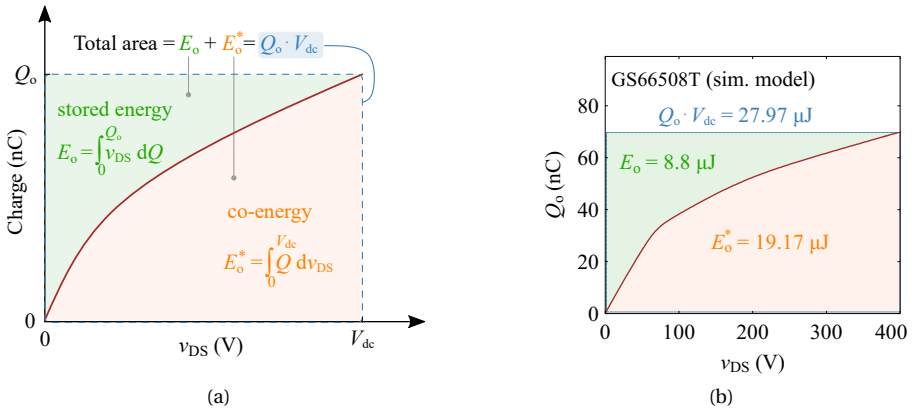


Figure 5.6: (a) Stored energy and co-energy components related to the output capacitance of a FET (which is a nonlinear function of v_{DS}) can be identified on a charge versus voltage (QV) plot: V on *the* x-axis and Q on the y-axis. For a given dc-bias $v_{DS} = V_{DS} = V_{dc}$, the stored energy is taken as the area between Q and the y-axis, whereas co-energy is calculated by taking the area between Q and the x-axis. (b) QV curve of a GaN HEMT (GS66508T) based on the data extracted from the manufacturer simulation model (version 4.0) for LTspice *XVII*.

Figure 5.5(b) also shows that the energy supplied by the source is always $QV_{dc} = CV_{dc}^2$, as expected from Eq. (5.3). Additional time-domain waveforms are shown in Figure 5.5(c). An increase in R results in a reduction in the peak current but increases the duration of the decay of i: in effect, these two behaviours result in a fixed i^2R power loss, or equivalently an energy loss E_R.

A nonlinear capacitor behaves similarly, keeping Eq. (5.3) always true, as seen in Figure 5.3(b). Consider the QV curve shown in Figure 5.6(a) related to the nonlinear C_o of a typical FET. The stored energy component is calculated as

$$E_o = \int_0^{Q_o} v_{DS} \cdot dQ. \tag{5.12}$$

The related co-energy component is given as

$$E_o^* = \int_0^{V_{dc}} Q dv_{DS}. \tag{5.13}$$

An example QV curve of an actual FET model is plotted in Figure 5.6(b); the output capacitance of this FET is charged with a dc voltage source, in series with a resistor R, as shown by Figure 5.7. The energy distributions for the charging process show that irrespective of the value or the time variation of R, both the stored energy (E_o) and the energy loss in R (E_R) converge to fixed values at the end of the transient. More importantly, E_R converges to the co-energy of C_o, E_o^*. The results also show that the energy (E_{in}) supplied by the fixed voltage source is only determined by the product $Q_o V_{dc}$:

$$E_{in} = Q_o V_{dc}. \tag{5.14}$$

This analysis indicates that when a power electronic topology dictates an operating condition where C_o is charged with a fixed voltage source, such as the case presented for $C_{o,S2}$ in Figure 5.1(d), an energy loss equivalent to the co-energy is dissipated in the resistive path, irrespective of the value of resistance; in this regard, the co-energy can be considered as a *charge loss*. If the stored energy is also

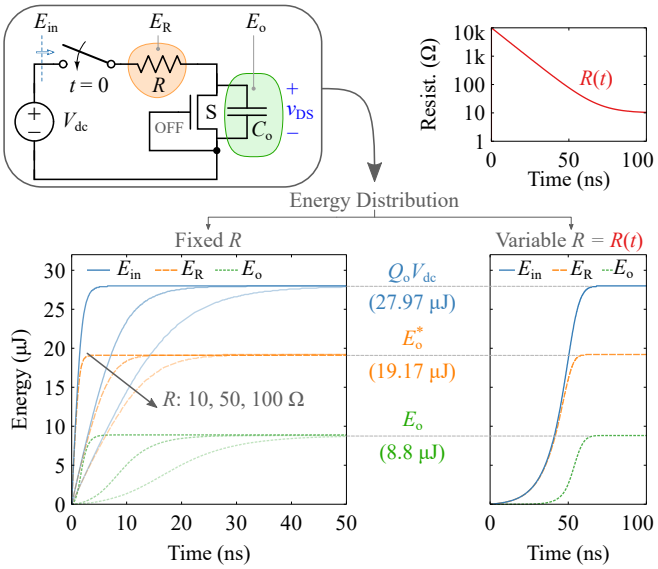


Figure 5.7: GaN HEMT (GS66508T) model, with its gate–source terminals shorted, is put in series with a resistor, R, and an ideal dc voltage source $V_{dc} = 400$ V. The circuit is turned ON at $t = 0$, and C_o of the FET is charged. An LTspice simulation is carried out for five different fixed values of R, as well as for a case where R is made to behave as a time-dependent function $R(t)$. The energy stored in C_o, lost in R, and supplied by the voltage source are denoted as E_C, E_R, and E_{in}, respectively; each component converges to a fixed value irrespective of the value or the time dependence of R.

lost due to hard turn-ON in a subsequent operating mode, then all of E_{in} ($= Q_o V_{dc}$) is completely lost in the circuit. This is the basis of the presented no-load technique (Section 5.6). Note that if either the charging or the discharging of C_o is achieved by a transfer of inductive energy through resonance [46, 84] as in the cases shown in Figures 5.1(e) and 5.1(f), or with an ac voltage source, any related loss is of hysteretic nature.

5.4.3 Historical Background on co-energy and $Q_o V_{dc}$ Loss

The previous analysis showed that the co-energy component creates a *real* energy loss when a capacitor is charged by a fixed dc voltage source [52, 84].[3] While this loss looks quite foreign—and even counter-intuitive—for a power electronic circuit,[4] it is a known topic in switched-capacitor circuits [83, 86], and in the research on optimal charging of capacitors[82, 87].

A profound discussion on the losses associated with the charging and discharging of C_o is presented in an article by Gauen in 1989 [84]. The article specifically addresses and separates charge–discharge losses based on small-signal capacitance curves, with individual attention to the contributions from C_{DS} and C_{DG}. An analytical description of charging and discharging of a nonlinear capacitance using charge-voltage and energy-voltage relationships was presented by Kazimierczuk et al. in the book Resonant Power Converters [88]; the analysis was carried out regarding the operation of a class-D series resonant converter. It was shown that the resistive energy loss in the charging path of the nonlinear capacitance (during the charging process, or equivalently, at the MOSFET turn-OFF transition) is higher than the energy stored in the capacitance, and then lost in the MOSFET ON-resistance during the

[3] It should also be noted that the standard gate-loss equation $P_G = f_{sw} \cdot Q_G \cdot V_{drive}$ is based on the same principle [85].

[4] The observation of the co-energy loss may have been veiled by another apparent discrepancy in conventional loss analysis related to measured and theoretical switching energies: the externally measured $i_{DS} \cdot v_{DS}$ underestimates the turn-ON loss and overestimates the turn-OFF loss [39] (see also Chapter 2). See Section 3.1.5 for additional details.

discharging process of the capacitance (at the turn-ON transition) by a factor of 2.[5] The more recent articles by Miftakhutdinov [20] and Deboy et al. [89] consider the co-energy component as a charge loss and a Q_{oss}-related loss, respectively; the works also describe the product $Q_o V_{dc}$ as the total C_o-related loss for hard switching. The two articles also emphasize the importance of the use of large-signal capacitance curves to estimate these losses, with particular reference to the large-signal anomalies reported by Fedison and Harrison for Si-SJ devices [14]. In relation to a DPT circuit, Jones et al. [77] and Hou et al. [40] analysed the effects of co-energy loss but treated it as a 'Q_{oss} loss mechanism' occurring at the switch-node.

In the domain of soft-switching converters, in 2012, Elferich used the terms 'co-energy'[6] and 'dual energy' to represent the energy associated with the area below a QV curve [Q on the y-axis and V on the x-axis as shown in Figure 5.6(a)] in connection analysis on ZVS transition energy [78]. The ideas were also discussed by the subsequent work by Oeder et al. [79] concerning the estimation of switching losses in resonant converters.

Using energy balance for a switching period in ZVS operation, Kasper et al. showed the product $Q_o V_{dc}$ as the upper limit of partial-ZVS operation, which reflects a fully hard-switched condition [46]. This is the basis for the subsequent works by Azura Anderson et al. [90, 91] and Guacci et al. [92] on the analysis of *minimum* hard-switching losses in bridge and multi-level topologies. The authors employed calorimetric measurements to assess switching losses under both soft- and hard-switching conditions. The test circuits possess a special mode with *zero-current switching*—that is, in fact, a half-bridge operating at no load—that permits the calculation of $Q_o V_{dc}$ loss. Regarding the electrical measurement of C_o-related losses in hard switching, Miftakhutdinov utilized (in 2014[93] and 2017 [20]) a half-bridge circuit without any load to evaluate $Q_o V_{dc}$ loss. However, the details of the circuit operation, measurement technique and its limitations were not discussed.

Although all these research works have addressed either the $Q_o V_{dc}$ loss or the importance of large-signal measurements, a comprehensive synthesis of these ideas with a clear focus on the basic hard-switching operation was missing. In particular, a theoretical explanation as to how the co-energy loss takes place in a simple inverter leg needs to be provided from a circuit perspective. And finally, we believe a comparison of the QV curves based on small-signal and Sawyer–Tower methods to that related to hard switching could bring forth additional insights. We address these considerations in the following sections.

5.4.4 co-energy Component in Switching Circuits

The co-energy component is practically important as a loss in hard-switching circuits, whereas in soft-switching applications it increases the energy requirement of the resonant inductance [46]. These aspects should be considered when a power semiconductor is selected for a given application.

Figure 5.8 compares the distribution of stored energy and co-energy components related to the output capacitances of several commercial devices; the ratio E_o^*/E_o is indicated by red dots. Devices 2–5 have similar levels of stored energies in the range of 7–9 μJ; however, their co-energies are much larger and show significant differences. Among the devices 2–5, device 3 offers the least amount of co-energy, resulting in the lowest $E + E_o^*$. This makes the device also ideal for ZVS applications as it requires the least amount of transition energy [78]. The Si-SJ device (number 5), has the highest E_o^*/E_o

[5] See Chapter 6 (Section 6.7.2) [88].

[6] We prefer the term co-energy as it provides the much-needed distinction for this energy component; the terms charge loss and Q_{oss} loss are often confusing and do not set themselves apart from the stored energy in a meaningful way.

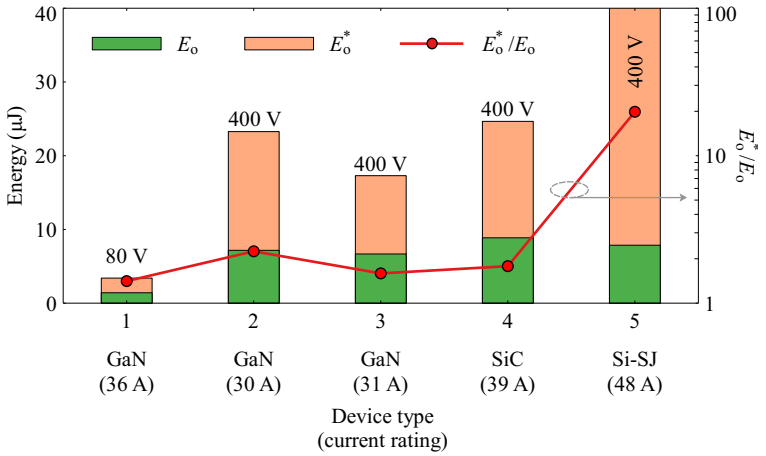


Figure 5.8: Variation of E_o, E_o^*, and the ratio $n_{co} = E_o^*/E_o$ evaluated at the marked voltages, for different commercial field-effect transistors. Device 1 is the DUT in this work, which is a 100-V GaN HEMT. Devices 2–5 are rated for 600–700 V and have similar E_o values. Note that for device 5, the E_o^* portion exceeds the graph limit. The calculations are based on datasheet-provided small-signal C_{oss} curves.

ratio, approximately equal to 20.

5.5 C_o-related Turn-ON Energy Loss in Hard Switching

A standard DPT circuit is shown in Figure 5.9(a). During the turn-ON transition of S_1, first, the load current (I_{dc}) commutation takes place while the switch-node voltage, v_{SW}, is clamped at V_{dc}[40, 41]—see Figure 5.9(b). When the channel current increases up to the load current (i.e., $i_{CH,S1}$ =

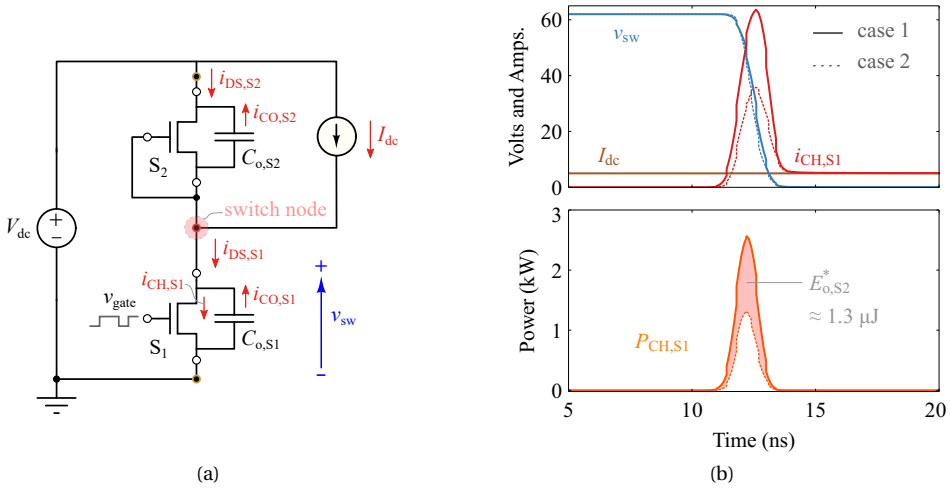


Figure 5.9: (a) In a double-pulse-test (DPT) circuit, switch S_1 (the DUT) experiences a fully hard-switched operation, while the complementary switch S_2 is kept OFF. S_2 is of the same device type as S_1. (b) LTspice simulation results of voltage, channel current and power waveforms of S_1 during its turn-ON transient, where S_1 and S_2 are EPC2001C devices (case 1: solid lines), with V_{dc} = 60 V and I_{dc} = 5 A. The dashed lines (case 2) show the same waveforms when the SPICE model of S_2 is modified to have near-zero output capacitance. *Note*: this modification can be achieved in SPICE by breaking down the device's full sub-circuit model to separate sub-circuit models. The *QV* curve of an EPC2001C device is shown in Figure 5.10(a).

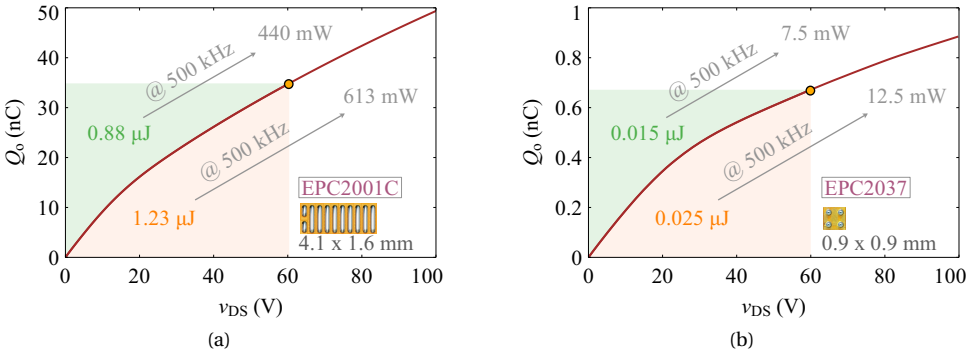


Figure 5.10: *QV* curves of the GaN HEMTs (a) EPC2001C and (b) EPC2037, where E_o and E_o^* values are evaluated at a voltage of V_{dc} = 60 V, using datasheet-provided small-signal capacitance (C_{oss}) curves. The related power dissipations at f_{sw} = 500 kHz are also shown.

I_{dc}), the voltage commutation commences. Since the channel of S_1 is now conducting (although not fully enhanced), its output capacitance ($C_{o,S1}$) discharges through its channel, adding a second current component $i_{CO,S1}$ to the channel [40, 41]. While this self-discharge happens in S_1, the output capacitance of S_2, $C_{o,S2}$, gets charged by the dc voltage source; this causes an additional third current component to pass through the channel of S_1 such that

$$i_{CH,S1} = I_{dc} + i_{CO,S1} + (-i_{CO,S2}). \tag{5.15}$$

It should be noted that for this charging process of $C_{o,S2}$, the channel of S_1 acts as the resistance in series with the dc voltage source.[7]

At the end of the voltage commutation period, two loss components relevant to device capacitances can be identified in the channel of S_1.

1. The first is the discharge loss of $C_{o,S1}$ that is equal to the energy that was stored in $C_{o,S1}$ at OFF state (equal to $E_{o,S1}$).

2. The second is the loss incurred due to the charging of the complementary device's output capacitance that is equal to the co-energy of $C_{o,S2}$, $E^*_{o,S2}$.

Therefore, the total energy loss in S_1 at its turn-ON, due to the charge–discharge processes of device output capacitances, is equal to

$$E_{on\text{-}Co} = E_{o,S1} + E^*_{o,S2}. \tag{5.16}$$

Note that the total turn-ON energy loss in S_1 is given as

$$E_{on} = E_{on\text{-}Co} + E_{on\text{-}VI}, \tag{5.17}$$

where $E_{on\text{-}VI}$ is the energy loss in S_1 due to the load current [40]. And for the case where S_1= S_2, using Eq. (5.14) we deduce that

$$E_{on\text{-}Co} = E_{o,S1} + E^*_{o,S1} = Q_{o,S1}|_{V_{dc}} \cdot V_{dc}. \tag{5.18}$$

[7] Since S_2 is in OFF-state, we can safely assume that any resistance in parallel with $C_{o,S2}$ is infinite and has no effect on the *RC* charging process.

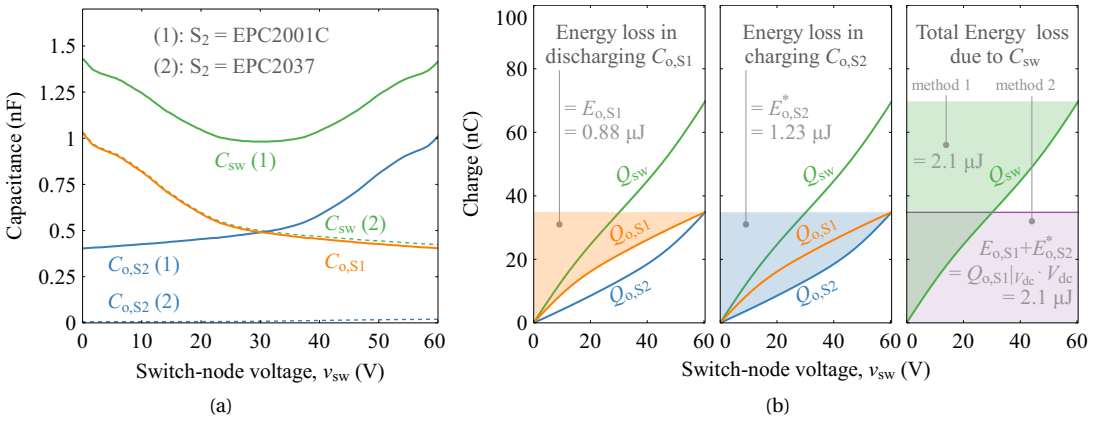


Figure 5.11: Variation of (a) switch-node capacitance, C_{sw}, and (b) switch-node charge, Q_{sw}, during the turn-ON process of a fully hard-switched bottom switch S_1 of an inverter leg with V_{dc} = 60 V. The capacitance and charge variations are equally valid for the DPT circuit and the proposed no-load circuit. In sub-figure (a), the solid lines show the case where both S_1 and S_2 are EPC2001C devices, while the dashed curves show the case when S_2 is an EPC2037 device, which has a negligible C_o value compared to an EPC2001C device. Sub-figure (b) considers S_1= S_2 case only.

The simulation results in Figure 5.9(b) show the significant influence of capacitive co-energy on the turn-ON loss by considering two cases for S_2. Case 1 considers the normal circuit: $C_{o,S2} = C_{o,S1}$ (shown with solid lines). Case 2 considers the circuit operation when $C_{o,S2} \approx 0$, which makes the co-energy loss component in Eq. (5.16) equal to zero (i.e., $E^*_{o,S2} \approx 0$). By going from case 2 to case 1, $E_{on\text{-}Co}$ of S_1 increases by an amount $E^*_{o,S1} \approx 1.3\ \mu$J, which lies in close range to the analytically obtained co-energy of 1.23 μJ in Figure 5.10. In terms of power, this translates to a non-negligible loss of about 0.6 W at a switching frequency f_{sw} = 500 kHz.

It needs to be pointed out that Hou et al. [40] investigated this additional component of turn-ON loss (on a hard-switched device) due to the charging of the complementary device's output capacitance, and coined the term E_{qoss} *loss mechanism*. However, its basic relation to the co-energy (i.e., $E_{qoss} = E^*_{o,S2}$), was not identified. Moreover, the evaluation of E_{qoss} in the reported works uses a different approach (and rather complicated), where a total switch-node capacitance (C_{sw}) is first evaluated [40, 77], as shown in Figure 5.11(a). This is then followed by the calculation of a total switch-node charge, Q_{sw}, also known as the *displacement charge* [77], as shown in Figure 5.11(b). Finally, $E_{on\text{-}Co}$ is calculated as the energy loss that occurs when Q_{sw} is discharged as v_{sw} changes from V_{dc} to 0 V as S_1 turns ON—marked as method 1 in Figure 5.11(b). However, it can also be seen that this loss is exactly equal to $E_{o,S1} + E^*_{o,S2}$ (marked as method 2).

One of the main messages of this analysis on the DPT circuit is that during the turn-ON of S_1, the capacitance $C_{o,S2}$, the channel resistance of S_1 and the dc voltage source resemble the simple *RC* charging process discussed in Section 5.4, and hence the occurrence of a co-energy related loss in the switching device's channel. For such scenarios, the following conclusions can be made for a fully hard-switched device:

- During its turn-ON process, a total energy loss equal to $E_{on\text{-}Co} = E_{o,S1} + E^*_{o,S2}$ occurs in the device channel due to discharging of $C_{o,S1}$ and charging of $C_{o,S2}$.
- The co-energy loss component causes a significant power loss in the device during its turn-ON.
- $E_{on\text{-}Co}$ depends only on dc-link/bus voltage and the related Q value; it does not depend on the

particulars of the pattern of the *QV* curve.

It should also be noted that the relationship $E^*_{o,S1} > E_{o,S1}$ (i.e., $n_{co} > 1$) generally holds for all FETs because the output capacitances of FETs are monotonically decreasing functions of v_{DS}. For the case of $S_1 = S_2$, it could be further said that $E_{on\text{-}Co}$ is independent of the ratio n_{co}.

5.6 The No-Load Concept

In this section, we focus our attention on the turn-ON energy under a zero load-current condition (i.e., a *no-load condition*). Based on the concepts that were developed in the previous sections, a new method to evaluate the co-energy related loss in a hard-switched device is presented, followed by experimental validation of the concepts.

Although the standard DPT circuit subjects the DUT to a co-energy related loss, the existence of the load current complicates the power measurement process as the DUT also experiences a conduction loss, P_{con} as well as a *VI*-overlap loss. Decoupling these from $E_{on\text{-}Co}$-related power loss is difficult: for electrical measurements, this is especially challenging at high frequencies, where the current measurements are prone to high inaccuracies [22]; on the other hand, basic thermal measurements do not allow decoupling of the losses in the DUT. Furthermore, the standard DPT circuit does not allow to experimentally differentiate between the co-energy loss $E^*_{o,S1}$ and the discharge loss $E_{o,S1}$.

The proposed no-load circuit is shown in Figure 5.12: the circuit is similar to the DPT circuit, however, without the existence of a load current. This effectively decouples and removes the effects of the load current and duty ratio on the losses: P_{con} and *VI*-overlap losses are non-existent. Thus, the losses in the circuit are solely caused by the charging and discharging processes related to the device output capacitances.[8]

5.6.1 Operation of the No-load Circuit

Consider the no-load circuit shown in Figure 5.12. The switch node is left floating, involving zero load-current. The two switches S_1 and S_2 are switched complementarily with a chosen dead-time, T_{dead}, and subjected to a dc-link voltage of V_{dc}. The channel, drain, and output-capacitance currents are also shown. The operation of the circuit can be analysed through six operating modes as Figure 5.13 illustrates, where important waveforms during switching transitions are given in Figure 5.14. Throughout this work, the following is maintained for the external gate-driver resistor values:

- $R_{GH1} = R_{GH2}$ and is denoted by the general term R_{GH}.
- $R_{GL1} = R_{GL2}$ and is denoted by the general term R_{GL}.

During the turn-ON transition of S_1 (t_1–t_2 in Figure 5.13), no current commutations take place as there is zero load current. Therefore, as soon as v_{GS} approaches $V_{GS(th)}$, the voltage commutation commences unlike in a DPT circuit. Since the channel of S_1 is now conducting (although not fully enhanced), its output capacitance $C_{o,S1}$ discharges through its channel, adding a current component $i_{CO,S1}$ to the channel. While this self-discharge happens in S_1, the output capacitance of S_2, $C_{o,S2}$, gets charged by the dc voltage source; this causes an additional second current component to pass through

[8] The effect of gate drive losses can be neglected at the considered switching frequencies.

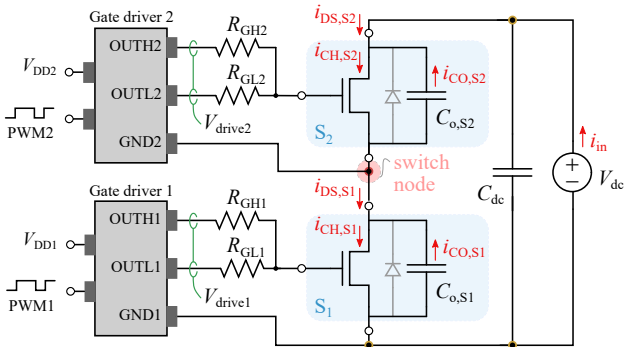


Figure 5.12: The no-load topology consists of a half-bridge circuit where the bottom and top devices (S_1 and S_2) are switched complementarily using an asymmetrical gate-driving configuration. A dc-link capacitance C_{dc} is placed very close to the switching devices. C_o of each device is represented as a capacitance in parallel with drain–source terminals. Any third-quadrant operation (denoted by the diodes) is inhibited due to the non-existence of any load current at the switch node.

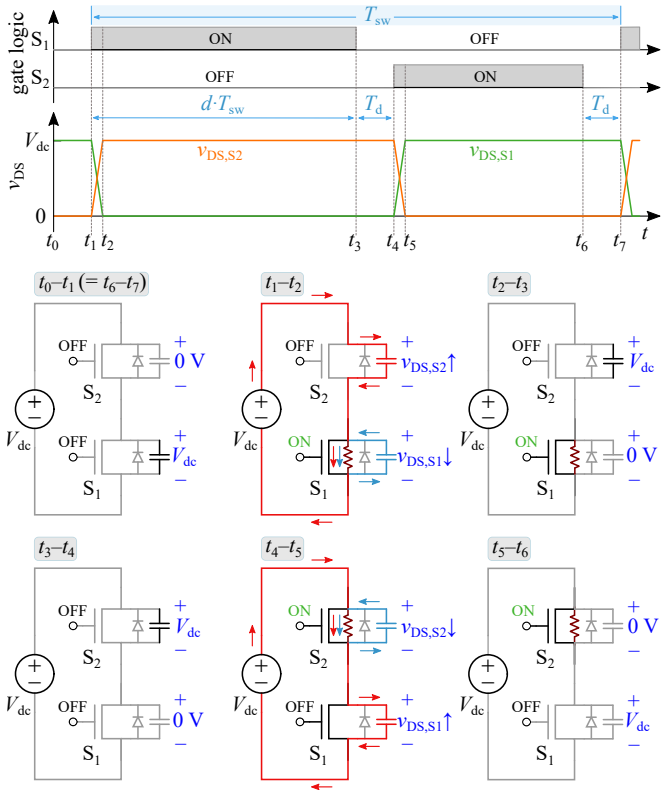


Figure 5.13: Operation of the no-load circuit can be divided into six modes, where $T_{sw} = 1/f_{sw}$ is the switching period, T_d is the dead-time and d is the duty ratio. During the dead-times (t_0–t_1 and t_3–t_4), and as well during the ON-periods (t_2–t_3 for S_1 and t_5–t_6 for S_2), no charge or discharge process related to output capacitances occurs; such a process would only take place during switching transitions. During t_1–t_2, $C_{o,S1}$ gets discharged while $C_{o,S2}$ gets charged; during t_4–t_5, $C_{o,S1}$ gets charged while $C_{o,S2}$ gets discharged; for the two charging processes, V_{dc} acts as the energy source.

the channel of S_1 such that $i_{CH,S1} = i_{CO,S1} + (-i_{CO,S2})$ (see Figure 5.14). For this charging process of $C_{o,S2}$, the channel of S_1 acts as a resistance (variable in nature as both Figures 5.1(a) and 5.7 describe) in series with the dc voltage source; thus this loss is independent of the value or nature of R_{ch}.

At the end of the voltage commutation period, two loss components are identified in the channel

of S_1, which are caused solely due to device capacitances. The first is the discharge loss of $C_{o,S1}$ that is equal to the energy that was stored in $C_{o,S1}$ at OFF-state (equal to $E_{o,S1}$). The second is the loss incurred due to the charging of the output capacitance of the complementary device ($C_{o,S2}$) that is equal to the co-energy of $C_{o,S2}$, $E^*_{o,S2}$. Thus, the total energy loss in S_1 at its turn-ON transition in the no-load circuit—due to the charging and discharging of device output capacitances—is equal to

$$E_{\text{on-C}_o\text{(NL)}} = E_{o,S1} + E^*_{o,S2}. \tag{5.19}$$

And for the case where $S_1 = S_2$, which is the typical case in half-bridge configurations, Equations 5.14 and 5.19 give

$$E_{\text{on-C}_o\text{(NL)}} = E_o + E^*_o = Q_o V_{dc}. \tag{5.20}$$

The same analysis can be carried out for the turn-ON transition of S_2 (t_4–t_5 in Figure 5.13).

As Figure 5.13 illustrates, all the other operating modes in the circuit are inactive modes.[9] They do not involve any charge–discharge processes of C_o, and therefore, assume no change in v_{DS}, as Figure 5.14 indicates. Thus, the total energy

$$E_{in(NL)} = 2\, Q_o V_{dc} \tag{5.21}$$

drawn from the dc voltage source in each switching cycle is completely dissipated as heat. It is important to note that during practical operation, the dc-link capacitance C_{dc} acts as the dc voltage source that supplies the energy ($E_{\text{on-C}_o\text{(NL)}}$) required for a single switching transition. C_{dc} then gets charged by the external voltage source before the next switching transition takes place; this process however involves negligible energy loss. This is because the voltage drop caused by the extraction of an amount of charge equal to Q_o is insignificant as C_{dc} is very large.

The above analysis shows that the input energy in the no-load circuit is independent of the following.

1. Value or time variations of R_{ch}, and hence, also any dynamic $R_{DS(on)}$ degradation related to WBG devices.

2. Dead-time and duty ratio, as any transfer of energy takes place only during voltage-commutation periods.

3. Switching frequency, as long as Q_o does not show any frequency dependence [23].

Moreover, $E_{in(NL)}$ is not affected by any C_o-hysteresis as it is determined by the final Q_o value.

5.6.2 Experimental Demonstration of the co-energy Component

Here, we experimentally demonstrate the existence of the co-energy loss component related to device output capacitance using a thermal loss estimation method [52]. Using the same thermal technique, in Section 5.7, we verify the electrical measurements used in the proposed *QV* measurement technique as well.

[9] Note: during the dead times, the topology does not allow any transfer of charge, and thus, only one device holds off the dc-link voltage. The reasons are as follows: 1) as the circuit involves no load-current, any external charging or discharging does not take place through the switch node; 2) the input supply V_{dc}, for example during t_3–t_4, cannot charge $C_{o,S1}$, as $C_{o,S2}$ is holding a voltage equal to V_{dc}, not allowing a charging current to commence.

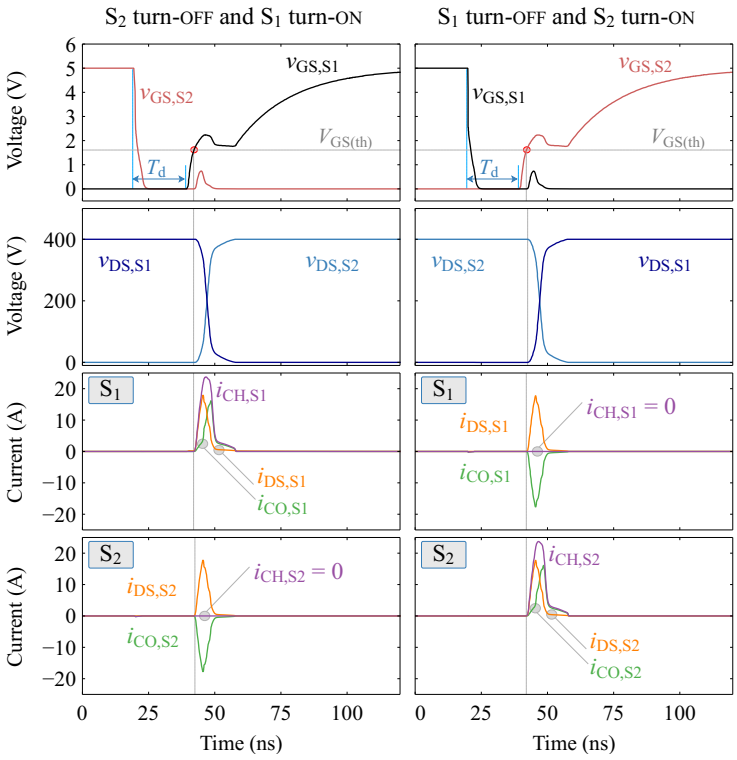


Figure 5.14: LTspice simulation results showing the turn-ON and turn-OFF transitions of S_1 and S_2 in the no-load circuit, where $V_{dc} = 400$ V, $f_{sw} = 100$ kHz, $d = 0.5$, $T_d = 20$ ns, $R_{GH} = 20\,\Omega$ and $R_{GL} = 0.1\,\Omega$. S_1 and S_2 are GS66508T GaN HEMT models. During the dead-times, the voltages $v_{DS,S1}$ and $v_{DS,S2}$ stay at their before-dead-time values as there is no load current to charge or discharge the switch-node capacitance. When a device turns ON, it experiences a channel current larger than its drain current due to the discharge of its output capacitance; the already-OFF device experiences zero current in its channel.

5.6.2.1 Concept

A special device selection in the no-load circuit is used to verify the co-energy concept. For a given device S_1, we separately evaluate its $E^*_{o,S1}$ and $E_{o,S1}$ components by selecting S_2 such that

$$Q_{o,S2}|_{V_{dc}} \ll Q_{o,S1}|_{V_{dc}}.$$

Two GaN HEMTs were selected where S_1 is an EPC2001C device with $Q_{o,S1}|_{60\,V} = 35$ nC and S_2 is an EPC2037 $Q_{o,S2}|_{60\,V} = 0.66$ nC—see Figure 5.10. In other words, $C_{o,S2}$ has negligible influence on the switch-node capacitance, which is now dominated by $C_{o,S1}$ as shown by the dashed green line in Figure 5.11(a). Therefore, it can be assumed that $E_{o,S2} = E^*_{o,S2} \approx 0$. This means that the loss in S_1 is only caused by $E_{o,S1}$ and the loss in S_2 is only caused by $E^*_{o,S1}$. This in effect makes S_1 and S_2 two physically-separate heat sources that are representative of $E_{o,S1}$ and $E^*_{o,S1}$, respectively. Thus, thermal loss estimation becomes a viable option to decouple the two loss components. Graphical representations of the two localized losses in the two switches are given in Figures 5.15(a) and 5.15(b).

The circuit operation is first verified by the simulation results shown in Figure 5.16: the solid curves correspond to Case 1, where both S_1 and S_2 are EPC2001C devices; the dashed curves represent Case 2, where S_2 is changed to an EPC2037 device. Consider Case 2. During the turn-ON of S_2, the channel current of S_2 charges $C_{o,S1}$ while $i_{CO,2} \approx 0$, indicating that $E_{o,S2} \approx 0$. During the turn-ON of S_1, $i_{DS,S1} \approx 0$ indicating that $E^*_{o,S2} \approx 0$. The significant slowing down of the drain–source voltage transient is caused by

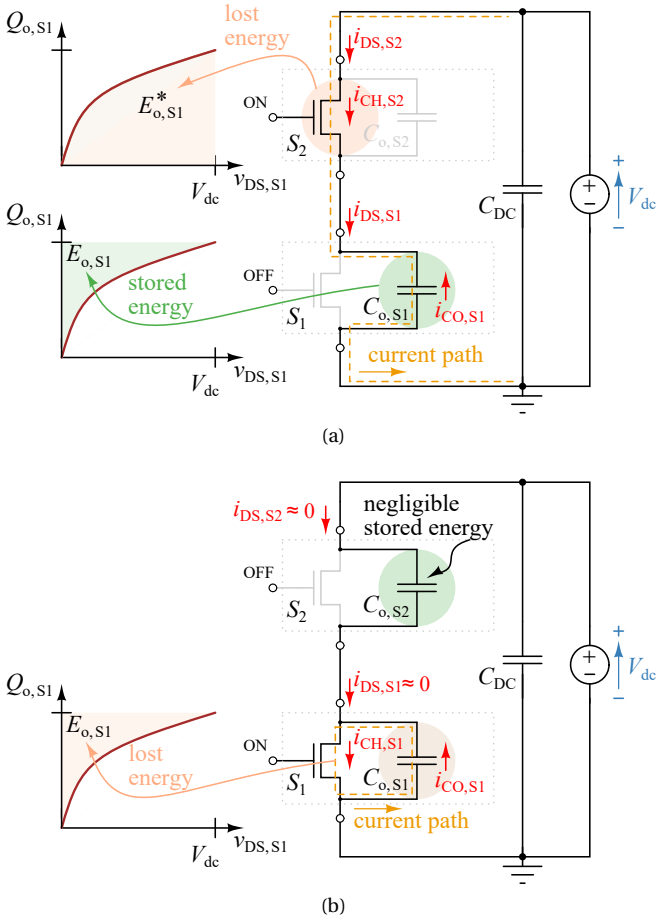


Figure 5.15: (a) During the turn-ON transient of S_2, $C_{o,S1}$ stores an amount of energy equal to $E_{o,S1}$ and causes an energy loss equal to its co-energy ($E^*_{o,S1}$) in S_2. (b) During the turn-ON transient of S_1, it discharges its previously-stored energy $E_{o,S1}$ through its channel, causing an energy loss on itself. Note: any loss due to the discharge of energy stored in $C_{o,S2}$ is insignificant as $Q_{o,S2}|_{V_{dc}}$ is negligible.

the much larger channel resistance of the chosen S_2 device ($R_{DS(on),S2}$ = 550 mΩ, whereas $R_{DS(on),S1}$ = 7 mΩ).

Looking at Case 1, it can be also observed that device S_1 experiences an $E_{on\text{-}Co}$ of 2.1 μJ, agreeing with the results from Figure 5.11(b). For this case, the turn-ON transient of S_2 is identical to that of S_1, showing an $E_{on\text{-}Co}$ of 2.1 μJ. It should be noted that in the DPT circuit, the turn-ON transient of S_2 is quite different as the load current forces S_2 to a ZVS or partial ZVS turn-ON.

5.6.2.2 Design and Results

The experimental system shown in Figure 5.17 was developed to demonstrate the co-energy loss concept. To overcome the limitations of electrical measurements at high f_{sw}(specifically the instantaneous currents), here a thermal loss evaluation technique with accurate emissivity correction was devised using a Quantum Focus Instrument (QFI) IR microscope. A dc axial fan with an airflow rate of 13.8 CFM was used, alongside a wind tunnel [as shown in Figure 5.17(b)] to improve the linearity of surface temperature rise versus power (ΔT versus P) curves. The ambient temperature was measured

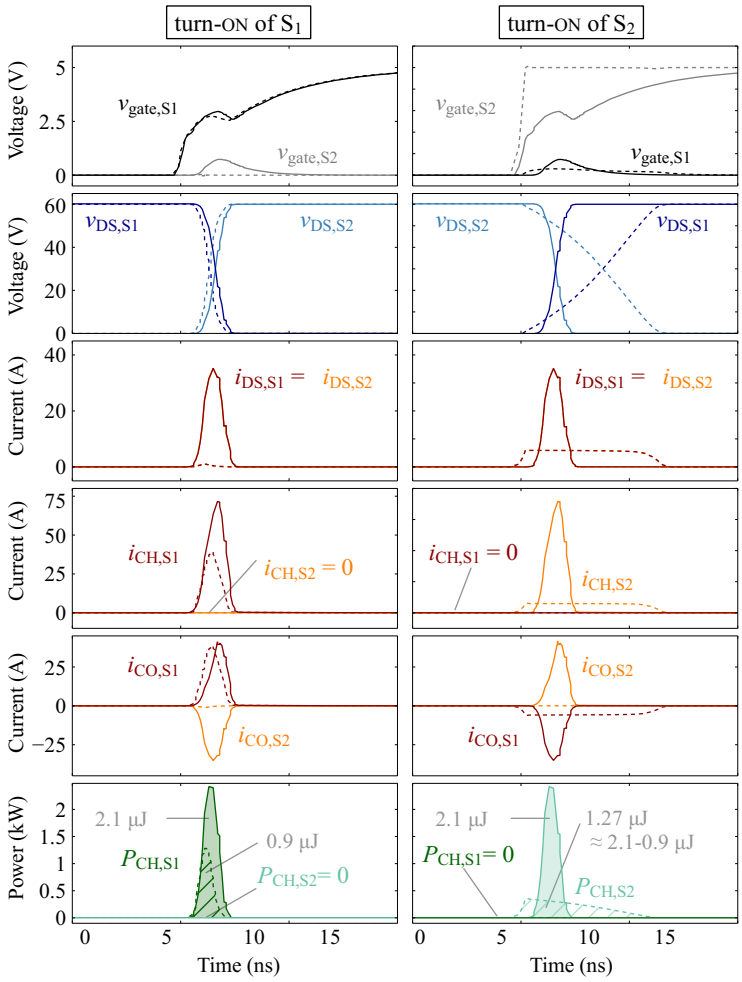
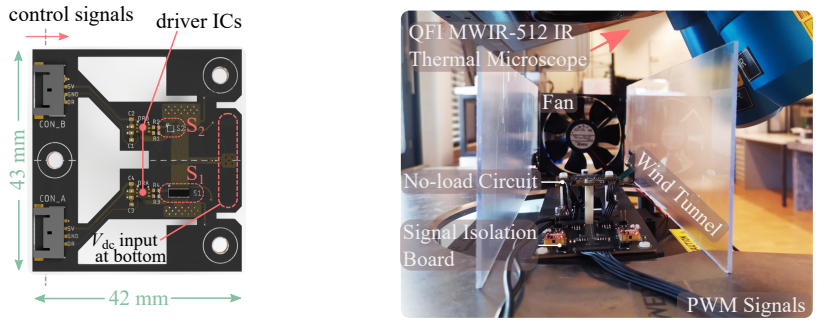


Figure 5.16: LTspice simulation results showing the turn-ON transients of S_1 and S_2, where $V_{dc} = 60$ V, $f_{sw} = 500$ kHz, duty = 0.5, $T_{dead} = 50$ ns, $R_{G1H} = R_{G2H} = 1\ \Omega$. The solid lines show Case 1, where both S_1 and S_2 are EPC2001C devices, while the dashed curves show Case 2, where S_2 is an EPC2037 device that has a negligible C_o value compared to an EPC2001C device. Note: for the turn-OFF gate paths $R_{G1L} = R_{G2L} = 0.2\ \Omega$ was used to avoid convergence problems in simulations. During the dead-times, the voltages $V_{DS,S1}$ and $V_{DS,S2}$ stay at their before-dead-time values as there is no load current to charge or discharge the switch-node capacitance. Therefore, the circuit is practically inactive during the dead time as can be seen in all the waveforms when $t < 5$ ns.

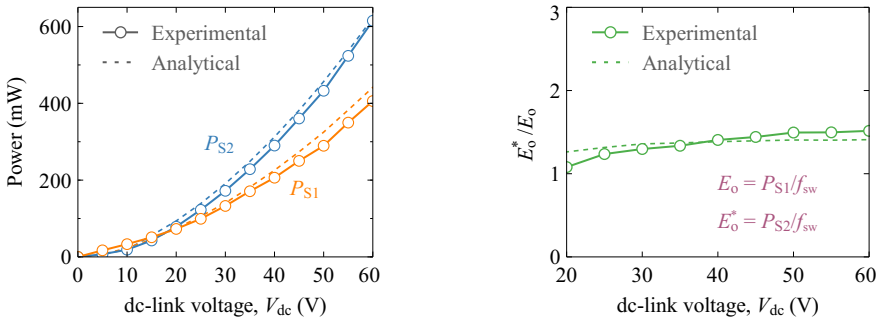
to correct for any environmental changes during the experiment.

First, a dc calibration was performed on the power circuit for each of the devices S_1 and S_2. Since they are in close proximity, the spreading of heat through the PCB should be taken into consideration by measuring the temperature rise of both devices. To calibrate the device S_1, a known dc current I_0 was passed through it. At thermal steady state, the dc voltage drop across the device S_1, $V_{DS,S1}$, and the surface temperature rise of the two devices were accurately measured. In this case, S_1 acts as the heat source with a power $P_{S1} = V_{DS,S1} \cdot I_0$, while S_2 sources zero heat ($P_{S2} = 0$). Different I_0 values were used to obtain power dissipations up to 1 W. Similarly, a second calibration was performed for the case where S_2 is the only heat-dissipating source ($P_{S2} \neq 0$ and $P_{S1} = 0$). Because high linearity in the ΔT versus P curves was obtained for the calibration process ($R^2 > 0.997$), a linear fit could be used to determine a matrix of thermal resistances considering the thermal crosstalk between the devices, as given in Eq. (5.22). Eq. (5.23) gives the values of the thermal resistances. For the normal switching



(a) (b)

Figure 5.17: (a) A 3-d render of the designed no-load circuit with symmetrical layout and (b) the experimental test setup showing the test circuit, wind tunnel and Quantum Focus Instrument (QFI) IR microscope.



(a) (b)

Figure 5.18: Experimental results showing (a) the dissipated power versus dc-link voltage, and (b) the ratio $n_{co} = E_o^*/E_o$. The analytical results are based on datasheet-provided small-signal C_{oss} curves. P_{S1} and P_{S2} are power dissipations in the switches S_1 and S_2, respectively. Conditions: V_{dc} = 5–60 V, f_{sw} = 500 kHz, duty = 0.5, T_{dead} = 25 ns.

operation, the inverse of this matrix was then used to calculate the power losses in each device based on ΔT values.

$$\begin{bmatrix} \Delta T_{S1} \\ \Delta T_{S2} \end{bmatrix} = \begin{bmatrix} \alpha_{11} & \alpha_{12} \\ \alpha_{21} & \alpha_{22} \end{bmatrix} \begin{bmatrix} P_{S1} \\ P_{S2} \end{bmatrix} \tag{5.22}$$

$$\begin{aligned} \alpha_{11} &= 48.96\ \text{K/W} \quad \alpha_{12} = 9.31\ \text{K/W} \\ \alpha_{21} &= 8.14\ \text{K/W} \quad \alpha_{22} = 81.45\ \text{K/W} \end{aligned} \tag{5.23}$$

To obtain the C_o-related losses, the circuit was switched at f_{sw} = 500 kHz and subjected to a sweep of different dc-link voltages from 0 to 60 V at 5 V intervals. The increase in temperature of both devices was measured under steady-state conditions, and the power loss in each device was calculated. The results are plotted in Figure 5.18(a). A good agreement between the analytical (based on datasheets) and experimental results can be observed. The non-zero power loss in S_2 confirms the losses related to the co-energy of S_1. The observation that $P_{S2} > P_{S1}$ states that $E_o^* > E_o$ for S_1. This further justifies the separation of E_o^* and E_o by the proposed method. Furthermore, the results in Figure 5.18(b) show that the ratio E_o^*/E_o is captured well with the proposed circuit.

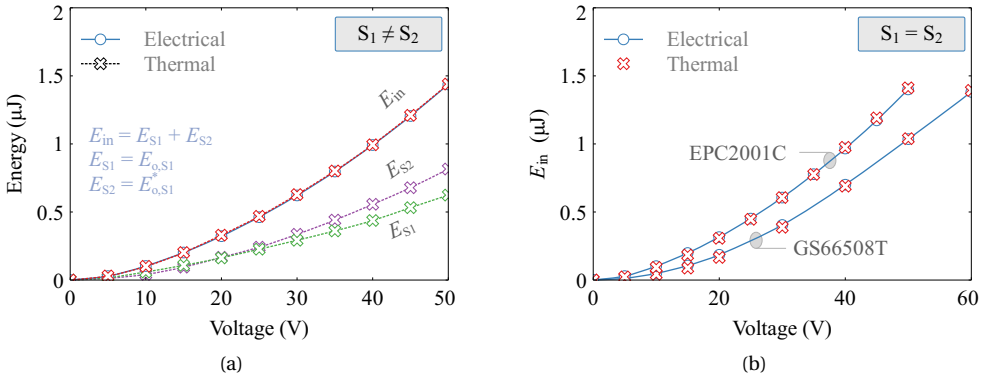


Figure 5.19: (a) Experimental verification of the presented concepts with thermal loss measurements. The energies dissipated in S_1 and S_2 in the no-load circuit are denoted as E_{S1} and E_{S2}, respectively. Here, S_1 is an EPC2001C GaN HEMT; and S_2 is an EPC2037 GaN HEMT, which has negligible C_o compared to an EPC2001C device, making $E_{o,S2} = E^*_{o,S2} \approx 0$. Thus, E_{S1} represents the stored energy in $C_{o,S1}$, whereas E_{S2} represents the co-energy of $C_{o,S1}$. Conditions: $R_{GH} = R_{GL} = 1.1\,\Omega$, $f_{sw} = 500$ kHz, $T_d = 40$ ns. The addition of thermally measured E_{S1} and E_{S2} agree well with electrically measured total input energy, E_{in}, validating the presented concepts. (b) Thermal validation for the case of $S_1 = S_2$, which is the basis for the proposed *QV* measurement method: one half-bridge is made with EPC2001C devices while the other is made with GS66508T devices. Conditions: $R_{GH} = R_{GL} = 2.2\,\Omega$, $f_{sw} = 500$ kHz and $T_d = 40$ ns.

5.7 Generation of *QV* Curves for Hard Switching

In Section 5.6.2, we utilized a thermal technique to separately evaluate the co-energy and stored energy components. However, as the C_o-related turn-ON energy is defined by the product $Q_o V_{dc}$ in hard switching, the combined value $E_o + E^*_o$ is satisfactory for device characterization purposes. To evaluate this, here we present an easy-to-implement technique based on the measurement of *average* electrical input-power P_{in} going into the no-load circuit, presented in Figure 5.12. The circuit is arranged such that $S_1 = S_2$ and duty ratio = 0.5. The input energy E_{in} is then calculated as

$$E_{in} = P_{in} / f_{sw}. \tag{5.24}$$

First, we validate this approach with the thermal loss-estimation method developed in Section 5.6.2. Figure 5.19(a) indicates that for the same circuit (S_1: EPC2001C and S2: EPC2037), the electrically measured E_{in} shows very good agreement with the total input energy calculated based on thermal measurements ($= E_{S1} + E_{S2}$), thus validating the accuracy of the electrical measurements. Results for two no-load circuits for the case where $S_1 = S_2$ are shown in Figure 5.19(b); the thermal and electrical results show excellent agreement. Therefore, using Equations 5.21 and 5.24, we obtain that

$$P_{in} = E_{in} \cdot f_{sw} = 2\, Q_o V_{dc} \cdot f_{sw}. \tag{5.25}$$

Thus, the *QV* curve of a device is obtained by calculating Q_o at each sweep-step of V_{dc} as

$$Q_o = \frac{1}{2} \frac{P_{in}}{V_{dc} f_{sw}}. \tag{5.26}$$

Note that Eq. (5.26) is valid for the case where $S_1 = S_2$, which is the typical case for inverter legs.

Figure 5.20 shows the experimental system with measurement equipment, the control unit and one of the no-load circuits. A *MAGNA Power* TSD800-18/380 power supply was used to supply dc-link

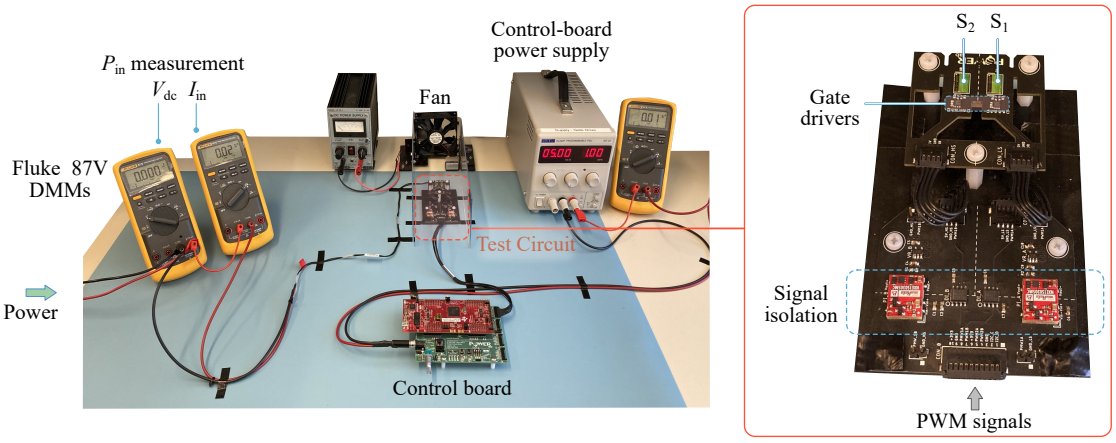


Figure 5.20: Experimental test system with electrical-measurement units. The gate-driver supply voltages and the PWM signals for the high- and low-sides were isolated using two dc–dc converters and two digital-signal-isolators.

voltages up to 400 V. The dc-link capacitance was 2.2 μF. The average input current I_{in} and voltage are measured using Fluke 87V digital multimeters (DMMs).

5.7.1 Use of Asymmetrical Gate-Driving

In our no-load circuit, we utilize an asymmetrical gate-driving approach (more details on gate-driving approaches are discussed in Chapter 6). This is extremely important, especially for GaN devices when R_{GH} values of 10 Ω or lower are used. The low Q_G of GaN devices and low R_{GH} values create very large dv_{DS}/dt values for the device that turns ON. This could eventually cause a false triggering (partial turn-ON event) in the OFF-state device, which results in a cross-conduction in the inverter leg.[10] As Figure 5.21 shows, such a condition causes for observations where $E_{on\text{-}C_o} > Q_o V_{dc}$: the increased switching energy observed by Guacci et al. [92] for a 200-V Si device in zero-current operation is due to this reason. An asymmetrical gate-driver and a very low R_{GL} value are required to keep the OFF-state device's gate-voltage spikes below $V_{GS(th)}$. In all our experiments that follow, this was achieved by using

[10]The spikes in the gate voltage $v_{GS,S2}$ observed in Figure 5.29 are due to this high dv_{DS}/dt condition and can be seen to reduce with increasing R_{GH}.

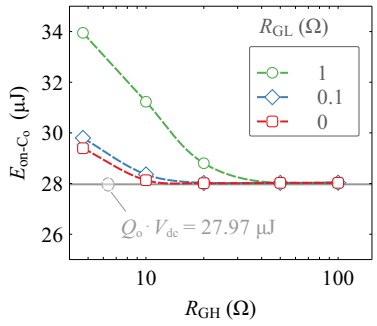


Figure 5.21: Simulation results for device GaN-2 showing how $E_{on\text{-}C_o}$ could deviate from expected values due to the cross-conduction events resulting from the false triggering of the OFF device. The lower the value of R_{GH}, the greater the dv_{DS}/dt value, increasing the current due to the Miller effect. By using an asymmetrical gate driver with low R_{GL} values, this could generally be solved. The reason $E_{on\text{-}C_o} > Q_o V_{dc}$ for $R_{GH} < 10$ and $R_{GL} = 0$ is the internal-gate-terminal resistance (= 1 Ω) used in the device simulation model.

Table 5.1: Evaluated Devices

Label	Part Number	Voltage (V)	Current Rating (A) @ T_C = 25 °C
GaN-1	TPH3212PS	650	27
GaN-2	GS66508T	650	30
SiC-1	MSC060SMA070B	700	39
SiC-2	C3M0065090D	900	36
Si-1	STW38N65M5	650	30
Si-2	NTHL110N65S3F	650	30

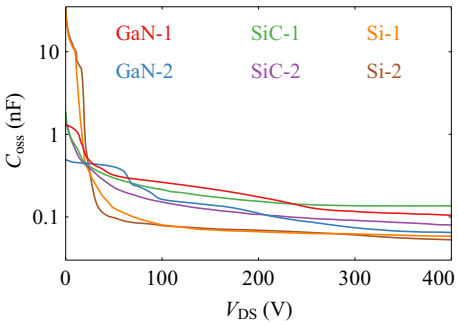


Figure 5.22: Variation of small-signal output capacitance, C_{oss}, with V_{DS} for the commercial power FETs tested in this study. The FETs have a current rating in the vicinity of 30 A (see Table 5.1 for details). The data is extracted from datasheet curves.

an R_{GL} of 1 Ω. Although Figure 5.21 suggests using $R_{GL} \leq 0.1$ Ω, 1 Ω was low enough due to the current limit of the gate diver that inhibited high dv_{DS}/dt conditions. Also, the minimum value of T_d is limited by the value of R_{GL}; T_d should be large enough to fully accommodate the turn-OFF transients of v_{GS}.

5.8 Output-Capacitance Losses in Hard-Switching Circuits

Here we apply the measurement method developed in Section 5.7 to compare commercial GaN, SiC, Si devices with similar voltage and current ratings. The selected devices are listed in Table 5.1 and the corresponding C_{oss} curves from their datasheets are plotted in Figure 5.22. The obtained QV curves are shown in Figures 5.23, 5.24 and 5.26, respectively. The datasheet-based curves (marked by solid black lines) were obtained by integrating C_{oss} with v_{DS}. The Sawyer–Tower measurements (marked by red and blue dashed lines for charge and discharge processes) were performed at an excitation frequency of 100 kHz and a peak voltage (V_p) of 400 V.

The hard-switching results for the two GaN devices closely follow the datasheet values (with a maximum deviation of 9% for GaN-2 device for 100 < V_{dc} < 200 V). The Sawyer–Tower curves also exhibit good agreement up to 300 V but tend to deviate moderately beyond that. Sawyer–Tower results for device GaN-1 from a previous research work have shown that the hysteresis pattern emerges suddenly after V_p > 100–150 V [23], when different V_p values were tested; in Figure 5.23(a), the hard-switching curves do not show any abrupt deviation in its trend above 100 V, affirming that $E_{in(NL)}$ depends only on the final Q_o value and that C_o-hysteresis does not affect it. The tests were repeated using different samples of the devices,[11] and the results (marked by additional circles on the two plots in Figure 5.23) further confirm the validity of the measurements.

[11] The variation between the results for different pairs (2x of GaN-1 and 3x of GaN-2) of samples is not significant and is around 2–5% for the whole range of V_{dc}. The slight differences are due to the small variations in device properties between different samples of the same product, as small-signal measurements in Figure 5.27 indicate.

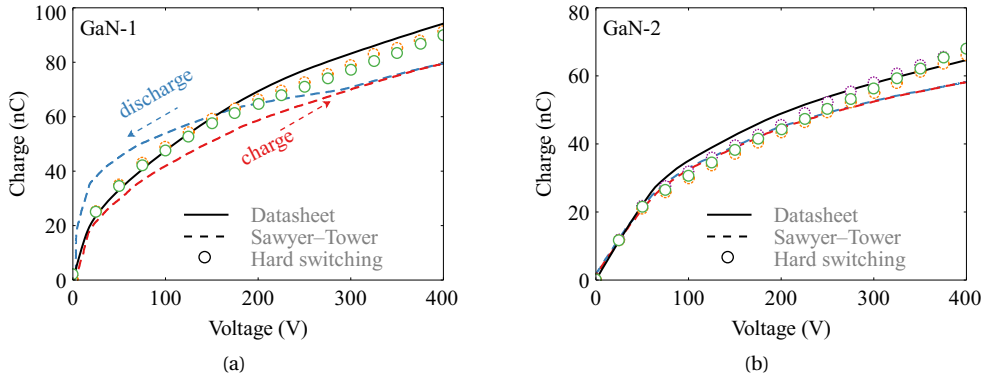


Figure 5.23: Experimental *QV* curves (marked by circles) of two different GaN HEMT device types obtained using the proposed hard-switching method, where f_{sw} = 100 kHz, d = 0.5 and T_d = 100 ns. The results are also compared with curves based on the datasheets and Sawyer–Tower method. To show that the results are repeatable, a device-sampling was carried out for (a) two pairs (solid and dashed circles) of GaN-1 devices with $R_{GH} = R_{GL}$ = 47 Ω, and (b) three pairs (solid, dashed, and dotted circles) of GaN-2 devices with R_{GH} = 10 Ω and R_{GL} = 1 Ω. For both device types, the results for hard-switching follow the datasheet-based values quite closely.

Results for the two SiC devices (Figure 5.24) indicate that the Q_o values in hard switching are considerably different in comparison with the datasheet values. Although the Sawyer–Tower measurements agree well with the datasheet curve for device SiC-2, it is not the case for device SiC-1. This shows that neither the small-signal curves nor the large-signal soft-switching curves can correctly predict the actual charge capacity for hard switching. To understand if this difference is due to any high-frequency effects, as hard switching is achieved at large dv/dt values, the switching speed was decreased for device SiC-2 by increasing the R_{GH} value up to two orders magnitude as Figure 5.24(b) shows. The corresponding v_{DS} waveforms are given in Figure 5.25, where the slowest speed (for R_{GH} = 4.3 kΩ) corresponds to charge and discharge times of ≈ 5 μs each, which matches in frequency for a 100-kHz excitation in the Sawyer–Tower circuit. The results indicate that Q_o stays unchanged with switching speed. One possible explanation of this could lie in the topological difference between hard-switching and Sawyer–Tower circuits. In the former, C_o is allowed a prolonged fully-OFF-state after the transient (where v_{DS} is settled at the blocking voltage V_{dc}), which allows the stored charge to settle to the dc

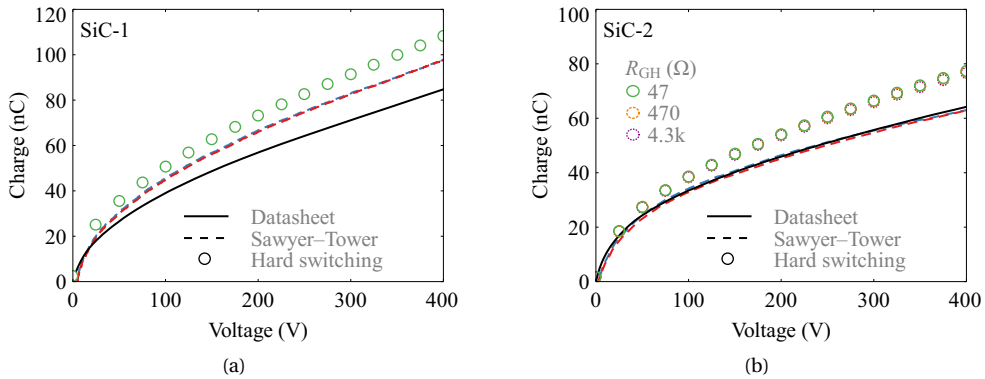


Figure 5.24: Experimental *QV* curves of two different SiC device types obtained using the proposed hard-switching method: conditions (a) f_{sw} = 100 kHz, d = 0.5, T_d = 100 ns, R_{GH} = 47 Ω and R_{GL} = 1 Ω; (b) f_{sw} = 20 kHz, d = 0.5, T_d = 2 μs and R_{GL} = 1 Ω. For device SiC-2, the switching speed in hard switching was varied by changing R_{GH}: 47 Ω (solid circles), 470 Ω (dashed circles) and 4.3 kΩ (dotted circles). The results show that there is no dependence on switching speed.

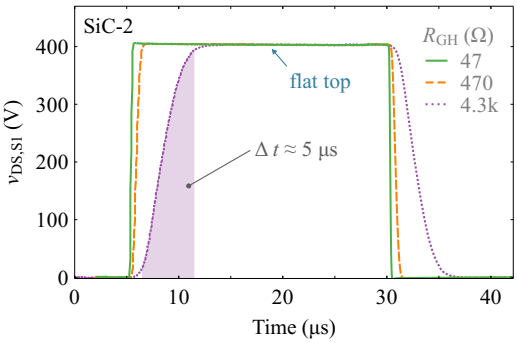


Figure 5.25: The v_{DS} waveforms corresponding to different R_{GH} values used for device SiC-2 in Figure 5.24. The switching speed slows down with increasing R_{GH}.

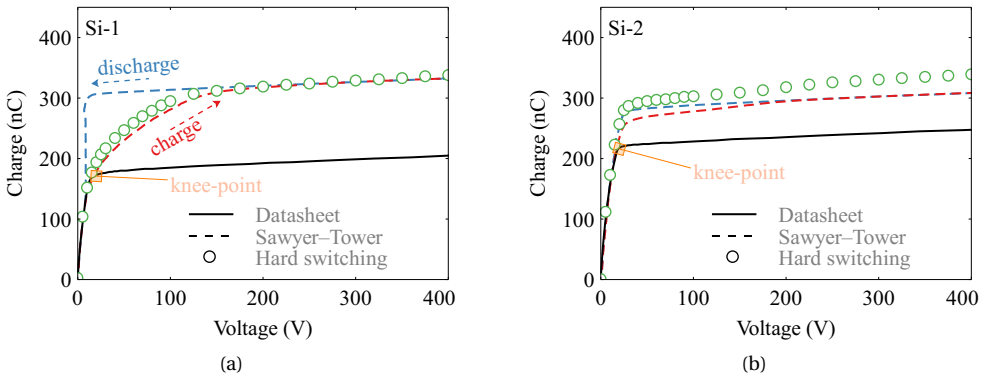


Figure 5.26: Experimental QV curves of two different Si-SJ device types obtained using the proposed hard-switching method are compared with respective curves based on the datasheets and Sawyer–Tower method. The conditions are $d = 0.5$, $T_d = 100$ ns, $R_{GH} = 47\ \Omega$, and $R_{GL} = 1\ \Omega$. A lower f_{sw} of 20 kHz was used to keep the device power dissipation low due to much larger Q_o values (≈ 300 nC at 400 V) of the Si-SJ devices.

electric field created by V_{dc}. In the latter on the other hand, the OFF-state voltage is continuously changing and a flat top in v_{DS} is never achieved. There, the charges are subjected to a time-varying electric field; this might create a different overall charge capacity in C_o.

For the Si-SJ devices (Figure 5.26), the Q_o values in hard switching are significantly larger in comparison with the datasheet values beyond the knee-point voltages (marked by a square). The Sawyer–Tower curves lie close to the hard-switching curves, indicating that the large-signal behaviour of C_o is considerably different to datasheet values. This observation is in agreement with the works by Zulauf et al. [18, 22], where the Sawyer–Tower measurements showed considerable discrepancies for Q_o against the datasheet values. Our results further reveal that the hard-switching charge capacity in Si-SJ devices could vary from the Sawyer–Tower curves as can be observed for device Si-2.

5.8.1 Interpretation of the Results

As datasheet values could differ from the tested batch of devices, small-signal CV measurements on five samples of each device type were performed. The measured small-signal output charge values for each transistor, normalized with respect to their corresponding datasheet values, are plotted in Figure 5.27. All devices are contained within a 10% variation from datasheet values, apart from device Si-1,

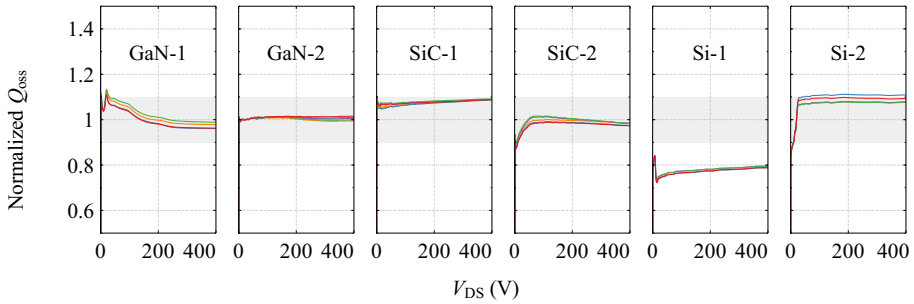


Figure 5.27: Small-signal measurement results showing normalized Q_{oss} values (measured/datasheet) for a dc sweep of V_{DS} = 0 to 400 V. Five samples of each tested device type were measured with a Keysight B1505A curve tracer at an excitation frequency of 100 kHz. The light-grey areas correspond up to a ± 10% variation from the datasheet.

which shows a 20 % variation. The results for the samples of the GaN devices and device SiC-2 stay very close to their datasheet values.

Figure 5.28 compares $E_{\text{on-C}_\text{o}}$ at 400 V for the tested devices, evaluated using the small-signal methods (datasheet and measured) and the hard-switching method (measured). For the two GaN-devices, all three methods show good agreement with differences contained within 5%. On the other hand, for example, device SiC-2 shows a 21.1% difference between datasheet and measured hard-switching values, which translates to a 0.211 × 25.56 μJ = 5.39 μJ difference in energy loss; and at an f_{sw} of 200 kHz, this means an additional power loss of 1 W, which is not negligible. The devices Si-1 and Si-2 show significant differences around 64.9% and 35.6% between methods 1 and 3, which cannot be explained even by the measured small-signal values. These results reveal two very important aspects about the large-signal behaviour of Q_o in hard switching:

1. Highly dependent on the semiconductor technology and the particular structures used within a given technology.

2. For certain devices, it cannot be predicted correctly with either the datasheet or the large-signal curves related to the soft-switching operation.

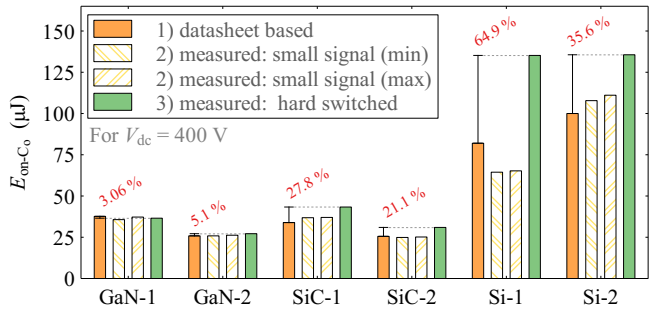


Figure 5.28: Comparison of measured (hard-switching method) and datasheet-based $E_{\text{on-C}_\text{o}}$ at 400 V for the devices studied in this work. Values of $E_{\text{on-C}_\text{o}}$ based on the small-signal measurements in Figure 5.27 are also shown (only the lowest and highest cases are compared). The percentage differences between the datasheet and measured hard-switching results are not negligible for SiC and Si-SJ devices. This directly affects the accuracy of E_{on} since $E_{\text{on-C}_\text{o}}$ is a load-independent contribution–see Eq. (5.27).

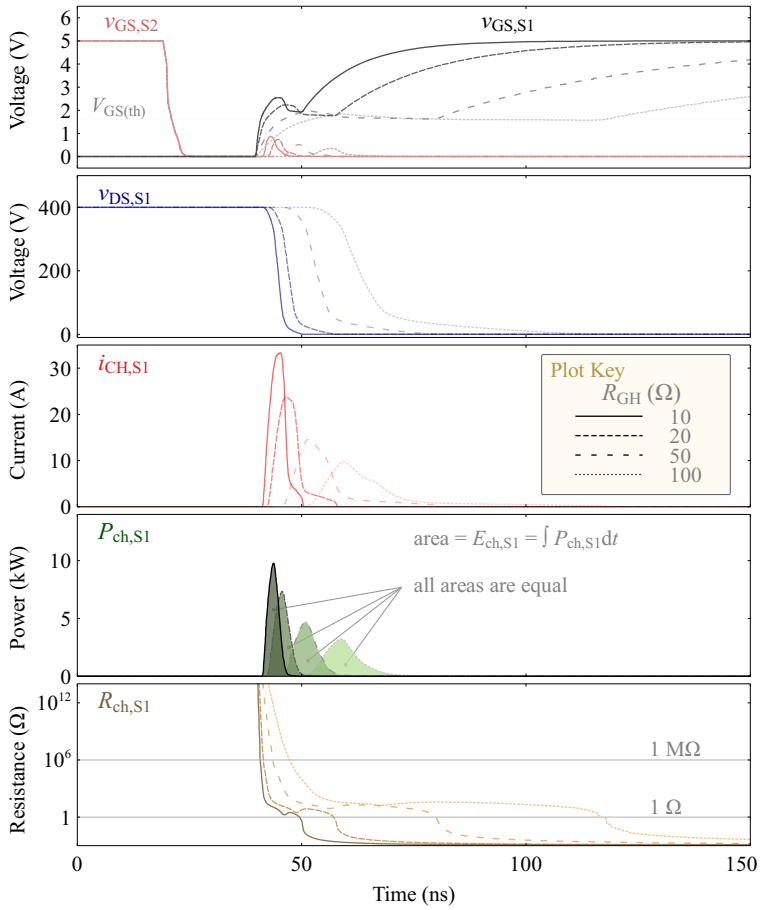


Figure 5.29: LTspice simulation results detailing the turn-ON transient of S_1 in the no-load circuit for different switching speeds achieved by sweeping the value of R_{GH}. A GS66508T GaN HEMT SPICE model was used. With increasing R_{GH}, the duration of the transient increases, whereas the peak values of the channel current decrease. This effectively makes the energy dissipation in the channel, $E_{ch,S1}$, the same for all R_{GH} values; in other words, $E_{ch,S1}$ is independent of the switching speed. The relevant variation of channel resistance is also shown; R_{CH} or its variation also does not effect on $E_{ch,S1}$. Simulation conditions: V_{dc} = 400 V, f_{sw} = 100 kHz, d = 0.5, T_d = 20 ns Ω and R_{GL} = 0.1 Ω.

5.8.2 Other Possibilities of the Method

In addition, the proposed measurement technique could be utilized to identify if Q_o exhibits any frequency- or dv/dt-dependence in hard switching by changing the value R_{GH} to control the switching speed (as was shown for device SiC-2). For a device without such dependence, the power loss and hence the energy related to the turn-ON process stays independent of R_{GH}, and hence the switching speed, as Figure 5.29 shows. This is because, although the increase of R_{GH} increases the time duration of the voltage commutation period, at the same time it decreases the peak value of the channel current. The variation of the channel resistance is also shown in Figure 5.29.

5.8.3 Gate-Driving

For the experimental work indicated in Figures 5.23, 5.24, and 5.26, the gate-driver supply voltage was set to $V_{DD1} = V_{DD2} = V_{DD} = 5$ V and a Texas instruments UCC27611 gate-driver IC was used. Thus, the drive voltage was also set to 5 V (i.e., $V_{drive} = 5$ V). Note that $V_{GS(th)}$ was less than 5 V for all the tested

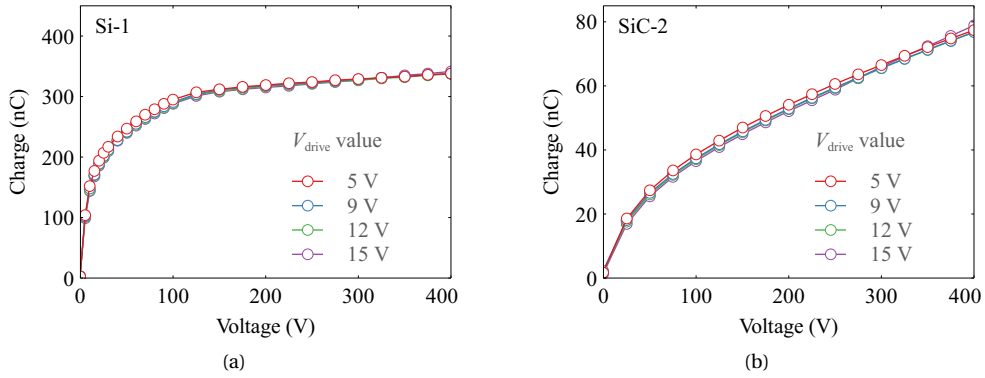


Figure 5.30: Experimental *QV* Curves for different drive voltages (V_{drive}) of 5, 9, 12 and 15 V, which effectively create different $R_{\text{DS(on)}}$ values for the FETs: (a) Si-1 and (b) SiC-2 are considered here. The conditions are f_{sw} = 20 kHz, d = 0.5, T_{d} = 100 ns, R_{GH} = 47 Ω and R_{GL} = 1 Ω. A Texas Instruments UCC27511 gate-driver IC is used that is capable of handling supply and drive-output voltages up to 18 V. Each V_{drive} value is obtained by using different dc-dc converters (Murata MTE1S03XXMC series, where XX = 05, 09, 12 and 15) to derive the gate-driver supply voltage. Results show that the *QV* curves remain practically unchanged with V_{drive}, confirming the independence of the product $Q_{\text{o}}V_{\text{dc}}$ on device $R_{\text{DS(on)}}$.

devices. In addition, we tested V_{DD} values of 9, 12 and 15 V for the devices Si-1 and SiC-2: for this purpose, the gate-driver was changed to a Texas instruments UCC27611 IC, which supports up to 18 V of supply and drive voltage. The resulting *QV* curves matched well with the 5-V case as Figure 5.30 shows; as different V_{DD} values create different $R_{\text{DS(on)}}$ values, this further proves the independence of the product $Q_{\text{o}}V_{\text{dc}}$ on $R_{\text{DS(on)}}$ for a given device.

5.8.4 Implications of the Loaded Operation

As was mentioned for the DPT circuit in Eq. (5.17), in a hard-switching half-bridge with an external load current i_{L} at the switch node, the total turn-ON energy loss in a FET can be described as

$$E_{\text{on}} = E_{\text{on-C}_{\text{o}}} + E_{\text{on-VI}}. \tag{5.27}$$

The existence of $E_{\text{on-C}_{\text{o}}}$ depends on the topology and its value is solely determined by the Q_{o} value of the device. For example, in the DPT circuit, $E_{\text{on-C}_{\text{o}}}$ of S_1 equals $E_{\text{o}} + E_{\text{o}}^{*}$. However, the turn-ON for S_2 is different and depends on T_{d}: if T_{d} is large enough, S_2 achieves ZVS turn-ON (facilitated by i_{L}), and hence, $E_{\text{on-C}_{\text{o}}}$ of S_2 would be zero; if T_{d} is too small, then S_2 experiences a partial-ZVS condition.

In contrast to $E_{\text{on-C}_{\text{o}}}$, the quantity $E_{\text{on-VI}}$ is a result of the product between v_{DS} and i_{L} [40]. For a constant load current ($i_{\text{L}} = I_{\text{L}}$), the magnitude of $E_{\text{on-VI}}$ mainly depends on the value of dv_{DS}/dt during the miller plateau, which can be controlled by the gate-driver circuit [25]. For this case, a quadratic equation in I_{L} can be used to model E_{on} as

$$E_{\text{on}} = a + b \cdot I_{\text{L}} + c \cdot I_{\text{L}}^2 \tag{5.28}$$

Here, $a = E_{\text{on-C}_{\text{o}}}$; b and c are circuit-specific coefficients. Such modelling is used in the recent work by Guacci et al. to experimentally characterize hard-switching losses in 200-V Si and GaN devices [92].

Table 5.2 lists the E_{on} (given in datasheet) and $E_{\text{on-C}_{\text{o}}}$ (based on datasheet C_{oss} and measured) of the tested devices. For most of the devices, $E_{\text{on-C}_{\text{o}}}$ is a considerable portion of E_{on}. Moreover, the

lower the value of I_{L}, the less significant the $E_{\text{on-VI}}$ component in Eq. (5.27) becomes, increasing the significance of $E_{\text{on-C}_{\mathrm{o}}}$ on the total turn-ON loss. Thus, it is important that manufacturers provide large-signal Q_{o} (or C_{o}) curves in device datasheets. It is favourable that the E_{on} parameter (if given) is separated into two parts in the datasheets as given by Eq. (5.27); this distinguishes between the effects of C_{o} and I_{L} on the turn-ON loss. These efforts help the circuit designers to make an informed decision on device selection for optimum designs.

Table 5.2: Comparison of E_{on} and $E_{on\text{-}C_o}$ Values of the Tested Devices

Device	Conditions for E_{on} Measurement [Datasheet]						E_{on} (μJ)	$E_{on\text{-}C_o}$ (μJ)	$E_{on\text{-}C_o}$ (μJ)
	V_{dc} (V)	I_L (A)	$V_{drive\text{-}OFF}$ (V)	$V_{drive\text{-}ON}$ (V)	R_G (Ω)	L (μH)	[Datasheet][1]	[Datasheet, at 400 V][2]	[Measured, at 400 V][3]
GaN-1	-	-	-	-	-	-	-	37.7	36.6
GaN-2	400	15	0	6	10/1	40	47.5	25.8	27.2
SiC-1	470	20	-5	20	4	-	130	33.9	43.3
SiC-2	400	20	-4	15	2.5	65.7	343	25.6	31
Si-1	400	20	-	-	10	50	260	82	135.2
Si-2	-	-	-	-	-	-	-	100	135.6

[1] Value is directly given in datasheets.
[2] Value is calculated from the datasheet C_{oss} curve.
[3] Measured using the proposed experimental no-load circuit.

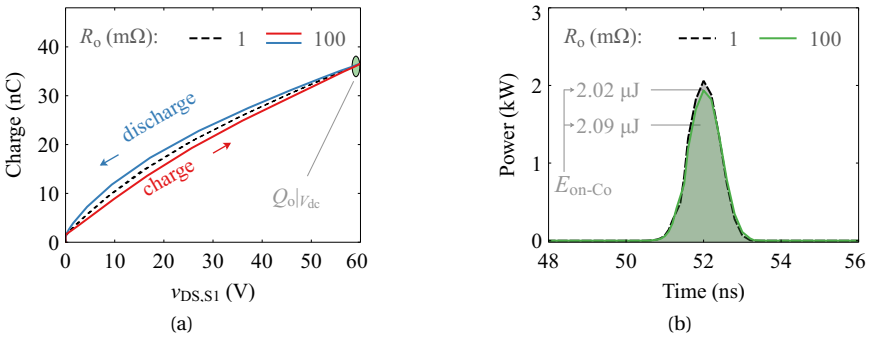


Figure 5.31: LTspice simulation results showing (a) the introduction of a large-signal hysteresis loop by having an external displacement resistance $R_o = 100$ mΩ (see [63]) in series with C_o, and (b) the resulting $E_{on\text{-}Co}$ loss for the device S_1. The inverter leg configuration is such that $S_1 = S_2$. The circuit was switched at 500 kHz.

5.8.5 Effects from the Large-Signal Hysteresis of C_o

In Chapter 4 we reported the differences between datasheet-provided small-signal output capacitance (or charge) values and experimentally measured large signal values in field-effect transistors. Two scenarios related to these observations can be considered when the $E_{on\text{-}Co}$ loss of a hard-switched device is concerned.

The first scenario concerns the device's charge value at the considered dc-link test voltage, $Q_o|_{V_{dc}}$. If the large-signal $Q_o|_{V_{dc}}$ value differs from the small-signal value from datasheets (for example, in the cases we reported in this Section for Si and SiC devices), then the correct large-signal value should be used for loss calculations.

A second scenario should be considered if the large-signal QV curve exhibits hysteresis by showing different paths for charge and discharge processes. For the case of $S_1 = S_2$ in the no-load circuit, this should not affect the final $E_{on\text{-}Co}$ loss as it is determined only by the final value $Q_o|_{V_{dc}}$ according to the energy conservation requirement of Eq. (5.20). Figure 5.31(a) shows an example operation of the no-load circuit with $S_1 = S_2$, where a large-signal hysteresis in the QV curves is created by adding an external displacement resistance, R_o, in series with the $C_o$of the two devices, as presented by Perreault et al. [63]. The separation of the charge and discharge curves in the $R_o = 100$ mΩ case, in comparison with the case of no hysteresis ($R_o = 1$ mΩ ≈ 0), is due to the loss in R_o in each charge and discharge process. The $E_{on\text{-}Co}$ losses—the addition of the loss in the device channel and R_o—related to the two cases are shown in Figure 5.31(b). The results show that there is a negligible difference between the two cases for the total loss in S_1 during its turn-ON process, indicating no influence from large-signal hysteresis (as $Q_o|_{V_{dc}}$ is kept unchanged). This is easily understood by realising that now the stored energy in $C_{o,S1}$ is discharged through the series combination of R_{ch} and R_o, and nevertheless, is lost. The observations are the same for S_2 during its turn-ON.

5.9 Important Technical Considerations

The effects of the parasitic inductances in the circuit paths are assumed to be negligible in the presented analysis; further investigations on this could provide additional insights on the subject. The external parasitic capacitances contributing to the switch-node capacitance should be considered if they are large enough (compared to device output capacitances) [40].

Table 5.3: Specifications of Average Measurements with FLUKE 87V DMM

Measurement	Type	Used Range	Resolution	Accuracy[1]
V_{dc}	Average	0–600 V	0.1 V	± (0.05% + 1)
I_{in}	Average	0–60 mA	0.01 mA	± (0.2% + 4)

[1] For a measured value M, a ± (X% + Y) accuracy means an absolute error of ± $[0.01MX + (Y \cdot \text{Resolution})]$.

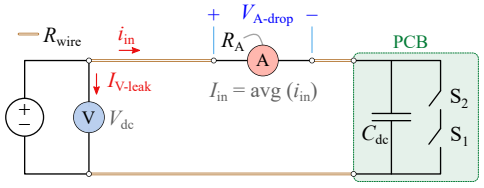


Figure 5.32: Placement of voltage and current measurement units to measure the average input power. R_{wire} is the dc resistance of the wires from the voltmeter to the dc-link capacitance C_{dc}; R_A is the insertion resistance of the ammeter and was measured to be 1.8 Ω in the mA-range setting.

In the following subsections, we detail technical considerations related to the QV measurement method presented in Section 5.7, which are extremely important.

5.9.1 Average Current and Voltage Measurements

The current i_{in} drawn from the input power source contains high-frequency components at f_{sw} and above. Thus, if the current measurement hardware does not contain any averaging process before sampling is done by the analogue-to-digital converter (ADC), the measurements could be erroneous. We have specifically used a Fluke 87V DMM as it contains an analogue 2-pole filter (with poles around 5 Hz) that implements an accurate averaging process before the ADC sampling takes place. As Table 5.3 indicates, both the average voltage and average current measurements have very good accuracies and high resolutions.

5.9.2 Loading Effects of DMMs

As shown in Figure 5.32, the voltage measurement takes place before the current measurement. This means that the ammeter measures the actual current going into the circuit. Therefore, any current ($I_{V\text{-leak}}$) flowing through the voltmeter does not affect the measurements. Furthermore, the voltage-drop across the line ($= i_{in} \cdot (R_A + R_{wire})$) is negligible compared to the measured input voltage range used in our experiments (50–400 V). Note that the average input current I_{in} was less than 30 mA in our measurements (based on our observations, the instantaneous current i_{in} could have a peak of two times I_{in}). An example can be considered: for $i_{in(peak)} = 0.1$ A and $R_{wire} = 3\ \Omega$, which is an extreme case, $V_{A\text{-drop}} = 0.1 \times (1.8 + 3) \approx 0.5$ V. Therefore, the line resistance has negligible effects on the measurement results.

5.9.3 Probing of the Switch Node

It is advised not to place voltage probes across the switch-node during the measurement of P_{in}; the added capacitance of the probe increases the switch-node capacitance, and hence, the measured I_{in}. The error in $\Delta Q_o / \Delta v_{DS}$ could be quite significant at high v_{DS} values, where device capacitances could

Table 5.4: Datasheet-Provided Drain–Source Leakage Currents

Device	I_{DSS} (μA)		V_{DS} (V)
	Typical	Maximum	[v_{GS} = 0 V]
GaN-1	3	30	650
GaN-2	2	50	650
SiC-1	-	100	700
SiC-2	1	100	900
Si-1	-	1	650
Si-2	-	10	650

be as low as 50 pF; the probe capacitances are generally around 5–10 pF. For instance, we have observed an 8 nC increase in Q_o at 400 V for device SiC-2 when a Tektronix THDP0200 differential voltage probe was placed across the switch node.

5.9.4 Drain–Source Leakage Current (I_{DSS})

In the OFF state of a device, I_{DSS} creates a power loss due to $I_{DSS} \cdot V_{dc}$. Ideally, this loss should be deducted from P_{in} to get C_o related losses. For the devices tested in this work, I_{DSS} is less than 100 μA (see Table 5.4), where the measured I_{in} is around 3–20 mA at V_{dc} = 400 V. Generally, typical I_{DSS} values are much lower than the maximum values. Therefore, the effects of device leakage current are considered negligible. In addition, we measured I_{DSS} of several samples of the tested devices using a power device analyser; all values were below 20 μA for V_{dc} = 400 V.

5.9.5 Selection of dc-link Capacitance

The value of C_{dc} should be large enough not to cause a large drop in voltage during the switching transients. A large ripple-voltage in C_{dc} could cause additional losses in the circuit due to its equivalent series resistance (ESR). Also, Class-II multilayer ceramic (MLC) capacitors, such as X7T and X7R types, exhibit a decrease in their capacitance at high voltages [47]; this should also be considered when selecting the type and value of C_{dc}.

5.10 Summary

We have revisited the fundamental concepts of hard switching and investigated the distinct role of device output capacitance in creating switching losses. It was shown that when a device is fully hard switched during its turn-ON process, a fixed energy loss is incurred in the device channel equal to $Q_o V_{dc}$, which is separated into co-energy and stored energy components of the top and bottom device output capacitances. Based on this theoretical foundation, an easy-to-implement technique to obtain large-signal QV curves of the output capacitance of FETs under hard switching was presented. The method is based on a no-load half-bridge circuit and is independent of the load current, dead-time, and device on-resistance. It was then applied to characterize commercial Si, SiC and GaN devices. Results showed that for certain device types, neither the datasheet nor the Sawyer–Tower results represent the actual charge capacity of device output capacitance in hard-switching operation. We emphasize the following.

- $Q_o V_{dc}$ is the proper measure for a fully hard-switched device, such as the switching device in a

DPT circuit.

- Small-signal values of charge (or stored energy) related to C_o do not necessarily translate to large-signal values.
- The large-signal behaviour of Q_o in the soft-switching operation does not correspond to the large-signal behaviour in hard switching. This is because the two operations subject C_o to fundamentally different charging mechanisms.

6 Gate-Driving Losses

CHAPTERS 4 and 5 focused on the direct consequences of the output capacitance of a power device for both hard- and soft-switching power converters. In this chapter, we discuss another energy loss that results from switching events and device output capacitance, however, related to the output-stage of gate-driving circuits.

Based on the concepts developed—especially in Chapter 5, here we analyse gate-driving losses under hard-gating conditions for MHz-range soft-switching applications. First, concepts are developed to identify the effective charge $Q_{\text{G-ZVS}}$ that determines the gate loss related to turning ON and OFF the power device, where the turn-ON is achieved under ZVS conditions. Then we reapply the no-load concept presented in Chapter 5 to experimentally measure the total gate-driving loss when a power device is turned ON with ZVS conditions. With these results, we demonstrate that there exists another comparable loss component in this process apart from the gate loss of the power device; this secondary loss component is characteristic of the output-stage of the gate-driving IC and is independent of the $Q_{\text{G-ZVS}}$ of the power device. Finally, with the developed concepts, we quantify both these loss components for a collection of commercial power FETs and gate-driver integrated circuits (ICs).

6.1 Motivation

Power loss related to driving the gate of a power FET becomes non-negligible in MHz-range switching frequencies. More specifically, and if we consider a *hard-gating* condition (discussed in Section 6.2.5), this loss is related to the complete charging of the input capacitance of the power device at its turn-ON

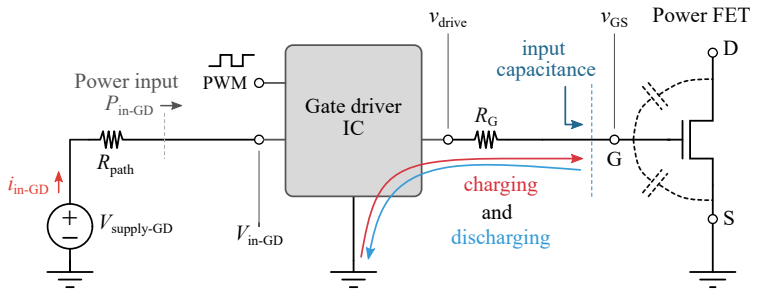


Figure 6.1: A simple representation of a gate-driving circuit.

and complete discharging of the same capacitance at its turn-OFF process (see Figure 6.1). In this regard, the conventional approach [94, 95] used to calculate gate-driving losses accounts only for what is known as the *gate loss*, which we denote as P_G in this thesis work.

The previous paragraph requires further clarification. What we identify by the *gate loss* is the power (or energy) loss solely linked with the gate charge, Q_G. Therefore, the gate loss does not take into consideration any other *additional* losses taking place inside the driver IC. With these additional losses,[1] the total gate-driving loss is greater than P_G for hard-gating conditions, or in other words

$$P_{\text{in-GD}} > P_G. \tag{6.1}$$

In most technical literature, only the gate loss is discussed in relation to gate-driving losses [96–99]; this could be misleading, especially for novice circuit designers and engineers. Therefore, our endeavour here is the following.

1. Elucidate the difference between the gate loss and the driver-related losses.
2. Show that additional losses in the driver are comparable to the gate loss for certain driver-IC and power-FET combinations.
3. Devise a simple experimental method to separately evaluate these two loss components.

Some works have separated P_G into driver and transistor losses based on the physical location of gate-loop path resistances [100, 101]. But this approach still leaves the additional losses inside the gate driver itself unaccounted for. In particular, a recent Application Note by Texas Instruments discusses the effect of the power FET on the gate-driver IC or a PWM controller with an integrated driver. However, the work only discusses the breakdown of the gate loss between the power FET, external gate resistors and the on-resistance of the driver transistors.

Our investigation on this additional loss was first motivated by the observation of unexpected losses (measured electrically and then compared to a value estimated based on datasheet Q_G) in driving a GaN HEMT (15 A and 650 V) with a UCC27611 driver IC. The work by Lopez et al. (in 2003) on a resonant gate-driving technique—that discusses the difference between the gate loss and additional losses in the driver—partly lays the foundation for our analysis in this chapter [85]. The distinction between these two components is essential for a correct breakdown of active-device losses and to make an informed decision on the gate-driver selection for high-frequency converters.

[1] In Section 6.3.2, we will define this loss as $P_{\text{GN-NL}}$.

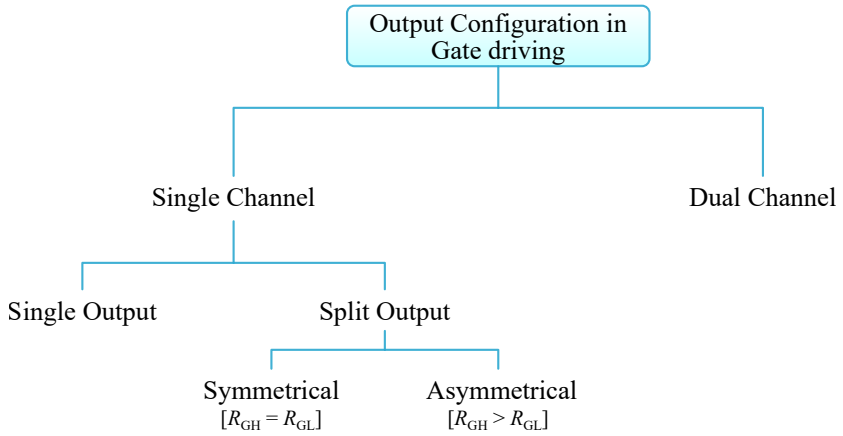


Figure 6.2: Classification of the output configuration in gate driving.

6.2 Basic Concepts

In this section, some basic concepts are reviewed alongside relevant terminology. We also discuss and present analytical means to distinguish between the gate charge value in ZVS and non-ZVS turn-ON of the power FET. The reader may skip Subsections 6.2.1 and 6.2.2, and move directly to Section 6.2.3, if familiar with the topics contained.

6.2.1 Output Configuration in Gate Driving

One important aspect in gate driving is selecting the required output configuration; this is partly defined by the gate-driver itself and partly by the circuit designer. Figure 6.2 provides a general overview of common configurations.[2]

A *dual-channel* IC can drive two power transistors, for example, the two switches in an inverter leg. These ICs come in two different variants: 1) non-isolated version, which uses a bootstrap technique to derive the high-side drive voltage; 2) isolated version, which generally requires two isolated power supplies (usually 1–2 W isolated dc/dc converters) to obtain the low-side and high-side drive voltages.

In contrast, and as the name implies, a *single-channel* gate-driver IC can only drive a single transistor. However they can be combined externally to drive two switches in an inverter leg: for instance, this was the configuration we have used in our no-load circuit introduced in Chapter 5 (see Figure 5.12). In this chapter, however, our focus is on driving a single transistor. In this regard, two variations can be found in commercially available gate-driver ICs as Figure 6.2 indicates:

1. *Single-output* configuration [see Figure 6.3(a)] involves only one output pin (OUT) and one external resistor, R_G; therefore, separate speed control of turn-ON and turn-OFF transitions of a FET is not possible.

2. S*plit-output* configuration [see Figure 6.3(b)] has two separate outputs, OUTH and OUTL, that allow individual control of turn-ON and turn-OFF paths, respectively. This is a design choice, and it is achieved by changing the values of two external gate resistors R_{GH} and R_{GL}. In gen-

[2] Details on the standard implementation of gate-drivers can be found in the textbook *Power Electronics Handbook* (Chapter 20, 3rd Edition) [29].

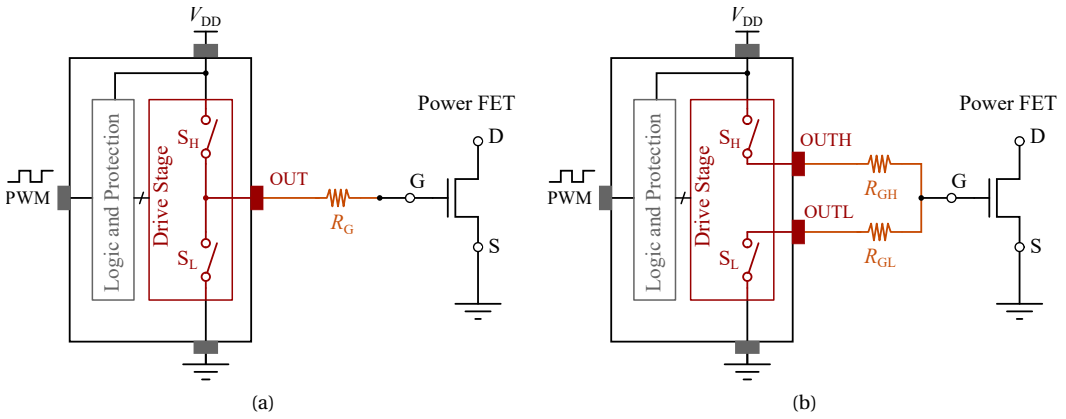


Figure 6.3: Single-output versus split-output gate driving. (a) Single-output configuration involves only one output pin (OUT) and one external resistor, R_G. (b) Split-output configuration has two separate outputs, OUTH and OUTL, and two external gate resistors R_{GH} and R_{GL}.

eral, split-output gate drivers have different source (through OUTH) and sink (through OUTL) current capabilities—See Table 6.2 in Section 6.5 for a set of practical values. The split-output configuration can be subdivided into two categories.

(a) *Symmetrical gate driving*, where $R_{GH} = R_{GL}$.

(b) *Asymmetrical gate driving*, where $R_{GH} > R_{GL}$. This is, in fact, the approach we have utilized in the no-load circuit technique presented in Chapter 5.

6.2.2 Input Capacitance, and Charge Stored in Input Capacitance

Here, we concern ourselves only with Si and SiC MOSFETS and GaN HEMTs. In our analysis, we denote the input capacitance as C_i, where the subscript 'i' stands for input. The value of C_i is defined as the addition of gate–source and drain–gate capacitances.

$$C_i = C_{GS} + C_{DG} \tag{6.2}$$

Note that, in device datasheets, the input capacitance is given as a small-signal parameter, which has been traditionally denoted as C_{iss}. Figure 6.4 shows, the datasheet-provided C_{iss} curves for a GaN HEMT and a Si-SJ MOSFET; the related C_{iss} values are also shown. It should be pointed out that C_{iss} is evaluated at a fixed dc-bias on drain–source terminals ($v_{DS} = V_{DS}$) in its standard characterization as documented by International Electrotechnical Commission (IEC) [31].[3] The dc bias on the gate–source terminals is also a condition that can be specified [31]; the test conditions used in device datasheets generally keep this at 0 V.

C_{rss} is referred to as the *reverse-transfer capacitance*, which is simply equal to the small-signal value of C_{DG}. Figure 6.4 also shows that datasheets provide C_{iss} and C_{rss} as a function of device drain–source voltage; they rarely provide the variation of these two capacitances with the gate–source voltage.

Referring to the datasheet C_{iss} curves in Figure 6.4, we can observe that C_{iss} stays relatively constant

[3] IEC 60747-8 ed 3.0 "Copyright © 2010 IEC Geneva, Switzerland. www.iec.ch".

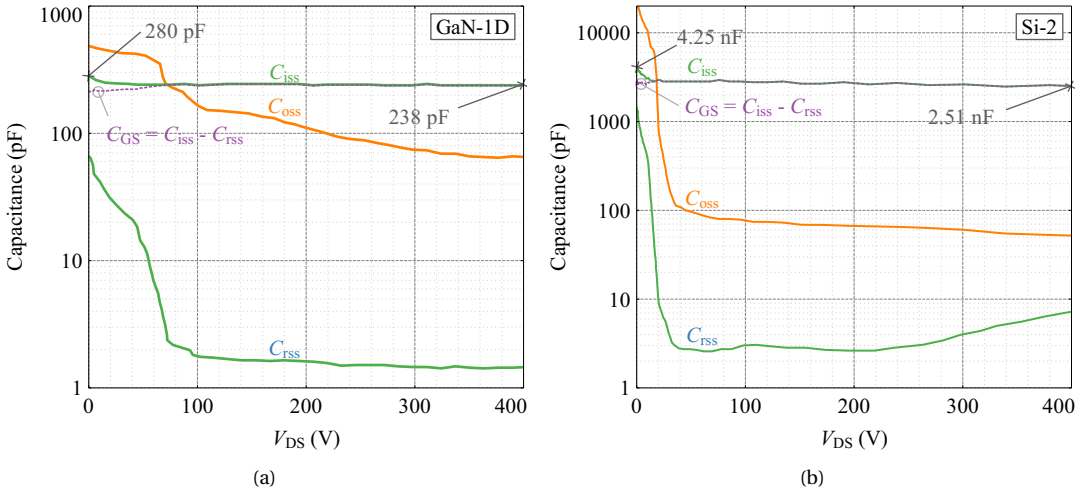


Figure 6.4: Variation of device parasitic capacitances for 650-V (a) a GaN device and (b) a Si-SJ device. Data is extracted from device datasheets (see Table 6.4 for the details of the two devices). The value of C_{iss} (the input capacitance defined in datasheets) at V_{DS} = 0 V and 400 V are also marked. Note: C_{GS} versus V_{DS}curve is simply evaluated as $C_{GS} = C_{iss} - C_{rss}$.

for both devices for $V_{DS} > 20$ V. As V_{DS} gets smaller, the value of C_{iss} starts to increase, due to the highly nonlinear nature of C_{rss}. This is also evident by the flat nature of the C_{GS} versus V_{DS} curves calculated and plotted in Figure 6.4.

Figure 6.5(a) illustrates how Q_G varies with V_{GS} for a hard-switched turn-ON event of a FET. Our analysis here is based on the principles presented in the application note *'MOSFET Gate-Charge Origin and its Applications'* by ON Semiconductor [98]. The document presents an extensive discussion on how Q_G is related to C_{iss} versus V_{DS} and C_{iss} versus V_{GS} curves. However, the document does not discuss any implications for a ZVS turn-ON event of a FET. The more recent Application Note '*CoolMOS™ gate drive and switching dynamics*' by Infineon also provides a good summary on the determination of gate

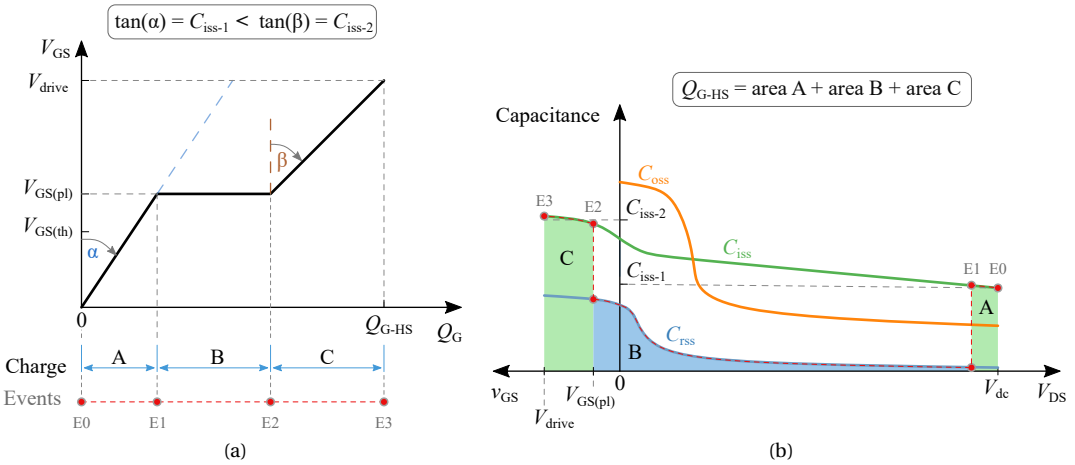


Figure 6.5: Charging process of the gate capacitance during a hard-switched turn-ON event of a FET. v_{DS} is at V_{dc}0 when the charging event starts. (a) The variation of gate charge versus gate–source voltage is shown by the solid black line. The process can be divided into three parts: 1) E0–E1, 2) E1–E2, and 3) E2–E3. (b) The variation of input capacitance with v_{GS} and v_{DS}.

charge. The note also points out the assumptions and limitations in the traditional Q_G versus V_{GS} curve given in datasheets and highlights that the gate charge is different for soft-switching conditions. Here we use concepts from both these documents and clarify the principles related to Q_G while providing additional analysis.

We start by identifying the selection of the correct voltage range for C_{iss} evaluation. The hard turn-ON event of a power FET consists of three separate stages as shown by the events in Figure 6.5(a) and Figure 6.5(b). Here we provide a qualitative analysis as follows, considering the small-signal capacitance values given in datasheets:

1. E0–E1: the device v_{DS} is clamped at $v_{DS} = V_{dc}$ by the external circuit and does not change. Therefore, for this charging stage, the value of C_{iss} in the region marked as E0–E1 (in Figure 6.5(b)) should be used. In this stage, C_{iss} is dominated by C_{GS}, as C_{rss} is considerably small [see Figure 6.4]. Thus, C_{iss} can be considered to be fixed at $C_{iss\text{-}1}$, and hence the linear increase in Q_G in Figure 6.5(a) with $\tan(\alpha) = C_{iss\text{-}1}$.
2. E1–E2: this is commonly referred to as the *flat plateau* or the *miller plateau* in a Q_G versus V_{GS} curve. v_{DS} starts to drop significantly and approaches the device's ON-state voltage. For simple analysis, it is generally accepted v_{GS} generally remains constant at $V_{GS(pl)}$ during this period. This means, only the charge stored in C_{rss} is subjected to change: voltage across C_{GD} is changed from a large positive voltage to a small negative voltage, equal to $-V_{GS(pl)}$.
3. E2–E3: the device is in ON-state and C_{iss} is charged up to the drive voltage V_{drive}. As we have mentioned before, device datasheets do not provide C_{iss} as a function of V_{GS}, while v_{DS} is clamped at 0 V (or more specifically, at the ON-state voltage of the device). However, related discussions and analysis can be found in an early work by Gauen [84] and the recent Application Note by ON Semiconductor [98]. According to these works, C_{iss} increases from its $V_{DS} = 0$ value for positive V_{GS}, while v_{DS} is clamped to ON-state voltage. For simplicity in our analysis, we consider C_{iss} to be fixed at $C_{iss\text{-}2}$. This results in a linear increase in Q_G for this period as Figure 6.5(a) shows, with $\tan(\beta) = C_{iss\text{-}2}$.

6.2.3 $Q_{G\text{-}HS}$ and Q_{ZVS}

Total gate charge (Q_G) is treated as the charge stored in the *input capacitance* of a power transistor for a given V_{GS} value. It should be, however, noted that Q_G is not a fixed parameter for a given transistor at a given V_{GS} value, but depends on the particulars of the circuit conditions. We can distinguish two definitions for Q_G at a given drive voltage ($V_{GS} = V_{drive}$) as shown below.

1. $Q_{G\text{-}HS}$: charge stored in input capacitance for a hard-switched turn-ON event of a FET.
2. $Q_{G\text{-}ZVS}$: charge stored in input capacitance for a ZVS turn-ON event of a FET.

6.2.3.1 $Q_{G\text{-}HS}$

$Q_{G\text{-}HS}$ is indeed the typical gate charge value provided in datasheets, for a given V_{GS} value. The datasheets also include the related drain current (I_{DS}) and drain–source voltage (V_{DS}) values (see Table 6.4 in Section 6.5 for example values), indicating that $Q_{G\text{-}HS}$ is also dependent on the I_{DS} and V_{DS} values of a given circuit. This is because, the plateau voltage $V_{GS(pl)}$ is a function of I_{DS}, whereas the duration of $V_{GS(pl)}$ is a function of V_{DS} [98].

Then, based on our analysis in Section 6.2.2, we can summarize the charge components in each stage as follows:

1. E0–E1: an amount of charge equal to A is stored in C_i, which can be approximated as $C_{iss} = C_{iss\text{-}1}$ (see Figure 6.5(b)). The gradient of Q_G with y-axis Figure 6.5(a) is given by $\tan(\alpha) = C_{iss\text{-}1}$.
2. E1–E2: an amount of charge equal to B is stored in C_{iss}, which is equal to the shaded blue area under the C_{rss} curve in Figure 6.5(b).
3. E2–E3: an amount of charge equal to C is stored in C_{iss}, which can be approximated as $C_{iss} = C_{iss\text{-}2}$. The gradient of Q_G with y-axis Figure 6.5(a) is given by $\tan(\beta) = C_{iss\text{-}2}$.

The total charge stored in Q_G is $Q_{G\text{-}HS}$, which is equal to the addition of areas A, B and C in Figure 6.5(b).

6.2.3.2 $Q_{G\text{-}ZVS}$

The difference between the charge paths for C_{iss} in hard-switched and ZVS turn-ON events can be visually identified in Figure 6.5(b) and Figure 6.6(b), respectively. In the latter case, the charging process starts when v_{DS} is already zero. This is because the drain–source voltage transition takes place before the device is turned ON at its gate, as mandated by the ZVS process. Therefore, $Q_{G\text{-}ZVS}$ involves only a single charging stage (from E0 to E1) as depicted by Figure 6.6(b). Here, for ease of analysis, we use the same fixed capacitance $C_{iss\text{-}2}$ that was used for the event E2–E3 in the previous analysis. This corresponds to a simple linear charging process as indicated by Figure 6.6(a), where the gradient of Q_G with y-axis Figure 6.5(a) is given by $\tan(\beta) = C_{iss\text{-}2}$. Although $\tan(\beta) > \tan(\alpha)$, we generally observe $Q_{G\text{-}ZVS} < Q_{G\text{-}HS}$, which is a result of E1–E2 event in a hard-switched turn-ON of a FET.

Since the value of $C_{iss\text{-}2}$ is not readily available in datasheets, we can use the C_{iss} value at $V_{DS} = 0$ for general calculations. However, the experimental method we present to evaluate $Q_{G\text{-}ZVS}$ does not require this simplification as it is not reliant on C_{iss} measurements.

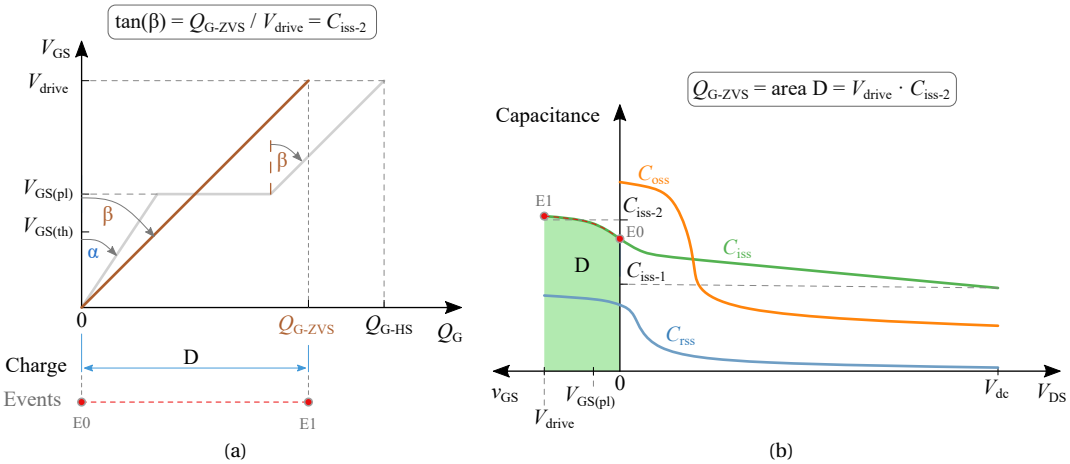


Figure 6.6: How the gate capacitance is charged during a ZVS turn-ON event of a FET. Here, v_{DS} is already zero when the charging process starts. (a) The variation of gate charge versus gate–source voltage is shown by the solid brown line. Compared to a hard-switched turn-ON event, this is a single process: E0–E1. (b) Variation of input capacitance with v_{GS}.

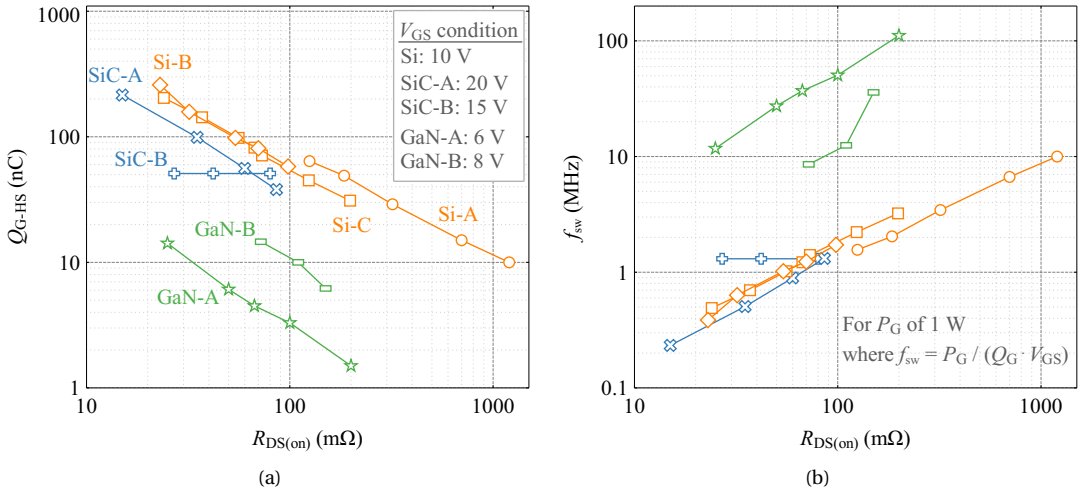


Figure 6.7: Analytical performance-evaluation of several commercial power-FET families (500–700 V) as a function of device $R_{DS(on)}$. (a) Variation of the reported $Q_{G\text{-}HS}$ value. (b) Maximum possible switching-frequency to keep $P_G < 1$ W. The gate-drive voltage (recommended value) for each family is also indicated. Details of the FET families are as follows. GaN-A = GaN Systems GS665 series; GaN-B = Transphorm TPH series; SiC-A = Microsemi MSC series; SiC-B = UnitedSiC UF3C series; Si-A = Vishay D series; Si-B = ONsemi NTHL series; Si-C = STMicro STW series.

6.2.4 $Q_{G\text{-}HS}$ values: a Practical View

To provide some practical perspective, Figure 6.7(a) plots datasheet provided $Q_{G\text{-}HS}$ with the power device's $R_{DS(on)}$ value for several GaN, SiC and Si families. The related V_{GS} values are also indicated. For GaN devices, generally, $Q_{G\text{-}HS}$ values are below 10 nC while for Si and SiC devices these values could range up to several hundreds of nanocoulombs.

Figure 6.7(b) plots the maximum switching frequency possible for the same devices for a gate power loss of 1 W.[4] This provides a qualitative picture of the capabilities of different semiconductor technologies (as well as different architectures/structures for a given semiconductor type) to be switched in the MHz-range frequencies, where the advantage of GaN devices is quite evident. As $Q_{G\text{-}ZVS} < Q_{G\text{-}HS}$, the limit of f_{sw} will further increase for soft-switching applications, which is our focus in this chapter as well as in Chapter 7.

6.2.5 Hard-Gating versus Resonant Gate-Driving

In this thesis, we identify a gate-driving process of a power FET as a hard-gating technique when the following conditions are satisfied.

1. The charging process of the input capacitance is driven by a fixed voltage source.

2. During the ON-state of the device (after the ON-transient is completed), v_{GS} becomes fixed at a dc level equal to the positive drive voltage (i.e., $v_{GS} = V_{drive}$).

[4] In practice, the isolated dc–dc converters that are used to power gate-driver ICs and that also have a small footprint, are generally rated for 1 W of output power. [102, 103]. This is why we have considered 1 W of power in Figure 6.7(b). As we will see later, part of this power will be assigned to $P_{GD\text{-}NL}$, leaving less than 1 W of power for P_G. This will ultimately require the circuit designer to choose a lower f_{sw}.

3. During the OFF-state of the device, v_{GS} is fixed at a dc level equal to 0 V ($v_{GS} = 0$).[5]

It is understood that v_{GS} changes during the ON and OFF transitions; but, it should settle to a fixed value after the transitions. These conditions result in a square-wave-type waveform for v_{drive} (see Figure 6.1) that vary between 0 V and V_{drive}. Then, we identify that the charging and discharging of the input capacitance resemble the process we presented in Section 5.3: the charging–discharging process of an *RC* load by a fixed voltage source. As we had proved, in such a process, the total energy supplied by the driver is completely lost. We identify such a gate-driving process as a hard-gating process. In the work by Lopez et al. [85], this is referred to rightly as *conventional gate-driving* as it is the most common gate-driving technique.

To improve the efficiency of gate driving, one could use resonant gate-driving, where the driver circuit is made to be a resonant one—a simple approach is to introduce an inductive element to the gate-drive path [85]. Another method is to use external sinusoidal excitation as demonstrated by Rivas et al. [50]. Both these approaches in effect, make the voltages and current in the circuit sinusoidal (or ac-excited). It is also evident that conditions 2 and 3 (listed above as requirements for hard-gating) are not satisfied in these approaches.

It should also be pointed out that hard-gating can be equally employed in hard-switching and ZVS-based soft-switching. For the rest of this chapter, our focus will be on the latter: hard-gating in ZVS circuits. Therefore, only $Q_{G\text{-}ZVS}$ applies for the following analysis.

6.3 Analysis of the Loss Mechanisms in Gate Driving

A typical gate-driver circuit consists of the gate-driver IC (denoted as GD) and external resistances R_{GH} and R_{GL}, as Figure 6.8(a) illustrates. The power FET is denoted as S. The energy source is a fixed dc voltage source with a voltage $V_{in\text{-}GD}$. The gate-driving is hard-gated (i.e., the gate-driving path is an *RC* circuit and involves no inductive components to achieve resonant gate-driving).

6.3.1 Gate Loss (P_G)

For ZVS conditions, the total gate charge in S is denoted by $Q_{G\text{-}ZVS}$ as Figure 6.8(b) shows [27]. During the turn-ON transient of S, C_i gets charged up to $Q_{G\text{-}ZVS}$ through the combined resistance $R_{DS(on)\text{-}S_H} + R_{GH} + R_{G\text{-}int}$ and the fixed voltage source.[6] This causes an energy loss in these resistors, in total, equal to the co-energy loss associated with C_i, which we denote as $E^*_{G\text{-}ZVS}$ [see Figure 6.8(b)]. This corresponds to a power loss

$$P_{G\text{-}ON} = f_{sw} \cdot E^*_{G\text{-}ZVS} \tag{6.3}$$

as marked by the area shaded in red in Figure 6.8(a). The energy stored in C_i during this process is $E_{G\text{-}ZVS}$.

During the turn-OFF transient, $E_{G\text{-}ZVS}$ is lost as the C_i is discharged through the combined resistance $R_{DS(on)\text{-}S_L} + R_{GL} + R_{G\text{-}int}$ [area shaded in purple in Figure 6.8(a)]. The relevant power loss is expressed as

$$P_{G\text{-}OFF} = f_{sw} \cdot E_{G\text{-}ZVS}. \tag{6.4}$$

[5] We do not consider negative drive voltages here.

[6] Here, we have assumed that R_{path} in Figure 6.1 is negligible.

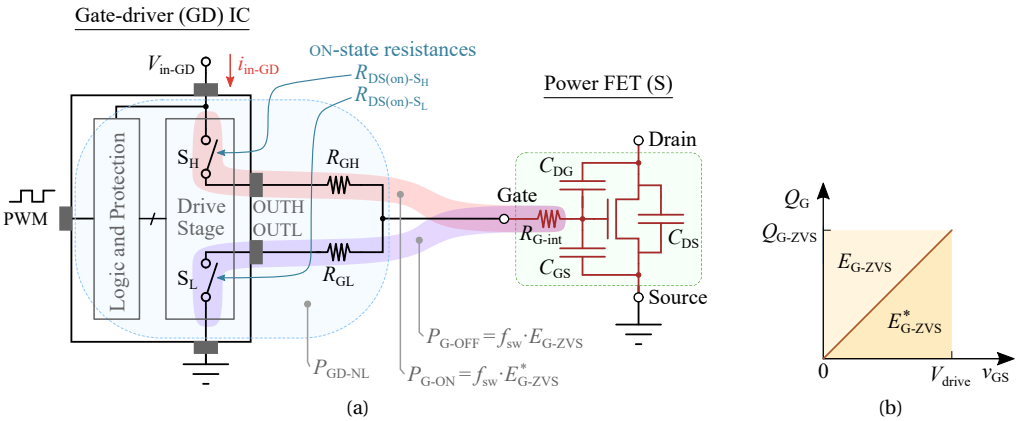


Figure 6.8: (a) A gate-driver IC with split outputs can be configured for asymmetrical gate driving to control the turn-ON (through OUTH pin and R_{GH}) and turn-OFF (through OUTL pin and R_{GL}) processes of the power FET, S. In hard gating, the input power to the gate-driver IC, $P_{\text{in-GD}}$, is completely lost. This loss has two components: 1) a gate loss $P_G = P_{\text{G-ON}} + P_{\text{G-OFF}}$ in charging–discharging of the input capacitance of S; 2) additional losses inside the gate-driver IC, denoted as $P_{\text{GD-NL}}$, dominated by the switching losses of the drive-stage transistors S_L and S_H. (b) In ZVS conditions for the power FET, the gate capacitance gets charged up to $Q_{\text{G-ZVS}}$ during the turn-ON transient and then gets discharged at the device turn-OFF, resulting in a total gate-energy-loss $Q_{\text{G-ZVS}} \cdot V_{\text{drive}}$.

Based on the concepts we developed in Chapter 5, we identify that both these losses are independent of the resistance values and are determined by $Q_{\text{G-ZVS}}$, V_{drive} and f_{sw}. The total gate-loss (P_G) is therefore given as

$$P_G = P_{\text{G-ON}} + P_{\text{G-OFF}} \tag{6.5}$$

$$P_G = f_{sw}(E^*_{\text{G-ZVS}} + E_{\text{G-ZVS}}) \tag{6.6}$$

$$P_G = f_{sw} \cdot Q_{\text{G-ZVS}} \cdot V_{\text{drive}} \tag{6.7}$$

Also, note that P_G is what Lopez et al. refer to as *'RMS loss' in conventional gate drivers [85].*

6.3.2 Losses in the Gate-Driver IC

The total loss in the gate driver IC can be separated into two main categories.

1. **Quiescent power loss**.

   This is mainly related to the power consumption in logic and control circuitry inside the IC. Generally, the quiescent power loss is considered negligible.

2. **Output-stage (or drive-stage) power loss**

   This is related to the two transistors S_L and S_H in Figure 6.8(a). The two transistors S_L and S_H are hard switched, and thus, create their own

   (a) output-capacitance losses (related to C_{o,S_H} and C_{o,S_L}),

   (b) gate losses (related to C_{i,S_H} and C_{i,S_L}), and

   (c) *VI* losses, which consist of

      i. VI overlap loss related to switching transients of S_L and S_H, and

ii. conduction loss related to the ON-states of S_L and S_H (the ON-state current is typically a pulse and quickly die off as the gate capacitance is charged and v_{GS} approaches V_{drive}).

In most of the state-of-the-art gate drivers, the quiescent current is less than 1 mA. In the drivers we have tested, the maximum current we observed was around 500 μA at a 5-V supply voltage (see Table 6.2 in Section 6.4.2). For most of the drivers, this was below 200 μA, which results in a dissipation of 1 mW; this loss is insignificant in comparison with the driver switching loss when the switching frequency is above 1 MHz.

The *VI* loss occurs in the channels of the S_L and S_H when the input capacitance of the power FET is charged and discharged. Therefore, this loss is already taken into account by the gate loss P_G of the power device, as we have seen in Section 6.3.1. Although it is true that part of P_G physically occurs inside the driver IC, the true cause of the loss should be correctly understood as the input capacitance of the power device, S.

Therefore, the total gate driving loss in driving a power FET should be correctly identified as the addition of two *independent* loss components:

1. The gate-loss related to the power FET, P_G.
2. The switching loss (which we denote as $P_{GD\text{-}NL}$) related to the charging and discharging of output capacitances and gate capacitances of S_L and S_H.

$P_{GD\text{-}NL}$ is marked by the area shaded in light blue in Figure 6.8(a). It should be noted that $P_{GD\text{-}NL}$ is often overlooked in the literature. In the notation, 'GD' refers to **g**ate **d**river and 'NL' refers to **n**o-**l**oad.[7]

It should be emphasized that $P_{GD\text{-}NL}$ cannot be calculated from the power device characteristics as it is an attribute of the chosen gate-driver IC. In this work, we present a simple no-load method to measure this power loss.

6.3.3 Total Gate-Driving Loss

Therefore, for hard-gating in ZVS circuits, the total power loss in gate driving is given as

$$P_{in\text{-}GD} = P_G + P_{GD\text{-}NL}. \tag{6.8}$$

6.4 Experimental Technique

Based on the concepts we developed so far, here we describe an experimental technique to separately evaluate P_G and $P_{GD\text{-}NL}$ for a given gate-driver IC and a power FET.

First, to evaluate $P_{GD\text{-}NL}$, we use the setup shown in Figure 6.9(a). Here, no load-capacitance is soldered to the PCB.[8] However, the external gate resistors (R_{GH} and R_{GL}) are put in place, as they are required to allow a closed electrical path for the output capacitances of S_L and S_H to be charged and

[7] The reason for the use of 'NL' is the fact that $P_{GD\text{-}NL}$ can be characterized by switching the driver IC under no-load conditions; we will see this next.

[8] Although PCB stray capacitances will act as loads here, they have negligible effect. For instance, it is less than 1 pF in our PCB design.

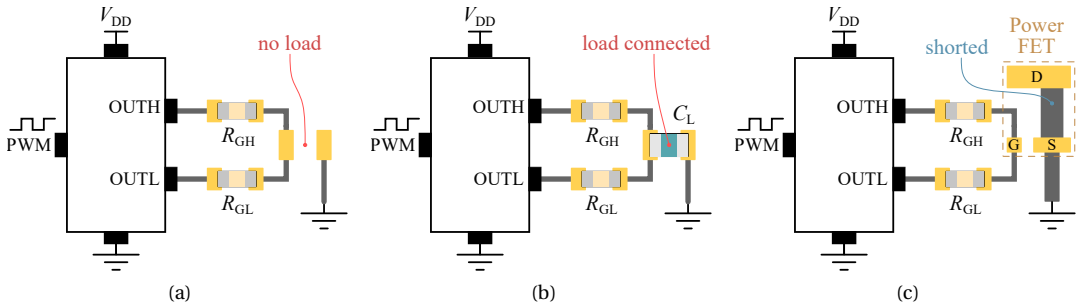


Figure 6.9: Three types of test circuits used in our measurement approach. (a) The no-load test circuit. (b) Gate-driver IC drives a linear-capacitor load, C_L. (c) Gate-driver IC drives the input capacitance of a FET under ZVS conditions (achieved by shorting the drain–source terminals of the FET).

discharged. In all our experiments, we keep $R_{GH} = R_{GL}$.[9] Then the driver is supplied with the required input voltage and switched at a switching frequency f_{sw}. Then the average power input to the gate driver $P_{in\text{-}GD}$ is measured as illustrated in Figure 6.10: $P_{in\text{-}GD} = V_{in\text{-}GD} \cdot I_{in\text{-}GD}$. For the circuit shown in Figure 6.9(a), $P_{in\text{-}GD}$ is equal to $P_{GD\text{-}NL}$.

The same electrical measurement technique is used for the loaded conditions. We consider two types of loads here. First, a linear-capacitive load as shown by Figure 6.9(b) is tested; this test serves as an additional verification of the measurement approach as will be seen in the next section. Second, the gate-driver is used to drive the input capacitance of a power FET as shown by Figure 6.9(c). In this condition, the measured power loss $P_{GD\text{-}L}$ is equal to the addition of P_G and $P_{GD\text{-}NL}$.[10] Finally, to get the value of P_G is calculated as

$$P_G = P_{GD\text{-}L} - P_{GD\text{-}NL}. \tag{6.9}$$

6.4.1 Important Measurement Considerations

An important practical consideration is the measurement of average input current, $I_{in\text{-}GD}$ (see Figure 6.10). In our investigations, we have come to understand that some DMMs (as well as the current measurement indicated on power supplies) sample the current directly without any filtering and then take the average of these samples. This can create significant errors in the *average*-current measurements. We have identified Fluke DMMs (more specifically, the FLUKE 87V DMM—see Table

[9] This is not a requirement as $P_{GD\text{-}NL}$ is independent of the values of R_{GH} and R_{GL}.
[10] The subscript 'L' in $P_{GD\text{-}L}$ refers to Loaded.

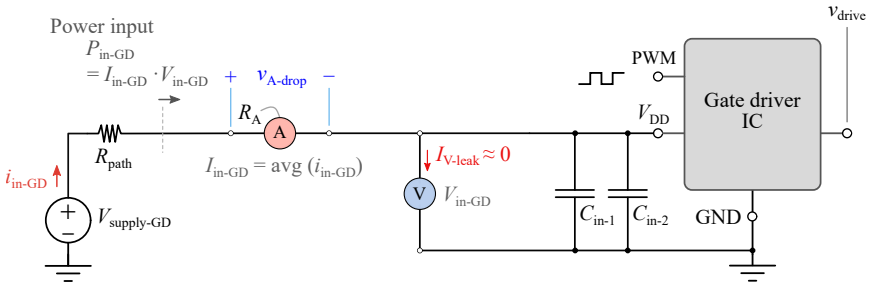


Figure 6.10: Electrical measurement approach showing the ammeter (A) and voltmeter (V) placements.

Table 6.1: Specifications of Average Measurements Performed with FLUKE DMMs

Measurement	DMM	Type	Used Ranges	Resolution	Accuracy[1]
$V_{\text{in-GD}}$	Fluke 117	Average	0–6 V 0–60 V	0.001 V 0.01 V	± (0.5% + 2) ± (0.5% + 2)
$I_{\text{in-GD}}$	Fluke 87V	Average	0–60 mA 0–400 mA	0.01 mA 0.1 mA	± (0.2% + 4) ± (0.2% + 2)

[1] For a measured value M, a ± (X% + Y) accuracy means an absolute error of ± $[0.01MX + (Y \cdot \text{Resolution})]$. Note: resolution and accuracy depend on the selected range.

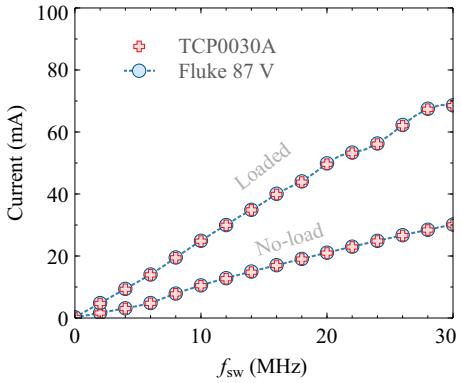


Figure 6.11: Variation of average input current $I_{\text{in-GD}}$ going into a gate-driver IC (a UCC27511A IC is used) with f_{sw}. Measurements with a Fluke DMM and a Tektronix TCP0030A (120 MHz) current probe are compared. Both no-load (no S is soldered to the PCB) and loaded conditions (S is a GS66504B device) are shown.

6.1 for details) as an adequate solution for this particular measurement.[11] Based on a discussion with an application engineer from Fluke, it was understood that the units can measure the average value of $I_{\text{in-GD}}$, with μA-level accuracy, owing to an analogue 2-pole filter (with poles at 5 Hz) implemented before the ADC. The average-current measurement process can be summarized as follows:

1. the analogue signal is fed to the filter.

2. the filter output is sampled by the ADC approximately every 100 ms.

The results from the DMM were verified by measuring $I_{\text{in-GD}}$ using a Tektronix TCP0030A current probe. The two measurements exhibit very good agreement and are compared in Figure 6.11.

Also note that the input voltage to the gate-driver IC, $V_{\text{in-GD}}$, is measured (we use a Fluke 117 DMM) very close to the supply input pin of the driver IC as Figure 6.10 indicates. This is because the average input current causes a voltage drop across the path resistance (R_{path}) and the ammeter resistance (R_{A}); this voltage can go up to several hundreds of millivolts under heavily-loaded conditions at high f_{sw}. However, to keep a consistent measurement condition, we have maintained the supply voltage $V_{\text{supply-GD}}$ fixed in our experiments: e.g., for an experiment with a 5-V supply (i.e., $V_{\text{supply-GD}} = 5$ V), $V_{\text{in-GD}}$ could be lower than 5 V.

[11] This was also the requirement for current measurements in the no-load method we presented for hard-switching losses in Chapter 4.

(a) (b) (c) (d)

Figure 6.12: (a) Some of the selected gate-driver ICs. (b)–(c) Examples of the designed PCBs. MMCX jacks are used for PWM-input connections. Two bypass capacitors $C_{\text{in-1}}$ = 1 μF (0603 package) and $C_{\text{in-2}}$ =0.1 μF (0402 package) are placed very close to the supply-input and ground pins of the driver ICs. The external driver resistors (R_{GL} and R_{GH}) are of 0603 package and soldered very close to the output pins of the drivers.

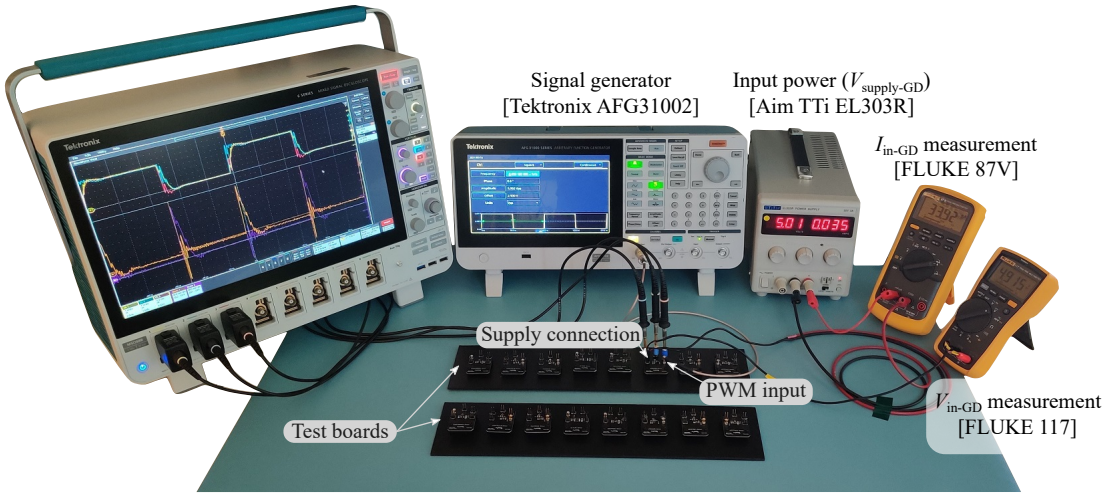


Figure 6.13: Complete experimental test setup consisting of an input power supply, a signal generator to derive PWM signals, two Fluke 87V DMMs to measure input voltage and current in average mode, and the PCB. The oscilloscope was used to observe the drive signal at various stages; however, the oscilloscope probes were disconnected from the PCB when the power measurements were carried out.

6.4.2 Details of the Experiments

Figure 6.12 shows some of the gate drivers and test PCBs. The complete experimental system is shown in Figure 6.13. A signal generator is used to generate the required PWM signals. As explained earlier, the average voltage and current measurements were carried out with Fluke DMMs.

The general conditions used in the experiments and presented in Section 6.5 are summarized as follows.

- In practice, a replica of the PCB that is used to measure $P_{\text{GD-L}}$ is employed to measure $P_{\text{GD-NL}}$, on which the power device S is not soldered.
- Two bypass capacitors $C_{\text{in-1}}$ = 1 μF and $C_{\text{in-2}}$ =0.1 μF were placed very close to the supply-input and ground pins of the driver ICs (see Figure 6.10).
- The duty ratio of the PWM is kept at 0.5 for all the tests.

- The external driver resistors (R_{GL} and R_{GH}) were chosen from the PCAN surface-mount-resistor series from Vishay [104]. These were specially chosen as they can handle relatively high levels of power for their package size. We have chosen the 0603 package (case size), which can handle up to 500 mW (voltage rating is 75 V). For the no-load and linear-capacitor-load tests, $R_{GH} = R_{GL} = 2$ Ω was used.
- The linear capacitors are of C0G(NP0) dielectric type, and therefore their capacitance has no dependence on voltage.
- All current measurements are taken on the dc setting on the mA range in the Fluke 87V DMMs (also see Table 6.1).

6.5 Performance Comparison of Commercial Gate Drivers for MHz-Range Switching

The concepts and measurement techniques we have developed in this chapter are used here to evaluate the performance of commercial gate-driver ICs, which are is listed in Table 6.2. Some important aspects of the selected drivers are summarized below.

- All the ICs are surface mount devices (SMDs).
- IC3 (LMG1020) is a GaN-driver with a maximum voltage output of 5 V. This Texas instruments driver claims a maximum operation up to 60 MHz, which is the highest frequency reported for a commercial driver IC by the time of writing this chapter.
- IC2 (UCC27611) is also specified as a GaN device driver. Although the driver can take input voltages up to 18 V, its output voltage is fixed at 5 V by an internal regulator (in our testing we have observed that the regulated value is generally around 4.7–4.9 V when operating at MHz-range frequencies).
- The datasheets of the gate driver ICs 1, 4 and 5 (UCC27511, 1EDN7511B and MAX5048C, respectively) specify that drivers are suitable to drive both Si MOSFETs and GaN devices.
- ICs 6 (EL7104) and 7 (ZXGD3009E6) are detailed as MOSFET drivers in their datasheets, while IC8 (UCC27531) is specified as a driver for both MOSFETs and IGBTs. It is also interesting to note that IC7 has an output stage that consists of two BJTs in NPN+PNP emitter follower configuration, unlike the other ICs, inside which the driver stage transistors are FETs.

Table 6.2: List of Split-Output Gate-Driver ICs Used in This Study

ID	Part Number	Manufacturer	Input voltage (V) [Datasheet]	Source current (A) [Datasheet]	Sink current (A) [Datasheet]	Quiesc. current at 5 V (μA) [Measured]	Package
IC1	UCC27511	Texas Instruments	4.5–18	4	8	161	SOT-23 6
IC2	UCC27611	Texas Instruments	4–18	4	6	159	WSON 6
IC3	LMG1020	Texas Instruments	4.75–5.4	7	5	43	WCSP
IC4	1EDN7511B	Infineon	4.5–20	4	8	295	SOT-23 6
IC5	MAX5048C	Maxim Integrated	4–14	3	7	534	SOT-23 6
IC6	EL7104	Renesas	up to 16	4	4	166	SOIC-8
IC7	ZXGD3009E6	Diode Incorporated	up to 40	1	1.6	-	SOT-23 6
IC8	UCC27531	Texas Instruments	10–35	2.5	5	154	SOT-23 6

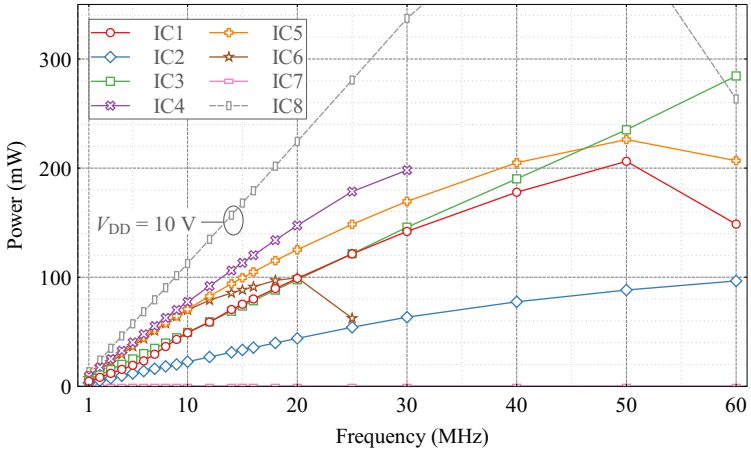


Figure 6.14: No-load power consumption of the selected gate-driver ICs (IC1–IC8) with switching frequency, f_{sw} (or the PWM frequency). All the ICs are supplied with a supply voltage of 5 V, except for IC8, which is supplied with 10 V. See Table 6.2 for the details of the ICs.

- All the ICs can be used at an input supply of 5 V, except for IC8, which requires a minimum of 10-V supply voltage.

In the next subsections, we investigate the performance of these gate-driver ICs using the circuits described in Figure 6.9 and according to the techniques presented in Section 6.4.

6.5.1 Power Loss in No-load Operation

The no-load power consumption (with switching frequency) for all the ICs is evaluated and plotted in Figure 6.14. All the drivers show a linear increase of power up to 10 MHz. Apart from IC6, they continue this linear relationship up to 30 MHz.

It can also be observed in Figure 6.14 that after a certain upper frequency (f_{max}) the power consumption starts to drop. This shows the limit beyond which the driver is not fast enough (i.e., not able to provide enough current, or power, within a short duration of time). The result is that the v_{drive} waveform collapses and it is no longer of square-wave type. This creates a situation where v_{drive} no longer settles to a fixed voltage (equal to V_{drive}) during the ON-period of a switching cycle.

The linear nature of the curves up to f_{max} suggests that the no-load power loss can be modelled as a loss caused by an effective linear capacitance ($C_{driver\text{-}eff}$) in the drive stage:

$$P_{GD\text{-}NL} = f_{sw} \cdot C_{driver\text{-}eff} \cdot V_{drive}^2. \tag{6.10}$$

By rearranging Eq. (6.10) for $C_{driver\text{-}eff}$, we get

$$C_{driver\text{-}eff} = \frac{P_{GD\text{-}NL}}{f_{sw} \cdot V_{drive}^2}. \tag{6.11}$$

In Figure 6.15, we have evaluated $C_{driver\text{-}eff}$ for all the ICs and plotted it as a function of frequency.

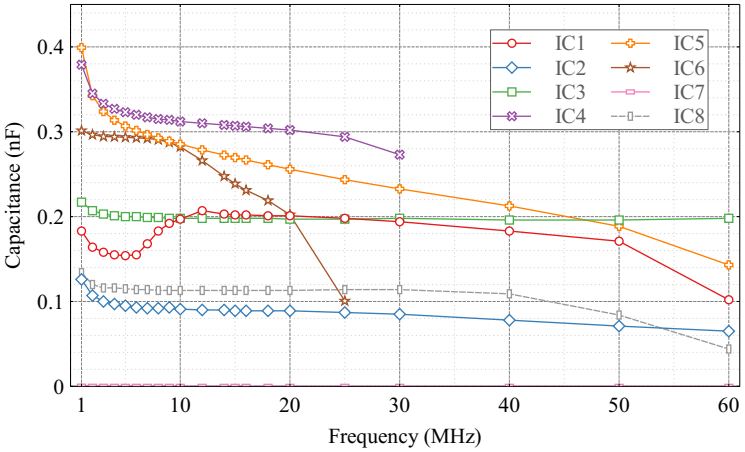


Figure 6.15: No-load losses observed in Figure 6.14 are used to derive an effective linear capacitance related to the output stage of the gate-driver ICs. This is derived as $C_{\text{driver-eff}} = \frac{P_{\text{GD-NL}}}{f_{\text{sw}} \cdot V_{\text{drive}}^2}$. The values range between 100–400 pF, which is comparable to the input-capacitance values of power FETs (rated for 400-V and up to 30-A operation).

Between 3–30 MHz, a fixed capacitance can be observed for all the ICs. This suggests that our hypothesis that $P_{\text{GD-NL}}$ consists of driver-stage QV losses associated with input and output capacitance of S_L and S_H is valid. To clarify again, since these capacitances are fixed values, the losses associated with them are independent of frequency as long as V_{drive} is fixed. Beyond f_{max}, the capacitance evaluated from Eq. (6.11) is seen to decrease in Figure 6.15 due to the collapse of the v_{drive} waveform. Therefore, Eq. (6.11) is not valid beyond f_{max}. Evidently, the correct $C_{\text{driver-eff}}$ should be taken from the fixed part of the curve.

From Figure 6.15, we can observe that the values of $C_{\text{driver-eff}}$ range between 100 to 350 pF for the tested ICs. And interestingly, this range is comparable to the input capacitances of power FETs (rated for 500-700 V), especially of GaN devices.[12] In our efforts to verify the results, we contacted Texas Instruments, specifically about IC1. They informed us that the internal capacitances of the drive-stage transistors can be estimated to lie between 100 and 300 pF for IC1. Figure 6.15 shows that our evaluated value is around 200 pF, which lies very much within the given estimate.

As a final remark, we can observe that IC7 does not show any power loss in no-load conditions. We believe this is due to its specific drive-stage design with two BJTs. Therefore, for this driver $P_{\text{GD-NL}}$ is simply 0 W. We confirm this result in the next subsection, where we investigate loaded conditions.

In summary, we have observed that the no-load power of loss of gate-driver ICs can go up to 200 mW at 5 V as the frequency increases and that $C_{\text{driver-eff}}$ is around 100 to 350 pF. It should also be noted that f_{max} would be lower when external loads are driven (due to the increased capacitive loading).

6.5.2 Power Loss in Driving Linear Capacitors

Here we evaluate the total gate-driving loss when a linear-capacitor load (C_L) is driven by the same set of driver ICs. The circuit corresponds to Figure 6.9(b) and we selected the following values C_L: 100, 470, and 1000 pF. Additional details of the selected capacitors are listed in Table 6.3.

[12] More on this is discussed in Section 6.5.3.

Table 6.3: Details of the Capacitors used as C_L

C_L	Manufacturer	Part Number	Rated voltage (V)	Dielectric	Package	Tolerance
100 pF	TDK	C1608C0G2A101F080AA	100	C0G(NP0)	0603	1%
470 pF	TDK	C1608C0G1H471F080AA	50	C0G(NP0)	0603	1%
1 nF	TDK	C1608C0G1H102F080AA	50	C0G(NP0)	0603	1%

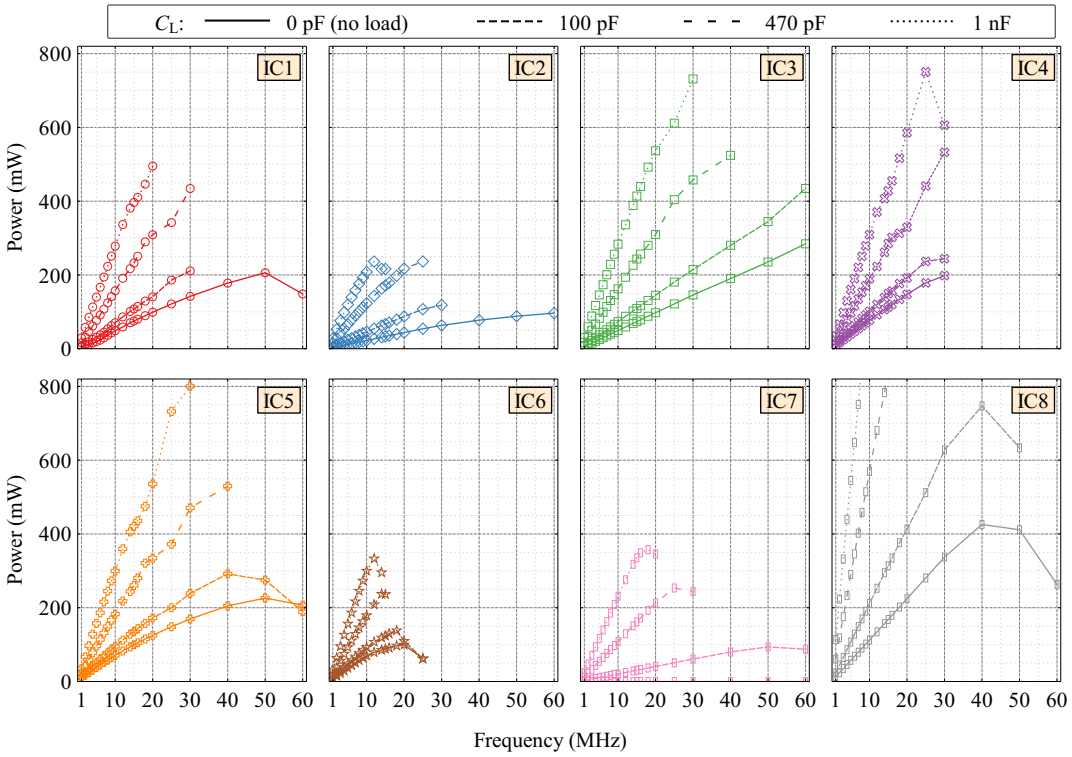


Figure 6.16: Total power consumption (or loss) in the selected driver ICs (IC1–IC8) with f_{sw} for different linear-capacitor loads. C_L values of 100 pF, 470 pF, and 1 nF were considered. No-load losses (C_L = 0 pF) are also shown for comparison. A $V_{supply\text{-}GD}$ = 5 V was used for all the ICs, except for IC8, which was supplied with 10 V. In general, the loss increases linearly with frequency according to the relation $P = f_{sw} \cdot C \cdot V_{drive}^2$ up to a certain f_{sw} value f_{max}, beyond which the switching no longer satisfies the hard-gating conditions.

The experimental results are presented in Figure 6.16: the eight plots represent IC1 and IC8, where each plot shows the loss for different loading conditions. The no-load losses are also indicated in plots (by solid lines) for comparison. As expected, the total gate-driving power loss is increased for all the ICs as C_L is changed from 100 to 470 pF, and then, to 1 nF. For each IC, linear curves can be observed for all loading conditions. However, the range of linearity is reduced with increasing C_L: and hence, f_{max} also reduces with increasing C_L, as we remarked in the previous subsection.

In Figure 6.16, we can also observe that beyond f_{max}, as for the case of no-load mode, v_{drive} does not settle to a fixed voltage after the ON-transient. The same applies to the v_{GS} waveform. This means that the excitation for the gate capacitance no longer satisfies the requirements for a hard-gating condition (see Section 6.2.5): therefore, the gate loss falls below $Q_{G\text{-}ZVS} V_{drive}$. This is because, although the input supply $V_{in\text{-}GD}$ is still fixed, the increased frequency no longer allows a complete charge–discharge process as ON and OFF times of a switching cycle are now comparable to the effective RC time constants in the circuit.

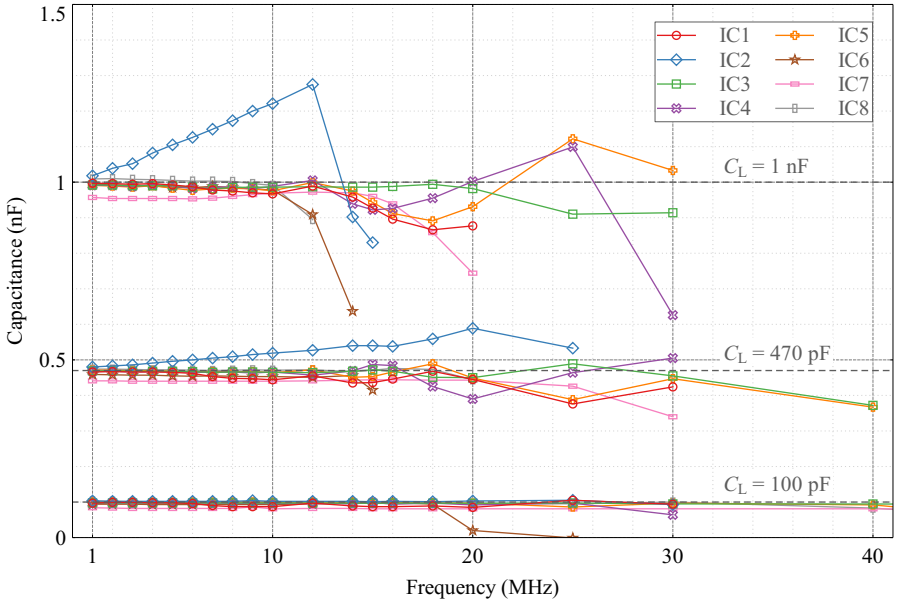


Figure 6.17: To examine the validity of the no-load concepts presented in this chapter, the load capacitance value (shown by solid lines) related to the results in Figure 6.16 is calculated using the equation $C_L = \frac{P_{GD\text{-}L} - P_{GD\text{-}NL}}{f_{sw} \cdot V_{drive}^2}$. The dashed lines show the exact C_L values.

From Figure 6.16, we can also remark that for C_L = 1 nF, the total power loss at 5 V can go up to 600 mW at 20 MHz for some ICs. For IC8, the experiments could only be carried up to relatively low frequencies (20 MHz for C_L 470 pF and 12 MHz for C_L = 1 nF) due to thermal limitations.[13]

As an extra verification step of the developed concepts, we perform the following calculation. Since we already have $P_{GD\text{-}NL}$ values of all the drivers as a function of f_{sw}, we can calculate the power lost in charging and discharging C_L by deducting $P_{GD\text{-}NL}$ from $P_{GD\text{-}L}$. The value of C_L can be evaluated from our experimental results as

$$C_L = \frac{P_{GD\text{-}L} - P_{GD\text{-}NL}}{f_{sw} \cdot V_{drive}^2}. \tag{6.12}$$

The results are plotted in Figure 6.17. The grey dashed lines show the actual values C_L (the datasheet values are given with 1% accuracy). The solid lines show the C_L calculated from Eq. (6.12) for each IC. For all three values of C_L and frequencies up to 10 MHz, we can observe excellent agreement between the datasheet and calculated values, apart from the case with IC2. With the exclusion of IC4 and IC6, the agreement extends up to 40 MHz for C_L = 100 pF. An important observation can be made about IC2. The actual and measured values agree well for the case of C_L = 100 pF. However, the values start to differ moderately for the case of 470 pF and significantly for the case of 1 nF. With these results we arrive at two very important conclusions:

1. Our approach for $P_{GD\text{-}NL}$ is valid for the tested gate-driver ICs.
    - A fixed value for $C_{driver\text{-}eff}$ for a reasonable frequency range indicates that the IC's output stage can be modelled as an effective capacitive load under no-load operation. The same conclusions can be made by observing a good agreement between actual and measured C_L

[13] The power losses are higher in this case because the supply voltage is 10 V.

values in Figure 6.17.

2. By looking at the plots of C_L, f_{max} for a given IC can also be identified for that C_L value.
    - A significant variation between measured and actual values for a given C_L indicates that the IC is no longer capable of performing hard-gating.

6.5.3 Power Loss in Driving Commercial Power FETs

In the light of our results and conclusions of the loaded (linear-capacitive) operation of gate-driver ICs, here we employ the same concepts for the input capacitance of power FETs, which has some nonlinear features. In the experiments, the same set of gate-driver ICs is selectively used in combination with several power FETs, whose details are tabulated in Table 6.4.

First, we investigate the total power loss ($P_G + P_{GD\text{-}NL}$) in driving the GaN HEMTS 1A to 1E (from the series GS665 from GaN Systems). As device GaN-1A is the smallest of the series, it has the lowest C_i, while device GaN-1E is the largest and has the highest C_i; the input capacitance of the other transistors

Table 6.4: List of Transistors Tested in this Study for Their Gate Loss

Index	Part Number	Manufacturer	Voltage	Current	Q_G typ.	Q_G given at		
			(V)	(A)	(nC)	v_{GS}(V)	v_{DS}(V)	I_{DS}(A)
Si-1	SIHG32N50D	Vishay	550	30	64	0–10	400	16
Si-2	NTHL110N65S3F	ON Semiconductor	650	30	58	0–10	400	15
Si-3	STW38N65M5	STMicroelectronics	650	30	71	0–10	520	15
SiC-1	MSC090SMA070B	Microsemi	700	28	38	-5–20	470	15
SiC-2	UF3C065080K3S	United SiC	650	31	51	-5–15	400	20
GaN-1A	GS66502B	GaN Systems	650	7.5	1.6	0–6	400	-
GaN-1B	GS66504B	GaN Systems	650	15	3.3	0–6	400	-
GaN-1C	GS66506T	GaN Systems	650	22.5	4.5	0–6	400	-
GaN-1D	GS66508T	GaN Systems	650	30	6.1	0–6	400	-
GaN-1E	GS66516B	GaN Systems	650	60	14.2	0–6	400	-
GaN-2	TPH3212PS	Transphorm	650	27	14.6	0–8	400	17

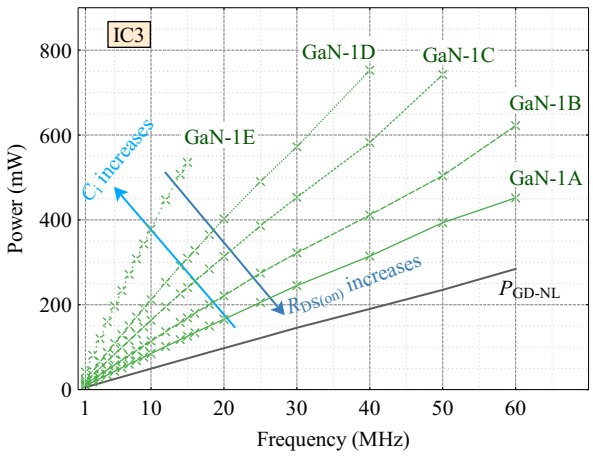


Figure 6.18: Variation of total power dissipation ($P_{in\text{-}GD} = P_{GD\text{-}L} = P_G + P_{GD\text{-}NL}$) versus frequency for the combination of driver IC3 (LMG1020) and the devices GaN-1A to 1E (as listed in Table 6.4). The GaN HEMTs belong to the GS665 series from GaN Systems. Device GaN-1A is the smallest transistor of the series (the lowest current rating and the highest $R_{DS(on)}$), whereas device GaN-1E is the largest (the highest current rating and the lowest $R_{DS(on)}$). $P_{GD\text{-}NL}$ of IC3 is also shown for comparison. Test conditions: $V_{supply\text{-}GD}$ = 5 V, $R_{GH} = R_{GL}$ = 4.7 Ω.

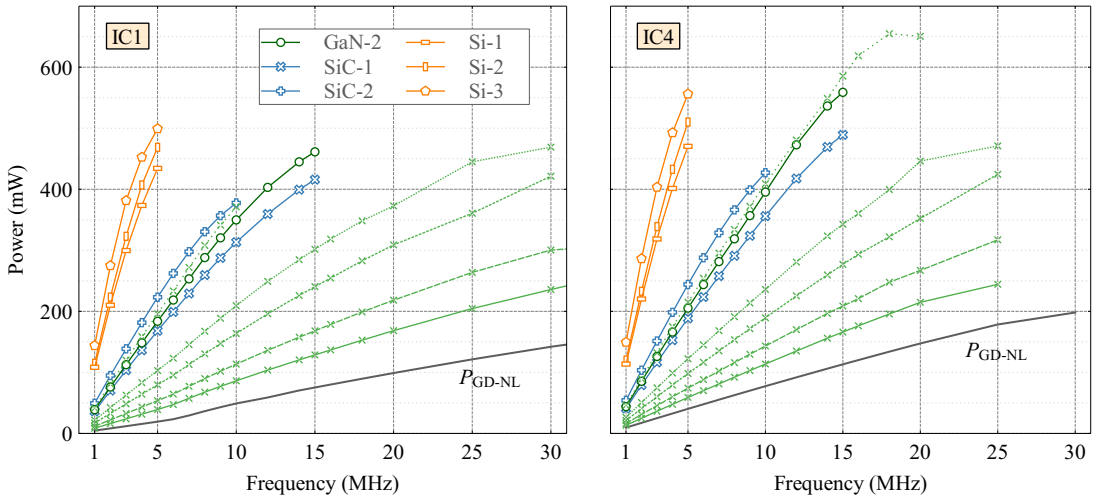


Figure 6.19: Variation of total power dissipation ($P_{in\text{-}GD} = P_{GD\text{-}L}$) versus frequency for all the devices listed in Table 6.4. The devices GaN-1A to 1E follow the same line styles that are used in Figure 6.18. (a) Gate driver IC1 (UCC27511) is used. (b) Gate driver IC4 (1EDN7511B) is used. Test conditions: $V_{supply\text{-}GD} = 5$ V, $R_{GH} = R_{GL} = 4.7\ \Omega$. The variation of $P_{GD\text{-}NL}$ is also shown for both ICs.

in the series lies between these two ranges. Figure 6.18 plots power loss against f_{sw} when this transistor series is driven by IC3 (which is specifically designed to drive GaN devices up to 60 MHz). As expected, device 1A results in the lowest $P_{GD\text{-}L}$, and hence, the lowest P_G, for the whole frequency range.[14] Both devices 1A and 1B can operate up to 60 MHz due to their low P_G values.[15] As the size of the device increase (or C_i), the value of f_{max} decreases as expected from our previous results in Section 6.5.2.

The total loss in driving all the selected transistors with ICs 1 and 4 is plotted in Figure 6.19. Here we have used a supply voltage of 5 V to perform a meaningful comparison for gate-charge. At 5 V, the GaN-1 series is fully enhanced, while the device GaN-2 is partially enhanced. All the tested SiC and Si devices also have a $V_{GS(th)}$ less than 5 V, and therefore, can be turned ON at 5 V. For the GaN devices, especially for the GaN-1 series, a lower $P_{GD\text{-}L}$ is observed for a given switching frequency. SiC devices also result in lower $P_{GD\text{-}L}$ than Si devices. We also evaluated the Si and SiC devices at $V_{supply\text{-}GD} = 10$ V (not plotted): around $f_{sw} = 4$–5 MHz, the total loss approaches 2 W for the Si devices; for the SiC devices f_{sw} can be increased up to 10- 15 MHz until the total loss approaches 1.5–2 W.[16]

6.5.4 Discussion

The total gate-driving loss related to the selected transistors and driver ICs gives an overall sense of the driving performance. However, the total loss does not reflect how good a driver-IC is for a particular application. To determine the best driver-transistor combination for MHz-range operation, we use the normalized metric

[14] Note that $P_{GD\text{-}NL}$ is fixed for the results in Figure 6.18 because the same driver is used.
[15] This also verifies the claim by the manufacturer of being able to operate up to 60 MHz.
[16] The results are similar for both IC1 and IC4 as the total loss is dominated by P_G. More on this will be discussed next in Section 6.5.4.

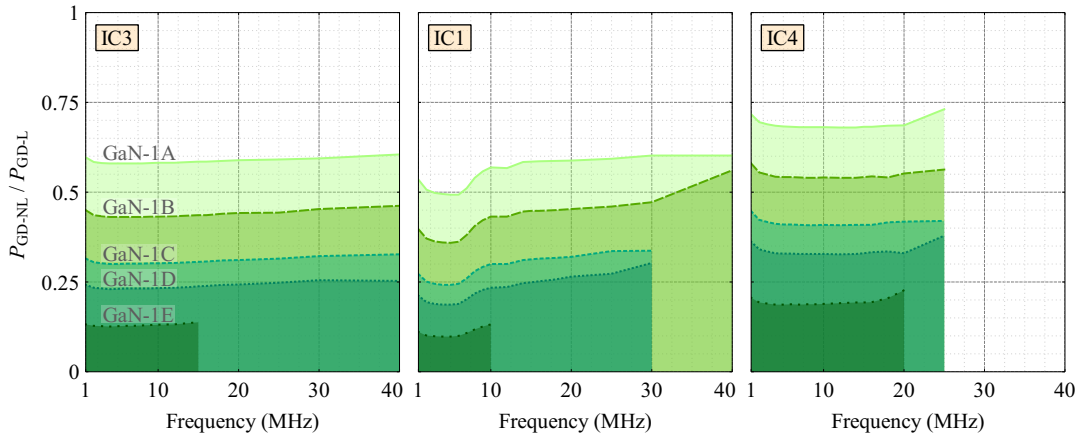


Figure 6.20: Normalized no-load power loss ($P_{GD\text{-}NL}/P_{GD\text{-}L}$) for the transistors GaN-1A to 1E (see Table 6.4) in combination with three different gate-driver ICs (see Table 6.2).

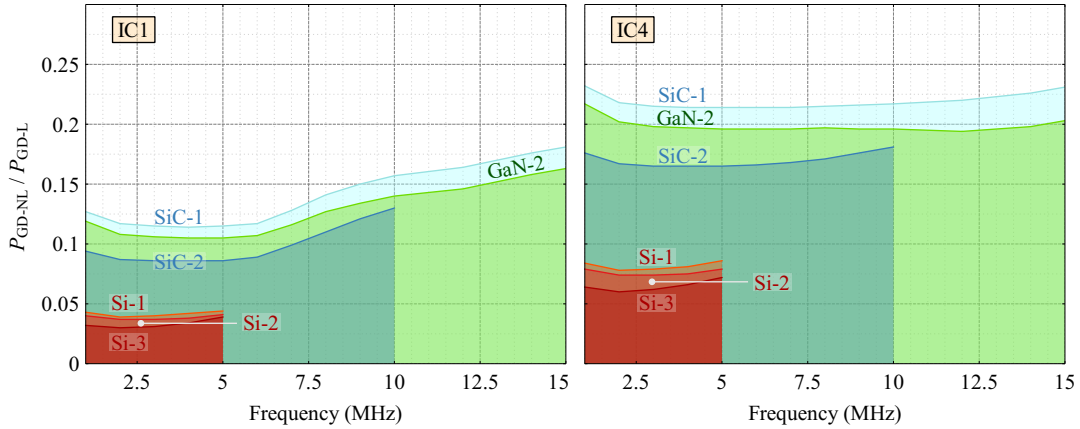


Figure 6.21: Normalized no-load power loss ($P_{GD\text{-}NL}/P_{GD\text{-}L}$) for GaN-2, Si and SiC transistors (see Table 6.4) in combination with two different gate-driver ICs.

$$\frac{P_{GD\text{-}NL}}{P_{GD\text{-}L}} = \frac{P_{GD\text{-}NL}}{P_{GD\text{-}NL} + P_G}.$$

This depicts how much power is lost due driver's internal switching in the total gate-driving process for a given driver-transistor combination.

Figure 6.20 plots this metric with f_{sw} for the combinations of GaN-1-series transistors and driver ICs 3, 1 and 4. Consider the case for driver IC3. The no-load power loss is a significant portion of the total driving loss for the cases of devices GaN-1A and GaN-1B, with 60% and 45% contributions, respectively. The loss percentage increases up to 70% and 55% for IC4. It should be noted that devices GaN-1A and GaN-1B are relatively low-current devices (7.5 A and 15 A, respectively), and hence, have lower input capacitances or gate-charge values(see Table 6.4). Therefore, for such devices, the total gate-driving loss is dominated by the driver internal-switching-losses, rather than the gate loss related to the power FET. To limit the $P_{GD\text{-}NL}$ a driver with lower $C_{driver\text{-}eff}$ can be used (see Figure 6.17); for example, the driver-IC 7 (see Figure 6.16). However, this is only possible up to several megahertz of

f_{sw}, as the source and sink current capabilities of this driver is limited. According to Figure 6.17, IC2 will be another good option, but again for low frequencies, as in this case, the driver's f_{max} for loaded conditions is severely limited, especially in comparison with IC3. Similar levels of performances can be observed with IC1 as with IC3, devices in GaN-1 series, with the main observable difference being the lower f_{max} for device GaN-1C to GaN-1E.

Figure 6.21 evaluates the ratio $P_{\text{GD-NL}}/P_{\text{GD-L}}$ for all the other power FETs when driven by ICs 1 and 4. The end frequency on the x-axis for each power device was decided by the value of f_{max} of a given driver-transistor combination. The main observation is that the percentage of the no-load loss is less than 25% of the total driving loss for both driver ICs. For Si devices, this is less than 10% ($f_{\text{max}} = 5$ MHz), which indicates that the driver loss is dwarfed by the gate loss of the power device. In contrast, SiC devices show a slightly higher ratio, mainly due to their relatively lower C_{i}.

Another interesting observation can be made about device GaN-2. This is a 27-A cascode GaN device, where the effective gate–source terminals of the device consist of a low-voltage normally-OFF Si MOSFET. Figure 6.21 shows that, for this device, the no-load loss is about 10–15% for IC1 and about 20% for IC4: both these values are higher in contrast to the no-load loss ratios for Si devices (1 to 3). This is because the input capacitance of device GaN-2 is smaller as it is a low-voltage ($\ll 650$ V) MOSFET, while the input capacitances of the tested Si transistors are much larger as their device structures are rated for 650 V.

6.6 Evaluation of $Q_{\text{G-ZVS}}$

In Section 6.4, the experimental method to separately evaluate $P_{\text{GD-NL}}$ and $P_{\text{GD-L}}$ was presented, which was then utilized in Section 6.5 to compare the performance of commercial drive ICs in driving power FETs. In this final section, we evaluate $Q_{\text{G-ZVS}}$ (at 5V) of the power FETs we have studied so far.

Using Equations 6.7 and 6.9, we get the relationship

$$P_{\text{G}} = P_{\text{GD-L}} - P_{\text{GD-NL}} = f_{\text{sw}} \cdot Q_{\text{G-ZVS}} \cdot V_{\text{drive}}. \tag{6.13}$$

Rearranging this equation, we get,

$$Q_{\text{G-ZVS}} = \frac{P_{\text{GD-L}} - P_{\text{GD-NL}}}{f_{\text{sw}} \cdot V_{\text{drive}}}. \tag{6.14}$$

For the tested power devices, Figure 6.22 plots the $Q_{\text{G-ZVS}}$ values calculated using Eq. (6.14). Consider Figure 6.22(a), which shows the results for GaN-1-series. It can be noticed that for devices A to D in the series, the curves related to the three different driver ICs (1, 2 and 3) are flat, and they coincide up to 20 MHz. For device 1E, this flatness and coincidence can be observed up to 15 MHz. This demonstrates two important points:

1. Our approach in evaluating $Q_{\text{G-ZVS}}$ is valid. This is because, for the method to be valid, $Q_{\text{G-ZVS}}$ curves should be independent of the driver IC. In other words, for the shown driver ICs, the driver switching loss can be described by $C_{\text{driver-eff}}$.

2. For a given power device, the maximum frequency up to which the $Q_{\text{G-ZVS}}$ curves stay flat is approximately the same for each driver IC. The value of $Q_{\text{G-ZVS}}$ should be evaluated in this region.

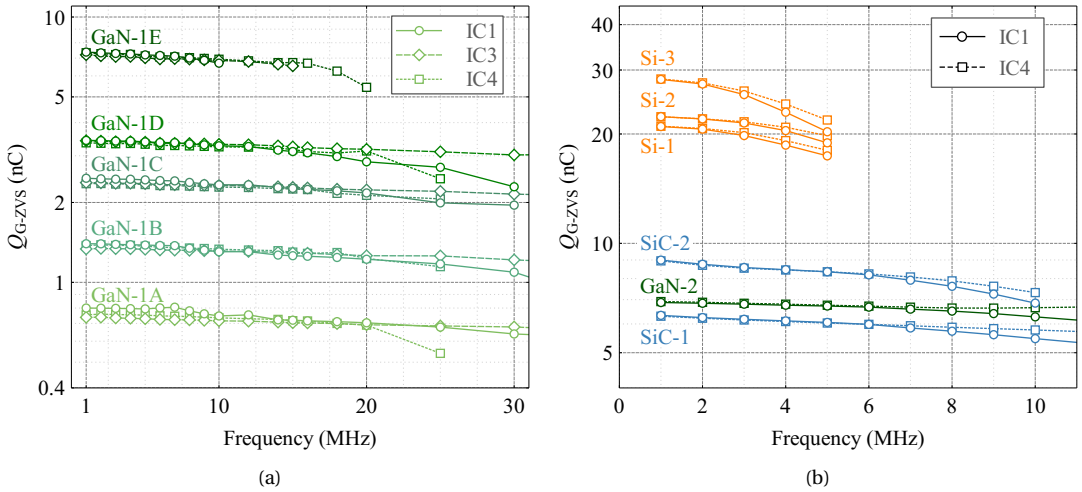


Figure 6.22: Experimentally evaluated value of $Q_{\text{G-ZVS}}$ (at 5 V) based on the proposed measurement technique. This is calculated using $Q_{\text{G-ZVS}} = \frac{P_{\text{GD-L}} - P_{\text{GD-NL}}}{f_{\text{sw}} \cdot V_{\text{drive}}}$. (a) Devices Gan-1A to 1E from Table 6.4 are considered with the driver ICs i, 2 and 4. (b) Rest of the devices from Table 6.4 are considered with the driver ICs 1 and 4.

The results also mean that, for practical operation, f_{max} is generally determined by the C_{i} of the power device rather than the $C_{\text{driver-eff}}$ of the driver.

In addition, Figure 6.22(b) considers the $Q_{\text{G-ZVS}}$ values of the other transistors. Similar observations about curve flatness and coincidence can be observed for device GaN-2 and both SiC devices. However, here, f_{max} values are relatively lower: $Q_{\text{G-ZVS}}$ should be evaluated below 8 MHz. For Si devices 1 and 3, a reasonable flatness in $Q_{\text{G-ZVS}}$ can be observed up to 4 MHz, whereas for device Si-3, frequencies below 2 MHz should be considered.

6.7 Summary

In this chapter, we have studied and analysed the gate-driving process concerning ZVS circuits operating in the megahertz range. First, different output configurations in commercial gate drivers were discussed to provide some practical perspective to the circuit topologies involved in gate-driving. The important distinctions between the following concepts were explained and analysed in detail: 1) $Q_{\text{G-HS}}$ and $Q_{\text{G-ZVS}}$; 2) hard-gating and resonant-gate-driving; 3) gate loss (P_{G}) related to the power FET and the driver-switching-loss ($P_{\text{GD-NL}}$). A simple experimental technique was presented to evaluate P_{G} and $P_{\text{GD-NL}}$ for a given driver-transistor combination. Practical aspects of the method were also discussed in detail.

The developed concepts were employed to evaluate $P_{\text{GD-NL}}$ of state-of-the-art gate-driver ICs and to calculate $Q_{\text{G-ZVS}}$ of commercial power FETs of Si, SiC, and GaN technologies. Experimental results showed that the losses in the output stage of driver ICs can be modelled by an effective capacitance $C_{\text{driver-eff}}$, which is charged and discharged every switching cycle. The aspects of identifying f_{max} for a given driver-transistor combination were also discussed. It was also found that, for GaN devices, the driver loss can be a significant portion of the total gate-driving loss due to their smaller C_{i} values, suggesting, that further improvements for loss minimizations should be made on the driver's output stage rather than on the power device.

7 Case Study with a Class-E Inverter

UTILIZING the theoretical basis and the experimental results we have presented so far, here we investigate the active-device losses in a resonant power converter. First, a new measurement approach—including the development of a novel milliwatt-level compact calorimeter—is presented to perform a complete loss breakdown of the active-device losses in a class-E inverter operating at 5 and 10 MHz.

Based on the technique, we provide an in-situ demonstration of output-capacitance hysteresis loss for two different GaN device structures and compare it with Sawyer–Tower circuit results. A final comparison of the conduction and hysteresis losses of the transistors is presented alongside the additional separation of the gate-loss and driver-switching loss related to gate driving.

This chapter is partly based on the material published in the following articles:

C3. **N. Perera**, R. van Erp, J. Ançay, A. Jafari, and E. Matioli, 'Active-Device Losses in Resonant Power Converters: A Case Study with Class-E Inverters', in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2021, pp. 5312–5319.

C4. R. van Erp, **N. Perera**, and E. Matioli, 'Microchannel-based Calorimeter for Rapid and Accurate Loss Measurements on High-efficiency Power Converters', in 2021 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2021, pp. 5709–5715.

7.1 Introduction to the Case Study

The use of GaN devices in resonant power converters, such as in the class-E topology [42–44, 51, 105–107], has gained recent popularity due to high-efficiency operation at MHz-range frequencies [8, 26, 48, 108, 109]. Precise determination of all the power losses in these converters is paramount for their optimization from a designer's perspective; it is equally important from a device engineer's perspective to identify non-ideal loss processes in the active devices in a converter. Such a task necessitates accurate measurement techniques that enable the breakdown of converter losses down to milliwatt level and a clear understanding of transistor and gate-driver loss distributions.

And it has never been more important as a notable output-capacitance hysteresis loss in GaN transistors has been reported, compromising the converter efficiency. This loss cannot be predicted by device datasheets and is related to a hysteresis energy loss, E_{diss}, in the transistor output capacitance as we have discussed in Chapter 4; and it is a function of device drain–source voltage, v_{DS}.

Exclusive measurement of C_{o}-hysteresis loss in an actual resonant power converter is challenging. This is due to several factors as listed below.

- The requirement of small circuit size in high-frequency operation creates probing difficulties for electrical measurements.
- Although total converter losses can be calculated using average and RMS electrical measurements (the actual possibilities are dependent on the circuit topology), the separation of active- and passive-device losses is not straightforward. Electrical measurement of device voltage and current to determine active-device losses is not feasible mainly due to bandwidth limitations.
- Loss quantification issues in thermal/calorimetric methods [17] (due to thermal cross-coupling when several devices are involved).

Therefore, indirect electrical methods such as the Sawyer–Tower technique [17, 23, 47] or calorimetric methods [110, 111] have been used to predict C_{o}-hysteresis losses in a working converter. However, these techniques offer difficulties in certain aspects. On the one hand, although an excellent technique (detailed in Chapter 4), the Sawyer–Tower method cannot always replicate the actual v_{DS} waveform, and in some cases, the subsequent estimations could not fully explain the difference between measured versus predicted efficiencies in certain converters [17, 108]. Thus, a direct and accurate method to measure hysteresis losses during actual circuit operation is of interest. On the other hand, existing calorimetric methods involve relatively slow systems that also have limited accuracy, especially in mW-range power levels [112]. Furthermore, they often determine system-level losses, and therefore, cannot perform a complete loss breakdown of a converter in real operation.

Moreover, the losses in gate driving become non-negligible in MHz-range switching frequencies. In this regard, the conventional approach used to calculate gate-driving losses accounts only for the gate loss (P_{G}) as was discussed in Chapter 6. The distinction between gate loss and the driver switching-loss is essential for a correct breakdown of active-device losses and to make an informed decision on the gate-driver selection for high-frequency converters.

To address these issues, we targeted a complete and accurate loss breakdown of a resonant converter operating at 5 and 10 MHz. The aim and contribution of this case study can be summarized as follows.

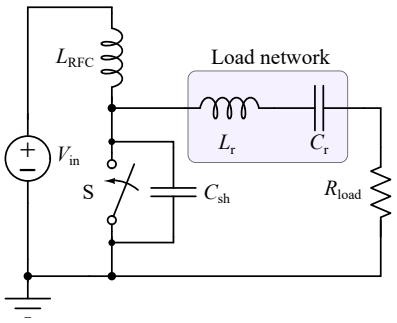


Figure 7.1: Standard *Class-E* inverter topology.

1. Select a versatile topology: class-E topology was selected (reasons discussed next).
2. Accurately measure active-device losses at mW-level: a compact and high-precision flow-calorimeter was developed.
3. Separate the active-device loss into transistor and gate-driving losses, using a combination of average current and voltage measurements.
4. Further divide the transistor power loss into ON-state (or the conduction loss, P_{con}) and OFF-state losses.
5. Based on the techniques developed in Chapter 6, separate the gate-driving loss into gate loss and driver internal loss.

We have chosen the class-E topology (see Figure 7.1), especially as a platform to measure the OFF-state loss of a transistor, as it offers several practical advantages:

- the existence of only a single transistor eliminates the issue of thermal cross-coupling between two devices [17].
- the path inductances between the input, the device-branch, and the output can be incorporated into circuit inductances, thus permitting direct electrical measurements, without complicating the circuit operation.
- all the parasitic shunt capacitances can be lumped together to a single shunt capacitance [43].

This case study also aims to serve as a practical point of reference for high-frequency losses in transistors and gate drivers, their relative contributions and practical measurement.

7.2 Basic Concepts and Analysis

In our analysis, we consider only field-effect transistors (FETs)—such as Si and SiC MOSFETS, and GaN HEMTs—as the switching device, which is denoted as S and undergoes zero-voltage-switching (ZVS). All the expressions and abbreviations for power refer to their average values unless otherwise stated. The power losses generated in S and the gate-driving sub-circuit constitute the active-device losses, P_{active}. The total power loss in a converter, $P_{\text{loss-tot}}$, consists of P_{active} and passive-device losses, P_{passive}:

$$P_{\text{loss-tot}} = P_{\text{active}} + P_{\text{passive}} \tag{7.1}$$

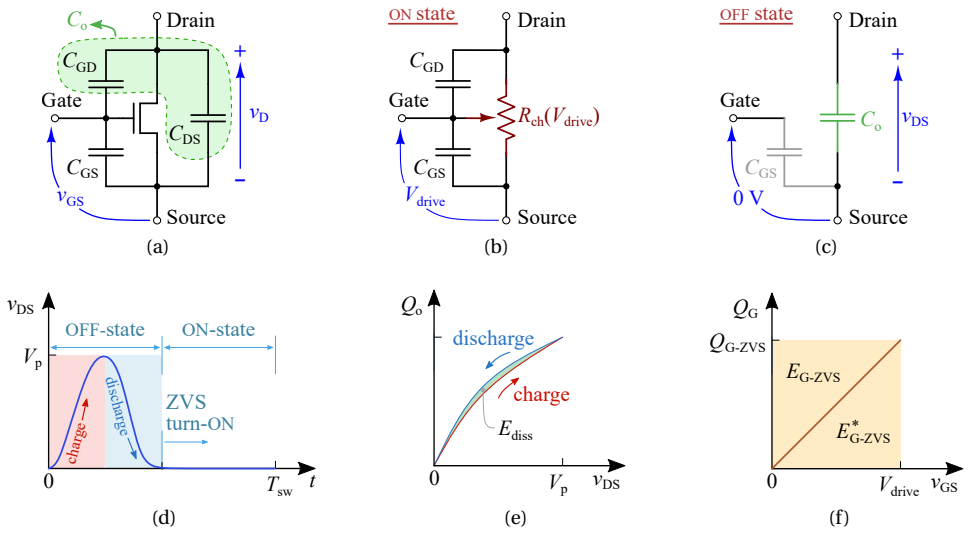


Figure 7.2: (a) Model of a FET showing its parasitic capacitances, where $C_o = C_{GD} + C_{DS}$ is defined as the output capacitance. For a class-E inverter, C_o is inactive during (b) the ON state of the device; and undergoes a complete charge–discharge cycle during (c) the OFF state of the device, where (d) the drain–source voltage, v_{DS}, shows a large-signal variation that generally occupies 50% of the switching period, T_{sw}. (e) Variation of the output charge (Q_o) with v_{DS} is represented by a QV curve; different charging (red line) and discharging (blue line) paths result in a hysteresis energy loss, E_{diss}, which is specified for a given maximum voltage V_p of v_{DS}. (f) The gate of the device gets charged up to $Q_{G\text{-}ZVS}$ during the turn-ON transient and then gets discharged at the device turn-OFF, resulting in a total gate-energy-loss $Q_{G\text{-}ZVS} \cdot V_{drive}$.

The total input power, $P_{in\text{-}tot}$, of the converter is described as

$$P_{in\text{-}tot} = P_{loss\text{-}tot} + P_{load}, \tag{7.2}$$

where P_{load} is the useful output power. In terms of average input power measurements, $P_{in\text{-}tot}$ can be expressed as the addition of the power-circuit input power (or the dc-link power), P_{in}, and gate-driver IC input power, $P_{in\text{-}GD}$:

$$P_{in\text{-}tot} = P_{in} + P_{in\text{-}GD}. \tag{7.3}$$

A FET model with its parasitic capacitances is shown in Figure 7.2(a), highlighting the output capacitance. When the device is in ON state [Figure 7.2(b)], a conduction loss, P_{con}, occurs which is a function of the ON-state resistance of the device channel, $R_{ch}(V_{drive}) = R_{DS(on)}$, and the channel current, i_{CH}. Here, V_{drive} is the voltage across the gate–source terminals of S, v_{GS}, in a fully-ON state. In the class-E inverter, which is a load-resonant soft-switching converter [28], C_o gets charged and discharged during the OFF state [Figure 7.2(c)] of the device. The corresponding v_{DS} waveform is shown in Figure 7.2(d). This charge–discharge process of C_o results in a non-ideal hysteretic energy loss,[1] E_{diss}, and can be calculated using a charge versus voltage (QV) curve as Figure 7.2(e) indicates [23, 47]. The OFF-state losses related to the leakage current through the device channel are generally negligible, especially in comparison with E_{diss} losses at MHz-range frequencies [47]. Therefore, the total power loss in S at a switching frequency of f_{sw} is given by Eq. (7.4), where $P_{diss} = f_{sw} \cdot E_{diss}$. Any loss related to gate driving is treated separately.

$$P_S = P_{con} + P_{diss} \tag{7.4}$$

[1] A similar phenomenon can be observed [46] for resonant-transition [81] converters; however, in that case, the charge and discharge processes occur during switching transitions (OFF-state v_{DS} is fixed at dc-link voltage).

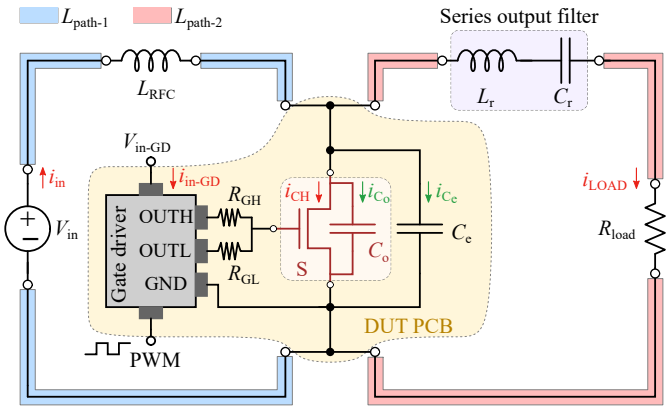


Figure 7.3: Detailed class-E inverter circuit. The transistor S and gate driver can be placed in a separate PCB, allowing physical separation of the active- and passive-device losses in the circuit. The extra inductances (L_{path1} and L_{path2}) of connecting wires introduced by this separation are simply added to the inductances of the RF choke L_{RFC} and the series output filter inductor L_r; these inductors and the capacitor C_r account for $P_{passive}$. Important currents (total instantaneous) in the circuit are also marked.

From our analysis in Chapter 6, we here summarize the important equations related to gate-driving when the power switch undergoes a ZVS turn-ON. The complete gate loss (P_G) is given as

$$P_G = f_{sw}(E^*_{G\text{-}ZVS} + E_{G\text{-}ZVS}) = f_{sw} \cdot Q_{G\text{-}ZVS} \cdot V_{drive}. \tag{7.5}$$

The total power loss in gate driving is

$$P_{in\text{-}GD} = P_G + P_{GD\text{-}NL}. \tag{7.6}$$

7.3 Class-E Inverter

Here, the loss components presented in Section 7.2 are identified with a class-E inverter circuit. The fundamental operating principles of this circuit are widely available in technical literature [28, 42–44, 108], and hence, are not discussed here.

Figure 7.3 shows a detailed schematic of the circuit: the transistor S and the gate driver constitute P_{active}; the input choke L_{RFC} and the series output filter consisting of L_r and C_r are responsible for $P_{passive}$. The total shunt capacitance consists of the transistor output capacitance C_o and any external linear capacitance C_e added for optimum class-E operation.[2] The operation of the circuit is summarized in Figure 7.4, highlighting how the energy losses related to the active devices in the circuit are distributed within a single switching cycle under steady-state operating conditions. The circuit is always operated in ZVS conditions—$v_{DS} = 0$ V when $v_{GS} = V_{GS(th)}$, as seen at t_1 in Figure 7.4. The gate-driving losses occur during the turn-ON and turn-OFF switching transients. For the duration (t_1–t_4) of the conduction loss, it is assumed that the channel is fully enhanced with $R_{ch} = R_{DS(on)}$. The hysteresis energy loss E_{diss} in C_o occurs during the OFF state (ideally extends up to some part of the switching transient).[3]

[2] The effects of the addition of an external linear capacitance (in parallel with device drain–source terminals) on class-E circuit operation are discussed by Suetsugu et al. in their 2014 publication [113].

[3] Detailed investigations on the effects of MOSFET parasitic capacitances on the class-E circuit operation were carried out by M. Hayati et al. in several publications [114–116]. However, the hysteresis loss effects of C_o were not considered in these publications.

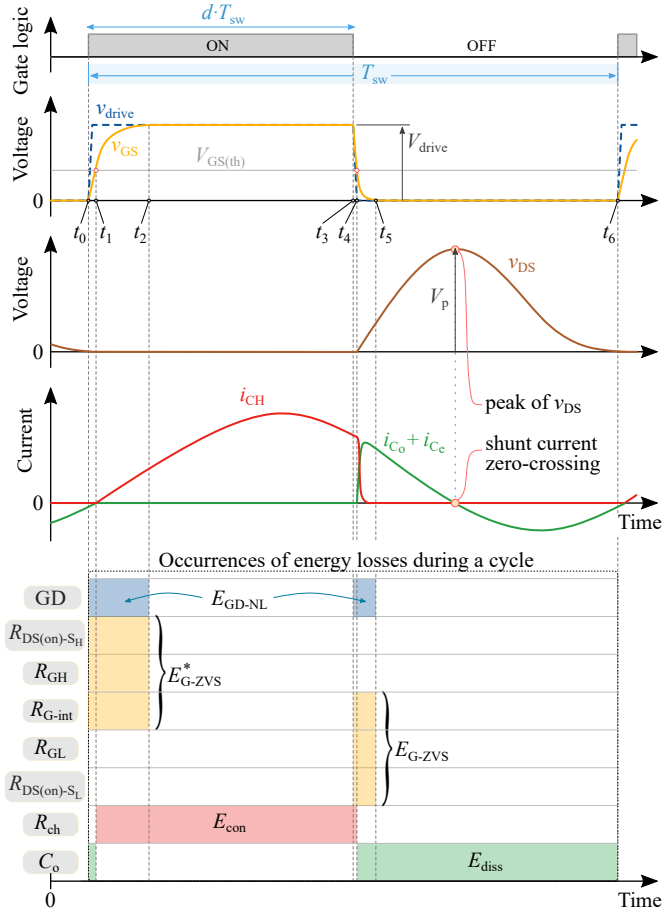


Figure 7.4: Class-E circuit basic waveforms and time distributions of active-device energy losses during a switching cycle $T_{sw} = 1/f_{sw}$. Generally, the duty ratio d is kept at 0.5. The gate-driver output terminals OUTH and OUTL determine the effective drive voltage v_{drive}. At t_0, OUTH is activated and v_{GS} rises. At t_1, v_{GS} equals gate–source threshold voltage $V_{GS(th)}$: the device channel turns ON and i_{CH} starts to rise at ZVS conditions. At t_2, the charging process of device input capacitance ceases ($v_{GS} = V_{drive}$) and the channel is fully enhanced. At t_3, OUTH is turned OFF and OUTL is activated: v_{GS} starts to decrease. At t_4, $v_{GS} = V_{GS(th)}$: device channel is cut off, i_{CH} decreases rapidly, and v_{DS} rises and charges C_o. At t_5, v_{GS} approaches 0 V. The discharge of C_o ideally ceases at the next $v_{GS} = V_{GS(th)}$ condition after t_6. The period t_1–t_4 is considered as the effective conduction period of the device channel (energy loss = E_{con}).

7.4 Design of the Measurement System

Referring to Figure 7.3, it can be noticed that physical separation of the heat generated due to P_{active} and $P_{passive}$ is possible with the class-E topology. This is the underlying principle of the proposed measurement approach for the accurate breakdown of losses.

The device under test (DUT) and the gate driver can be placed in a single PCB that is separated from the rest of the circuit. This requires longer connecting cables as marked by $path_1$ and $path_2$ in Figure 7.3. The advantage of the class-E circuit is that L_{path1} (and its related losses) is easily incorporated into L_{RFC}; thus, L_{path1} requires no compensation.[4] Similarly, L_{path2} is added to L_r; but, as L_{path2} alters the circuit operating conditions, in this case, the circuit should be tuned to achieve optimum class-E operation.[5] The use of calorimetric and electrical measurements, together with the approach for the

[4] This is valid as long as $L_{path1} \ll L_{RFC}$.Generally, this is the case for most designs.

[5] This is achieved by adjusting one or a combination of the components C_e, L_r, C_r, and R_{load} for a given f_{sw} [44].

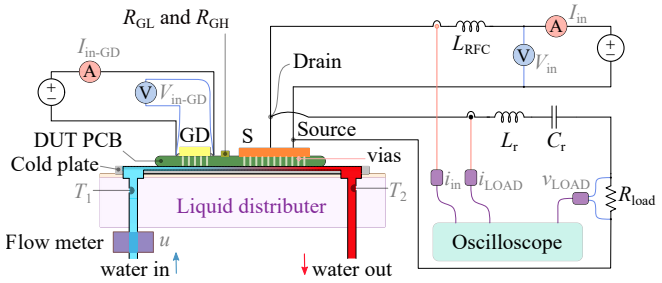


Figure 7.5: Simplified block diagram of the presented measurement system showing the class-E inverter, the DUT PCB, and the application of calorimetric and electrical measurements. Two thermocouples (type K) measure the inlet and outlet temperatures, T_1 and T_2, respectively. An Elveflow MFS-A-5 flow meter accurately measures the flow rate u. I_{in}, V_{in}, $I_{in\text{-}GD}$ and $V_{in\text{-}GD}$ are average electrical measurements carried out with Fluke 87V DMMs. i_{in} and i_{LOAD} are total instantaneous current measurements carried out with Tektronix TCP0030A current probes and an MSO68B oscilloscope. v_{LOAD} is measured with a Tektronix THDP0200A differential voltage probe.

full-breakdown of losses are discussed in the following subsections and Section 7.5, with reference to the block diagram of the measurement system depicted in Figure 7.5.

7.4.1 Design of a Compact Calorimeter

A novel and compact calorimetric unit [see Figures 7.6(a)–7.6(c)] was designed to evaluate the active-device losses in the circuit. The heat generated in S and GD (including the heat generated in R_{GL} and R_{GH}) is extracted by a microchannel-based cold plate fabricated on a piece of silicon [see Figure 7.6(a)], which is attached to the bottom of the PCB as Figure 7.5 illustrates.

A pressure controller is used to pass deionized water through the microchannels embedded in the cold plate [117]. The cold plate is brought in to good thermal contact with the circuit using

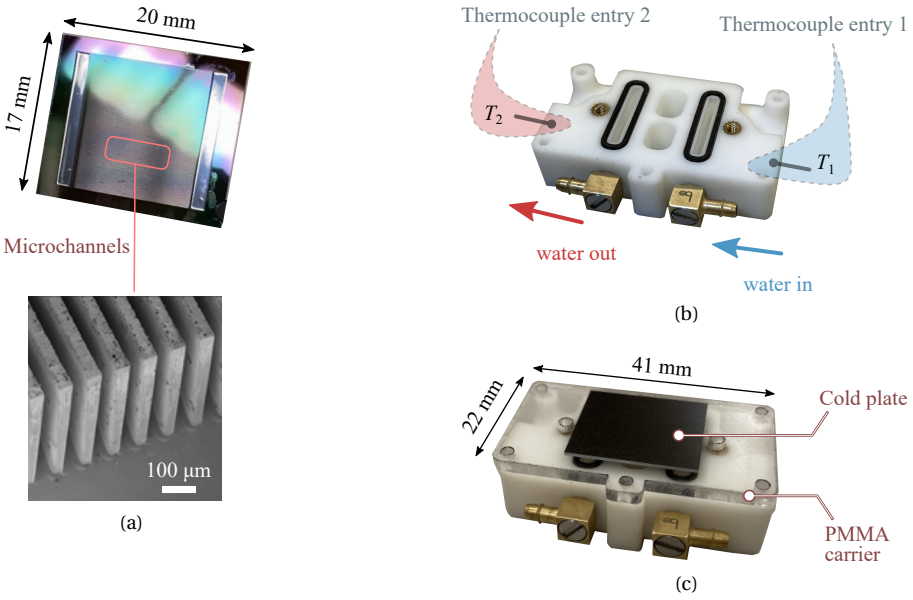


Figure 7.6: (a) A silicon microchannel-based cold plate and (b) a 3d-printed liquid distributor, with entries for water and thermocouples, are assembled as (c) a compact calorimeter and an efficient cooler.

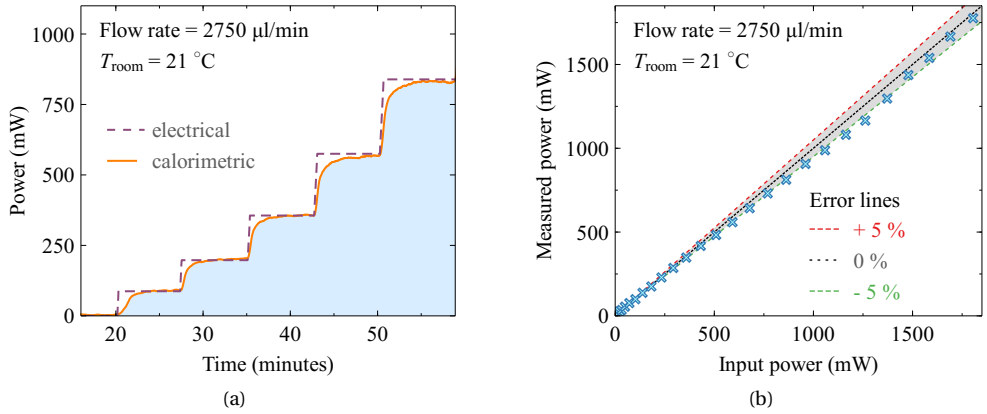


Figure 7.7: (a) Example showing that the power loss measured with the developed calorimeter (solid line) approaches the dc input power $V_{DS} \cdot I_{DS}$ (dashed lines) quite fast, allowing 6–7 measurements within an hour at the given flow rate; the calorimeter tracks power levels as low as 100 mW with very good accuracy. Here, the transistor S is in ON state and a dc current I_{DS} was passed through it while measuring the dc drain–source voltage V_{DS} (a 4-point measurement was used). (b) Calorimeter measurements exhibit good agreement with the dc input power, keeping the error ≈ 5%.

thermal grease, which enables a high level of heat extraction in a small form factor [118]. This provides an additional benefit of cooling the active devices, permitting higher power dissipations without approaching critical temperatures. Due to its small size, the cold plate has a small heat capacity, resulting in short measurement times. The calorimeter evaluates the power dissipated on the PCB as

$$P_{\text{calori}} = \rho\, C_{\text{p}}\, u\, \Delta T. \tag{7.7}$$

Here, ρ is the density of the liquid with a specific heat of C_{p}; and u is the flow rate of the liquid. The temperature difference

$$\Delta T = T_2 - T_1 \tag{7.8}$$

between the outlet and inlet water is measured using two thermocouples [see Figure 7.6(b)].

The accuracy of the calorimetric system was verified with a dc calibration as Figure 7.7(a) shows. The power measured with the calorimeter approaches the value of the dc input power within a few minutes, where the error in measurement [see Figure 7.7(b)] is kept around 5% for the whole power range, indicating very good accuracy. The system can measure a wide power range of 20 mW to 10 W; this is especially beneficial as E_{diss} vary quite significantly between different device structures and with f_{sw} [23]. A detailed discussion on the design, operation, and performance of the calorimeter is presented in one of our recent papers [117].[6]

7.4.2 Electrical Measurements

The power inputs to the gate-driver IC and the power circuit are measured with Fluke 87V DMMs, whose average-mode specifications are listed in Table 7.1 [119]. The total gate-driving loss is calculated as

$$P_{\text{in-GD}} = V_{\text{in-GD}} \cdot I_{\text{in-GD}}, \tag{7.9}$$

[6] Remco van Erp, Nirmana Perera, and Elison Matioli, 'Microchannel-Based Calorimeter for Rapid and Accurate Loss Measurements on High-Efficiency Power Converters', in 13th Annual IEEE Energy Conversion Congress and Exposition (ECCE 2021).

Table 7.1: Specifications of Average Measurements Performed with FLUKE 87V DMM

Measurement	Type	Used Range	Resolution	Accuracy[1]
V_{in}	Average	0–600 V	0.1 V	± (0.05% + 1)
$V_{\text{in-GD}}$	Average	0–6 V	0.001 V	± (0.05% + 1)
I_{in}	Average	0–6 A	0.001 A	± (0.2% + 4)
$I_{\text{in-GD}}$	Average	0–60 mA	0.01 mA	± (0.2% + 4)

[1] For a measured value M, a ± (X% + Y) accuracy means an absolute error of ± $[0.01MX + (Y \cdot \text{Resolution})]$. Note: resolution depends on the selected range.

Table 7.2: Specifications of Measurements Carried out with Tektronix MSO68B-Oscilloscope and Probe System

Probe	Bandwidth	Measurement	Type	Used Range
TCP0030A	120 MHz	i_{in}, i_{LOAD}	Total instantaneous	0–5 A
THDP0200	200 MHz	v_{LOAD}	Total instantaneous	0–150 V
TPP1000	1 GHz	v_{DS}	Total instantaneous	0–300 V

Table 7.3: Extra Specifications of the Electrical Probes Used

Probe	Maximum Value (Rated)	Sensitivity	Gain Accuracy	@ 10 MHz[1]	
				Input Impedance	Derating Starts at
TCP0030A	30 A	1 mA	1% (dc, typical)	≈ 0.1 Ω	4 A_{peak}
THDP0200	150 V or 1500 V	-[2]	2% (dc)	≈ 4.8 kΩ	80 V_{RMS}
TPP1000	300 V	-	2.2%	≈ 4.1 kΩ	160–200 $V_{\text{ac-RMS}}$[3]

[1] Values are approximated from the specification-sheet curves.
[2] A vertical resolution can be considered, where Resolution = Full-Scale Range/No. of Bits.
[3] v_{DS} measurement is carried out for a very short duration of time.

where $V_{\text{in-GD}}$ and $I_{\text{in-GD}}$ are measured very accurately according to the measurement technique presented in Section 6.4.

The input power of the converter,

$$P_{\text{in}} = V_{\text{in}} \cdot I_{\text{in}}, \tag{7.10}$$

is evaluated using the same method of average electrical measurements (also see Figure 7.5), where I_{in} is the average value of i_{in}.

The load power is calculated as

$$P_{\text{load}} = V_{\text{LOAD(RMS)}} \cdot I_{\text{LOAD(RMS)}}, \tag{7.11}$$

where the instantaneous load voltage (v_{LOAD}) and instantaneous load current (i_{LOAD}) are measured using a Tektronix THDP0200 voltage probe and a TCP0030A current probe, respectively.[7] The specifications of the current and voltage probes are tabulated in Tables 7.2 and 7.3. For amplitude measurements, the probes and the oscilloscope system retain an error < 3%, up to 30% of its specified bandwidth [120].[8]

[7] We have verified the accuracy of current and voltage measurements by calculating P_{load} using $V^2_{\text{LOAD(RMS)}}/R_{\text{load}}$ and $I^2_{\text{LOAD(RMS)}} \cdot R_{\text{load}}$, where an impedance analyser was used to measure R_{load}. This testing shows that as the load voltage is near-sinusoidal in class-E inverters, both current and voltage probes perform well even at high frequencies such as 10 MHz.

[8] We have verified these details and the practicality of our measurement approach directly with application engineers from Tektronix.

7.5 Loss Breakdown Approach

First, the total power loss in the system and the passive-device loss is evaluated. With P_{in}, $P_{\text{in-GD}}$ and P_{load} available, using Eq. (7.2) and Eq. (7.3) the total power loss in the system is

$$P_{\text{loss-tot}} = P_{\text{in}} + P_{\text{in-GD}} - P_{\text{load}}. \tag{7.12}$$

As P_{active} is directly measured with the calorimeter, the passive-device loss can be calculated according to Eq. (7.1):

$$P_{\text{passive}} = P_{\text{loss-tot}} - P_{\text{active}}. \tag{7.13}$$

The active-device losses are further separated into the four components detailed in Equations 7.4 and 7.6 as follows. First, the total power loss in the transistor is calculated as

$$P_{\text{S}} = P_{\text{active}} - P_{\text{in-GD}}. \tag{7.14}$$

The transistor conduction loss is then separately calculated as

$$P_{\text{con}} = f_{\text{sw}} \cdot R_{\text{DS(on)}} \int^{T_{\text{ON}}} i_{\text{CH}}^2 \, dt, \tag{7.15}$$

where T_{ON} is the ON period of S, which is experimentally measured[9] by observing the v_{DS} waveform (a TPP1000 passive probe was used). The value of $R_{\text{DS(on)}}$ is experimentally evaluated using dc electrical measurements: an example is shown in Figure 7.8 for one of the DUTs. For the ON resistance of GaN devices, dynamic $R_{\text{DS(on)}}$ degradation should be considered when Eq. (7.15) is evaluated [55, 121]. The specific application of this effect to the class-E circuit is discussed in Section 7.7.3. The instantaneous channel current for the ON state of S is obtained as

$$i_{\text{CH}} \quad = \quad i_{\text{in}} - i_{\text{LOAD}} - (i_{\text{C}_\text{o}} + i_{\text{C}_\text{e}}), \tag{7.16}$$

to be used in Eq. (7.15). And since no current passes through C_{o} or C_{e} as $v_{\text{DS}} = 0$ V in ON state, we get

$$i_{\text{CH}} \quad = \quad i_{\text{in}} - i_{\text{LOAD}}. \tag{7.17}$$

Using Eq. (7.4), finally, the hysteresis energy loss of C_{o} is calculated as

$$E_{\text{diss}} = \frac{P_{\text{S}} - P_{\text{con}}}{f_{\text{sw}}}. \tag{7.18}$$

One could consider using the multiplication of instantaneous shunt-capacitance current ($i_{\text{C}_\text{o}} + i_{\text{C}_\text{e}} = i_{\text{in}} - i_{\text{LOAD}}$ in OFF state) and voltage (v_{DS}) waveforms for the duration of the OFF period to evaluate E_{diss}. As this approach takes the difference of two similar values (as v_{DS} is always positive and the current crosses zero at V_{p}—see Figure 7.4), it could result in a large error,[10] especially at high f_{sw}, for which the switching periods are in the range of probe propagation-delay times.

[9] This could also be approximated with the duty ratio and the switching frequency values. However, we used the experimental approach for better accuracy.

[10] The significance of the error is dependent on f_{sw} and the voltage and current probe characteristics. The input impedance of the voltage probe, which is frequency-dependent, is an important factor here as a certain amount of device-branch-current could pass through it. These factors require further investigations.

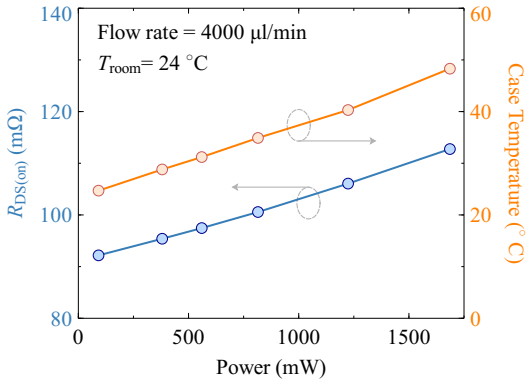


Figure 7.8: Device's dc ON-state resistance ($R_{DS(on)} = V_{DS}/I_{DS}$) is experimentally determined using 4-point dc measurements to calculate the conduction loss for the case where S is a GS66504B GaN HEMT—see Eq. (7.15). The case temperature of S, measured with an IR camera, is also indicated.

We use the techniques presented in Chapter 6 to separate the gate-driving losses into $P_{\text{GD-NL}}$ and P_{G}—see Eq. (7.6). $P_{\text{GD-NL}}$ is individually evaluated by measuring the gate-driving loss on a replica of the PCB used for the DUT, but without soldering the transistor S. Then, when the gate-driver is switched at f_{sw}, its measured input power solely represents $P_{\text{GD-NL}}$. Consequently, the device gate-loss is evaluated as

$$P_{\text{G}} = P_{\text{in-GD}} - P_{\text{GD-NL}}. \tag{7.19}$$

7.6 Experimental System and Procedure

In our study, we consider two *cases* for experimental evaluation as tabulated in Table 7.4. For *Case 1*, we selected a GaN Systems GS66504B e-mode GaN device as the power transistor, whereas *Case 2* uses a Transphorm TPH3212PS cascode GaN device. A Texas Instruments UCC27511A IC was used as the gate driver for both designs. The details of these devices are listed in Table 7.5. Case 1 targets a 10-MHz switching frequency. However, this was limited to 5 MHz for case 2 (due to increased hysteresis losses).

The passive components were calculated using the design equations derived by Sokal [44] and the final tuned values are tabulated in Table 7.6, alongside external gate-driver resistance values. The external shunt-capacitance C_{e} and series-filter capacitance C_{r} are multi-layer-ceramic (MLC) capacitors with a C0G (NP0) dielectric and have high quality-factors. The load resistance has a temperature

Table 7.4: Details of the Two Case Designs

Case	Transistor	Frequency (MHz)	V_{p} range (V)	V_{drive} (V)	Gate Driver
1	GS66504B	10	100–300	5	UCC27511A
2	TPH3212PS	5	100–300	8	UCC27511A

Table 7.5: Specifications of the Active Components

Component	Designation	Part No.	Specifications
Transistors	S	GS66504B	650 V, 15 A, 100 mΩ, GaN*PX* package
		TPH3212PS	650 V, 27 A, 72 mΩ, TO-220 package
Gate driver	GD	UCC27511A	Split output, 4.5–18 V, 4-A source,8-A sink, SOT-23 (6) package

Table 7.6: List of Passive Components

Component	Value	Unit	Used in Case	Remarks
R_{GH}	4.7	Ω	1,2	0402 package, 1/5 W, 1%
R_{GL}	1	Ω	1,2	0402 package, 1/5 W, 1%
R_{load}	25	Ω	1	Ohmite TGHMV25R0JE, ±100 ppm/K, 0.23 °C/W, #187 tab terminals
	10	Ω	2	Ohmite TGHMV10R0JE, ±100 ppm/K, 0.23 °C/W, #187 tab terminals
L_{RFC}	10.8	μH	1,2	Air core, at 10 MHz, quality factor = 300
L_r	4.44	μH	1	Air core, at 10 MHz, quality factor = 343
	9.27	μH	2	Air core, at 5 MHz, quality factor = 262
C_r	56.9	pF	1	NP0 MLC capacitors, 1111 package
	112	pF	2	”
C_e	0–40.5	pF	1	”
	0–150	pF	2	”

Notes: C_e and C_r are high-Q / low-ESR non-magnetic multi-layer ceramic (MLC) capacitors with a C0G (NP0) dielectric, from Johanson Technology (E-series). L_{RFC} and L_r are made with 20-AWG and 14-AWG magnet wires, respectively. Inductance and quality factor values are measured with a Keysight 4990A impedance analyser and a 16047E test fixture. $L_{path\text{-}2}$ (Figure 7.3) was measured to be around 410–420 nH at 10 MHz.

coefficient of resistance (TCR) of 100 ppm/K, and thus, its variation within the operating temperatures here is negligible. The implementation of the circuit and the complete measurement system is shown in Figure 7.9.

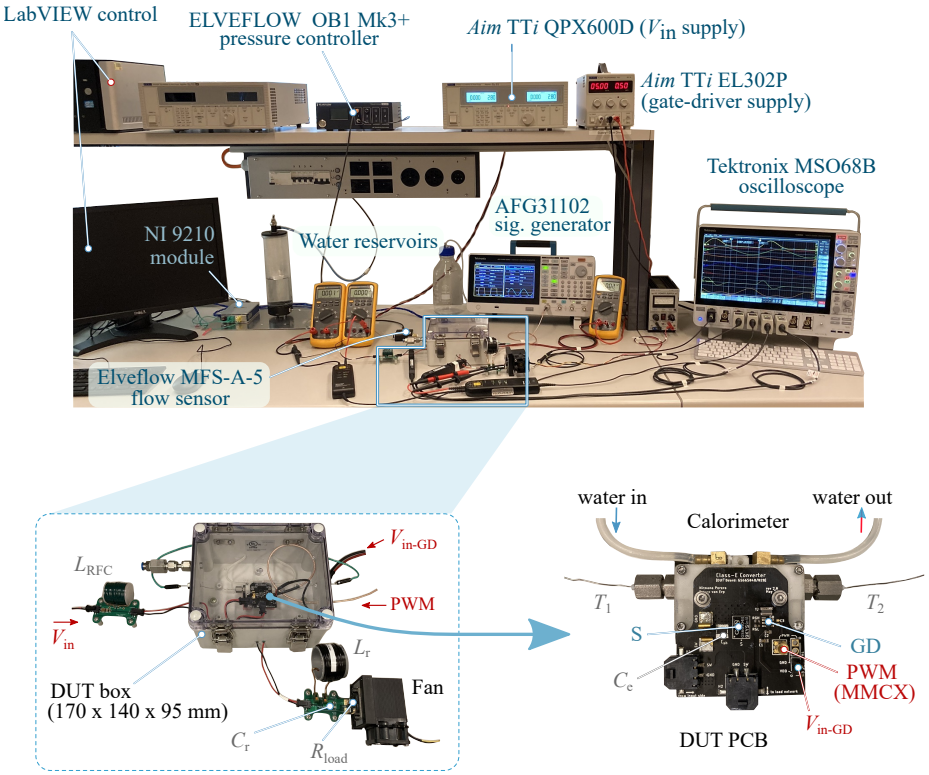


Figure 7.9: Complete experimental system highlighting the measurement equipment and probes, calorimeter control system, class-E inverter circuit components, and the PCBs. The two active devices in the circuit (S and GD) and C_e are built into a separate DUT PCB. A Tektronix AFG31102 signal generator is used to generate the PWM signals. For P_{active} measurement, a LabVIEW-based control system is utilized: set the flow rate using a pressure controller, read the actual flow rate using the flow sensor; record the thermocouple readings T_1 and T_2; calculate P_{active} in real-time.

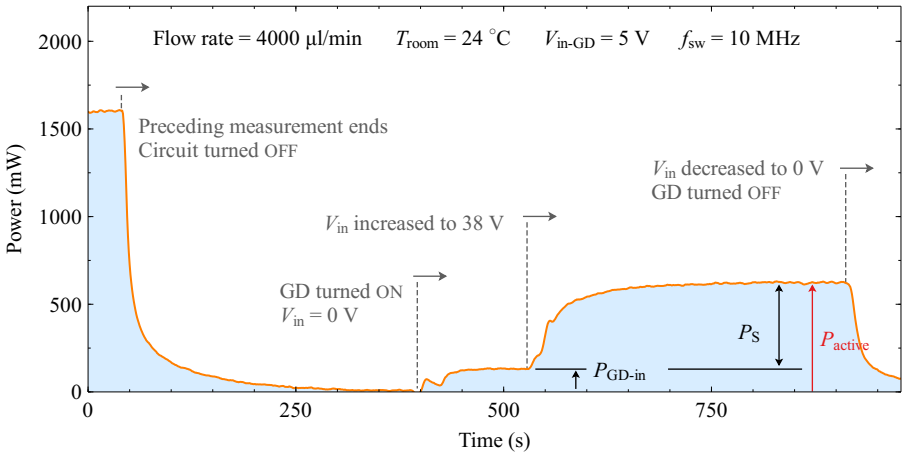


Figure 7.10: Example showing the application of the developed calorimeter to measure P_{active} of the designed class-E inverter: the distinction between the gate-driving loss and the transistor losses is also observed.

An example of using the calorimeter to measure P_{active} is presented in Figure 7.10. The related experimental procedure is summarized as follows.

1. Allow the DUT board to cool down from a preceding measurement.
2. Then, the gate-driver circuit is turned ON and PWM is applied while $V_{in} = 0$ V.
3. Next, V_{in} is gradually increased to the target value.
4. Once the thermal steady state is reached, the value of P_{active} is recorded.

One major aim of this study was to evaluate E_{diss} as a function of V_p for a given transistor. This was achieved by varying the input voltage of the circuit. We considered V_p values of 100 to 300 V, at 50 V steps. The ZVS conditions were maintained by changing the value of C_e for $V_p \geq 200$ V, while $d = 0.5$ was maintained. For $V_p \leq 200$ V, C_e was 0 and d was slightly adjusted from 0.5 to achieve ZVS conditions.

7.7 Results and Discussion

Figure 7.11(a) shows the total input power and the load power for different V_{in} values for Case 1, where S is a GS66504B device. The input power was 102.6 W for $V_{in} = 81.4$ V, which corresponds to a V_p of 300 V. Figure 7.11(b) shows the breakdown of the corresponding power losses in the converter into passive-device, transistor, and gate-driving losses. The passive-device losses are predominant and increase with the input power due to the increased average current in L_{RFC} and RMS current in L_r. The latter is responsible for the largest contribution as it is subjected to a large ac current, hence, increasing its ac winding loss; on the other hand, L_{RFC} experiences a relatively small ac ripple as the input current is nearly dc in the topology.

Figures 7.12(a) and 7.12(b) show the corresponding power components for Case 2 (S is a TPH3212PS device). Here, for a V_p of 300 V and f_{sw} of 5 MHz, an input power of 71.4 W was observed for $V_{in} = 81.8$ V. The relatively large difference between $P_{in\text{-}tot}$ and P_{load} in Figure 7.12(a) is due to the increased power dissipation in the transistor as shown by Figure 7.11(b); the reasons are discussed in Section 7.7.3.

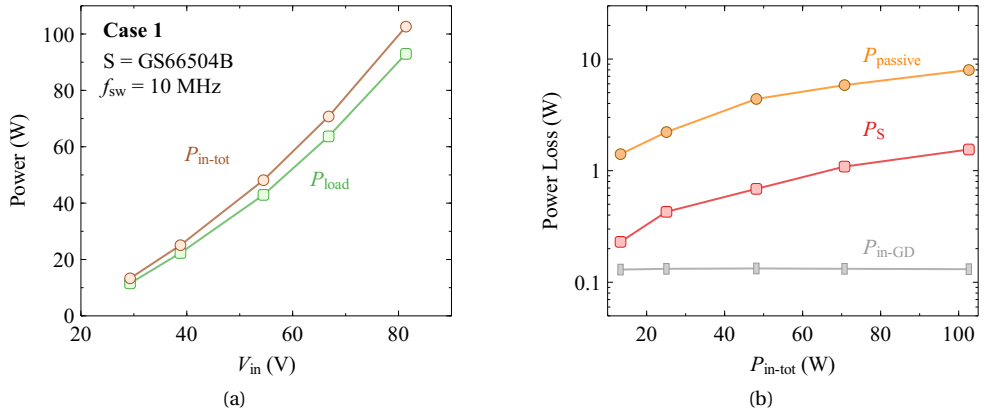


Figure 7.11: Experimental results for the class-E inverter designed for Case 1: f = 10 MHz; S = GS66504B; GD = UCC27511; V_{drive} = 5 V. (a) Variation of the total input power, $P_{in\text{-}tot}$, and the load power, P_{load}, with input voltage. (b) Breakdown of the losses with $P_{in\text{-}tot}$: the gate-driving loss $P_{in\text{-}GD}$, transistor loss P_S and passive-device losses $P_{passive}$. The presented method is capable of measuring mW-range power levels, enabling accurate loss and efficiency calculations.

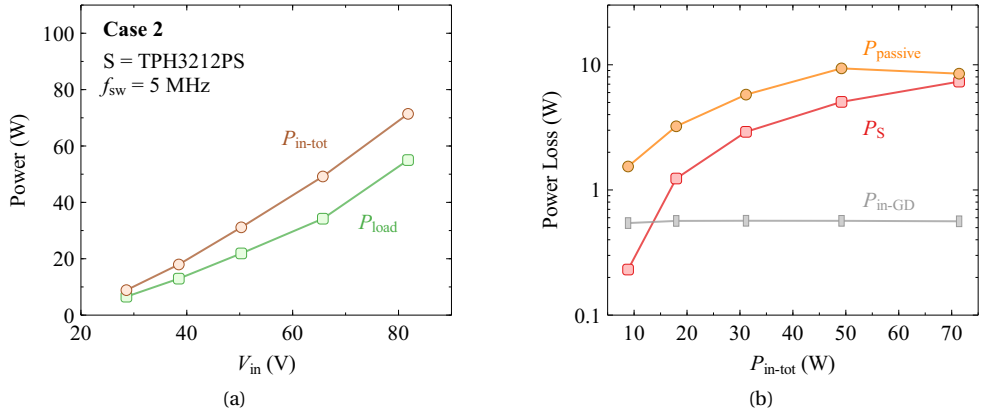


Figure 7.12: Experimental results for the class-E inverter designed for Case 2: f = 5 MHz; S = TPH3212PS; GD = UCC27511; V_{drive} = 8 V. (a) Variation of the total input power, $P_{in\text{-}tot}$, and the load power, P_{load}, with input voltage. (b) Breakdown of the losses with $P_{in\text{-}tot}$: the gate-driving loss $P_{in\text{-}GD}$, transistor loss P_S and passive-device losses $P_{passive}$.

In addition, for both cases, we observe that V_p/V_{in} is around 3.67 at the full power conditions, which agree quite closely with the *optimum class-E operation* value of 3.56, calculated by Raab [107].

7.7.1 Gate-driving Losses

The gate-driving loss $P_{in\text{-}GD}$ stays constant for both cases. The loss is approximately around 120 mW [see Figure 7.11(b)] for case 1, whereas this is around 500 mW for case 2. The fixed nature of gate-driving loss is expected as f_{sw} was fixed and ZVS conditions were maintained at each power level. Based on the measurement concepts presented in Section 7.5, this loss is divided into $P_{GD\text{-}NL}$ and P_G in Figure 7.13 for both cases, where a wide switching frequency is investigated. For Case 1, the loss distribution is such that $P_{GD\text{-}NL}$ = 52.7 mW and P_G = 71.1 mW at 10 MHz. In other words, for the combination of S and GD in Case 1, $P_{GD\text{-}NL}$ amounts to 40% of the total gate-driving loss. For comparison, results for Case 2 are shown in Figure 7.13(b). Here, $P_{GD\text{-}NL}$ amounts to only 10–12% of the total gate-driving loss

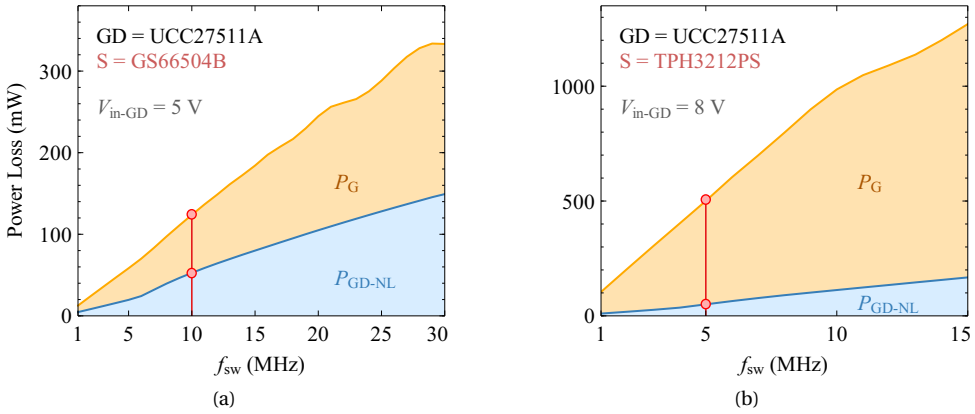


Figure 7.13: Distribution of gate-driving loss components (hard-gating) with f_{sw} for two different transistors. In MHz-range and high-efficiency resonant power converters, the gate-driver loss cannot be neglected. For the GS66504B device, $P_{\text{GD-NL}}$ is around 40% of $P_{\text{in-GD}}$. Relevant equations are $P_{\text{in-GD}} = P_{\text{G}} + P_{\text{GD-NL}}$ and $P_{\text{G}} = P_{\text{G-ON}} + P_{\text{G-OFF}}$.

as the power transistor has a much higher input capacitance in comparison with the driver's effective output-stage capacitance.

7.7.2 Transistor Conduction Losses

Referring to Figure 7.11, it is observed that the losses in the transistors also increase with $P_{\text{in-tot}}$ for both cases. This is due to two reasons. On the one hand, the conduction loss increases with V_{in} (or $P_{\text{in-tot}}$) because of the increased RMS current through S—note that $R_{\text{DS-on}}$ of S does not vary significantly (stays around 90-110 mΩ for GS66504B device and 70–90 mΩ for TPH3212PS device) for the considered power-dissipation ranges [see Figure 7.8]. On the other hand, the OFF-state loss increases with V_{in}, or more specifically with V_{p}, due to the hysteresis loss that occurs in C_{o} while it is being charged and discharged during the OFF-state in each cycle, which is discussed next.

7.7.3 Output-Capacitance Losses

Our approach for calculating E_{diss} in the class-E circuit requires the conduction loss of the device [see Eq. (7.18)]. Therefore, before C_{o}-hysteresis loss results are discussed, some explanation should be provided concerning the dynamic $R_{\text{DS(on)}}$ degradation reported in certain GaN HEMTs, as it directly affects the conduction loss.

On the one hand, some manufacturers do not report any details related to dynamic $R_{\text{DS(on)}}$ degradation in their datasheets, which is the case for the GS66504B device. However, for the TPH3212PS device, the manufacturer reports an effective $R_{\text{DS(on)}}$ value, $R_{\text{DS(on)}}$(eff), considering these effects. On the other hand, recent works have reported that for soft-switching circuits, dynamic $R_{\text{DS(on)}}$ shows a smaller degradation in contrast to hard-switching circuits [121, 122]. However, such studies do not consider the specific OFF-state conditions imposed on the switch by the class-E circuit.

To investigate this, for case 1 with the GS66504B device, we have considered the effect of an increase up to 20% in the measured dc $R_{\text{DS(on)}}$ value, based on recent works [122]. Figure 7.14(a) plots the corresponding E_{diss} values, where $R_{\text{DS(on)}}$ in Eq. (7.15) is multiplied by a positive factor k_{dyn} to

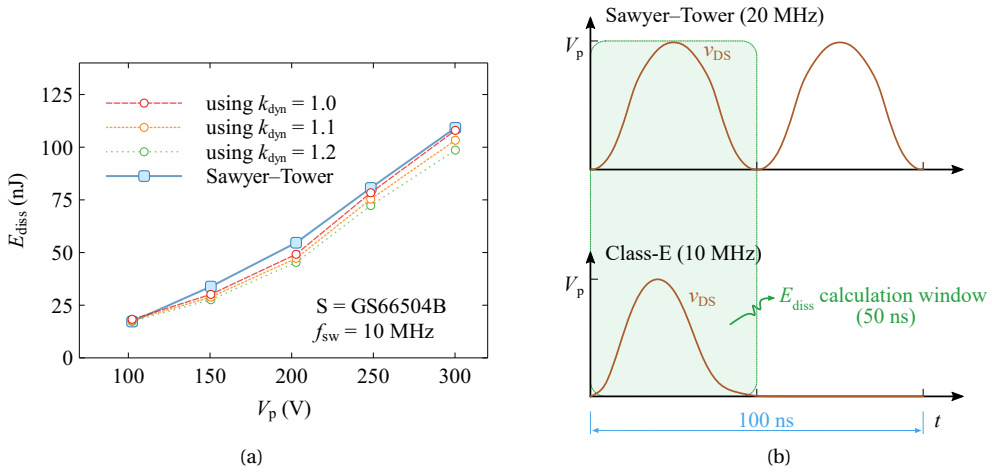


Figure 7.14: (a) Variation of output-capacitance hysteresis losses with V_p for the GS66504B transistor in actual converter operation at 10 MHz. k_{dyn} = 1.0, 1.1 and 1.2 correspond to 0, 10, and 20% increase in the $R_{DS(on)}$ value (measured in dc conditions) to investigate dynamic $R_{DS(on)}$ effects. The corresponding Sawyer–Tower results are marked in solid blue (from Zulauf et al. [17]). (b) The v_{DS} waveform of a class-E inverter at 10 MHz with d = 0.5 has a 50 ns of charge–discharge time for C_o; this corresponds to a Sawyer–Tower excitation at 20 MHz.

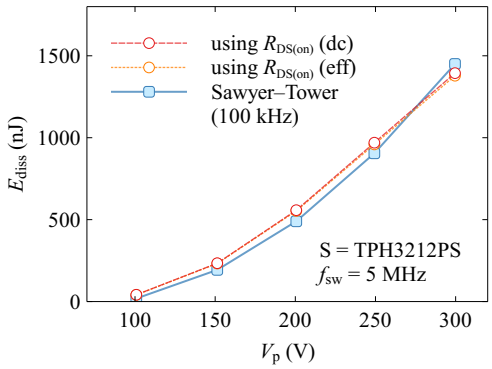


Figure 7.15: Variation of output-capacitance hysteresis losses with V_p for the TPH3212PS transistor in actual converter operation at 5 MHz.

evaluate P_{con}. The corresponding Sawyer–Tower results, reported by Zulauf et al. [17], are also marked (in solid blue). The comparison reveals that, as the value of k_{dyn} increases, the measured E_{diss} value deviates from the Sawyer–Tower results, suggesting that dynamic $R_{DS(on)}$ degradation is much smaller in a class-E circuit compared to other circuits [55, 121]. This could be explained by the short duration of the peak OFF-state-voltage in a class-E circuit, which can create different charging dynamics during the OFF state; however, more studies are needed to understand such effects.

Another very important point should be highlighted here. Note that although the class-E circuit operates at f_{sw} of 10 MHz (T_{sw} = 100 ns), the actual charging–discharging event of C_o corresponds to a duration of 50 ns (for d = 0.5), or an effective frequency of 20 MHz [see Figure 7.14(b)]. Therefore, the Sawyer–Tower results at 20 MHz should be used for comparison. This is important as most GaN devices show a frequency dependence for E_{diss} [17, 23].

Moving into the TPH3212PS device (Case 2), hysteresis losses are considered in Figure 7.15. The dashed lines show the results obtained with Eq. (7.18) using two different approaches. The first method

uses $R_{DS(on)}(dc)$ value in Eq. (7.18): $R_{DS(on)}(dc)$ values were measured using the same technique that was used for the GS66504B device. The second method uses $R_{DS(on)}(eff)$ value in Eq. (7.18): as mentioned earlier this value is provided in the device datasheet.[11] Moreover, our Sawyer–Tower results from Chapter 4 indicated that this particular cascode-GaN-device exhibits a relatively large frequency-independent hysteresis loss. Therefore, for the Sawyer–Tower results in Figure 7.15, we have multiplied the E_{diss} value at 100 kHz (for each V_p value) by 50 to get the corresponding E_{diss} values at 5 MHz. Here again, the Sawyer–Tower results and measured results show very good agreement.

In addition, for both cases, C_e is subjected to the same voltage swing as C_o. Since C_e was chosen to have a low equivalent-series-resistance (ESR), any ESR losses can be assumed negligible for the considered RMS current through the device branch; this assumption was validated by the observation of insignificant temperature rise in C_e during the circuit operation for all power levels.

7.7.4 Complete Loss Breakdown of Active Devices

For the full power operation modes of the two cases, Figure 7.16 breaks down the active-device losses into the four main components described in Eq. (7.4) and Eq. (7.6). The results reveal that for Case 1, P_{diss} dominates active-device losses with a contribution of 64.28%, which amounts to 1.08 W; this is 88.23% (6.97 W) for Case 2.[12] This observation demonstrates the major implication of output-capacitance hysteresis losses in MHz-range operation, inhibiting the ideal advantages of zero switching-losses (or OFF-state losses) offered by soft-switching operation. It is also important to note

[11] In the TPH3212PS device datasheet, this is given as a normalized resistance curve with junction temperature. First, we interpolated the corresponding normalized resistance values for actual operating temperatures in our circuit. Then, the resulting normalized values were multiplied with the typical $R_{DS(on)}(eff)$ given in the datasheet tables (at 25 °C).

[12] The almost 90% contribution of P_{diss} for Case 2 is also due to the fact that the circuit operates at a moderate load current. At higher output powers, but at the same V_p conditions, the contribution of P_{diss} is expected to drop. However, our aim here is to show that, at the tested output power (which is an acceptable power level), P_{diss} loss is significant.

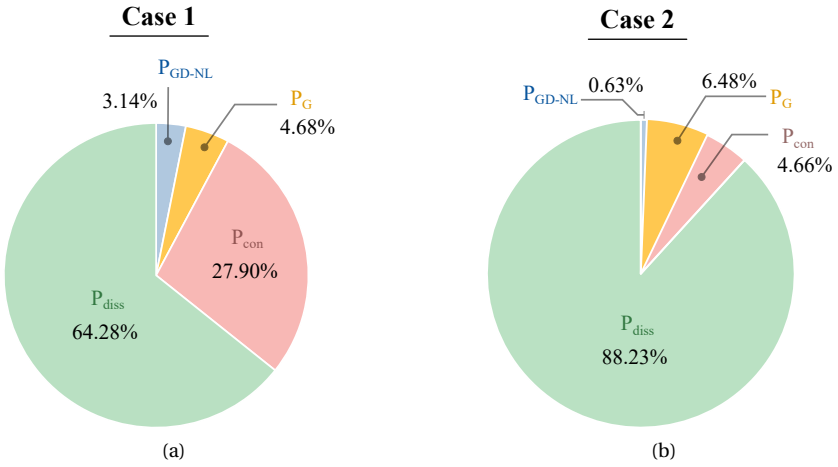


Figure 7.16: Complete breakdown of the active-device power losses (average) in the tested class-E inverters. The total active-device loss P_{active} is distributed between the gate-driver internal loss $P_{GD\text{-}NL}$, gate loss P_G, transistor conduction loss P_{con}, and C_o-hysteresis loss P_{diss}. (a) Case 1: P_{active} = 1.68 W, total input power $P_{in\text{-}tot}$ = 102.6 W and V_{in} = 81.4 V; S is a GS66504B GaN HEMT and GD is a TI UCC27511A IC. C_o-hysteresis loss is the major contributor accounting for 64.28% of losses. (b) Case 2: P_{active} = 7.9 W, $P_{in\text{-}tot}$ = 71.4 W and V_{in} = 81.8 V; S is a TPH3212PS GaN HEMT and GD is a TI UCC27511A IC. C_o-hysteresis loss is again the major contributor accounting for 88.23% of losses. These results are based on in-circuit measurements (without using any estimation based on indirect measurements) and therefore represent actual operating losses.

that the gate-driving losses in total amount to 7.82% of P_{active} for Case 1 and where it is 7.11% for Case 2, which are not negligible.

7.7.5 Overlook

We have provided a comprehensive breakdown of active-device losses in this Chapter. This aids the power electronic circuit designer to identify the causes of power losses and also to choose the best transistor and gate-driver IC combination for the most favourable design. The measurement approach can be extended to other resonant converter circuits, but the complexity depends on the topology. For example, in an LLC half-bridge resonant converter [123], the temperature rise in the PCB is due to the power dissipation of two transistors. A single gate-driver can be used by employing a bootstrap method for direct $P_{\text{in-GD}}$ measurement. And dead-time should not extend much beyond the required minimum value to avoid errors in conduction loss calculations.

7.8 Summary

We have demonstrated a complete loss-breakdown concept for a class-E inverter. The presented ideas allow comparing and separating the active-device losses into transistor ON- and OFF-state losses, as well as gate and internal-gate-driver losses. An experimental method with mW-level precision is presented and utilized to measure these losses. The approach provides an accurate and in-converter evaluation of the hysteresis losses related to the output capacitance of transistors. It was shown that the distinction between the transistor-related gate loss and the driver-related internal loss is also important for the loss characterization of MHz-range converters.

8 Conclusion and Future Directions

8.1 Summary

With energy-efficient power conversion as the general theme, in this thesis, we investigated the losses created by the parasitic output capacitance of power FETs in switching events. Broad investigations were carried out on both soft-switching and hard-switching events. In addition, gate-driving losses were revisited, and important loss contributions were identified for megahertz-range hard-gating conditions. Finally, a case study was presented to demonstrate important loss contributions for soft-switching converters operating in HF and VHF ranges.

8.2 Conclusions and Outlook

With the new possibilities enabled by WBG semiconductor devices, existing topologies are being pushed to higher switching frequencies. We believe soft-switching topologies will eventually only operate in megahertz ranges for high-power-density applications, and the ones already operating in this range will further push their operational frequencies. One major hindrance to this would be the output-capacitance hysteresis energy loss: the power loss simply scales with the operational frequency. Although several publications have presented root causes for these losses [18, 21, 22, 72, 74, 124], they are still being understood even for the mature Si devices [125]. Therefore, it is paramount that device manufacturers acknowledge these losses and seek device-level solutions. At the time of writing, to the best of our knowledge, these losses are not reflected in device datasheets as quantitative values or in device SPICE models. As our results have shown, output-capacitance hysteresis is highly dependent

on operational parameters as well as device structure; thus, deriving a generalized SPICE model of a FET that reflect these losses is challenging. Recent research works have also tried to model these losses in circuit-level simulations. [71, 126, 127]. We believe, SPICE models need to be structure-specific to derive fast models that are still capable of incorporating the hysteresis losses.

The operating frequency of hard-switching circuits will also be pushed; the frequency limit is mainly dependent on the switching losses. As losses due to *VI* overlap tend to decrease with higher switching speeds, especially with the capabilities of WBG devices, the ultimate bottleneck would be the $Q_{\mathrm{o}}V_{\mathrm{dc}}$ loss component related to device output capacitance at the device turn-ON. This also highlights the importance of topological distinction for the correct understanding of loss contributions.[1] As our results have shown for the first time, for some devices, the datasheets do not reflect the correct $Q_{\mathrm{o}}V_{\mathrm{dc}}$ for actual large-signal operation under hard-switching. This could lead to a significant difference in loss predictions when a multitude of devices are hard-switched in converters such as multi-level converters or magnetic-less switched capacitor converters. A good research endeavour would be to identify module- or cell-level loss indicators for these high-level converters.

Based on our work on both hard-switching and soft-switching topologies, we believe more attention should be given to the dynamic characterization of power FETs under large-signal operation. Device datasheets mainly concern dc characteristics and small-signal conditions. The main large-signal data given, in certain cases, is the switching energy values for inductive-load testing, under a selected set of conditions. Additional large-signal characteristics would be highly beneficial for power electronics designers for accurate loss predictions.

As the switching frequency is being pushed towards the megahertz range, gate-driving losses also become important. As our work in chapter 6 showed, for certain driver and power-device combinations the switching loss in the driver become as important as the device gate loss. As integrated power module solutions are being sought, the design of the driver output stage needs to be revisited.[2] This would be an extremely challenging task, as the higher switching speeds of WBG devices demand driver stages that could sink and source large peak currents. These peak currents need to be supplied for a shorter period, but with a very high repetition rate. Currently, to the best of our knowledge, the peak current values for high switching frequency applications lie between 1–10 A. To support the requirements of WBG devices, these limits also need to be increased.[3] Another challenging task for high switching speeds would be the mitigation of EMI noise created by extremely fast switching transitions (below 10 ns for state-of-the-art GaN devices). New solutions for clean switching will be essential and existing gate-driving approaches may need to be revised, going beyond traditional hard-gating and resonant gate-driving solutions.

8.3 Additional Future Directions

Here we discuss some additional directions for future research work.

- Our case study in Chapter 7 suggested that dynamic-$R_{\mathrm{DS(on)}}$-degradation effects of GaN devices could manifest differently under soft-switching operation. In addition, the conditions in standard pulsed-IV testing are far from conditions in actual converter operations, may it be hard-switching

[1] Complex analytical equations may accurately recreate and represent an observation, but more often than not, a simple approach will yield high-value insights that will help to develop a better design.

[2] For example, Navitas, Power Integrations, Texas Instruments, EPC, and STMicroelectronics are pursuing such integrated solutions.

[3] For discrete solutions, resonant-gate driving could be a solution where applicable.

or soft switching. This is another instance that shows the importance of topological distinction for large-signal and dynamic characterization of device properties. We believe investigations on dynamic-$R_{\mathrm{DS(on)}}$-degradation effects with a measurement technique that resembles actual soft-switching conditions would be essential for sound conclusions.

- The experimental results from chapter 5 showed that the output charge value (for a given drain–source voltage) in hard-switching operation could significantly differ from the values predicted from datasheet curves or the results from the Sawyer–Tower circuit. The exact reasons for this behaviour are not clear and require a device-level investigation. A root-cause analysis on this would yield important details on improving the performance of the device structures from the design stage.

- In our measurement techniques used in hard-switching loss characterization (Chapter 5), we employed a dc-power calibration stage. There, we observed different stabilization times and trends when GaN power FETs were operated in the first quadrant (positive drain–source voltage and the device is in ON-state) and in reverse conduction (negative drain–source voltage and the device is in OFF-state) mode. In our experiments, depending on the GaN HEMT type we had to alter between these two modes and constant current or voltage modes of the dc power supply to achieve stable power dissipations. Additional studies on the reverse conduction of the emerging GaN HEMTs would be beneficial for future device characterizations based on thermal techniques.

- As the switching frequencies approach the megahertz domain, a limitation could be reached in the practical generation of PWM with digital control. On the one hand, the employment of an accurate dead-band would become increasingly difficult as switching periods start to go below 1 μS. Eventually, a limit would reach in achieving the desired duty ratio with enough accuracy as the turn-ON time approaches the resolution of the PWM module of the digital signal processor. It would be interesting to analyse the existing technical limit for these parameters and identify possible solutions to overcome them.

- As it was highlighted in Section 8.2, the gate-driving process will require improvements for both discrete and integrated solutions. Additional studies on suitable driving topologies from a topological point of view would be beneficial. At the same time, the output stage of the gate driving ICs will require improvements. This could be approached from two perspectives: improving the output-stage transistors or employing new topologies in the output stage. Our results and methods from Chapter 6 could be a good starting point to identify performance limitations in existing gate-driver ICs.

A Acknowledgements: Technical

1. For the use of device capacitance-related definitions from IEC 60747-8:2010 document in Sections 2.2.1 and 6.2.2 in this thesis:

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2. Free/Open-Source-license software

   - **Lyx**: used for the typesetting of the thesis.
   - **Texstudio**: used for the typesetting of conference and journal publications.
   - **WebPlotDigitizer**: used for the digitization of datasheet curves.
   - **Veusz**: used for plotting data from experiments and simulations.
   - **Inkscape**: used for creating the diagrams/illustrations presented throughout the thesis.
   - **Zotero**: used for the organization of references.

3. Other software

   - **LTspice**, freeware: used for all the SPICE simulations carried out in my research works. Analog devices distribute this tool for free.

- **Autodesk Eagle**: used for the creation of PCB schematic and layout files. Since January 2020, Eagle is distributed with Fusion 360. Students and educators can get a free license to use the software.
- **PLECS**: I would like to thank Samuel Güttinger from Plexim GmbH for providing a free student license of PLECS. I used the TI C2000 Target Support Package from PLCES to program the F28379D MCU from Texas Instruments.

Nirmana Perera

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Nirmana **Perera**

Power Electronics Engineer and Researcher

Lausanne, **Switzerland**

Experience

2017–2022 | **Doctoral researcher**, Power and Wide-bandgap Electronics Research Lab, EPFL, Switzerland
- Hardware design and testing of switching power converters (kHz and MHz range).
- Investigation and measurement of power losses in power converters.
- Development of electrical and calorimetric techniques to characterize power semiconductor devices.
- Supervision of 3 undergraduate projects, 6 master's projects and 1 master's thesis.
- Establishing the power electronics section of the lab (grant writing, equipment selection and testing).

2017–2018 | **Electrical designer**, EPFL Team, **SpaceX Hyperloop Competition** - 2018, California, USA
Design of the low-voltage electrical system and the electronics of the hyperloop pod.
- Planning and hardware implementation of the 24-V electrical system in the pod.
- Electrical wiring between the main control unit and peripheral units (sensors, batteries, actuators).

2017 | **Research intern**, Power and Wide-bandgap Electronics Research Lab, EPFL, Switzerland
- Design of boost converter topologies for an autonomous LED street lighting system.

2015–2017 | **Lecturer**, University of Peradeniya, Sri Lanka
- Teaching undergraduate and graduate courses in electrical engineering: Power Electronics, Electronic Circuits, AC Machines, Power Electronic Applications and Design.

2013–2015 | **Research and teaching assistant**, University of Alberta, Canada
- Design of SiC-based versatile inverter-leg modules.
- Implementation of a soft-starting scheme for 3-phase induction motors using dSPACE.
- Instructed the laboratory sessions for the undergraduate course Variable Speed Drives.

2011–2012 | **Teaching assistant and instructor**, University of Peradeniya, Sri Lanka
- Designed and conducted lab sessions for undergraduate courses in electrical engineering.

Education

2017–2022 | **Doctor of Philosophy** in *Electrical Engineering*
École Polytechnique Fédérale de Lausanne, **Switzerland**
Thesis title | Hard and Soft Switching Losses in Power Converters: Role of Transistor Output Capacitance

2013–2015 | **Master of Science** in *Energy Systems, and Electrical and Computer Engineering*
University of Alberta, Edmonton, **Canada**
Thesis title | DSP based Realization of Pre-Processed Discontinuous PWM Schemes for 3-Limb-Core Coupled Inductor Inverters

2007–2011 | **Bachelor of Science** *in Electrical and Electronics Engineering*
University of Peradeniya, **Sri Lanka**
First Class Honours, GPA – 3.9/4.0, Class rank – 5 (out of 100 students)

Research Projects and Designs

Performance evaluation of Si and wide-bandgap (WBG) power devices 2017–2022

The goal of this research was to investigate the losses created by the output capacitance of field-effect transistors in switching power converters. All three prominent FET technologies were investigated: Si (planar and super-junction), SiC and GaN.

- Analysis and development of novel electrical and electronic circuits to understand the behaviour of device output capacitance in actual hard- and soft-switching conditions.
- Development of a 10-MHz class-E inverter (up to 100 W) and performing a complete breakdown of the active-device losses in the circuit.

Gate-driver design in MHz range 2020–2021

Studied the capabilities of state-of-the-art gate drivers in driving GaN, SiC and Si FETs in HF and VHF ranges.

- Devising a new electrical technique to separate the gate-related and driver-related losses.
- Design of the measurement system and testing the maximum limits of the gate drivers (from 1 to 60 MHz).

Design of dc-dc converters facilitated by in-chip liquid cooling (Collaboration) 2020–2022

A GaN-based high-power-density 32nd-brick 48/24 V Buck Converter (at 1–2 MHz and 350 W) was developed. The work demonstrates the advantages of integrated liquid cooling by embedding microchannels in the silicon substrate of the device.

- PCB design of the converter (device: EPC 2152 80-V, 15-A ePower^{TM} Stage) using Fusion 360 Electronics Design.
- Implementation of the control and electrical testing of the converter.

High-frequency pulse generator (Collaboration) 2019

A GaN-based pulse generator was developed to drive a nanoplasma switch to achieve pulse sharpening. The power devices were TI 600-V LMG3410R070 GaN ICs. A 4-layer PCB was designed using Autodesk Eagle.

- Design, implementation and testing of the 10-MHz half-bridge circuit.
- Control of the half-bridge using a C2000 TMS320F28379d MCU.

3-phase inverter system 2014–2015

Realization of a Coupled-Inductor Inverter (CII) utilizing Discontinuous PWM (DPWM).

- Design and testing of inverter-leg modules (based on SiC MOSFETs).
- Design of the main control board and analogue interface boards.
- Formulation of DPWM schemes in a TI TMS320F28335 MCU using the VisSim software package.

Embedded Systems Projects 2007–2012

- Temperature-sensing digital data logger (PIC 16F84A MCU, I^2C, assembly language).
- Sound-following pet robot (PIC 16F877A MCU, motor control, sound detection).
- SMS-based home automation system: interfaced a PIC MCU with a commercially available mobile phone to control electrical lights in a model house with the use of standard SMS messages.

Scientific Publications

Journals **16** including *IEEE Transactions on Power Electronics*, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, and *IEEE Transactions on Industry Applications*

Conferences **22** including *ECCE*, *ECCE-Asia*, *COMPEL*, *THERMINIC* and *IECON*

Technical Skills

Practical Troubleshooting	Soldering, active and passive device selection, electrical and thermal measurements All aspects including circuits, devices, gate driving, signals, modulation, and control
PCB Design Tools	Autodesk Eagle, Autodesk Fusion 360 Electrical Design, Altium Designer, Proteus
Simulation Software	*LTSpice*, PLECS, MATLAB Simulink, Saber RD, Cadence PSpice
Hardware Control	TI C2000 MCUs with Code Composer Studio, PLECS and VisSim; dSPACE; PIC MCUs
Equipment	Oscilloscope systems and probes (Tektronix, Lecroy), function generators (Tektronix, Keysight), voltage amplifiers, curve tracers (Keysight), device probe-stations, impedance analysers (Keysight, GW Instek), thermal imaging (QFI IR microscope, Fluke)
Programming	C++, Embedded C, Python, Assembly
Word Processing	LaTeX, Lyx, TeXstudio, MS office, Pages
Other Software	Confluence, PTC Mathcad, Zotero, Inkscape, Veusz, Origin Pro

Competitions and Team Achievements

July 2018	**3rd Place**, SpaceX Hyperloop Competition, California, USA.
2011	**Finalist, International Future Energy Challenge 2011 (IFEC 2011)**, organized by IEEE Power Electronics Society, held at University of Michigan-Dearborn, Michigan, for developing a "Low-Cost Lithium-ion Battery Charger for Automotive and Renewable Energy Applications".

Languages

Sinhala (native), English (fluent)