Active-Device Losses in Resonant Power Converters: A Case Study with Class-E Inverters

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***Abstract*—Recent research has reported an undesirable OFF-state loss in high-frequency soft-switching power converters, such as resonant converters. This loss is attributed to a hysteresis loss related to the charging–discharging process of the output capacitance of the power transistor. However, precise estimation of transistor power loss and its breakdown into ON-state and OFF-state losses is challenging in the MHz-range operation due to the small circuit size, parasitic effects, and limited accuracy in existing methods to measure low-loss systems. We present a measurement concept to perform a complete loss breakdown of MHz-range resonant converters, as well, directly determine the OFF-state losses in transistors, which is demonstrated for a GaN-based class-E inverter operating at 10 MHz. A novel and compact calorimeter was designed to measure the converter active-device losses down to 20 mW within a 5 % error. This measured loss is then separated into four components using a combination of average and instantaneous electrical measurements: transistor ON-state loss, transistor OFF-state loss, gate-driver internal loss and gate loss. A simple no-load technique was devised to evaluate the gate-driver internal loss. The proposed approach directly determines output-capacitance hysteresis losses during the actual converter operation, which is not possible with existing measurement methods. The presented knowledge of individual loss components permits better optimization of MHz-range power converters.**

***Index Terms*—Active devices, calorimeter, class-E inverter, gate-driver losses, hysteresis losses, electrical measurements, output capacitance (C_o), soft switching, switching losses.**

I. Introduction

The use of GaN devices in resonant power converters, such as in the class-E topology [1]–[4], has gained recent popularity due to high-efficiency operation at MHz-range frequencies [5], [6]. Precise determination of all the power losses in these converters is paramount for their optimization. Such a task necessitates accurate measurement techniques to breakdown converter losses down to milliwatt level, and a clear understanding of transistor and gate-driver loss distributions. And it has never been more important as a notable OFF-state power loss in GaN transistors has been reported [7], [8], compromising the converter efficiency. This loss cannot be predicted by device datasheets and is related to a hysteresis energy loss (E_{diss}) in the transistor output-capacitance, C_o [9]; and it is a function of device drain–source voltage, v_{DS}.

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Exclusive measurement of C_o-hysteresis loss in an actual resonant power converter is challenging. This is due to the requirement of small circuit-size in high-frequency operation that in turn creates measurement issues: for example, probing difficulties in electrical measurements and loss quantification issues in thermal/calorimetric methods [8] (due to thermal cross-coupling when several devices are involved). Therefore, indirect electrical methods such as the Sawyer–Tower technique [7], [8], [10] or calorimetric methods [11], [12] have been used to predict C_o-hysteresis losses in a working converter. However, they offer difficulties in certain aspects. On the one hand, although an excellent technique [7], the Sawyer–Tower method cannot always replicate the actual v_{DS} waveform, and in some cases, the subsequent estimations could not fully explain the difference between measured versus predicted efficiencies in certain converters [6], [8]. Thus, a direct and accurate method to measure hysteresis losses during actual circuit operation is required. On the other hand, existing calorimetric methods involve relatively slow systems that are also limited in accuracy, especially in mW-range power levels [13]. Furthermore, they often determine system-level losses, and therefore, lack the ability to perform a complete loss break-down of a real converter in operation.

Moreover, the losses in gate driving become non-negligible in MHz-range switching frequencies. In this regard, the conventional approach used to calculate gate-driving losses accounts only for the gate loss, P_G, which is related to the turn-ON and turn-OFF processes of the power transistor [14], [15], with some works separating P_G into driver and transistor losses based on the physical location of gate-loop path resistances [16]. But this approach leaves the switching loss inside the gate driver itself unaccounted for [17]. The distinction between these two components is essential for a correct breakdown of active-device losses and to make an informed decision on the gate-driver selection for high-frequency converters.

In this research work, we demonstrate a complete and accurate loss breakdown of a class-E inverter operating at 10 MHz. A high-precision and compact flow-calorimeter is developed to accurately measure active-device losses at mW-level. This loss is then separated into transistor and gate-driving losses, using a combination of average current and voltage measurements. The transistor power loss is divided into ON-state (or the conduction loss, P_{con}) and OFF-state losses. A no-load concept

is utilized to separate the gate-driving loss into gate loss and driver internal-loss. We have chosen the class-E topology, especially as a platform to measure the OFF-state loss of a transistor, as it offers several practical advantages:

1) The existence of only a single transistor eliminates the issue of thermal cross-coupling between two devices [8].
2) The path inductances between the input, the device-branch, and the output can be incorporated into circuit inductances, thus permitting direct electrical measurements, without complicating the circuit operation.
3) All the parasitic shunt capacitances can be lumped together to a single shunt capacitance [18].

This paper aims to serve as a practical point of reference for high-frequency losses in transistors and gate drivers, their relative contributions and practical measurement. Section II introduces the important concepts on active-device losses, with special focus on C_o-hysteresis losses and gate-driving losses. Section III discusses the class-E topology. Section IV details the measurement concept and the development of the test system. Experimental results are presented in Section V. Section VI concludes the paper.

II. Active-Device Losses in Resonant Power Converters

In our analysis, we consider only field-effect transistors (FETs)—such as Si and SiC MOSFETS, and GaN HEMTs—as the switching device, which is denoted as S and undergoes zero-voltage-switching (ZVS). All the expressions and abbreviations for power refer to their average values, unless otherwise stated. The power losses generated in S and the gate-driving sub-circuit constitute the active-device losses, P_{active}. The total power loss in a converter, $P_{\text{loss-tot}}$, consists of P_{active} and passive-device losses, P_{passive}:

$$P_{\text{loss-tot}} = P_{\text{active}} + P_{\text{passive}} \tag{1}$$

The total input power, $P_{\text{in-tot}}$, of the converter is described as

$$P_{\text{in-tot}} = P_{\text{loss-tot}} + P_{\text{load}}, \tag{2}$$

where P_{load} is the useful output power. In terms of average input power measurements, $P_{\text{in-tot}}$ can be expressed as the addition of the power-circuit input power (or the dc-link power), P_{in}, and gate-driver IC input power, $P_{\text{in-GD}}$:

$$P_{\text{in-tot}} = P_{\text{in}} + P_{\text{in-GD}}. \tag{3}$$

A FET model with its parasitic capacitances is shown in Fig. 1(a), highlighting the output capacitance. When the device is in ON state [Fig. 1(b)], a conduction loss, P_{con}, occurs which is a function of the ON-state resistance of the device channel, $R_{\text{ch}}(V_{\text{drive}}) = R_{\text{DS(on)}}$, and the channel current, i_{CH}. Here, V_{drive} is the voltage across the gate–source terminals of S, v_{GS}, in fully-ON state. In the class-E inverter, which is a load-resonant soft-switching converter [19], C_o gets charged and discharged during the OFF state [Fig. 1(c)] of the device. The corresponding v_{DS} waveform is shown in Fig. 1(d). This charge–discharge process of C_o results in a non-ideal hysteretic

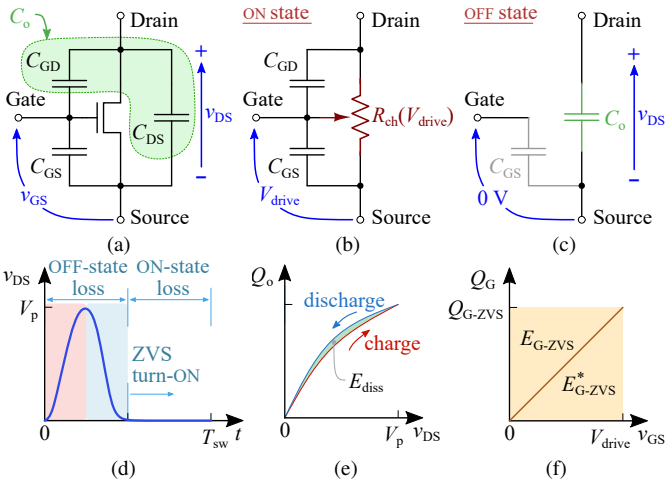


Fig. 1. (a) Model of a FET showing its parasitic capacitances, where $C_o = C_{GD} + C_{DS}$ is defined as the output capacitance. C_o is inactive during (b) the ON state of the device; and gets charged and discharged during (c) the OFF state of the device for a class-E inverter, where (d) the drain–source voltage, v_{DS}, shows a large-signal variation that generally occupies 50 % of the switching period, T_{sw}. (e) Related variation of the output charge (Q_o) with v_{DS} is represented by a QV curve; different charging (red line) and discharging (blue line) paths result in a hysteresis energy loss, E_{diss}, which is specified for a given maximum voltage V_p of v_{DS}. (f) Gate of the device gets charged up to $Q_{G\text{-}ZVS}$ during the turn-ON transient and then gets discharged at the device turn-OFF, resulting in a total gate-energy-loss $Q_{G\text{-}ZVS} \cdot V_{drive}$.

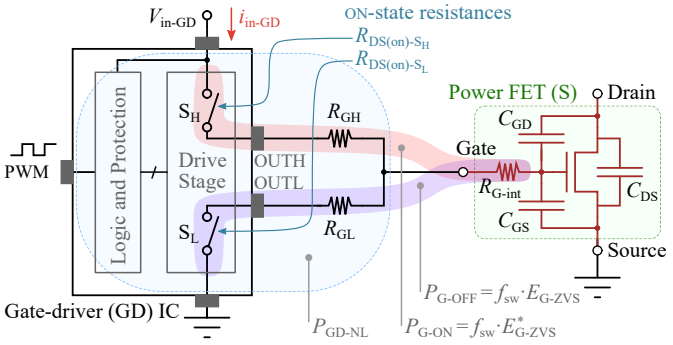


Fig. 2. An asymmetrical gate-driver IC has split outputs to control the turn-ON (through OUTH pin and R_{GH}) and turn-OFF (through OUTL pin and R_{GL}) processes of the power FET, S. In hard gating, the input power to the gate-driver IC, $P_{in\text{-}GD}$, is totally lost. This loss has two components: 1) losses inside the gate-driver IC, dominated by the switching losses of the drive-stage transistors S_L and S_H, and denoted as $P_{GD\text{-}NL}$; 2) a gate loss $P_{G\text{-}ON} + P_{G\text{-}OFF}$ in charging–discharging of the input capacitance of S.

energy loss,[1] E_{diss}, and can be calculated using a charge versus voltage (QV) curve as Fig. 1(e) indicates [7], [10]. The OFF-state losses related to the leakage current through the device channel are generally negligible, especially in comparison to E_{diss} losses for MHz-range frequencies [10]. Therefore, the total power loss is in S, at a switching frequency of f_{sw}, is given by (4), where $P_{diss} = f_{sw} \cdot E_{diss}$. Any loss related to gate driving is treated separately as shown next.

$$P_S = P_{con} + P_{diss} \tag{4}$$

A typical gate-driver circuit consists of the gate-driver IC

[1] A similar phenomenon can be observed [20] for resonant-transition [21] converters; however, in that case, the charge and discharge processes occur during switching transitions (OFF-state v_{DS} is fixed at dc-link voltage).

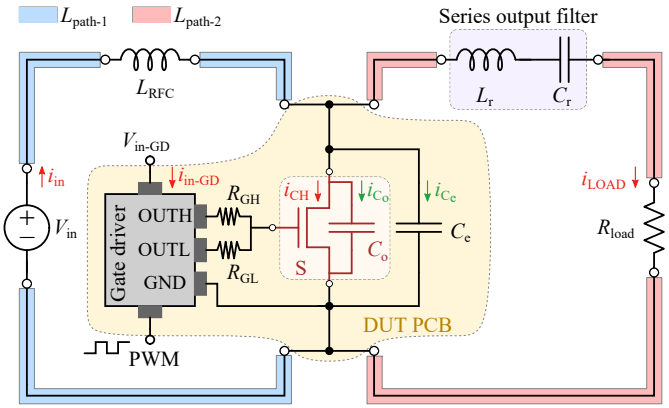


Fig. 3. Class-E inverter circuit. The transistor S and gate driver can be placed in a separate PCB, allowing the physical separation of the active- and passive-device losses in the circuit. The extra inductances (L_{path1} and L_{path2}) of connecting wires introduced by this separation are simply added to the inductances of the RF choke L_{RFC} and the series output filter inductor L_r; these inductors and the capacitor C_r account for $P_{passive}$. Important currents (total instantaneous) in the circuit are also marked.

(denoted as GD) and external resistances R_{GH} and R_{GL}, as Fig. 2 illustrates. From the perspective of the power transistor, the traditional gate-driving is hard-gated, i.e., the gate-driving path is an *RC* circuit and involves no inductive components to achieve resonant gate-driving [17]. For ZVS conditions, the total gate charge in S is denoted by $Q_{G\text{-}ZVS}$ as Fig. 1(f) shows [22]. During the turn-ON transient of S, a power $P_{G\text{-}ON} = f_{sw} \cdot E^*_{G\text{-}ZVS}$ is dissipated in the resistances $R_{DS(on)\text{-}S_H} + R_{GH} + R_{G\text{-}int}$ as marked by the area shaded in red in Fig. 2; and during the turn-OFF transient, a power $P_{G\text{-}OFF} = f_{sw} \cdot E_{G\text{-}ZVS}$ is dissipated in the resistances $R_{DS(on)\text{-}S_L} + R_{GL} + R_{G\text{-}int}$ (area shaded in purple). Both these losses are independent of the resistance values and are determined by $Q_{G\text{-}ZVS}$, V_{drive} and f_{sw}. The complete gate loss (P_G) is therefore given as

$$P_G = P_{G\text{-}ON} + P_{G\text{-}OFF} = f_{sw}(E^*_{G\text{-}ZVS} + E_{G\text{-}ZVS}) \quad (5)$$

There exists another loss (marked by the area shaded in light blue in Fig. 2) that is often overlooked in the gate-driving process, which is related to the drive stage of the IC; the two transistors S_L and S_H are hard switched and thus create their own output-capacitance-related losses and gate losses [17]. It should be emphasized that this loss cannot be calculated from the power device characteristics as it is an attribute of the chosen gate-driver IC. In this work, we present a simple no-load method to measure this power loss, which is denoted here as $P_{GD\text{-}NL}$. Finally, the total power loss in gate driving is

$$P_{in\text{-}GD} = P_G + P_{GD\text{-}NL}. \quad (6)$$

III. Class-E Inverter and Loss Distribution

In this section, the loss components introduced in Section II are identified with a class-E inverter circuit. The fundamental operation principles of this circuit are widely available in technical literature [2], [3], [6], [19], and hence, are not discussed here. Fig. 3 shows a detailed schematic of the circuit: the transistor S and the gate driver constitute P_{active}; the input choke L_{RFC} and the series output filter consisting of L_r and C_r

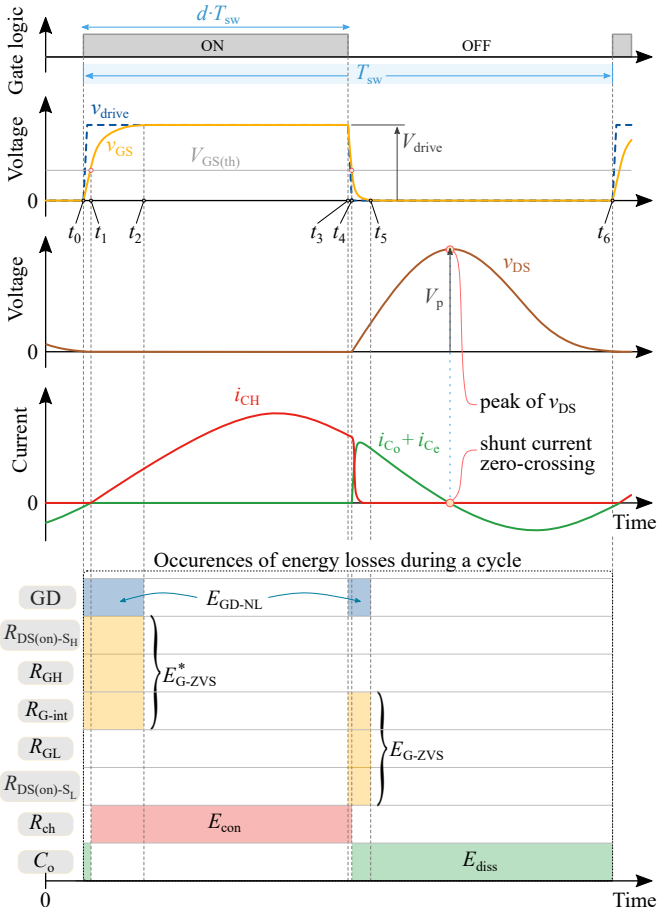


Fig. 4. Class-E circuit basic waveforms and time distributions of active-device energy losses during a switching cycle $T_{sw} = 1/f_{sw}$. Generally, the duty ratio d is kept at 0.5. The gate-driver output terminals OUTH and OUTL (see Fig. 2) determine the effective drive voltage v_{drive}. At t_0, OUTH is activated and v_{GS} rises. At t_1, v_{GS} equals gate–source threshold voltage $V_{GS(th)}$: the device channel turns ON and i_{CH} starts to rise at ZVS conditions. At t_2, the charging process of device input capacitance ceases and the channel is fully enhanced. At t_3, OUTH is turned OFF and OUTL is activated: v_{GS} starts to decrease. At t_4, $v_{GS} = V_{GS(th)}$: device channel is cut off, i_{CH} decreases rapidly, and v_{DS} rises charging C_o. At t_5, v_{GS} approaches 0 V. The discharge of C_o ideally ceases at the next $v_{GS} = V_{GS(th)}$ condition after t_6. The period t_1–t_4 is considered as the effective conduction period of the device channel (energy loss = E_{con}).

are responsible for $P_{passive}$. The total shunt capacitance consists of the transistor output-capacitance C_o and any external linear capacitance C_e added for optimum class-E operation.

The operation of the circuit is summarised in Fig. 4, highlighting how the energy losses related to the active devices in the circuit are distributed within a single switching cycle in steady state. The circuit is always operated in ZVS conditions ($v_{DS} = 0$ V at t_1 where $v_{GS} = V_{GS(th)}$). The gate-driving losses occur during the turn-ON and turn-OFF switching transients. For the duration (t_1–t_4) of the conduction loss, it is assumed that the channel is fully enhanced with $R_{ch} = R_{DS(on)}$. The hysteresis energy loss E_{diss} in C_o occurs during the OFF state (ideally extends up to some part of the switching transient).

IV. Measurement Concept and Design

Referring to Fig. 3, it can be noticed that a physical separation of the heat generated due to P_{active} and $P_{passive}$ is

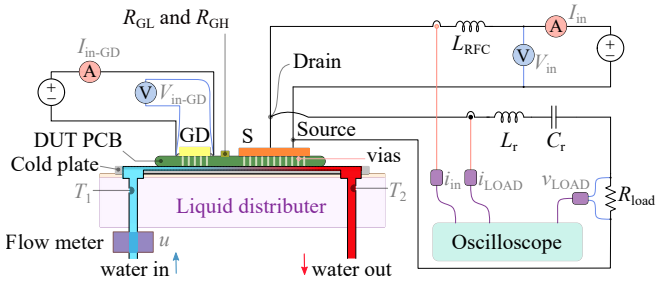


Fig. 5. Simplified block diagram of the presented measurement system showing the class-E inverter, the DUT PCB, and the application of calorimetric and electrical measurements. Two thermocouples (type K) measure the inlet and outlet temperatures, T_1 and T_2, respectively. An Elveflow MFS-A-5 flow meter accurately measures the flow rate u. I_{in}, V_{in}, $I_{in\text{-}GD}$ and $V_{in\text{-}GD}$ are average electrical measurements carried out with Fluke 87V DMMs. i_{in} and i_{LOAD} are total instantaneous current measurements carried out with Tektronix TCP0030A current probes and a MSO68B oscilloscope. v_{LOAD} is measured with a Tektronix THDP0200A differential voltage probe.

possible with the class-E topology. This is the underlying principle of the proposed measurement approach for the accurate breakdown of losses. The device under test (DUT) and the gate driver can be placed in a single PCB that is separated from the rest of the circuit. This requires longer connecting cables as marked by *path*$_1$ and *path*$_2$. The advantage of the class-E circuit is that L_{path1} (and its related losses) is easily incorporated into L_{RFC}, and requires no further compensation. Similarly, L_{path2} is added to L_r; but as L_{path2} alters the circuit operating conditions in this case, the circuit should be tuned to achieve optimum class-E operation.[2] The use of calorimetric and electrical measurements, together with the approach for the full-breakdown of losses are discussed in the following subsections with reference to the block diagram of the measurement system depicted in Fig. 5.

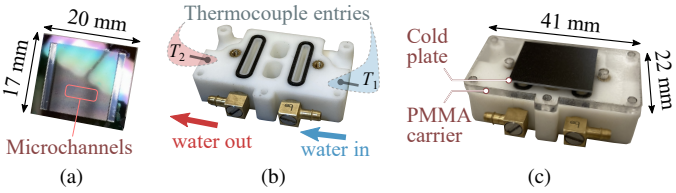
A. Calorimetric Measurements and Calorimeter Design

A novel and compact calorimetric unit [see Figs. 6(a) to 6(c)] was designed to evaluate the active-device losses in the circuit. The heat generated in S and in GD (including the heat generated in R_{GL} and R_{GH}) are extracted by a microchannel-based cold plate fabricated on a piece of silicon [see Fig. 6(a)], which is attached to the bottom of the PCB as Fig. 5 illustrates. A pressure controller is used to pass deionized water through the microchannels embedded in the cold plate [23]. The cold plate is brought in to good thermal contact with the circuit using thermal grease, which enables a high level of heat extraction in a small form factor [24]. This provides an additional benefit of cooling the active devices, permitting higher power dissipations without approaching critical temperatures. Due to its small size, the cold plate has a small heat capacity, resulting in short measurement times. The calorimeter evaluates the power dissipated on the PCB as

$$P_{calori} = \rho\, C_p\, u\, \Delta T. \tag{7}$$

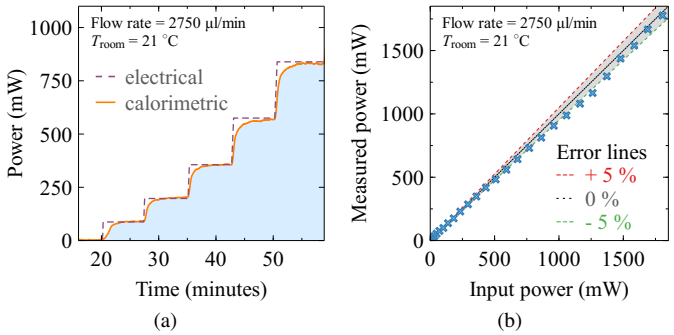
Here, ρ is the density of the liquid with a specific heat of C_p; and u is the flow rate of the liquid. The temperature difference

[2]This is achieved by adjusting one or a combination of the components C_e, L_r, C_r and R_{load} for a given f_{sw} [3].



(a) (b) (c)

Fig. 6. (a) A silicon microchannel-based cold plate and (b) a 3d-printed liquid distributor, with entries for water and thermocouples, are assembled as (c) a compact calorimeter and an efficient cooler.



(a) (b)

Fig. 7. (a) Example showing that the power loss measured with the developed calorimeter (solid line) approaches the dc input power $V_{DS} \cdot I_{DS}$ (dashed lines) quite fast, allowing 6–7 measurements within an hour at the given flow rate; the calorimeter tracks power levels as low as 100 mW with very good accuracy. Here, the transistor S is in ON state and a dc current I_{DS} was passed through it, while measuring the dc drain–source voltage V_{DS} (a 4-point measurement was used) (b) Calorimeter measurements exhibit good agreement with the dc input power, keeping the error ≈ 5 %.

($\Delta T = T_2 - T_1$) between the outlet and inlet water is measured using two thermocouples [see Fig. 6(b)].

The accuracy of the calorimetric system was verified with a dc calibration as Fig. 7(a) shows. The power measured with the calorimeter approaches the value of the dc input power within a few minutes, where the error in measurement [Fig. 7(b)] is kept around 5 % for the whole power range, indicating very good accuracy. The system can measure a wide power range of 20 mW to 10 W; this is especially beneficial as E_{diss} vary quite significantly between different device structures and with f_{sw} [7]. A complete discussion on the design, operation and performance of the calorimeter is presented in a companion paper [23].

B. Electrical Measurements

The power inputs to the gate-driver IC and the power circuit are measured with Fluke 87V digital multimeters (DMMs), whose average-mode specifications are listed in Table I [25]. The gate-driving loss is calculated as $P_{in\text{-}GD} = V_{in\text{-}GD} \cdot I_{in\text{-}GD}$, where $V_{in\text{-}GD}$ is a dc quantity and is measured very accurately. The input current to the gate driver, $i_{in\text{-}GD}$, contains high-frequency components at f_{sw} and above. Fluke DMMs can measure the average value of this current, $I_{in\text{-}GD}$, with μA-level accuracy, owing to an analogue 2-pole filter implemented before the ADC. The results from the DMM were verified by measuring $I_{in\text{-}GD}$ using a Tektronix TCP0030A current probe. The two measurements exhibit very good agreement and are compared in Fig. 8(a).

The input power of the power circuit, $P_{in} = V_{in} \cdot I_{in}$, is evaluated using the same method of average electrical measure-

TABLE I
SPECIFICATIONS OF AVERAGE MEASUREMENTS WITH FLUKE 87V DMM

Measurement	Type	Used Range	Resolution	Accuracy[1]
V_{in}	Average	0–600 V	0.1 V	± (0.05 % + 1)
$V_{in\text{-}GD}$	Average	0–6 V	0.001 V	± (0.05 % + 1)
I_{in}	Average	0–6 A	0.001 A	± (0.2 % + 4)
$I_{in\text{-}GD}$	Average	0–60 mA	0.01 mA	± (0.2 % + 4)

[1] For a measured value M, a ± (X % + Y) accuracy means an absolute error of ± [$0.01MX + (Y \cdot$ Resolution)]. Note: resolution depends on the selected range.

ments (also see Fig. 5), where I_{in} is the average value of i_{in}. The load power is calculated as $P_{load} = V_{LOAD(rms)} \cdot I_{LOAD(rms)}$, where the instantaneous load voltage (v_{LOAD}) and current (i_{LOAD}) are measured using a Tektronix THDP0200 voltage probe and a TCP0030A current probe, respectively.[3] The specifications of the current and voltage probes are tabulated in Table II. For amplitude measurements, the probes and the oscilloscope system retain an error < 3 %, up to 30 % of its specified bandwidth [26].

C. Approach for Full Breakdown of Converter Losses

First, the total power loss in the system and the passive-device loss is evaluated. With P_{in}, $P_{in\text{-}GD}$ and P_{load} available, using (2) and (3) the total power loss in the system is

$$P_{loss\text{-}tot} = P_{in} + P_{in\text{-}GD} - P_{load}. \tag{8}$$

As P_{active} is directly measured with the calorimeter, the passive-device loss can be calculated according to (1):

$$P_{passive} = P_{loss\text{-}tot} - P_{active}. \tag{9}$$

The active-device losses are further separated to the four components detailed in (4) and (6) as follows. First the total power loss in the transistor is calculated as

$$P_S = P_{active} - P_{in\text{-}GD}. \tag{10}$$

The transistor conduction loss is then separately calculated as

$$P_{con} = f_{sw} \cdot R_{DS(on)} \int^{T_{ON}} i_{CH}^2 \, dt, \tag{11}$$

where T_{ON} is the ON period of S, which is experimentally measured by observing the v_{DS} waveform (a TPP1000 passive probe was used). The value of $R_{DS(on)}$ is experimentally evaluated using dc electrical measurements as shown in Fig. 8(b). For the device ON resistance of GaN devices, dynamic $R_{DS(on)}$ degradation should be considered when (11) is evaluated [27], [28]. The specific application of this effect to the class-E circuit is discussed in Section V.

For the ON state of S, the channel current is calculated as $i_{CH} = i_{in} - i_{LOAD}$ (no current passes through C_o or C_e as $v_{DS} = 0$ V). Using (4), hysteresis energy loss of C_o is calculated as

$$E_{diss} = \frac{P_S - P_{con}}{f_{sw}}. \tag{12}$$

[3]We have verified the accuracy of current and voltage measurements by calculating P_{load} using $V_{LOAD(rms)}^2/R_{load}$ and $I_{LOAD(rms)}^2 \cdot R_{load}$, where an impedance analyser was used to measure R_{load}. This testing shows that as the load voltage is near-sinusoidal in class-E inverters, both current and voltage probes perform well even at high frequencies such as 10 MHz.

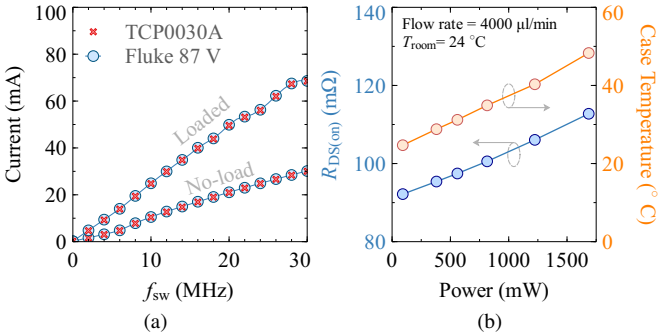


Fig. 8. (a) Variation of average input current $I_{in\text{-}GD}$ going into the gate-driver IC (a UCC27511A IC is used) with f_{sw}. Measurements with a Fluke DMM and a Tektronix TCP0030A current probe are compared. Both no-load (no S is soldered to the PCB) and loaded conditions (S is a GS66504B device) are shown. (b) Device dc ON-state resistance ($R_{DS(on)} = V_{DS}/I_{DS}$) is experimentally determined using 4-point dc measurements to calculate the conduction loss in S—see (11). The case temperature of S, measured with an IR camera, is also indicated.

One could consider using the multiplication of instantaneous shunt-capacitance current ($i_{C_o} + i_{C_e} = i_{in} - i_{LOAD}$ in OFF state) and voltage (v_{DS}) waveforms for the duration of the OFF period to evaluate E_{diss}. As this approach takes the difference of two similar values (as v_{DS} is always positive and the current crosses zero at V_p—see Fig. 4), it could result in a large error,[4] especially at high f_{sw}, for which the switching periods are in the range of probe propagation-delay times.

To separate the gate-driving losses according to (6), $P_{GD\text{-}NL}$ is individually evaluated by measuring the gate-driving loss on an exact replica of the DUT PCB, but without soldering the transistor S. Then, when the gate-driver is switched at f_{sw}, its measured input power solely represents $P_{GD\text{-}NL}$. Consequently, the device gate-loss is evaluated as

$$P_G = P_{in\text{-}GD} - P_{GD\text{-}NL}. \tag{13}$$

V. EXPERIMENTAL SYSTEM, RESULTS, AND DISCUSSION

In this section, the developed measurement concept is applied to identify individual loss components in a class-E inverter circuit operating at 10 MHz.

A. Experimental Procedure

A GaN Systems GS66504B GaN HEMT was used as the transistor and a Texas Instruments UCC27511A IC was used as the gate driver (details are listed in Table III). The passive components were calculated using the design equations derived by Sokal [3] and the final tuned-values are tabulated in Table IV. The external shunt-capacitance C_e and series-filter capacitance C_r are multi-layer-ceramic (MLC) capacitors with a C0G (NP0) dielectric and have high quality-factors. The load resistance has a temperature coefficient of resistance (TCR) of 100 ppm/K, and thus, its variation within the operating temperatures here is negligible. The implementation of the

[4]The significance of the error is dependent on f_{sw}, and voltage and current probe characteristics. The input impedance (frequency dependent) of the voltage probe is an important factor here as a certain level of device-branch-current could pass through it. These factors require further investigations.

TABLE II
SPECIFICATIONS OF MEASUREMENTS CARRIED OUT WITH TEKTRONIX MSO68B-OSCILLOSCOPE AND PROBE SYSTEM

Probe	Bandwidth	Measurement	Type	Used Range	Sensitivity	Gain Accuracy	@ 10 MHz[1]	
							Input Impedance	Derating Starts at
TCP0030A	120 MHz	i_{in}, i_{LOAD}	Total instantaneous	0–5 A	1 mA	1 % (dc typ.)	≈ 0.1 Ω	4 A_{peak}
THDP0200	200 MHz	v_{LOAD}	Total instantaneous	0–150 V	-[2]	2 % (dc)	≈ 4.8 kΩ	80 V_{rms}
TPP1000	1 GHz	v_{DS}	Total instantaneous	0–300 V	-	2.2 %	≈ 4.1 kΩ	160–200 $V_{ac\text{-}rms}$[3]

[1] Values approximated from the specification-sheet curves; [2] A vertical resolution can be considered, Resolution = Full-Scale Range / No. of Bits; [3] v_{DS} measurement is carried out for a very short duration of time.

TABLE III
LIST OF ACTIVE COMPONENTS

Component	Part No.	Specifications
Transistor (S)	GS66504B	650 V, 15 A, 100 mΩ
Gate driver (GD)	UCC27511A	Split output, 4.5–18 V, 4-A source, 8-A sink, SOT-23 (6) package

TABLE IV
LIST OF PASSIVE COMPONENTS

Component	Value	Unit	Remarks
R_{GH}	4.7	Ω	0402 package, 1/5 W, 1%
R_{GL}	1	Ω	0402 package, 1/5 W, 1%
R_{load}	25	Ω	Ohmite TGHMV25R0JE, ± 100 ppm/K, 0.23 °C/W, #187 tab terminals
L_{RFC}	10.8	μH	Air core, at 10 MHz, quality factor = 300
L_r	4.44	μH	Air core, at 10 MHz, quality factor = 343
C_r	56.9	pF	NP0 MLC capacitors, 1111 package
C_e	0–40.5	pF	NP0 MLC capacitors, 1111 package

Notes: C_e and C_r are high-Q / low-ESR non-magnetic multi-layer ceramic (MLC) capacitors with a C0G (NP0) dielectric, from Johanson Technology (E-series). L_{RFC} and L_r are made with 20-AWG and 14-AWG magnet wires, respectively. Inductance and quality factor values are measured with a Keysight 4990A impedance analyser and a 16047E test fixture. $L_{path\text{-}2}$ (Fig. 3) was measured to be around 410–420 nH at 10 MHz.

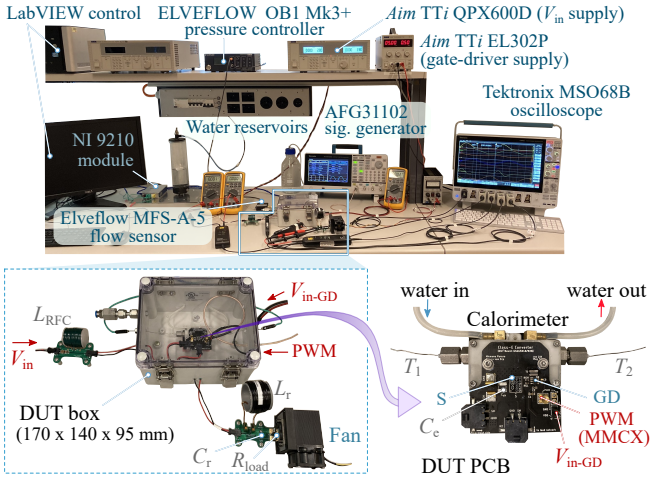


Fig. 9. Complete experimental system highlighting the measurement equipment and probes, calorimeter control system, class-E inverter circuit components, and the PCBs. The two active devices in the circuit (S and GD) and C_e are built into a separate DUT PCB. A Tektronix AFG31102 signal generator is used to generate the PWM signals. For P_{active} measurement, a LabVIEW-based control system is utilized: set the flow rate using a pressure controller, read the actual flow-rate using flow sensor; record the thermocouple readings T_1 and T_2; calculate P_{active} in real time.

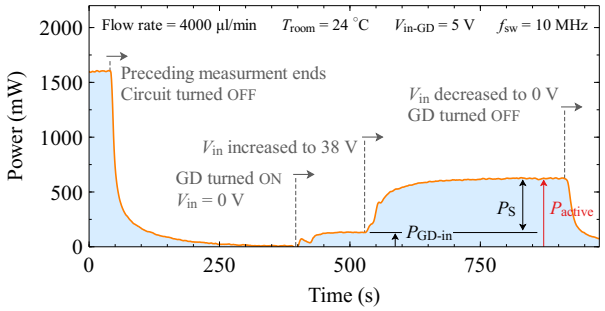


Fig. 10. Example showing the application of the developed calorimeter to measure P_{active} of the designed class-E inverter: the distinction between the gate-driving loss and the transistor losses is also observed.

circuit and the complete measurement system is shown in Fig. 9. An example of using the calorimeter to measure P_{active} is presented in Fig. 10: after the DUT board cools down from a preceding measurement, first the gate-driver circuit is turned ON and PWM is applied while V_{in} = 0 V; then V_{in} is gradually increased to the target operating mode. Once the thermal steady state is reached, P_{active} value is recorded.

One major aim of this work is to evaluate E_{diss} as a function of V_p for a given transistor, which is achieved by varying the input voltage of the circuit. V_p values of 100 to 300 V, at 50 V steps, were considered. The ZVS conditions were maintained by changing the value of C_e for $V_p \geq 200$ V, while $d = 0.5$ was maintained. For $V_p \leq 200$ V, C_e was 0 and d was slightly adjusted from 0.5 to achieve ZVS conditions.

B. Experimental Results and Discussion

Fig. 11(a) shows the total input power and the load power for different V_{in} values (at f_{sw} = 10 MHz). An input power of 102.6 W is reached for V_{in} = 81.4 V, which corresponds to a V_p of 300 V. Fig. 11(b) shows the breakdown of the corresponding power losses in the converter into passive-device, transistor, and gate-driving losses. The passive-device losses are predominant and increase with the input power due to the increased average current in L_{RFC} and RMS current in L_r. The latter is responsible for the largest contribution as it is subjected to a large ac current, hence increasing its ac winding losses; on the other hand, L_{RFC} experiences a relatively small ac ripple as the input current is nearly dc in the topology.

The gate-driving loss $P_{in\text{-}GD}$ stays constant, approximately around 120 mW [see Fig. 11(b)]; this result is expected as f_{sw} was fixed and ZVS conditions were maintained at each power level. Based on the measurement concepts presented in Section IV, this loss is divided into $P_{GD\text{-}NL}$ and P_G in Fig. 12(a), where a wide switching-frequency is investigated. At 10 MHz, the loss distribution is such that $P_{GD\text{-}NL}$ = 52.7 mW and P_G = 71.1 mW, i.e., for this combination of S and GD, $P_{GD\text{-}NL}$ amounts for 40 % of total gate-driving loss. For comparison,

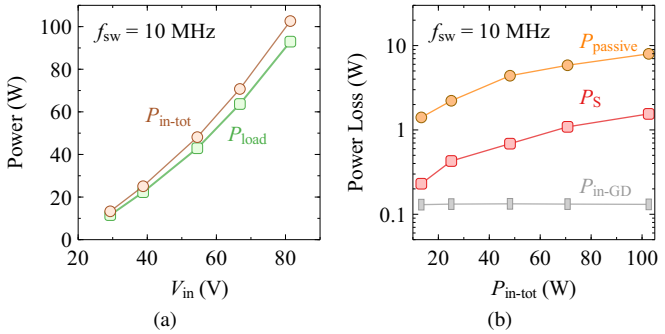


Fig. 11. Experimental results for the designed class-E inverter (see Table III and Table IV) operating at f = 10 MHz. (a) Variation of the total input power, $P_{in\text{-}tot}$, and the load power, P_{load}, with input voltage. (b) Breakdown of the losses with $P_{in\text{-}tot}$: the gate-driving loss $P_{in\text{-}GD}$, transistor loss P_S and passive-device losses $P_{passive}$. The presented method is capable of measuring mW-range power levels, enabling accurate loss and efficiency calculations.

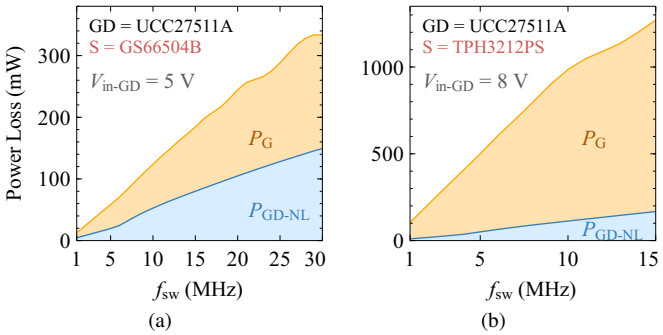


Fig. 12. Distribution of gate-driving loss components (hard-gating) with f_{sw} for two different transistors. In MHz-range and high-efficiency resonant power converters, the gate-driver loss cannot be neglected. For the GS66504B device, $P_{GD\text{-}NL}$ is around 40 % of $P_{in\text{-}GD}$. Relevant equations are: $P_{in\text{-}GD} = P_G + P_{GD\text{-}NL}$ and $P_G = P_{G\text{-}ON} + P_{G\text{-}OFF}$.

results for a Transphorm TPH3212PS GaN HEMT, which is a cascode structure, is shown in Fig. 12(b). Here, $P_{GD\text{-}NL}$ amounts for only 10–12 % of total gate-driving loss as the power transistor has a much higher input capacitance.

Referring to Fig. 11(b), it is observed that the losses in the transistor also increase with $P_{in\text{-}tot}$. This is due to two reasons. On the one hand, the conduction loss increases with V_{in} (or $P_{in\text{-}tot}$) because of the increased RMS current through S—note that $R_{DS\text{-}on}$ of S does not vary significantly (stays around 100 mΩ) for the considered power-dissipation range [see Fig. 8(b)]. On the other hand, the OFF-state loss increases with V_{in}, or more specifically with V_p, due to the hysteresis loss that occurs in C_o while it is being charged and discharged during the OFF-state in each cycle.

Recent works have reported that for soft-switching circuits, dynamic $R_{DS(on)}$ shows a smaller degradation in contrast to hard-switching circuits [27], [29]. However, such studies do not consider the particular OFF-state conditions imposed on the switch by the class-E circuit. To investigate this, we have considered the effect of an increase up to 20 % in the measured dc $R_{DS(on)}$ value, based on recent works [29]. Fig. 13 plots the corresponding E_{diss} values, where $R_{DS(on)}$ in (11) is multiplied by a positive factor k_{dyn} to evaluate P_{con}. The corresponding Sawyer–Tower results, reported by Zulauf et al. [8], are also marked (in solid blue). The comparison reveals that, as the

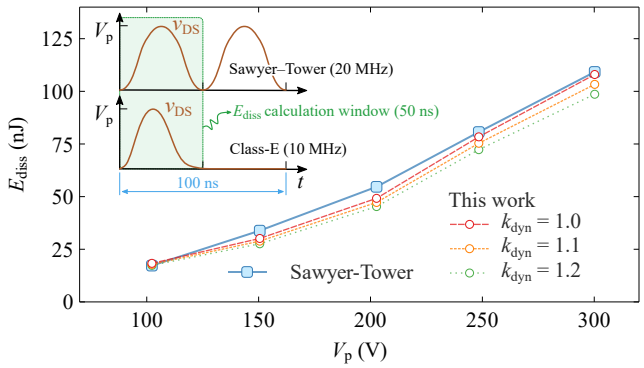


Fig. 13. Variation of output-capacitance hysteresis losses with V_p for the GS66504B transistor in actual converter operation at 10 MHz. k_{dyn} = 1.0, 1.1 and 1.2 correspond to 0, 10, and 20 % increase in the $R_{DS(on)}$ value (measured in dc conditions) to investigate dynamic $R_{DS(on)}$ effects. The corresponding Sawyer–Tower results are marked in solid blue (from Zulauf et al. [8]). Note that the v_{DS} waveform of a class-E inverter at 10 MHz with d = 0.5 has a 50 ns of charge–discharge time for C_o; this corresponds to a Sawyer–Tower excitation at 20 MHz.

value of k_{dyn} increases, the measured E_{diss} value deviates from the Sawyer-Tower results, suggesting that dynamic $R_{DS(on)}$ degradation is much smaller in class-E circuit compared to other circuits [27], [28]. This could be explained by the short duration of the peak OFF-state-voltage in class-E circuit, which can create different charging dynamics during the OFF state; however more studies are needed to understand such effects.

Note that although the circuit operates at f_{sw} of 10 MHz (T_{sw} = 100 ns), the actual charging–discharging event of C_o corresponds to a duration of 50 ns (for d = 0.5), or an effective frequency of 20 MHz (see Fig. 13). Therefore, the Sawyer–Tower results at 20 MHz should be used for comparison to get a similar charge–discharge frequency, as most GaN devices show a frequency dependence for E_{diss} [7], [8]. In addition, C_e is subjected to the same voltage swing as C_o. Since C_e was chosen to have a low equivalent-series-resistance (ESR), any ESR losses can be assumed negligible for the considered RMS current through the device branch; this assumption was validated by the observation of insignificant temperature rise in C_e during the circuit operation for all power levels.

Fig. 14 breaks down the active-device losses at f_{sw} = 10 MHz into the four main components described in (4) and (6) for the case of V_{in} = 81.4 V (or equivalently V_p = 300 V). The results reveal that P_{diss} dominates active-device losses with a contribution of 64.28 %, which amounts to 1.08 W. This observation demonstrates the major implication of output-capacitance hysteresis losses in MHz-range operation, inhibiting the ideal advantages of zero switching-losses (or OFF-state losses) offered by soft-switching operation. It is also important to note that the gate-driving losses in total amount to 7.82 % of P_{active}, which is not negligible.

This comprehensive breakdown of active-device losses aids the power electronic circuit designer to identify the causes for losses and choose the best transistor and gate-driver IC combination for the most favourable design. The measurement approach can be extended to other resonant converter circuits, but the complexity depends on the topology. For example, in an LLC half-bridge resonant converter [30], the PCB heats

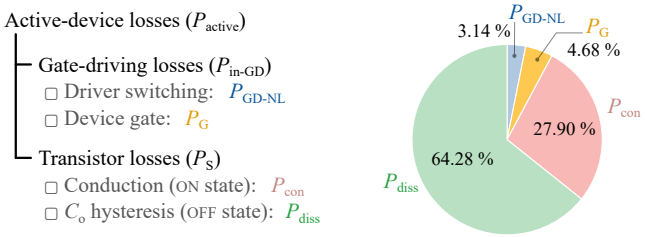


Fig. 14. Complete breakdown of the active-device average power losses in the tested class-E inverter at 10 MHz. Here, total active-device loss P_{active} = 1.68 W, total input power $P_{in\text{-}tot}$ = 102.6 W and V_{in} = 81.4 V. S is a GS66504B GaN HEMT and GD is a Texas instrument UCC27511A IC. C_o-hysteresis loss is the major contributor accounting for 64.28 % of losses. These results are based on in-circuit measurements (without using any estimation based on indirect measurements) and therefore represent actual operating losses.

up due two transistors. A single gate-driver can be used by employing a bootstrap method for direct $P_{in\text{-}GD}$ measurement. And dead-time should not extend much beyond the required minimum value to avoid errors in conduction loss calculations.

VI. Conclusions

We have demonstrated a complete loss-breakdown concept for a class-E inverter. The presented ideas allow to compare and separate the active-device losses into transistor ON- and OFF-state losses, as well as gate and internal-gate-driver losses. An experimental method with mW-level precision is presented and utilized to measure these losses at 10 MHz. The approach provides an accurate and in-converter evaluation of the hysteresis losses related to the output-capacitance of transistors. It was shown that the distinction between transistor-related gate loss and the driver-related internal loss is important for the loss characterization of MHz-range converters.

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