EPFL

Thèse n°7662

Low-Power and Wide-Tuning Range Frequency Generation for FMCW Radars in Advanced CMOS Technologies

Présentée le 10 décembre 2021

Faculté des sciences et techniques de l'ingénieur
Laboratoire de circuits intégrés
Programme doctoral en microsystèmes et microélectronique

pour l'obtention du grade de Docteur ès Sciences

par

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École polytechnique fédérale de Lausanne

2021

Unless you try to do something beyond what you have already mastered,
you will never grow.
— Ronald E. Osborn

To my parents. . .

Acknowledgements

First and foremost I would like to express my sincere gratitude to my thesis director, Professor Christian Enz. His inspiring work has been a golden reference for me throughout the whole Ph.D. and his continuous guidance lead me to deepen my knowledge of device modeling and circuit design and motivated me to aim for the highest goals. Working with him I learned the value of the methodical analysis of a problem, how to extract the essential meaning hidden in the most complex results and how to be effective in writing scientific publications.
I would like then to thank Dr. Alain-Serge Porret and Mr. Nicolas Raemy of CSEM for giving me the opportunity to pursue my Ph.D. degree in an industrial environment , where I received invaluable technical support and I had the chance to participate in projects beyond the scope of this thesis. I owe a special thanks to Mr. Erwan Le Roux, who was the main sponsor of the projects and activities related to radars. I will always be grateful for his selfless commitment to helping me widening my knowledge of the various aspects of radio systems during endless discussions also late in the evening, his priceless support in the laboratory during the testing phase and his ideas from the system-level to the circuit design. In addition, I would like to thank the whole RF and analog design team for their advice and help to solve the problems that I encountered throughout this journey. Dr. Franz Pengg, Dr. Alexandre Vouilloz, Dr. David Ruffieux, Dr. Nicola Scolari, Mr. Pascal Persechini, Dr. Camillo Salazar Gutierrez, Mr. Ernesto Pérez Serna, Mr. Nicola Gerber, Dr. Konstantinos Manetakis, Mr. Cédric Barbelenet and Ms. Felicity Hiscott have supported me with discussions, reviews, design of circuits and codes. Moreover, I would also like to thank Mr. Ricardo Caseiro, Mr. Cedric Monneron and Mr. Srdjan Stanarevic for all the help with the layout design, Mr. Daniel Sigg for the support with CAD tools, and Mr. Pierre-Alain Beuchat and Mr. Yann Liechti for the PCB design and help in the laboratory. Finally, I would like to thank Dr. Dragan Manic for taking care of all the logistics and support regarding the planning and execution of tape-outs.
I wish to thank Dr. Alessandro Pezzotta for the precious collaboration in ICLAB for the activities related to device modeling and characterization. His help and encouragement was really crucial to introduce me to the world of scientific publications and how to disseminate properly my work.
I would also like to express my deepest gratitude to Prof. Edoardo Charbon, Prof. Andrea

Baschirotto, Dr. David Ruffieux and Prof. Catherine Dehollain for being part of my jury, evaluating my thesis and providing comments and remarks about my work.
Particular thanks go to all my colleagues from ICLAB, current and former, for making these past few years a memorable experience. I wish to thank first Vladimir Kopta for everything he taught me during my studies, the technical discussions and the support in design and measurements. Moreover, the quality of his thesis has been another reference that pushed me to do always more and better and I am happy we have become friends. Then, I want to thank Sammy Cerida Rengifo, with whom I worked side by side in the radar project and I have become a good friend. Our collaboration has been really valuable and achieving the results presented in this thesis would have been much harder without his excellent work. A special thanks goes to Raffaele Capoccia and Mattia Cacciotti for the long discussions together but especially because we shared the best moments of this journey, which I will cherish forever with our friendship. I also want to thank all the rest of my lab mates: Claudio Bruschini, Raghavasimhan Thirunarayanan, Huang Huaiqi, Vincent Camus, Jérémy Schlachter, Assim Boukhayma, Farzan Jazaeri, Antonio D'Amico, Antonino Caizzone, Arnout Beckers, Chunmin Zhang, Minhao Yang, Hung Chi Han, Daniel Bold, Marta Franceschini and Salvatore Collura for all the fun we had together.
I am also thankful to all the friends I had fun with in these years outside of EPFL, between mountain hikes and parties. I want to acknowledge in particular Jacopo, with whom I shared all the path from the first years of engineering school in Torino to the Ph.D. in Switzerland and then to being my best man, for his invaluable friendship; Michela, who had to tolerate all the times Mattia and I talked about work during the weekends spent together; Carlotta, for her enthusiasm in all the activities we have done together, from skiing to board gaming.
Finally, I wish to acknowledge my deep gratitude to my family for their continuous love. I am grateful to my brothers, Federico and Andrea and their families, and my parents, Luigia and Renato. I am forever in dept to them for the opportunities they gave me, everything they taught to me from they day I was born and their unparalleled support for the path I chose even if it lead me far from home.
Finally I want to thank my wife Eleonora, who shared with me all the different shades of this Ph.D., from the happiness of the successes to the difficulties of the tough moments. She has been not only supportive and patient with me, but also outspoken when I needed to hear a different point of view. This mix has been the fuel that has propelled our journey together started twelve years ago and thanks to our love for each other I was able to never lose sight of what really matters in life for me.

Lausanne, 2021 Francesco Chicco

Abstract

Nowadays, the internet of things (IoT) nodes have started to spread in various domains of our society, from the industrial to the domestic environment. The remote sensing is one among their fundamental functions. The implementation of a radio detection and ranging (RADAR or radar) system in the millimeter wave (mm-wave) frequency band for vital signs monitoring, hand gestures recognition and localization has become more and more attractive over the past decade thanks to a large available bandwidth and an uncongested spectrum. In particular, the frequency-modulated continuous wave (FMCW) radars greatly benefit from the high carrier frequency and the multi-gigahertz bandwidth for the improvement of the angular and the radial resolution.

This thesis focuses primarily on the analysis and the design of rf and mm-wave circuits for frequency generation for FMCW radars in advanced CMOS technologies, namely 28-nm bulk and 22-nm fully-depleted silicon-on-insulator (FDSOI). The first fundamental step of this process is to analyze the performance of the devices available in such technologies from dc to rf. The transistors are characterized to extract the parameters of the simplified Enz–Krummenacher–Vittoz (EKV) model from dc measurements. A simple model for the output conductance versus the inversion coefficient (IC) for short-channel devices is proposed introducing an additional parameter. Moreover, the linearity of the devices is modeled with the simplified EKV which allows to predict the harmonic distortion and the other metrics as a function of IC. This was the missing piece in the EKV framework and it is validated versus measurements of short devices.

The second important step is to analyze the several harmonic (LC) oscillator topologies in the literature with the IC methodology in order to evaluate which bias region is the most power efficient for each of them. The same approach is used to study the phase noise in the 1/f2 region including all the noise sources of the transistors. These analyses indicate clearly that once again the moderate inversion is the sweet spot to design a low-power cross-coupled pair.

The last crucial step is the implementation of the low-power and wide-tuning range oscillator required in a phase-locked loop (PLL) for a short-range FMCW radar. Two different solutions are proposed. The first is an oscillator at 20 GHz. In order to assess the most suited topology and tuning technique two 20-GHz class-C LC oscillators are designed in 28-nm bulk

technology, one relying only on switched capacitors (DCO) and another with both switched capacitors and varactors (VCO). Thanks to the higher quality factor of the metal capacitors compared to varactors at such frequency, the DCO performs better in terms of phase noise for a similar power consumption of 1.2 mW in low-voltage conditions with an very large frequency tuning range of 5.8 GHz (27 %). The second solution is a DCO at 60 GHz. In order to ease the generation of a monotonic and linear chirp over several gigahertz in an all-digital PLL (ADPLL), a property of oscillators coupled in quadrature is exploited to obtain a very large tuning range without resorting to multiple banks of switched capacitors. This technique is applied in the design of a 60-GHz quadrature DCO in 22-nm FDOSOI technology. The oscillator achieves an extremely large seamless frequency tuning range of 11 GHz, a total range of 16.7 GHz (26 %) and an average power consumption of 10.4 mW.

Keywords: remote sensing, FMCW radar, advanced CMOS technology, EKV model, linearity, low-power oscillator, wide-tuning oscillator, dynamic divider, mm-wave, ADPLL.

Sommario

Oggigiorno, i dispositivi dell'internet delle cose (IoT) hanno iniziato a diffondersi in vari ambiti della nostra società, dall'ambiente industriale e quello domestico. Il rilevamento a distanza è una delle loro funzioni fondamentali. L'implementazione di un sistema per radiorilevamento e misurazione di distanza (RADAR o radar) nella banda di frequenza delle onde millimetriche (mm-wave) per il monitoraggio di parametri vitali, il riconoscimento dei gesti delle mani e la localizzazione è diventata sempre più attraente nel corso dello scorso decennio grazie ad un'ampia larghezza di banda disponibile e ad uno spettro poco congestionato. In particolare, i radar ad onda continua modulata in frequenza (FMCW) beneficiano grandemente di una portante ad alta frequenza e di una banda di parecchi gigahertz per migliorare la risoluzione angolare e radiale.

Questa tesi si focalizza primariamente sull'analisi e la progettazione di circuiti a radiofrequenza e onde millimetriche per la sintesi di frequenze in tecnologie CMOS molto avanzate, ossia 28-nm substrato e 22-nm silicio su isolante completamente svuotato (FDSOI). Il primo passo fondamentale di questo processo è l'analisi del comportamento dei dispositivi a disposizione in tali tecnologie dalla condizione di corrente continua alle radiofrequenze. I transistori sono qualificati per estrarre i parametri del modello Enz–Krummenacher–Vittoz (EKV) semplificato dalle misure a corrente continua. Un modello semplice per la conduttanza di uscita in funzione del coefficiente di inversione (IC) per dispositivi a canale corto viene proposto introducendo un parametro addizionale. Inoltre, la linearità dei dispositivi è modellata con l'EKV semplificato il quale permette di predire la distorsione armonica e le altre metriche in funzione di IC. Questo era il pezzo mancante nella struttura dell'EKV ed è validato con misure su dispositivi a canale corto.

Il secondo importante passo è analizzare le svariate topologie di oscillatori armonici (LC) in letteratura con la metodologia dell'IC per valutare quale regione di polarizzazione è la più efficiente energeticamente per ognuno di loro. Lo stesso approccio è usato per studiare il rumore di fase nella regione $1/f^2$ includendo tutte le sorgenti di rumore dei transistori. Queste analisiindicano chiaramente che ancora una volta l'inversione moderata è la condizione migliore per la progettazione di una coppia incrociata a basso consumo.

L'ultimo cruciale passo è la progettazione dell'oscillatore a basso consumo e ampio intervallo

di accordo richiesto in un circuito ad aggancio di fase (PLL) per radar FMCW a corta distanza. Vengono proposte due diverse soluzioni. La prima riguarda un oscillator a 20 GHz Per identificare la topologia e la tecnica di sintonizzazione più adatta, due oscillatori LC in classe C a 20 GHz sono progettati nella tecnologia CMOS substrato 28-nm, uno basato solo su capacità commutate (DCO) e un altro sia con capacità commutate sia varactor (VCO). Grazie al fattore di qualità maggiore delle capacità tra metalli rispetto a quello dei varactor a tali frequenze, il DCO mostra un comportamento migliore in termini di rumore di fase per un consumo simile di 1.2 mW in condizioni di bassa tensione di alimentazione con un intervallo di accordo molto ampio di 5.8 GHz (27 %). La seconda soluzione prevede un DCO a 60 GHz. Per facilitare la generazione di una rampa di frequenza monotona e lineare di diversi gigahertz in un PLL completamente digitale (ADPLL), viene sfruttata una proprietà degli oscillatori accoppiati in quadratura per ottenere un intervallo di accordo molto ampio senza ricorrere a diversi banchi di capacità commutate. Questa tecnica è applicata nel progetto di un DCO in quadratura a 60 GHz in una tecnologia FDSOI 22-nm. L'oscillatore raggiunge un intervallo di accordo senza soluzione di continuità estremamente ampio di 11 GHz, un intervallo totale di 16.7 GHz (26 %) e un consumo di potenza medio di 10.4 mW.

Parole chiave: rilevamento a distanza, radar FMCW, tecnologia CMOS avanzata, modello EKV, linearità, oscillatore a basso consumo, oscillatore ad ampio intervallo di accordo, divisori dinamici, mm-wave, ADPLL.

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1 Introduction

1.1 Low-Power Applications for the Internet of Things

The “Internet of Things” (IoT) has evolved from an abstract and appealing concept to a real and promising opportunity to set the biggest digital revolution after the introduction of the Internet. A lot of technologies converged on it throughout this evolution as they were born or developed. For example, an IoT device is the fitting environment for the application of edge computing as it brings a preliminary trimming of data and hence reduces the energy spent for communication and the space occupied in the cloud, another key factor in the picture. Machine learning (ML) is also helpful in the task of handling a huge amount of data, as neural networks can train with such datasets and focus only on the relevant patterns. All of these aspects ultimately fall under the umbrella of artificial intelligence (AI); the collection of information by the sensors in the IoT devices may serve as the input for a digital brain capable of behaving like a human, making decisions on its own.

The number of connected devices in the world has grown tremendously over the past 30 years, overtaking the number of human beings during 2010 and reaching 50 billion in 2020 (see Fig. 1.1). The machine-to-machine (M2M) applications are the main driver for the increase of connected devices today and they are expected to represent the 50 % of the total by 2023 [2]. The domains in which the applications for IoT nodes have developed in these years range from smart homes to healthcare, manufacturing, infrastructures and defense. Fig. 1.2 shows the shares by field: the connected homes are the largest in number while the connected cars have the fastest growth for the upcoming years [2]. The spectrum of required performance is very wide: where fast computing, low latency and large data throughput in communication are needed, the power consumed is necessarily quite high. On the other side of the spectrum there are low power applications which demand an efficient data processing and a low data rate. The communication aspect is crucial given the amount of devices to connect and the volume of data to exchange. Indeed, several wireless communication technologies are involved to satisfy the requirements of such heterogeneous applications [3, 4]. For contact and very short-range communications there are radio-frequency identification (RFID) and near field

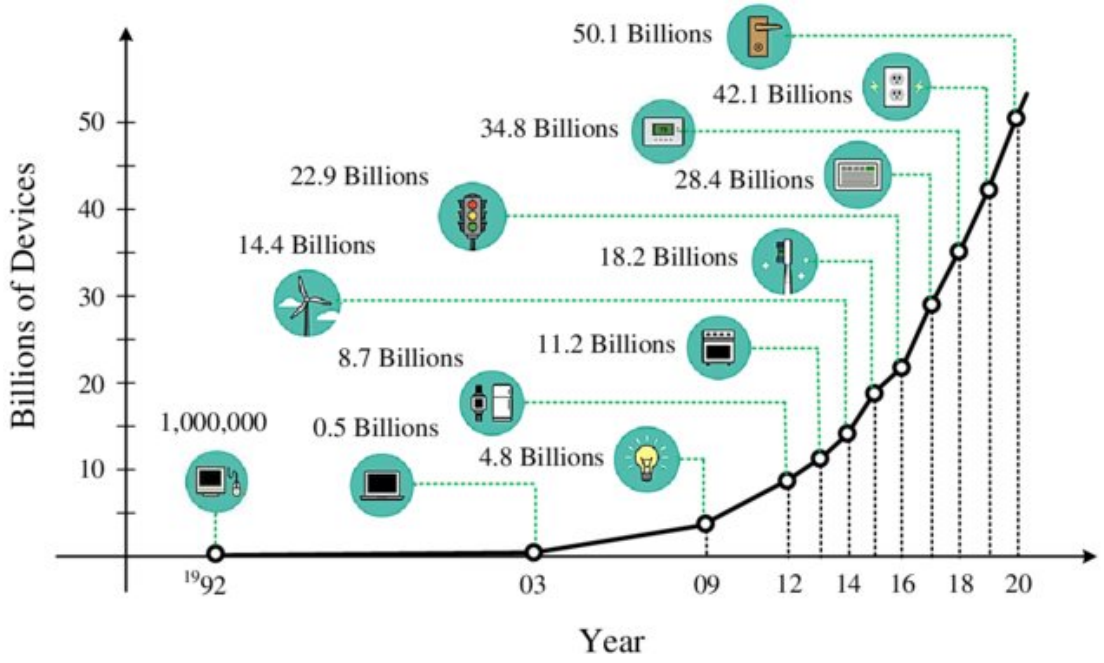


Figure 1.1: Number of connected devices in the world [1].

communication (NFC). For a short-range wireless connection, a Bluetooth Low Energy (BLE), a ZigBee or an ultra-wide band (UWB) radio can be used for personal area networking (PAN): they are low-power but based on different network structures. Moreover, Zigbee is included among others in the IEEE 802.15.4 standard, which is specific for IoT applications and defines the operation of low-rate wireless personal area networks (LR-WPAN). The Wi-Fi, which is a family of wireless network protocols and is based on the IEEE 802.11 family of standards, is an alternative between the short and the medium-range, with a capillary presence in every building; more throughput but higher power consumption. Moving to the medium-range radios there are the broadband cellular network technologies, such as 4G and 5G: they both grant high performance and low latency at the expense of the power consumption. 5G has a dedicated profile for IoT devices to handle a large number of nodes with low latency even while they are in motion. Finally the long-range, low-power, wide area networks (LPWAN), such as Sigfox, LoRa and NB-IoT, address directly this segment with dedicated low throughput, large coverage and ultra-low power consumption.

This thesis focuses on the low-power and short-range applications with a limited data throughput. Such systems are usually meant to be deployed in an environment and to work for years on a button cell or energy harvesting. Their limited power budget is the primary design specification and the main challenge for circuit designers and system engineers. In this perspective, the low-power design of rf and analog circuits is the key to expand the capabilities of such devices. Indeed, typically the radio power consumption is dominant in an IoT device with more than 50 % of the total [5]. However, the main functionality is gathering data through sensors integrated in their system. In general it is devoted to the monitoring of the parameters

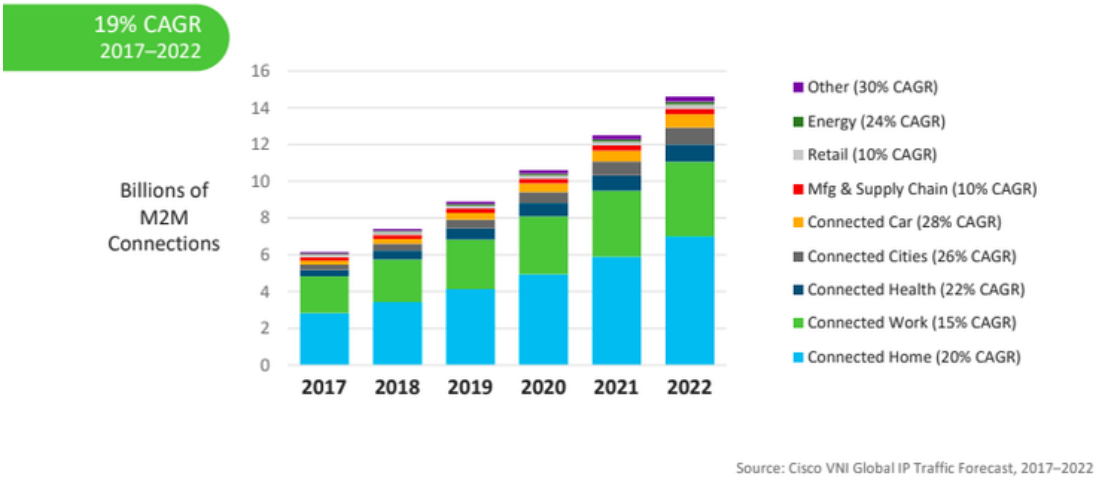


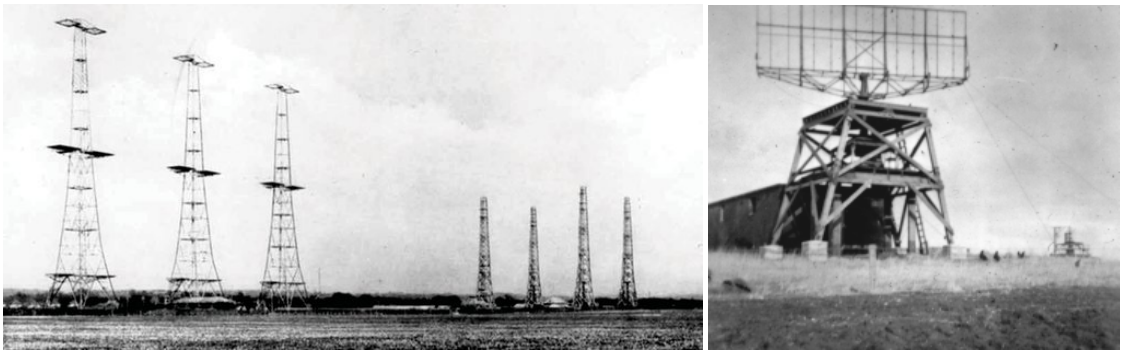
Figure 1.2: Share of M2M connections by field with expected compound annual growth rate (CAGR) (Source: Cisco).

of a target, ranging from the environmental situation, to the status of a structure or the health condition of a living subject. Among the sensing techniques, wireless sensing by means of rf signals offers some unique advantages [6–8]: it does not require contact, hence it allows to place, more freely, the devices in the surroundings of the targets and to monitor more of them at the same time. Moreover, it becomes a crucial technology to enable and develop a deeper interaction between humans and machines.

1.2 Remote Sensing with Radar Systems

Some of the radios mentioned for communications have also been used as wireless sensors, amongst those being Wi-Fi, Bluetooth, UWB and RFID. Moreover, a dedicated detection system can be effectively exploited for this purpose, such as a radio detection and ranging (radar) system. They have greatly evolved from their early employment and reached integrated circuits benefiting from the development of advanced technologies. Nowadays they can be found, for example, in most vehicles equipped with autonomous- and self-driving capabilities as one of the primary enablers. Nevertheless, this is just the beginning and numerous platforms are quickly developing. For this scope, the millimeter wave (mm-wave) frequency band has become highly attractive over the past decade thanks to the large available bandwidth and the less crowded spectrum. In fact, a wider band not only enables new wireless communication standards supporting higher data rate, but also significantly enhances the performance of radar systems.

In this thesis the target application is the detection of human features like vital signs and hand gestures by means of a radar system and in particular the implications on the generation of the RF signals with a limited power budget are explored. The details about the type of radar



(a) (b)

Figure 1.3: Pictures of British radars in World War 2: a) Chain Home [9] and b) Chain Home Low (source: Scottish Engineering Hall of Fame).

chosen for the project and the designed circuits are the subject of chapters 4 and 5, while in the rest of this Chapter the history of radar systems is described, the difference between long- and short-range radars is explained and the state-of-the-art on this topic in publications and commercial products is reported.

1.2.1 History of Radars in World War II

Radar emerged in the 1930s independently in several countries (USA, UK, URSS, Germany, France, Italy, Japan and the Netherlands) due to imminence of war and their vulnerability to air strikes [10]. It had been discovered several decades earlier but not developed: the first experiments had been carried out by Heinrich Hertz in the late 19th century and the first prototype had been patented in 1904 by the German Christian Hülsmeyer. Before that period, during the First World War the detection of aircrafts was performed listening for acoustic emissions [11]. Radar was only one of the candidates for a more sophisticated detection method. The first to produce a working radar system, the Home Chain, were the British with the physicist Sir Robert Watson-Watt in 1935: it was operated at a frequency of 22 MHz (13.6 m wavelength) and allowed to detect aircrafts at 3000 m of altitude and at a distance of 150 km in good weather conditions. Such a system gave the RAF an edge against the German attempt to invade Britain in the Second World War. The term “radar” itself was coined in 1939 in the USA [10]. In the same period, Germany had the most advanced radar systems but failed to understand its powerful use in defensive tactics, due to the extreme focus on the offense. Yet, the German navy developed the system Freya, which was used effectively over land and water by the Luftwaffe to support the bombing offense.

On the Allies side, the Home Chain was still too bulky and limited to wavelengths of tens of meters. First, with the development of Chain Home Low, working at 200 MHz, it was possible to detect low-flying aircrafts. The real technological break-through came with the invention of the cavity magnetron in 1940 by J. T. Randall and H. A. Boot. It allowed the generation of

shorter wavelength with higher power with smaller and more sensitive radars. It was used in the development of the Chain Home Extra Low: it worked at 3 GHz and allowed to detect planes flying below 100 ft of altitude. The magnetron was also the basis for the H2S, a system integrated on the aircrafts themselves for ground scanning: initially it worked at 3 GHz and later it reached 9.6 GHz. In 1941 a British mission to USA led by Sir Henry Tizard sought help for the mass production of the military equipment that UK needed to continue the war in exchange for the magnetron technology, superior to the American klystron. It led quickly to centimetric airborne radars, which gave the Allies a key advantage over the Nazis and the Japanese. In the advanced phase of the war, airborne radars were used for supporting naval battles, changing completely the fighting strategies. It allowed to counter the German U-Boat in the Battle of the Atlantic, initially dominated by the latter, due to their higher vulnerability to aircrafts than to battle ships.

1.2.2 From the Military to the Civilian Applications

Radar systems were of great importance in winning the war both on land and on sea but they also represented the onset for a new phase in the development of microwave techniques. After the war, radars found application in numerous fields, including civil aviation, marine navigation, speed control, meteorology and medicine [10]. The discovery of the magnetron had deep consequences not only for the radar technology but for many others, such as television, frequency-modulated (FM) radio and very high frequency (VHF) and microwave communication. In the field of radar systems, two key advancements were represented by the synthetic aperture radars (SAR) and the phased-array radars. The SAR was presented by C. Wiley in 1951 and first researched in the 50s and 60s for military purposes and then in the 70s and 80s for civilian applications. It allowed to bring the radar imaging to a new level of resolution overcoming the limitations of real aperture radars (RAR). A Synthetic Aperture Radar is an imaging radar mounted on a moving platform [12]. The conventional radar operation combined with the different positions of transmission and reception due to the platform movement, translates in a much longer virtual aperture compared to the physical antenna length. They have been placed on aircrafts and satellites since then for ground monitoring. Compared to the alternative optical imaging, SARs work in all weather and light conditions. As far the phased-array radars are concerned, they had been intensively studied since the 50s and fully developed in the 80s [13]. It consists of radar with an controlled array of antennas which creates a beam of radio waves which can be electronically steered in different directions without moving the antennas. The signal is distributed to the antennas through level-shifters which control the phase and provide the beam steering capability with constructive and destructive interference. After the initial employment in the military field, phased-array radars became part of the main civilian applications. The multiple-input-multiple-output (MIMO) radars are a special class of phased-arrays where higher spacial resolution is not obtained by increasing the number of physical antennas but by transmitting mutually orthogonal signals from multiple transmit antennas and recovering them from each of the receive antennas. The result is obtaining a virtual number of antennas equal to the product of the transmit and

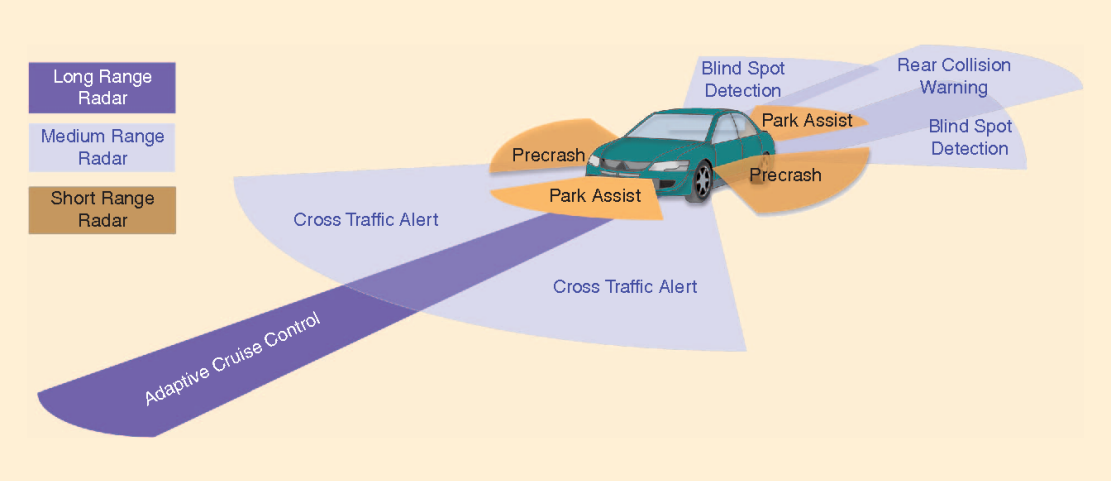


FIGURE 1. An ADAS consists of different range radars.

Figure 1.4: Application of short- to long-range radars for automotive [15].

receive ones [14].

1.2.3 Low-Cost, Short-Range, Low-Power Integrated Radars

All the civil applications mentioned above still use very big radar systems with long-range targets and hence large power consumption. With the improvement of semiconductor technologies for the design of rf and mm-wave circuits, radars now aim for the consumer market segment. The target is to build miniaturized fully-integrated radar systems which consume much lower power, overcoming the existing solutions made by connecting multiple boards with specific functions and with high-performance expensive custom designed components [16]. Building such a system-on-chip (SoC) would make radar sets low-cost and ubiquitous thanks to large-volume productions. Full integration comes with challenges and trade-offs. The chip size is limited and imposes high frequencies to allow integrated antennas, which still cannot achieve the gain and directivity of off-chip ones. On chip the transmitted output power is limited by the supply voltage which is set by the technology reliability and it is not suited for far targets. Integrating the analog front-end and the digital processing can result in higher noise and interference between them, hindering the overall performance.

Today the automotive application in the 76-77 GHz or 77-81 GHz bands and at 24 GHz is one of the main drivers for research from industry and academia in the field of low-cost miniaturized integrated radar systems [16–18]. In 1999 Mercedes Benz introduced a radar in one of its premium models for autonomous cruise control (ACC). The goal is to reduce as much as possible the cost of a radar set to make possible its diffusion to medium cars as well and mount several of them per car for different functions. Such systems are generally divided into two categories, long-range and short-range (Fig. 1.4). The former are designed in the 76-77 GHz or 77-81 GHz bands and are used for ACC. They are based on the frequency-modulated

continuous wave (FMCW) or the pulsed technique and they can cover up to 200 m with a resolution of 1 m and a view angle of 10°. They are placed in the front of the car and have to distinguish among several types of targets. The short-range radars instead are designed at 24 GHz with UWB technology for higher accuracy with targets which are closer to each other [16]. Their maximum range is limited to 30 m with a resolution below 0.1 m and a much wider angle of view (70°). They are used for parking aid, blind spot detection and collision warning on all sides: for these reasons, they are placed on the front, on the rear and on the sides of the car.

Nevertheless, other short-range sensing applications in the fields of healthcare and human-machine interaction (HMI) have recently been drawing a lot of attention, such as vital signs monitoring [19] and gesture recognition [20]. Moreover, due to the sanitary crisis, the interest in non contact people monitoring and interaction with machines and devices is growing even faster. The favorite frequency band for such applications is the license-free industrial,scientific and medical (ISM) band between 57 and 66 GHz. It is free because the oxygen molecule shows a peak of absorption around those frequencies, making it useless for medium- to long-range applications [16]. Typically continuous wave (CW) radars exploiting the Doppler and micro-Doppler effects or impulse-radio UWB (IR-UWB) radar have been employed for such applications. However, as discussed in chapter 4, FMCW offers several advantages which fit a re-configurable radar SoC with adaptive performances, suited for multiple scenarios.

1.3 Radar Systems: an Overview

In this section some representative state-of-the-art radar implementations are presented, both from academic papers and from commercial products.

1.3.1 Academic Works

Mitomo et al. [17]

This work targets a low-cost integrated radar SoC at 77 GHz for the mobility sector in 90-nm complementary metal–oxide–semiconductor (CMOS) technology. Only the phase-locked loop (PLL) and the RF front-end are integrated. The modulation is again FMCW thanks to the lower peak-to-average power ratio compared to IR-UWB radars. The frequency generation approach is an analog integer-N PLL with a direct digital frequency synthesizer (DDFS) used as reference and generating a stair-like triangular frequency sweep. Instead of a a high-resolution, power hungry and large DDFS, a coarse external one is employed in order to test its suitability for radar applications. The whole transceiver (TRX) consumes 520 mW for an output power of −2.8 dBm, 15.6 dB noise figure, −85 dBc/Hz phase noise at 1 MHz offset and covers 600 MHz bandwidth with an rms frequency error of 1.05 MHz. The chip area is 6.825 mm^2. Range measurements between 1 and 8 m are reported.

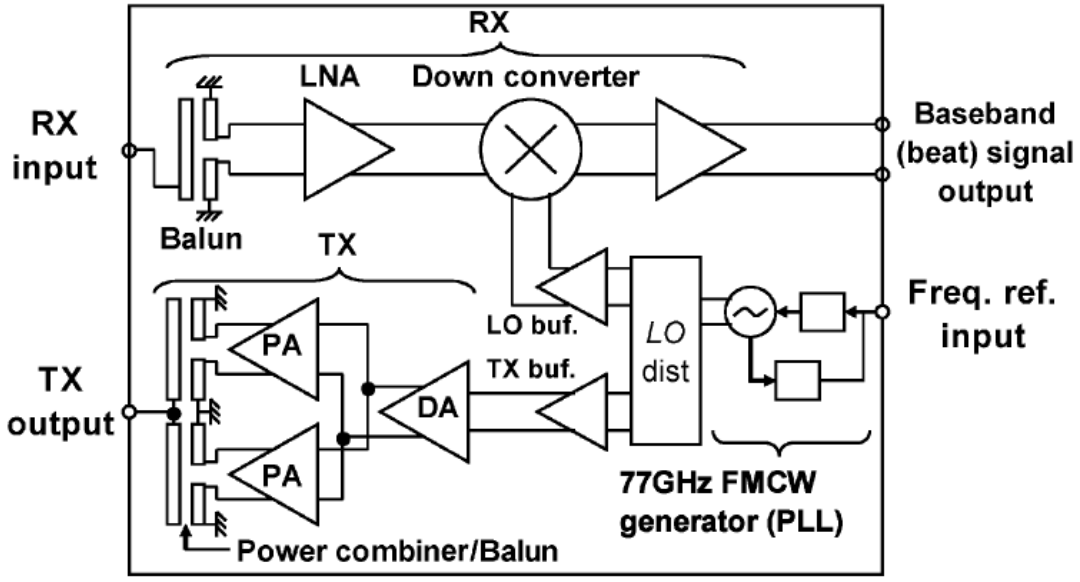


Figure 1.5: Schematic of the fully-integrated transceiver presented in [17].

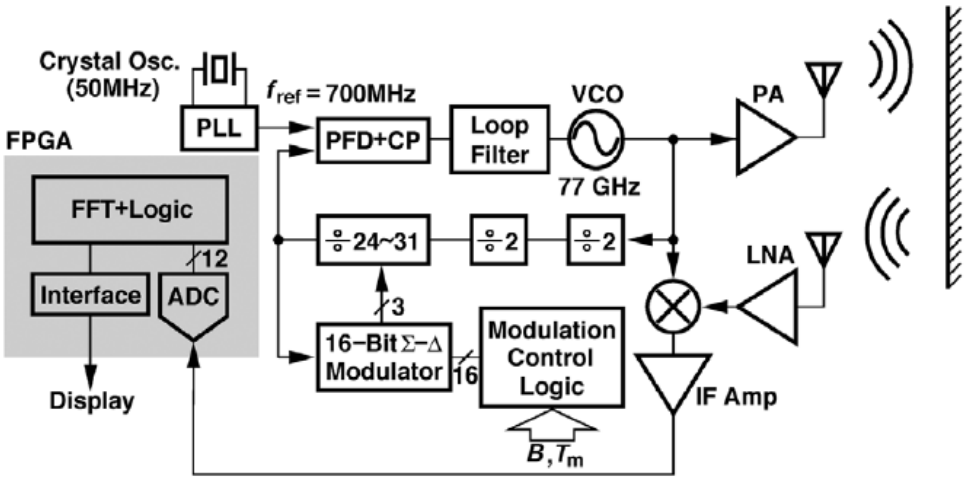


Figure 1.6: Schematic of the fully-integrated transceiver presented in [21].

Lee et al. [21]

This work was published the same year as the previous one, i.e. 2010, and proposes a fully-integrated FMCW radar system for automotive applications at 77 GHz in 65-nm CMOS technology. It relies on an analog fractional-N frequency synthesizer with a 700 MHz reference generated by a secondary external PLL. This system is one of the first chips integrating the whole transceiver, compared to previous works. It consumes 243 mW with an output power of 5.1 dBm, 7.4 dB low-noise amplifier (LNA) noise figure, −85 dBc/Hz phase noise at 1 MHz

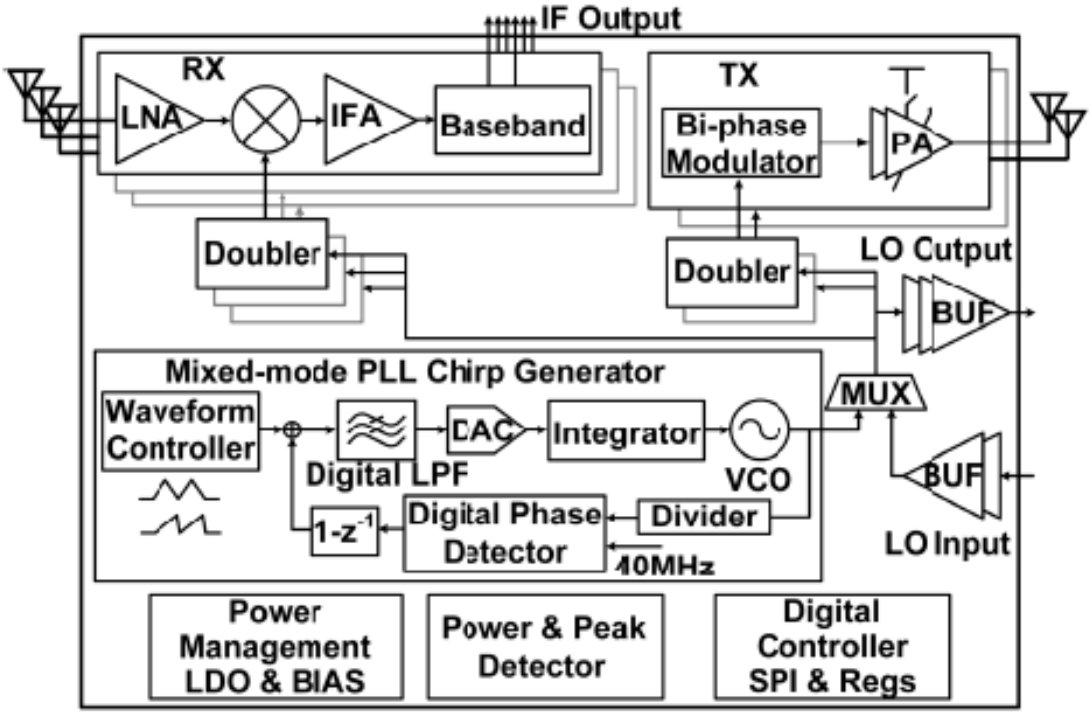


Figure 1.7: Schematic of the fully-integrated transceiver presented in [22].

offset and it covers a 700 MHz bandwidth with a frequency error below 300 kHz. The chip area is 1.045 mm^2. Both range and velocity measurements are shown: the maximum reported distance is 106 m and the velocity between 10 and 30 km/h.

Ma et al. [22]

This work presents a fully integrated 76–81-GHz FMCW radar transceiver in a 65-nm CMOS technology. It is composed of two transmitters (TX) and three receivers (RX) for MIMO processing. The goal is to improve the poor anti-interference ability and TX-to-RX leakage of previous implementations. For the MIMO approach, on-off keying (OOK) modulation is used on each TX channel. A mixed-mode PLL is proposed with flexible loop bandwidth configuration and a fast frequency ramping-down capability for sawtooth chirps, which grants better rms frequency error. The TX-to-RX leakage resilience is improved with a highly linear RX thanks to passive voltage-mode down-conversion. The chips consumes 921 mW with the power amplifier (PA) delivering 13.4 dBm, a 15.3 dB noise figure and a −87.4 dBc/Hz phase noise at 1 MHz offset. The covered bandwidth is 4 GHz and the rms frequency error is 110 and 4620 kHz for a chirp of 300 and 30 µs respectively. The chip area is 7.29 mm^2. The TRX achieves a range resolution of 5 cm and an angular resolution of 9° with the MIMO.

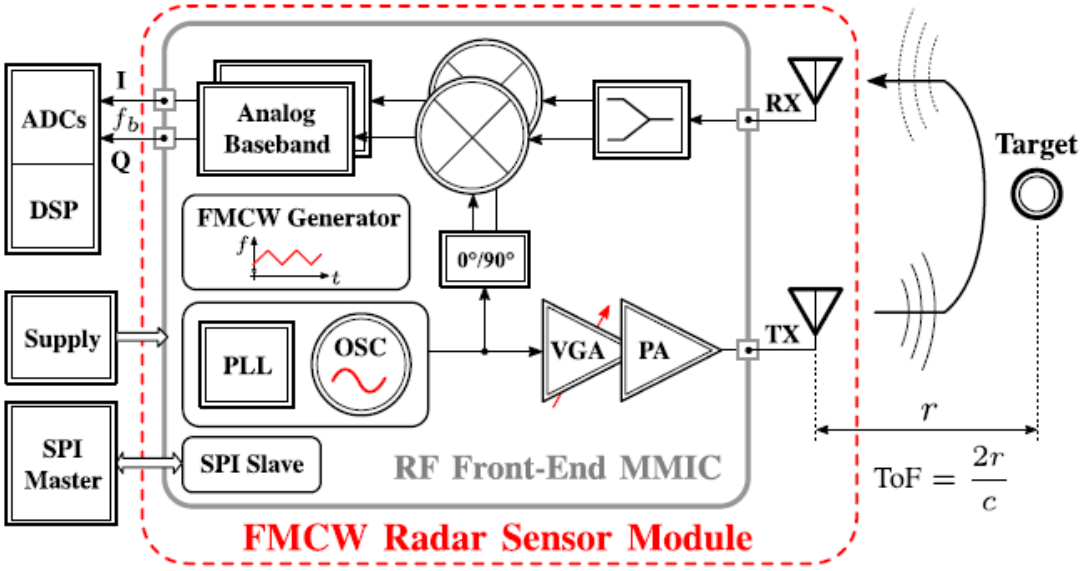


Figure 1.8: Schematic of the fully-integrated transceiver presented in [23].

Milosavljević et al. [23]

This work presents a compact 60-GHz FMCW radar sensor module with integrated antennas in 0.13-µm bipolar CMOS (BiCMOS) technology. The transceiver is composed of one TX and one RX channel and a fractional-N frequency synthesizer which covers around 10 GHz, from 54.5 to 64.5 GHz. The whole chip consumes around 690 mW and it delivers an output power of 6-7.5 dBm; the simulated noise figure is 15-17 dB and the phase noise is between -79 and −86 dBc/Hz at 1 MHz offset. With a modulation rate higher than 200 MHz/µs, the system is able to detect close proximity targets below 20 cm and achieves a range resolution below 2 cm. The chip area is 4.84 mm^2.

Kankuppe et al. [24]

The system presented in this work is the closest to the one targeted by this thesis. In fact, it consists of a low-power 60-GHz FMCW radar transceiver in 28-nm CMOS technology for indoor applications. The TRX is composed of one TX and one RX chain and a 10 GHz sub-sampling PLL followed by a cascade of a frequency tripler and a frequency doubler. The RX chain is based on a passive mixer-first architecture with a 3-stage high pass filter which reduces the TX-to-RX leakage and improves the linearity of the chain. The chips consumes only 62 mW with the PA delivering between 8.3 and 10.2 dBm, a 10.5 dB noise figure and a −92.9 dBc/Hz phase noise at 1 MHz offset. The covered bandwidth is 7.2 GHz and the rms frequency error is 168 kHz for a chirp of 51.2 µs. The chip area is 4.13 mm^2. An artificial heart beat is successfully measured at 5 m distance; overall the range resolution is 4.3 cm.

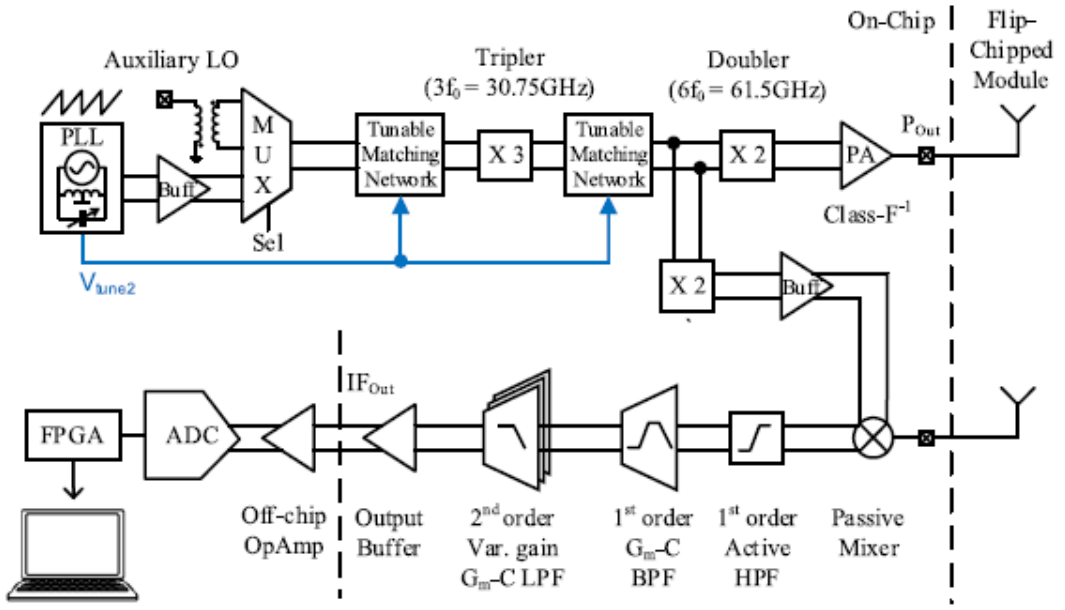


Figure 1.9: Schematic of the fully-integrated transceiver presented in [24].

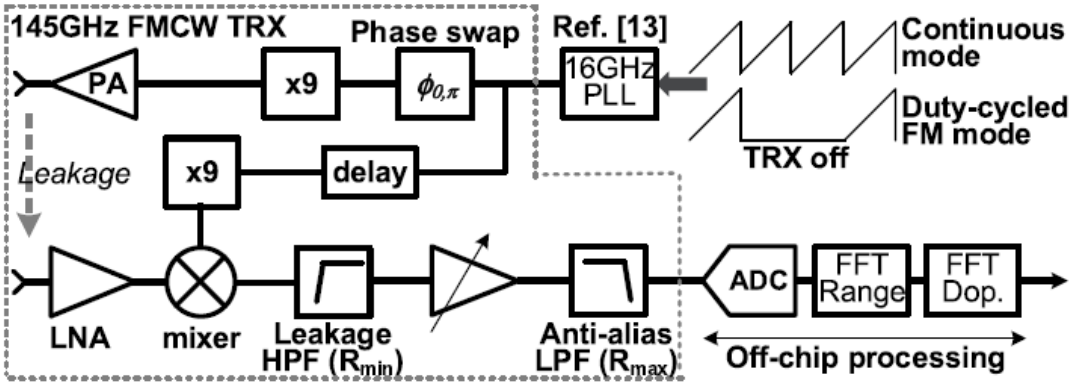


Figure 1.10: Schematic of the fully-integrated transceiver presented in [25].

Visweswaran et al. [25]

This work is reported because of the same targeted applications and the interesting analysis and features proposed even though the frequency band is very different. It presents a 145-GHz FMCW radar transceiver for vital signs and gesture recognition in 28-nm CMOS technology. The TX contains only one TX and one RX channel with on-chip antennas but separate chips with two TX or one RX are integrated as well for composing a MIMO system on PCB. The carrier is generated with an external sub-sampling PLL at 16 GHz followed by an on-chip multiplication by nine. The TX-to-RX leakage is neutralized with a delay in the local oscillator (LO) distribution toward the RX. The 1TX/1RX chip consumes 500 mW (without PLL) with the

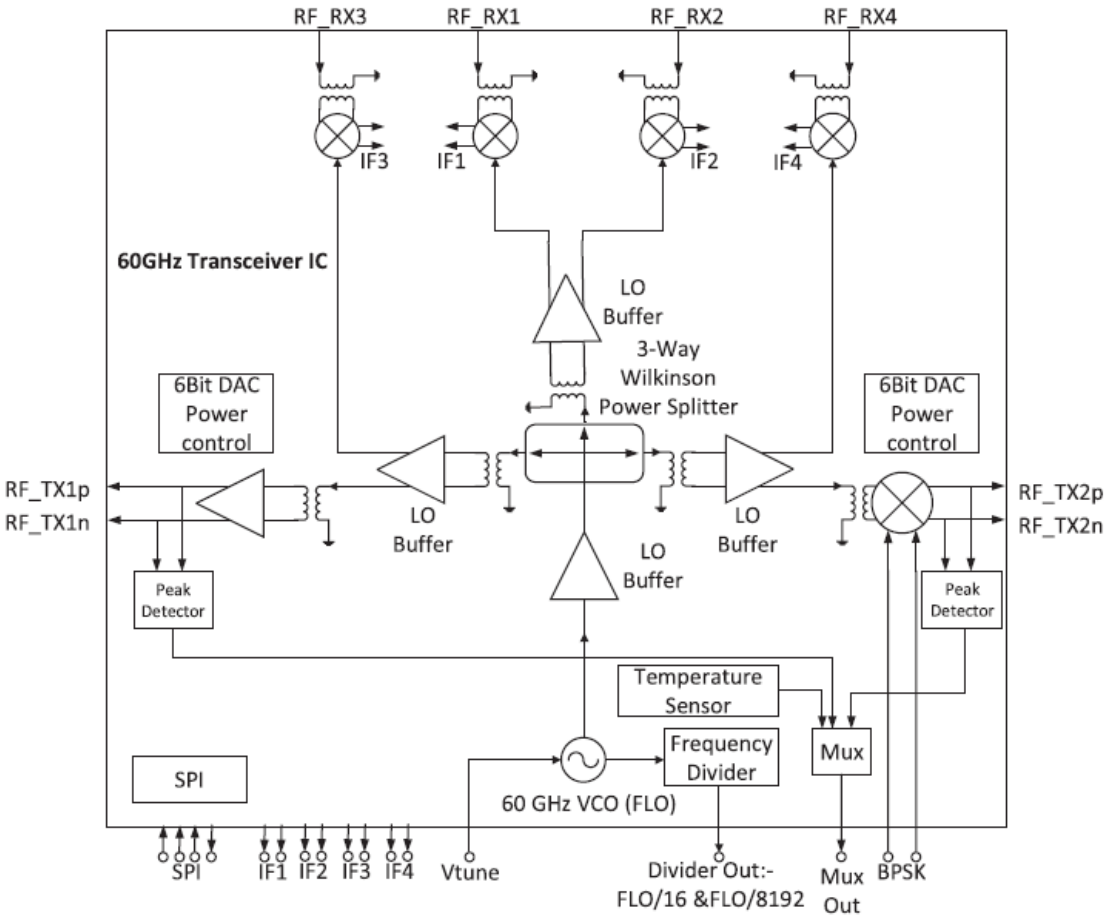


Figure 1.11: Schematic of the fully-integrated transceiver presented in [26].

PA delivering 11.5 dBm of effective isotropic radiated power (EIRP) and a 8 dB noise figure. The covered bandwidth is 13 GHz and the rms frequency error is 2.07 kHz for a chirp of 30 µs. The chip area is 6.55 mm^2. An artificial heart beat and breathing are successfully measured at 5.2 m distance with the MIMO system; overall the range resolution is about 3 cm.

1.3.2 Commercial Works

Infineon 60 GHz radar (Soli project) [20, 26, 27]

Infineon presents a highly integrated 57-64-GHz transceiver for smart sensing and short-range communications in 350-nm SiGe technology. The TRX is composed of two TX and four RX channels while the frequency chirp is generated with an integrated voltage-controlled oscillator (VCO) driven by an external PLL. The PA of one of the TX chains can work as a binary phase shift keying (BPSK) modulator at 400 MHz as well; the RX chains are based on a mixer-first architecture. The chips consumes 990 mW with the PA delivering 4 dBm, a 9.5 dB noise figure and a −105 dBc/Hz phase noise at 1 MHz offset. The covered bandwidth is 7 GHz

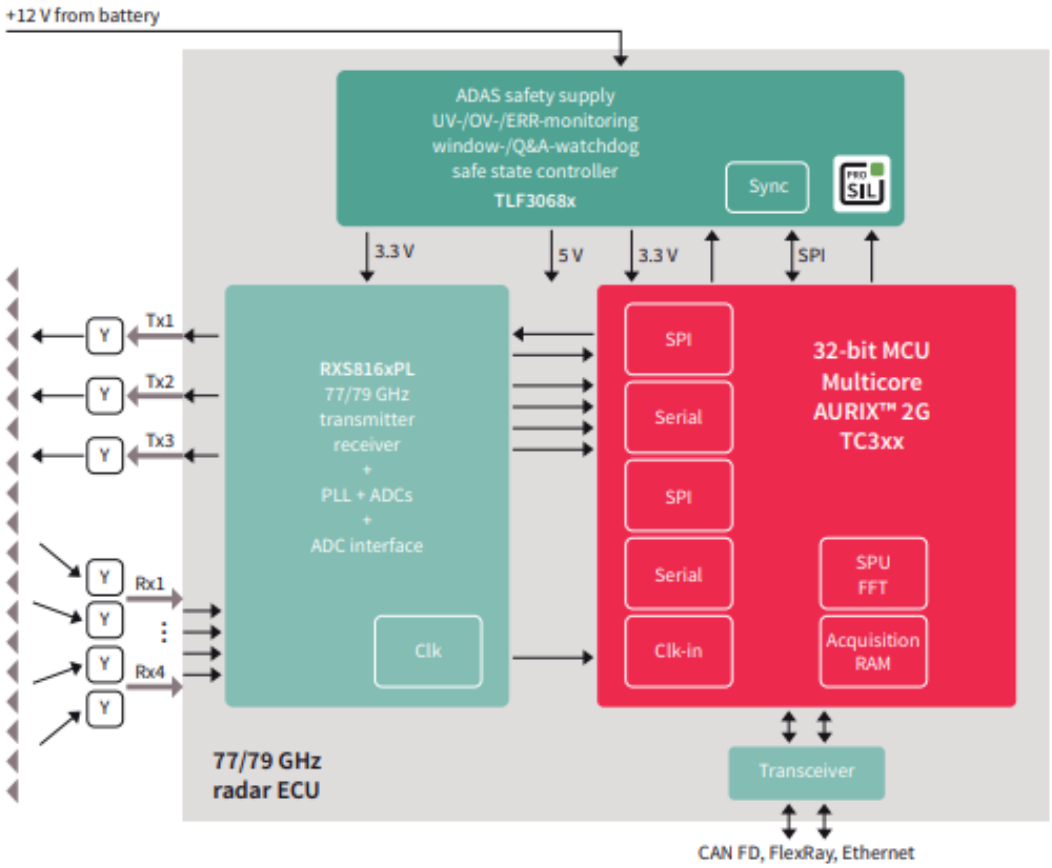


Figure 1.12: Schematic of the Infineon 77 GHz transceiver [28].

and the sawtooth chirp duration is lower than 100 µs. The chip area is 20.25 mm^2. The TRX achieves a range resolution of 2 cm. The board comes with antennas-in-package.

This chip is used by the Google's project Soli as the platform to develop their gesture recognition software. A newer version of this chip, integrated into the smartphone Google Pixel 4, has been presented in 2021. The technology is a 0.13-µm BiCMOS with a peak power consumption of 400 mW. It consists of a transceiver with one TX and three RX channels. It covers 7 GHz with a maximum chirp slope of 400 MHz/µs. With heavy duty-cycling it achieves 5 mW consumption and 5 m detection range.

Infineon 77 GHz radar [28]

Infineon has also a lineup of radars for automotive application at 24, 77 and 79 GHz. Focusing on the 77-GHz solution, there are several versions available, with different channel configurations (three TX and four RX or two TX and four RX) and different modulation bandwidth (1 and 2 GHz respectively). These products are in pre-production and not many details are available.

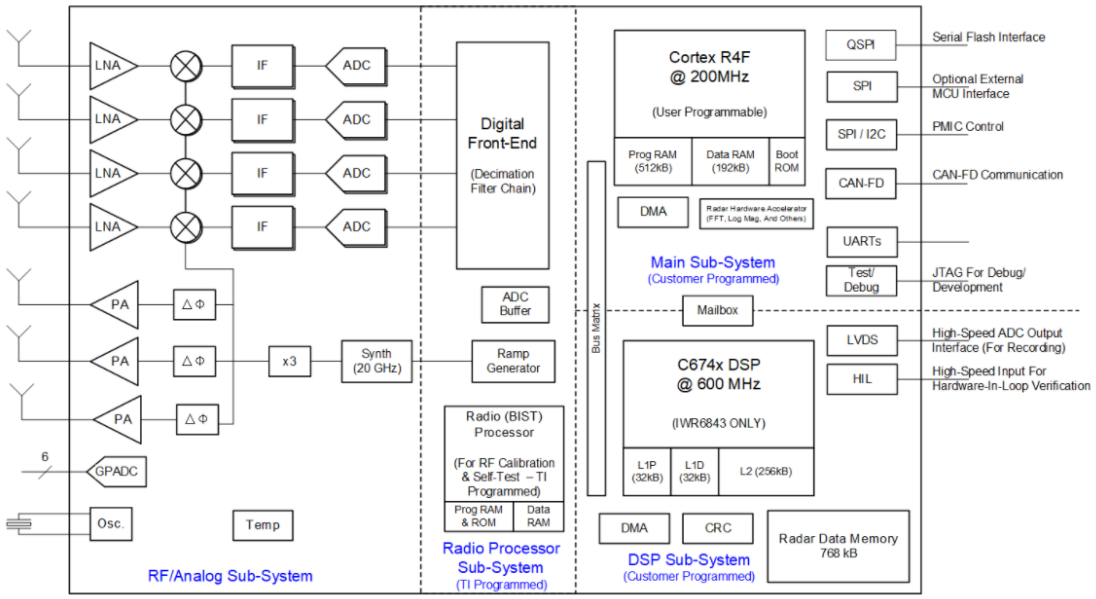


Figure 1.13: Schematic of the TI 60 GHz transceiver [29].

Texas Instruments 60 GHz and 77 GHz radars [29]

Texas Instrument lineup of radar systems for automotive applications includes several products in the 60-64 GHz and 76-81 GHz bands. Most of them have three TX and four RX, the PA output power is around 10-12 dBm, the noise figure is 13-14 dB and phase noise between -92 and −97 dBc/Hz at 1 MHz offset. They are built with a 45-nm CMOS technology and achieve 4 cm range resolution and 300 km maximum velocity detection.

NXP 77 GHz radar [30]

NXP offers a fully integrated 77-GHz fully integrated radar transceiver for automotive applications. The TRX is composed of three TX with BPSK modulation and four RX channels. The PLL works between 25.3 and 27 GHz and it covers 2 GHz bandwidth or 4 GHz with chirp stitching and it is optimized for fast chirp modulation. The overall power consumption in below 1.2 W for an output power of 11-12 dBm, a noise figure of 12-13 dB and a phase noise of -90/−86 dBc/Hz at 1 MHz offset.

1.4 Thesis Motivation and Organization

This thesis originates from the interest in designing low-power rf and mm-wave circuits in very advanced CMOS technologies for nowadays IoT applications. In particular, the hypothesis of including a radar SoC for remote sensing in IoT nodes is gaining a lot of traction and pushes academic and industrial research to investigate more this field. From the analysis of the

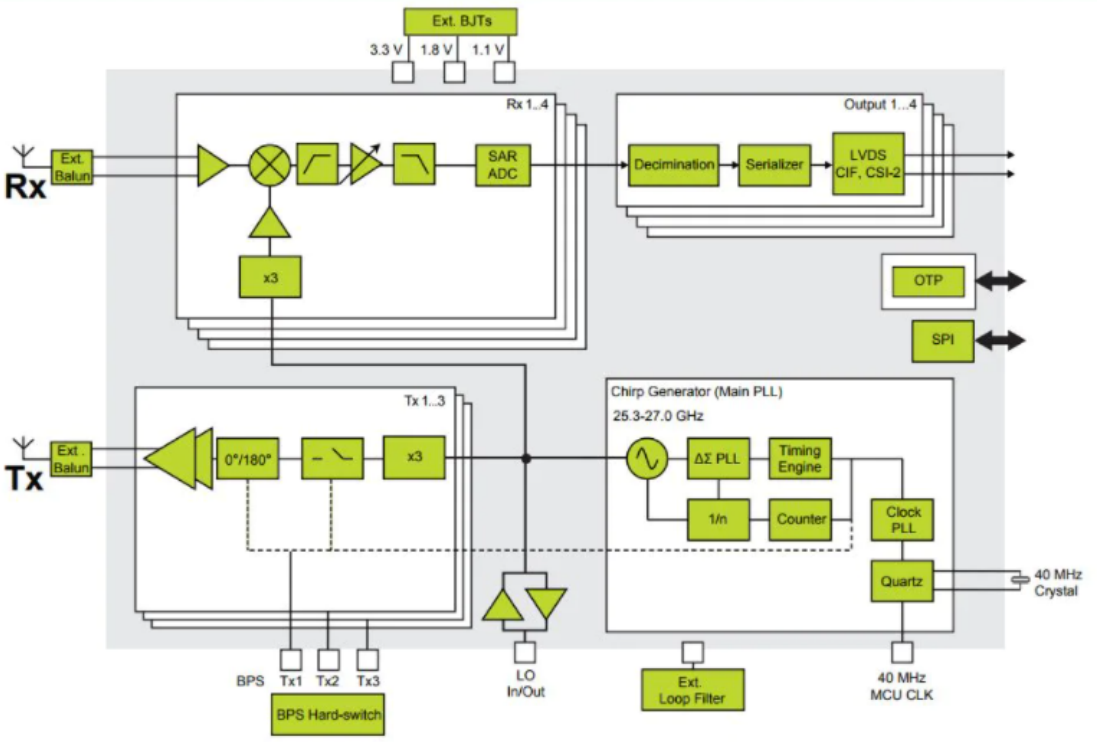


Figure 1.14: Schematic of the NXP 77 GHz transceiver [30].

state-of-the-art of fully-integrated radar transceivers, it is clear that great improvements were developed in the past ten years in terms of miniaturization, performance and number of channels targeting the MIMO approach. Nevertheless, in most cases the total power consumption is still quite high since the target is the automotive segment which can afford to consume more power to assure adequate performance. Having in mind SoCs for autonomous IoT nodes, there is margin to reduce it from several hundreds of milliwatts to a few tens of milliwatts for a TRX with one TX and one RX channel. This work focuses of the task of minimizing the power consumption of the frequency generation, which is the heart of any radio and a quite power hungry block. A dedicated design methodology is necessary, especially given the challenges posed by the advanced technologies which come into play when discussing the development of a complex system. Several research directions are explored to pursue this goal and they are described in the following chapters.

First, some advanced CMOS technologies are analyzed by means of the simplified Enz–Krummenacher–Vittoz (EKV) model of metal–oxide–semiconductor field-effect transistors (MOSFETs), which allows to identify the best low-power design trade-offs with a few extracted parameters and the concept of inversion coefficient *IC* [31]. In this framework, additional figures-of-merit are calculated with simple expressions to describe the transconductance efficiency, the voltage gain and the linearity of the transistors in all bias conditions, namely several decades of *IC* values. Moreover, the modeling and electromagnetic extraction of passive devices is analyzed and included in the design methodology for mm-wave circuits. The

careful co-design of schematic and layout is recognized as a crucial step in the successful optimization of low-power circuits getting the best performance with the given power budget.

Second, the LC oscillator is studied focusing on the minimization of the power consumption and the calculation of phase noise with a linear analysis including all the noise sources of the transistors. The optimum *IC* value for maximum power efficiency and figure-of-merit is identified for several oscillator topologies and a comparison among them is proposed.

Third, the task of designing the oscillator and the divider chain for a 60-GHz FMCW radar SoC is undertaken. Two different approaches are shown: one consists of designing a 20-GHz oscillator followed by a frequency multiplier (not studied in this thesis) and the other a fundamental 60-GHz oscillator. In the context of the first design, carried out in 28-nm CMOS technology, a comparison between a VCO and a digitally-controlled oscillator (DCO) is proposed to understand which frequency tuning technique is more suited for mm-wave frequency synthesis and they are optimized for the lowest power consumption and very large tuning range. In the second design, instead, a quadrature DCO with a seamless tuning technique, based on changing the coupling strength, is proposed. This is an alternative approach to having multiple banks of tuning elements which are tough and time consuming to calibrate in an all-digital PLL (ADPLL) to get a linear and very wide frequency sweep. Low power consumption and very wide bandwidth while preserving the phase noise required by the application and the target constraints. Such DCO is followed by a divider chain with a very wide input frequency range and low power consumption.

This thesis is organized as follows:

- **Chapter 2** describes the modeling and characterization of MOSFETs in advanced CMOS technologies. It consists in the first research direction described above. It starts with the basic equations of the simplified EKV model for long- and short-channel devices. It describes the main small-signal parameters and figures-of-merit versus the *IC*. A simplified extension to fully-depleted silicon-on-insulator (FDSOI) devices is included and the procedure to extract the EKV parameters is reported. Then, the EKV model is used to analyze the distortion in single transistors by means of the Taylor expansion of the drain current. All of the previous topics are described with equations and validated with experimental results. Finally, the design methodology is extended to the modeling of passive devices at mm-wave, including the optimization of the signal distribution and the best layout techniques.
- **Chapter 3** explains the analysis of LC oscillators for a low-power and low-noise design. It represents the second research direction. It starts with the description of the most popular oscillator topologies and then follows with a simulation-based analysis of their power consumption versus the *IC*. The goal is to find the optimum bias point for minimum power and best noise to maximize the figure-of-merit. Finally, a linear analysis of $1/f^2$ phase noise is proposed, including all the noise sources of the transistors. The formulas are then validated with simulations in two different advanced technologies.

- **Chapter 4** focuses on the design of 20-GHz VCO and DCO in 28-nm CMOS technology. First, the basic radar equations are reported and the choice of FMCW over the other modulation schemes is addressed. This allows to define some design specifications for the oscillators. Then, the optimization of the circuit and the resonators is explained, with the details regarding the tuning elements of each bank. The experimental results are presented and compared. Finally, the VCO is included in a 60-GHz radar system built with COTS and range measurements are carried out.

- **Chapter 5** presents the design of a 60-GHz quadrature DCO (QDCO) and divider chain in 22-nm FDSOI technology. First, the ADPLL principle of operation is reported and the advantages of this approach over the analog counterpart are explained. Then, the overall system is described to set the context of the designed blocks. The working principle of frequency tuning through the coupling strength in quadrature oscillators is addressed and the implementation with a 10-bit current-steering digital to analog converter is shown. Finally, the experimental results are reported with the comparison with the state-of-the-art.

- **Chapter 6** concludes the dissertation providing a summary of the main results and achievements and suggesting directions for future research.

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2 Modeling of MOSFETs in Nanoscale CMOS Technologies

In the past 40 years the evolution of CMOS technologies brought the critical dimensions of MOSFETs from more than 1 µm to 5 nm and even below. The increase of the density of devices on chip allowed a dramatic improvement of the performance of digital circuits and enabled new applications. The scaling was a key factor also in the success of rf integrated circuits design with CMOS technologies, thanks to the increase of the peak transit frequency f_T from below 1 GHz to more than 400 GHz [1–3]. Nowadays the development of a SoC for communication or remote sensing can take full advantage of the advanced technologies, integrating a powerful digital signal processor (DSP) with the analog front-end. The choice of a specific technology for a SoC depends on several factors: the implications of the trade-off among performance, area and cost are complex and need to be estimated carefully. Even purely from the development point of view, advanced technologies bring a lot of challenges to the design of analog and rf circuits for achieving the target specifications with the short-channel effects and the layout constraints. Moreover, a lot of different device flavors are available, which increase the spectrum of possibilities for optimization.

A model of the nanoscale devices with simple equations and a limited number of extracted parameters allows designers to have a clear understanding of the circuits and a powerful tool in the preliminary design phase. This is particularly crucial when focusing on low-power applications. The charge-based EKV model is the most suited for this purpose, especially in the simplified form which relies only on a handful of parameters. In this framework, the *IC* is used as an essential design parameter that replaces the overdrive voltage $V_G - V_{T0}$ and spans the entire range of operating points from weak (WI) via moderate (MI) to strong inversion (SI), including the effect of velocity saturation (VS). With a simple extraction procedure, the simplified EKV parameters can be obtain from measured $I_D(V_G)$ and $I_D(V_D)$ characteristics. Then, the small-signal transconductances, such as G_m and G_{ds}, can be expressed as a function of charge and hence of *IC*.

Another crucial aspect in the design of mixed-signal integrated circuits is the linearity of an analog building block. Some examples are operational amplifiers, power amplifiers, low-noise amplifiers, analog-to-digital converters, G_m-C filters, etc., which can be found in sensor in-

terfaces, instrumentation for measurements, audio applications, image sensors and wireless transceivers [4–12]. The improvement of linearity can be achieved by biasing the transistor in SI with a large overdrive voltage $V_{GS} - V_{T0}$, at the cost of a higher power consumption [13]. Moreover, VS is dominant in short-channel devices biased in SI, making their $I_D(V_G)$ characteristic almost perfectly linear. However, it is not possible to benefit from this improvement, due to the maximum overdrive voltage reduction imposed by technology scaling. Indeed, the supply voltage has reduced, while the threshold voltage has almost remained constant to preserve a low channel leakage current. Consequently, the operating point of MOSFETs is progressively pushed towards MI and eventually WI, regimes in which the distortion caused by the nonlinear $I_D(V_G)$ characteristic increases more dramatically. On the other hand, these bias regions are convenient for low-power and low-voltage designs, which are required by applications such as the Internet of Things.

Finally, the definition of a design methodology that merges the schematic and layout stages becomes mandatory when moving to the mm-wave frequency band for the radar application. Indeed, at such frequencies every metal connection on the rf nodes is critical and needs to be carefully evaluated and extracted with electromagnetic (EM) tools. The design process involves several iteration to identify the right trade-off between a comprehensive extraction and a reasonably quick simulation time. Besides, the simulation result is relevant to adjust layout choices to improve the performance and meet the specifications.

In this chapter, first the reasons for choosing GF 22-nm FDSOI for the development of a radar SoC are explained, comparing it with other advanced bulk technologies and presenting the available devices. Then, the simplified EKV equations for long- and short-channel transistors are described and the figures-of-merit (FoMs) for low-power design are calculated and compared to experimental results on 40- and 28-nm bulk devices. A simple extension to FDSOI is proposed and validated with a 22-nm technology. Part of this material in presented in [2, 3]. After that, the harmonic analysis of distortion in MOSFETs based on the simplified EKV is shown and validated with measurements on TSMC 28-nm samples: this material is presented in [14]. Finally, the design approach at mm-wave is described, including the layout techniques and the modeling of the passive devices, the distribution of the critical signals and the parasitics.

2.1 Deep-Submicron CMOS Technologies

With a planar structure, transistors manage to reach down to a gate length $L = 20\,\text{nm}$, both with a standard bulk and a silicon-on-insulator (SOI) process. To reach even smaller sizes, the FinFET technology has to be employed. The latter offer the highest density of devices for digital circuits and excellent performance for analog design. Nevertheless, the cost per wafer is considerable, especially for the most recent processes, and it is affordable only for very high volumes and for high-performance applications. For low-power, where the speed of digital circuits is limited and digital gates even avoid minimum length to keep leakage currents under

control, planar technologies provide a valid solution.

2.1.1 Bulk and FDSOI

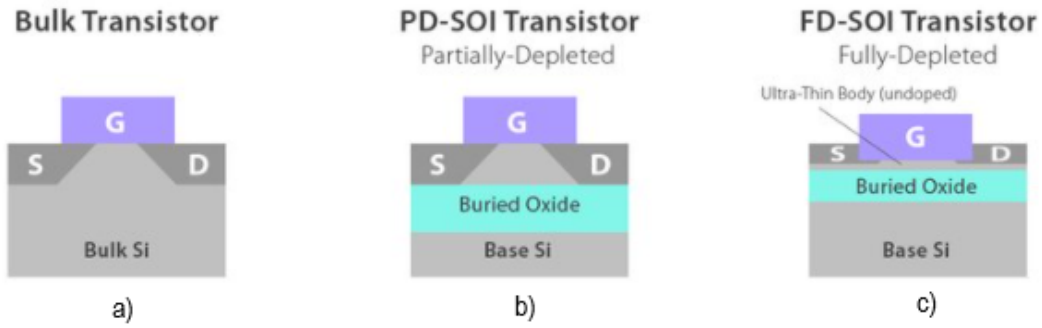


Figure 2.1: Planar CMOS technologies: (a) Bulk, (b) PDSOI and (c) FDSOI [15].

There are two main types of planar commercial CMOS technologies, i.e. the standard bulk and the SOI, in the partially-depleted SOI (PDSOI) and the FDSOI versions. As shown in Fig. 2.1, in the former case devices are fabricated in the bulk of the silicon wafer. The bulk is taken as reference node in the EKV model and it is usually connected to ground voltage. Indeed, the p-n junctions which are generated at the source and drain have to be maintained in reverse bias to prevent a large leakage current. The short-channel effects (SCEs) have risen with the transistor scaling, as the gate has partially lost control of the channel. In fact, since the device length is very small, the portion of inversion charge on which the source and drain have influence is relevant, the channel potential doesn't flatten and it results in a threshold voltage V_{T0} reduction. Moreover, the drain voltage contributes additional V_{T0} shift, effect known as drain-induced barrier lowering (DIBL). On top of that, VS happens due to the extremely high electric field in the channel close to the drain, reducing the maximum drain current. Several process solutions have been found in the years to counter the SCEs and extend the relevance of bulk technologies down to few tens of nm.

Nevertheless, the SOI processes (first the PDSOI and then the FDSOI) represent an alternative answer to partially reduce the impact of SCEs in planar devices. A thick oxide layer separates the bulk silicon and the transistors. The difference between PDSOI and FDSOI lays in the channel thickness and consequently in the portion of it that gets depleted of charges. Indeed, in the former case the devices are fabricated in a rather thick silicon layer, called body, and the gate generates the inversion layer in a similar fashion as in bulk devices. The undepleted portion of the body is left floating and this is the major issue of this technology. Instead, in the latter case an ultra-thin body is grown on top of the oxide and the gate manages to deplete all of it, granting great control on the channel inversion charge and surface potential. The result is a steeper sub-threshold slope and hence lower allowed V_{T0} and better switching performance.

In the SOI technologies the bulk acts as a second gate (back gate): since the source and

drain are above the buried oxide, the bulk voltage can vary without risking leakage currents. The practical effect of the back gate is to shift the threshold voltage allowing to have an additional degree of freedom in the design process. Moreover, higher operating frequencies can be reached thanks to the removal of the parasitic source and drain junction capacitances and lower output conductance is given by the better control of the gate on the channel. Nevertheless, SOI technologies have a weakness in the heat dissipation due to the isolation provided by the buried oxide.

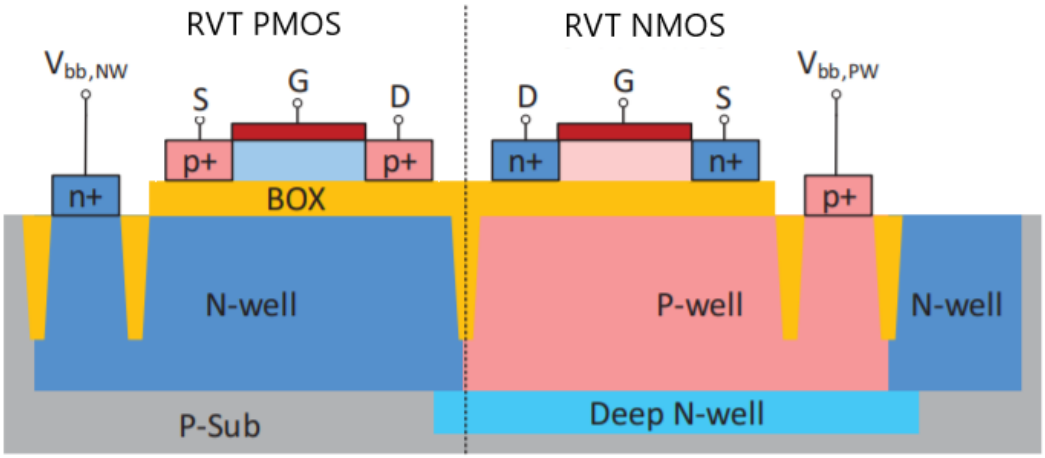
2.1.2 Choice of the CMOS Technology for a Radar SoC: GF 22-nm FDSOI

For the development of the target radar SoC, the GF 22-nm FDSOI technology (22FDX) is chosen [16]. The alternatives are the TSMC 28-nm bulk and the recently released TSMC 22-nm bulk. Both of them are based on the same 30-nm technology on which a different shrinking factor is applied: 0.9 for the former and 0.855 for the latter. At the time when GF 22-nm was chosen for this project, the TSMC 22-nm was not available and the comparison was done with respect to the 28-nm. Nevertheless, as detailed afterwards, the second shrink is beneficial mostly for digital circuits as it aims at increasing the device density offering an alternative to the more expensive FinFET technology. There are not explicit advantages for analog design: due to the limitations of bulk, the intrinsic gain of the devices is low because of the higher output conductance and the SCEs affect the transistors efficiency, especially when biased with a large overdrive voltage.

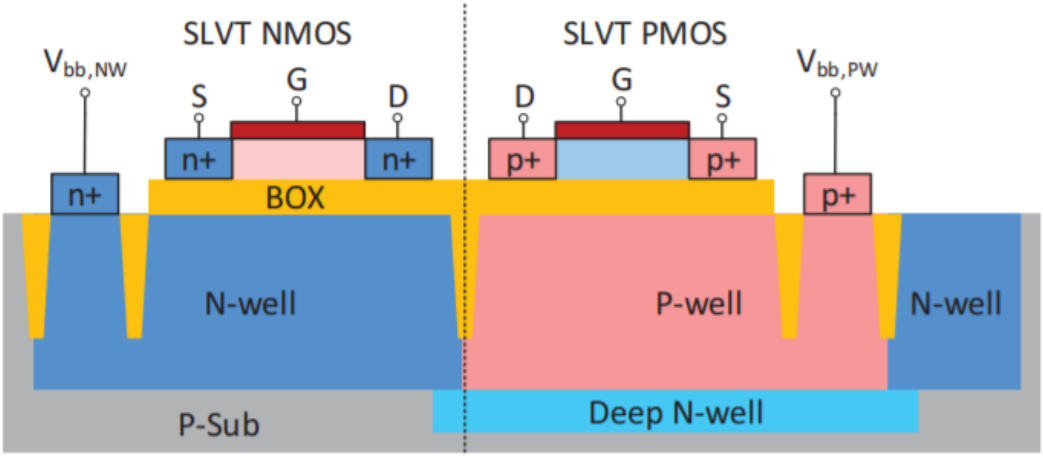
The original fabrication process of the GF 22-nm FDSOI technology manages to satisfy the needs of both the digital and the analog designers. In fact, for the former the bulk biasing can shift the V_{T0} to both higher and lower values, which allows to dynamically adapt the circuit behavior for the low leakage standby mode to the fast switching high performance mode. It can be also used to level the differences coming from PVT variations with automatically adapting biasing blocks. In analog circuits the body voltage allows to get lower V_{T0} compared to similar nodes and hence to increase the voltage headroom for devices, especially considering the low supply voltage of 0.8 V allowed in this technology. Moreover, the output conductance of minimum length devices is improved and hence their intrinsic gain: this is particularly important for rf design, where length is minimized to get minimum gate-source capacitance C_{GS} and highest transit frequency ω_t. p-type devices show superior performance thanks to their SiGe channel. Finally I/O devices for higher voltages are available with a fine granularity, i.e. 1.2 V, 1.5 V and 1.8 V, with increasing minimum gate length, which improves dramatically the design freedom.

2.1.3 Types of Devices in GF 22-nm FDSOI

Thanks to the variety of device types in its library, this technology offers some unique solutions. First of all, there are four flavors of core devices, for both n- and p-type MOSFETs (NMOS and PMOS respectively): two of them are build with a normal-well structure and the other two



(a)



(b)

Figure 2.2: Available device structures in the FDSOI technology: (a) normal-well and (b) flip-well.

with the so-called flip-well structure. As shown in Fig. 2.2, in the former case a NMOS device is built on a P-well and a PMOS on a N-well, while in the latter the NMOS on a N-well and the PMOS on the P-well. The two normal-well flavors are the high threshold voltage (HVT) and the regular threshold voltage transistors (HVT and RVT respectively), while the two flip-well flavors are the low threshold voltage and the super low threshold voltage transistors (LVT and SLVT respectively). The V_{T0} sensitivity to the body bias is around 70 mV/V and the back gate can sustain from -2 to 2 V. In a practical case, there are some limitations to the range of body bias voltages that can be applied for NMOS and PMOS in order to keep the p-n junctions between the wells in reverse bias and because often negative voltages are not available on chip. As far as the I/O devices are concerned, two flavors are available: one with normal-well and one with flip-well (LVT and SLVT respectively). Fig. 2.3 shows the measured $I_D(V_G)$ characteristics with

different back gate voltage V_{BG} for four devices, namely a short- and a long-channel NMOS RVT (nRVT) device and a short- and a long-channel PMOS SLVT (pSLVT) device. The nRVT is a normal-well device and the pSLVT a flip-well one: the former sees a V_{T0} decrease when the V_{BG} increases, while the latter a V_{T0} increase. The opposite happens with nSLVT and pRVT devices respectively. The existence of complementary devices that can share the same well opens up the option of new combination: the most interesting is pairing a high V_{T0} NMOS with a low V_{T0} PMOS for a more balanced structure. In fact, NMOS is naturally stronger in this technology without body bias and in this configuration one could ideally aim for a perfect balance.

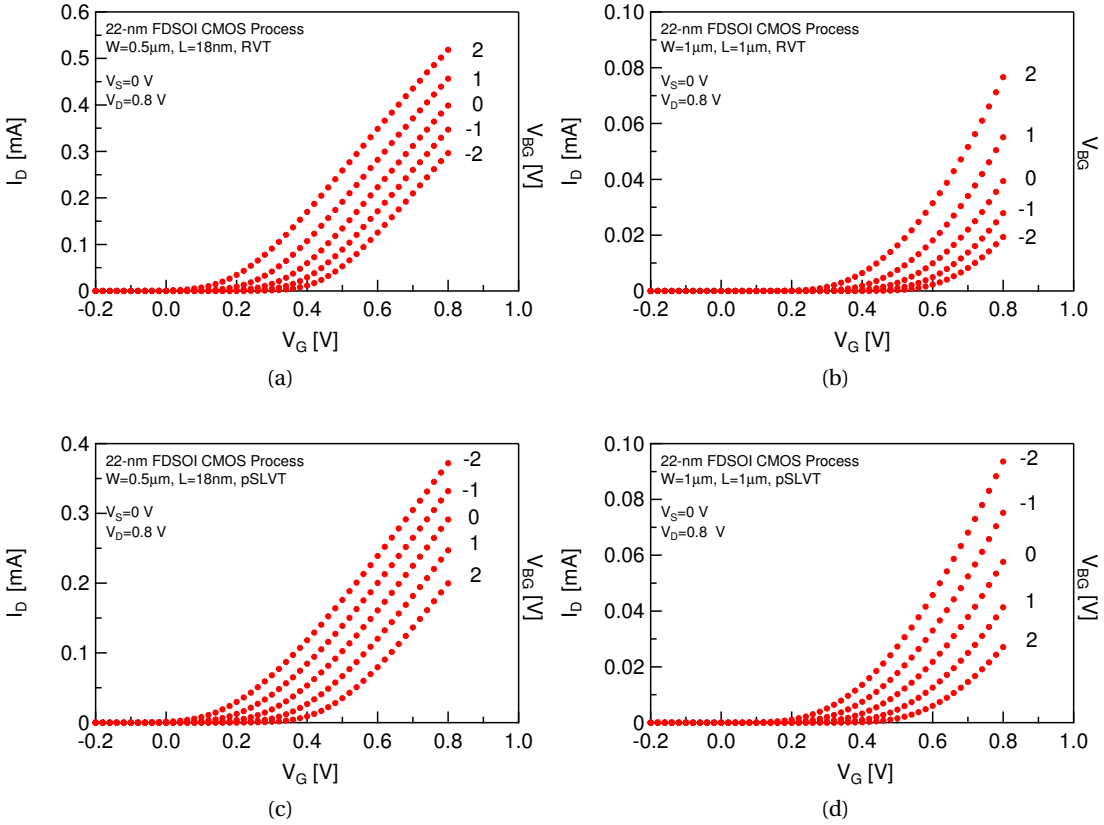


Figure 2.3: $I_D(V_G)$ of four devices in 22-nm FDSOI (a) nRVT with $L = 18\,\text{nm}$ (b) nRVT with $L = 1\,\mu\text{m}$, (c) pSLVT with $L = 18\,\text{nm}$ and (d) pSLVT with $L = 1\,\mu\text{m}$.

2.2 Simplified EKV model for Nanoscale MOS Transistors

The simplified charge-based EKV MOSFET model can be used to model devices in saturation even in advanced CMOS processes with only a few parameters including the effect of VS. It is a symmetrical model with respect to source and drain, since all terminal voltages are referred to the local substrate. The charge-based expression of the drain current I_D is normalized to decouple it from the technology and device specific parameters: it is convenient to handle

normalized quantities to understand the trends of the large-signal and small-signal quantities useful for analog design as functions of the Inversion Coefficient *IC*.

2.2.1 Basic Long-Channel Charge-based Model

The core equations of the simplified model for long-channel MOSFETs are the same as for the complete EKV model [2, 3, 17]:

$$2\,q_\mathrm{i} + \log q_\mathrm{i} = v_\mathrm{p} - v \tag{2.1}$$

$$i_\mathrm{d} = i_\mathrm{f} - i_\mathrm{r} = q_\mathrm{s} + q_\mathrm{s}^2 - q_\mathrm{d} - q_\mathrm{d}^2 \tag{2.2}$$

where q_i is the inversion charge density normalized to the specific charge

$$Q_\mathrm{spec} \triangleq -2nU_\mathrm{T}C_\mathrm{ox}, \tag{2.3}$$

v_p and v are the pinch-off and channel voltages respectively normalized to the thermal voltage $U_\mathrm{T} = kT/q$, i_d is the drain current normalized to the specific current

$$I_\mathrm{spec} = I_{\mathrm{spec}\square}\frac{W}{L} \quad \text{with} \tag{2.4}$$

$$I_{\mathrm{spec}\square} \triangleq 2n\mu_0 C_\mathrm{ox} U_\mathrm{T}^2 \tag{2.5}$$

and q_s and q_d are the value of q_i at source and drain respectively. n is the slope factor, μ_0 is the constant low-field electron mobility and C_ox is the gate capacitance per unit area. Since (2.1) is not invertible analytically, i_d cannot be expressed in closed form as a function of the voltage, unless the expressions are simplified for low or high values of q_i. For this reason, the pinch-off voltage $V_\mathrm{P} = (V_\mathrm{G} - V_\mathrm{T0})/n$ is not a convenient way to explore all the bias regions of the MOSFET. Indeed, the proposed method relies on the metric that allows to precisely address the channel inversion level of a MOSFET, namely the inversion coefficient *IC*,

$$IC \triangleq \frac{I_\mathrm{D}|_\mathrm{saturation}}{I_\mathrm{spec}} = i_\mathrm{d,sat}. \tag{2.6}$$

Note that being normalized to I_spec, *IC* strips off any size and technology dependence. Using *IC*, the different regions of operation of a MOSFET can be classified as illustrated in Fig. 2.4 and defined as

$$IC < 0.1 : \text{Weak Inversion (WI)}$$
$$0.1 < IC < 10 : \text{Moderate Inversion (MI)}$$
$$IC > 10 : \text{Strong Inversion (SI)}$$

In long-channel devices, q_d vanishes at pinch-off giving

$$i_\mathrm{d,sat} = q_\mathrm{s} + q_\mathrm{s}^2. \tag{2.7}$$

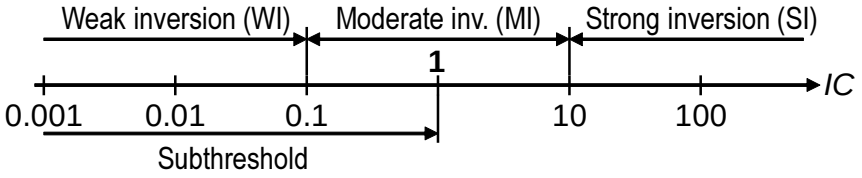


Figure 2.4: Regions of operation in terms of inversion coefficient.

2.2.2 Simplified Charge-based Model for Short-Channel Bulk MOS Transistors

In the most advanced technology nodes, (2.7) fails in describing correctly the behavior of minimum- and close-to-minimum-length devices due to VS, which has a dramatic impact on the drain current and hence on the transconductance. Indeed, the electron mobility μ is not constant for high values of horizontal electric field in the channel E_x: the shorter the channel, the more this phenomenon affects negatively the devices performance. Consequently, (2.2) is not valid anymore, being it derived from the drift-diffusion equation without including VS. It is necessary to go back to the drift-diffusion equation and to solve it including the bias dependence of the mobility. The mobility reduction caused by high values of the vertical electric field is not taken into account in this work. There are several models to describe the dependence of the effective electron mobility μ_eff on E_x: in this work a simple piece-wise linear model is employed,

$$\mu_\mathrm{eff}(E_\mathrm{x}) \triangleq \frac{v_\mathrm{drift}}{|E_\mathrm{x}|} = \begin{cases} \mu_0 & \text{for } \mathrm{E_x} < \mathrm{E_c} \\ v_\mathrm{sat}/|E_\mathrm{x}| & \text{for } \mathrm{E_x} \geq \mathrm{E_c} \end{cases} \tag{2.8}$$

where v_sat is the maximum electron velocity and E_c is the critical electric field, which depends only on the substrate properties,

$$E_\mathrm{c} \triangleq \frac{v_\mathrm{sat}}{\mu_0}. \tag{2.9}$$

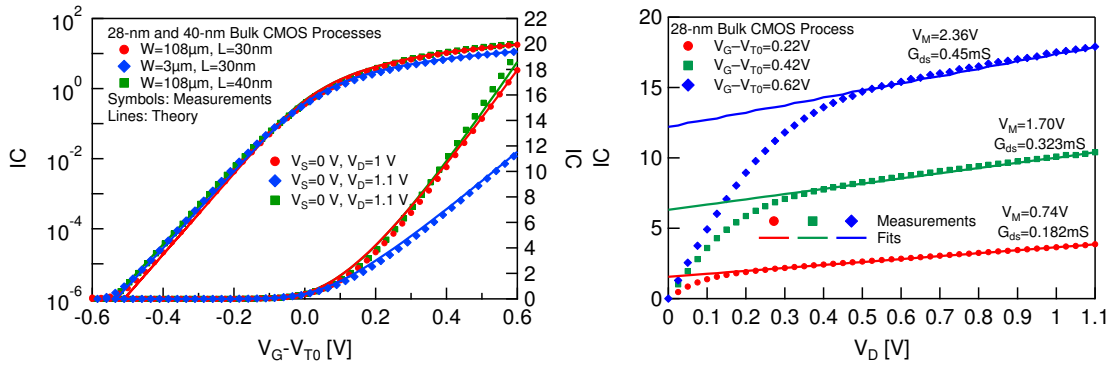
Including this model in the drift-diffusion equation leads to the same expression as (2.2); nevertheless, in this case VS happens before pinch-off and hence q_d saturates to $q_\mathrm{d,sat}$, which is a specific value set by the bias conditions and the channel length [17]. If $q_\mathrm{d,sat}$ is expressed in terms of q_s, $i_\mathrm{d,sat}$ then becomes [2, 3, 18]

$$q_\mathrm{d,sat} = \frac{2\lambda_\mathrm{c}\left(q_\mathrm{s}+q_\mathrm{s}^2\right)}{2+\lambda_\mathrm{c}+\sqrt{4\left(1+\lambda_\mathrm{c}\right)+\lambda_\mathrm{c}^2\left(1+2q_\mathrm{s}\right)^2}} \tag{2.10}$$

$$i_\mathrm{d,sat} = \frac{4\left(q_\mathrm{s}+q_\mathrm{s}^2\right)}{2+\lambda_\mathrm{c}+\sqrt{4\left(1+\lambda_\mathrm{c}\right)+\lambda_\mathrm{c}^2\left(1+2q_\mathrm{s}\right)^2}} \tag{2.11}$$

where

$$\lambda_\mathrm{c} = \frac{L_\mathrm{sat}}{L} \tag{2.12}$$



(a) (b)

Figure 2.5: (a) IC versus the overdrive voltage $V_G - V_{T0}$ measured in saturation on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes. (b) IC versus V_D measured for different overdrive voltages on a minimum length transistor 30-nm from a 28-nm bulk CMOS processes.

is the fraction of the channel under full velocity saturation which scales as $1/L$ and L_{sat} the saturated portion of the channel. L_{sat} is another technology parameter extracted from measurements and it is ideally unique for any transistor length. Consequently, it allows to transit smoothly from the drain current for short-channel devices (2.11) to the one for long-channel devices (2.7). Since this simplified EKV model is built on normalized quantities, it has the advantage of being independent from any technology. In fact, in order to employ it, only four technology parameters are needed: $I_{spec_\square}$, n, V_{T0} and L_{sat}. They can be easily extracted from the measured $I_D(V_G)$ characteristic of the device of interest as explained in Section 2.2.6. These parameters allow to normalize the input terminal voltages and to denormalize the drain current.

The IC versus $V_G - V_{T0}$ transfer characteristics are plotted in Fig. 2.5a and compared to measurements made on wide and minimal length transistors from three different processes, namely a 40-nm and two different 28-nm bulk CMOS processes. Although the drain current is measured from sweeping the gate voltage, the simplified EKV model is calculated from the measured current by first normalizing it to the specific current for each transistor to get the inversion coefficients, from which the overdrive voltages are computed using (2.11) and (2.1). Despite the very few number of parameters, the simple model fits the measurements very well over more than six decades of current. Note that the extraction of the parameters $I_{spec_\square}$ and L_{sat} is done for several different geometries (in particular different length) illustrating the rather good scalability of the simplified model. Notice that the measured points and analytical models of the $W = 108\,\mu m$, $L = 30\,nm$ (red circles) and $W = 108\,\mu m$, $L = 40\,nm$ (green squares) transistors almost fall on top of each other, indicating that the normalization almost completely strips off the technology dependence. The difference with the $W = 3\,\mu m$, $L = 30\,nm$ (blue diamond) characteristic is due to a slightly larger value of λ_c. In other words, the four parameters almost fully characterize the technology at least for the transfer characteristics in saturation and in

the regions of operation used for analog circuit design.

The large-signal output characteristic in the saturation region has always been the most difficult part to model due to a combination of several effects including VS, channel length modulation (CLM) and DIBL. Fig. 2.5b shows the inversion coefficient versus the drain voltage for different overdrive voltages measured on a large and minimal length transistor from a 28-nm process. It shows that the current can be approximated in saturation by a simple linear characteristics

$$I_D \cong G_{ds} \cdot (V_D + V_M), \tag{2.13}$$

where V_M is the channel length modulation (CLM) (or Early) voltage[1] and G_{ds} is the output conductance which corresponds to the slope and is discussed further in the next section.

2.2.3 The Small-Signal Model

The most important small-signal parameter is without doubt the gate transconductance G_m. Since in the EKV model the voltages are all referred to the bulk, we can define two other transconductances: the source transconductance $G_{ms} \triangleq -\partial I_D/\partial V_S$ and the drain transconductance $G_{md} \triangleq \partial I_D/\partial V_D$ [17]. Note that G_{md} should not be confused with the output conductance G_{ds}. In saturation $G_{md} = 0$ and $G_{ms} = n \cdot G_m$. The normalized source transconductance in saturation g_{ms} can be expressed in terms of IC as [18, 19]

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{n \cdot G_m}{G_{spec}} = \frac{\sqrt{(\lambda_c IC+1)^2+4IC}-1}{\lambda_c(\lambda_c IC+1)+2}, \tag{2.14}$$

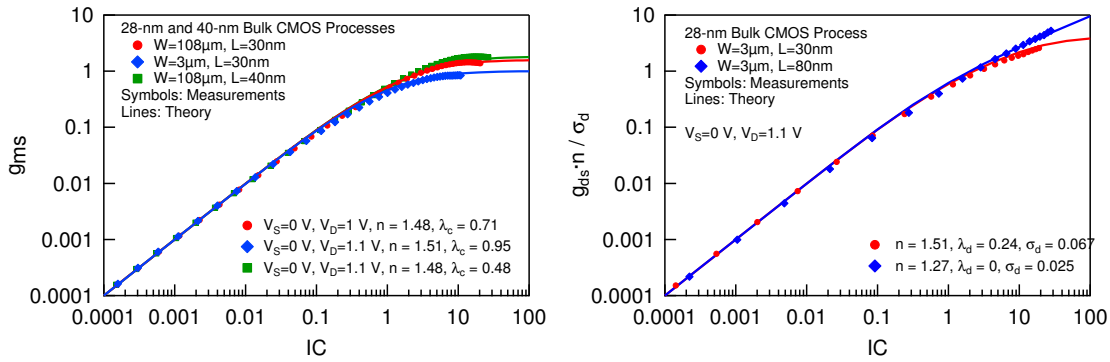
where $G_{spec} \triangleq I_{spec}/U_T = 2n\mu_0 C_{ox} U_T$. Note that for short-channel devices in SI, the $I_D(V_G)$ transfer characteristic becomes a linear function of the gate voltage as illustrated in Fig. 2.5a and hence the gate transconductance becomes independent of the drain current and of the gate length L. It then only depends on W and v_{sat} according to

$$g_{ms} \cong 1/\lambda_c \text{ for } IC \gg 1 \quad \text{or} \quad G_m \cong WC_{ox}v_{sat}. \tag{2.15}$$

The inverse of the VS parameter $\lambda_c$is therefore a key parameter since it gives the maximum normalized transconductance that can be achieved for a short-channel device in a given technology.

The other key small-signal parameter is the output conductance G_{ds} which, together with the transconductance, defines the intrinsic (or self) gain G_m/G_{ds}. As mentioned above, the output conductance is the result of several physical effects including VS, CLM and DIBL. In advanced short-channel devices biased in MI or WI, DIBL is the dominant effect. The latter is defined as the variation of the threshold voltage with respect to the applied drain-to-source voltage, i.e.

[1] Note that even though the parameter V_M is called the CLM voltage, it actually embeds all the effects, including VS and DIBL, which is actually dominant in WI.



(a) (b)

Figure 2.6: (a) Normalized transconductance g_{ms} versus IC measured on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes. (b) Normalized output conductance g_{ds} versus IC measured on minimum and medium length transistors from a 28-nm bulk CMOS process.

$\partial V_T/\partial V_{DS}$ and can be modeled as [20–22]

$$V_T \cong V_{T0} - \sigma_d \cdot V_{DS}, \tag{2.16}$$

where the parameter $\sigma_d \triangleq -\partial V_T/\partial V_{DS}$ accounts for DIBL and depends on L and V_S [21, 22]. The output conductance can then be written as [23]

$$G_{ds} \triangleq \frac{\partial I_D}{\partial V_{DS}} = \frac{\partial I_D}{\partial V_T} \cdot \frac{\partial V_T}{\partial V_{DS}} = \sigma_d \cdot G_m, \tag{2.17}$$

where $\partial I_D/\partial V_T = -G_m$ has been used. A model of the output conductance versus IC can now be derived using the expression of $G_m = G_{ms}/n$ in saturation given in (2.14), where λ_c is replaced by an additional parameter λ_d

$$g_{ds} \triangleq \frac{G_{ds}}{G_{spec}} = \frac{\sigma_d}{n} \cdot \frac{\sqrt{(\lambda_d IC+1)^2+4IC}-1}{\lambda_d(\lambda_d IC+1)+2}. \tag{2.18}$$

The normalized output conductance versus IC given by (2.18), multiplied by the factor n/σ_d, is plotted in Fig. 2.6b and compared to measurements made on a long and a short transistor from a 28-nm CMOS process. The model fits very well the measured data over more than five decades of current despite its simplicity.

2.2.4 The Transconductance Efficiency

The transconductance efficiency G_m/I_D, sometimes also called the current efficiency, is one of the most important FoM for low-power analog circuit design. It is a measure of how much transconductance is produced for a given bias current and is a function of IC. The transcon-

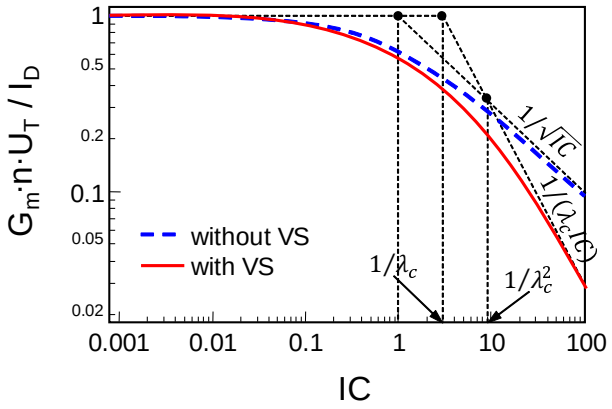


Figure 2.7: g_{ms}/i_d vs. IC showing the long and short channel asymptotes.

ductance efficiency (or its inverse) appears in many expressions related to the optimization of analog circuits. In normalized form, the transconductance efficiency is defined as the actual transconductance obtained at a given IC with respect to the maximum transconductance $G_m = I_D/(nU_T)$ reached in WI [18, 19]

$$\frac{g_{ms}}{IC} = \frac{G_m \cdot nU_T}{I_D} = \frac{\sqrt{(\lambda_c IC+1)^2+4IC}-1}{IC\cdot[\lambda_c(\lambda_c IC+1)+2]}. \tag{2.19}$$

The expression in (2.19), which is continuous from WI to SI and includes the effect of VS, is plotted in Fig. 2.7. The figure shows that $G_m nU_T/I_D$ is maximum in WI and decreases as $1/\sqrt{IC}$ in SI for long-channel devices in which VS is absent (dashed blue curve). Note that the specific current has been defined from the $G_m nU_T/I_D$ versus I_D characteristic of a long channel transistor as the current at which the WI and SI asymptotes cross. This is why these two asymptotes cross at $IC = 1$ when $G_m nU_T/I_D$ is plotted versus IC as in Fig. 2.7.

As shown in Fig. 2.5a, for short-channel devices subject to VS, the drain current in SI becomes a linear function of the gate voltage, independent of the transistor length. Hence, the transconductance becomes independent of the current and of the length. Since G_m becomes independent of I_D, and hence of IC, the $G_m nU_T/I_D$ curve scales like $1/(\lambda_c IC)$ in SI (red curve) instead of $1/\sqrt{IC}$ when VS is absent. In essence, the effect of VS is to degrade the transconductance efficiency in SI, meaning that more current is required to obtain the same transconductance than without VS. Nevertheless, irrespective of the channel length, $G_m nU_T/I_D$ remains invariant (i.e. $g_{ms}/IC = 1$) in WI, since SCEs, including VS, have the same effect on G_m than on I_D simply because G_m is proportional to I_D in WI. As shown in Fig. 2.7, the inversion coefficient for which the SI asymptote of a short-channel device crosses the horizontal unity line is equal to $1/\lambda_c$.

The normalized transconductance efficiency given by (2.19) is compared to measurements in Fig. 2.8a for the same devices as shown in Fig. 2.5a and Fig. 2.6a. Despite the $G_m nU_T/I_D$ only requires one parameter (λ_c or L_{sat}), the model fits very well to the data over more than five

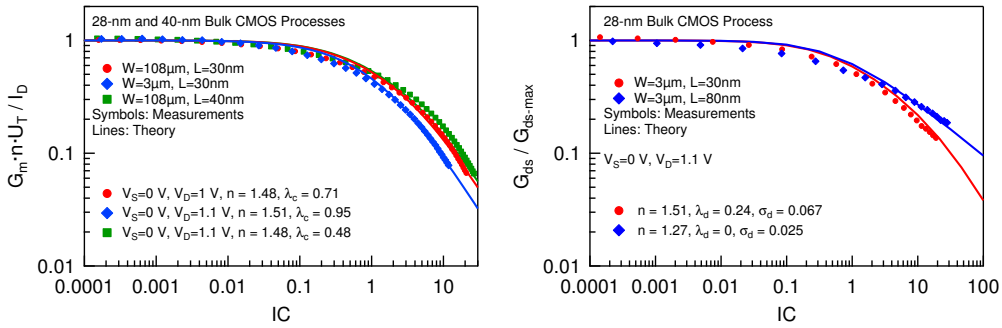


Figure 2.8: (a) Normalized transconductance efficiency g_{ms}/IC versus IC measured on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes. (b) Normalized output conductance efficiency g_{ds}/IC versus IC measured on minimum and medium length transistors from a 28-nm bulk CMOS process.

decades of IC.

In a similar way, we can define the G_{ds}/I_D ratio, which from (2.13) turns out to be about equal to $1/V_M$ for $V_D \ll V_M$. In normalized form, we have

$$\frac{U_T}{V_M} \cong \frac{G_{ds}U_T}{I_D} = \frac{g_{ds}}{IC} = \frac{\sigma_d}{n} \cdot \frac{\sqrt{(\lambda_d IC+1)^2+4IC}-1}{IC\cdot[\lambda_d(\lambda_d IC+1)+2]}. \tag{2.20}$$

From (2.20), we can deduce that the highest output conductance for a given current is reached in WI and is equal to $G_{ds,max} \triangleq \sigma_d I_D/(nU_T)$. We can then normalize the output conductance to $G_{ds,max}$ in order for the normalized output conductance to reach unity in WI

$$\frac{G_{ds}}{G_{ds,max}} = \frac{n}{\sigma_d} \cdot \frac{g_{ds}}{IC} = \frac{\sqrt{(\lambda_d IC+1)^2+4IC}-1}{IC\cdot[\lambda_d(\lambda_d IC+1)+2]}. \tag{2.21}$$

Expression (2.21) is plotted in Fig. 2.8b and compared to measurements made on the same transistors than in Fig. 2.6b and shows good agreement with the measured data. Note that, unlike for the transconductance, where we want to get the highest transconductance for a given current which is reached in WI, the output conductance should be minimized for a given current.

2.2.5 Extension of the Simplified Charge-based Model for FDSOI Transistors

Although the simplified model described above was developed for transistors fabricated in a bulk CMOS process, it can also be used for transistors fabricated in a FDSOI process. However, it does not model the effect of the additional back gate available in FDSOI processes and the extracted parameters would be valid only for a single back gate voltage. An example of IC versus $V_G - V_{T0}$ and $G_m = I_D/(nU_T)$ versus IC measured on three different transistor lengths

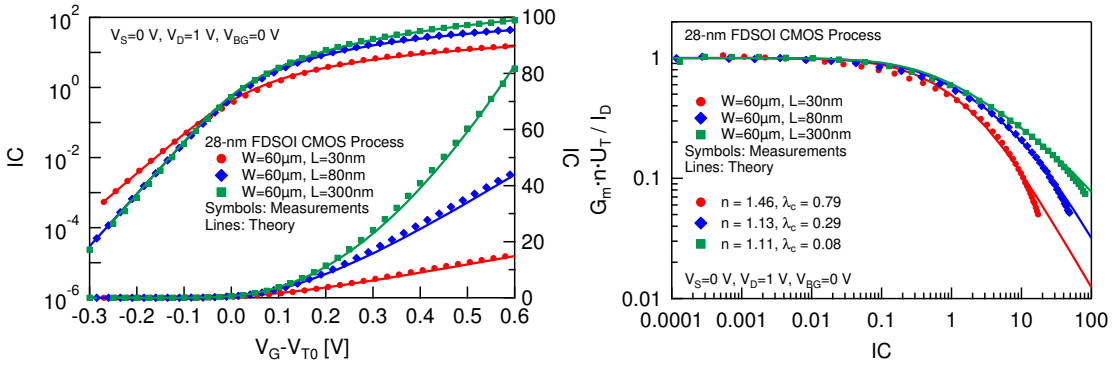


Figure 2.9: The simplified EKV model applied to a 28-nm FDSOI CMOS process. a) IC versus $V_G - V_{T0}$ and b) $G_m n U_T / I_D$ versus IC for three different transistor length.

	28-nm Bulk		22-nm FDSOI	
	$L = 30\,\text{nm}$	$L = 1\,\mu\text{m}$	$L = 18\,\text{nm}$	$L = 1\,\mu\text{m}$
$I_{spec\square}$	1.07 µA	850 µA	520 nA	850 nA
n	1.6	1.16	1.29	1.05
V_{T0}	490 mV	430 mV	250 mV	410 mV
L_{sat}	14.5 nm		5.4 nm	
σ_d	0.067		0.046	
λ_d	0.24		0.226	

Table 2.1: The parameters of the simplified EKV from a 28-nm bulk and a 22-nm FDSOI technology

from a 28-nm FDSOI process are shown in Fig. 2.9. Except for some deviation observed on the $G_m n U_T / I_D$ versus IC at high IC values, which is probably due to additional mobility reduction due to vertical field, the match between the model and the measured characteristics is surprisingly good. Another example of g_{ms}, $G_m n U_T / I_D$, $g_{ds} n / \sigma_d$ and $G_{ds} / G_{ds,max}$ versus IC on NMOS devices with three different transistor lengths from a 22-nm FDSOI technology are provided in Fig. 2.10. It is notable that the behavior of the normalized output conductance changes drastically between a minimum length device to a slightly longer one, i.e. from $L = 18\,\text{nm}$ to $L = 28\,\text{nm}$. The fitting parameter λ_d is reduced to 0 in the latter case and σ_d is halved. The control over the channel in FDSOI technology improves very quickly with L.

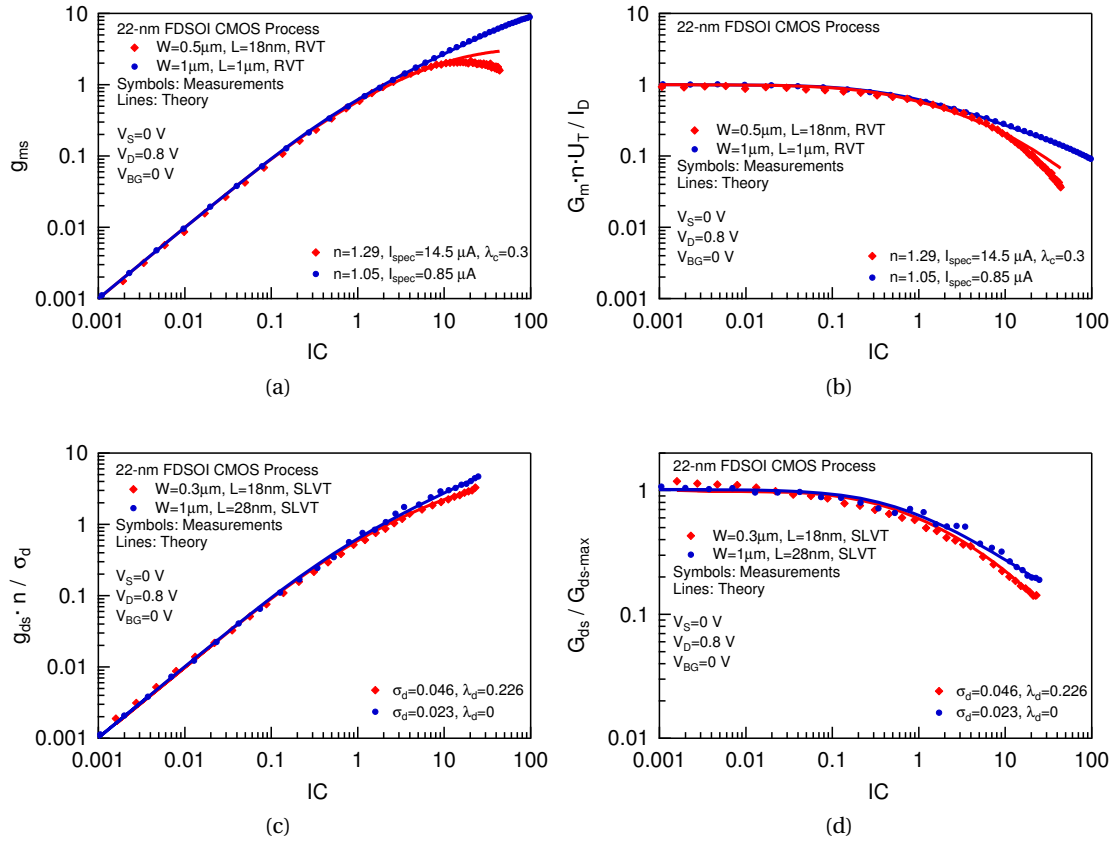
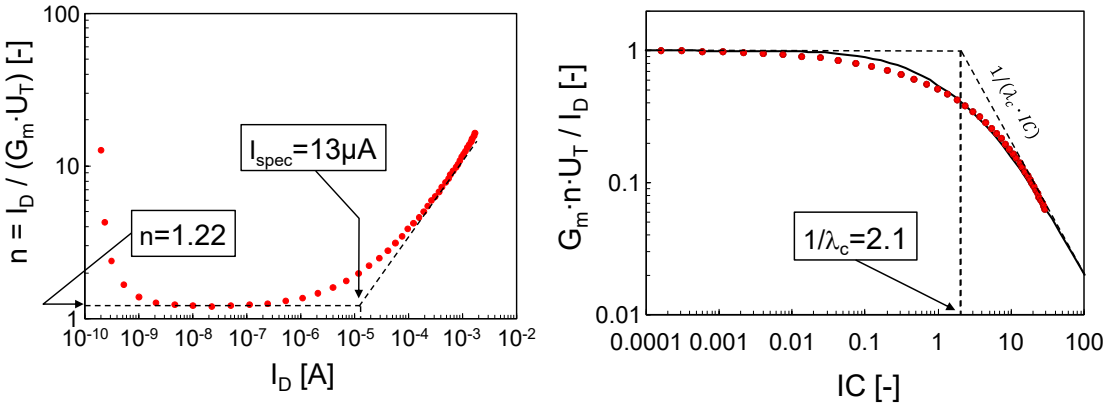


Figure 2.10: The simplified EKV model applied to a 22-nm FDSOI CMOS process. (a) g_{ms}, (b) $G_{\mathrm{m}}nU_{\mathrm{T}}/I_{\mathrm{D}}$, (c) $g_{\mathrm{ds}}n/\sigma_{\mathrm{d}}$ and d) $G_{\mathrm{ds}}/G_{\mathrm{ds,max}}$ versus IC for three different transistor length.

2.2.6 Simplified EKV Parameters Extraction

The four parameters n, I_{spec}, V_{T0} and L_{sat} required for fitting the simplified model described in Section 2.2.2 to measured $I_{\mathrm{D}}(V_{\mathrm{G}})$ data can be extracted from measurements following the procedure described below [2]. The extraction starts from the $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristic measured on a wide and long transistor. After calculating (or measuring) the derivative G_{m} , the slope factor n is extracted from the plateau reached by the $I_{\mathrm{D}}/(G_{\mathrm{m}}U_{\mathrm{T}})$ curve in WI as in Fig. 2.11a. As shown in the same figure, the specific current for this particular device is then obtained by the intersection between the SI asymptote $\propto I_{\mathrm{D}}$ and the slope factor horizontal line. We can derive the specific current per square $I_{\mathrm{spec}_{\square}}$ by dividing I_{spec} by the aspect ratio W/L. The VS parameter λ_{c} is extracted in Fig. 2.11b from the normalized $G_{\mathrm{m}}nU_{\mathrm{T}}/I_{\mathrm{D}}$ characteristic of a wide and short-channel transistor as the IC corresponding to the intersection of the $1/IC$ asymptote with the unity horizontal line after having properly extracted the slope factor n, which is usually affected by SCEs. Finally, the threshold voltage is extracted from the $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristic to fit the measured data as shown in Fig. 2.5a. In addition, the DIBL parameter σ_{d} used for the output conductance can be extracted in a similar way than the



(a) (b)

Figure 2.11: (a) Extraction of the slope factor n and the specific current I_{spec}. (b) Extraction of λ_c on a short device.

slope factor n by looking at the plateau of the normalized $G_{\text{ds}}nU_{\text{T}}/I_{\text{D}}$ curve reached in WI, while the λ_{d} parameter can be extracted in a similar way than the VS parameter λ_{c} from the normalized $G_{\text{ds}}/G_{\text{ds,max}}$ given by (2.21) for a short transistor. Table 2.1 shows the 4 parameters extracted from sample NMOS transistors with long-and short-channel in a 28-nm bulk and 22-nm FDSOI technology. In principle the I_{spec} is unique and extracted from the long-channel devices as explained above. Nevertheless, due to effects that are not accounted for in this simplified model, its value varies to obtain a better fit.

2.3 Analysis of Distortion in Nanoscale MOS Transistors

The analysis of the harmonic distortion in devices and building blocks has been a research topic for decades [13, 24–28]. In [13], Sansen carried out one of the first systematic distortion analysis on BJTs and MOSFETs in order to explain the origin of frequency spurs in telecommunication circuits. Moreover, in this work all the metrics related to one-tone and two-tone analyses were defined. In [24] a comparison in terms of rf performance among several CMOS nodes (from 350-nm to 50-nm) was presented. The third-order Input Intercept Point was derived using the first- and third-order gate transconductances G_{m1} and G_{m3} obtained from dc measurements. In [25] Kang et al. took into account also the nonlinear behavior of the output conductance G_{ds} in the Taylor expansion of the drain current. They used the BSIM3 model and compared the simulated results with measurements on 180- and 250-nm devices. In [26] both G_{m} and G_{ds} nonlinearity were accounted for: the inclusion of cross-terms in the Taylor expansion allowed to optimize the design of a LNA with 65-nm devices reducing the second-order distortion. In [27] Cheng et al. presented a general model for weak nonlinearity which takes into account all nonlinear sources in the MOSFET, namely both transconductances and parasitic capacitances. They used the PSP model and measured devices and circuits in 90-nm node. In [28] Jespers and Murmann used the core long-channel equations of EKV model in

order to express the first-, second- and third-order gate transconductances as a function of the normalized inversion charge and then of the transconductance efficiency G_m/I_D. Moreover, they took into account also the non-linearity introduced by $G_{ds.}$ The analytical results were compared to simulations carried out with the PSP model. However, their approach is proposing a design methodology using G_m/I_D as the main design parameter. The current density is then obtained from G_m/I_D through simulations with a compact model that includes VS and second-order effects. Although this design methodology is effective, it actually relies on a compact model. Instead, the approach proposed in this section is a simple self-consistent model that includes the impact of VS on distortion without requiring any compact model.

Taking advantage of the theory developed about MOSFETs non-linearity in the literature aforementioned, improvements can be introduced in the transistor model, in order to describe more accurately the harmonic distortion behavior in all the bias regions. Besides, it is important to keep the analysis simple, making it a powerful tool in the design phase. When dealing with older technology nodes, MOSFETs behavior is well-described by the quadratic $I_D(V_G)$ expression in SI and by the exponential one in WI. The latter shows better transconductance efficiency with respect to the former, which means higher transconductance for a given current, at the cost of larger area. On the other hand, if linearity is the strongest limitation, SI is the optimal choice. Nevertheless, in the case of nanoscale technologies, the old models are not suited anymore to describe the MOSFET behavior due to the presence of VS. This is the reason why it is important to analyze the linearity performance of advanced technologies by means of a model which takes into account this effect. On the other hand, as mentioned above, the same model should be essential enough to keep the analysis simple and the results easily employed in the design process.

Following the work in [28], the best choice would be to exploit the core equations of the simplified charge-based EKV model, since they would allow to characterize the devices in all bias regions, from WI to SI [2]. Consequently, the metrics associated to the distortion analysis could be formulated as a function of *IC*. Moreover, the goal is to capture accurately the behavior of the non-linearity associated to G_m at low frequencies. In several circuits with current outputs this one is assumed to be the dominant contribution to the overall harmonic distortion. One of the most common examples of this class of circuits is the operational transconductance amplifier (OTA) [29], which is used in several systems, such as G_m-C filters and switched-capacitor circuits. Even though several nonlinearities arise as the operation frequency increases, i.e. those related to the parasitic capacitances of the MOSFET, they are typically much smaller than the non-linearity introduced by the transconductance, as shown in [30]. This is valid especially in MI and WI, which are almost the only choices in a nanoscale technology. For $V_D > V_{D,sat}$, I_D is taken constant in this model, neglecting the effect of CLM and DIBL. Nevertheless, this choice has little impact on the following analysis: V_D is kept constant in the experimental setup by using a TIA at the drain of the device-under-test (DUT), behaving as an ac ground. Consequently, the impact of the output conductance G_{ds} is minimized. For the same reason, also the junction capacitance C_{DB} doesn't contribute with additional non-linearity. Nevertheless, due to the assumption of low-frequency operation, the

contribution of all parasitic capacitances is negligible.

2.3.1 Harmonic Analysis of Distortion based on Simplified EKV Model

For the scope of this analysis, only the saturation region of the MOSFET is taken into account and $i_d = i_{d,sat}$. At the gate, the input voltage $V_G = V_{G0} + \Delta V_G$ provides both the bias and the signal. In order to describe the large-signal ac behavior of the MOSFET, first the nonlinear relation between I_D and V_G is expressed in the form of a Taylor expansion around the bias point of the device:

$$I_D = \sum_{k=0}^{\infty} \frac{1}{k!} \frac{\partial^k I_D}{\partial V_G^k}\bigg|_{V_{G0}} \Delta V_G^k = \sum_{k=0}^{\infty} \frac{1}{k!} G_{mk}\, \Delta V_G^k, \tag{2.22}$$

where G_{mk} is the gate transconductance of order k. Being under low distortion conditions [13], (2.22) can be approximated to the third-order:

$$I_D \simeq I_{D0} + G_{m1}\Delta V_G + \frac{G_{m2}}{2}\Delta V_G^2 + \frac{G_{m3}}{6}\Delta V_G^3. \tag{2.23}$$

This choice allows to take into account the effect of both even and odd order harmonics, trading off accuracy and complexity. It has to be noted that in case of strongly nonlinear behaviors, this approximation would provide inaccurate results. Two different analyses are carried out, namely with a one-tone input signal and with a two-tone one.

One-tone analysis

Assuming the input voltage signal to be $\Delta V_G|_I = A\cos(\omega t)$, (2.23) can be decomposed in terms of the three harmonic components [13]:

$$I_D|_I \simeq I_{D(0)}|_I + I_{D(1)}|_I \cdot \cos(\omega t) + I_{D(2)}|_I \cdot \cos(2\omega t) + I_{D(3)}|_I \cdot \cos(3\omega t), \tag{2.24}$$

where

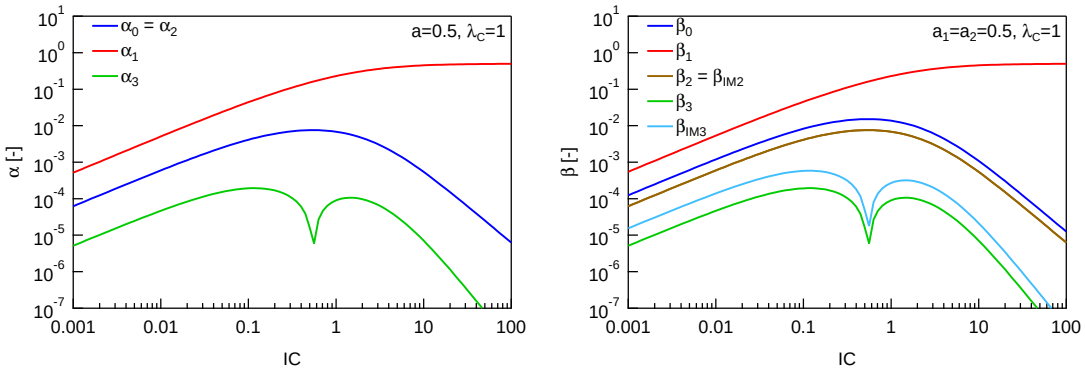
$$I_{D(0)}|_I = I_{D0} + \frac{G_{m2} A^2}{4}, \tag{2.25}$$

$$I_{D(1)}|_I = G_{m1} A + \frac{G_{m3} A^3}{8}, \tag{2.26}$$

$$I_{D(2)}|_I = \frac{G_{m2} A^2}{4}, \tag{2.27}$$

$$I_{D(3)}|_I = \frac{G_{m3} A^3}{24}. \tag{2.28}$$

These formulas show that the second-order nonlinear term in (2.23) generates a dc offset while the third-order one influences the fundamental, either decreasing (compression) or increasing its amplitude (expansion) depending on the sign of G_{m3}. This behavior can be generalized to all nonlinear terms of order higher than three as follows: even-order terms contribute to dc



(a) (b)

Figure 2.12: Amplitude of the harmonics of the output current normalized to I_{spec}in the case of (a) one-tone and (b) two-tone analyses.

offset while odd-order ones affect the fundamental.

In order to quantify the linearity performance of a device, several metrics can be derived from the output tone amplitudes in (2.26)-(2.28). First, the second-order and third-order harmonic distortion parameters, i.e. HD_2 and HD_3, are defined as the ratio of the amplitude of the second and third harmonic versus the amplitude of the fundamental respectively:

$$HD_2 \triangleq \left|\frac{I_{D(2)}|_I}{I_{D(1)}|_I}\right| = \frac{2G_{m2}A}{8G_{m1}+G_{m3}A^2} \tag{2.29}$$

$$HD_3 \triangleq \left|\frac{I_{D(3)}|_I}{I_{D(1)}|_I}\right| = \frac{G_{m3}A^2}{3(8G_{m1}+G_{m3}A^2)}. \tag{2.30}$$

Note that, in order to keep these expressions as general as possible, $I_{D(1)}|_I$ should not be approximated with the ideal value $G_{m1}A$ because the additional term $G_{m3}A^3$ may be relevant to achieve a better accuracy. The disadvantage of these two parameters is that they depend on the input signal amplitude: they cannot describe the performance of a device or a circuit with an unique value. On the contrary, this is achieved by another metric, the 1 dB compression (expansion) point $A_{\mp 1dB}$, defined as the input amplitude for which the fundamental tone in the output signal, $I_{D(1)}|_I$ is reduced (increased) by 1 dB with respect to the ideal value, $G_{m1}A$:

$$A_{\mp 1dB} = \sqrt{\pm\left(1-10^{\mp\frac{1}{20}}\right)\left|\frac{8G_{m1}}{G_{m3}}\right|}. \tag{2.31}$$

Two-tone analysis

Assuming the input voltage signal to be $\Delta V_G|_{II} = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)$, (2.23) can be decomposed accordingly as $I_D|_{II}$ in terms of the harmonic components, which are reported in

Appendix A [13]. Several metrics can be calculated also in the case of two-tone analysis. The most valuable parameters are the second-order and third-order intercept point, A_{IP2} and A_{IP3} respectively, defined as the input amplitude for which the ideal fundamental tone, $G_{\mathrm{m1}}A_1$ (or $G_{\mathrm{m1}}A_2$), and the second- or third-order inter-modulation product, $I_{\mathrm{D(IM2)}}|_{\mathrm{II}}$ and $I_{\mathrm{D(IM3,1)}}|_{\mathrm{II}}$ (or $I_{\mathrm{D(IM3,2)}}|_{\mathrm{II}}$) respectively, have the same amplitude in the output signal. Assuming $A = A_1 = A_2$, they are expressed as

$$A_{\mathrm{IP2}} = 2\left|\frac{G_{\mathrm{m1}}}{G_{\mathrm{m2}}}\right| \tag{2.32}$$

$$A_{\mathrm{IP3}} = \sqrt{8\left|\frac{G_{\mathrm{m1}}}{G_{\mathrm{m3}}}\right|} \tag{2.33}$$

Derivation of the normalized transconductances

An analytical expression of the harmonic coefficients, and consequently all the metrics defined in the previous section, as a function of *IC*, can be calculated by means of the simplified EKV model. First, the normalized form of G_{m1}, G_{m2} and G_{m3} can be conveniently expressed applying the composite derivative method [18]:

$$g_{\mathrm{mk}} \triangleq \frac{G_{\mathrm{mk}}}{G_{\mathrm{spec}}/\left(n^k U_{\mathrm{T}}^{k-1}\right)} = \frac{\partial^k i_{\mathrm{d,sat}}}{\partial v_{\mathrm{g}}^k} = \frac{\partial^k i_{\mathrm{d,sat}}}{\partial q_{\mathrm{s}}^k}\left(\frac{\partial^k v_{\mathrm{g}}}{\partial q_{\mathrm{s}}^k}\right)^{-1}. \tag{2.34}$$

Then, the calculation of the derivatives in (2.34) is straightforward starting from (2.1) and (2.11), leading to the normalized expression of G_{m1}, G_{m2} and G_{m3} as a function of q_{s}:

$$g_{\mathrm{m1}}(q_{\mathrm{s}}) = \frac{a-1}{\sqrt{4+4\lambda_{\mathrm{c}}+a^2\lambda_{\mathrm{c}}^2}}, \tag{2.35}$$

$$g_{\mathrm{m2}}(q_{\mathrm{s}}) = \frac{g_{\mathrm{m1}}}{a}\frac{4+4\lambda_{\mathrm{c}}+a\lambda_{\mathrm{c}}^2}{4+4\lambda_{\mathrm{c}}+a^2\lambda_{\mathrm{c}}^2}, \tag{2.36}$$

$$g_{\mathrm{m3}}(q_{\mathrm{s}}) = \frac{g_{\mathrm{m1}}}{a^3}\frac{16+32\lambda_{\mathrm{c}}+8b\lambda_{\mathrm{c}}^2+8a^2c\lambda_{\mathrm{c}}^3+a^3d\lambda_{\mathrm{c}}^4}{(4+4\lambda_{\mathrm{c}}+a^2\lambda_{\mathrm{c}}^2)^2}, \tag{2.37}$$

where

$$a = 1+2q_{\mathrm{s}}, \tag{2.38}$$

$$b = (1-2q_{\mathrm{s}})(3+7q_{\mathrm{s}}+6q_{\mathrm{s}}^2), \tag{2.39}$$

$$c = 1-3q_{\mathrm{s}}, \tag{2.40}$$

$$d = 1-4q_{\mathrm{s}}, \tag{2.41}$$

and $G_{\mathrm{spec}} = I_{\mathrm{spec}}/U_{\mathrm{T}}$ is the specific transconductance.

Finally, the normalized transconductances can be expressed as a function of *IC* inverting

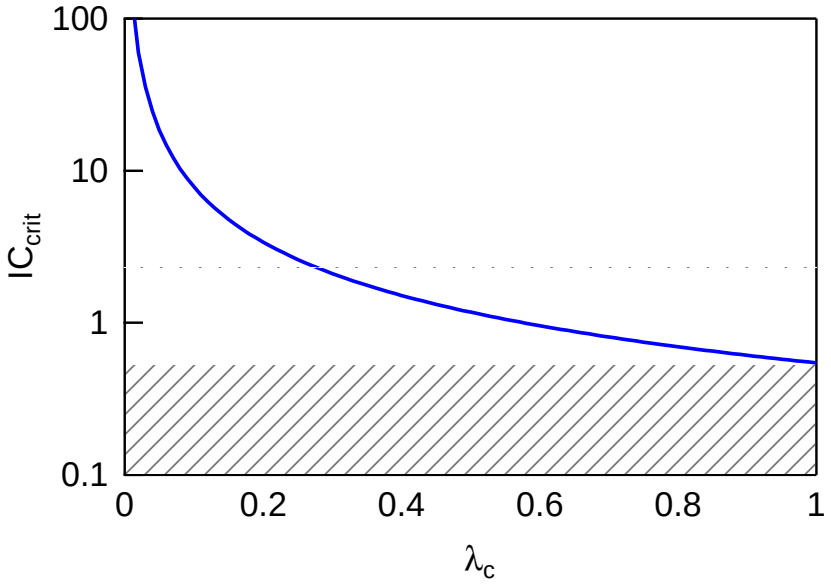


Figure 2.13: Position of the singularity in G_{m3} (IC_{crit}) as a function of the saturation of the channel (λ_c).

(2.11) and replacing $q_s(IC)$ in (2.35)-(2.37) with

$$q_s(IC) = \frac{\sqrt{(1+\lambda_c IC)^2 + 4IC} - 1}{2}. \tag{2.42}$$

After the de-normalization of $g_{m1}(IC)$, $g_{m2}(IC)$ and $g_{m3}(IC)$, all the parameters shown above can be plotted as a function of IC as well. Fig. 2.12 shows the harmonics amplitude of the output current normalized to I_{spec}, α and β respectively, resulting from the one-tone and the two-tone analyses. a, a_1 and a_2 are the input voltage amplitudes for the two analyses normalized to U_T. Note that (2.35)-(2.37) are consistent with the results in [28]: the latter can be simply obtained by setting $\lambda_c = 0$ in the former, which is equivalent to impose the long-channel case.

Moreover, the simplified EKV model is capable to reproduce precisely the well-known singularity in α_3, β_3 and β_{IM3}. This behavior is due to the fact that G_{m3} changes sign going from WI to SI and so there is a value of IC for which it is equal to 0, namely IC_{crit}. Note that the value of IC_{crit} depends uniquely on λ_c: since this parameter is by definition always between 0 and 1, it is easy to show that tends asymptotically to infinity (SI) for long-channel devices, while it gets to MI when λ_c increases. In Fig. 2.13 the position of IC_{crit} is plotted as a function of λ_c. It is evident that the singularity cannot occur in WI: for $\lambda_c = 1$, $IC_{crit} = 0.55$. The relevance of L_{sat} on IC_{crit} proves that the inclusion of VS is indispensable to describe well the behavior of a minimum-length MOSFET. Moreover, Fig. 2.13 shows that for short-channel devices MI offers a good trade-off for linearity in addition to area and current consumption [3].

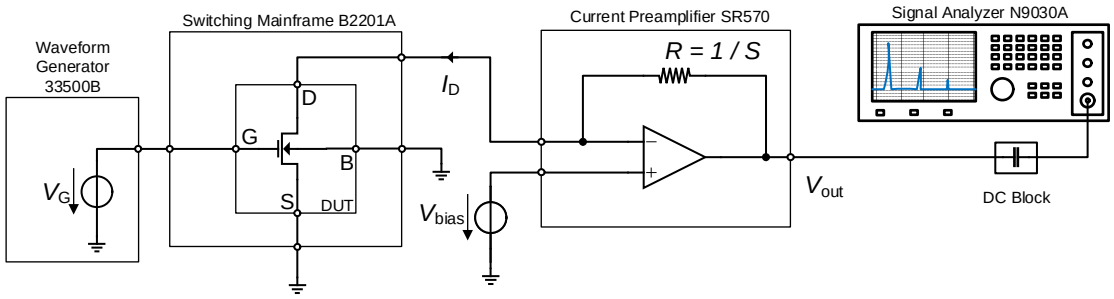


Figure 2.14: Experimental setup for ac measurements.

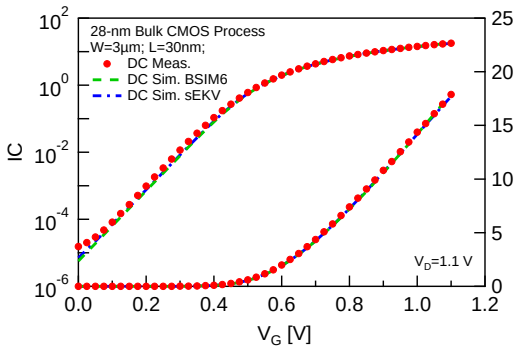


Figure 2.15: Comparison among simulated and measured I_D-V_G, in linear scale (left axis) and logarithmic scale (right axis).

Parameter	Value
$I_{spec\square}$	1.07 µA
n	1.6
V_{T0}	490 mV
L_{sat}	14.5 nm

Table 2.2: Simplified EKV extracted parameters for the 28-nm bulk CMOS technology

2.3.2 Validation of Distortion Analysis

Simulation with Verilog-A and BSIM6 model

The simplified EKV model is coded in Verilog-A to make it available for designers in simulation environments (Appendix B). Moreover, such simplified model is compared with a full compact model, i.e. BSIM6, to show the validity of the proposed approach. The simplified EKV Verilog-A code takes the terminal voltages as inputs, together with the four technology parameters ($I_{spec\square}$, n, V_{T0} and L_{sat}), the drawn dimensions W and L, the shrink factor of the technology and the thermal voltage U_T; it provides the drain current as output. Since (2.1) cannot be inverted analytically, q_s and q_d are computed with a non-recursive function which inverts it numerically achieving very good accuracy in spite of its simplicity. The same function is used in BSIM6 to calculate the inversion charge. Depending on the value of q_d, either (2.2) or (2.11) is chosen and then de-normalized with I_{spec} to provide the output current. Note that internally the model works with all normalized quantities. The input voltages are normalized to U_T before being used. As mentioned above, isolating all the technology dependence in four parameters makes the model easily portable from one technology node to another.

In order to extract the value of the technology parameters for simplified EKV model and the

dc model card for BSIM6, the static $I_D(V_G)$ characteristic of the device under test (DUT) is measured. The details about the measurements are reported in Section 2.3.2. The dc model card for BSIM6 consists of a subset of all the BSIM6 parameters which allows to describe faithfully only the dc behavior of the device. Since the claim of this work is that the first-, second- and third-order gate transconductances are sufficient to describe the harmonic distortion behavior, this kind of model card is supposed to be accurate enough. Both models are fitted to the measured dc drain current (both in linear and logarithmic scale) and to the first-, second- and third-order numerical derivatives (i.e. the three transconductances) by means of an optimization routine in Keysight IC-CAP. In the case of BSIM6, the fitting procedure follows the instructions in [31], while for simplified EKV it follows [2]. Concerning the bias conditions, the latter is fitted only to the curve at $V_D = 1.1\,V$, while the former is fitted for several values of V_D, from linear to saturation region. Table 2.2 shows the four parameters of the simplified EKV obtained by the fitting. While BSIM6 is a scalable model and it uses a unique set of parameters, simplified EKV is not: n changes with L and $I_{spec_\square}$ also through n, and consequently they need to be extracted for each length used in the design. Nevertheless, in a consistent extraction, $I_{spec_\square}/n$ should be kept constant, as well as L_{sat}.

The two models are used to carry out simulations in Keysight ADS. First, dc simulations are carried out to extract the $I_D(V_G)$ characteristic of the device, both in linear and logarithmic scale. Then, the first-, second- and third-order gate transconductances are obtained by derivating numerically $I_D(V_G)$. Finally, the first, second and third harmonics of I_D are extracted from harmonic balance (HB) simulations. The simulated test-bench is built in such a way to mimic as much as possible the experimental setup described in Section 2.3.2: the transimpedance amplifier (TIA) is replaced by an ideal operation amplifier with a feedback resistor equal to the inverse of the TIA sensitivity and a constant voltage $V_{bias} = 1.1\,V$ on the positive terminal to set V_D on the other one.

Experimental results

The analysis presented so far is validated by means of measurements on TSMC 28-nm bulk CMOS samples. The DUT is an NMOS with $L = 30\,nm$ and $W = 3\,\mu m$. The effective dimensions are $L = 27\,nm$ and $W = 2.7\,\mu m$ due to the 0.9 shrinking factor of the technology. The device has a single finger and it is wide enough to minimize the contribution of the drain access resistance. The nominal maximum voltage which can be applied to the terminals of the devices in such technology is 1 V. Nevertheless, a margin of 10% is allowed and consequently for these measurements V_{DD} is set to 1.1 V in order to explore SI as much as possible.

Regarding the dc measurements, the chip is tested with a probe-card connected to the Keysight B2201A Switching Mainframe. The four terminals of the device are controlled by the Keysight Semiconductor Analyzer, which generates the bias voltages and measures the current through them. V_G is swept from 0 to 1.1 V by 25 mV steps and this measurement is repeated sweeping V_D from 0 V to 1.1 V by 100 mV steps. Regarding the large-signal ac measurements, the objective is to measure the amplitude of the first, second and third harmonic of the drain current I_D.

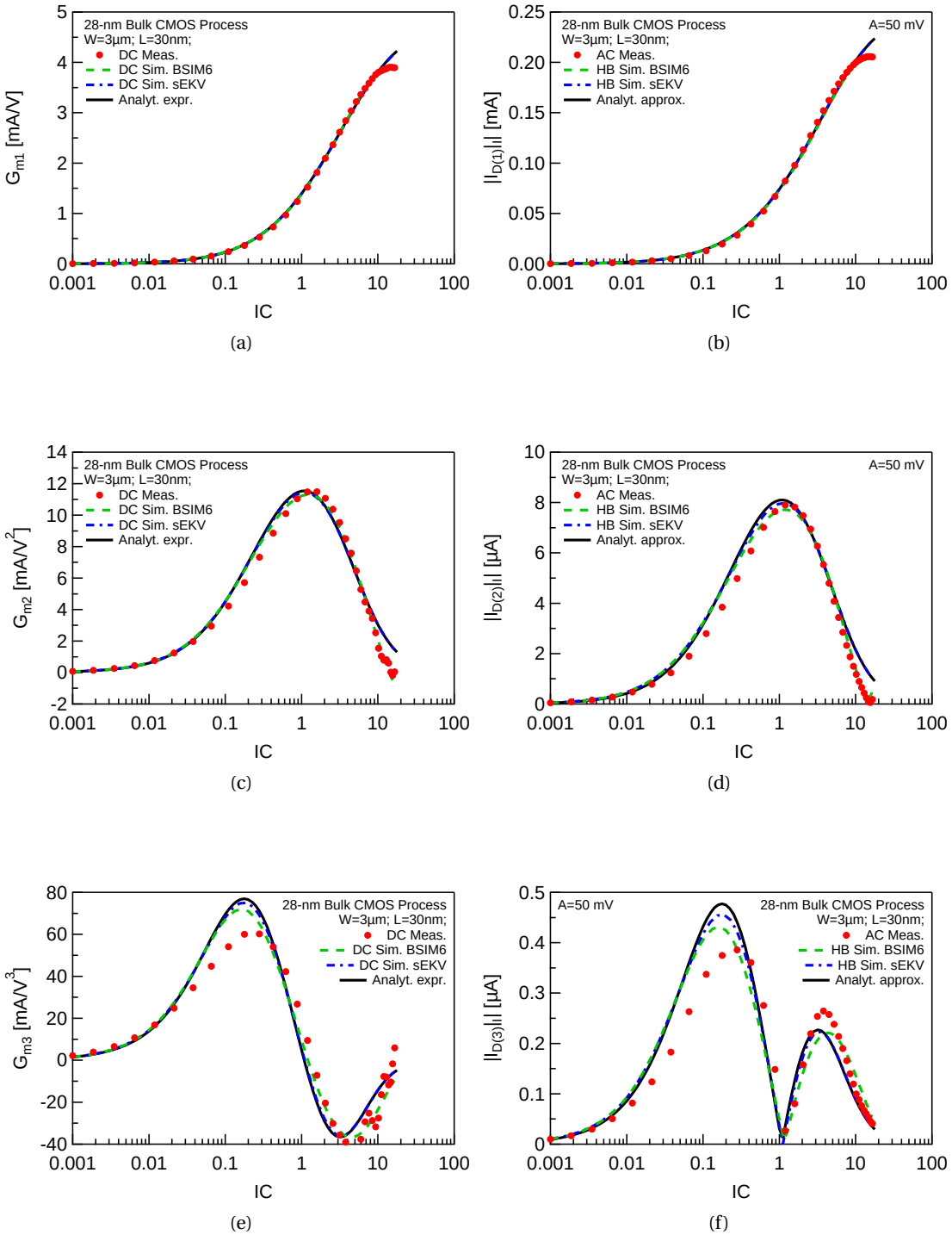


Figure 2.16: Comparison among the dc measured, the dc simulated and the analytical (a) G_{m1}, (c) G_{m2} and (e) G_{m3}. Comparison among the ac measured, the HB simulated and the analytically approximated (b) $|I_{D(1)}|_I|$, (d) $|I_{D(2)}|_I|$ and (f) $|I_{D(3)}|_I|$.

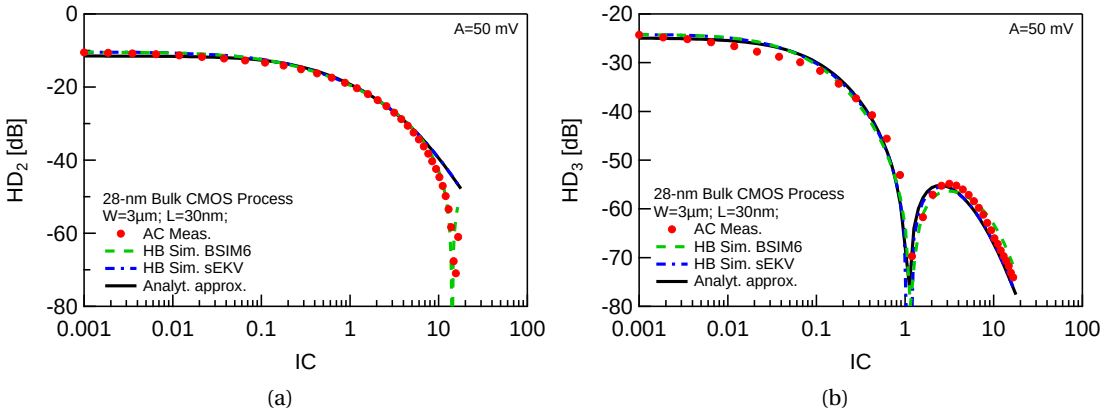


Figure 2.17: Comparison among the ac measured, the HB simulated and the analytically approximated (a) HD_2 and (b) HD_3.

Nevertheless, it is way more practical to measure the spectrum of a voltage rather than a current. For this reason, I_D is converted to a voltage by means of a TIA.

Fig. 2.14 shows the experimental setup for the large-signal ac measurements. The chip is still accessed through the Switching Mainframe and the probe-card. The sinusoidal input signal as well as the dc component is generated with the Keysight 33500B Waveform Generator and connected to the gate probe. Source and bulk probes are connected to ground and the N-well probe for the ESD diodes is biased to supply voltage $V_{DD} = 1.1\,V$, both generated by the Keysight E2646A Power Supply. The drain probe is connected to the negative input of the Stanford SR570 Low-Noise Current Preamplifier, used as TIA. In order to bias this node to the proper voltage, the positive input of the TIA is connected to V_{DD} and the negative feedback is exploited to fix the other input. The sensitivity is set to $500\,\mu A\,V^{-1}$. In the end, the output of the TIA is connected to the Keysight N9030A PXA Signal Analyzer. A dc block capacitor is placed before the PXA to allow the use of the dc-coupled mode. In order to explore all the operation regions, from WI to SI, the dc component of the input signal V_{G0} is swept from 0.1 V to 1.1 V by 25 mV steps. Moreover, the amplitude of the sinusoid is set to 50 mV for both the one-tone and the two-tone analysis. The frequency of the one-tone signal is set to 6 kHz. Instead, the two tones are generated from one tone at 5.5 kHz amplitude modulated by another tone at 500 Hz, resulting in two tones at 5 and 6 kHz. The amplitude of the modulated signal is set to twice the target amplitude for the subcarriers being the modulation coefficient equal to 0.5.

Comparison among analytical model, simulation and experimental results

The results obtained from the simulations and the measurements are processed and compared to the analytical expressions. The latter are based on the normalized transconductances shown in (2.35)-(2.37), which are calculated using the four parameters of the simplified EKV model (Table 2.2) and denormalized following (2.34). Fig. 2.15 shows the comparison among the

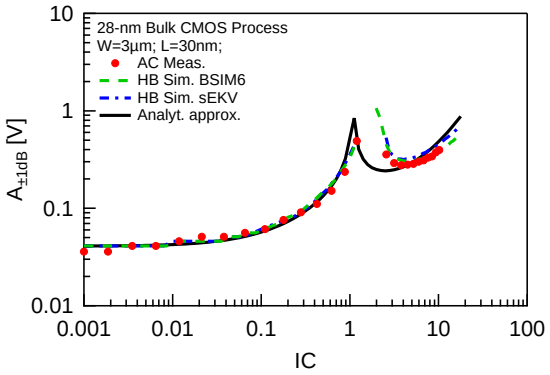
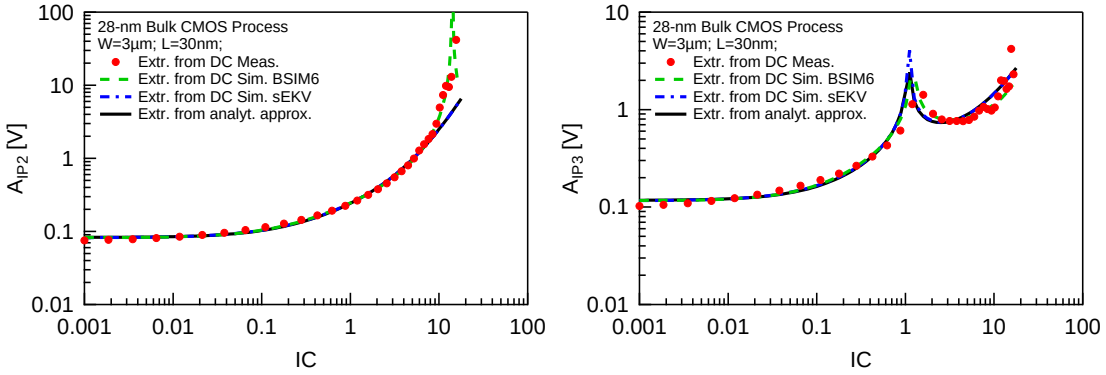


Figure 2.18: Comparison among the ac measured, the HB simulated and the analytically approximated $A_{\pm 1\mathrm{dB}}$.



(a) (b)

Figure 2.19: Comparison among extrapolated (a) A_{IP2} and (b) A_{IP3} from dc measurements, dc simulations and analytical expressions.

simulated $I_{\mathrm{D}}(V_{\mathrm{G}})$ curve with simplified EKV and BSIM6 and the measurements, in both linear and logarithmic scale. The match among the three curves is very good from WI to SI in both scales. The analytical expression (2.11) is not plotted because equal to the core equation of the simplified EKV Verilog-A model. It is evident the difficulty in biasing the transistor in SI, as pointed out in the introduction. Indeed, the highest IC achievable in lower than 20 at V_{G} and V_{D} equal to 1.1 V, which is beyond the nominal V_{DD}.

The analytical expressions of G_{m1}, G_{m2} and G_{m3} (2.35)-(2.37) are compared to the numerical derivation of the simulated I_{D} using the simplified EKV and the BSIM6 models and those obtained derivating the measured I_{D} in Fig. 2.16. The match between the curves is very good: this proves that the simplified EKV model is accurate in describing the dc behavior of the MOSFET. It can be noticed that the measured and the BSIM6 G_{m2} change sign for IC close to 20: it is due to mobility reduction caused by the vertical electric field. Indeed, the simplified EKV G_{m2} remains positive because it does not include such effect. The analytical approximation of

the amplitudes of the three drain current harmonics, namely $I_{D(1)}|_I$, $I_{D(2)}|_I$ and $|I_{D(3)}|_I|$ (2.26)-(2.28), are compared to those obtained by a one-tone HB simulation using the two models and those measured on the DUT with a one-tone test in Fig. 2.16. The 4 curves clearly match from WI to SI. The meaning of this result is twofold: it confirms that the simplified EKV Verilog-A model is compatible with a HB simulation regarding the nonlinear behavior of the device, and it also supports the claim that the dc model is sufficient to describe such behavior precisely. It is noted again that these results are valid in the assumption of low-frequency operation. The analytical approximation of HD_2 and HD_3 obtained from (2.29)-(2.30) are compared to simulations and measurements in Fig. 2.17; the latter are calculated from the drain current harmonics (Fig. 2.16) using the definition of HD_2 and HD_3. The match among the curves is very good for both parameters. This result follows exactly what stated above regarding Fig. 2.16. Moreover, the singularity is effectively caught and it is located in the middle of the MI region. This confirms once more that this bias region is very convenient for several trade-offs [3, 32]. Nevertheless, in practice it is quite difficult to exploit such singularity, due to process and temperature variations. Still, even if the third-order distortion is not fully canceled, *IC* values around this point represent an interesting trade-off [27, 33]. Another singularity appears in HD_2 with BSIM6: it comes from the change of sign of G_{m2}, which has been already discussed above.

Fig. 2.18 and Fig. 2.19 report three rf design metrics, namely $A_{\pm 1dB}$, A_{IP2} and A_{IP3}, as a function of *IC*. The goal is to prove that the proposed model is a powerful tool to gain insight in the device and circuit performance during the design process. The analytical approximation of $A_{\pm 1dB}$ is compared to simulations and measurements in Fig. 2.18. For the latter, the amplitude of the fundamental is measured and simulated increasing the signal amplitude until reaching the 1 dB deviation with respect to the ideal linear extrapolation. In the measurements of $A_{\pm 1dB}$, the signal amplitude superimposed to the bias voltage is limited to 30% above V_{DD} to avoid deteriorating the device. There are not hence values beyond 0.5 V but still the trend is very clear. The presence of a low impedance at the drain of the device allows to measure $A_{\pm 1dB}$ without the occurrence of voltage clipping. Fig. 2.18 shows a good match up to the peak; however, the simple analytical approximation slightly underestimate IC_{crit}. This is due to the fact that (2.31) does not account for higher order harmonics above the third, which become important particularly at this critical point where amplitude grows significantly. Since G_{m3} changes sign, in the same plot there are both A_{+1dB} and A_{-1dB}. For *IC* values smaller than the sweet spot IC_{crit}, G_{m3} is positive and therefore the device shows expansive behavior (A_{+1dB}), while for *IC* values greater than IC_{crit}, G_{m3} becomes negative and the device has compressive behavior (A_{-1dB}). A_{IP2} and A_{IP3} are instead extrapolated from (2.32)-(2.33) using the gate transconductances obtained from the analytical expressions, dc simulations and dc measurements. The match is once more very good, especially in WI and MI. A_{IP2} presents a singularity similarly to HD_2 due to mobility degradation which is well-predicted only by BSIM6, while for A_{IP3} all the curves describe accurately the peak in MI.

The outcome of this comparison proves that it is possible both to estimate the amplitude of the current harmonics by means of a dc simulation by computing the three gate transcon-

ductances from the dc drain current and also to extract a small-signal parameters from a HB simulation. Moreover, there is a direct relation between the *IC* and the most relevant rf design metrics for linearity through the analytical expressions for G_{m1}, G_{m2}, G_{m3} and q_s (2.35)-(2.42).

2.4 Design Methodology for Layout in Nanoscale Technologies

The simplified EKV model is the foundation of the design methodology for low-power analog and rf circuits even in nanoscale technologies. The model of the drain current leads to simple expressions for the key small-signal quantities like the gate transconductance, the output conductance and the self gain. Starting from these parameters, an insight in the optimization of the circuits is provided by the calculation of FoMs like the transconductance efficiency, the 1-dB compression point, the second- and third-order intermodulation products versus *IC*. One missing fundamental piece for establishing an effective design methodology regards the best techniques for the layout of rf and mm-wave circuits and the appropriate approach to model and extract passive devices and parasitic components. Schematic and layout co-design is a necessity with the most advanced technologies: on one side the DRC rules are so specific and constraining that going to layout as soon as possible can show how to adapt the schematic accordingly and it saves a huge amount of time. On the other, even with a clean layout there is not the guarantee that the device matching and the parasitic contributions are satisfactory without applying a clear methodology.

One of the toughest layout limitations coming from the design rule checking (DRC) in advanced nodes is the fulfillment of the density of metals, polysilicon and diffusion regions. This is important mainly for analog blocks, which use long and wide transistors, often to be matched in differential pairs or current mirrors. Instead of designing a long series of fingers belonging to one or more transistors sharing the same diffusion region, it is better to design a unit containing only a couple of fingers with their own diffusion region and then create a matrix of such units with the desired matching scheme. Moreover, every unit can be designed to respect the densities adding dummy polysilicon and metal lines. The latter can be either used as interconnection among fingers or remain floating. The byproduct is that there is no need to run a script for the automatic generation of filling structures. Metal lines can even be drawn above the gate of transistors since every unit is affected in the same way. A unit can be used also as a dummy at both ends of rows and columns in the matrix. This approach grants matching thanks to the repetition of the same structure, helps to mitigate the layout-dependent effects (LDEs), which have become more severe with scaling, and reduce the discrepancy of post-layout simulations with schematic ones. Instead, in rf and mm-wave circuits transistors have minimum length and their occupied area is much smaller. For this reason, the core devices are more compact and can be designed as a single diffusion region, while filling structures can be safely placed further away from the active regions and the metal interconnections to avoid increasing the parasitic capacitance. However, if device matching is important, the entire device should be replicated and such dummy cells placed all around the core transistors. In fact, adding just a few dummy gates on both sides is not enough any more,

since the effect of the LDEs can extend up to few tens of micrometers.

As a general rule, the layout of analog and rf circuits requires a validation by means of an extraction of parasitic capacitors and resistors in the metal interconnections. Indeed, in the case of analog circuits, the parasitic capacitance contributes with additional poles in given nodes while the parasitic resistors on the dc current paths lead to asymmetries and hence to mismatch. Instead, for rf circuits such parasitics may lead to lower efficiency in power amplifiers, to lower resonator quality factor and shifted frequency tuning range in oscillators and in general to higher load on critical nodes. In all the mentioned cases the increase of power consumption is required to overcome the performance loss and respect the specifications with a margin. This situation is particularly critical in the design of low-power radios, where the minimization of the current consumption is the priority. A first estimation of the effect of parasitic components can be studied in schematic adding them manually and trying different values which represent from the best to the worst case. Then, it is important to go quickly to the layout to prepare the unit cell that will compose the designed devices. A parasitic extraction of the single transistors with their vias and routings on gate, source and drain is crucial. It allows to replace the bare transistor model with a first-order model including the actual LDEs and preliminary parasitic components.

The situation is even more critical when one moves to mm-wave frequencies. In such circuits, the tolerated parasitic capacitance on the signal path is very limited and it must be mastered precisely to avoid a blunder. Moreover, the parasitic inductance of thick and ultra-thick metal lines starts to play a role as well. Such metal layers are introduced to allow inductors with a high quality factor. For example, as long as the frequency does not exceed 10 GHz, most of the inductance in a resonator is contributed by the functional component. Nevertheless, when the designed inductor is only about 100 to 200 pH, even a relatively short top metal line can contribute 10 to 20 % of it with its own parasitic inductance. At this point inductors cannot be simply connected to the core transistors carelessly but such lines need to be well conceived and modeled. The same is valid for interstage connections: critical blocks should be co-designed and co-layed out to optimize the transition. As a general rule, such metal lines should be minimized and the best way to model their impact is to use an electromagnetic (EM) simulator, which is a software meant to calculate the S-parameters of a structure with a given number of ports. Several software are available on the marker: for this thesis, Keysight Momentum and Ansys RaptorX have been used. The difficulty consists in selecting only the relevant metal layers in a given net, which usually correspond to the thick and ultra-thick ones. Such lines have to be isolated and extracted with the right simulation parameters. A port should be placed everywhere the connection descends to lower metals to reach a group of devices, which is then extracted separately with a tool for parasitics. The use of several ports allows to describe correctly the signal distribution and the effect of the multiple loads. The next step is the EM simulation of all the inductors and the critical nets in a design. The outcome is a black box with a very large number of ports represented by an S-parameter file which can be used in simulation. In this thesis this approach is applied to the design of oscillators at mm-wave frequencies: the result is the correct estimation of both the oscillation

frequency and the quality factor of the inductor.

2.5 Summary

This chapter describes some fundamental pieces that constitute a design methodology for low-power analog and rf circuit design. It starts with a brief comparison between bulk and FDSOI technologies and explains the reasons for opting for GF 22FDX technology for developing a radar SoC. Then, the charge-based simplified EKV model is presented. It allows to describe the behavior of long- and short-channel transistors in advanced bulk and FDSOI CMOS technologies using only a few extracted parameters. By means of the inversion coefficient it is possible to explore all bias regions of a MOSFET from weak inversion to strong inversion. All small-signal quantities and FoMs which are relevant for analog and rf design can be expressed as functions of *IC*, helping to identify the optimum size and bias point of devices in a circuit. The output conductance is a crucial parameter for design and it is very hard to model properly, especially in nanoscale devices. One step in this direction is provided with a simple expression of the normalized output conductance versus *IC* for short-channel dominated by DIBL. It is validated with experimental results from 28-nm bulk and 22-nm FDSOI CMOS technologies.

The analysis of the MOSFET linearity has been the missing piece in the EKV framework for a long time. The drain current non-linearity is expressed with a Taylor expansion up to the third order and the simplified EKV model enables the derivation of analytical expressions for the first-, second- and third-order gate transconductances including the effect of VS. This feature allows to describe the behavior of nanoscale technologies while keeping the model simple. All the metrics for one- and two-tone analyses are derived as a function of *IC*. Indeed, a dc model is demonstrated to be sufficient for the analysis at low-frequency operation, since all the metrics depend only on G_{m1}, G_{m2} and G_{m3}. In detail, the evident "sweet spot" in HD_3, A_{IP3} and A_{1dB} is caused by the sign change of G_{m3}, which is effectively captured only when VS is included. Such singularity is located at a specific *IC* value, defined as IC_{crit}, whose value depends only on λ_{c}. The model is implemented in Verilog-A and compared with the analytical expressions, a dc BSIM6 model and with measurements carried out on a 28-nm Bulk CMOS technology. The match between the three cases is very good from WI to SI for all metrics. For this technology IC_{crit} is close to 1, confirming the MI region as an interesting operating point in terms of trade-offs.

Finally, the layout techniques for advanced nodes are included in the methodology together with the modeling with EM simulators of passive devices and critical signal routings at mm-wave frequencies. This aspect is often overlooked but extremely important for effective designs which achieve the target specifications without lengthy and expensive respins.

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3 Analysis of Low-Power and Low-Noise LC Oscillators

As seen in Chapter 1, in the framework of IoT, all portable devices will become the center of a network made of sensors and beacons spread in every other object which will allow to receive information or to control them remotely. In order to achieve this, it will be necessary to produce very power-efficient nodes, ideally able to work for years out of a coin battery cell or even smaller. In order to be able to communicate with the outside world, they will need ultra-low-power radios and specifically ultra low-power frequency synthesizers.

The typical architecture of transceivers used in radios relies on frequency synthesizers for generating accurate and low-noise carriers, which are used to up- and down-convert the base-band signal carrying data. Oscillators are one of the key building blocks of frequency synthesizers and they are usually classified in two families: harmonic (e.g.. LC-based) and relaxation oscillators (e.g. ring-based). The former category includes the oscillators which are more suited for the aforementioned purpose, since they embed an LC tank to select the target frequency. As a consequence, the output is an almost perfect sinusoidal signal and its phase noise performance is pretty good, compared to the more noisy square wave produced by a ring-oscillator. However, the better output signal quality comes at the price of a larger power consumption and usually a larger area.

In the context of PLLs for low-power applications, it is of paramount importance to analyze the oscillator from the efficiency point of view since it is the circuit that contributes the most to the overall power consumption: this analysis is presented in [1]. Moreover, since the phase noise is not the primary design constraint in low-power applications, the operation point is chosen to minimize the power consumption rather than maximize the figure of merit. As a consequence, all the noise sources in the oscillator have to be properly identified and analyzed in order to optimize as much as possible the phase noise accounting for the limited power budget: this analysis is presented in [2].

3.1 Desciption of the LC Oscillator Topologies

During the last ten years, new LC-based topologies are reported in the literature, where an increased voltage and/or current efficiency is achieved introducing modifications on top of the basic differential topology. The simple cross-coupled-based structure has evolved employing transistors with different conduction angle or bias region. As a consequence, due to the similarities with some power amplifiers, the members of the family of harmonic oscillators are categorized in similar classes.

This section focuses on the analysis of the basic version of three topologies, i.e. class-B, class-C, and class-D (Fig. 3.1), since they are representative enough for understanding their pros and cons in terms of power consumption and phase noise, aiming at investigating the trade-offs and providing the best choice for IoT applications.

3.1.1 The Class-B Cross-Coupled Oscillator

Fig. 3.1a shows a class-B oscillator with an NMOS cross-coupled pair only, one of the best-known and widely employed topologies [3]. When the single-ended oscillation amplitude is lower than the supply voltage V_{DD} (theoretical limit), the oscillator operates in the so-called "current limited" regime [4]. In this condition, the output differential voltage amplitude A_{diff} is set by the nonlinear characteristic of the active transistors, namely when the transconductance of the fundamental component $G_{m(1)}$ matches G_{mcrit}, defined as the cross-coupled transistor's G_m for obtaining a zero amplitude oscillation [5]. Indeed, the fundamental component of the current is the only one not filtered out by the LC tank.

The bias current is steered from one branch to the other once per period, when the respective transistors are active: the larger the amplitude, the harder the current is steered. Since each transistor is active for approximately half a period, which means a conduction angle of 180°, this topology is called class-B. When the amplitude reaches V_{DD}, it remains almost constant even if the bias current is increased further, making the oscillator working in the so-called "voltage limited" regime [4]. Several variations are studied for this topology, in order to improve the power consumption and the phase noise performance [6, 7].

3.1.2 From the Class-B to the Class-C Cross-Coupled Oscillator

Fig. 3.1b shows a class-C oscillator with an NMOS cross-coupled pair only. It is pretty similar to a class-B, but it contains two essential modifications. First of all, a large capacitor C_{tail} is connected to the source of the cross-coupled pair in parallel to the bias transistor. Secondly, the cross-coupled transistors' gates are not anymore biased at V_{DD} but at a lower voltage, through a RC net (R_{bias} and C_{bias}) which enables AC coupling of the output signal. The role of C_{tail} is to allow a more efficient generation of the current first harmonic, so that a higher oscillation amplitude can be obtained out of the same bias current [8]. Indeed, it prevents

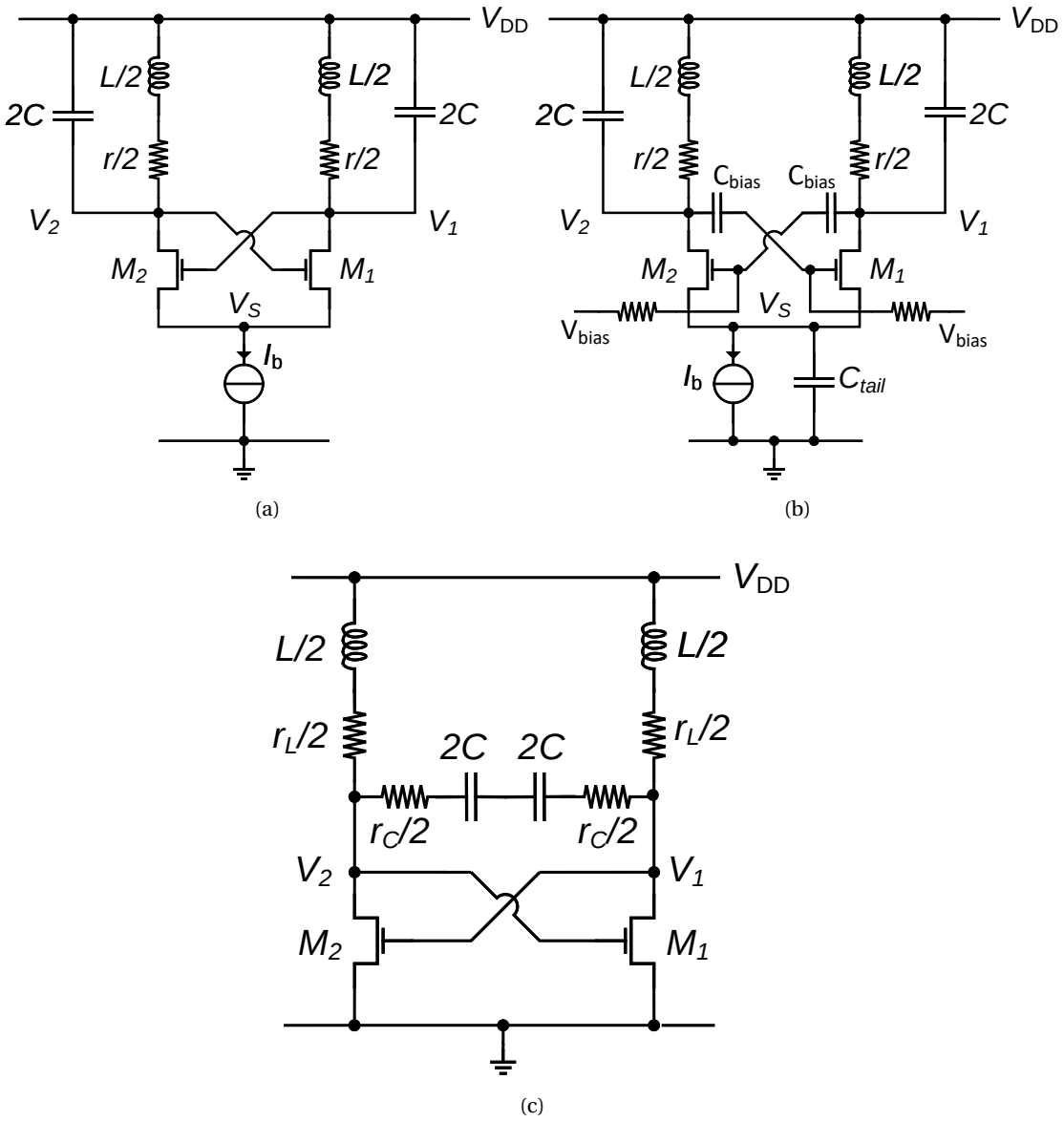

Figure 3.1: Three topologies of LC oscillators: a) class-B, b) class-C, and c) class-D oscillators.

the source node from swinging, providing sharp current spikes at the peak of voltage swing [9]. The current waveform does not look like a square wave anymore but it shows narrow and high pulses, since the active transistor conducts for less than half a period (conduction angle < 180°). This behavior gives the name to the topology. Moreover, it filters out noise at the second harmonic coming from the bias transistor, preventing it from contributing to phase noise after down-conversion around the fundamental.

C_{tail} alone is not enough for the oscillator to benefit from working in class-C. As it can be observed also in class-B, when the oscillation amplitude exceeds a given limit, the active tran-

sistor goes from saturation to triode region for a fraction of the semi-period. As a consequence, it loads the tank due to any capacitance at the source, increasing the phase noise. In class-C this effect is even worse, because it either vanishes the benefits coming from class-C operation or it affects the phase noise even more. In order to prevent it, the active transistor must not leave the saturation region or, at least, must not go in deep triode region. This is obtained by lowering its overdrive voltage, biasing the gate below V_{DD} and accepting a reduction of the maximum achievable differential oscillation amplitude A_{diff}, which depends on the chosen bias voltage. Unfortunately, the implementation of class-C oscillators suffers from a trade-off between start-up robustness and maximum oscillation amplitude in steady-state condition [3].

3.1.3 The Class-D Cross-Coupled Oscillator

Fig. 3.1c shows a class-D oscillator, whose behavior is quite different from the previous two topologies, since it is even more nonlinear. Indeed, the bias transistor is removed forcing the oscillator to work in the "voltage controlled" regime instead of the "current controlled". The oscillation amplitude is set by V_{DD} and it is allowed to peak well above the supply voltage boosting the voltage efficiency (A_{diff}/V_{DD}), while the current consumption depends either on V_{DD} or on the tank losses [10]. Moreover, the differential transistors do not work anymore as transconductors but as switches: when active they are in triode region, since their gate voltage is close to V_{DD} and the drain voltage falls to ground. Due to this behavior the oscillator is classified as class-D.

As a whole, the circuit is very simple and it can benefit a lot from device scaling due to improved switching performance. Since the output nodes are ideally shorted to ground during half of the oscillation period, the inductor and the capacitance are not in parallel for the same amount of time. For this reason, the tank has a time-variant nature, differently from the two previous topologies, and the oscillation frequency cannot be predicted by the standard tanks formula. Moreover, the oscillation frequency is different whether the capacitance is differential or single-ended. Finally, the equivalent parallel resistance approximation is not valid anymore, so the losses of the capacitor and of the inductor (r_C and r_L) have to be separately taken into account.

3.2 Analysis of Power Consumption in LC Cross-Coupled Oscillators

3.2.1 Simulation-based Analysis

In order to address the requirements imposed by IoT applications, especially in terms of power budget, the *IC* is used as the driving parameter for the forthcoming analysis. This is mainly due to the capability to investigate the performance of CMOS transistors in all the regions of operation, to be identified through the value of *IC* itself. Table 3.1 shows the parameters which is kept constant throughout the analysis in order to get a fair comparison

L (nm)	$I_{spec_\square}$ (nA)	n	f_0 (GHz)	L_T (nH)	Q_L	r_L (Ω)	$C_{T,tot}$ (pF)
40	650	1.48	1	8	10	5	3.13

Table 3.1: Description of the simulation parameters for the analysis of power consumption

among the three topologies. A commercial 40-nm bulk CMOS technology is chosen, whose model card for BSIM6 model is extracted with Keysight IC-CAP starting from dc, cv, rf and rf noise measurement data [11]. Keysight ADS is used as simulator. A first set of parameters is defined as specifications, including the transistors channel length L, the process parameters n and $I_{spec_\square}$, the oscillator output frequency f_0, the inductor used in the tank L_T and its quality factor Q_L. From the previous values a second group of parameters is calculated, such as the inductor series resistance $r_L = 2\pi f_0 L_T Q_L$ and the total tank capacitance $C_{T,tot} = 1/\left[(2\pi f_0)^2 L_T \left(1 + 1/Q_L^2\right)\right]$. In order to keep the oscillator frequency precisely at 1 GHz, the value of $C_T = C_{T,tot} - C_{par}$ is tuned while sweeping the *IC* parameter to take into account the contribution of the parasitic capacitances of the differential transistors $C_{par} = (4C_{GD} + C_{GS} + C_{GB})/2$, which change depending on their width and bias region. For each *IC* value, the bias current I_b is set by simulation to achieve a target amplitude A_{diff} and the transistors width W is sized accordingly from $W = I_b L/(2IC I_{spec_\square})$.

Two sets of simulation are carried out: one having as a target a differential oscillation amplitude A_{diff} of 300 mV and another with 1 V. For the class-C oscillator, the simulation is done with two values of C_{tail}: 2 pF and 6 pF, which are both within the limit to avoid the phenomenon called "squegging" since C_T is around 3 pF [8]. Moreover, V_{bias} is set for each *IC* to the minimum value which would guarantee a sufficient voltage headroom to the current source. Fig. 3.2a and Fig. 3.2b show the bias current I_b and width of the differential transistors W needed for reaching the above-mentioned amplitudes respectively depending on *IC*.

3.2.2 Discussion about the Simulation Results

A general trend can be identified for both topologies at different A_{diff} values, i.e. an overall reduction of current when moving from SI to MI and WI at the cost of an exponential increase of the area (W). A reasonable trade-off is then experienced in MI, where *IC* is close to unity. In particular, for $A_{diff} = 300$ mV, as shown in Fig. 3.2a, I_b increases slightly between WI and MI, while it starts rising fast going from MI to SI. The class-C current consumption decreases with increasing C_{tail} as expected due to the improved efficiency; it shows around 20 % improvement with respect to class-B with $C_{tail} = 6$ pF in WI and MI, while in SI there is not appreciable difference.

Fig. 3.2b shows the results for $A_{diff} = 1$ V. The increase of I_b shows up only going in deep SI, and there is a minimum around MI for class-C. The lower increase of I_b in class-B is due to the fact that the relation between I_b and A_{diff}, which comes from the nonlinear behavior of

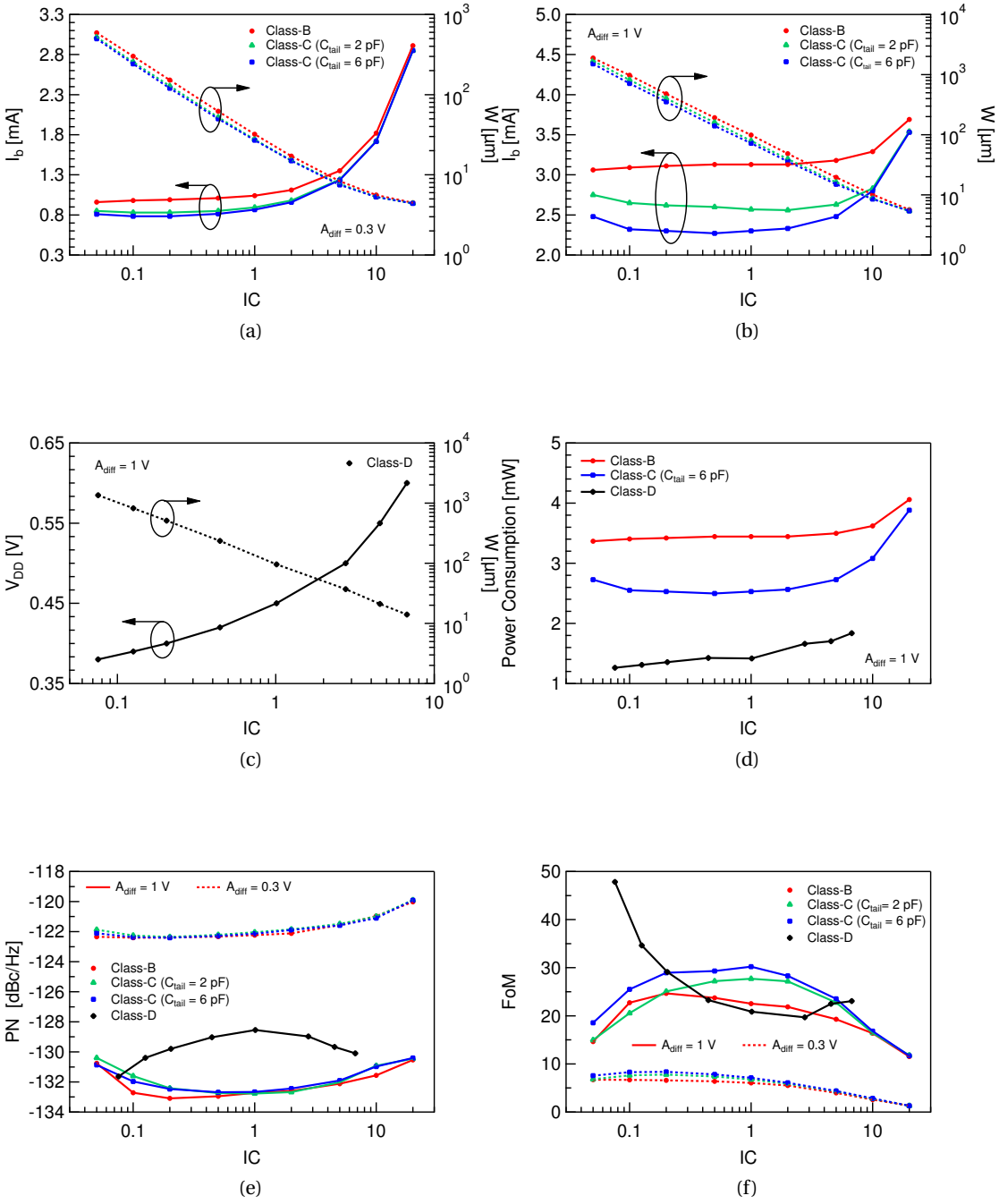

Figure 3.2: Comparison between LC oscillators vs. *IC*: (a) I_b and W for class-B and class-C at $A_{diff} = 300\,mV$; (b) I_b and W for class-B and class-C at $A_{diff} = 1\,V$; (c) V_{DD} and W for class-D at $A_{diff} = 1\,V$; (d) phase noise at 1 MHz offset for class-B, class-C and class-D; (e) FoM for class-B, class-C and class-D; (f) power consumption for class-B, class-C and class-D.

the oscillator, depends strongly on *IC* only at small A_{diff}, while it converges to the asymptotic value valid for WI for large A_{diff} [5]. The improvement in current consumption going from

class-B to class-C is more evident in this case for all *IC* values.

As far as the phase noise (PN) is concerned, its value at 1 MHz offset from the carrier frequency is reported in Fig. 3.2e in order to check how it varies across *IC* and topology. This work focuses on far-out phase noise: it is verified by simulation that the corner frequency f_{1/f^3} is lower than 1 MHz in all cases. Only a slight increase is noticed going from deep WI to deep SI, around 1.5−2 dB, and also between class-B and class-C. The difference between the $A_{\text{diff}} = 300\,\text{mV}$ and the 1 V cases, ∼ 10 dB, is due to the phase noise dependence on $1/A_{\text{diff}}^2$.

The standard FoM for oscillators is defined as [12]:

$$\text{FoM} = \frac{kT}{\mathscr{L}\left(\Delta f, IC\right) P_{\text{osc}}\left(IC\right)} \left(\frac{f_0}{\Delta f}\right)^2, \tag{3.1}$$

which includes the power consumption $P_{\text{osc}} = I_{\text{b}} V_{\text{DD}}$, the phase noise $\mathscr{L}$ and it is plotted in Fig. 3.2e. It shows that the FoM is maximum when biasing the differential transistors in WI for both topologies at small A_{diff}, while this remains valid at larger A_{diff} only for class-B, while class-C FoM has a peak around MI.

In order to carry out a fair comparison in terms of power consumption among the three oscillator topologies, some parameters have to be kept constant and particularly the differential oscillation amplitude A_{diff}. Moreover, also the *IC* has to be changed, setting it accordingly to the width of the differential transistors. In class-B and class-C the I_{b} is imposed with a current source, which allows to play with *IC* easily. On the other hand, in class-D A_{diff} is determined by V_{DD} but the expression of I_{b} for all regions of operation as a function of the terminal voltages is quite complex to handle. Nevertheless, a slight dependence of A_{diff} on W is noticed, since it changes the channel resistance when in triode region. This effect has allowed to find different combinations of V_{DD} and W which result in the target $A_{\text{diff}} = 1\,\text{V}$. It has not been possible to get $A_{\text{diff}} = 300\,\text{mV}$ as well, since it would have required a too small V_{DD} for the oscillation to start.

Notice that some of these points are shown only for the sake of comparison, even if they are not practical: W is quite small, which results in a large channel resistance, risking to vanish the benefits of class-D and to obtain long start-up time in a real circuit. A differential capacitance configuration is used, since it is shown that it provides better results in terms of frequency, power consumption and phase noise with respect to its single-ended counterpart [10]. Moreover, the inductor is assumed to have the lower quality factor and its losses to dominate over those of the capacitance.

Fig. 3.2c shows the values of V_{DD} and W chosen to get $A_{\text{diff}} = 1\,\text{V}$. As the power supply gets lower, the differential transistors have to be biased more and more in WI in order to meet the specification, becoming wider and wider. As a consequence, the dc component of the current varies only slightly with *IC*. This is coherent with the expression of the current consumption for this topology found in [10] since at the same time V_{DD} is decreased and the tank quality factor is affected negatively by the higher channel resistance, causing an increase of the overall

tank losses. Asymptotically, *IC* depends quadratically on V_{DD}, which is the gate voltage at DC, in SI. In fact, the dc current is kept almost constant (3.1-3.3 mA) by reducing W accordingly, and it depends exponentially on V_{DD} in WI. This trends can be identified in Fig. 3.2c.

As far as the phase noise of class-D is concerned, its value at 1 MHz offset from the carrier frequency is reported in Fig. 3.2e. Compared to class-B and class-C, class-D has a worse performance, due to the difficulty to guarantee the same losses for the tanks of the three topologies. Indeed, in the latter the differential transistors channel resistance loads directly the tank. In detail, the larger it is, the more severely the quality factor is affected. This effect is limited in WI where the W is very large, but it emerges toward MI. The reason for the phase noise to decrease again going in SI is that the increase of V_{DD} prevails on the decrease of Q_L and/or increase of noise factor, as shown in [10].

The FoM of class-D defined in (3.1) is plotted in Fig. 3.2f. This topology allows for a somewhat higher FoM in WI with respect to the others, but, due to the phase noise degradation, in MI and SI the class-D performs worse. Nevertheless, even if the FoM is an useful parameter to compare different designs, it does not imply that having a good value means that all the specifications are met singularly. So, the power consumption by itself is plotted in Fig. 3.2d. The progressive improvement going from class-B to class-C and class-D for all regions of functioning, especially for WI, is then obvious.

3.3 Linear Analysis of $1/f^2$ Phase Noise in the Class-B LC Cross-Coupled Oscillator

The careful optimization of phase noise in LC oscillators is critical with a limited power budget and in designs with deep-submicron nodes. Due to technology scaling, the impact of parasitic resistances has increased. Indeed, even if the metallic gate has become a process option for most recent technology nodes (e.g. 28-nm and 22-nm technologies), the gate resistance measured on these devices is significant compared to older nodes [13, 14]. Moreover, the gate leakage shot noise contribution has increased mainly due to the shrinking of the gate oxide thickness, although the inclusion of high-k dielectric materials in latest nodes should attenuate this effect.

In this section, a comprehensive analytical derivation of phase noise is carried out for a class-B LC oscillator. All noise sources are included and the transfer function of each of them to the output is calculated. The complete expressions come also in a simplified form, in order to provide an insight into possible strategies for noise optimization.

3.3.1 Phase Noise Analysis

LTI vs LTV phase noise analyses

Phase noise is the random phase quantity which perturbs the oscillation and shifts the output waveform zero-crossings with respect to the ideal values, corresponding to the integer multiples of the nominal period. It originates from the various noise sources in the circuit. In frequency domain, the phase noise manifests itself as a broadening of the output signal spectrum, ideally represented by a single tone at the nominal frequency. Oscillator phase noise has been studied for decades by means of several different methods and techniques. The main approaches are the linear time-invariant (LTI) [15, 16] and the linear time-variant (LTV) analyses [17]. The former consists in representing the circuit with its small-signal equivalent and transferring the contribution of each noise source to the output, which is then converted from voltage noise to phase noise. The latter takes into account the instant in which the noise is injected throughout the oscillation period. As a consequence, the impulse sensitivity function (ISF) is derived looking at the effect produced by such an injection. At the end, the output phase is computed by the convolution of each noise source with its own ISF. This method allows to include the contribution from noise sources at frequencies different from the oscillation frequency since they get up- or down-converted. Nevertheless, the improved accuracy comes at the price of increased complexity. For this reason, the first method still provides a reliable tool for a quicker and still reasonably accurate evaluation of an oscillator phase noise performance in the $1/f^2$ region.

Noise sources in MOSFETs

For this analysis, the two transistors M_1 and M_2 in Fig. 3.1a) are replaced by their quasi-static (QS) rf small-signal equivalent circuit in saturation with their noise sources, fully described in [13, 18, 19]. The complete rf model includes: the gate and the bulk resistances, R_G and R_B, the source/drain access resistances, R_S and R_D, the parasitic capacitances between gate and source, C_{GS}, gate and drain, C_{GD}, gate and bulk, C_{GB}, source and bulk, C_{BS}, drain and bulk, C_{DB}. All the capacitances include both extrinsic and intrinsic contributions. Nevertheless, when the operating frequency is in the gigahertz range, the extrinsic part of the capacitances dominates. The extrinsic components of C_{GS}, C_{GD} and C_{GB} consist of overlap and fringing capacitances, while those of C_{BS} and C_{DB} are junction capacitances. Finally, $I_{m1(2)} = G_m(\Delta V_{Gi1(2)} - \Delta V_{Bi1(2)})$ and $I_{ms1(2)} = -G_{ms}\Delta V_{Bi1(2)}$, where G_m is the gate transconductance, G_{ms} is the source transconductance and G_{ds} is the output conductance of the cross-coupled transistors. In saturation region, $G_{ms} = nG_m$ where n is the slope factor [19].

In Fig. 3.3 the studied noise current sources are reported. $I_{nD1(2)}$ represents the thermal noise generated in the transistor channel, while $I_{nRB1(2)}$ and $I_{nRG1(2)}$ model the parasitic resistances thermal noise. As described in [19], at high frequencies the charge fluctuations within the channel are coupled to the gate terminal through the gate-oxide capacitance. The resulting noise current is called “induced gate noise” and it is modeled by the noise source

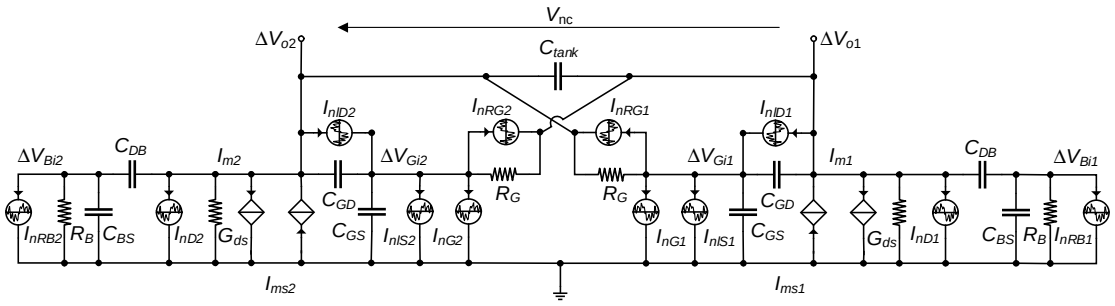

Figure 3.3: Cross-coupled pair small signal model with noise sources

I_{nG}. Moreover, since this noise shares the same origin with the channel thermal noise, they are partially correlated [20]. Finally, the noise originated by the gate leakage current due to carrier tunneling through the oxide is represented by the two sources I_{nlS} and I_{nlD}. In fact, the gate tunneling current is partitioned between source and drain. Since these leakage currents are due to barrier control processes, they give rise to shot noise, which features a white power spectral density (PSD).

The list of the unilateral PSDs of all the previously described noise sources follows:

$$S_{\mathrm{I_{nD}}} = 4\,k\,T\,\gamma_{\mathrm{nD}}\,G_{\mathrm{m}} \tag{3.2}$$

$$S_{\mathrm{I_{nRG(B)}}} = 4\,k\,T/R_{\mathrm{G(B)}} \tag{3.3}$$

$$S_{\mathrm{I_{nG}}} = 4\,k\,T\,\beta_{\mathrm{nG}}\,(\omega C_{\mathrm{GS}})^2/G_{\mathrm{m}} \tag{3.4}$$

$$I_{\mathrm{nG}} \cdot I^*_{\mathrm{nD}} = j\,c_{\mathrm{g}}\,4\,k\,T\sqrt{\gamma_{\mathrm{nD}}\,\beta_{\mathrm{nG}}} \tag{3.5}$$

$$I^*_{\mathrm{nG}} \cdot I_{\mathrm{nD}} = -j\,c_{\mathrm{g}}\,4\,k\,T\sqrt{\gamma_{\mathrm{nD}}\,\beta_{\mathrm{nG}}} \tag{3.6}$$

$$S_{\mathrm{I_{nlS(D)}}} = 2\,q\,I_{\mathrm{lS(D)}} \tag{3.7}$$

where k is the Boltzmann constant, T is the temperature (300 K), q is the electron charge, γ_{nD} is the drain thermal noise excess factor ($2n/3$ in SI and $n/2$ in WI for long-channel devices), β_{nG} is the gate thermal noise excess factor ($4/(15n)$ in SI and $1/(5n)$ in WI), c_{g} is the correlation coefficient (0.4 in SI and 0.6 in SI), $\mathrm{I_{lS}}$ is the gate to source and $\mathrm{I_{lD}}$ the gate to drain leakage current [19].

LTI analytical derivation of phase noise

As mentioned above, the linear time-invariant analysis consists in computing the transfer functions of each noise current source to the output and then to convert it from voltage noise to phase noise. The last step takes into account that only half of the total noise power is carried by phase-modulate (PM) components and contributes to phase noise, since amplitude-modulated (AM) components are rejected by the oscillator itself [4].

Fig. 3.3 shows the small-signal equivalent circuit of the system. To reduce the complexity of the analysis with respect to the complete transistor small-signal model, source and drain access resistances are excluded, since they are generally so small that the poles associated to them are placed beyond the transistor transit frequency, where this model is no more valid. The gate-bulk capacitance C_{GB} is neglected as well, since it is the smallest among the parasitic capacitances as resulting from device simulations and/or measurements. In the end, the analyzed noise sources are drain noise current, induced gate noise and their correlation, gate and substrate resistance noise current, source and drain leakage noise current. Being a small signal analysis, a small differential oscillation amplitude A_{diff} (a few U_{T}) is assumed in order to get valid results. Moreover, this assumption allows to consider the source node V_{S} as an ac ground.

The first step of the analysis is to apply the KCL to the 6 nodes in the circuit for each noise current, yielding the equivalent differential output noise voltage of the cross-coupled pair $V_{\mathrm{nc}} = V_{\mathrm{o2}} - V_{\mathrm{o1}}$ as a function of the given noise source I_{ni}. The second step is to compute the PSD of V_{nc}, i.e. $S_{\mathrm{V_{nc}}} = V_{\mathrm{nc}}^* \cdot V_{\mathrm{nc}} = |H_{\mathrm{I_{ni}}}|^2 S_{\mathrm{I_{ni}}}$, where $H_{\mathrm{I_{ni}}}$ is the transfer function from I_{ni} to V_{nc}. Then, including the noise coming from the inductor losses, $S_{\mathrm{V_{nL}}} = 4kTr$, the total noise voltage PSD $\mathrm{V_n}$ is derived as $S_{\mathrm{V_n}} \simeq [\omega_0/(2\Delta\omega)]^2 (S_{\mathrm{V_{nL}}} + S_{\mathrm{V_{nc}}}) = [f_0/(2\Delta f)]^2 (S_{\mathrm{V_{nL}}} + S_{\mathrm{V_{nc}}})$. In the end, the previous result is used to obtain the phase noise in dBc/Hz, $\mathscr{L} = 10\log_{10}(S_{\mathrm{V_n}}/A^2)$.

The list of $S_{\mathrm{V_{nc}}}$ of each noise source follows

$$I_{\mathrm{nD}} : 4kT\gamma_{\mathrm{nD}} G_{\mathrm{m}}\, ab/c, \tag{3.8}$$

$$I_{\mathrm{nRG}} : 4kTR_{\mathrm{G}} \left[G_{\mathrm{m}}^2 + (2C_{\mathrm{GD}} + C_{\mathrm{GS}})^2 \omega^2\right] a/c, \tag{3.9}$$

$$I_{\mathrm{nRB}} : 4kTR_{\mathrm{B}} \left[G_{\mathrm{m}}^2 (n-1)^2 + C_{\mathrm{DB}}^2 \omega^2\right] b/c, \tag{3.10}$$

$$I_{\mathrm{nG}} : 4kT \left(\beta_{\mathrm{nG}} C_{\mathrm{GS}}^2 \omega^2 / G_{\mathrm{m}}\right) \left[(1 + G_{\mathrm{m}} R_{\mathrm{G}})^2 + C_{\mathrm{GD}}^2 R_{\mathrm{G}}^2 \omega^2\right] a/c, \tag{3.11}$$

$$I_{\mathrm{nD}}^* I_{\mathrm{nG}} : -4kTc_{\mathrm{g}} R_{\mathrm{G}} C_{\mathrm{GS}} \omega \sqrt{\gamma_{\mathrm{nD}} \beta_{\mathrm{nG}}}\, ad/c, \tag{3.12}$$

$$I_{nlS} : 2qI_{\mathrm{lS}} \left[1 + \left(2 + G_{\mathrm{mR_G}}\right) \left(G_{\mathrm{mR_G}} + C_{\mathrm{GD}}^2 R_{\mathrm{G}}^2 \omega^2\right)\right] a/c, \tag{3.13}$$

$$I_{nlD} : 2qI_{\mathrm{lD}} \left(2 + G_{\mathrm{mR_G}}\right) \left(2 + G_{\mathrm{mR_G}} + C_{\mathrm{GS}}^2 R_{\mathrm{G}}^2 \omega^2\right) a/c, \tag{3.14}$$

where

$$a = 1 + (C_{\mathrm{DB}} + C_{\mathrm{BS}})^2 R_{\mathrm{B}}^2 \omega^2, \tag{3.15}$$

$$b = 1 + (C_{\mathrm{GD}} + C_{\mathrm{GS}})^2 R_{\mathrm{G}}^2 \omega^2, \tag{3.16}$$

$$c = (G_{\mathrm{ds}} - G_{\mathrm{m}})^2 + (C_{\mathrm{DB}} + 4C_{\mathrm{GD}} + C_{\mathrm{GS}} + 2C_{\mathrm{tank}})^2 \omega^2, \tag{3.17}$$

$$d = \left[C_{\mathrm{GD}} + (C_{\mathrm{GD}} + C_{\mathrm{GS}}) \left(1 + G_{\mathrm{mR_G}}\right)\right] \omega. \tag{3.18}$$

Tech	$I_{\text{spec}_\square}$ (nA)	n	f_0 (GHz)	L_{tank} (nH)	Q_{L}	r_{L} Ω	C_{tot}
40-nm	650	1.48	1	8	10	5	3.13
28-nm	850	1.46	1	8	10	5	3.13

Table 3.2: Description of the simulation parameters for the analysis of phase noise

3.3.2 Validation of the Phase Noise Analysis

Simulation strategy

In order to validate the PSDs shown in Section 3.3.1, the class-B oscillator is simulated in ADS and the same parameters are used to get numerical results from the previous analytical expressions. Two different commercial bulk CMOS technologies are investigated, namely a 40-nm [13] and a 28-nm. Similarly to the analysis in Section 3.2, the simulations are carried out keeping the parameters shown in Table 3.2 constant, where $r_{\text{L}} = 2\pi f_0 L_{\text{tank}}/Q_{\text{L}}$ and $C_{\text{tot}} = 1/[(2\pi f_0)^2 L_{\text{tank}}\left(1+1/Q_{\text{L}}^2\right)]$. The Inversion Coefficient methodology is employed in order to validate the results across all the regions of operation of the cross-coupled pair, as described in [19]. Three values of IC are chosen, i.e. 0.1, 1 and 10, representing WI, MI and SI. The bias current I_{b} is chosen such that $A_{\text{diff}} = 100$ mV for each value of IC and the transistors are sized accordingly, $W/L = I_{\text{b}}/\left(2IC I_{\text{spec}_\square}\right)$. The parasitic capacitances, G_{m} and G_{ds} are extracted from the Y-parameters of the transistors, obtained with a separate S-parameter simulation, as described in [13]. Moreover, the leakage currents I_{lS} and I_{lD} are evaluated using the DC current through the transistors gate. In the end, R_{G} and R_{B} are estimated from the measurements reported in [13, 14, 21]. As a consequence, they are removed from the compact model of the transistors.

A harmonic balance simulation is carried out for verifying the oscillator functionality and the phase noise extraction is run on top of it. In order to carry out a fair comparison between analytical and simulated results, explicit noise sources are introduced in the schematic. This strategy allows to have direct control on the PSDs of such noise sources. Therefore, in addition to R_{G} and R_{B} and their noise, the drain noise current, the induced gate noise current and the gate leakage currents are removed from the compact model. As a consequence of the explained approach, the correlation between I_{nD} and I_{nG} could not be included and verified.

Simulation results

Figs. 3.4a and 3.4b show the phase noise for each noise source separately as $\mathscr{L}_{\text{I}_{\text{ni}}}$ evaluated at $\Delta f = 1$ MHz frequency offset. For each noise source, analytical and simulated results are reported, including the contribution of both transistors. In general, the simulated values match the analytical counterpart very well for both technologies, except for the phase noise associated to R_{B}. As shown by (3.10), this contribution depends strongly on the sub-threshold

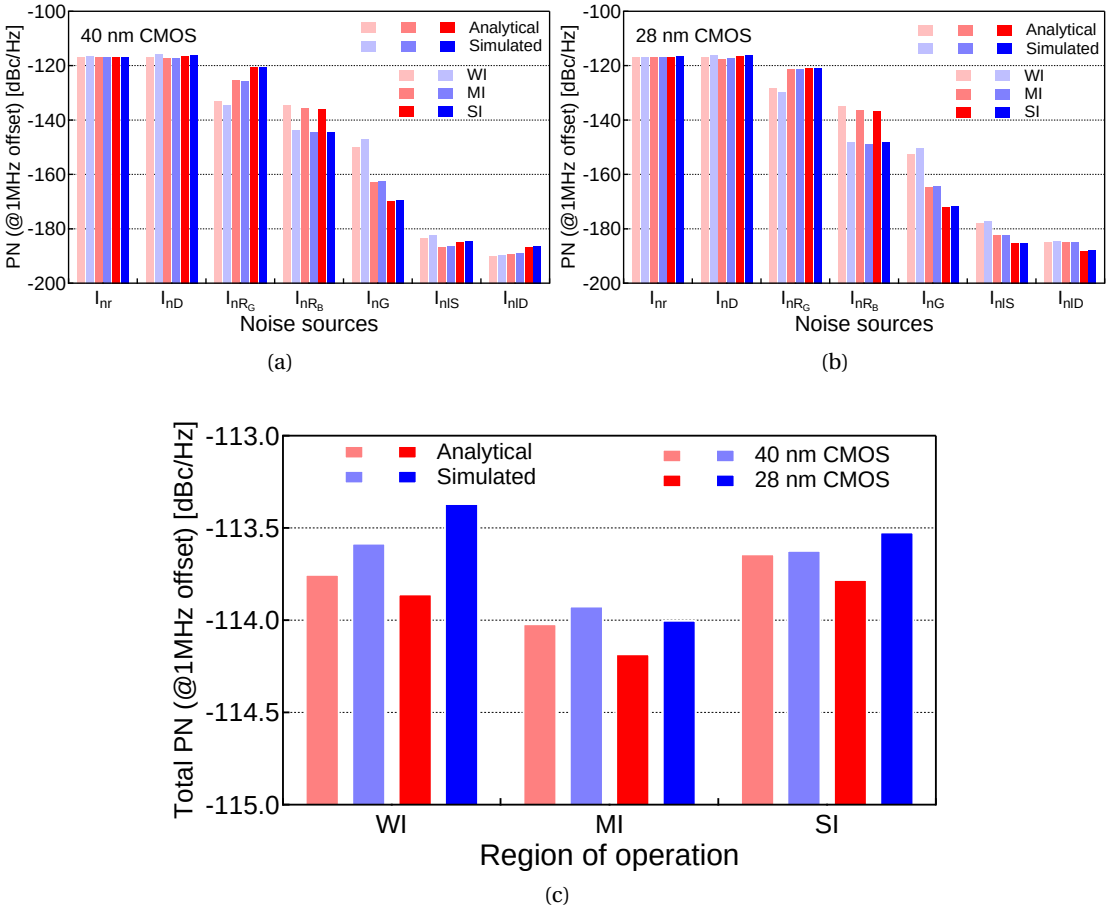

Figure 3.4: Phase noise single contributions (a) for 40-nm CMOS technology, (b) for 28-nm CMOS technology and (c) total phase noise vs. *IC*

slope factor n. This value is extracted from measurements and it is considered constant from WI to SI although it is actually bias dependent [19]. A first explanation for this mismatch is that it is not possible to extract directly the value of n used in BSIM6, where it is bias dependent. The strong dependence on n is verified with a simplified EKV transistor model in which this parameter is defined externally: the phase noise due to R_B changes strongly with n as expected. In order to have a good matching, n should be around 1.2 instead of the values given in Table 2.2. Another reason can be related to the model used to describe the bulk resistance. A single resistance placed between the intrinsic and the extrinsic bulk nodes may not be suited for the purpose and a more complex model may be necessary.

Fig. 3.4 shows the total phase noise including all contributions as a function of *IC*. The match between the analytical and simulated results is good across all the values of *IC* for both technologies. The results coming from the analysis are in both cases slightly underestimating the simulated results (typically 0.5 dB), but remain a very good guess. The MI is identified as a sweet spot for both low-power and low-noise oscillator design. Moreover, the most relevant

contribution, after the noise of the tank resistance and the channel thermal noise, is the one of the gate resistance, whose value in SI is only 4-5 dB lower than the former ones in both technologies. The reason is that the gate resistance per unit finger has increased dramatically with respect to older technologies [13, 14]. In addition to that, this value increases even further for finger width below 1 µm. For these reasons, a large number of fingers with 2 µm or more per finger is recommended in order to minimize this contribution. For most of practical cases, the noise of the tank resistance, of the drain current and of the gate resistance dominate and are sufficient to accurately estimate the total phase noise of the oscillator.

3.4 Summary

In this chapter, the LC oscillator is analyzed under the point of view of power consumption and phase noise. First, several circuit topologies are studied to understand which one requires the lowest power consumption to get a given amplitude at a specific frequency without spoiling the phase noise performance. In this perspective, class-B, class-C and class-D oscillators are analyzed. Their bias current, supply voltage, width and phase noise are simulated as a function of the inversion coefficient of the cross-coupled transistors. In order to quantify their overall performance, a FoM is considered, showing that depending on *IC*, class-D shows the best behavior in WI, while class-C in MI. Nevertheless, comparing the power consumption, class-D clearly is the less power-hungry for any *IC* value, taking advantage of the reduced supply voltage. MI is the best trade-off between power and area for class-B and class-C, while the region between WI and MI is the best one for class-D.

Then, a study is carried out to understand to which extent an analytical small-signal approach is suitable to analyze phase noise in class-B LC oscillators. For this, an extended small-signal model of the transistors is used including all the noise sources, in order to derive the transfer function of each of them and to calculate their contribution to the total phase noise. The analytical expressions are simplified and compared with the simulated results obtained from a LC oscillator with a 40-nm and a 28-nm CMOS technology. This linear analysis is capable of predicting the phase noise contributions in the $1/f^2$ region with good accuracy throughout all values of *IC*. The MI is identified as a sweet spot not only for low-power but also for low-noise oscillator design. The only noise source which shows a consistent discrepancy between the two results is the one associated to R_B. One possible cause is that the bulk resistance is not modeled accurately enough with a single resistance for this purpose and therefore requires further investigations. However it remains still much smaller than the total noise of the other dominant contributions.

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4 Power-Optimized Oscillators for a FMCW Radar SoC

As introduced in the previous chapters, a highly integrated radar SoC embedded in mobile devices and IoT nodes requires the use of an advanced CMOS technology and sets a strong constraint on the power budget. Developing an efficient design methodology in these advanced technology nodes to reach the lowest power at low voltage becomes of paramount importance. Within the PLL, the oscillator is clearly the most power-hungry building block, particularly at mm-wave frequency. The objective is therefore to minimize the power consumption while ensuring a very large tuning range without significantly degrading the phase noise. In addition, the novel design methodology for mm-wave oscillators needs to overcome the challenges posed by the ultra low voltage, the large gate resistance, the highly resistive metal lines and vias and the strong layout constraints of advanced CMOS technologies.

In this chapter, the design of a low-power oscillator with a wide frequency tuning range for a 60-GHz FMCW radar application is addressed. First, FMCW approach is described and the advantages over the other types of radars for low-power applications are assessed. Then, the crucial choice of the oscillator output frequency and the frequency tuning method are addressed. A comparison between a 20-GHz VCO and a DCO is proposed, in order to analyze which tuning approach is best suited at mm-wave, mainly accounting for the limited quality factor of passive devices. Finally, the proposed VCO is embedded in a radar system built with discrete components in order to show its robust performance for the measurement of the distance of a static target. Part of the material in this chapter is presented in [1, 2].

4.1 FMCW Radar Systems

A radar system can be built on different working principles, among which the more notable are CW, FMCW and IR-UWB. FMCW is chosen for the targeted short-range and low-power applications.

	CW	FMCW	IR-UWB
Measured Quantities	Speed	Distance Speed	Distance Speed
Bandwidth	No	Large	Large
Peak Output Power	Low	Low	High
Maximum Detection Range	Long	Long	Short
Range Resolution	No	High	High
System Complexity	Low	Low	High

Table 4.1: Comparison of features among radar implementations.

4.1.1 Comparison among Radar Implementations

FMCW offers several advantages over the other radar implementations. Table 4.1 shows a comparison of the main features of each radar architecture. CW can detect only the speed of the target through Doppler effect while FMCW and IR-UWB can detect both distance and speed. The former transmits at a single frequency, while the others either sweep across a large bandwidth or generate a narrow pulse with a rich frequency content. Compared to CW and FMCW, IR-UWB needs to transmit a pulse with a large peak output power to improve signal-to-noise ratio (SNR) at longer distance: such peak output power can be challenging to achieve in advanced technology nodes with limited voltage supply. Nevertheless, averaging across the required bandwidth the output power is limited for both FMCW and IR-UWB. They both achieve good range resolution but the latter requires a high-speed analog-to-digital converter (ADC) while the beat frequency in FMCW is limited to few tens of megahertz. Overall, for the targeted applications, the system complexity and the expected power consumption, FMCW is preferred over IR-UWB.

4.1.2 Principles of FMCW Radars

A FMCW radar transmits continuously a frequency chirp $x_{\mathrm{TX}}(t)$ with a given bandwidth B, which allows to sense the distance d_{T} from a target and its speed v_{T}. The distance is extracted from the delay $\Delta\tau$ accumulated by the signal while traveling to the target and then back to the sensor after the reflection. In the receiver, the transmitted chirp $x_{\mathrm{TX}}(t)$ is mixed with the delayed one $x_{\mathrm{RX}}(t,\Delta\tau)$ and the result is a low frequency signal x_{LF} containing the so-called beat frequency f_{b} which is proportional to $\Delta\tau$. Finally, it is trivial to extract d_{T}. As far as the speed v_{T} is concerned, due to the Doppler effect, a frequency shift is applied to $x_{\mathrm{RX}}(t)$ by the moving target and it can be observed in x_{LF} as well.

Fig. 4.1 and Fig. 4.2 show the FMCW working principle in the case of a triangular modulation

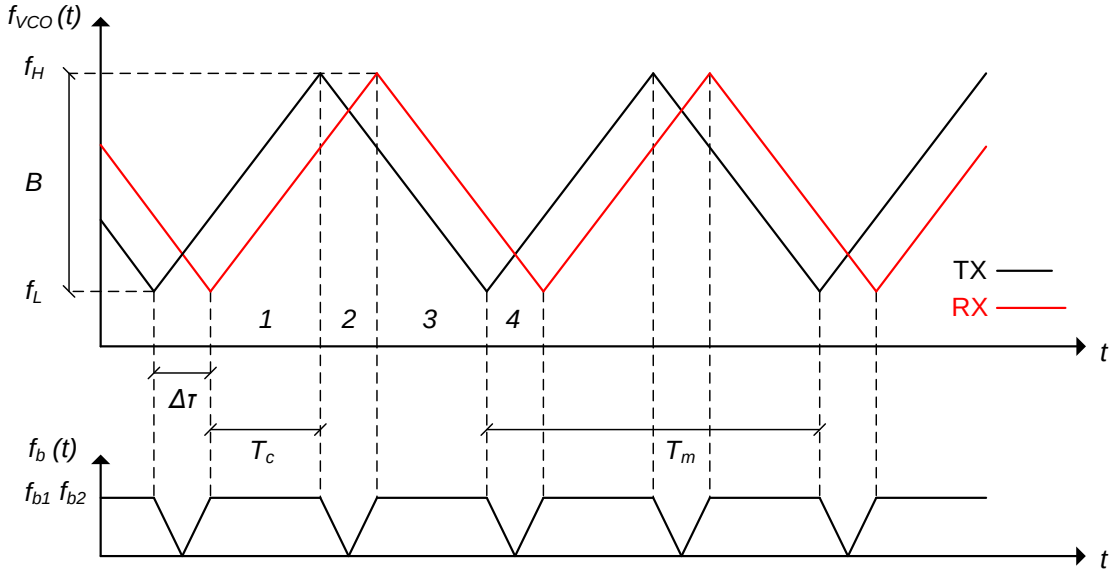


Figure 4.1: FMCW working principle with triangular modulation for a static target.

with two different scenarios. A similar analysis applies to the case of a sawtooth modulation. The first scenario consists in a static target. The transmitted signal is given by

$$x_{\mathrm{TX}}(t) = A_{\mathrm{TX}} \begin{cases} \cos\left[2\pi\left(f_{\mathrm{L}}\, t_{\mathrm{rep}} + \dfrac{B}{T_{\mathrm{m}}}\, {t_{\mathrm{rep}}}^2\right)\right] & \text{if } 0 < t_{\mathrm{rep}} \leq \frac{T_{\mathrm{m}}}{2} \quad (4.1a) \\ \cos\left[2\pi\left((f_{\mathrm{L}} + 2B)\, t_{\mathrm{rep}} - \dfrac{B}{T_{\mathrm{m}}}\, {t_{\mathrm{rep}}}^2\right)\right] & \text{if } \frac{T_{\mathrm{m}}}{2} < t_{\mathrm{rep}} < T_{\mathrm{m}} \quad (4.1b) \end{cases}$$

where A_{TX} is the amplitude of the transmitted signal, f_{L} is the lowest value in the oscillator's frequency sweep, B is the sweep bandwidth, T_{m} is the modulation period and $t_{\mathrm{rep}} = t - nT_{\mathrm{m}}$ represents the cyclic time in the n^{th} cycle. The received signal is an echo with a delay of $\Delta\tau$ and is given by

$$x_{\mathrm{RX}}(t, \Delta\tau) = A_{\mathrm{RX}} \begin{cases} \cos\left[2\pi\left(f_{\mathrm{L}}(t_{\mathrm{rep}} - \Delta\tau) + \dfrac{B}{T_{\mathrm{m}}}(t_{\mathrm{rep}} - \Delta\tau)^2\right)\right] & \text{if } 0 < t_{\mathrm{rep}} \leq \frac{T_{\mathrm{m}}}{2} \quad (4.2a) \\ \cos\left[2\pi\left((f_{\mathrm{L}} + 2B)(t_{\mathrm{rep}} - \Delta\tau) - \dfrac{B}{T_{\mathrm{m}}}(t_{\mathrm{rep}} - \Delta\tau)^2\right)\right] & \text{if } \frac{T_{\mathrm{m}}}{2} < t_{\mathrm{rep}} < T_{\mathrm{m}} \quad (4.2b) \end{cases}$$

where A_{RX} is the amplitude of the received signal, $\Delta\tau = 2d_{\mathrm{T}}/v$ and v is the propagation speed. The down-converted signal in sections 1 and 3 is given by

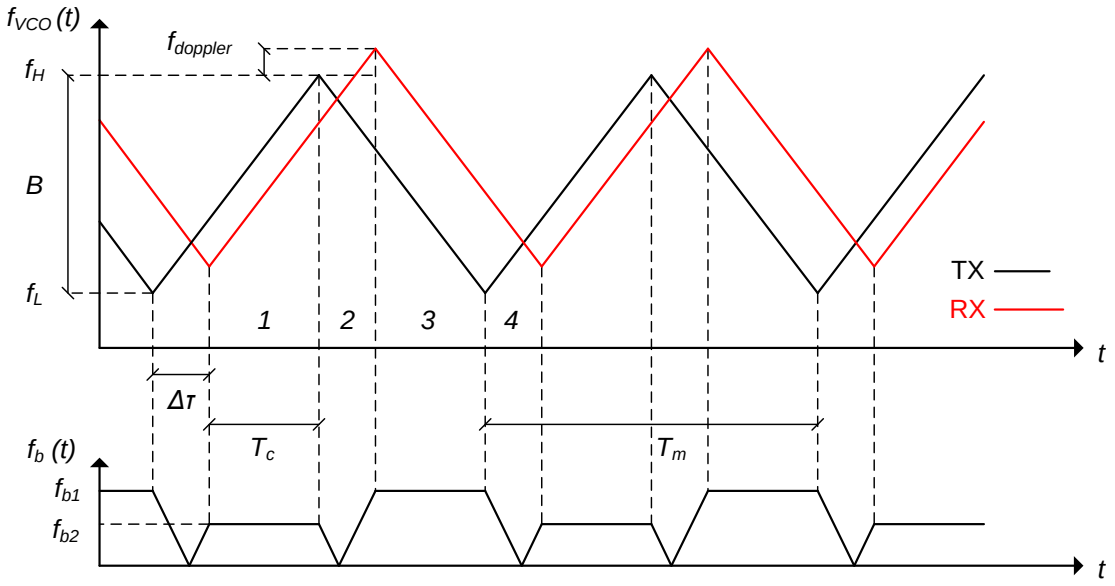


Figure 4.2: FMCW working principle with triangular modulation for a moving target.

$$x_{\mathrm{LF}}(t,\Delta\tau) = A_{\mathrm{LF}} \begin{cases} \cos\left[2\pi\left(f_{\mathrm{L}}\Delta\tau + \dfrac{B}{T_{\mathrm{m}}}\left(2t_{\mathrm{rep}}\Delta\tau - \Delta\tau^2\right)\right)\right] & \text{if } \Delta\tau < t_{\mathrm{rep}} \leq \frac{T_{\mathrm{m}}}{2} \quad (4.3a) \\ \cos\left[2\pi\left((f_{\mathrm{L}}+2B)\Delta\tau - \dfrac{B}{T_{\mathrm{m}}}\left(2t_{\mathrm{rep}}\Delta\tau - \Delta\tau^2\right)\right)\right] & \text{if } \frac{T_{\mathrm{m}}}{2} + \Delta\tau < t_{\mathrm{rep}} < T_{\mathrm{m}} \quad (4.3b) \end{cases}$$

where A_{LF} is the amplitude after mixing and G_{mixer} is the gain of the mixer. The phase of $x_{\mathrm{LF}}(t,\Delta\tau)$ contains a constant factor and a time-dependent component. Sections 2 and 4 are neglected assuming $\Delta\tau \ll T_{\mathrm{m}}$. The resulting beat frequency can be calculated as

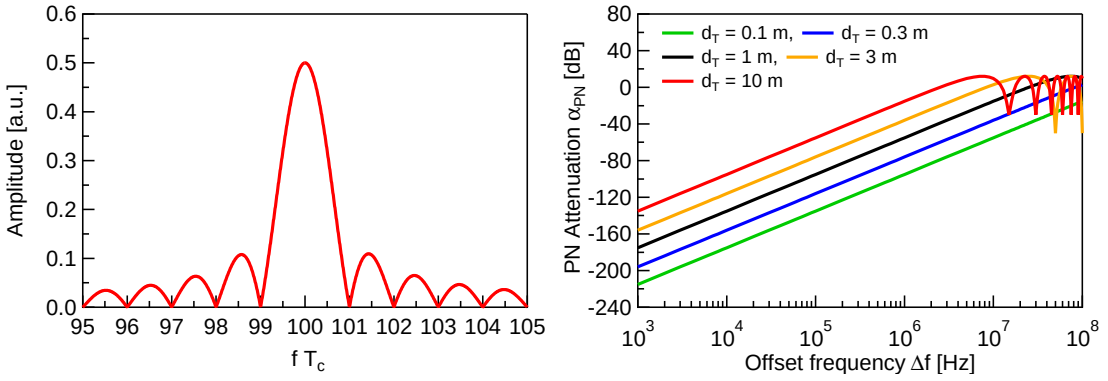
$$f_{\mathrm{b}}(t,\Delta\tau) = \frac{1}{2\pi}\frac{d\varphi(t,\Delta\tau)}{dt} = \frac{2B}{T_{\mathrm{m}}}\Delta\tau = \frac{2B}{T_{\mathrm{m}}}\frac{2d_{\mathrm{T}}}{v} \tag{4.4}$$

As shown in Fig. 4.1, d_{T} can be extracted as:

$$d_{\mathrm{T}} = \left(\frac{f_{\mathrm{b1}} + f_{\mathrm{b2}}}{2}\right)\frac{v}{4}\frac{T_{\mathrm{m}}}{B} \tag{4.5}$$

An important metric for a radar is the range discrimination, which represents the theoretical lower limit distance between two or more targets to distinguish among their respective echoes. Starting from (4.4), the beat frequency can be observed for a limited time, i.e. the chirp duration T_{c}, which is equal to

$$T_{\mathrm{c}} = \frac{T_{\mathrm{m}}}{2} - \Delta\tau = \frac{T_{\mathrm{m}}}{2} - \frac{2d_{\mathrm{T}}}{v} = \frac{T_{\mathrm{m}}}{2}\left(1 - \frac{4d_{\mathrm{T}}}{vT_{\mathrm{m}}}\right) \simeq \frac{T_{\mathrm{m}}}{2} \tag{4.6}$$



(a) (b)

Figure 4.3: (a) Positive spectrum of the beat signal with $f_b T_c = 100$ and (b) IF phase noise attenuation due to autocorrelation for different distances from the target.

In such a window, measuring the beat frequency is equivalent to observe a truncated sinusoidal signal at frequency f_b:

$$x(t) = \begin{cases} \cos(2\pi f_b t) & \text{if } 0 \le t \le T_c \\ 0 & \text{otherwise} \end{cases} \tag{4.7}$$

whose Fourier transform is given by

$$X(f) = \frac{T_c}{2}\{\text{sinc}[T_c(f+f_b)] + \text{sinc}[T_c(f-f_b)]\} \tag{4.8}$$

Fig. 4.3a shows $X(f)$: the distance between the peak and the first zero is $\delta f T_c = 1$, which can be used as a rough estimation of the discrimination bandwidth. As a consequence, together with (4.4) and (4.6), we can get an estimate of the range discrimination as well:

$$\delta f = \frac{1}{T_c} = \frac{2B}{T_m}\delta\tau = \frac{2B}{T_m}\frac{2\delta d}{v} \tag{4.9}$$

$$\rightarrow \delta d = \frac{T_m}{2T_c}\frac{v}{2B} = \frac{1}{1-4\frac{d_T}{vT_m}}\frac{v}{2B} \simeq \frac{v}{2B} \tag{4.10}$$

As shown in (4.10), the range discrimination is only limited by the sweep bandwidth: in order to improve the resolution, it is mandatory to increase the frequency excursion covered by the oscillator and hence to choose a suited frequency band for the targeted application. In practice, when f_b is calculated, a windowed digital Fourier transform (DFT) is used. When the Blackman-Harris windowing is employed, the range resolution is worsened by a factor 1.8 [3].

In the second scenario, depicted in Fig. 4.2, a moving target is taken into account. The received

signal is an echo with a delay of $\Delta\tau$ and a frequency shift of f_D and is given by

$$x_{RX}(t,\Delta\tau) = A_{RX}\begin{cases} \cos\left[2\pi\left(\left(f_L+f_D\right)\left(t_{rep}-\Delta\tau\right)+\right.\right. \\ \left.\left.\frac{B}{T_m}\left(t_{rep}-\Delta\tau\right)^2\right)\right] & \text{if } \Delta\tau < t_{rep} \le \frac{T_m}{2} \quad (4.11a) \\ \cos\left[2\pi\left(\left(f_L+f_D+2B\right)\left(t_{rep}+\right.\right. \\ \left.\left.-\Delta\tau\right)-\frac{B}{T_m}\left(t_{rep}-\Delta\tau\right)^2\right)\right] & \text{if } \frac{T_m}{2}+\Delta\tau < t_{rep} < T_m. \quad (4.11b) \end{cases}$$

The down-converted signal is then given by

$$x_{LF}(t,\Delta\tau) = A_{LF}\begin{cases} \cos\left[2\pi\left(\left(f_L+f_D\right)\Delta\tau - f_D t_{rep}+\right.\right. \\ \left.\left.+\frac{B}{T_m}\left(2t_{rep}\Delta\tau-\Delta\tau^2\right)\right)\right] & \text{if } \Delta\tau < t_{rep} \le \frac{T_m}{2} \quad (4.12a) \\ \cos\left[2\pi\left(\left(f_L+f_D+2B\right)\Delta\tau - f_D t_{rep}+\right.\right. \\ \left.\left.-\frac{B}{T_m}\left(2t_{rep}\Delta\tau-\Delta\tau^2\right)\right)\right] & \text{if } \frac{T_m}{2}+\Delta\tau < t_{rep} < T_m \quad (4.12b) \end{cases}$$

and the resulting beat frequency can be calculated as

$$f_b(t,\Delta\tau) = \frac{1}{2\pi}\frac{d\varphi(t,\Delta\tau)}{dt} = \frac{2B}{T_m}\Delta\tau \pm f_D = \frac{2B}{T_m}\frac{2d_T}{v} \pm \frac{2v_T f_c}{v}, \quad (4.13)$$

where $f_c = (f_L + f_H)/2$ is the average swept frequency. As shown in Fig. 4.2, d_T and v_T can be extracted as:

$$d_T = \left(\frac{f_{b1}+f_{b2}}{2}\right)\frac{v}{4}\frac{T_m}{B}, \quad (4.14)$$

$$v_T = \left(\frac{f_{b1}-f_{b2}}{2}\right)\frac{v}{2f_c}. \quad (4.15)$$

Another important aspect in FMCW radars is the impact of phase noise on the measurement of distance and velocity. Since the transmitted and the received signals are partially correlated, the phase noise at IF after mixing is attenuated by a coefficient which is dependent on both the offset frequency and the distance of the target [2, 3]:

$$\alpha_{PN} = 4\sin^2\left(\frac{2\pi\,\Delta f\, d_T}{c}\right). \quad (4.16)$$

Fig. 4.3b shows α_{PN} versus Δf for several values of d_T. There are different limitations due to phase noise. First, there is the phase noise of the TX-to-RX leakage, which is a quite strong component at very low frequency due to several paths, both on- and off-chip. The close-in phase noise of the leakage is strongly attenuated by autocorrelation while the far-out phase noise can impact the RX NF. As shown in [3, 4], the thermal noise PSD at the RX input equal to 174 dBm/Hz + NF has to be compared to the attenuated phase noise equal

to $\mathscr{L}(\Delta f) + P_{\text{TX,out}} - A_{\text{TX-RX}} + \alpha_{\text{PN}}$, where $P_{\text{TX,out}}$ is the TX output power and $A_{\text{TX-RX}}$ is the TX-to-RX isolation. Second, the phase noise of the down-converted IF signal contributes to the deterioration of the SNR and hence on the precision on the measurement of distance and velocity [5, 6]. For a given SNR, taking into account the attenuation due to autocorrelation, the phase noise should be lower than

$$\mathscr{L}(\Delta f) < \frac{f_{\text{PLL}}}{4\pi\,\text{SNR}\,\Delta f^2} \frac{1}{1-\exp\left(-\frac{4\pi f_{\text{PLL}} d_{\text{T}}}{c}\right)}. \tag{4.17}$$

Third, the phase noise of a clutter with a large radar cross-section (RCS) may mask the presence of a small target, which generates a weaker signal [4]. Forth, the phase noise has also an impact on the range resolution. In fact, two close targets are harder to distinguish if the width of the lobe shown in Fig. 4.3a is increased by phase noise [7].

4.2 Toward a FMCW Radar SoC

The frequency band V is the most suited for the target applications since it is license free in many countries, it is not heavily occupied by communication systems, it allows the use of a large bandwidth and its high absorption of signals is not a limit at short distances. As far as the frequency generation is concerned, a lot of different paths can be chosen at the system-level taking into account the trade-offs which involve power consumption, covered bandwidth, frequency resolution and phase noise.

4.2.1 Approaches to Frequency Synthesis for FMCW Radar

At the center of the FMCW radar SoC there is the frequency chirp generator. A PLL is chosen for its lower power consumption compared to direct digital frequency synthesizer (DDFS) and its better phase noise and robustness against process-voltage-temperature (PVT) variations compared to an open-loop approach. Since the primary goal in the design of this SoC is achieving a minimum in terms of power consumption and the oscillator is the most power-hungry block in the PLL, this circuit is the first target of the power optimization process. The design choices regarding the output frequency and the frequency tuning method are of paramount importance pursuing this goal.

As far as the output frequency of the oscillator is concerned, it can be set equal to the transmitted one or a sub-harmonic of it, which requires a frequency multiplication. The former approach saves the power of the multiplier but it implies a faster frequency divider in the PLL feedback; moreover, the quality factor of capacitors is degraded at higher frequencies while the quality factor of inductors doesn't increase as much due to the parasitic capacitance [8]. For an output frequency of 60 GHz, the choice to design the oscillator at 20 GHz is shown to be more efficient and with wider tuning range and better phase noise performance. The reason is the lower tank quality factor at higher frequency and the limited head-room for tuning given

the impact of parasitic capacitances [8].

Regarding the best frequency tuning method at such operating frequencies for the lowest power consumption, it remains an open question. A comparison is carried out in the next sections and it revolves around the use of a varactor to cover part of the frequency bandwidth assisted by a limited number of bands controlled with switched capacitors in a VCO and the use of switched capacitors only to cover the whole band in a DCO. These two techniques are the only available around 20 GHz; if the synthesis of a 60-GHz signal had been chosen, there would have been the option to use transmission lines with configurable floating metal shields as shown in [9].

In order to validate experimentally the suitability of the designed oscillators for radar applications, the VCO is connected to a PLL evaluation board. The synthesized FMCW signal is used in a radar setup including a TX chain and a RX chain which allow to perform ranging measurements.

4.2.2 Design Specification for the Oscillators

The two oscillators have to fulfill some specifications to allow the generation of the FMCW signal. The first is the power consumption P which is to be as small as possible. Then, there is the constraint on the bandwidth B. As described in Section 4.1.2, B defines the theoretical range discrimination and it is expected to be as large as possible. The widest frequency bandwidth available in band V is from 57 to 66 GHz (only 57 to 64 GHz in USA and Canada), i.e. 9 GHz, which translates to a resolution of 1.66 cm. As a consequence, the oscillators have to cover from 19 to 22 GHz.

Regarding the phase noise, a specification can be calculated from (4.17): for a PLL bandwidth f_{PLL} of 1 MHz, a maximum detection range $d_{\mathrm{T,max}}$ of 10 m, a SNR of 15.4 dB (corresponding to a worst case scenario with only one TX, one RX, without averaging, a detection probability of 99 % and a false alarm rate (FAR) of 10^{-8}), the phase noise has to be better than -81.7 and -101.7 dBcHz at 1 MHz and 10 MHz offsets respectively [6]. Considering that the oscillators work a 1/3 of the output frequency, the required phase noise decreases roughly by 9.5 dB to -91.2 and -111.2 dBcHz at 1 MHz and 10 MHz offsets respectively. Such estimation holds if the phase noise is already in the -20 dB per decade region.

4.3 Design of the 20-GHz Oscillators and Divider

The oscillators design is mostly focused on the minimization of power consumption. The strategy to achieve this goal is two-fold: optimizing the resonator to maximize the overall quality factor Q across a very large frequency range; making the circuit as efficient as possible and able to work also at reduced voltage supply. The frequency tuning of the DCO is purely digital, while in the VCO it is a combination of analog and digital. In order to make a fair

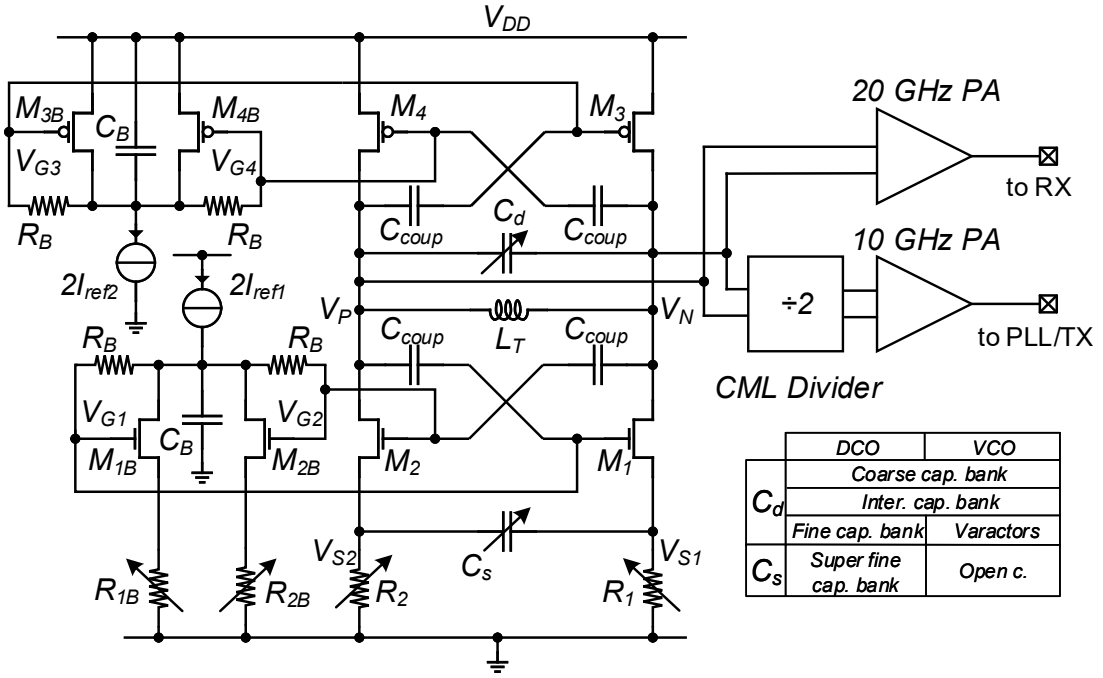


Figure 4.4: Oscillators schematic with the detailed biasing approach, the tuning techniques and the rest of the circuit.

comparison, the two oscillators are designed with the same topology and the same inductor. In addition, a modified version of the DCO is integrated, in which the whole area inside the inductor is filled with active devices and MOM capacitors instead of high resistivity substrate and metal filling. The goal is to study the influence of these devices on the performance of the inductor. A 20-GHz PA is used to output the oscillators signals. Moreover, for measurement purposes and for the integration of the chip in the discrete radar system, a divider by 2 is added to obtain a 10-GHz signal, which is output by a 10-GHz PA.

4.3.1 Design of the Oscillators Core

Fig. 4.4 shows the oscillators schematic: the negative resistance is provided by a complementary cross-coupled (CC) pair structure which allows to increase the transconductance for the same bias current through current reuse achieving higher efficiency. Voltage-biasing is an obvious choice dictated by the limited supply voltage: four diode connected devices M_{1B-4B} provide V_{G1-4} to impose the bias current $I_B = NI_{ref}$, where I_{ref} is a programmable current produced by a proportional to absolute temperature (PTAT) circuit and a current digital-to-analog converter (DAC). I_B is chosen such that the all the transistors work in moderate inversion for best efficiency [10]. Table 4.2 shows the design values for all devices in the VCO and DCO cores.

After start-up, the oscillation amplitude grows and it is sensed by M_{1B-4B}. Due to the nonlinear

L_{1-4} (nm)	W_{1-2} (µm)	W_{3-4} (µm)	C_{coup} (fF)	R_{1-2} (Ω)	I_{ref1} (µA)
30	30	44	30.7	7 - 50	9 - 68.7
L_{1B-4B} (nm)	W_{1B-2B} (µm)	W_{3B-4B} (µm)	R_B (kΩ)	C_B (fF)	I_{ref2} (µA)
60	1	1	14	72	6.3 - 77.9

Table 4.2: Design values in the VCO and DCO.

$I_D(V_G)$ MOSFET characteristic, the sinusoidal voltage around the bias point does not produce a sinusoidal current, but a distorted waveform whose dc component should become larger than I_{ref}. However, the dc current cannot increase since it is imposed equal to I_{ref} by the current source. Consequently, V_{G1-4} decreases such that the dc component of the distorted current in presence of oscillation is exactly equal to I_{ref} [11]. The benefits of this biasing scheme are multiple: it allows to control the oscillation amplitude while keeping a fixed current consumption, it brings the oscillator to work in class-C and it provides a reliable start-up thanks to the larger initial V_{G1-4} [12]. To keep good control on the bias point, the V_D of M_{1B-4B} have to be constant limiting the interference coming from the oscillator differential signal and its harmonics: it is achieved thanks to the shared V_D nodes and the low-pass filtering provided by R_B and C_B.

Some transistors biased in the linear region are placed between the sources and the ground of the NMOS CC pair to implement two variable resistors, R_1 and R_2, which decouple the two nodes and allow to fine tune the frequency through a modified version of the capacitive degeneration technique as explained in Section 4.3.2. The contribution of $R_{1,2}$ to the total phase noise is assessed by getting their ISF and cyclo-stationary noise from simulation as shown in [13]. The latter simulations show that their impact is negligible compared to the CC pairs in the $1/f^3$ and $1/f^2$ regions.

4.3.2 Design of the Oscillators Resonators

The inductor used in the tank is differential with a single turn. In order to obtain the best quality factor, it is implemented using the layer with lowest resistivity. However, a shield is not used, allowing to layout the oscillator partially under the inductor. The parameters are determined with a planar electromagnetic simulator leading to $L = 130\,\text{pH}$ with $Q_L = 25$ at 20 GHz. The placement of decoupling capacitor under the inductor in the middle of the loop where the magnetic field is minimum has a marginal impact on Q_L and the self resonance frequency, as emerged from EM simulations (less than 1% for both parameters).

The digital frequency tuning in the DCO is implemented with four capacitor banks with frequency steps of decreasing size. This approach allows to achieve both a large tuning range and high frequency resolution with a reasonable number of tuning elements (TE). The banks

Bank	No. TE	C (fF)	ΔC (fF)	Q_C	C_{on}/C_{off}
Coarse	32	18.4	5.9	20	2.8
Intermediate	32	1.9	0.6	22	2.2
Fine	32	1.1 / 1.7	0.036	240	1.04
Super fine	16	6	0.004	20	3.1
Varactor	1	49.4 (at −0.45 V) 60.8 (at 0 V) 97.6 (at 0.45 V)	48.2	16.5 (at −0.45 V) 10.8 (at 0 V) 4.5 (at 0.45 V)	2

Table 4.3: Performance of the capacitor banks.

are matrices of identical TE composed of MOM capacitors and switches controlled by binary to thermometer decoders. The thermometric approach is chosen over the binary to ensure monotonicity in spite of a larger number of control lines. In each matrix, row and column signals are used to control each element; when all the TE of Nth row are on, the (N+1)th row signal is used to lock the whole Nth row to be able to turn off all the column signals. Table 4.3 reports the performance of each capacitor bank.

In Fig. 4.5a C_1 and C_2 are the capacitors of the coarse and intermediate TE banks. On top of the proper sizing of the capacitors and the switches, the optimization of the TE layout is crucial to get the best trade-off between the tuning range and the quality factor (Fig. 4.4b). The metal lines between the capacitors and the switch terminals both increase the parasitic capacitance and especially the series resistance. Switches and digital gates, which are part of the decoder, are placed under the capacitors, making their connection easier and achieving a very compact layout for the TE and consequently also for the matrices.

Fig. 4.5b shows the structure of the fine TE bank. When the technique presented in [14] is applied at mm-wave, the capacitors absolute value is very small and the parasitic capacitance $C_{par,3}$ in parallel to the switch is significant. When the switch turns on, the capacitance changes by:

$$\Delta C_3 = \frac{\delta C^2}{(4(C_3 + C_{par,3}) + 2\delta C)} \cong \frac{\delta C^2}{(4(C_3 + C_{par,3}))} \quad \text{if } \delta C \ll C_3. \tag{4.18}$$

The layout is implemented with the same approach as for the coarse and intermediate arrays.

In Fig. 4.5a C_4 is the capacitor of the super fine bank. It is composed of TE with the same structure as the coarse and intermediate bank but it is placed at the source of the NMOS CC pair. This technique, called capacitive degeneration, is presented in [15, 16] and it is implemented differently here. It relies on a property of the CC pair: any capacitance placed at the source (C_s) appears as a negative capacitance at the drain multiplied by a factor $K \ll 1$:

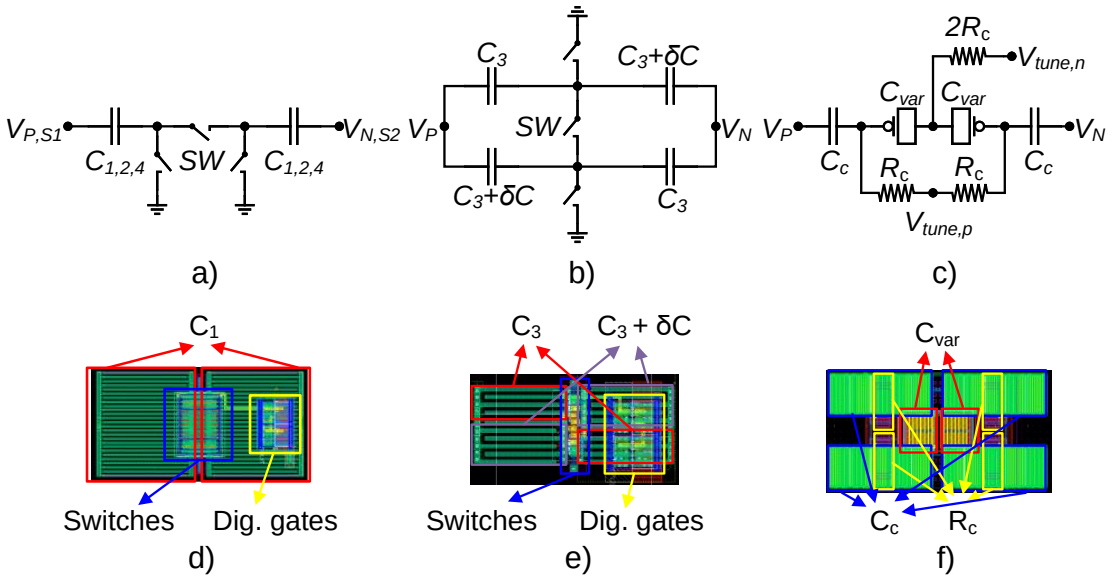


Figure 4.5: Schematic of the TE of the a) coarse, medium and super fine bank, b) fine bank and c) the varactors, and the d), e) and f) respective layouts.

$\Delta C_4 = KC_s$ [17]. Nevertheless, instead of two current sources that would require a large V_{DD} for proper strong inversion operation giving good current matching and low noise, two transistors biased in the linear region are used for the chosen low voltage supply and voltage-biased topology. At high frequency, the impedance toward ground is low and the factor K becomes:

$$K = \frac{G_m^2}{(G_m + \frac{1}{R})^2 + (4\pi f_0 C_{4,tot})^2}, \tag{4.19}$$

where G_m is the transconductance of the transistors in the NMOS CC pair, f_0 is the oscillation frequency and $C_{4,tot}$ is the total capacitance between the sources, obtained by summing a fixed and a variable portion. Since Q_f is inversely proportional to $C_{4,tot}$ and f_0, it is possible to obtain a linear tuning only in a small frequency range.

The frequency tuning in the VCO is implemented with both analog and digital systems. For the analog tuning, 2 ac-coupled PMOS varactors (Fig. 4.5c) are used: this allows to control them differentially, without depending on the output common mode hence reducing the flicker noise up-conversion due to common mode fluctuations. Minimum length varactors have a better Q_{var} but have worse C_{on}/C_{off}: twice the minimum length is chosen to obtain a ratio of 3 while preserving a Q_{var} of 10. To cover a wider frequency range, digital tuning is included using the coarse and the intermediate banks described above.

Among the capacitor bank, the coarse one is the biggest contributor to the total capacitance: since Q_{C1} is comparable to Q_L, it is the dominant factor in the degradation of the overall Q. For this reason, it is placed as close as possible to the inductor. The same applies to the varactors,

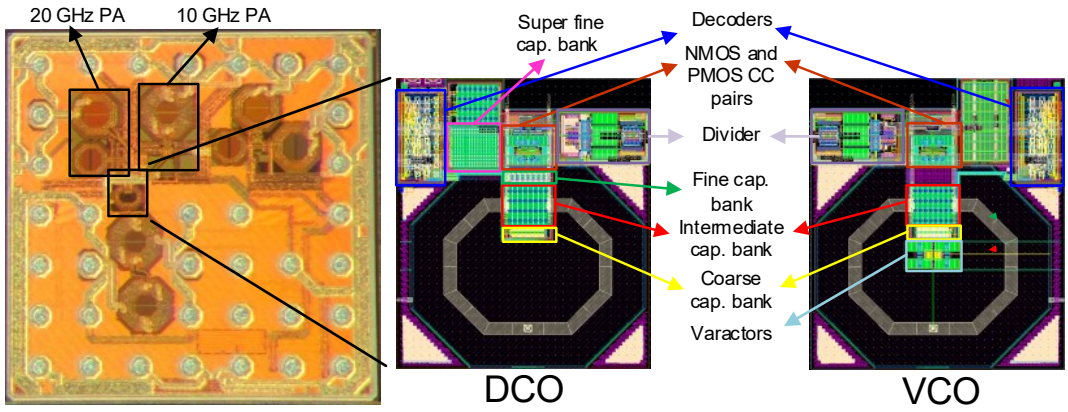


Figure 4.6: Chip micrograph (1.25 mm x 1.25 mm) with the detailed layout of DCO and VCO.

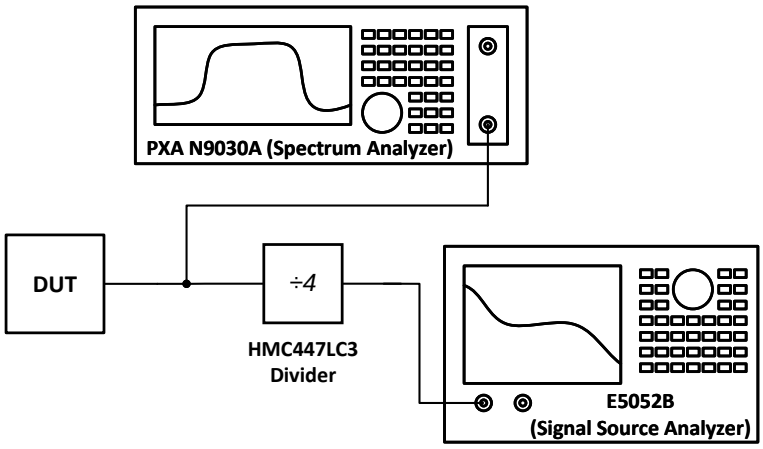


Figure 4.7: Experimental setup used to measure the 20 GHz output of the chip.

whose quality factor $Q_{C,var}$ is half of Q_L. Fig. 4.6 shows the layout of the DCO, which occupies only 0.026 mm^2.

4.3.3 Design of the CML-based Divider and the 20-GHz and 10-GHz PAs

The 20-GHz output buffer is a two-stage PA. Both stages are differential, cascoded and ac-coupled: the first one is loaded with an inductor, while the second with an on-chip balun, which provides a single-ended output, impedance matching and electrostatic discharge (ESD) protection. This PA is designed to provide an output power of 0 dBm across the whole tuning range.

The 20-GHz divider by 2 is implemented with current-mode logic (CML) latches with resistive loads. The 10-GHz buffer is a two-stage PA, in which both stages are differential: the pre-PA is a cascade of two push-pull amplifiers, while the output stage is again cascoded and loaded

Bank	Δf (MHz)	
	at f_{max}	at f_{min}
Coarse	250	120
Intermediate	19	9
Fine	1.6	0.7
Super fine	0.15	0.06
Varactor	910 (total)	420 (total)
	520 (linear)	240 (linear)

Table 4.4: Frequency steps of the switched capacitor banks and frequency tuning range covered with the varactors at f_{min} and f_{max}.

with an on-chip balun. It provides an output power of 2 dBm.

4.4 Experimental Results

The chip is flip-mounted in order to minimize parasitics. The oscillators outputs are measured through the 20-GHz port using a PXA signal analyzer (Keysight N9030A). The phase noise is measured by means of a signal source analyzer (Agilent E5052B), which is connected through an ultra low SSB phase noise frequency divider-by-four (Analog Devices HMC447LC3). Fig. 4.7 shows the experimental setup. The VCO and DCO are tested and compared in open-loop in terms of power consumption, frequency tuning range (FTR) and phase noise. In addition, the VCO is included in a radar system built with discrete components: first, the VCO is tested in closed-loop with the external charge-pump PLL board only; then, its operation with the whole system is evaluated.

4.4.1 Open-loop Measurements

First, the oscillators are tested in open-loop. The DCO achieves an overall frequency tuning range from f_{min} = 18.4 GHz to f_{max} = 24.2 GHz (FTR = 27.2 %), while the VCO achieves an overall FTR from f_{max} = 19 GHz to f_{min} = 25.4 GHz (FTR = 29 %). The modified DCO shows a frequency tuning range slightly shifted to higher frequencies, namely from f_{max} = 18.7 GHz to f_{min} = 24.4 GHz (FTR = 26.5 %). The impact of devices inside of the inductor does not influence noticeably the f_{max} and the FTR. The VCO reaches a higher frequency due to lower capacitive load. The frequency range covered in the VCO and the DCO is shown in Fig. 5.19a while Table 4.4 reports the frequency resolution for each bank at both f_{max} and f_{min}. The frequency range covered with the coarse bank is shown in Fig. 4.8a and Fig. 4.8b for DCO and VCO respectively. Fig. 4.8c shows the tuning achieved with the varactors in the VCO with all

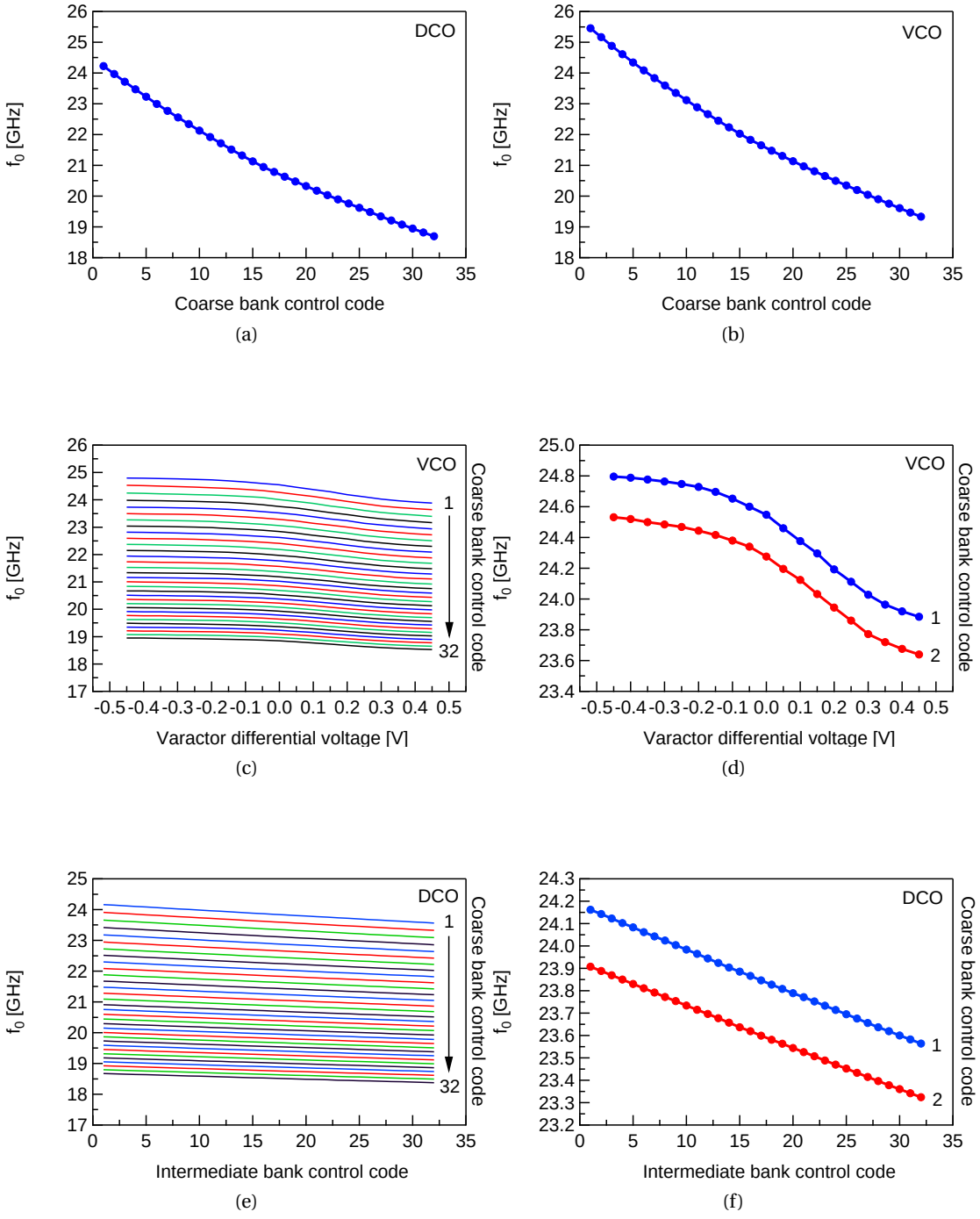


Figure 4.8: Measured VCO and DCO performance: FTR with coarse bank for a) DCO and b) VCO, varactor with c) all coarse bands and d) only 2 bands, intermediate bank with e) all coarse bands and f) only 2 bands, fine bank with g) all intermediate bands and h) only 2 bands, super fine bank with i) all fine bands and j) only 2 bands.

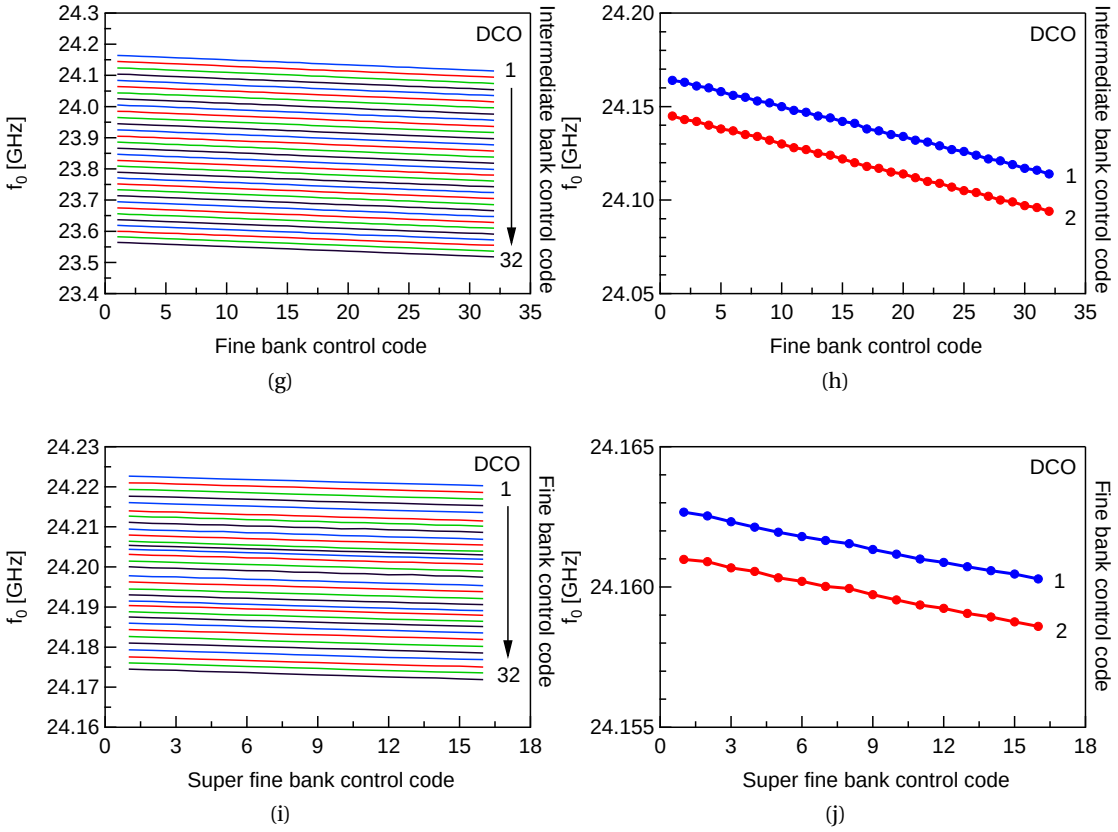


Figure 4.8: Measured VCO and DCO performance: FTR with coarse bank for a) DCO and b) VCO, varactor with c) all coarse bands and d) only 2 bands, intermediate bank with e) all coarse bands and f) only 2 bands, fine bank with g) all intermediate bands and h) only 2 bands, super fine bank with i) all fine bands and j) only 2 bands.

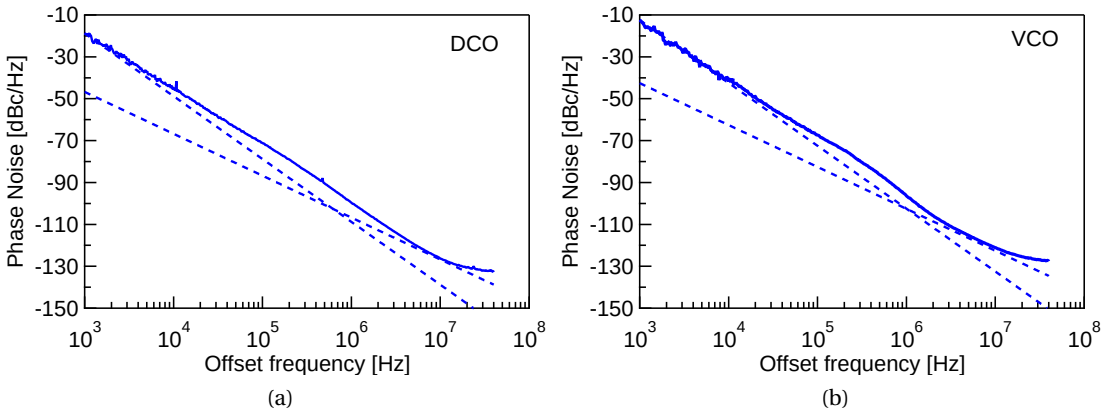


Figure 4.9: Measured a) DCO and b) VCO phase noise at 22 GHz and 1 MHz offset.

the coarse bands, while in Fig. 4.8d only the first two coarse bands are reported, which overlap by more than 50 %. In one coarse band the varactors cover from 910 MHz to 420 MHz from f_{max} to f_{min}; however, the linear portion of such characteristic covers only between 520 MHz and 240 MHz in the range from $V_{bias,diff} = 0$ to 0.3 V, where $V_{bias,diff} = V_{bias,p} - V_{bias,n}$. In this test $V_{bias,n}$ is kept constant at $V_{DD}/2$ and $V_{bias,p}$ is swept from 0 V to V_{DD}. This is the region where the K_{VCO} is constant, which goes from 1.9 GHz/V at f_{max} to 0.9 GHz/V at f_{min}. Fig. 4.8e shows the DCO frequency tuning versus the intermediate bank control code with all coarse bands while Fig. 4.8f in only 2 consecutive coarse bands. The DCO fine tuning is shown in Fig. 4.8g with all the intermediate bands and in Fig. 4.8h for only 2 consecutive intermediate bands. Finally, Fig. 4.8i shows the DCO frequency tuning versus the super fine bank control code for all fine bands while Fig. 4.8j for only 2 consecutive fine bands. For all the capacitor banks the overlap between consecutive bands is larger than 50 % as shown in the graphs. The modified DCO shows frequency steps similar to the standard DCO. For all DCO measurements, R_{1-2} and R_{1B-2B} are set to 15 Ω.

The current consumption P_{avg} and the phase noise $\mathscr{L}$ are compared at 22 GHz. When optimized for the best performance, the VCO consumes 2.7 mW while both the standard and the modified DCO consume 2.6 mW at V_{DD}= 0.9 V. The phase noise is measured after a division by 4 and then referred back to the output frequency of the oscillators (Fig. 4.9). At 1 MHz offset the phase noise is −96 dBc/Hz for the VCO ($V_{diff} = 0$ V), −99 dBc/Hz for the standard DCO and −98 dBc/Hz for the modified DCO. The f_{1/f^3} is around 500 kHz for the DCO and 1 MHz for the VCO. Moreover, the phase noise is measured also at the two extremes of the frequency tuning range. At 1 MHz offset and f_{max} the DCO phase noise is 0.2 dB higher than the one reported at 22 GHz. At f_{min}, the phase noise shows an increase of 6 dB at 1 MHz offset. This increase is due to the reduced overall Q when all the tuning elements are switched on. The same behavior is observed in the modified DCO. This result confirms that the placement of decoupling capacitors under the inductor does not have any detrimental effect on the DCO performance in this technology and it allows to reuse large areas across the chip normally not exploited.

The oscillators are measured also at reduced V_{DD} for low-voltage operation. At $V_{DD,min} = 0.65$ V, both the VCO and the standard DCO consume approximately 1.2 mW, while the phase noise at 1 MHz offset increases to −94 dBc/Hz for the former and to −97 dBc/Hz for the latter. Table 4.5 reports the performance of the VCO and the DCO at both V_{DD} and $V_{DD,min}$ and compares them to the state-of-the-art DCOs and VCOs around 20 GHz, including the traditional oscillator FoM and the FoM_T calculated at 22 GHz:

$$\mathrm{FoM} = \mathscr{L} - 20\log_{10}\left(\frac{f_0}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{avg}}{1\,\mathrm{mW}}\right) \tag{4.20}$$

$$\mathrm{FoM_T} = \mathrm{FoM} - 20\log_{10}\left(\frac{\mathrm{FTR}}{10}\right) \tag{4.21}$$

	This work		[8]	[18]	[19]	[20]	[21]	[22]
Osc. Type	VCO	DCO	VCO	DCO	VCO	DCO	VCO	DCO
Class	C	C	C	F23	F234	B	B	B
Tech (nm)	28	28	130	28	65	65	65	65
V_{DD} (V)	0.9 / 0.65	0.9 / 0.65	1	1	0.55	1	1	1
P_{avg} (mW)	2.7 / 1.2	2.6 / 1.2	4.1	13	6.6	10	18	4.8
f_{max} (GHz)	25.4	24	17.9	31.2	29.5	24.6	29.6	23.7
FTR (%)	29	27.2	17	14	16	17	7.3	24.4
PN[a] (dBc/Hz)	-96 / -94	-99 / -97	-109	-104	-108	-102	-106	-106.6
FoM[a] (dBc/Hz)	-179 / -182[b]	-182 / -184[b]	-188	-183	-189.6	-180	-182.3	-187.2
FoM_T^a (dBc/Hz)	188 / -191[b]	-191 / -193[b]	-192.5	-186	-193	-184	-179.6	-194.9
Area (mm^2)	0.023	0.026	N/A	0.15	0.083	0.08	0.15	0.046

[a] at $\Delta f = 1\,MHz$ [b] at $f_0 = 22\,GHz$

Table 4.5: Performance comparison of oscillators around 20 GHz

The presented designs in an ultra scaled node achieve the largest continuous frequency tuning range and the lowest power consumption with a state-of-the-art FoM_T. Both the FoM and the FoM_T benefit from the lower V_{DD}: the power consumption is by far the best among the oscillators found in the literature at this frequency and it compensates for the phase noise degradation. Note that in spite of the ultra low power consumption, both oscillators provide an output swing which is suited for driving the following blocks without a voltage buffer. Moreover, the continuous frequency tuning range is the largest reported as well and it brings additional benefits from the radar perspective. As far as the comparison between the VCO and the DCO is concerned, the main difference is the phase noise. The use of varactors with limited Q_{var} affects the performance at such frequencies more than the use of switched capacitors. This fact suggests to favor the latter as frequency tuning technique for the target application.

4.4.2 Closed-loop and Radar Measurements

Fig. 4.10 shows the radar system under test, composed of the chip and mm-wave discrete components. The PLL is composed of the VCO, the divider, the 10-GHz PA, the PLL evaluation board (EV-ADF4159EB1Z) and the active RC loop filter on the chip PCB. The PLL board includes the crystal oscillator (XO), the phase frequency detector (PFD) and the charge-pump (CP). A power divider is used to connect the 10-GHz output to both the PLL and the TX chain. The latter is composed of a switch that implements the OOK modulation, an active frequency multiplier-by-six and a directive antenna. As far as the RX chain is concerned, a LNA is placed

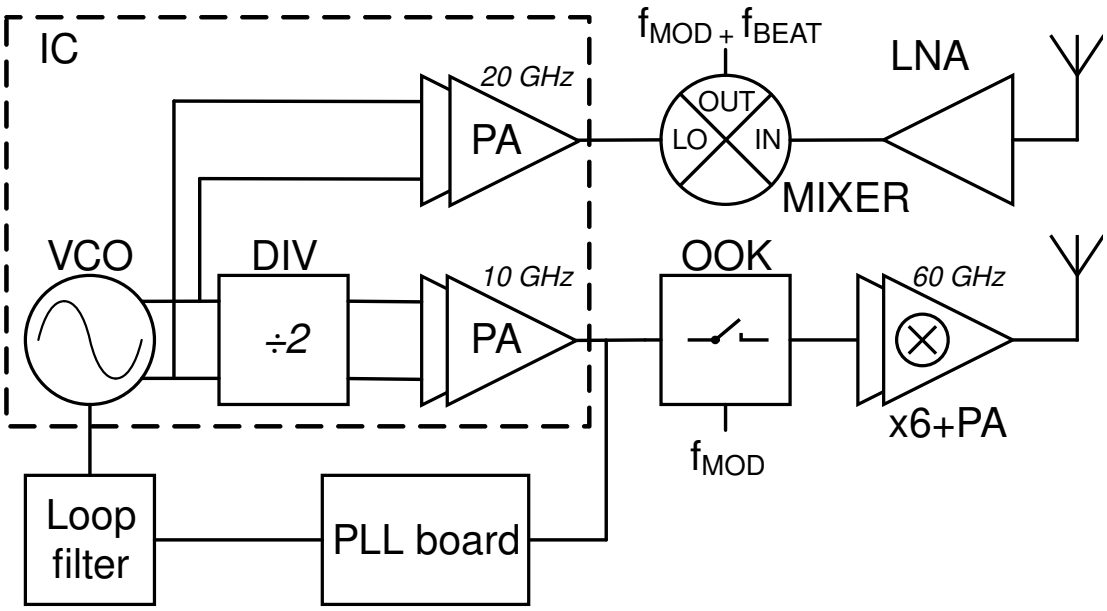


Figure 4.10: Radar system block diagram.

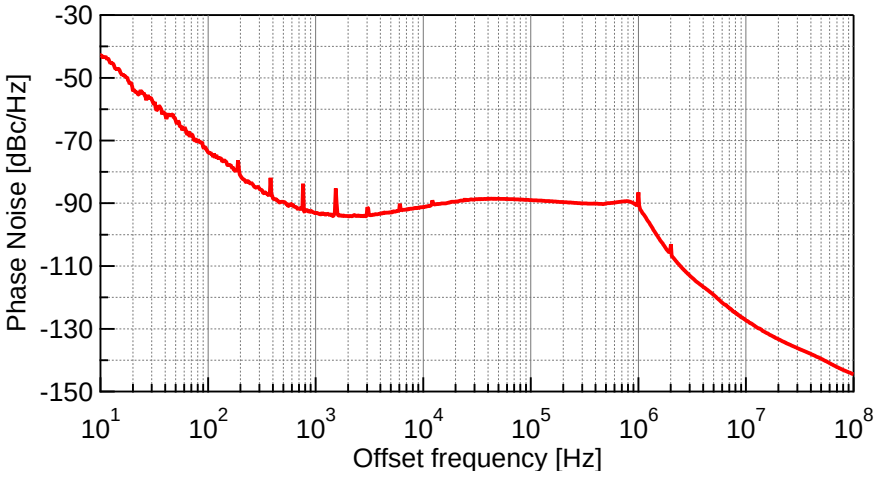


Figure 4.11: PLL phase noise at 20 GHz.

before the harmonic mixer that takes the 20-GHz output of the chip as LO signal to perform the down conversion. The OOK modulation is used to shift f_b to higher frequency: indeed, for the values of B, T_c and d achievable in this system, f_b needs to be frequency-shifted above the flicker noise corner frequency of the RX chain. Moreover, thanks to the fact that the same PLL is used to produce the transmitted signal and the LO and the traveled distance d_T is short, the phase noise of the mixed signals is still largely correlated and the residual phase noise in the output is much reduced [23].

The VCO is tested first in closed-loop with the PLL board. The loop filter is designed according

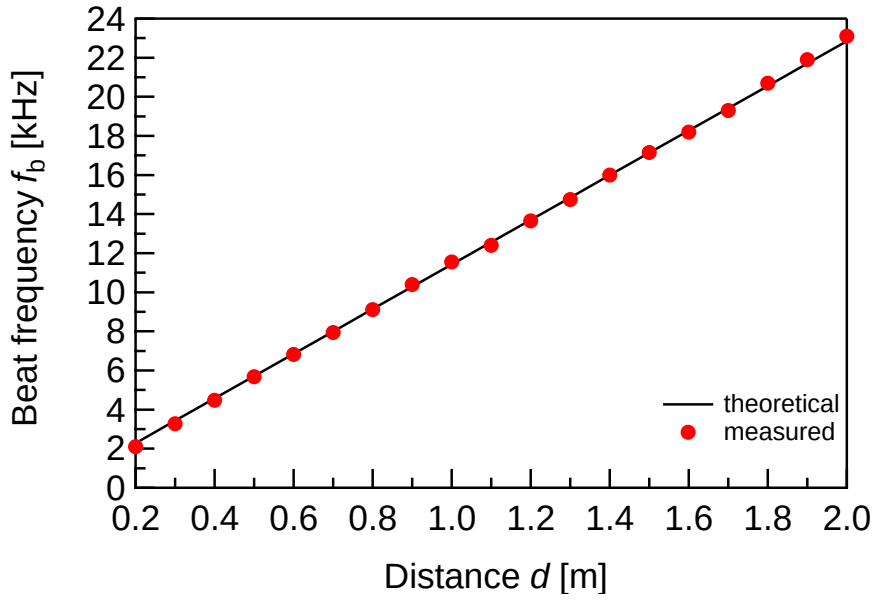


Figure 4.12: Measurement of beat frequency versus distance.

to the K_{VCO} to obtain 1 MHz PLL bandwidth f_{BW}. Fig. 4.11 shows the PLL PN at the output of the 20-GHz PA. The PLL is then configured to perform a triangular frequency sweep: the transmitted signal has an initial frequency of 57 GHz with $B = 860$ MHz and $T_c = 500\,\mu$s. With these parameters, the range discrimination δd is around 17.4 cm. The modulation frequency f_{mod} is set to 2 MHz. Fig. 4.12 shows f_b versus the distance d from the metallic plate target of 10 cm × 10 cm placed in front of the two antennas. The black line represents the theoretical f_b calculated with (4.4) while the red dots are the measured values. There is a very good match between the two curves, demonstrating that the performance of this oscillator is suited for this kind of applications. Fig. 4.13 reports the measured spectrum at two distances, i.e. 1 m (red trace) and 2 m (blue trace). The frequency is reported relative to f_{mod} while the amplitude is normalized to the peak value. The spectra show clearly a well-defined peak corresponding to f_b, which rises much above the other smaller peaks. The component at dc comes from the TX-to-RX leakage, while the peaks at higher frequencies represent the clutters, namely reflections from other stationary objects in the laboratory. Indeed, the test is not performed in an anechoic chamber to demonstrate the radar operation in a real case scenario containing several secondary reflectors.

4.5 Summary

In this chapter two oscillators targeting a low-power fully-integrated FMCW radar SoC are presented in 28-nm bulk CMOS technology. Contrary to most other implementations which focus only on the optimization of the FoM, here the goal is primarily to minimize the power consumption. The VCO and the DCO achieve by far the lowest consumption while maintaining

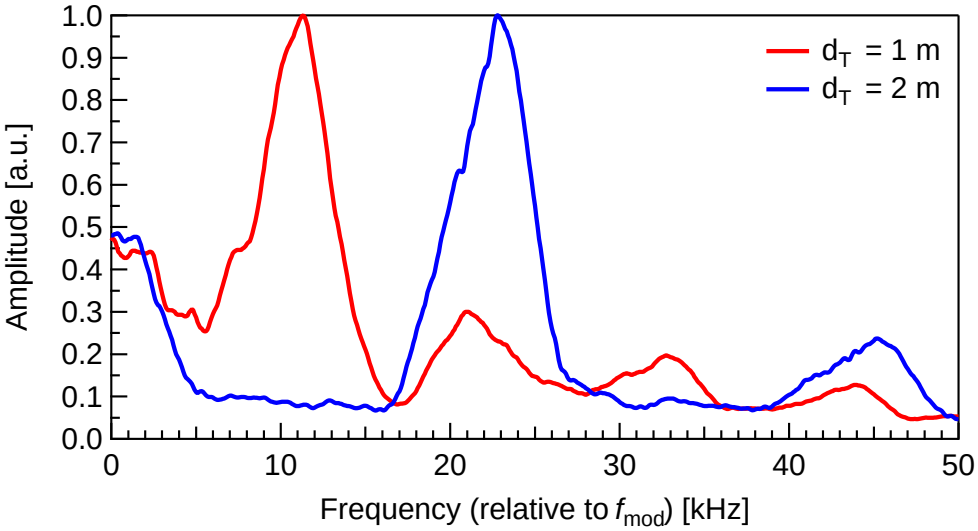


Figure 4.13: Spectra at 1 m (red trace) and 2 m distance (blue trace) from the target.

a comparable FoM, and satisfying all the given radar specifications. Indeed, they consume only 1.2 mW in low-voltage conditions with 29 % and 27.2 % frequency tuning range respectively. The DCO has around 150 kHz frequency resolution. They achieve - 191 and -193 FoM_T thanks to the record low power consumption. The use of decoupling capacitors as metal filling under the inductor does not affect the DCO performance and it allows to reuse large areas across the chip for low dropout regulators (LDOs) loads. Between the two oscillators, the DCO is more suited to operate at mm-wave frequency due to the better quality factor that switched capacitors can achieve compared to varactors.

The VCO is tested in closed-loop with a PLL board and afterwards in a 60 GHz radar system composed of discrete components. Distance measurements with a metallic plate in a real environment are carried out. A good match between the theoretical and the measured f_b is achieved, demonstrating that the oscillator design aiming for low-power operation is robust and suited for the requirements of such a low-power radar application.

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5 60-GHz Low-Power Wide-Tuning Range QDCO for a FMCW Radar SoC

As explained in the previous chapters, the short-range remote sensing is a very promising application for radar systems in the unlicensed V Band around 60 GHz. Indeed, the FMCW approach requires a large bandwidth to achieve a high range discrimination and the limited maximum permitted output power and high path loss still allow to detect targets at short distance. Moreover, the integration of such a radar SoC in IoT nodes demands low power consumption and an advanced CMOS technology for edge computing to limit the data to transmit.

Chapter 2 showed that the best choice for a low-power frequency synthesizer is to rely on a DCO thanks to the higher quality factor of switched capacitors compared to varactors at mm-wave frequencies. However, when considering how the PLL has to interface with the DCO for the FMCW modulation scheme, a critical aspect emerges. In fact, whatever is the method used to tune the resonator, i.e. TE based on switched capacitors, switched transmission lines, switched inductors or varactors, the best strategy to break the trade-off between number of TEs and frequency resolution is to split them in several banks with different sizes and types. This approach was proposed because typical modulation schemes in communication require bandwidths of few tens of megahertz at most in a given channel, allowing to devote a single bank for modulation and the rest of them for channel selection. This is not the case for FMCW radars, which require a continuous and linear frequency sweep across several gigahertz to achieve high range discrimination. The use of multiple banks is still viable but it requires extensive calibration to handle the transitions across overlapping sub-bands, for example by means of a look-up table (LUT) [1–3].

Another system-level aspect to keep in mind is how the heart rate, respiration rate or gesture are extracted from the reflected signal. The micro-Doppler effect is exploited, which allows to detect the mechanical vibration or rotation of the target or of any structure on it. Indeed, these micro-motions generate sidebands around the target's Doppler frequency shift produced by its radial velocity [4]. As a consequence, the target's feature can be recognized and classified by means of a receiver with an in-phase/quadrature (I/Q) demodulation. The I and Q LO signals are typically generated with a fundamental oscillator followed by poly-phase filter,

an oscillator at twice the frequency followed by a divider-by-two, a sub-harmonic injection-locked quadrature oscillator or a fundamental quadrature oscillator. The first method struggles to reach high frequency of operation due to limitations in reducing the value of passive components, the load posed by it to the oscillator and it is affected by the components mismatch. The second strategy is widely used to reduce the pulling effect of the PA over the oscillator but is not feasible at mm-wave since it would require a PLL working above 100 GHz with twice the frequency tuning range. The third method is very interesting because it is based on a sub-harmonic oscillator which is used to injection-lock two fundamental oscillators coupled in quadrature and hence it benefits from the PLL working at lower frequency. The forth approach is simple but still requires a PLL at high frequency and a large tuning range.

This chapter presents a 60-GHz QDCO with an alternative frequency tuning technique. Indeed, a property of quadrature oscillators can be used to achieve a very wide and seamless tuning range. Two oscillators coupled in quadrature are forced naturally to oscillate apart from the resonance frequency and this shift is proportional to the coupling strength. As a consequence, by acting on the coupling strength it is possible to tune the frequency. In the perspective of developing a complete ADPLL, a low-power divider chain is designed as well. The proposed approach simplifies greatly the design of the digital loop filter and it allows to achieve a seamless and ultra-wide FTR of 11 GHz maintaining a low power consumption and fulfilling the phase noise requirements for short-range radar applications. The chapter starts with an overview of the radar SoC in which the ADPLL would be integrated. Then, the working principle of an ADPLL is described and compared to its analog counterpart and the specific architecture chosen for this project is illustrated. After that, the tuning technique is explained and the design choices for the QDCO and the divider chain are reported. Finally the results of the chip characterization are shown and commented. Part of the material in this chapter is presented in [5, 6].

5.1 Description of the Radar SoC

Fig. 5.1 shows the block diagram of the system for which the QDCO and the divider chain presented in this chapter are designed. The QDCO generates two quadrature differential voltage carriers for the frequency band from 57 to 66 GHz. The oscillator's frequency is tuned with a 10-bit current-steering DAC as explained in Section 5.3.1. The two carriers (I and Q) drive two buffers each providing the input signal for the TX chains (I), the two LO signals for the RX chains (I and Q) and the input signal for the divider chain of the ADPLL (Q). The buffers help increasing the isolation from TX and RX, reducing the loading presented to the oscillators by the following blocks and having a load as symmetrical as possible to limit the I/Q mismatch. A fundamental aspect to develop a MIMO system is the possibility to increase the number of TX and RX chain at will. For this reason, the TRX is designed to be modular; two TX and two RX chains are integrated in this chip, but they are structured in such a way that more of them can be easily added. Indeed, a part from the first TX and RX chain which are co-designed with the QDCO, all the others can be simply copied in layout. Additional buffers are used to pick

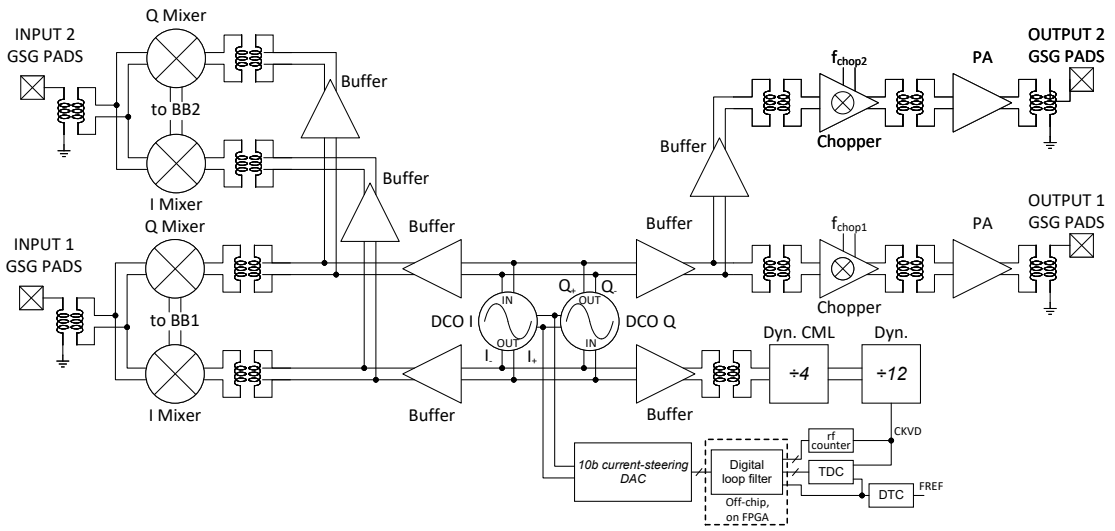


Figure 5.1: Block diagram of the radar transceiver.

the LO signals at the input of a chain and to distribute it to the next one compensating for the losses due to the long transmission lines.

The TX is composed of three stages: the buffer, the chopper and the PA [6]. The first two stage are coupled to the next one with transformers while the PA drives the GSG pad through an integrated balun. A small switched capacitor bank is placed at the output of each stage to tune the transformers and the balun to cover the whole FTR; the FMCW modulation occupies a very large bandwidth but it is instantaneously narrow-band and the frequency changes slowly. The role of the chopper is two-fold: on one side, as per the name, it shifts the f_{beat} by f_{chop} which would be buried in flicker noise when a slow chirp is employed; on the other side, by changing the value of f_{chop} among the different TX chains, it is possible to identify the origin of the received signal after demodulation in the MIMO scheme. As far as the RX is concerned, it is based on a mixer-first architecture: if a passive mixer is employed, the main advantage is the prevention of the saturation of the RX chain caused by a strong spillover from poor TX-to-RX isolation. After the mixer, the baseband signal is output by means of an open-drain buffer and amplified and converted off-chip.

Each block in the system is supplied through a dedicated LDO: this strategy offers the opportunity to distribute the regulators in the chip, to decouple supply voltages very close to the circuits and improve the isolation among them.

5.2 Principles of ADPLLs

The first ADPLL architecture was presented in [7, 8]. In spite of its name, such a system still contains at least one truly analog block, namely the DCO. However, it can be modeled as a normalized oscillator at an higher level of abstraction when considering the peripheral

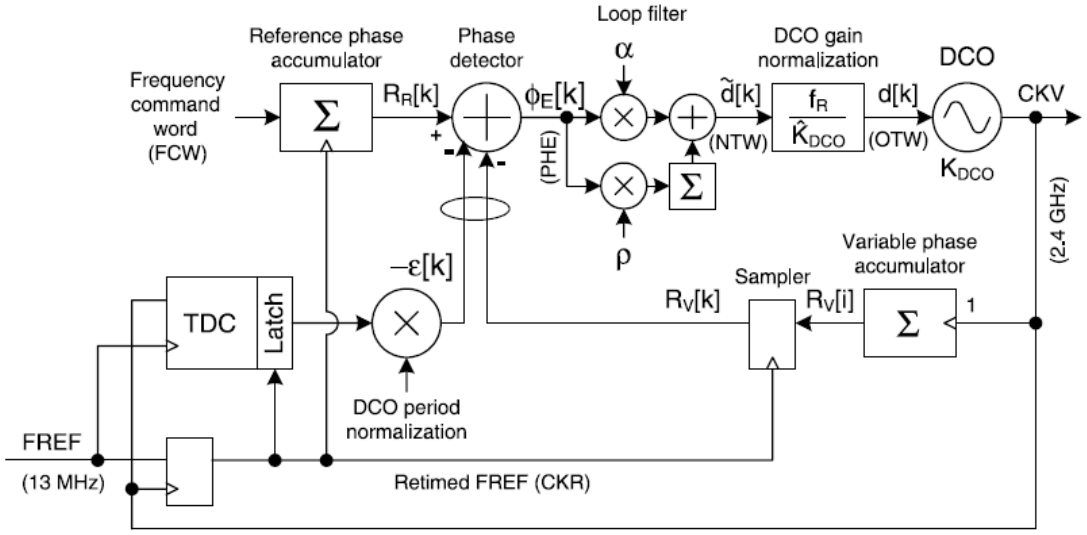


Figure 5.2: Block diagram of a typical type II ADPLL [8].

circuitry. These arithmetical functions track the variations of the oscillator gain K_{DCO} due to PVT and allow an accurate gain normalization. The high-level model sees a normalized tuning word (NTW) at the input and the resulting frequency deviation from the center frequency at the output.

The ADPLL architecture presents several advantages compared to its analog counterpart. First, it benefits fully from the deep-submicron technologies thanks to the digitally intensive approach, with ease of portability, less sensitivity to variability, smaller area, lower power and it can be easily integrated with the rest of the DSP in a SoC. Second, it has a very flexible dynamic behavior, which can be adapted depending on the operation phase: the locking procedure is split in several steps, starting in a broad frequency range with coarse steps for a PVT-calibration mode, moving to the acquisition mode in a medium range with smaller frequency steps and finishing with the tracking mode in a narrow frequency range using fine steps. Each mode is paired with a different loop bandwidth, going from a large to a narrow bandwidth, trading-off speed and phase noise performance.

5.2.1 The Original ADPLL Architecture

The ADPLL shown in Fig. 5.2 is a digitally synchronous fixed-point phase-domain architecture [8]. The output frequency f_V is set by the frequency command word (FCW), which is a fixed-point quantity representing the desired ratio f_V/f_R, where f_R is the frequency of the reference clock (FREF). The phase detection operation is linear and consists in the comparison between the reference-phase signal $R_R[k]$, whose value is set by the FCW, and the number of clock cycles of the DCO (CKV) in a reference clock period T_R. The former is obtained simply by accumulating FCW, while the latter is calculated by separating the integer and the fractional part. Indeed, the integer part represents the variable-phase signal $R_V[k]$ and it is the result of

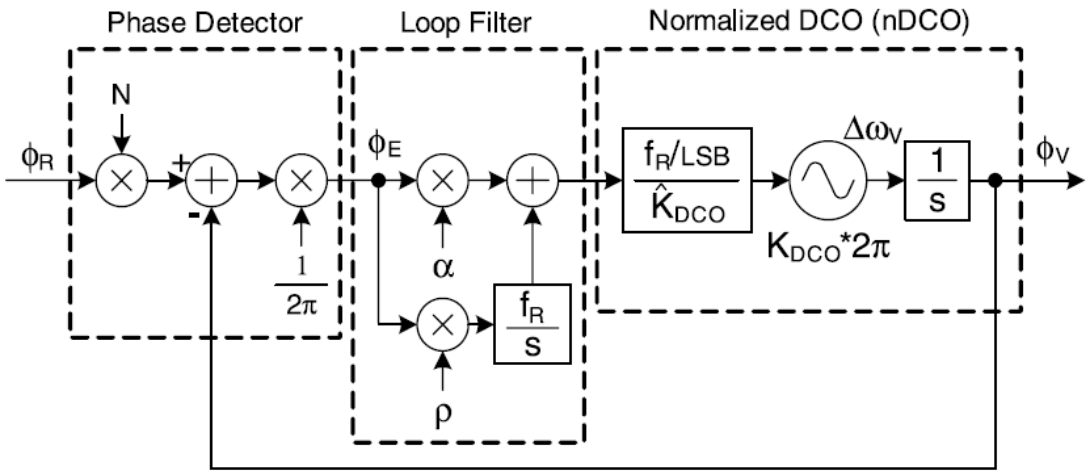


Figure 5.3: Linearized equivalent s-domain model of type II ADPLL [8].

the accumulation of a unit every DCO clock cycle and the sampling by the retimed FREF (CKR). The fractional part consists in the fractional correction $\epsilon[k]$ and is obtained by means of a time-to-digital converted (TDC), which tells how far the rising edge of CKV and FREF are. k is the index referring to a CKR transition. The whole system is synchronous to CKR, which is obtained with a crucial operation, namely the retiming of FREF with CLK. Before this step, there are two clock domains in the system, i.e. CKV and FREF, and it is difficult to operate on digital phase values at different instances without potential metastability issues. The comparison needs to happen in the same clock domain and this is achieved by oversampling FREF with CKV. After the phase detector, the phase error (PHE) samples $\phi_E[k]$ are processed by the digital loop filter, which is composed by a proportional path and an integral one with different gains, α and ρ respectively. These programmable parameters control the loop bandwidth and the presence of an integrator in the filter makes the ADPLL a type II. The advantages of a type II ADPLL over a type I are the superior noise filtering capability, the removal of the residual phase-error in the presence of a constant-frequency offset and the absence of steady-state frequency error when a frequency ramp is applied to the reference or the DCO [8]. The output of the loop filter is the NTW and it undergoes denormalization by multiplication with the factor $f_R/\hat{K}_{DCO}$ before being applied to the DCO itself. The correct estimation of the DCO gain in the parameter $\hat{K}_{DCO}$ allows to control precisely the loop bandwidth. During the fast acquisition step only the proportional path is active with a high α value: in this condition the loop is type I and the transient behavior is faster. Then, the type II operation is activated when the tracking mode is reached and a lower value for α is chosen. This operation is called "gear shifting" of the ADPLL gain.

Fig. 5.3 shows the linearized equivalent s-domain model of the type II ADPLL described above. Since the ADPLL is a discrete-time system, it should be described in the z-domain. However,

being $z = e^{(j\omega/f_R)}$, for $\omega \ll f_R$ z can be approximated as

$$z = e^{(j\omega/f_R)} \approx 1 + j\frac{\omega}{f_R} = 1 + \frac{s}{f_R} \tag{5.1}$$

which results in

$$s = f_R(z-1) \tag{5.2}$$

As a consequence, the s-domain model is used under the condition of fluctuation frequencies of interest much smaller than f_R and then the z-domain equivalent can be readily calculated.

The open-loop transfer function of the type II ADPLL is

$$H_{ol}(s) = \frac{1}{2\pi}\left(\alpha + \frac{\rho f_R}{s}\right)\frac{f_R}{\hat{K}_{DCO}}\frac{2\pi K_{DCO}}{s} = \left(\alpha + \frac{\rho f_R}{s}\right)\frac{f_R}{s}r \tag{5.3}$$

where $r = \frac{K_{DCO}}{\hat{K}_{DCO}}$ is equal to 0 if the DCO gain is estimated correctly. The closed-loop transfer function then is

$$H_{cl}(s) := \frac{\varphi_V}{\varphi_R} = N\frac{H_{ol}}{1+H_{ol}} = N\frac{(\alpha+\rho f_R/s)(f_R/s)r}{1+(\alpha+\rho f_R/s)(f_R/s)r} = Nr\frac{\alpha f_R s + \rho f_R^2}{s^2 + \alpha r f_R s + \rho r f_R^2} \tag{5.4}$$

If compared to the classical two-pole system transfer function, the natural frequency ω_n and the damping factor ζ can be obtained as

$$H_{cl}(s) = N\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{5.5}$$

$$\omega_n = \sqrt{\rho} f_R \tag{5.6}$$

$$\zeta = \frac{1}{2}\left(\frac{\alpha}{\sqrt{\rho}}\right) \tag{5.7}$$

5.2.2 Features for a Low-power ADPLL Architecture

In the traditional ADPLL the TDC has to cover an entire period of CKV and this requires a lot of delay stages if a fine resolution is needed. With the number of TDC elements the power consumption increases as well, since the block works at f_{CKV}. In [9, 10] an ADPLL architecture based on the use of both digital-to-time converted (DTC) and TDC is proposed. To break the trade-off between resolution and power, a DTC can be included to perform phase prediction: it can delay the FREF rising edge so to align it with the CKV one before it triggers the TDC. The resolution of the DTC can be coarser than the one of the TDC, which needs to detect only the residual phase error. In this way, the TDC need to use fewer elements with higher time resolution without incurring in excessive power consumption.

Moreover, to further reduce the power consumption of the ADPLL, a frequency prescaler can be inserted in the feedback loop [9, 10]. The divided CKV signal CKVD is sent to the phase

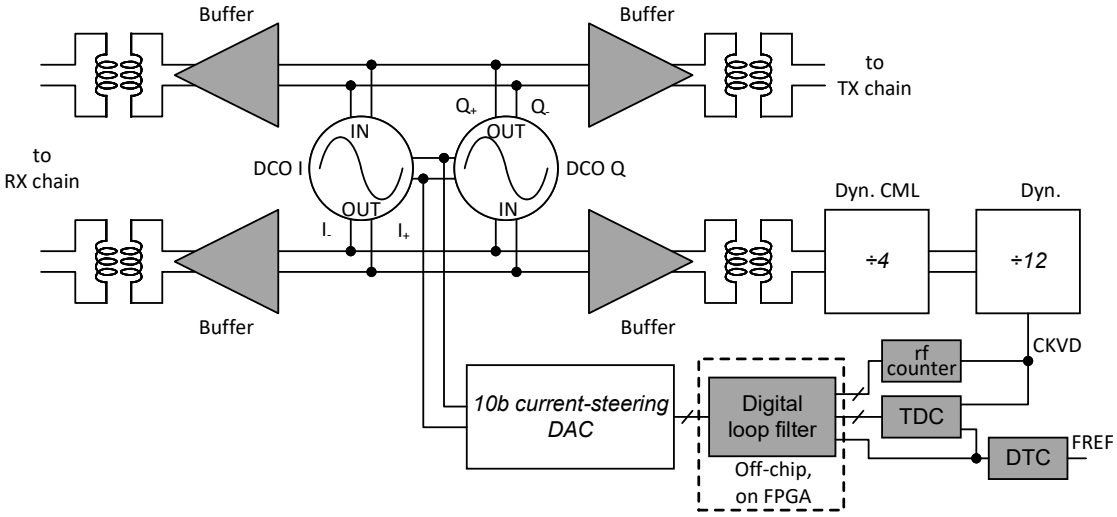


Figure 5.4: Zoom on the block diagram of the ADPLL: the blocks with gray background are not described in details in this thesis.

detector, which reduces its power consumption accordingly at the expense of the number of elements in the DTC.

5.3 Design of the ADPLL

Fig. 5.4 shows the main blocks of the designed ADPLL: this chapter focuses mainly on those with white background. After the QDCO generating the LO signal between 57 and 66 GHz, a frequency divider by 48 is used as prescaler to lower the output frequency to a range easily compatible with digital circuits built with standard cells. The divider chain is composed of a dynamic current-mode logic divider (DCMLD) by 4 and a dynamic divider (DD) by 12 and it brings the frequency down to 1.1875 to 1.375 GHz. After the frequency division, the signal CKVD is fed to the phase detector. A rf counter accumulates the CKVD cycles, which are then subtracted from the integer part of the FCW (FCW_{int}) to obtain the integer part of the phase error. The fractional phase is detected instead by a TDC clocked by an external reference frequency FREF which is re-timed by a DTC. The re-timed FREF is also delayed further and used in the rest of the digital circuits as clock. All the blocks mentioned above are full-custom designed, even though some are based on standard cells. Finally, the rest of the ADPLL loop, including the digital loop filter (DLF), are semi-custom designed. Each DCO core, the DCO bias, the TX buffer, the RX buffers, the divider buffer, the divider chain, the DTC and the TDC with the rf counter are supplied by dedicated LDOs to improve the rejection to supply noise and increase the isolation among them. At this stage of the full SoC development, the digital part of the ADPLL could not be integrated. For this reason, all the inputs and outputs of the blocks on chip are buffered and routed to I/O pads to be connected with a FPGA in the test setup. This solution offers flexibility since it allows to redesign at will the digital blocks implemented on FPGA. Nevertheless, considerable challenges are encountered as well in the

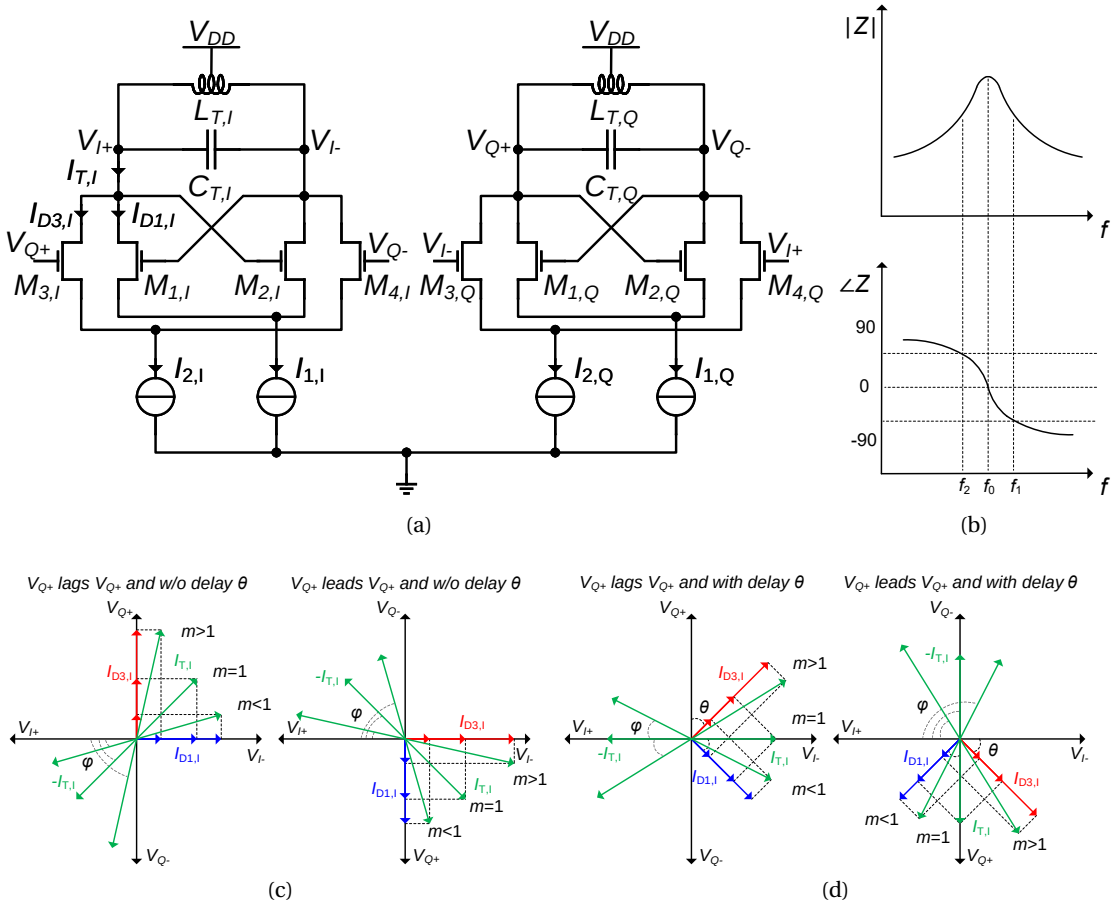


Figure 5.5: Seamless tuning technique: (a) schematic of a quadrature oscillator, (b) magnitude and phase of the impedance of the LC tank, (c) and (d) diagram with phasors of voltages and currents in the quadrature oscillator when V_{Q+} lags or leads V_{I+}, with and without the additional phase shift θ.

exchange of signals between the chip and the FPGA due to the loading provided by external level-shifters and the corruption of signals.

5.3.1 Seamless Tuning Technique in the QDCO

The seamless frequency tuning technique exploited in this oscillators is based on a fundamental property of oscillators coupled in quadrature. Fig. 5.5a shows the schematic of a quadrature oscillator. In the following, the I stage is taken as reference, but the same applies to the Q stage applying the same reasoning to its phasors. The devices and the currents in each stage are distinguished with the letters I and Q in the subscript of the symbols. When these letters are omitted, the symbol indicates both devices or currents.

A qualitative explanation of the working principle is reported in this Section while an analytical

description follows in the next one. When $I_{2,\mathrm{I}}$ is 0, there is no coupling and the stage oscillates freely. The drain current of $\mathrm{M}_{1,\mathrm{I}}$, $I_{\mathrm{D1,I}}$, is in phase with its gate voltage $V_{\mathrm{I-}}$ and it produces a drain voltage $V_{\mathrm{Q+}}$ in opposite phase when injected in the tank. Since $\mathrm{M}_{1,\mathrm{I}}$ and $\mathrm{M}_{2,\mathrm{I}}$ contribute both 180°, the total phase shift in the loop is already 360° and the oscillation condition is met at the resonance frequency f_0, where the tank contributes 0°, as shown in Fig. 5.5b [11]. The situation changes when $I_{2,\mathrm{I}}$ is larger than 0 and the two oscillator stages are coupled. As illustrated in Fig. 5.5c on the left, the drain current of M_3, $I_{\mathrm{D3,I}}$, is in phase with its gate voltage $V_{\mathrm{Q+}}$, as $I_{\mathrm{D1,I}}$ with $V_{\mathrm{I-}}$. The sum between $I_{\mathrm{D1,I}}$ and $I_{\mathrm{D3,I}}$ produces the tank current $I_{\mathrm{T}} = I_{\mathrm{D1,I}} + I_{\mathrm{D3,I}}$. Depending on the magnitude $I_{\mathrm{D1,I}}$ and $I_{\mathrm{D3,I}}$, the magnitude and phase of $I_{\mathrm{T,I}}$ changes. Nevertheless, the quadrature oscillation condition must be fulfilled and $V_{\mathrm{I+}}$ needs to be opposite phase with V_{I} and in quadrature phase with $V_{\mathrm{Q+}}$. Hence, the oscillation can only happen at a frequency at which the impedance of the tank contributes a phase shift that compensates the one between -$I_{\mathrm{T,I}}$ and $V_{\mathrm{I+}}$, namely φ. The result is that the oscillator does not operate any more at the f_0, further from the peak of the impedance. In principle, there are two possible solutions when two oscillators are coupled. In the case presented here, $V_{\mathrm{Q+}}$ lags $V_{\mathrm{I+}}$ and a negative phase shift is needed from the tank. Fig. 5.5b shows that such clockwise rotation is obtained at f_1, a frequency higher than f_0. However, if the $V_{\mathrm{Q+}}$ happens to lead $V_{\mathrm{I+}}$ (Fig. 5.5c on the right), in that case a positive phase shift is required from the tank and the appropriate counter-clockwise rotation is obtained at f_2, a frequency lower than f_0 [11]. If the tank is completely symmetrical, there is not theoretically a way to predict which solution prevails at each start-up of the circuit. This is a serious drawback of this type of coupling [12].

As stated above, since I_{T} has magnitude and phase that depend on the magnitude of I_{D1} and I_{D3}, by changing the latter it is possible to rotate continuously the former in the complex plane. The coupling strength is calculated as [11, 13]

$$m = \frac{G_{\mathrm{m3}}}{G_{\mathrm{m1}}} \tag{5.8}$$

where G_{m1} and G_{m3} are the gate transconductances of M_1 and M_3 respectively. m is related to $I_{\mathrm{D1,0}}$ and $I_{\mathrm{D3,0}}$ through G_{m1} and G_{m3} depending of the bias region of the transconductors. By increasing m, namely by increasing $I_{\mathrm{D3,0}}$ and/or decreasing $I_{\mathrm{D1,0}}$, the frequency is shifted further away from the natural frequency. If the the higher frequency between the two possible solutions of the quadrature coupling is selected, increasing m means increasing the frequency. This property of coupled oscillators can be effectively used to tune the operation frequency thereof [13, 14] with some caveats. The limit of this frequency tuning mechanism is imposed by specifications on the output amplitude and phase noise. Indeed, as departing from the resonance frequency, the impedance of the tank decreases and the quality factor as well. The overall quality factor can be approximated as [15]

$$Q_{\mathrm{T,tot}} \simeq 2Q_{\mathrm{T}} \cos\varphi \tag{5.9}$$

where Q_{T} is the quality factor of one tank and the factor 2 accounts for the two tanks in the system. The output amplitude decreases with a lower tank impedance and a lower I_1 while it

has a weaker dependence on I_2. The phase noise is degraded by a lower tank quality factor, lower amplitude and stronger coupling, since M_3 and M_4 inject noise during the zero crossings of the output waveform. As a consequence, the frequency tuning range is limited by these aspects.

Nevertheless, to alleviate the trade-off between the tuning range on one side and the amplitude and the phase noise on the other, a further phase shift can be introduced in the loop. Specifically, as shown in Fig. 5.5d on the left, if $I_{T,I}$ is delayed by θ, the angle φ with V_{I+} is reduced and the oscillation happens closer to f_0 and hence to the peak of the tank impedance, with all the advantages entailed. In order to rotate clockwise I_T by θ, I_{D1} and I_{D3} should be rotated by the same amount. This can be achieved by introducing a delay between the input voltage and the output current of M_1 and M_3. In particular, there is an optimum value for θ, namely $-45°$. As illustrated in Fig. 5.5c left, when $\theta = -45°$ -$I_{T,I}$ can be rotated symmetrically around V_{I+} and the impedance peak instead of only on one side of it benefiting from higher $Q_{T,tot}$ in a wider frequency tuning range. An additional benefit of the delay θ is that the second solution of the quadrature coupling is avoided by construction. In fact, as shown in Fig. 5.5d on the right, when V_{Q+} leads V_{I+}, the angle between -$I_{T,I}$ and V_{I+} is around 90°: such a phase shift can be produced by the tank where the impedance is extremely low, making oscillation almost impossible and surely its gain way lower. In this way, the problem of the oscillation ambiguity is solved. The delay θ can be obtained in several ways [14–16]. In this work, given the high operating frequency, two technique are combined: first, exploiting the intrinsic delay of transistors at high frequency [14]; second, using the parasitic inductance of the connection between the oscillator output and the gate voltage. The former technique is by far the larger contributor to the total phase shift: it is given by the transit time of charges in the channel, the parasitic gate resistance, inductance and capacitance and the drain-to-gate capacitance [14].

5.3.2 Small-signal Analysis of the QDCO

The behavior of the QDCO, which is described qualitatively in the previous Section, is here analyzed quantitatively by means of a small-signal model. The goal is to demonstrate the effect of the introduction of the phase shift θ on the current phasors, the oscillation frequency and the startup condition. Fig. 5.6 shows the linear model of a quadrature-coupled oscillator. G_m represents the transconductance of the cross-coupled pairs and G_{mc} the transconductance of the coupling pairs. The -1 factor takes into account the anti-phase coupling and θ is the fixed delay introduced between the input voltage and the output current of the transconductors. The equations that describe the system are

$$\begin{cases} V_I = (-V_Q G_{mc} e^{j\theta} + V_I G_m e^{j\theta}) Z(\omega), & \text{(5.10a)} \\ V_Q = (V_I G_{mc} e^{j\theta} + V_Q G_m e^{j\theta}) Z(\omega). & \text{(5.10b)} \end{cases}$$

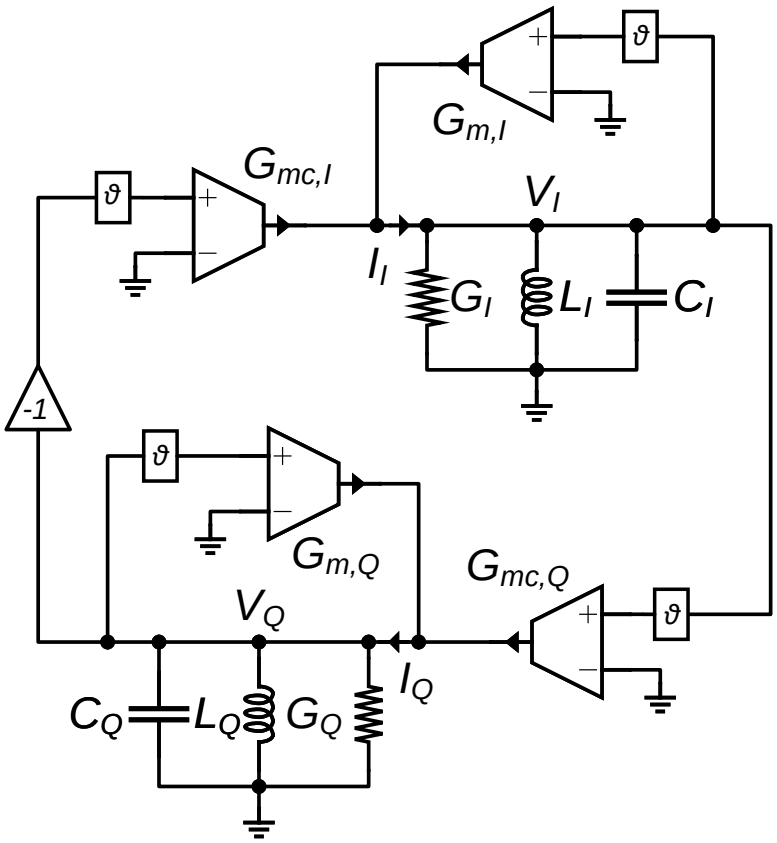


Figure 5.6: Seamless tuning technique: (a) schematic of one stage of a quadrature oscillator (b) diagram with phasors of voltages and currents in the quadrature oscillator and (c) magnitude and phase of the impedance of the LC tank.

Multiplying both sides of (5.10a) by $V_{\mathrm{I}} G_{\mathrm{mc}} e^{j\theta}$ and both sides of (5.10a) by $-V_{\mathrm{Q}} G_{\mathrm{mc}} e^{j\theta}$ and then subtracting the two resulting equations it is possible to obtain [11]

$$(V_{\mathrm{I}}^2 + V_{\mathrm{Q}}^2)(G_{\mathrm{m}} e^{j\theta} Z(\omega) - 1) = 0. \tag{5.11}$$

Since $G_{\mathrm{m}} Z(\omega) \neq 1$ at the oscillation frequency due to the presence of the coupling transconductor, the only solution is

$$V_{\mathrm{I}}^2 = -V_{\mathrm{Q}}^2 \quad \rightarrow \quad V_{\mathrm{I}} = \pm j V_{\mathrm{Q}}, \tag{5.12}$$

which proves that the V_{I} and V_{Q} are actually in quadrature as a sanity check for the model.

If only half of the circuit is analyzed, imposing $V_{\mathrm{Q}} = -j V_{\mathrm{I}}$ (V_{Q} lags V_{I}) it is possible to obtain easily the phase of the tank current, the startup condition, the oscillation frequency and the

tuning range. Starting from the tank current I_{I}, the following expression is found:

$$I_{\mathrm{I}} = (G_{\mathrm{m}} e^{j\theta} V_{\mathrm{I}} - G_{\mathrm{mc}} e^{j\theta} V_{\mathrm{Q}}) \tag{5.13}$$
$$= (G_{\mathrm{m}} e^{j\theta} + j G_{\mathrm{mc}} e^{j\theta}) V_{\mathrm{I}} \tag{5.14}$$
$$= (G_{\mathrm{m}}(\cos\theta + j\sin\theta) + j G_{\mathrm{mc}}(\cos\theta + j\sin\theta)) V_{\mathrm{I}} \tag{5.15}$$
$$= (G_{\mathrm{m}}\cos\theta - G_{\mathrm{mc}}\sin\theta) + j(G_{\mathrm{m}}\sin\theta + G_{\mathrm{mc}}\cos\theta)) V_{\mathrm{I}}. \tag{5.16}$$

The phase of I_{I}, φ, can be expressed as

$$\varphi = \angle I_{\mathrm{I}} = \arctan\left(\frac{G_{\mathrm{m}}\sin\theta + G_{\mathrm{mc}}\cos\theta}{G_{\mathrm{m}}\cos\theta - G_{\mathrm{mc}}\sin\theta}\right) = \arctan\left(-\frac{m\cos\theta + \sin\theta}{m\sin\theta - \cos\theta}\right). \tag{5.17}$$

When $\theta = -45°$, $\varphi = \arctan\left(\frac{m-1}{m+1}\right)$ and it simplifies as follows for 3 notable values of m:

- $m \approx 0$ ($G_{\mathrm{m}} \gg G_{\mathrm{mc}}$): $\varphi \approx -45°$;
- $m = 1$ ($G_{\mathrm{m}} = G_{\mathrm{mc}}$): $\varphi \approx 0°$;
- $m \gg 1$ ($G_{\mathrm{m}} \ll G_{\mathrm{mc}}$): $\varphi \approx 45°$.

Fig. 5.7a shows φ as a function of m for different values of θ and Fig. 5.7b shows (5.9) for $Q = 20$ using the φ obtained above [15].

Regarding the the startup condition, the oscillation frequency and the tuning range, they can be calculated as follows:

$$(G_{\mathrm{m}} e^{j\theta} V_{\mathrm{I}} - G_{\mathrm{mc}} e^{j\theta} V_{\mathrm{Q}}) Z(\omega) = V_{\mathrm{I}} \tag{5.18}$$
$$(G_{\mathrm{m}} e^{j\theta} + j G_{\mathrm{mc}} e^{j\theta}) Z(\omega) V_{\mathrm{I}} = V_{\mathrm{I}} \tag{5.19}$$
$$(G_{\mathrm{m}}(\cos\theta + j\sin\theta) + j G_{\mathrm{mc}}(\cos\theta + j\sin\theta) = Y(\omega) = G\left(1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right). \tag{5.20}$$

Eq. (5.20) can be decomposed into two expressions for the real and the imaginary parts on both sides:

$$\begin{cases} G_{\mathrm{m}}\cos\theta - G_{\mathrm{mc}}\sin\theta = G, & \text{(5.21a)} \\ G_{\mathrm{m}}\sin\theta + G_{\mathrm{mc}}\cos\theta = GQ\left(\dfrac{\omega}{\omega_0} - \dfrac{\omega_0}{\omega}\right). & \text{(5.21b)} \end{cases}$$

From (5.21a) the startup condition for the QDCO in the presence of a delay θ is obtained while

solving (5.21a) for ω leads to the oscillation frequency as a function of θ and m:

$$\omega^2 - \frac{G_\mathrm{m}\sin\theta + G_\mathrm{mc}\cos\theta}{GQ}\omega_0\omega - \omega_0^2 = 0 \tag{5.22}$$

$$\begin{aligned}
\omega_{1,3} &= \frac{G_\mathrm{m}\sin\theta + G_\mathrm{mc}\cos\theta}{2GQ}\omega_0 \pm \sqrt{\frac{(G_\mathrm{m}\sin\theta + G_\mathrm{mc}\cos\theta)^2}{4G^2Q^2}\omega_0^2 + \omega_0^2} \\
&= \frac{G_\mathrm{m}\sin\theta + G_\mathrm{mc}\cos\theta}{2GQ}\omega_0 \pm \omega_0\sqrt{\frac{(G_\mathrm{m}\sin\theta + G_\mathrm{mc}\cos\theta)^2}{4G^2Q^2} + 1} \\
&\simeq \omega_0\left(\frac{G_\mathrm{m}\sin\theta + G_\mathrm{mc}\cos\theta}{2GQ} \pm \left(1 + \frac{(G_\mathrm{m}\sin\theta + G_\mathrm{mc}\cos\theta)^2}{8G^2Q^2}\right)\right) \\
&\simeq \omega_0\left(\frac{G_\mathrm{m}}{2QG}(\sin\theta + m\cos\theta) \pm \left(1 + \frac{G_\mathrm{m}^2}{8Q^2G^2}(\sin\theta + m\cos\theta)^2\right)\right).
\end{aligned} \tag{5.23}$$

When $\theta = -45°$, the positive solution in (5.23) becomes

$$\omega_1 = \omega_0\left(\frac{G_\mathrm{m}}{2QG}(m-1) + \left(1 + \frac{G_\mathrm{m}^2}{8Q^2G^2}(m-1)^2\right)\right) \simeq \omega_0\left(1 + \frac{G_\mathrm{m}}{2QG}(m-1)\right). \tag{5.24}$$

Eq. (5.23) simplifies as follows for 3 notable values of m:

- $m \approx 0$ ($G_\mathrm{m} \gg G_\mathrm{mc}$): $\omega_1 \approx \omega_0\left(1 - \frac{G_\mathrm{m,max}}{2QG}\right)$;
- $m = 1$ ($G_\mathrm{m} = G_\mathrm{mc}$): $\omega_1 \approx \omega_0$;
- $m \gg 1$ ($G_\mathrm{m} \ll G_\mathrm{mc}$): $\omega_1 \approx \omega_0\left(1 + \frac{G_\mathrm{mc,max}}{2QG}\right)$.

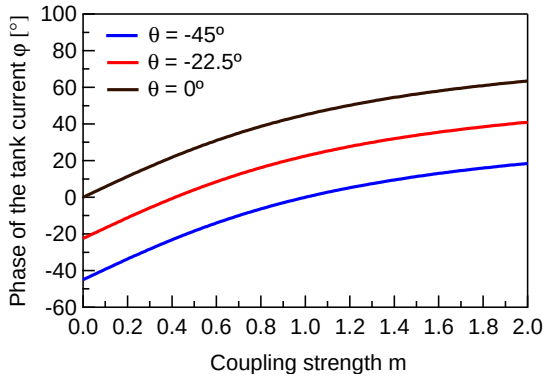
This result shows that the presented technique allows effectively to tune the oscillator around the resonance frequency with a total tuning range of $\Delta\omega_\mathrm{max} \approx \frac{G_\mathrm{mc,max}+G_\mathrm{m,max}}{GQ}$, where $G_\mathrm{mc,max}$ and $G_\mathrm{m,max}$ are the maximum values reached by G_mc and G_m respectively. Fig. 5.7c shows f_1 as a function of m for 3 different values of θ, with $f_0 = 2\pi\omega_0 = 61.5\,\mathrm{GHz}$, $G_\mathrm{m} = 5\,\mathrm{mS}$, $Q = 20$ and $G = 1.3\,\mathrm{mS}$. It is clear that, while at $\theta = 0°$ the frequency starts at the resonance, marked with the dashed line, and quickly reaches values at which the overall quality factor $Q_\mathrm{tot} = 2Q\cos\varphi$ is very low, for $\theta = -45°$ there is an optimum which allows to move around it benefiting of the better Q_tot.

If the solution $V_\mathrm{Q} = jV_\mathrm{I}$ (V_Q leads V_I) is imposed in (5.18), the following system of equations is obtained with the according positive frequency solution when $\theta = -45°$ are obtained :

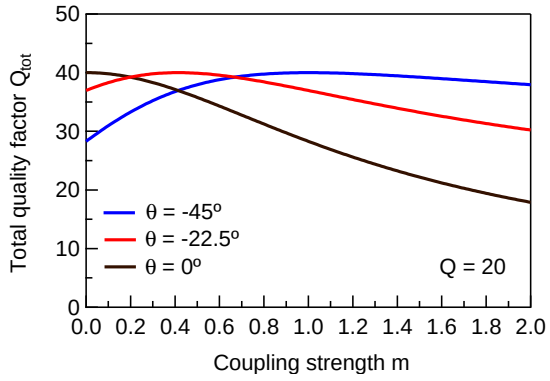
$$\begin{cases} G = G_\mathrm{m}\cos\theta + G_\mathrm{mc}\sin\theta, & \text{(5.25a)} \\ \omega^2 - \dfrac{G_\mathrm{m}\sin\theta - G_\mathrm{mc}\cos\theta}{GQ}\omega_0\omega - \omega_0^2 = 0, & \text{(5.25b)} \end{cases}$$

$$\omega_2 \simeq \omega_0\left(1 - \frac{G_\mathrm{m}}{2QG}(m+1)\right). \tag{5.26}$$

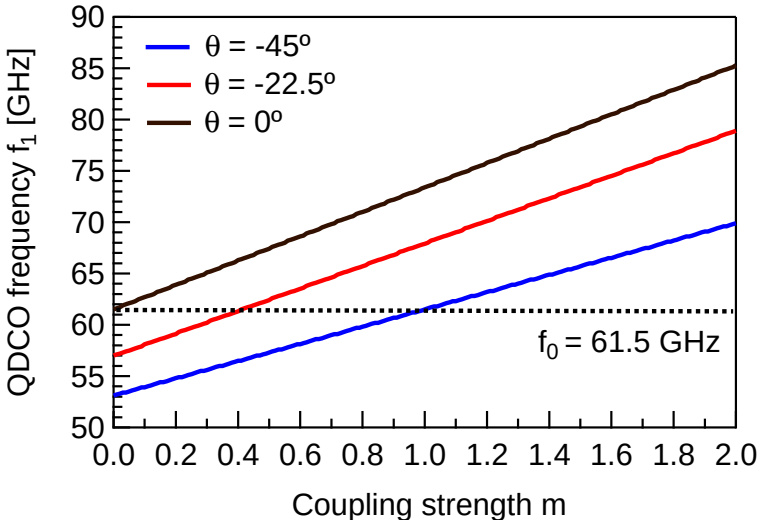
Eq. (5.23) simplifies as follows for 2 notable values of m:



(a)



(b)



(c)

Figure 5.7: QDCO linear model: a) Phase of the tank current and b) oscillation frequency as a function of the coupling strength m for different values of delay θ.

- $m \approx 0$ ($G_{\mathrm{m}} \gg G_{\mathrm{mc}}$): $\omega_1 \approx \omega_0 \left(1 - \frac{G_{\mathrm{m,max}}}{2QG}\right)$;
- $m \to 1$ ($G_{\mathrm{m}} = G_{\mathrm{mc}}$): startup condition is never met.

This result confirms that the quadrature solution leading to a frequency lower than the resonance frequency is strongly disadvantaged by the introduction of θ.

5.3.3 Design of the 60-GHz QDCO

The QDCO schematic is shown in Fig. 5.8. The oscillators cores are based on a current-biased class-B topology with a NMOS CC pair (M_1 and M_2) and a coupling pair (M_3 and M_4). The coupling is in parallel so that the pairs have independent biasing to be able to control the

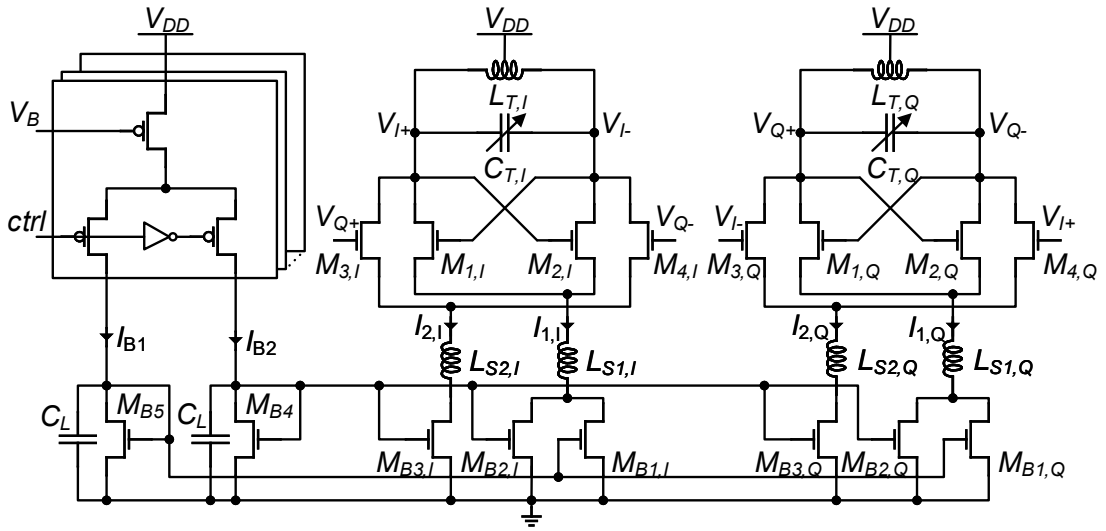


Figure 5.8: Schematic of the QDCO with the detailed biasing and tuning approach.

L_{1-4} (nm)	W_{1-4} (µm)	W_{f1-f4} (µm)	N° fingers M_{1-4}
20	30	1.5	20
$I_{D1-2,min}$ (mA)	$I_{D1-2,max}$ (mA)	$I_{D3-4,min}$ (mA)	$I_{D3-4,max}$ (mA)
1	1.5	0	4
L_T (pH)	Q_{LT}	L_1 (pH)	L_2 (pH)
100	23	80	130

Table 5.1: Design values in the QDCO.

coupling factor and hence the frequency. The intrinsic delay of the core transistors is studied versus the operation frequency and the bias point. Several strategies are applied to increase their delay. First, the MOSFETs are biased in MI: it represents once again the best trade-off between SI, where transconductance efficiency is low but the f_T is high, making the delay too short, and WI, where the efficiency and the delay are high but the load capacitance is too large to operate at mm-wave. Second, the gate resistance is increased by choosing wide finger widths. It can be increased as long as it does not affect too much amplitude and phase noise. On top of that, the interconnections between the outputs of the oscillators and the gate of the transistors is designed to be as symmetric as possible and to contribute additional phase shift thanks to their parasitic inductance. The optimal design values are obtained starting from these considerations and then optimizing through simulation iterations. Increasing I_2 and simultaneously decreasing I_1 is a good strategy to extend the tuning range compared to increasing only I_2. Moreover, it reduces the maximum and the average current consumption

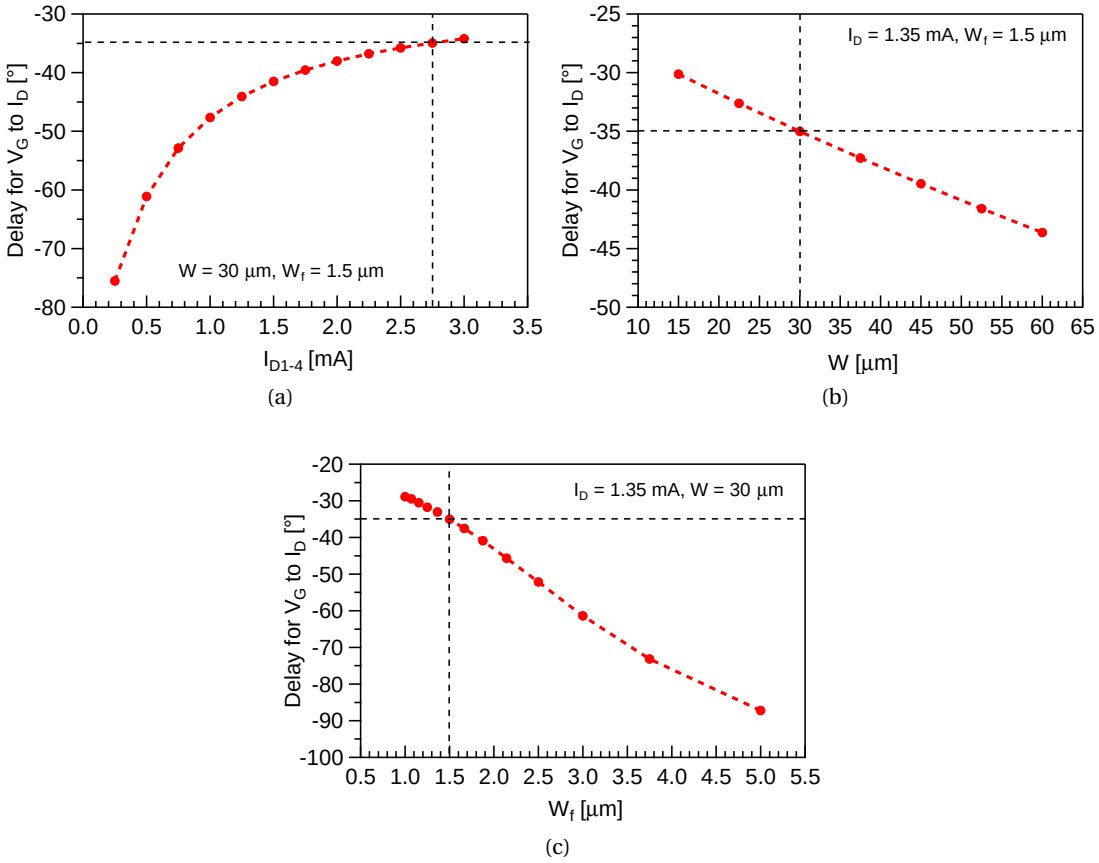


Figure 5.9: Analysis of delay between V_G and I_D in M_1 and M_3 versus (a) I_D at constant W and W_f, (b) W at constant I_D and W_f and (c) W at constant I_D and W.

compared to first increasing I_2 and then decreasing I_1 as done in [14] and it allows to save current using a current-steering DAC as shown afterwards. Nevertheless, the two currents cannot be reduced by the same amount since the output amplitude depends mostly on I_1. Hence, I_1 can only be reduced by a small amount while I_2 has to be increased up to a larger value impacting the current consumption. In addition, from this consideration it is deduced that the optimal θ is actually lower than $-45°$ to center the tuning range around the peak of the resonance to benefit from the best quality factor. Table 5.1 shows the design values that grant a phase shift around $-40°$ combining the two techniques. The delay is evaluated at $I_{D1} = I_{D3}$ for different drain currents, different total widths W with constant finger width W_f and different W_f with constant W, as shown in Fig. 5.9. The chosen design values are marked with dashed lines. Moreover, the parasitic inductance is extracted from the layout with an EM tool and it is around 15 pH.

Regarding the frequency tuning, as anticipated above, a current-steering DAC allows to change m acting simultaneously on I_{D1} and I_{D3}. Indeed, it allows to obtain a fast and smooth sweep without wasting part of the bias current into a dummy output or having to resort to current

branches with only one switch which limits strongly the switching speed. A 10-bit DAC is designed as a trade-off between the frequency resolution, the design complexity and required area. A higher number of bits necessarily demands an exponential increase of switching elements and long routing for the control bits. Indeed, the DAC is built as a huge current mirror with many outputs acting as current sources, for which the following expressions for thermal noise and flicker noise power spectral densities and output current mismatch hold:

$$S_{\mathrm{I_{out}},\mathrm{thermal}} = 4kT(B^2 G_{\mathrm{m1}} + G_{\mathrm{m2}}) + B^2 S_{\mathrm{I_{in}},\mathrm{thermal}} = 4kT(B+1)G_{\mathrm{m2}} + B^2 S_{\mathrm{I_{in}},\mathrm{thermal}}, \tag{5.27}$$

$$S_{\mathrm{I_{out}},\mathrm{flicker}} = G_{\mathrm{m2}}^2 \frac{4kT\rho}{f}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + B^2 S_{\mathrm{I_{in}},\mathrm{flicker}}, \tag{5.28}$$

$$\sigma_{\Delta \mathrm{I_{out}}} = \frac{1}{\sqrt{WL}}\sqrt{I_{\mathrm{out}}^2 A_\beta^2 + G_{\mathrm{m2}}^2 A_{\mathrm{V_{T0}}}^2} \simeq G_{\mathrm{m2}}^2 A_{\mathrm{Vto}} \sqrt{\frac{1}{2W_1 L_1} + \frac{1}{2W_2 L_2}}, \tag{5.29}$$

where B is the current multiplication factor of the mirror, the 1 and 2 subscripts refer to the input and the output transistor of the mirror, S_{Iin} is the noise power spectral density of the input current, A_β and $A_{\mathrm{V_{T0}}}$ are the mismatch parameters for the beta coefficient and the threshold voltage, ρ is the flicker noise parameter. First, a long channel increase the output impedance, leading to high precision. Second, the SI regime is desirable for low G_{m2} and hence low thermal noise from the transistors and low flicker noise and mismatch in the output current, requiring a small W/L ratio at a given current. Third, a large WL product grants a good matching and a low flicker noise from the transistors. As a consequence, the combination of low W/L and large WL leads to a large area for each unit current source. However, it has to be noted that there is a limit to the inversion level dictated by the available voltage headroom, which does not allow an excessively large saturation voltage. Moreover, a high B from the reference current to the output currents is not recommended to limit the amplification of the input noise. Conversely, the low-power operation is of great importance and the input current cannot be too large neither. A compromise is found with a reference current of 64 µA and a unit current of 1 µA. The reference current is generate on chip with a PTAT circuit. Another important aspect are the differential and the integral nonlinearity (DNL and INL respectively). The former is particularly important in this application because a poor performance may lead to a non-monotonous output current, a disruptive event for a closed-loop system such as the ADPLL. Since the DNL is dictated by the transition from the second-last bit to the most-significant bit (MSB), prohibitive sizes or more advanced topologies are required as the number of bits increases. A 10-bit DAC is already a quite tough design: the solution is the so-called segmentation, which consists in splitting the total number of bits in a binary-encoded part and a thermometer-encoded one. In this case the worst-case scenario for the DNL is relaxed by the lower number of binary-weighted current sources. The proportion between the two parts is set again by a trade-off between the DNL and an excessive number of control bits for the thermometer part. In this design, 6 bits for the binary part and 4 bits for the thermometer one are chosen. Each unit current source is designed with $L = 4\,\mu\mathrm{m}$ and $W = 2\,\mu\mathrm{m}$, while the switches have $L = 28\,\mathrm{nm}$ and $W = 500\,\mathrm{nm}$. The DNL is evaluated at schematic only due to the prohibitive size of the extracted netlist. After Montecarlo simulations with 200 runs at code

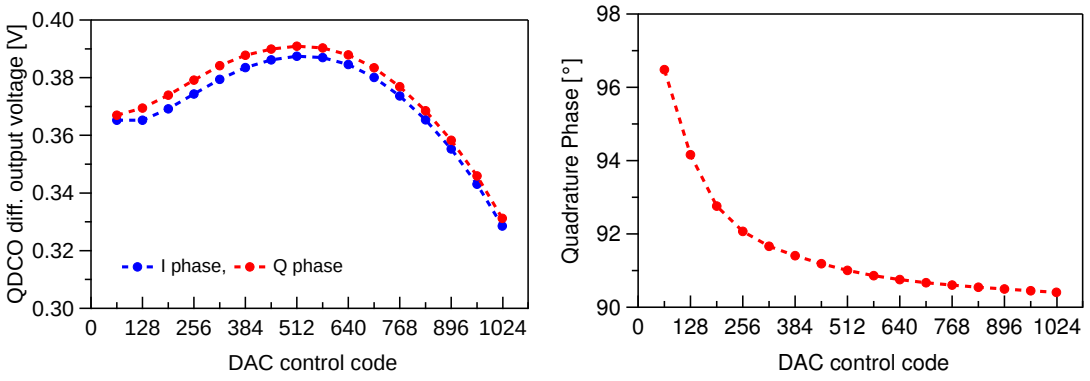


Figure 5.10: QDCO simulation results: (a) differential output voltage amplitude and (b) quadrature phase versus DAC input code.

63 and 64, the worst case for DNL due to the transition from the MSB-1 to the MSB of the binary-encoded part, the DNL is calculated evaluating the real current step versus the ideal one for each run and then computing the rms value. The result is DNL = 0.1 LSB when both process variations and mismatch are included. This value is much lower than the targeted 0.5 LSB and it gives a large margin to compensate for the worsening in DNL caused by the layout.

As explained above, the frequency tuning is controlled by choosing the minimum and maximum currents for M_1 and M_3, namely $I_{D1-2,min}$, $I_{D1-2,max}$, $I_{D3-4,min}$ and $I_{D3-4,max}$ shown in Table 5.1. The two output currents of the DAC I_{B1} and I_{B2} are mirrored with different coefficients to generate I_1 and I_2 and to optimize the width and linearity of the tuning range. I_{B2} is also injected in I_1 with a lower coefficient to sustain the oscillation amplitude and the phase noise. All the considerations made for the design of the current mirrors in the DAC are valid also for these ones. In addition, the B is implemented with a combination of series/parallel transistors. The advantages are a smaller occupied area: for example, if B is 16 and a 4 series and 4 parallel configuration is chosen, the total area is $8WL$ units versus $17WL$ of a 1 series and 16 parallel design. The higher equivalent WL on the input provides both a lower mismatch and a lower flicker noise contribution from this transistor, which is otherwise dominant due to the small size and the amplification. Even if the mismatch of a mirror is minimized in SI where the G_m is low and only the beta coefficient is left, still with limited V_{DD} such inversion levels cannot be achieved easily and the threshold coefficient is dominant. The capacitor $C_L = 9\,pF$ is added to slow down the transition between two current steps. In order to cover 9 GHz with the 10-bit DAC, the nominal frequency step Δf_{res} is of 10 MHz. The contribution of the frequency quantization of the QDCO to the total phase noise is given by [8]

$$\mathscr{L}_{DCO,quant} = \frac{1}{12}\left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \frac{1}{f_R}\left(\mathrm{sinc}\frac{\Delta f}{f_R}\right)^2. \tag{5.30}$$

For example, $\mathscr{L}_{DCO,quant} = -101\,dBc/Hz$ at $\Delta f = 1\,MHz$ and -121 dBcHz at 10 MHz offset. Eq.

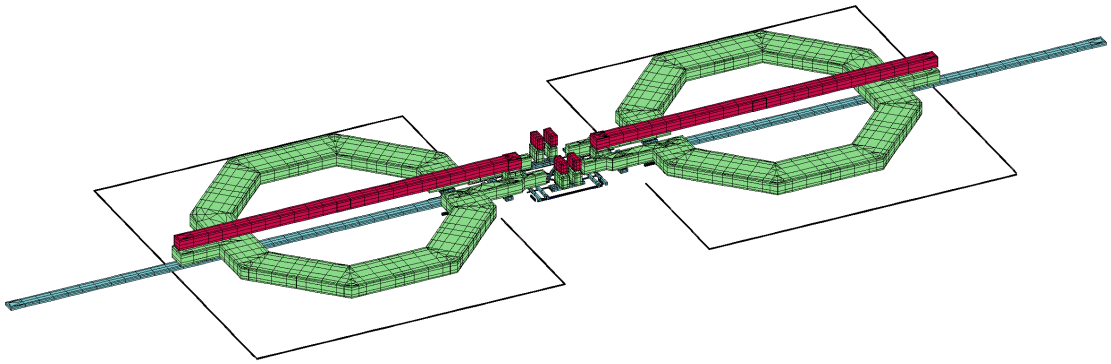
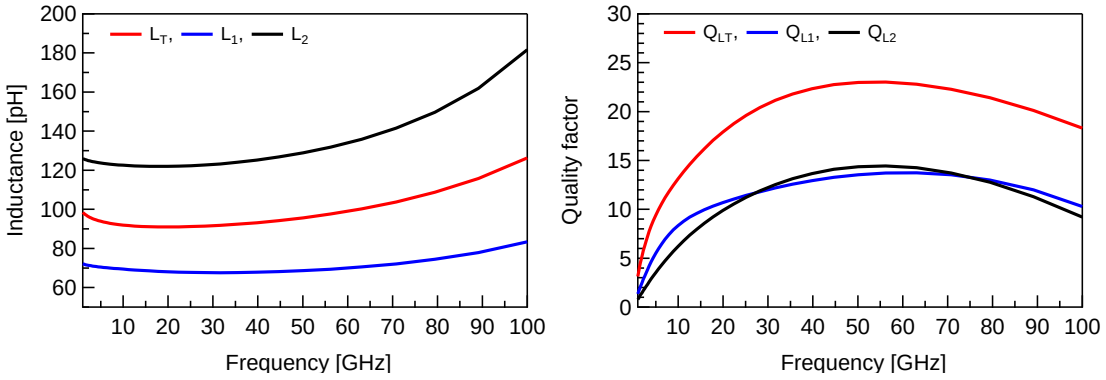


Figure 5.11: 3D view of the inductors in the QDCO.



(a) (b)

Figure 5.12: QDCO inductors: (a) inductance and (b) quality factor versus frequency.

(5.30) holds when Σ-Δ modulation is not applied. In this case it becomes

$$\mathscr{L}_{\mathrm{DCO,quant}} = \frac{1}{12}\left(\frac{\Delta f_{\mathrm{res,eq}}}{\Delta f}\right)^2 \frac{1}{f_{\mathrm{dth}}}\left(2\mathrm{sinc}\frac{\pi\Delta f}{f_{\mathrm{dth}}}\right)^{2n}, \tag{5.31}$$

where $\Delta f_{\mathrm{res,eq}} = \Delta f_{\mathrm{res}}/2^{W_{\mathrm{F,dth}}}$, $W_{\mathrm{F,dth}}$ is the number of fractional bits used for the dithering and n is the dithering order.

Fig. 5.10a reports the simulated differential I and Q output voltage amplitudes versus the DAC control code. A_{diff} varies between 320 and 390 mV along the tuning range. Fig. 5.10b reports the simulated quadrature phase along the coupling strength variation. The quadrature error remains always below 7°.

The design of the inductors in the QDCO follows the methodology described in Section 2.4. Given all the parasitic capacitance contributed by the wide core transistors, a 100 pH inductor is set as target. First, a synthesis tool is used to get a first estimate of an inductor around 80 pH, which is then refined by iterative simulations and EM extractions (the green inductors in Fig. 5.11). The second step is to include the metal connection from the inductor to the core

of the oscillator to the layout that has to be modeled with an EM tool. It is responsible for the last 20 pH needed. When working with a single turn inductor, every small extension has to be taken into account and it imposes even smaller devices. The third step is the inclusion of the routing of the output signal to the other core and to the two buffers. Since the two oscillators are aligned vertically, the buffers are placed horizontally, two on each side. Each couple of differential outputs have to turn by 90° and reach a buffer on the right and the other on the left. Their placement is critical, since any asymmetry may influence the tank inductance through coupling and also spoil the phase relation between the outputs. For the EM extraction, a differential port is placed at the level of each sub-block above-mentioned. Moreover, a small bank of 7 thermometer-coded switched capacitors is added to compensate for process variations and be able to cover the target frequency range. The simulated ΔC is around 2.5 fF. A pair of ports is added also for these, very close to the inductor.

Two inductors L_{S1} and L_{S2} are added in series with the tail current sources to increase the impedance around the oscillation frequency. This is beneficial to suppress the onset of a new oscillation mode as m increases. V_{I+} and V_{I-} would start to oscillate in-phase and V_{Q+} and V_{Q-} alike: hence, $M_{3,I}$ and $M_{4,I}$ would be in parallel and would form a new CC pair with $M_{3,Q}$ and $M_{4,Q}$. Provided that the output impedance of the tail current source of M_3 and M_4 is larger than the one of M_1 and M_2, this common mode oscillation does not prevail on the differential one. As a consequence, L_{S2} has to be larger than L_{S1}. The parasitic inductance of the interconnection is exploited to fit two more inductors in each core: they are routed one on top of the other on the vertical axis of L_T where the magnetic field is weaker (the red and the light blue lines in Fig. 5.11) [17]. This solution has an additional benefit: it allows to place decoupling capacitors very close to the center tap of L_T with a short common-mode return path. Thanks to the decoupling, this node becomes an ac ground and almost no rf current goes toward the current sources. This allows to layout all the current sources of the two cores together for matching and to place the block symmetrically with respect to both source nodes. Consequently, it is placed quite far from them, but with no impact on the rf behavior.

5.3.4 Design of the Divider Chain

The divider chain is composed of two different dividers, a DCMLD by 4 and a DD by 12, shown in Fig. 5.13 and Fig. 5.14 respectively. The first one consists in a standard CMLD where the CC pair is removed from the latches, which then become simple differential pairs [18, 19]. When the input transistor of a stage is off, the voltage at the outputs discharges slowly. A certain amount of output capacitance is needed to avoid excessive discharge in half of the input period. The capacitance contributed by the load and the parasitics are optimized for this scope. This inductor-less topology is compact and it allows to reach high working frequencies at a reduced power consumption. Moreover, this choice is driven by the interest for a wide-band divider that can follow the whole frequency tuning range of the QDCO without switching sub-bands. The input transformer is designed to be broadband, with a quite small loading capacitance allowed on the secondary winding. In order to reduce the loading, thanks to

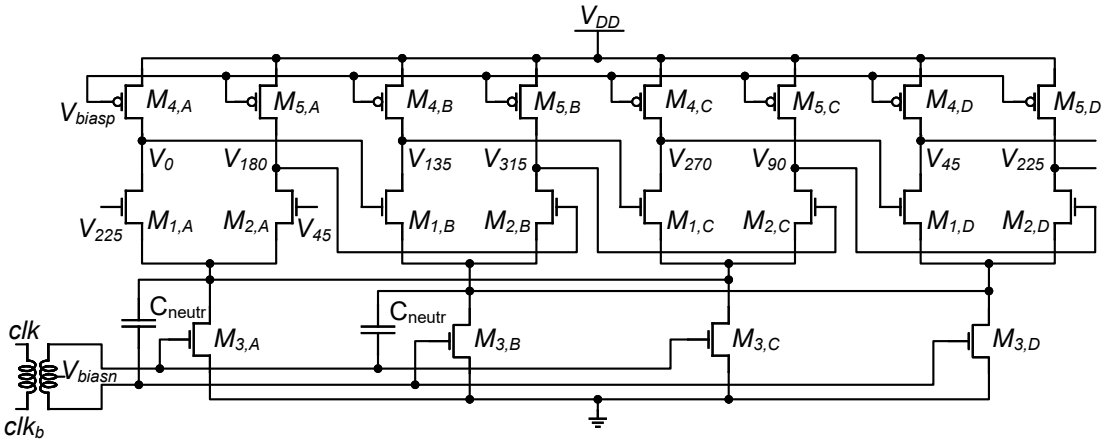


Figure 5.13: Schematic of the DCMLD by 4.

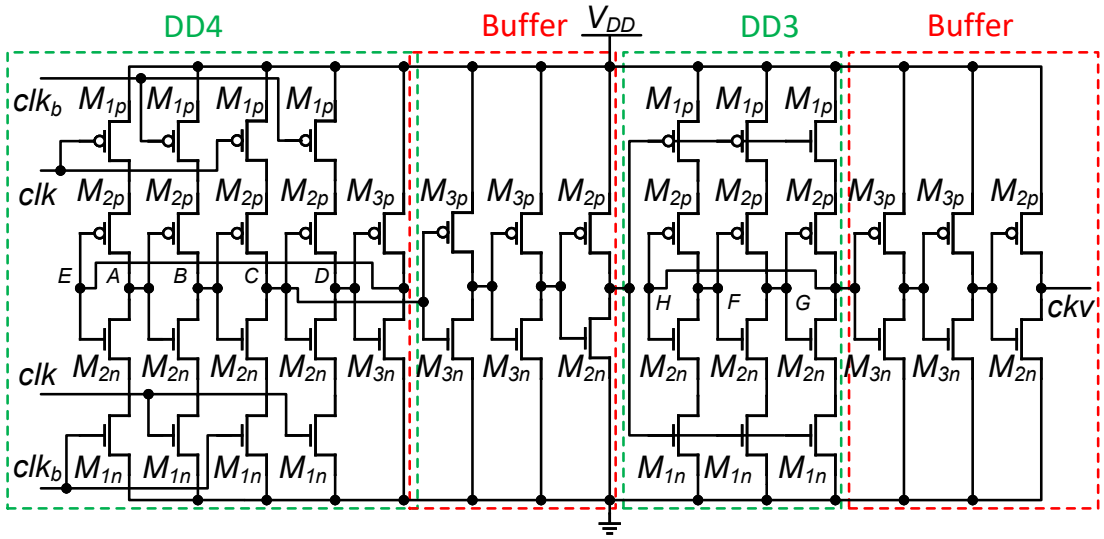


Figure 5.14: Schematic of the DD by 12.

the differential topology, two neutralization capacitors $C_{\text{neutr}} = 24\,\text{fF}$ are introduced: they minimize the impact of the drain-gate capacitance and improve the isolation from the rest of the circuit. The source node of the stages driven by the same clock phase are shorted [19]. In fact, when disconnected, these two nodes oscillate in opposite phase at twice the output frequency (or half the input one) because it is pulled up and down by the switching of the differential pair due to the limited output impedance of the short input transistor. As a consequence, the current injected is amplitude modulated and two consecutive cycles are uneven. The short presents a different path for this common-mode current, i.e. it is exchanged between the two differential pairs and the node swing is suppressed, avoiding the modulation of the injected current. V_{biasn} and V_{biasp} are controlled by means of two current DACs. However, in practice they cannot be controlled independently. When V_{biasp} increase, the R_{load} decreases to reach higher operating frequency. Then, V_{biasn} needs to increase as well

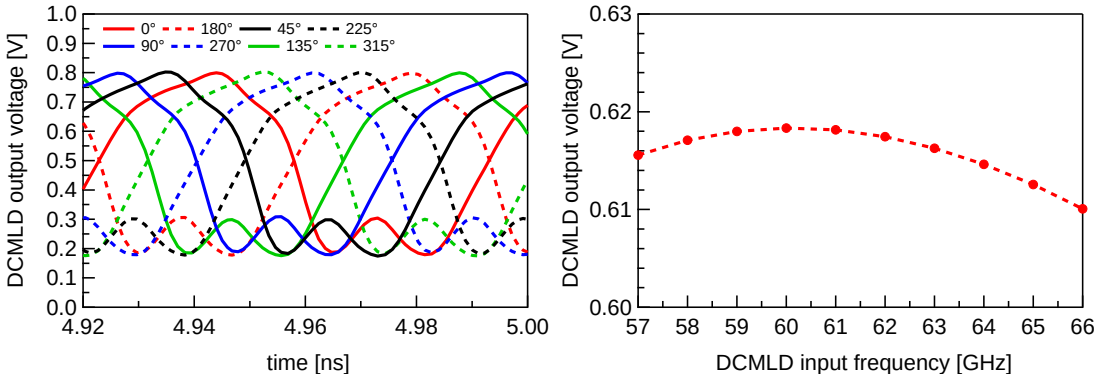


Figure 5.15: DCMLD by 4 simulation results: (a) output voltage waveforms and (b) differential output voltage amplitude versus DAC input code.

to sustain the loop gain and the output voltage swing and to get the right output common-mode voltage, since all of them depend on R_{load}. Fig. 5.15a reports the waveforms of the eight voltage outputs of the DCMLD and Fig. 5.15b their differential amplitude along the tuning range. It can be seen that the amplitude remains quite constant along the 9 GHz.

The DD by 12 is composed of a cascade of a DD by 4 and a DD by 3. They are built using dynamic logic and they are used in static configuration instead of the original multi-modulus application [20]. Typically the first stage in a cascade of such dividers is designed with a bias circuit for M_{1n} and M_{1p} since the input signal is not rail-to-rail. Nevertheless, the ac coupling and the bias circuit load excessively the DCMLD, which requires a small output capacitive load to work around 15 GHz. Since the DCMLD is able to provide a suitable input common-mode voltage and a large swing to the DD4, the bias circuit is removed and the two blocks are dc-coupled, occupying a very small area. Moreover, the common-mode voltage can be tuned by means of V_{biasn} and V_{biasp}. It has to be noted that in this DD by 4, not all output nodes have a duty cycle of 50 %. The node C is selected because it does. Another relevant aspect in the design of a DD is the parasitic capacitance at the drain of the current sources M_{1n} and M_{1p}. It has to be much smaller than the capacitance at the output of each slice to avoid excessive discharge of the output during the latch phase through charge redistribution [20]. Nevertheless, the great advantage of the DD topology is to scale very well with technology. For the chosen advanced technology node, the minimum gate length reduces, as well as the parasitic capacitance and the supply voltage. These factors lead to higher operating frequency, compact size and very low power consumption, which increases with frequency but also benefits from lower supply voltage and load capacitance. Thanks to the selected advanced technology, it is demonstrated for the first time to work around 15 GHz. For symmetry purpose each differential outputs of the DCMLD is loaded with a DD. Only one is connected to the TDC providing the variable clock signal CKV, while the others are dummies. Table 5.2 shows the design values for the DCMLD and the DDs.

$L_{1-5,\mathrm{A-D}}$ (nm)	$W_{3,\mathrm{A-D}}$ (µm)	$W_{1-2,\mathrm{A-D}}$ (µm)	$W_{4-5,\mathrm{A-D}}$ (µm)
20	16	8	8
$L_{1,\mathrm{n-p}}$ (nm)	$L_{2,\mathrm{n-p}}$ (nm)	$W_{1,\mathrm{n}}$ (µm)	$W_{1,\mathrm{p}}$ (µm)
32	20	500	640
$W_{2,\mathrm{n}}$ (µm)	$W_{2,\mathrm{p}}$ (µm)	$W_{3,\mathrm{n}}$ (µm)	$W_{3,\mathrm{p}}$ (µm)
400	480	200	240

Table 5.2: Design values in the DCMLD and the DD.

5.3.5 Description of DTC and TDC

The DTC is designed to cover the largest CKV period with a 20 ps resolution with some margin, while the TDC covers 25 % of it with 10 ps resolution. The expected phase noise from the TDC quantization is [8]

$$\mathscr{L}_{\mathrm{TDC}} = \frac{4\pi^2}{12}\left(\frac{t_{\mathrm{res}}}{N_{\mathrm{d}}\,T_{\mathrm{DCO}}}\right)^2 \frac{1}{f_{\mathrm{R}}} \simeq -108\,\mathrm{dBc/Hz}. \tag{5.32}$$

The output of the TDC is converted to binary and then sent to general-purpose input/outputs (GPIOs). In order to close the loop with a field-programmable gate array (FPGA), the output of the rf counter and the re-timed FREF are output as well.

5.3.6 Implementation of the Loop Filter and the Modulator with an FPGA

The rest of the ADPLL is synthesized on a FPGA and connected to the chip through GPIOs. The reference frequency of 48 MHz is provided by an external crystal oscillator. A gear-shifting scheme is implemented to have a fast coarse frequency search at first with a type-I loop and a proportional filter and to switch then to a type-II loop with a third-order filter for locking and modulation. When locking is achieved, the open-loop and closed-loop z-domain transfer functions are Fig. 5.3

$$H_{\mathrm{ol}}(z) = \frac{1}{2\pi} H_{\mathrm{filt}}(z)\, f_{\mathrm{r}}\, r \frac{2\pi}{(z-1) f_{\mathrm{r}}} z^{-n} = r \frac{H_{\mathrm{filt}}(z)}{z^n (z-1)}, \tag{5.33}$$

$$H_{\mathrm{cl}}(z) = N_{\mathrm{R}} \frac{H_{\mathrm{ol}}(z)}{1 + \frac{H_{\mathrm{ol}}(z)}{N_{\mathrm{D}}}} = N_{\mathrm{R}} N_{\mathrm{D}}\, r \frac{H_{\mathrm{filt}}(z)}{H_{\mathrm{filt}}(z)\, r + N_{\mathrm{D}} z^n (z-1)}. \tag{5.34}$$

where N_{R} is equivalent to FCW, N_{D} is the division ratio, $H_{\mathrm{filt}}(z)$ is the z transfer function of the loop filter and $n = 3$ is the number of additional delays in the digital domain. N_{R} and N_{D} are related by

$$f_{\mathrm{r}} N_{\mathrm{R}} = \frac{f_{\mathrm{V}}}{N_{\mathrm{D}}} \tag{5.35}$$

The transfer function $H_{\text{filt}}(z)$ is equal to

$$H_{\text{filt}}(z) = k_1 \frac{z-1+k_2k_3}{(z-1)(z-1+k_2)} \tag{5.36}$$

where k_1, k_2 and k_3 are three filter coefficients set with registers programmed with an SPI. The approximated closed-loop s-domain transfer function is then

$$H_{\text{cl}}(s) = k_1 N_{\text{R}} N_{\text{D}} r f_{\text{R}}^5 \frac{s+k_2k_3f_{\text{R}}}{N_{\text{D}}s^2(s+f_{\text{R}})^3(s+k_2f_{\text{R}}) + k_1 r f_{\text{R}}^5(s+k_2k_3f_{\text{R}})} \tag{5.37}$$

using the equivalence in (5.2). The transition between the locking phases is controlled with a finite state machine (FSM) and their duration is programmed with a register. The output of the filter in each phase is weighted differently when generating the DAC control word to get different DCO gains. Since the targeted chirp time T_{c} and the PLL bandwidth f_{PLL} are between 1 and 10 ms and 0.1 and 1 MHz respectively, there is not need of two-point modulation in principle and hence the modulation is applied only in band at the FCW level. This simplifies greatly the related circuitry, since the high-pass modulation path applied at the DCO level requires a precise estimation of the K_{DCO}, while in this case an inaccurate estimation leads only to a wrong loop gain prediction. As shown in [21, 22], when in-band modulation is applied, the f_{PLL} should be much larger than the inverse of T_{c} to avoid a delayed and distorted chirp, but also smaller than the frequency resolution, to avoid generating a stair-like chirp. Remaining inside these boundaries allows to interpolare linearly between two frequencies when FCW is updated. A counter with a programmable clock derived by f_{R} generates the ascending and descending ramps.

5.4 Experimental Results

The chip shown in Fig. 5.16 is mounted on a printed circuit board (PCB) and connected to it with bond wires for supplies and digital signals. The signal is on-chip probed on ground-signal-ground (GSG) pads at the output of the TX chain. The output of the divider chain is further divided by 32 in the digital domain and output on a GPIO. Fig. 5.17 shows the experimental setup to measure the rf signal. The frequency of the oscillator output is measured using a PXA signal analyzer (Keysight N9030A with harmonic mixer M1970V), while the phase noise is measured by means of a signal source analyzer (Agilent E5052B) after down-conversion, amplification and frequency division using a passive mixer (Pasternack PE15D1002), a low-noise amplifier (MC ZX60-24-S+) and two ultra low SSB phase noise frequency divider-by-four (Analog Devices HMC447LC3 and HMC365). The passive mixer LO port is driven by a 75 GHz carrier generated by the up-conversion of a 12.5 GHz signal (HP 83620B and R&S ZVA-Z75). Finally the frequency chirp is measured with a high frequency oscilloscope (Teledyne LeCroy SDA 813Zi-B).

First, the QDCO frequency and power consumption versus DAC control code are measured. Fig. 5.18 shows the spectrum at 61.615 GHz and Fig. 5.19a shows the whole FTR with the 8

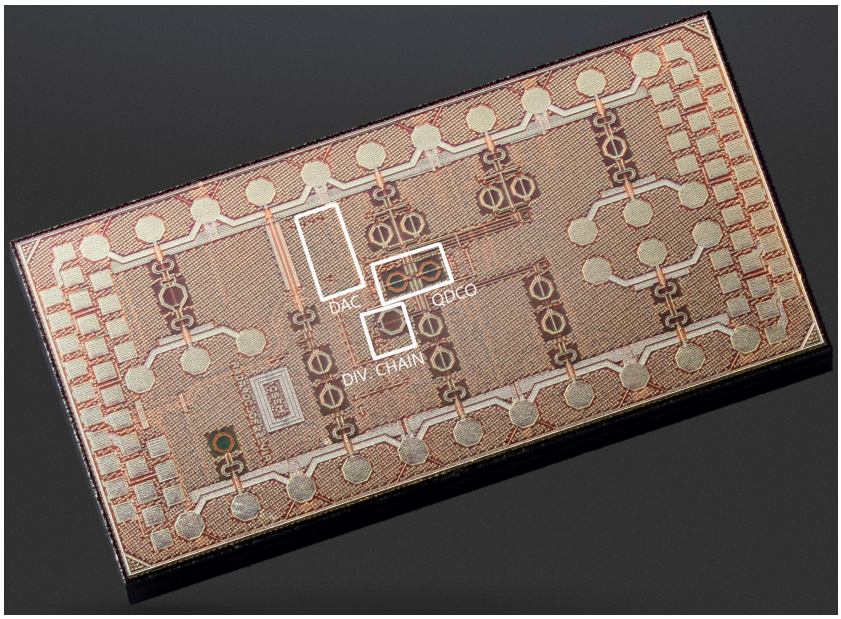


Figure 5.16: Chip micrograph (2.5 mm x 1.25 mm): QDCO, DAC and divider chain occupy around 0.083 mm^2.

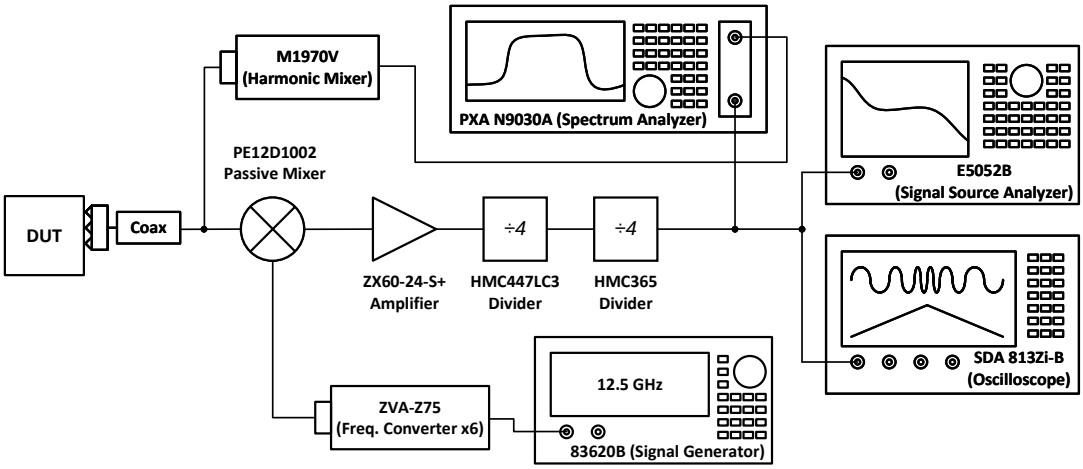


Figure 5.17: Experimental setup used to measure the rf output of the radar chip.

sub-bands controlled by the bank of capacitors. Each sub-band extends over between 10.7 and 12 GHz, while the total FTR covers 16.7 GHz (26 %) from 54.8 to 71.5 GHz. The frequency step is between 10 and 15 MHz. Fig. 5.19b shows the current consumption of the QDCO, which ranges from 6.3 to 18.3 mA across one sub-band, with an average of 13 mA considering a linear frequency sweep during the ADPLL modulation. Then, the phase noise at 61.615 GHz in the 6^{th} band is shown in Fig. 5.20a: it reports −78 dBc/Hz and −103 dBc/Hz at 1 MHz and 10 MHz offset respectively. The measured phase noise at these offset frequencies over one sub-band is shown in Fig. 5.20b. It has to be noted that the more advanced the technology node is,

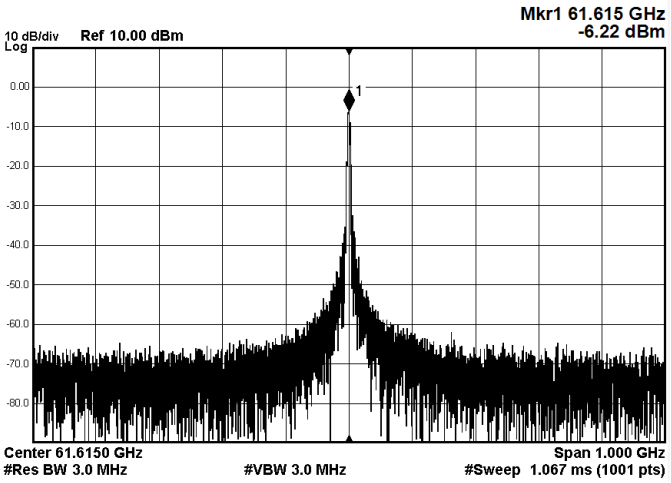


Figure 5.18: QDCO spectrum at $f = 61.615\,\text{GHz}$.

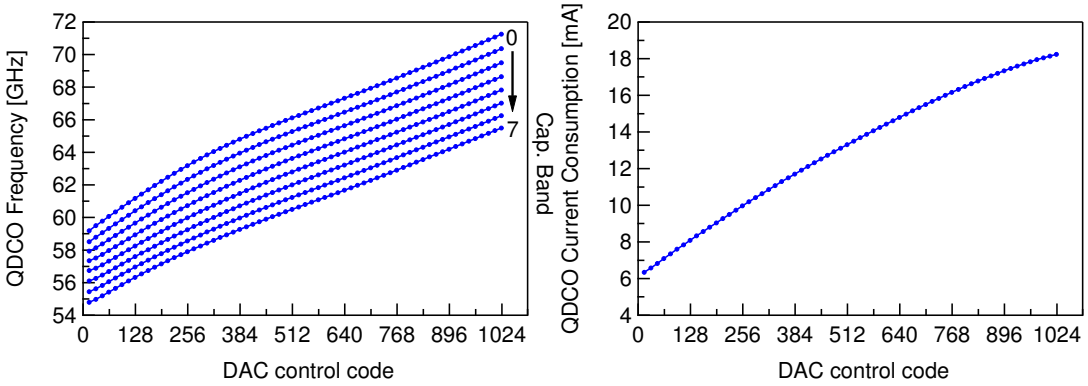
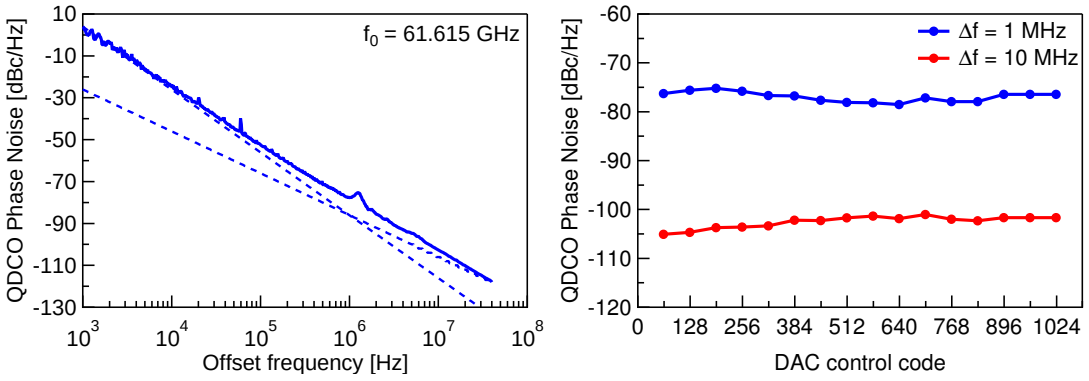


Figure 5.19: (a) QDCO frequency and (b) current consumption versus DAC input code and capacitor bank control.

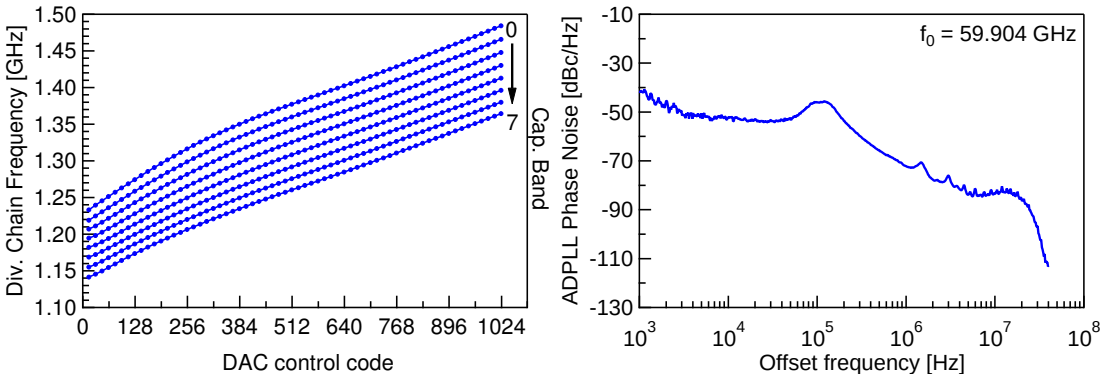
the inherently higher the flicker noise corner frequency is, which impacts the $1/f^3$ corner frequency. $1/f^3$ is around 1 MHz at 61.615 GHz). Considering that only 9 GHz are needed for the FMCW modulation, the best sub-bands are the 6^{th} and the 7^{th}: with the former, a lower average power consumption is obtained at the cost of a higher quadrature error, while it is the opposite for the latter.

Concerning the divider chain, it consumes around 7.2 mA across the whole FTR, with 7 mA for the DCMLD by 4 and 0.2 mA for the DD by 12. Overall, the power efficiency is very good, especially for the latter, whose input frequency is around 15 GHz. Indeed, this is the first demonstration of dynamic logic based divider working at such high frequencies. Fig. 5.21a shows the measured frequency band covered by the divider chain without changing the configuration: the wide-band capability matches very well the extremely large FTR provided by the QDCO.



(a) (b)

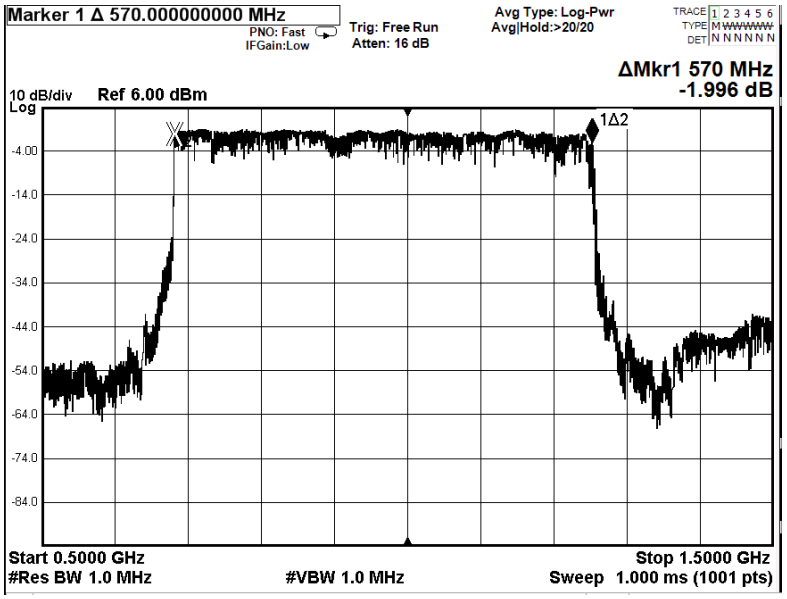
Figure 5.20: (a) QDCO phase noise at 61.615 GHz and (b) phase noise over tuning range at 1 MHz and 10 MHz offsets.



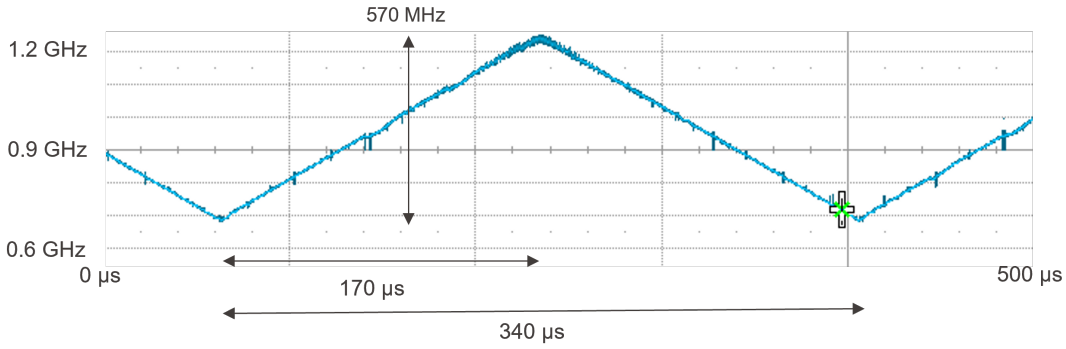
(a) (b)

Figure 5.21: Measurement of the (a) divider chain output frequency f_{CKV} versus DAC input code and of the (b) ADPLL phase noise.

The phase noise is measured in closed-loop as well: Fig. 5.21b reports the measurement at 59.904 GHz. The PLL bandwidth f_{PLL} is around 200 kHz. The bump observed around 100 kHz offset is peaking due to limited phase margin, difficult to improve with the current implementation, while the one at 10 MHz offset is the filtered QDCO quantization noise. In the given setup, with the loop filter on FPGA and all the signals exchanged between the two boards, it is complex to extend further the bandwidth. It would be beneficial for the close-in phase noise to increase f_{PLL} to filter more the QDCO noise. Finally, a triangular FMCW modulation of 9 GHz bandwidth is successfully generated with a minimum sweep time of 170 µs per ramp, which corresponds to a minimum repetition period of 340 µs. Fig. 5.22a and Fig. 5.22b show the screenshots of the covered bandwidth measured with the spectrum analyzer and the linear frequency chirp calculated from the output waveform with a high speed oscilloscope. The chirp is measured after division by 16 and for this reason the measured bandwidth is



(a)



(b)

Figure 5.22: Measurement of the ADPLL: (a) bandwidth covered with the frequency chirp and (b) frequency chirp versus time.

around 9 GHz/16. The glitches that appear in Fig. 5.22b are caused by the overlap with other components after down-conversion generated by the harmonics of the multiplied 12.5 GHz carrier in the LO signal.

Table 5.3 reports the comparison of the performance of the presented QDCO with other state-of-the-art oscillators in similar frequency band and application. Thanks to the combination of switched capacitors and coupling strength tuning, the largest overall FTR is achieved and a record 11 GHz of seamless tuning is reached. In spite of the extremely wide FTR, the lowest average power consumption for two oscillators coupled in quadrature is accomplished while fulfilling the phase noise specifications of the radar application. The designs presented in [1, 2] only report the phase noise at 1 MHz offset, while [14, 16, 23] only at 10 MHz. As a consequence, the FoM_T is calculated at these frequencies. However, if the phase noise of the

	This work	[1]	[2]	[14]	[23]	[16]
Tuning Method	Quad. coup. / Cap.	TL	Cap. / Var.	Quad. coup.	Ind. / Cap. / Var.	Quad. coup.
Tech. (nm)	22	65	65	65	65	130
V_{DD} (V)	0.8	1.2	1	1	1	0.8
Quad.	Yes	No	No	Yes	No	Yes
Freq. (GHz)	54.8-71.5	56.4-63.4	20.4-24.6	67.8-81.4	48.1-61.3	56-61.3
FTR (%)	26	11.6	18.7	18.2	24	9
P_{avg} (mW)	5 to 14.6	13.2	10	13 to 25	10	30 to 37
PN (dBc/Hz)	-103[a]	-92[b]	-102[b]	-113[a]	-115[a]	-120.6[a]
FoM_T (dBc/Hz)	-177[a]	-178[b]	-184[b]	-182[a]	-184[a]	-179.7[a]

[a] at $\Delta f = 10\,\text{MHz}$ [b] at $\Delta f = 1\,\text{MHz}$

Table 5.3: Performance comparison of mm-wave oscillators

former are already in the $1/f^2$ region, the FoM would remain constant when calculated at 10 MHz.

5.5 Summary

This chapter presents a QDCO and a divider chain for an ADPLL in the V Band around 60 GHz for a low-power and short-range FMCW radar SoC. The novelty is building the ADPLL on a frequency tuning technique which is peculiar to quadrature oscillators and fits perfectly the requirements of the targeted application. Indeed, a very wide and seamless frequency sweep is achieved by changing the coupling strength through the bias current. This technique is analyzes by means of a linear models of the QDCO, which allows to express the main design goals, such as oscillation frequency and tuning range, as a function of the coupling strength m and the resonance frequency of the tank. This tuning method is crucial for the generation of a linear frequency sweep between 57 and 66 GHz without extensive offline calibration. Indeed, when employing multiple banks of switching elements with different K_{DCO}, it is tricky to handle the transition between sub-bands without incurring excessive frequency glitches or even a non-monotonous behavior. The experimental results show a total FTR of 26 % with a extremely wide seamless tuning range of 11 GHz. This performance is achieved with an

average current consumption of the QDCO of only 13 mA, another record-low result which fulfills the radar specifications of the SoC in terms of phase noise. Moreover, the divider chain consumes only 7.2 mA, which is a very competitive results at such frequencies, made possible by the implementation of a 15 GHz dynamic divider. Finally, the digital part of the ADPLL is synthesized on the FPGA with an external 48 MHz crystal oscillator. After locking, the targeted triangular FMCW modulation with 9 GHz bandwidth is generated successfully with a minimum repetition period of 340 µs.

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6 Conclusion

In the last 20 years the business of portable devices has been extremely successful and has reached enormous volumes. The latest driver of the continuous growth of the number of devices in the world is the IoT in all its expressions. The blossoming of applications for the IoT nodes has given a new purpose to the design of low-power analog and rf circuits. In particular, the short-range remote sensing of human vital parameters and gestures is very promising and a lot of unanswered questions remain in this field. The focus of this work is on the circuits devoted to frequency generation at mm-wave and the technologies used to design them. The path toward the development of a low-power radar SoC in an advanced CMOS technology is full of challenges. This final chapter summarizes the research topics studied in this journey and the main achievements obtained and finally suggests the possible directions for future works in this field.

6.1 Summary of Research Topics

The development of a 60-GHz low-power FMCW radar SoC in an advanced CMOS technology passes through a number of fundamental steps, which represent the different topics researched in this thesis. As presented in chapter 2, the first task is the characterization of the chosen technology. Being an FDSOI technology, it is paramount to understand its full potential from the dc to the ac and rf operation. For this task, the EKV model [1–3] is a formidable tool and its simplified version allows to model the behavior of nanoscale MOSFETs by means of a handful of extracted parameters. The *IC* is the key to explore the full spectrum of the bias conditions for a device, from WI through the MI to the SI, crossing several decades of drain currents. Hence, it is possible to extract the FoMs that are needed in the design process. On top of this analysis, a further development of the existing low-power design methodologies is researched. In fact, the distortion in nanoscale MOSFEETs is studied by means of the simplified EKV model and all the related metrics are evaluated for several decades of IC. Finally, the methodology is extended to layout considerations and to the extraction of passive devices and parasitic elements.

The next step is presented in chapter 3 and it consists in the analysis of the most critical building block in a PLL in terms of power consumption and noise, namely the oscillator. A brief description of the most popular LC oscillator topologies is presented. Then, the optimum bias condition for best efficiency and lowest phase noise is studied again by means of the IC.

In chapter 4 the knowledge gathered in the previous chapters is applied to the design of two low-power oscillators at 20 GHz in 28-nm bulk CMOS technology. The use of such an oscillator, followed by a frequency tripler, is shown to be more efficient than the direct synthesis of a 60-GHz carrier [4]. The primary goal is the minimization of the power consumption at low-voltage conditions. The circuit topology and the bias scheme are optimized for this goal. Moreover, two traditional frequency tuning techniques are compared at millimeter wave to understand which one is more suited for low-power operation. One is based on a varactor for analog tuning assisted by some banks of switched capacitors while the other relies only on digitally-tuned capacitors. The former is also integrated in a radar system built with COTS used for range measurements, demonstrating the robustness of the design even with a very limited power budget.

Finally, an alternative tuning approach is studied in Chapter 5 presenting a quadrature oscillator devoted to an ADPLL for FMCW radars in 22-nm FDSOI CMOS technology. In fact, DCOs based on traditional frequency tuning technique consisting of several banks of switching elements are complex to integrate in an ADPLL when the modulation bandwidth is wide. Complex and lengthy calibration procedures for the DCO gain are required to obtain a linear sweep across several gigahertz. In the case of off-line calibration, at the end the result has to be stored in a memory and it has to be repeated periodically to compensate for variations. A very wide and seamless frequency tuning range is achieved applying a technique based on a property of quadrature oscillators. It consists in changing the coupling strength between the two oscillator cores in order to detune it from the resonance frequency [5]. The coupling is controlled by a current-steering DAC which allows to get a smooth transfer of current from the CC pair to the coupling pair. The tuning range is centered around the peak of the tank impedance by introducing an additional phase shift in front of each core transistor. The intrinsic delay of the MOSFETs at high frequency [6] and the metal lines are exploited to optimize such delay. The QDCO is followed by a wideband, efficient and compact divider chain, which is used in the feedback network of the ADPLL to perform the phase comparison in the TDC at an adequate frequency. It is composed of a DCMLD to bring the frequency below 20 GHz, followed by a cascade of DD. The former is more power-hungry but very wideband. The latter is extremely low power and compact since it benefits from the very advanced technology node. The rest of the custom-designed blocks of the ADPLL are integrated as well, while the digital circuitry is synthesized on FPGA and connected to the chip.

6.2 Main Achievements

After summarizing the main topics treated in this thesis, a list of the main achievements obtained is presented.

- A model of the output conductance G_{ds} versus the *IC* for nanoscale devices, dominated by the effect of DIBL, is proposed. Due to the complexity and the dependency on a multitude of different parameters, the old model based simply on the CLM is not valid for minimum length devices. A simple charge-based analytical expression is obtained by means of the simplified EKV model. It is a step forward toward a more comprehensive G_{ds} model and it captures its behavior as a function of the *IC*. Two additional parameters are needed to capture this behavior. An extraction method is described, complementing the procedure for n, I_{spec}, λ_c and V_{T0}. The expressions are validated versus experimental data from 28-nm bulk and 22-nm FDSOI CMOS technologies. These results are partially published in [2].

- An analysis of distortion in nanoscale MOSFETs is described. This was a missing piece in the EKV framework and it allows to implement a design methodology taking into account a specification on the linearity of the circuit. A previous analysis presented in [7] was based on a compact model and hence less suited for a simple analytical estimation. The proposed charge-based expressions of the first-, second- and third-order gate transconductances, based on the simplified EKV model, allow to precisely model the nonlinearity of minimum length devices as a function of the *IC* using only four parameters. All the linearity metrics are described accurately and even the singularity in A_{1dB}, HD_3 and A_{IIP3} is identified precisely when compared to experimental results.The outcome is that, even if in a real scenario the IC_{crit} is very hard to catch, still MI is the optimum bias condition for high linearity under low-voltage conditions where the SI is difficult to achieve due to prohibitive V_{DSsat}. These results are published in [8].

- An analysis of power consumption in LC oscillators with the *IC* methodology for class-B, class-C and class-D oscillators is proposed. The *IC* is once again the perfect tool to obtain a fair comparison among quite different topologies. The MI inversion is identified as the optimum bias point for highest efficiency for class-B and class-C, while class-D benefits more from very wide transistors and hence from the region between WI and MI. These results are published in [9].

- A complete LTI analysis of $1/f^2$ phase noise in class-B oscillators is described. Even though powerful LTV analyses were proposed in the past twenty years, a simple small-signal analysis already gives a good indication about the $1/f^2$ phase noise, which is typically dominant above 1 MHz offset and is not affected by the closed-loop operation in a PLL. The analytical expressions for the contributions to phase noise of all the noise sources in the core devices. In particular, the contribution of the gate resistance is not negligible if this parameter is not minimized with an adequate number of fingers. These results are published in [10].

- A record-low power consumption of 1.2 mW for a DCO at 20 GHz with a frequency tuning range of 27 % is demonstrated in 28-nm bulk CMOS technology. This result is made possible by the careful design of the structure and bias circuit of the oscillator for low-voltage operation, together with the optimization of the quality factor of the resonator. For the latter the design of the different switched capacitor elements is critical, especially the ones for the biggest frequency step. These results are published in [11].

- On top of the same power-optimized oscillator's structure, the DCO is compared with a VCO which reuses part of the capacitor banks. The result is that the switched capacitors are superior to varactors at 20 GHz in terms of quality factor, even when the latter covers a relatively small range. To improve it, the analog tuning should cover an even smaller range, in the order of a few tens of megahertz.

- A property of quadrature oscillators is exploited to achieve an extremely wide seamless frequency tuning range of 11 GHz in a 60-GHz QDCO for FMCW radars integrated in 22-nm FDSOI CMOS technology. This peculiar linear frequency modulation represents the perfect application for such technique, which in previous works did not have a specific purpose [5, 6]. The frequency is tuned with an optimized range of currents generated on -chip by a 10-bit current-steering DAC. The low-power aspect is not neglected even if not pushed to a minimum as in the 20-GHz DCO. Still, the lowest power consumption is achieved compared to other oscillators in a similar band or application, with a total tuning range of 26 %. These results are published in [12].

- The divider chain of the ADPLL contains a dynamic divider working up to 18 GHz. This is the first demonstration of such high frequency for a divider built with this digital-like structure, making it very attractive to replace the more power-hungry CML-based divider. These results are published in [12].

- After the synthesis of the digital part on a FPGA, the ADPLL is locked in phase to an external 48 MHz crystal oscillator and a triangular FMCW modulation with bandwidth of 9 GHz is generated with a sweep time of 170 µs per ramp and a repetition period of 340 µs.

6.3 Future Works

Throughout the course of this research, the results obtained in each area have finally left some additional questions that have not been investigated yet for a lack of time and different priorities. A short list of possible future research activities that spring from the topics covered in this thesis follows:

- Regarding the output conductance, the development of a simple model describing its behavior as a function of L would be of great importance for the design methodology for analog and rf circuits. Such a model should keep into account both DIBL and CLM

to be applicable for short- and long-channel MOSFETs. The complexity lays in the transition between the two models, namely the critical length above which the DIBL becomes negligible with respect to the CLM. The best case would be the definition of a charge-based drain current equation which includes a dependency on the drain charge from which to derive the small-signal G_{ds}.

- The development of a more comprehensive model for the output conductance would open the possibility to include its effect in the distortion analysis. Indeed, there are many circuits which have a voltage output and the inclusion of the output conductance is critical to correctly describe their linearity performance. Moreover, some basic structures with more than one transistor, like a differential pair, an OTA or a simple LNA, could be designed and characterized to show the effectiveness of the proposed model.

- If the design of a 20-GHz ADPLL is pursued, the ultra low-power DCO proposed could be used to have maximum efficiency in the frequency generation. However, some of the challenges left on this path are: the design of a low-power frequency tripler which provides I and Q outputs as well; the design of a divider chain purely based on dynamic dividers covering up to 22 GHz; conception of a light calibration procedure. A coarser DCO resolution could be envisioned, removing the fine bank and use a high-rate Σ-Δ modulator.

- If the design of the proposed 60 GHz ADPLL based on the current-controlled QDCO is pursued, the digital loop filter described could be implemented on chip after some improvements on the QDCO itself. First, a high-rate Σ-Δ modulator controlling a dedicated DAC section should be implemented to improve the frequency resolution and reduce the quantization phase noise at the expenses of power consumption. A higher resolution could be implemented by adding one or two bits in the DAC at the expenses of area if the same unit current source or worse noise and mismatch is smaller elements are used. An alternative would be to choose an hybrid tuning approach, using the coarse capacitor bank to cover a smaller range with the current technique. A bank with few elements would be easier to calibrate and the DAC could afford higher resolution in a smaller range. Moreover, it is suspected that the bias circuit of the QDCO still contributes too much noise to the total phase noise. A higher PTAT current could reduce it at the expenses of the power consumption; bigger transistors could bring lower flicker noise; a higher voltage supply domain (for example 1.2 V) for the bias circuit, which already has its own LDO, could help to reach higher *IC* values and hence lower noise.

References for Chapter 6

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A Two-Tone Analysis: Harmonic Components

In this appendix the harmonic components of $I_{\mathrm{D}}|_{\mathrm{II}}$ are reported:
DC term:

$$\omega = 0 \Rightarrow I_{\mathrm{D}(0)}|_{\mathrm{II}} = I_{\mathrm{D}0} + \frac{G_{\mathrm{m}2}(A_1^2 + A_2^2)}{4} \tag{A.1}$$

1st Harmonics:

$$\omega = \omega_1 \Rightarrow I_{\mathrm{D}(1,1)}|_{\mathrm{II}} = G_{\mathrm{m}1} A_1 + \frac{G_{\mathrm{m}3}}{4}\left(A_1 A_2^2 + \frac{A_1^3}{2}\right) \tag{A.2a}$$

$$\omega = \omega_2 \Rightarrow I_{\mathrm{D}(1,2)}|_{\mathrm{II}} = G_{\mathrm{m}1} A_2 + \frac{G_{\mathrm{m}3}}{4}\left(A_1^2 A_2 + \frac{A_2^3}{2}\right) \tag{A.2b}$$

2nd Harmonics:

$$\omega = 2\omega_1 \Rightarrow I_{(2,1)}|_{\mathrm{II}} = \frac{G_{\mathrm{m}2} A_1^2}{4} \tag{A.3a}$$

$$\omega = 2\omega_2 \Rightarrow I_{\mathrm{D}(2,2)}|_{\mathrm{II}} = \frac{G_{\mathrm{m}2} A_2^2}{4} \tag{A.3b}$$

3rd Harmonics:

$$\omega = 3\omega_1 \Rightarrow I_{\mathrm{D}(3,1)}|_{\mathrm{II}} = \frac{G_{\mathrm{m}3} A_1^3}{24} \tag{A.4a}$$

$$\omega = 3\omega_2 \Rightarrow I_{\mathrm{D}(3,2)}|_{\mathrm{II}} = \frac{G_{\mathrm{m}3} A_2^3}{24} \tag{A.4b}$$

2nd-order Intermodulation products:

$$\omega = \omega_1 \pm \omega_2 \Rightarrow I_{\mathrm{D}(\mathrm{IM}2)}|_{\mathrm{II}} = \frac{G_{\mathrm{m}2} A_1 A_2}{2} \tag{A.5}$$

3^{rd}-order Intermodulation products:

$$\omega = 2\omega_1 \pm \omega_2 \Rightarrow I_{\text{D(IM3,1)}}|_{\text{II}} = \frac{G_{\text{m3}} A_1^2 A_2}{8} \tag{A.6a}$$

$$\omega = 2\omega_2 \pm \omega_1 \Rightarrow I_{\text{D(IM3,2)}}|_{\text{II}} = \frac{G_{\text{m3}} A_1 A_2^2}{8} \tag{A.6b}$$

B Simplified EKV Model in VerilogA

This appendix contains the VerilogA code of the simplified EKV model used in ADS for simulation.

```
‘include "constants.vams"
‘include "disciplines.vams"

‘define QV(q,v)                                                                  \
begin                                                                            \
    if (v > -0.6)                                                                \
    begin                                                                        \
        z1 = 0.25 * (v - 1.4 + sqrt(v * (v - 0.394036) + 9.662671));             \
        ln_z1 = ln(z1);                                                          \
        z2 = (v - (2.0 * z1 + ln_z1)) / (2.0 * z1 + 1.0);                        \
        q = z1 * (1.0 + z2 * (1.0 + 0.070 * z2));                                \
    end                                                                          \
    else                                                                         \
    begin                                                                        \
        ln_z1 = 0.5 * (v - 0.201491 - sqrt(v * (v + 0.402982) + 2.446562));      \
        z1 = exp(ln_z1);                                                         \
        z2 = (v - (2.0 * z1 + ln_z1)) / (2.0 * z1 + 1.0);                        \
        q = z1 * (1.0 + z2 * (1.0 + 0.483 * z2));                                \
    end                                                                          \
end

module sEKV_NMOS_Model1(drain, gate, source, bulk);

inout drain, gate, source, bulk;
electrical drain, gate, source, bulk;
parameter real UT = 25.875E-3;
parameter real W = 1E-6;
parameter real L = 1E-6;
parameter real shrink = 0.9;
parameter real VT0 = 0.455;
parameter real Ispecsq = 870E-9;
parameter real n = 1.44;
parameter real Lsat = 15E-9;

real VG, VS, VD, VP, vp, vg, vs, vd, vps, vpd,
real qs, qd, qdsat, z1, z2, ln_z1_, Ids, lambdac, Ispec;

analog begin
```

```
    VG = V(gate,bulk);
    VS = V(source,bulk);
    VD = V(drain,bulk);
    VP = (VG - VT0)/n;
    vp = VP/UT;
    vg = VG/(UT);
    vs = VS/(UT);
    vd = VD/(UT);
    vps = vp-vs;
    vpd = vp-vd;
    lambdac=Lsat/(L*shrink);
    Ispec=Ispecsq*(W/L);

    `QV(qs,vps)
    `QV(qd,vpd)
    qdsat = 2*lambdac*(qs+qs*qs)/(2+lambdac+sqrt(4*(1+lambdac)+lambdac*lambdac
      *(1+2*qs)*(1+2*qs)));
    if (qd <= qdsat)
    begin
        Ids=Ispecsq*(W/L)*(qs + qs*qs - qdsat - qdsat*qdsat);
    end
    else
    begin
        Ids=Ispecsq*(W/L)*(qs + qs*qs - qd - qd*qd);
    end
I(drain,source) <+Ids;

end
endmodule
```

List of Publications

Journal Papers

- F. Chicco, A. Pezzotta, and C. C. Enz. “Charge-Based Distortion Analysis of Nanoscale MOSFETs”. In: IEEE Transactions on Circuits and Systems I: Regular Papers 66.2 (Feb. 2019), pp. 453–462.
- F. Chicco, S. Cerida Rengifo, F. X. Pengg, E. Le Roux, and C. Enz. “Power-Optimized Digitally- Controlled Oscillator in 28-nm CMOS for Low-Power FMCW Radars”. In: IEEE Microwave and Wireless Components Letters 31.8 (Aug. 2021) pp. 965-968.
- C. Enz, F. Chicco, and A. Pezzotta. “Nanoscale MOSFET Modeling: Part 1: The Simplified EKVModel for the Design of Low-Power Analog Circuits”. In: IEEE Solid-State Circuits Magazine 9.3 (Summer 2017), pp. 26–35.
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Conference Papers

- F. Chicco, A. Pezzotta, and C. C. Enz. “Analysis of Power Consumption in LC Oscillators based on the Inversion Coefficient”. In: 2017 IEEE International Symposium on Circuits and Systems (ISCAS).May 2017, pp. 1–4.
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Work Experience

June 2017- Today

PhD Student

CSEM, Neuchâtel, Switzerland

- Designed and laid out mm-wave circuits in TSMC 28nm Bulk CMOS technology for a 110 GHz CW and FMCW RADAR System demonstrator:
  - 20 GHz low-power and wide tuning range voltage-controlled oscillator (VCO);
  - 20 GHz low-power and wide tuning range digitally-controlled oscillator (DCO);
  - 20 GHz static current-mode logic (CML) divider-by-2.
- Performed measurements on the 28 nm chip and the RADAR demonstrator:
  - Compared open-loop performance of VCO and DCO;
  - Verified closed-loop behavior of VCO with PLL board;
  - Performed range and Doppler measurements with the RADAR system.
- Designed and laid out mm-wave and analog circuits in GF 22 nm FDSOI CMOS technology for a 60GHz ADPLL in a FMCW RADARoC:
  - 60 GHz low-power and wide tuning range quadrature DCO with seamless frequency tuning acting on coupling factor;
  - Divider chain composed of a 60 GHz wideband dynamic CML divider-by-4 and a 15 GHz dynamic divider-by-12;
  - 10b current-steering digital-to-analog converter (DAC) and proportional-to-absolute-temperature (PTAT) current references.
- Performed digital simulations of 60 GHz ADPLL model.

Nov 2015- Today

PhD Student

ICLAB - EPFL, Neuchâtel, Switzerland

- Performed analysis of power consumption and in LC oscillators based on the inversion coefficient methodology;
- Performed linear analysis of phase noise in LC oscillators including all MOSFET noise sources;
- Performed analysis of MOSFET distortion based on the inversion coefficient with comparison with measurements on TSMC 28 nm Bulk CMOS devices;
- Attended Mead courses on analog and RF low power design, PLL and oscillators, noise and variability; PhD course on wireless tranceivers design.

Publications

- F. Chicco, A. Pezzotta and C. C. Enz, "Charge-Based Distortion Analysis of Nanoscale MOSFETs", in IEEE Transactions on Circuits and Systems I: Regular Papers 66.2 (Feb. 2019), pp. 453-462;
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- C. Enz, F. Chicco and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 2: Using the Inversion Coefficient as the Primary Design Parameter", in IEEE Solid-State Circuits Magazine 9.4 (Fall 2017), pp. 73-81;
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Education

Oct 2013-Sept 2015

Master in Micro and Nanotechnologies for Integrated Systems

Joint degree with three universities:

- **Politecnico di Torino**, Italy
- **Institut Polytechnique de Grenoble - Phelma**, France
- **École Polytechnique Fédérale de Lausanne**, Switzerland

Final Grade: 110/110 cum Laude

Relevant modules: Analog circuit design, Advanced analog and RF integrated circuits design, Fundamentals of VLSI design, Hardware systems modeling, HF and VHF circuits and techniques, Lab in EDA based design, Test of VLSI systems, Integrated Optics, Microfabrication;

Master Thesis: "Design and Implementation of the Write and Read Circuitry for a 512 byte ReRAM Array in 40 nm Technology" at LSM - EPFL.

Skills

Software and Programming

Virtuoso, ADS, Calibre, Momentum, Helic, Questa
MATLAB, Mathematica, MathCad
C, Python, VHDL, VerilogA, LaTeX, MS Office

Languages

Italian: Mothertongue
English: Fluent, C1 level
French: Intermediate level, B2 level