IEEE Open Journal of Power Electronics, pp. 1–1, 2021

Distributed Real-Time Model of the M3C for HIL Systems Using Small-Scale Simulators

P. Bontemps, S. Milovanovic, and D. Dujic

POWER ELECTRONICS LABORATORY
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

OJ-PEL-2021-0069

Distributed Real-Time Model of the M3C for HIL Systems Using Small-Scale Simulators

Philippe Bontemps, *Student Member, IEEE,* Stefan Milovanovic, *Member, IEEE,* and Drazen Dujic, *Senior Member, IEEE*

Hardware-in-the-loop systems are an essential tool to verify controllers and deployed control algorithms in a risk-free environment. The inaccessibility of the converters used in applications such as pumped hydro storage power plants due to their high ratings, require the development of a hardware-in-the-loop platform to perform the validation of the deployed control structures and algorithms. This paper presents the modeling and splitting of the model of the matrix modular multilevel converter to allow the usage of small-scale simulators, such as the RT Boxes, to deal with the complex system exceeding capabilities of a single unit. To achieve an acceptable simulation step-size, this paper demonstrates the splitting of the model into multiple independent instances using the concept of virtual capacitance implementation. The verification of the proposed concept is done on a hardware-in-the-loop system compromising ten RT Boxes, where the physical model of the matrix modular multilevel converter is deployed, and control algorithms are implemented on the ABB PEC800 industrial controllers.

***Index Terms*—Hardware-in-the-Loop, Matrix Modular Multilevel Converter, Pumped Hydro Storage Power Plants, Real-Time Simulations, Variable Speed Drive**

I. Introduction

THE ever increasing installed power of renewable energy to fulfill the European goal of a 55% emission reduction requires reliable, large scale and fast responding energy storage systems [1]. Relying on existing infrastructure of Pumped Hydro Storage Power Plants (PHSPs) which has proven to be a large scale, reliable, energy storage system since its introduction over a century ago, reduces the environmental and economical impact. However, the majority of PHSP were designed for fixed speed generating during daytime and fixed speed pumping during night-time which lacks the required flexibility to cover the highly intermittent energy production of renewable energy sources such as wind and solar. Facing these requirements of increased flexibility to remain competitive on the energy market, PHSP need to migrate to variable speed, allowing for flexible operating power, fast speed reversal transients as well as increased efficiency [2]–[4].

In order to enable variable speed operation, the machine of the PHSPs requires to be interfaced to the grid through a power electronics converter. The high power requirements of PHSP constitute a challenge for Variable Speed Drive (VSD) due to the converter requirements, making conventional converters unsuited for such applications. However, the rise of the Modular Multilevel Converter (MMC) technology [5] allows, due to its modularity which relies on the series connection of cells, each with its own capacitor, to be scaled to the power and voltage requirements of PHSP [6], while current scaling can be achieved as explained in [7], [8]. Additionally the elimination of the connected transformer as well as the fact that the high quality output waveform, resulting form this cascaded connection, reduces the filtering requirements, the overall size of the installation can be reduced significantly which results in a reduction of civil engineering costs. Within the family of MMC, the Matrix Modular Multilevel Converter (M3C), shown in Fig. 1, is especially suited for PHSP being optimized for low frequency high power drives [9]. Recently, Austria saw the commissioning of the first Converter Fed Synchronous Machine (CFSM) PHSP installation using an M3C in the Malta Oberstufe power plant [10].

The inaccessibility of converters fulfilling the ratings needed for PHSP together with the complexity of MMC topology, require a thorough verification process of the control structure before the deployment in the field. The cascaded connection of cells being the main advantage of the MMC, it also constitutes the main challenge, namely the complex control structure including balancing of the energy among the cells. To ensure

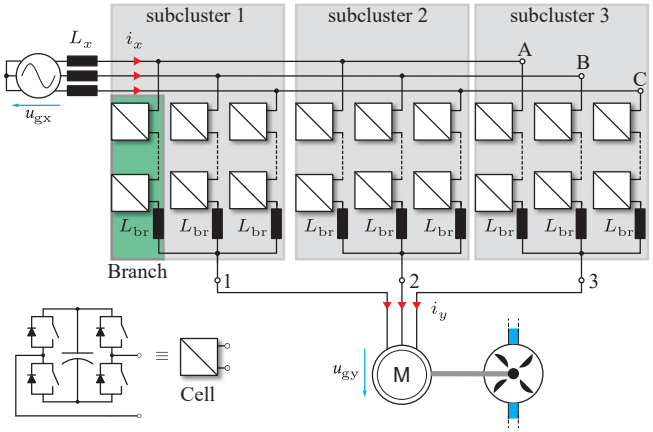

Fig. 1. The matrix modular multilevel converter with the three subclusters, highlighted in gray, each containing three branches, highlighted in green, and N cells per branch. The two AC systems connected to the terminals are represented by a grid on the input side and a 3 phase machine on the output side connected to a pump/turbine as is the case in a PHSP.

This paper was submitted on the 25^{th} of August 2021. "The results presented in this paper are a part of the Hydropower Extending Power System Flexibility (XFLEX HYDRO) project that has received funding from the European Union's Horizon 2020 research and innovation programme under grand agreement No 857832.".

The autors are with the Power Electronics Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: philippe.bontemps@epfl.ch; stefan.milovanovic@epfl.ch; drazen.dujic@epfl.ch)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

OJ-PEL-2021-0069

correct operation of the converter beyond simple simulations, but without the danger of damaging expensive equipment, the Hardware-In-The-Loop (HIL) testing system is widely used [11]–[18].

The HIL differs from simple real-time simulations by the usage of the same controller hardware of the actual converter which are interconnected to the real-time computers. In a properly set up HIL configuration, the controllers and deployed control algorithms behave exactly as they would in the real physical prototype, and should not be able to differentiate between the two situations. This property of the HIL allows for accurate verification of the control structure and control algorithm implementation. As a consequence, the risk for control failure during on-site testing is significantly reduced through analysis of the behavior throughout various scenarios using HIL simulations.

To achieve proper operation of the controller and accurately simulate a real system, the HIL system should be able to recreate the actual state of the system at each instance in time. This accuracy of the real time computers determines the quality and validity of the results recorded on the HIL simulator. The discrete time step of the HIL system depends on the hardware of the computer itself, as well as on the complexity of the model that is being implemented. Being able to simplify the model to achieve time step ranging from a few hundred of nanoseconds to several microseconds, is necessary to guarantee the fidelity of the simulations.

Even if large-scale simulators designed for complex circuits with multiple input/output exist (e.g. dSpace, Opal RT or RTDS), this paper focuses on the use of cheaper small-scale simulators such as the RT Box [19] or the Typhoon HIL [20]. In this work the software being used relies on the state-space approach using ideal switches. The simulation of switching devices relies on the implementation of state-space matrices for each possible combination of all the switching states, leading to a total of 2^N state-space matrices considering N switches in the system and the possibility to switch between the matrices depending on the current operating point of the converter.

The development of a HIL system for the MMC topology has been used in multiple publications [11]–[18], however these simulations are focusing on the Indirect Modular Multi-level Converter (IMMC) whereas in the literature, there are no available publications on how to model the M3C in real-time, or let alone, how to achieve cost effective HIL system. This paper is the first one developing a distributed real-time compatible M3C model using the concept of virtual capacitances to allow implementation on small scale simulators and this is considered its biggest contribution. This work aims to describe modeling of the M3C to be used in a real-time HIL testing platform and can be used for any type of interconnection between two 3 phase ac systems, thus also for the transition to VSD in PHSP.

The rest of the paper is organized as follows, section II provides a detailed description of the HIL system that is used for the simulations. Section III describes the modeling of the M3C for real-time applications and section IV presents the results acquired on the employed HIL platform.

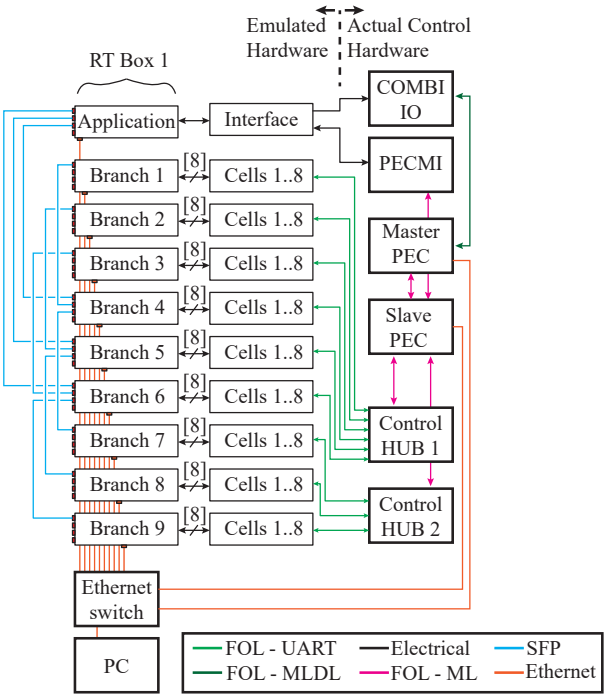

Fig. 2. HIL structure showing the connection between the real hardware on the right side and the emulated hardware on the left side. The type of connection between the devices is determined by the different colors.

II. Description of the Real-Time HIL System

The schematics of the HIL platform that is used in this paper is shown in Fig. 2 and is based on the interconnection of 10 RT Boxes to model the M3C, but shares the same control hardware as the setup used for IMMC described in [13] and [21]. One RT Box, hosting the input ac grid as well as the ac output application (ac machine or ac grid), will be referred to as Application RT Box. The nine remaining RT Boxes are used to model the cascaded connection of cells constituting a branch as shown in Fig. 1 and will be referred to as Branch RT Box. The Application RT Box is is interconnected to all nine Branch RT Boxes and maps their signal to simulate the M3C structure as seen in Fig. 1.

The interconnection between the elements as well as the nature of this interconnection is shown in Fig. 2. Two ABB PEC800 controllers are used, one acting as Master and one as Slave controller. The Master controller hosting the general state machine and references, whereas the Slave controller handles the control of the M3C. Communication between Master PEC and Slave PEC, as well as between the Slave PEC and PECMI is achieved through bidirectional Fiber Optical Link (FOL) using the ABB proprietary protocol named MultiLink (ML). The COMBI IO as seen in Fig. 2, manipulates the low level external signals (e.g. doors, fans, breaker status,...), the PECMI is responsible for input grid side current and voltage measurements, and the CONTROL HUB manages communication protocol with the cells through FOL.

Fig. 3 shows the picture of the front side of the HIL where the Application RT Box is marked by the number 1, and the nine Branch RT Boxes by the number 2. The scaling of the analog and digital input/output to fulfill the requirements of

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

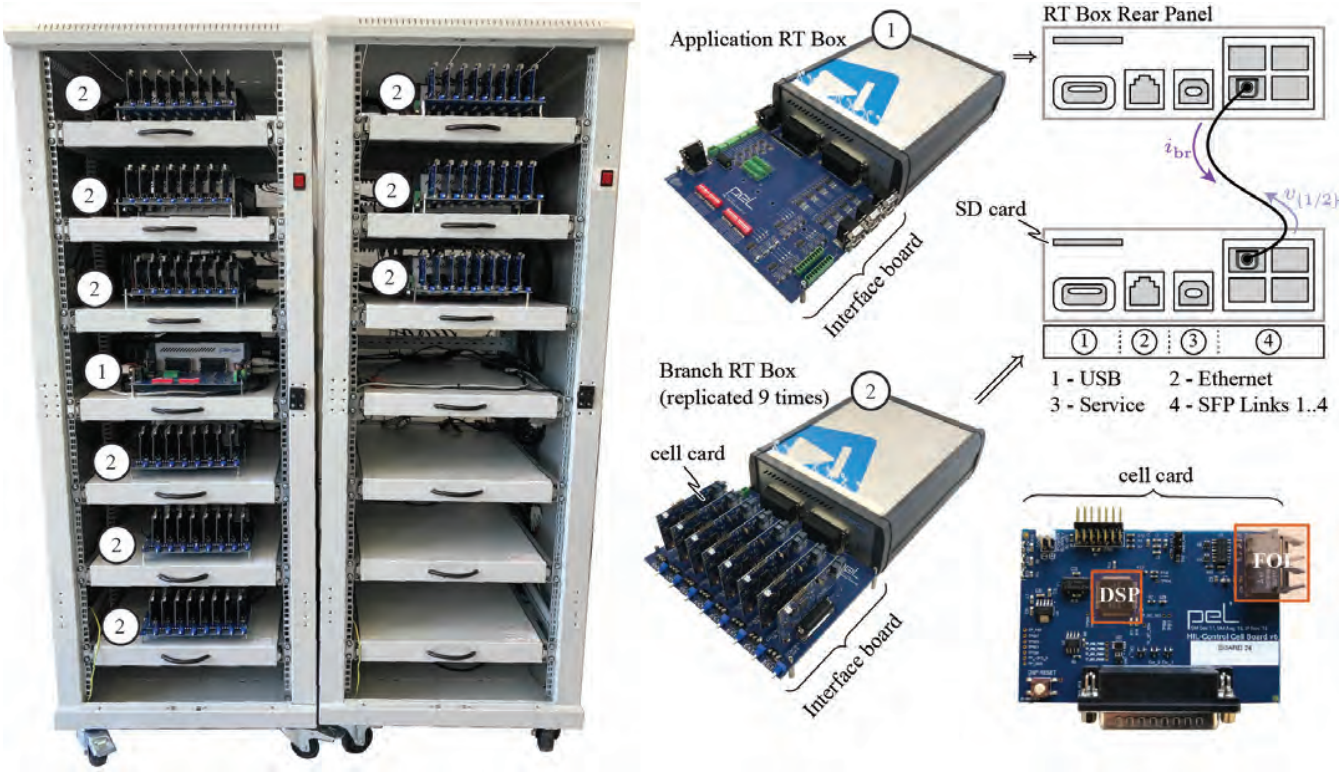

Fig. 3. HIL system used for model verification purpose. The left side shows a front picture of the HIL reconfigured for the M3C compared to the cabinet used in [13]. A zoomed picture of both the application and Branch RT Box is shown in the middle labeled by 1 and 2, and their interconnection is shown on the top right. The logical circuit of the cells is implemented on the cell card shown on the bottom right.

the PEC is achieved through the interface board connected to the Application RT Box. Two main parts can be distinguished on the MMC cell, namely the power part and the logic part. On the HIL system, the power part is modeled on the Branch RT Boxes and the logic part is implemented on the so called cell cards, each having a local cell control algorithm running on TI Digital Signal Processor (DSP) that are connected to the interface board [13] [22]. This interface board connected to the Branch RT Box allows for a connection of eight cell PCB cards as shown in Fig. 3. The cell card receives the voltage and current reference for the cell terminals through FOL and sends back both the measurement of the branch current and cell capacitance voltage, among other relevant exchanged data.

The Branch RT Box hosts the model of the series connection of several Full Bridge (FB) cells representing the power stage of the cascaded connected cells which form the branch in the system. The limited number of digital input ports on the RT Box, namely 32, together with the requirements of four switching signals per cell that are generated by the DSP on the cell card, limits the number of cells per RT Box to 8. Additionally through the analog outputs, the measurements of the branch current and the cell voltages is sent to each cell card, respectively. As shown in Fig. 3, the Branch RT Boxes communicate, through the SFP link, two voltage references for each branch to the Application RT Box, whereas the latter one sends the respective branch current to each Branch RT Box.

III. Real-time modeling of the M3C

The M3C outperforming the IMMC, due to the overall lower cost and smaller size as a consequence of the reduced number of branches, makes it the preferred solution for low-speed, high torque drives [23]. A HIL system being necessary to verify proper operation of the converter control algorithm to avoid damaging high value equipment, the following section is dedicated to the modeling of the M3C on the HIL. The HIL system presented above requires development of suitable models that can support real-time simulation requirements, even for a system as complex as the M3C.

The RT Box is relying on the use of state-space matrices, the number of which depends on the amount of switches in the system. Assuming a model with N ideal switches, and each switch having two distinct states (conducting or blocking), the number of state space matrices is defined by 2^N. The validity of a real-time model lies in the capability of the simulator to select and load, among the pre-computed matrices, the one corresponding to the next state of the converter. Logically, the higher the number of matrices, and the larger these matrices are, the longer it takes to the simulator to select the correct matrix, potentially increasing the computational burden above the threshold for achieving accurate real-time simulations.

The M3C, as seen in Fig. 1, relies on the usage of FB cells, as both positive and negative terminal cell voltages are required to fulfill proper operation, even though different cell topologies are possible [24]. Modeling of the M3C, without any simplifications, using FB cells and N cells per branch,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

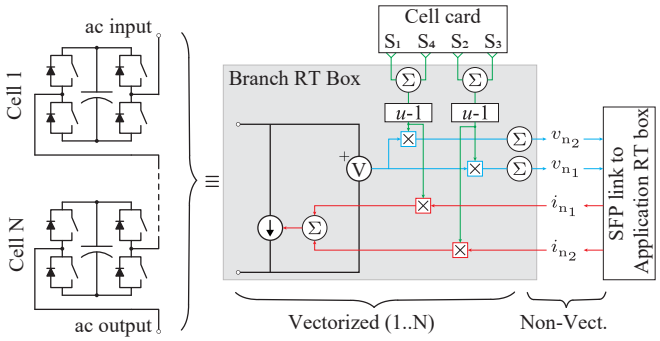

Fig. 4. Model running on each Branch RT Box

the total number of state space matrices related to this model is equivalent to $2^{9\times4\times N}$ which results in 2^{288} for the case of eight cells per branch, as in this work. Such a high number of state renders M3C real-time simulations impossible on the platform used in this work. Therefore simplifications, which guarantee simultaneous preservation of the model correctness, are required and they are discussed in the following paragraphs.

A. Branch RT Box

The implementation of the nine single branches on the nine Branch RT Boxes is done using the sub-cycle averaged model of the series connected FB cells without any loss of generality, as explained in [25] and used in [13]. While the use of sub-cycle averaged model does not interfere with the main purpose of the HIL, this being the verification of the control structure and algorithm, it makes the HIL simulations incompatible for converter loss calculations. Fig. 4 shows the model implemented on the Branch RT Box, and this model is equivalent for all the nine Branch RT Boxes. Four switching signals are generated by local cell controller DSP and sampled by RT Box digital inputs. With a combination of the switching signals, the voltages v_{n_1} and v_{n_2} where $n \in [1, 2, \ldots, 9]$ representing the number of the branch, is used in the M3C model defined in Fig. 6, which is further explained in the next sub-section.

B. Branch equivalent model

One of the challenges for real-time simulations of converters made from series connection of identical cells, is to find an equivalent branch model which reduces the number of switches to a minimum while not limiting the model to

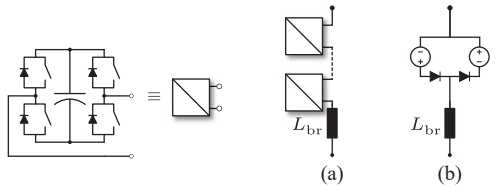

Fig. 5. Equivalent branch model for (a) the real converter using a cascaded connection of full bridge cells (b) the real time model using two controlled voltage sources and two diodes

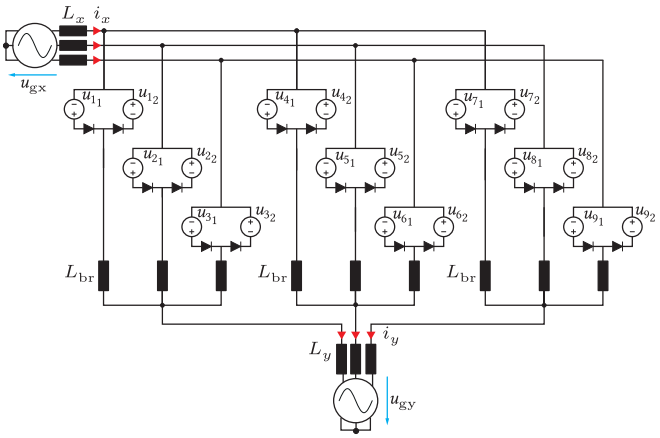

Fig. 6. M3C model using a branch equivalent representation reducing the number of switches and making them independent from the number of cells per branch.

certain operating points. The idea of replacing a branch by a controlled voltage source, as used in [26] and [27], and while working in steady state operation, it fails to model the blocking state of the converter correctly. While an extension of this model is proposed in [28], the increase in the number of switches makes it less suitable for real-time applications. With two diodes and two controlled voltage sources, as shown in Fig. 5(b), the model as proposed in [29] and [30] ensures correct simulation of both blocked and active states of the converter. The equivalent model of the converter using this branch simplification is shown in Fig. 6.

This simplification reduces the number of switches to two diodes per branch independently from the number of cells, thus the number of state space matrices is significantly reduced from 2^{288} to 2^{18}. Nevertheless, the complexity of this model due to the high number of state space matrices, makes it unsuitable for the implementation on the Application RT Box, to the point of not even being able to load this configuration onto the RT Box. Consequently, the already simplified model requires additional splitting to further reduce the number of state matrices to make it compatible with the RT Box and to reduce the simulation time step.

C. Splitting of the M3C model

The branch model as shown in Fig. 6, being simplified to the maximum while still being valid in all operating conditions, makes further simplification impossible without loss of generality. In order to further reduce the number of state space matrices, the dependency between the subclusters of the M3C shown in the Fig. 6 has to be eliminated, which requires splitting of the model into multiple smaller circuits running in parallel. From the topology, as shown in Fig. 6, an available separation would be the one of the three subclusters into three parallel running circuits and replacing them with current sources in the original circuit. Such a separation allows to reduce the number of state space matrices from 2^{18} to 3×2^{6}, which results in the reduction needed to allow an acceptable step size for the HIL simulations.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

OJ-PEL-2021-0069

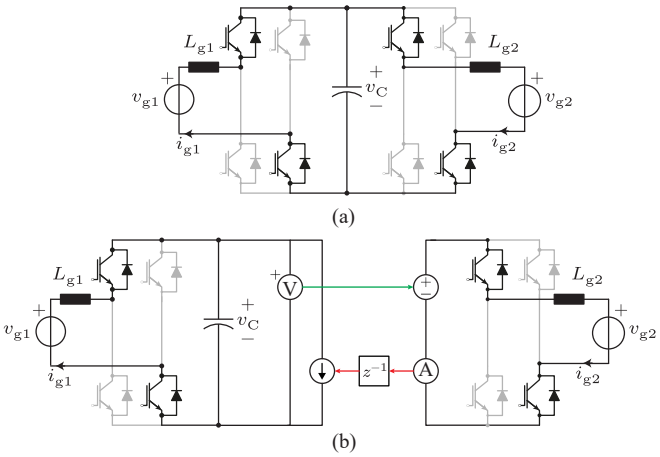

Fig. 7. Example of circuit splitting, with (a) showing the initial circuit an arbitrary switching state and (b) the equivalent split circuit in the same switching state

The concept of splitting a circuit into smaller independent circuits and the resulting benefits are demonstrated on the circuit shown in Fig. 7 using two FB cells with a common capacitance in an arbitrary switching stage. The state space matrix defining the initial circuit is expressed as:

$$\underbrace{\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{g1}} \\ v_{\mathrm{c}} \\ i_{\mathrm{g2}} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_{\mathrm{g1}}} & 0 \\ \frac{1}{C} & 0 & \frac{1}{C} \\ 0 & \frac{1}{L_{\mathrm{g2}}} & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_{\mathrm{g1}} \\ v_{\mathrm{c}} \\ i_{\mathrm{g2}} \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L_{\mathrm{g1}}} & 0 \\ 0 & 0 \\ 0 & -\frac{1}{L_{\mathrm{g2}}} \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} v_{\mathrm{g1}} \\ v_{\mathrm{g2}} \end{bmatrix}}_{u} \tag{1}$$

The total number of state-space matrices that define such a circuit is calculated by: $N_{ss} = 2^{4+4}$. An intuitive way of splitting this circuit is at the capacitance, resulting in two individual circuits with each four switches, thus resulting in $N_{ss} = 2 * 2^4$. The resulting state-space matrices of the split circuit in the same switching state is shown in Fig. 7 is:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{g1}} \\ v_{\mathrm{c}} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_{\mathrm{g1}}} \\ \frac{1}{C} & 0 \end{bmatrix}}_{A_1} \begin{bmatrix} i_{\mathrm{g1}} \\ v_{\mathrm{c}} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_{\mathrm{g1}}} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}}_{B_1} \begin{bmatrix} v_{\mathrm{g1}} \\ i_{\mathrm{s}} \end{bmatrix} \tag{2}$$

$$\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} = \underbrace{\begin{bmatrix} 0 \end{bmatrix}}_{A_2} \begin{bmatrix} i_{\mathrm{g2}} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_{\mathrm{g2}}} & -\frac{1}{L_{\mathrm{g2}}} \end{bmatrix}}_{B_2} \begin{bmatrix} v_{\mathrm{s}} \\ v_{\mathrm{g2}} \end{bmatrix} \tag{3}$$

Assuming a small time-step, such that the following approximation holds: $i_s = i_{\mathrm{g2}}[k-1] \approx i_{\mathrm{g2}}[k]$ and replacing $v_s = v_{\mathrm{c}}$ it is obvious that the resulting state space matrix from the split circuit corresponds to the initial one.

Applying the same logic to the model of the M3C seen in Fig. 6, is not possible due to the absence of centralized dc link. Nevertheless, this issue can be solved by the addition of artificial capacitances and resistances. As this addition exists only in the real-time model the added elements will be referred to as Virtual Resistor (VR) and Virtual Capacitor (VC) respectively. The HIL is all about processing virtual power, which allows the introduction of an additional components to the circuit under the condition that the virtual circuit which

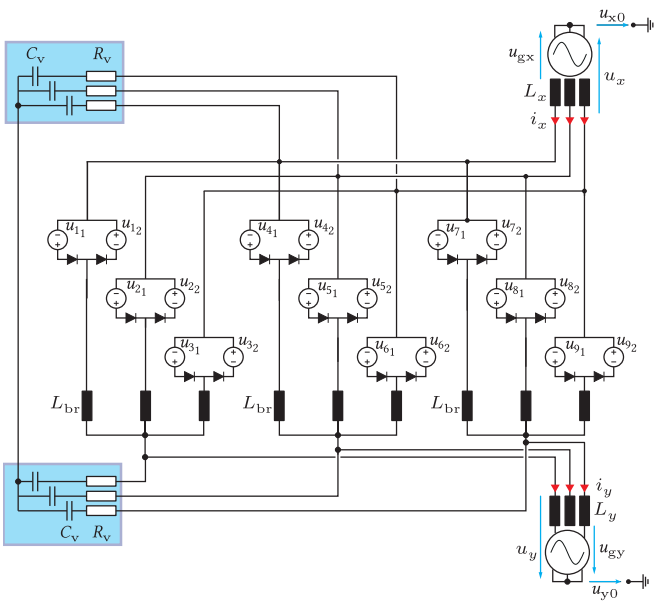

Fig. 8. Extension of the M3C model using VC and VR highlighted in blue. This addition allows splitting of the model resulting in further time step reduction while not changing its validity regarding the testing of the control scheme.

is introduced does not affect the frequency components of interest to allow the validation of the controller. Fig. 8 shows the addition of two sets, each consisting of three resistances and capacitances to the initial circuit shown in Fig. 6. The tuning of the VC and VR is presented afterwards.

The goal of the addition of the VC and VR is to split two of the three subclusters from the rest of the system, in this case subclusters 1 and 2 were chosen. To prove the validity of this separation, the Kirchhoff voltage and current laws can be analyzed and compared to the initial equations resulting from Fig. 6. The following analysis of Fig. 8 holds for any of the nine branches, where x denotes the input phase, $x \in [A, B, C]$ and y the output phase $y \in [1, 2, 3]$.

$$u_{\mathrm{xy}} = u_{\mathrm{x}} + u_{\mathrm{x0}} - u_{\mathrm{y}} - u_{\mathrm{y0}} \tag{4}$$

From (4), combining u_{y0} and u_{x0}, the common mode voltage can be defined by $u_0 = u_{\mathrm{y0}} - u_{\mathrm{x0}}$.

The AC terminal currents from both the input and output terminals of Fig. 1 can be defined by:

$$i_{\mathrm{x}} = \sum_{\mathrm{y}} i_{\mathrm{xy}} \qquad \text{for x} \in [A, B, C] \tag{5}$$

$$i_{\mathrm{y}} = \sum_{\mathrm{x}} i_{\mathrm{xy}} \qquad \text{for y} \in [1, 2, 3] \tag{6}$$

While it is obvious that (4) remains the same for the model with the virtual circuit shown in Fig. 8, (5) and (6) will be influenced by the addition of the virtual circuit.

$$i_{\mathrm{x}} = \sum_{\mathrm{y}} i_{\mathrm{xy}} + i_{\mathrm{vx}} \qquad \text{for x} \in [A, B, C] \tag{7}$$

$$i_{\mathrm{y}} = \sum_{\mathrm{x}} i_{\mathrm{xy}} + i_{\mathrm{vy}} \qquad \text{for y} \in [1, 2, 3] \tag{8}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

OJ-PEL-2021-0069

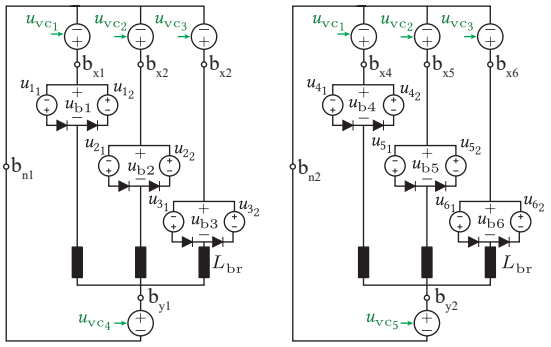

Fig. 9. Separating both subcluster 1 and 2 from the initial model of the M3C

To guarantee validity of the split model, it has to be proven that from the controller point of view following equations are verified (5) = (7) and (6) = (8). It is of importance to prove that, from the controller point of view, there is no influencing difference between the model on the HIL and the actual converter circuit. As the high frequencies are filtered out in the control loop, the frequencies that may interfere with the control are the low frequencies close to the nominal operating frequencies of the model. With a properly tuned virtual circuit, resulting in a very high impedance for low frequencies and thus a current lower than 1% of the nominal current flowing through the virtual circuit, this model can be considered equivalent to the actual converter circuit, at least from the controller verification viewpoint.

With a properly tuned virtual circuit, subclusters 1 and 2 in Fig. 8 can be separated from the model and be represented by Fig. 9. However, to guarantee Kirchhoff voltage laws to be equal to the initial model, some constraints are to be applied to the voltage sources present in the subcluster model.

- The potential between the points marked by $\mathrm{b_{x1}}$ and $\mathrm{b_{x2}}$ must be equal to the potential between the points A and B in Fig. 8. The same condition holds for $\mathrm{b_{x4}}$ and $\mathrm{b_{x5}}$.
- The potential at the points $\mathrm{b_{n1}}$ and $\mathrm{b_{n2}}$ should be equal.
- The potential between the points $\mathrm{b_{y1}}$ and $\mathrm{b_{y2}}$ must be equal to the potential between the points 1 and 2 in Fig. 8.

With these conditions, following voltages can be defined:

$$u_{\mathrm{vc}_{1,2,3}} = u_{\mathrm{A,B,C}} - 0.5u_0 \tag{9}$$

$$u_{\mathrm{vc}_{4,5,6}} = u_{1,2,3} + 0.5u_0 \tag{10}$$

With the conditions above, it can be shown that the Kirchhoff current laws from the initial model are verified as well. The expression of the branches from the two separated subclusters 1 and 2 are defined below:

$$\begin{aligned} L_{\mathrm{br}}\frac{\mathrm{d}i_{\mathrm{b}_{1,2,3}}}{\mathrm{d}t} &= u_{\mathrm{vc}_{1,2,3}} - u_{\mathrm{b}_{1,2,3}} - u_{\mathrm{vc4}} \\ &= u_{\mathrm{A,B,C}} - u_{\mathrm{b}_{1,2,3}} - u_1 - u_0 \end{aligned} \tag{11}$$

$$\begin{aligned} L_{\mathrm{br}}\frac{\mathrm{d}i_{\mathrm{b}_{4,5,6}}}{\mathrm{d}t} &= u_{\mathrm{vc}_{1,2,3}} - u_{\mathrm{b}_{4,5,6}} - u_{\mathrm{vc5}} \\ &= u_{1,2,3} - u_{\mathrm{b}_{4,5,6}} - u_2 - u_0 \end{aligned} \tag{12}$$

After both subclusters are modeled separately, as they constitute a series connection of a voltage source with an inductor, they can be replaced by a controlled current source in the initial model. Two additional conditions have to be fulfilled to guarantee proper operation of the split model, namely:

1. The virtual circuit is tuned in a way to constitute a very high impedance for low frequency currents, thus its influence on the model can be discarded.
2. The simulation time step should be small enough to validate the statement that two neighboring samples of any quantity, here labeled with x, can be considered negligible, which is mathematically formulated as: $x[k] - x[k+1] \approx 0$. This second condition is necessary as a delay between the current measurement of the split circuit and the main circuit has to be introduced to avoid an algebraic loop, and this delay should be negligible to the overall system.

With the previously mentioned conditions fulfilled, the split model shown in Fig. 10 can be defined. The main objective to reduce the number of state space matrices has successfully been achieved as with the splitting, this number was reduced to 3×2^6.

The final model seen in Fig. 10, contains additional splitting where both the AC grids are replaced each by two current sources. This additional splitting is a possibility because of the addition of the VC, and further simplifies the overall model, further reducing the computational resources needed to compute the circuit. From Fig. 10 it can be observed that the initial model is split into five separate instances:

- System 1 $\rightarrow$ Subcluster 3 including VCs and VRs
- System 2 $\rightarrow$ Subcluster 1
- System 3 $\rightarrow$ Subcluster 2
- System 4 $\rightarrow$ Input AC grid
- System 5 $\rightarrow$ Output AC grid or AC machine

Previously it was proven that the addition of the virtual circuit, if tuned properly does not influence the functionality of the basic model. Additionally the separation of the two subclusters from the initial model was shown to not change the operation of the converter. With all the circuits together, shown in Fig. 10, the final verification to prove that the replacement of the two subclusters with current sources as well as the addition of the VC and VR does not change the input and output terminal dynamics of the initial model is presented below. With 21 branches and 9 nodes in the circuit, a total of 13 voltage loops can be defined in the circuit shown in Fig. 10, from where the expression of the ac input grid voltage is found.

$$\begin{aligned} u_{\mathrm{g_{A,B,C}}} - L_{\mathrm{x}}\frac{\mathrm{d}i_{\mathrm{A,B,C}}}{\mathrm{d}t} &= \frac{u_{\mathrm{b}_{7,8,9}}}{3} + \frac{L_{\mathrm{br}}}{3}\frac{\mathrm{d}i_{\mathrm{b}_{7,8,9}}}{\mathrm{d}t} \\ &\quad + \frac{2u_{\mathrm{vc}_{1,2,3}}}{3} - \frac{u_{\mathrm{vc}_4}}{3} - \frac{u_{\mathrm{vc}_5}}{3} + u_0 \end{aligned} \tag{13}$$

Inserting (11) and (12), leads to the final expression:

$$\begin{aligned} u_{\mathrm{g_{A,B,C}}} - L_{\mathrm{x}}\frac{\mathrm{d}i_{\mathrm{A,B,C}}}{\mathrm{d}t} &= \overbrace{\frac{u_{\mathrm{b}_{1,2,3}} + u_{\mathrm{b}_{4,5,6}} + u_{\mathrm{b}_{7,8,9}}}{3} + u_0}^{u_{\mathrm{eq_{A,B,C}}}} \\ &\quad + \frac{L_{\mathrm{br}}}{3}\frac{\mathrm{d}i_{\mathrm{A,B,C}}}{\mathrm{d}t} \end{aligned} \tag{14}$$

With the same procedure, the expression of the ac output voltage can be developed:

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

OJ-PEL-2021-0069

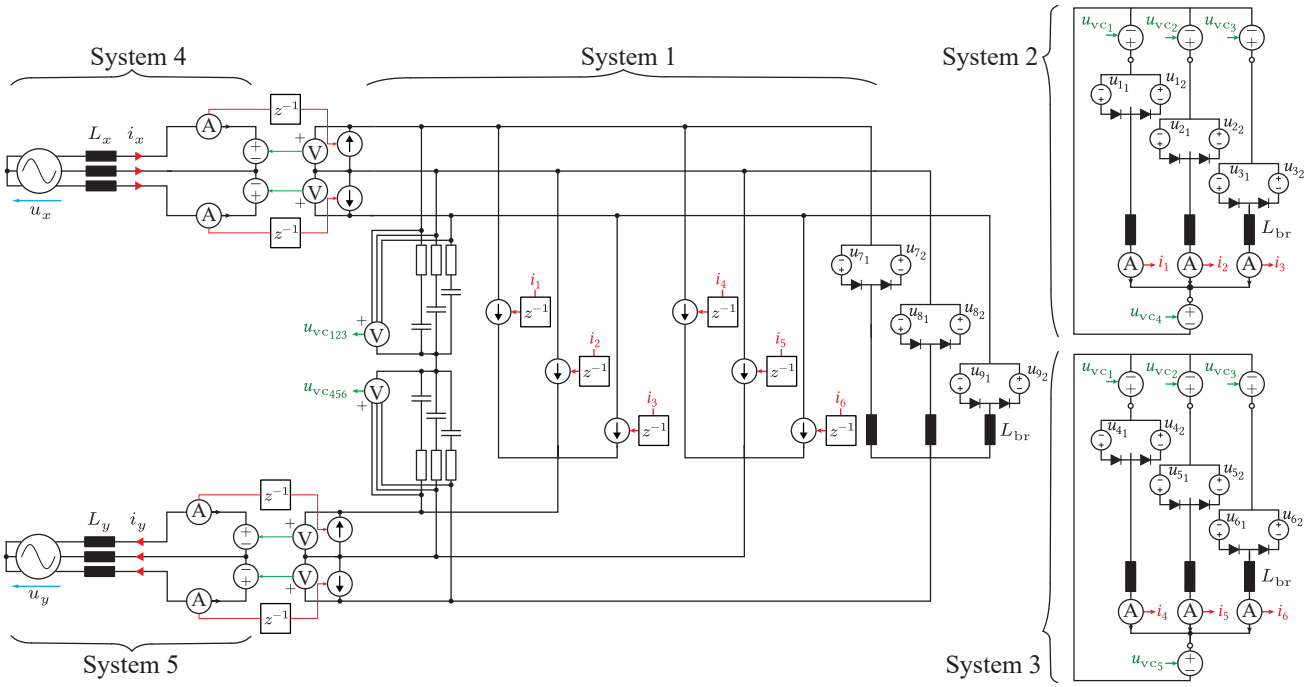

Fig. 10. Final real-time suitable model of the M3C divided into five independent circuits. System 1 incorporates the virtual circuit as well as all nine branches where the first six are replaced with ideal current sources. System 2 and 3 are the separated circuit of the branches 1 to 3 and 4 to 6 respectively. System 4 is the three phase as grid input and system 5 while shown as three phase output grid can also be replaced with a three phase machine as would be the case for a PHSP.

$$u_{\mathrm{g}_{1,2,3}} + L_{\mathrm{y}}\frac{\mathrm{d}i_{1,2,3}}{\mathrm{d}t} = -\overbrace{\left(\frac{u_{\mathrm{b}_{1,4,7}} + u_{\mathrm{b}_{2,5,8}} + u_{\mathrm{b}_{3,6,9}}}{3} + u_0\right)}^{u_{\mathrm{eq}_{1,2,3}}} - \frac{L_{\mathrm{br}}}{3}\frac{\mathrm{d}i_{1,2,3}}{\mathrm{d}t} \tag{15}$$

With both (14) and (15), an equivalent model of the analyzed M3C as seen from the input and output ac terminals can be developed. Thereafter, the dynamics of the M3C input and output ac currents can be described and compared to the dynamics of the initial model shown in Fig. 6 to validate the usage of the model shown in Fig. 10.

$$L_{\Sigma_x}\frac{\mathrm{d}i_{\mathrm{A}}}{\mathrm{d}t} = \frac{2u_{\mathrm{g_A}} - u_{\mathrm{g_B}} - u_{\mathrm{g_C}}}{3} - \frac{2u_{\mathrm{eq_A}} - u_{\mathrm{eq_B}} - u_{\mathrm{eq_C}}}{3} \tag{16}$$

$$L_{\Sigma_x}\frac{\mathrm{d}i_{\mathrm{B}}}{\mathrm{d}t} = \frac{2u_{\mathrm{g_B}} - u_{\mathrm{g_A}} - u_{\mathrm{g_C}}}{3} - \frac{2u_{\mathrm{eq_B}} - u_{\mathrm{eq_A}} - u_{\mathrm{eq_C}}}{3} \tag{17}$$

$$L_{\Sigma_x}\frac{\mathrm{d}i_{\mathrm{C}}}{\mathrm{d}t} = \frac{2u_{\mathrm{g_C}} - u_{\mathrm{g_A}} - u_{\mathrm{g_B}}}{3} - \frac{2u_{\mathrm{eq_C}} - u_{\mathrm{eq_A}} - u_{\mathrm{eq_B}}}{3} \tag{18}$$

$$L_{\Sigma_y}\frac{\mathrm{d}i_1}{\mathrm{d}t} = \frac{2u_{\mathrm{g}_1} - u_{\mathrm{g}_2} - u_{\mathrm{g}_3}}{3} - \frac{2u_{\mathrm{eq}_1} - u_{\mathrm{eq}_2} - u_{\mathrm{eq}_3}}{3} \tag{19}$$

$$L_{\Sigma_Y}\frac{\mathrm{d}i_2}{\mathrm{d}t} = \frac{2u_{\mathrm{g}_2} - u_{\mathrm{g}_1} - u_{\mathrm{g}_3}}{3} - \frac{2u_{\mathrm{eq}_2} - u_{\mathrm{eq}_1} - u_{\mathrm{eq}_3}}{3} \tag{20}$$

$$L_{\Sigma_y}\frac{\mathrm{d}i_3}{\mathrm{d}t} = \frac{2u_{\mathrm{g}_3} - u_{\mathrm{g}_1} - u_{\mathrm{g}_2}}{3} - \frac{2u_{\mathrm{eq}_3} - u_{\mathrm{eq}_1} - u_{\mathrm{eq}_2}}{3} \tag{21}$$

Where $L_{\Sigma_x} = L_{\mathrm{x}} + \frac{L_{\mathrm{br}}}{3}$ for the equivalent circuit seen from the input ac side, and $L_{\Sigma_y} = L_{\mathrm{y}} + \frac{L_{\mathrm{br}}}{3}$ for the equivalent circuit seen from the output ac side. Equations (16) to (21) are equivalent as the equations from the initial model seen in Fig. 6, thus this initial model can be interchanged with the one from Fig. 10, effectively reducing the number of state space matrices to 3×2^6, reducing the step size as to allow the usage of small scale RT Boxes.

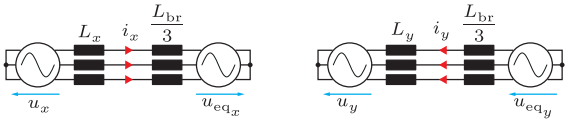

Fig. 11. Equivalent circuit of the split M3C model as seen from the input terminals shown on the left and from the output terminals shown on the right.

D. Tuning of the VC

To enable the splitting of the model, the addition of the VC is required, nevertheless, proper sizing of the capacitance is required to ensure its negligible influence on the converter terminal currents. To limit the current flowing through the VC, the smallest possible value of capacitance should be chosen, however this is not the only condition to be fulfilled. The addition of the VC might trigger resonance in the circuit and a thorough analysis of the system is needed to avoid such resonances by proper sizing of the VC. The resonant frequencies of the system can be obtained from the eigenvalues of the state matrix A for a specific circuit state, and to ensure stability the discretization time step should be at least ten times higher than the shortest of all resonant periods of the system [31].

Determining the shortest resonant period of the circuit shown in Fig. 10 analytically would require the development of all 3×2^6 possible A state matrices and analyze their

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

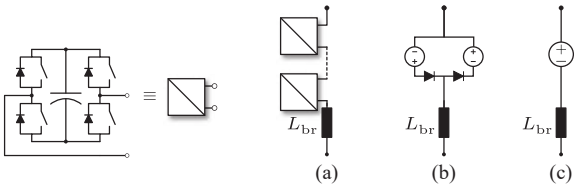

Fig. 12. Equivalent branch model for (a) the real converter using a cascaded connection of full bridge cells (b) the real time model using two controlled voltage sources and two diodes (c) the tuning of the virtual circuit using a single controlled voltage source

eigenvalues. While this method ultimately leads to the optimal solution of the VC value, it requires a high number of iterations to reach it. For this reason a simplification of the circuit seen in Fig. 10 is done to reduce the number of state space matrices.

The equivalent capacitance across the terminals of a branch changes with the switching state of each cell, however the analysis of the resonant frequency being orders of magnitudes higher than the operating frequency of the converter, these capacitance variation can be considered constant for several discretization steps. Similarly, due the fact that the dynamics of the cell voltage is lower than the discretization time step allows for the assumption that the variation of this voltage is negligible between the discretization steps. Additionally, in the model shown in Fig. 10, the equivalent electrical circuit between the terminals of the branch can be simplified to a single voltage source, as one of the diodes is always in blocking state. For these reasons the equivalent branch model that can be considered for the analysis of the resonant frequency can be simplified to a simple series connection of a voltage source and the branch inductor, which is also referred to as averaged model and shown in Fig. 12. Even if not accurate in simulation of the M3C, this model allows for an accurate calculation of the VC with the advantage of having only a single state space matrix.

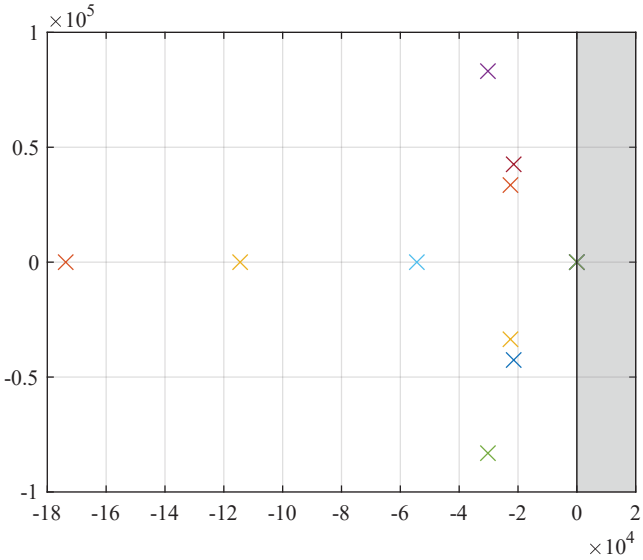

Fig. 13. Position of the poles of the system shown in Fig. 10 using the previously found values for the virtual circuit, $C_v = 850$ nF and $R_v = 35\ \Omega$. All 12 poles are situated in the left half-plane

In order for the split model to be valid, following conditions have to be fulfilled regarding the simplified model described above:

1 All the poles of the system must be located in the Left Half-Plane (LHP).
2 The low frequency current through the virtual circuit is limited to 1% of the nominal grid current.
3 The shortest resonant period is at least ten times bigger than the simulation time step.

Simply using a VC might not allow to fulfill all the conditions above, thus a VR is added with the aim to damp resonances while keeping a low capacitance value. With the system being of 12^{th} order and having two degrees of freedom, namely the value of the VR and the VC, solving the optimization problem analytically seems to be out of reach. For this reason a simple algorithm is developed which sweeps numerically values for VC and VR, and for each combination checks all the above mentioned conditions. As multiple sets of VR and VC fulfill all the above mentioned conditions, the set with the highest impedance is chosen as to have the lowest possible current flowing through the virtual circuit. The final result that is used is this work is:

$$C_v = 850\ \text{nF} \tag{22}$$
$$R_v = 35\ \Omega \tag{23}$$

IV. Model verification using HIL simulations

For the results presented in this section, the cell voltage of the simulated M3C is set to 680 V with 8 cells per branch, resulting in a 5440 V nominal branch voltage. The nominal voltage of the input grid is 3.3 kV, and the output terminals of the M3C are connected to a 2.5 kV machine with a nominal speed of 500 rpm and two pole pairs. The cell capacitance is set to $C_{\text{cell}} = 2.25$ mF and the branch inductances and resistances are set to $L_{\text{br}} = 2.5$ mH and $R_{\text{br}} = 66.4$ mΩ respectively. A spectral analysis of the currents flowing in the virtual capacitance for the different scenarios simulated in this paper is used to validate the equivalence between the M3C model implemented on HIL and the actual converter circuit. This current should fulfill the previously mentioned condition to be below 1% of the nominal ac input grid current, and this analysis should reveal the high frequency nature of the current which is filtered out in the control loop of the HIL. This spectral analysis allows to determine the influence of the virtual circuit with the parameters defined in (22) and (23) on the terminals of the converter.

The control of the machine side terminals of the converter is done using the vector control scheme following a given speed reference. The grid side converter ac terminal quantities are controlled in $\alpha\beta$-frame controlling the power to match the requirements of the machine and keep the average energy within the converter constant. The circulating currents used to balance the energy within the converter are controlled using the direct arm energy control as explained in [32], which as the name suggests creates a energy reference for each branch and through mathematical transformations, eliminates its influence on either input or output terminals.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

OJ-PEL-2021-0069

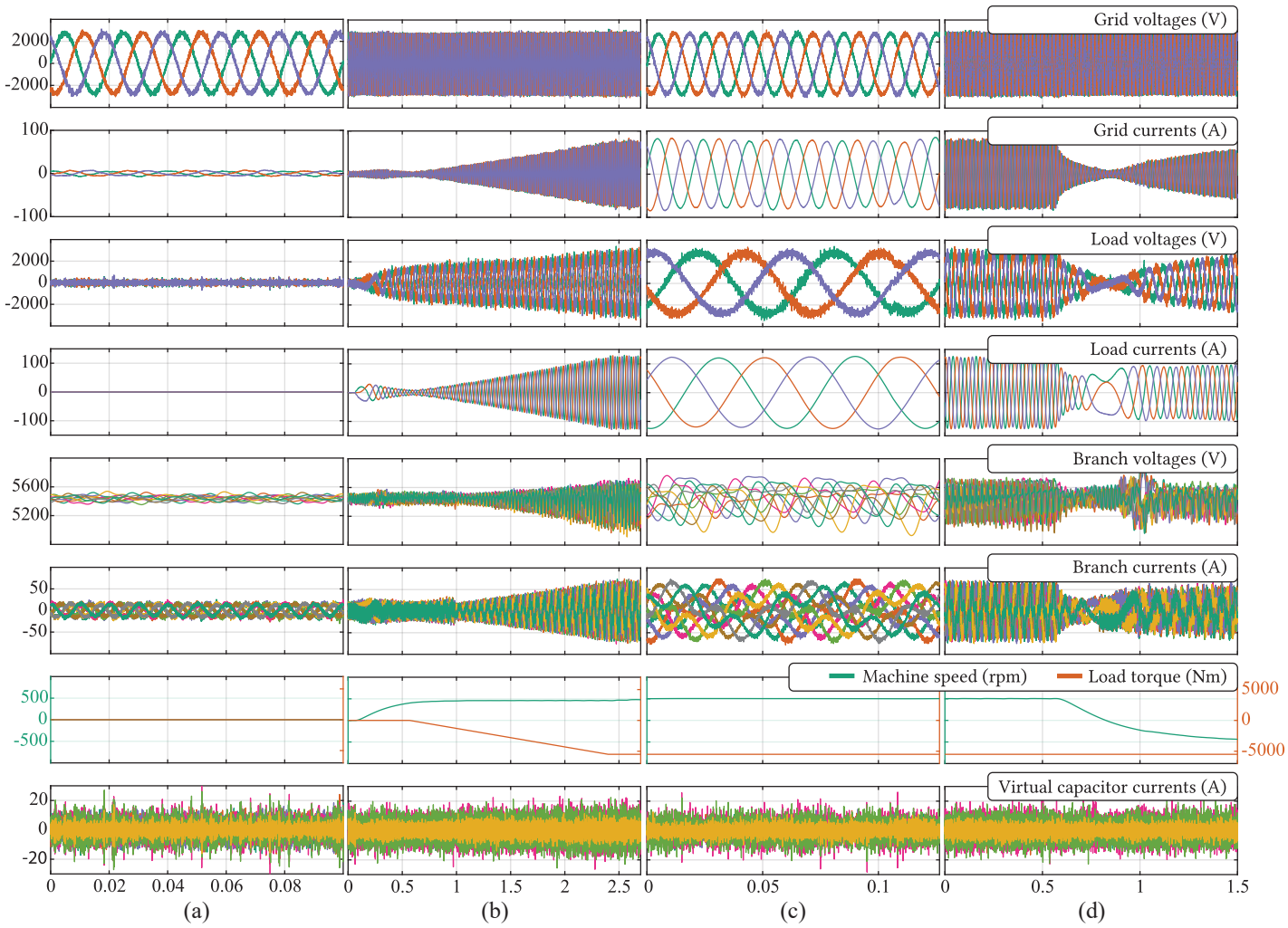

Fig. 14. Results of the HIL simulation showing input grid voltage and current, machine voltage and currents, branch voltages and currents, machine speed and torque as well as the currents through the virtual capacitances. (a) shows the idling stage of the converter without any output current. (b) shows the speed up and loading of the machine. (c) shows operation of the machine at full load and speed. (d) shows the speed reversal of the machine under full load.

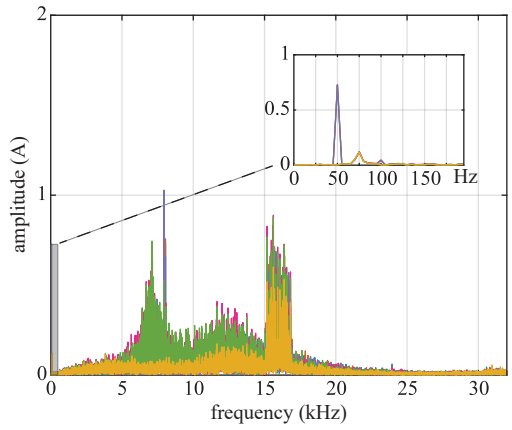

Fig. 15. Spectral analysis of the six currents passing through the virtual capacitances in idling mode, including a zoom on the amplitude for the frequency range from 0 Hz to 200 Hz. In these low frequency ranges, the three overlapping peaks at 50 Hz on the input side are staying below 0.73 A, and no peaks are observed at the nominal machine frequency as no output voltage is generated.

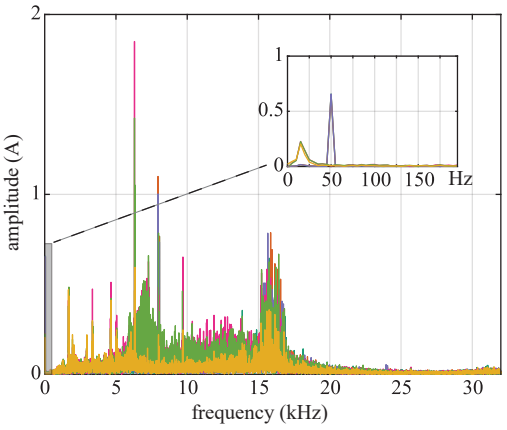

Fig. 16. Spectral analysis of the current passing through the virtual capacitances in full load mode, including a zoom on the amplitude for the frequency range from 0 Hz to 200 Hz. In these low frequency ranges, the three overlapping peaks at 50 Hz on the input side as well as the three overlapping peaks at 16.6 Hz are staying below 0.66 A and 0.23 A respectively.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/OJPEL.2021.3130996, IEEE Open Journal of Power Electronics

OJ-PEL-2021-0069

Fig. 14(a) shows the idling operating mode of the converter, where all cells are charged and balanced, but without generating any output voltage at the machine side. Without active power output, small reactive input currents are required to allow the balancing of the energies between the branches. However, using Phase Shifted Carrier (PSC) modulation, additional circulating currents are required as to keep the energy between the cells of a given branch balanced. These currents at double the fundamental grid input frequency and with an amplitude of 15 A are canceling each other out on both the input and output terminals.

A spectral analysis of the currents flowing through the VC during the idling operating mode is shown in Fig. 15 with an additional zoom on the frequency components below 200 Hz. Using (9) as well as (10) as well as the fact that there are no output voltages, it is straightforward to conclude that the first peak in the spectral analysis occurs at the fundamental input grid frequency, 50 Hz. The amplitude of this fundamental frequency component is $i_{\mathrm{Cv}}(f_{\mathrm{g1}}) = 0.73$ A which is around 0.9% of the nominal input ac current, thus within the predefined limits and not affecting the terminal currents. For the high frequency components, two main peaks stand out, namely around 8 kHz and 16 kHz, both related to the apparent branch switching frequency and thus a multiple of this frequency defined by: $Nf_{\mathrm{sw}} = 8$ kHz.

Fig. 14(b) shows the pumping start-up sequence, accelerating the machine to nominal speed, namely 500 rpm and applying the full 5500 Nm load torque. The previously used reactive input currents are reduced to zero as soon as the amplitude of the output voltage is high enough to allow balancing of the branch energies. Similarly, once the input currents reaches 10 A, the circulating currents at 15 A and fundamental frequency are eliminated as the current flowing through the branch is high enough to allow balancing of the cells within the branch.

Fig. 14(c) shows the operation of the machine under full load with the corresponding spectral analysis of the VC currents shown in Fig. 16. The presence of the 16.6 Hz output voltage component results in the peak at the same frequency of the VC currents as shown in the spectral analysis. With an amplitude of $i_{\mathrm{Cv}}(f_{\mathrm{g2}}) = 0.23$ A, which is less than 0.25% of the nominal output currents, these terminal currents remain unaffected. Compared to the VC current peak in idling mode at 50 Hz, the peak at this same frequency during full load operation is reduced to $i_{\mathrm{Cv}}(f_{\mathrm{g1}}) = 0.66$ A which is around 0.75% of the nominal input ac current. This reduction is explained by the elimination of the common mode voltage, which was previously used to balance the energy between the branches, and not needed when there is an active power flow through the converter, as is the case in this mode.

Fig. 14(d) shows a speed reversal of the electrical machine under full load, similar to a change in operation from pumping to turbine mode in a PHSP. The energy of the branches remain balanced throughout the process, and the VC current is not significantly different to the previous operating modes, thus still having a negligible influence regarding its low frequency components on the terminals of the converter.

V. Conclusion

This paper presents and develops a distributed model of the M3C for the deployment on small-scale simulators using the VC concept. This modeling approach reduces significantly the number of state-space matrices describing the system, which leads to a reduction in simulation time step, thus making deployment of a complex system such as the M3C on small-scale simulators relying on the use of state-space matrices the main focus of this paper. Proper tuning of the VC and VR achieved through a sweeping algorithm, as explained in this paper, allows for a negligible influence of the added circuitry on the terminals as well as on the circulating currents of the converter concerning the low frequency signals. The high frequencies being filtered in the control loop, are not affecting the operation of the M3C regarding the verification of the controllers and their deployed control algorithm, making it a suitable splitting method for HIL systems designed for this purpose. Using the RT Box in the above presented HIL system, the results demonstrate this negligible influence regarding low frequency currents by spectral analysis and demonstrating the validity of this splitting approach.

Acknowledgment

The results presented in this paper are a part of the Hydropower Extending Power System Flexibility (XFLEX HYDRO) project that has received funding from the European Union's Horizon 2020 research and innovation programme under grand agreement No 857832.

References

[1] E. Comission. (). "2030 climate & energy framework." https://ec.europa.eu/clima/policies/strategies/2030_en [Accessed on 14.06.2021].

[2] A. Iwadachi, K. Tani, and K. Aguro, "The design of adjustable-speed pump-turbine modified from existing constant-speed on okutataragi power station," in *2016 19th International Conference on Electrical Machines and Systems (ICEMS)*, 2016, pp. 1–4.

[3] A. Vargas-Serrano, A. Hamann, S. Hedtke, C. M. Franck, and G. Hug, "Economic benefit analysis of retrofitting a fixed-speed pumped storage hydropower plant with an adjustable-speed machine," in *2017 IEEE Manchester PowerTech*, 2017, pp. 1–6.

[4] P. Bontemps, N. Hugo, and D. Dujic, "Flexibility enhancements in pumped hydro storage power plants through variable speed drives," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 1820–1825.

[5] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, 2003, 6 pp. Vol.3-.

[6] M. Basić, A. Schwery, and D. Dujić, "Highly flexible indirect modular multilevel converter for high power pumped hydro storage plants," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 5290–5295.

[7] S. Milovanović and D. Dujić, "On facilitating the modular multilevel converter power scalability through branch paralleling," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 6875–6882.

[8] S. Milovanovic and D. Dujic, "On power scalability of modular multilevel converters: Increasing current ratings through branch paralleling," *IEEE Power Electronics Magazine*, vol. 7, no. 2, pp. 53–63, 2020.

[9] M. Vasiladiotis, R. Baumann, C. Häderli, and J. Steinke, "Igct-based direct ac/ac modular multilevel converters for pumped hydro storage plants," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 4837–4844.

[10] A. Christe. (). "Direct mmc for converter-fed synchronous machines." https://www.epfl.ch/labs/pel/wp-content/uploads/2021/05/2021.05.11_IEEE_Webinar_Direct-MMC-Control_export.pdf [Accessed on 06.07.2021].

[11] W. Li and J. Bélanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time hil test bench," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2401–2409, 2016.

[12] G. Li, D. Zhang, Y. Xin, S. Jiang, W. Wang, and J. Du, "Design of mmc hardware-in-the-loop platform and controller test scheme," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 2, pp. 143–151, 2019.

[13] S. Milovanovic, I. Polanco, M. Utvic, and D. Dujic, "Flexible and efficient mmc digital twin realized with small-scale real-time simulators," *IEEE Power Electronics Magazine*, vol. 8, no. 2, pp. 24–33, 2021.

[14] S. Dennetière, H. Saad, B. Clerc, E. Ghahremani, W. Li, and J. Bélanger, "Validation of a mmc model in a real-time simulation platform for industrial hil tests," in *2015 IEEE Power Energy Society General Meeting*, 2015, pp. 1–5.

[15] Y. Wang, C. Liu, H. Liu, B. Ling, and G. Li, "Real-time simulation model and experimental test bench for modular multilevel converter," in *2018 2nd IEEE Conference on Energy Internet and Energy System Integration (EI2)*, 2018, pp. 1–6.

[16] M. R. Lotz, M. Kohn, T. Öznur, and M. Könemund, "Hardware-in-the-loop setup for low voltage modular multilevel converter control development," in *2020 IEEE 29th International Symposium on Industrial Electronics (ISIE)*, 2020, pp. 126–133.

[17] C. Lin, D. Liu, X. Wu, Z. He, W. Wang, and W. Li, "Setup and performance of a combined hardware-in-loop and software-in-loop test for mmc-hvdc control and protection system," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015, pp. 1333–1338.

[18] W. Wu, X. Wu, L. Jing, and J. Li, "Design of modular multilevel converter hardware-in-loop platform based on rt-lab," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 2350–2355.

[19] PLEXIM, "The simulation platform for power electronics systems," [Online]. Available: https://www.plexim.com/sites/default/files/rtboxmanual.pdf.

[20] T. HIL, *Typhoon hil402*. [Online]. Available: https://www.typhoon-hil.com/doc/products/Typhoon-HIL402-brochure.pdf.

[21] S. Milovanovic, M. Luo, and D. Dujic, "Virtual capacitor concept for effective real-time mmc simulations," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–8.

[22] M. Utvic, I. P. Lobos, and D. Dujic, "Low voltage modular multilevel converter submodule for medium voltage applications," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1–8.

[23] A. J. Korn, M. Winkelnkemper, P. Steimer, and J. W. Kolar, "Direct modular multi-level converter for gearless low-speed drives," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–7.

[24] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, 2015.

[25] PLEXIM, *The simulation platform for power electronics systems*, English, version Version 4.5, 830 pp.

[26] "Modeling and simulation," in *Design, Control and Application of Modular Multilevel Converters for HVDC Transmission Systems*. John Wiley and Sons, Ltd, 2016, ch. 6, pp. 272–282.

[27] H. Saad, J. Peralta, S. Dennetière, J. Mahseredjian, J. Jatskevich, J. A. Martinez, A. Davoudi, M. Saeedifard, V. Sood, X. Wang, J. Cano, and A. Mehrizi-Sani, "Dynamic averaged and simplified models for mmc-based hvdc transmission systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 3, pp. 1723–1730, 2013.

[28] J. Xu, A. M. Gole, and C. Zhao, "The use of averaged-value model of modular multilevel converter in dc grid," *IEEE Transactions on Power Delivery*, vol. 30, no. 2, pp. 519–528, 2015.

[29] W. Li and J. Bélanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time hil test bench," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2401–2409, 2016.

[30] J. Allmeling and N. Felderer, "Sub-cycle average models with integrated diodes for real-time simulation of power converters," in *2017 IEEE Southern Power Electronics Conference (SPEC)*, 2017, pp. 1–6.

[31] Z. Xu, S. Wang, F. Xing, and H. Xiao, "Study on the method for analyzing electric network resonance stability," *Energies*, vol. 11, no. 3, 2018. [Online]. Available: https://www.mdpi.com/1996-1073/11/3/646.

[32] M. Utvić and D. Dujić, "Generalized theory on direct arm energy control in modular multilevel converters," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 4, pp. 388–399, 2020.