EPFL

Thèse n° 9096

Deep-UV approaches and printing of indium zinc oxide thin-film transistors targeting their processing on thermosensitive substrates

Présentée le 10 décembre 2021

Faculté des sciences et techniques de l'ingénieur
Laboratoire des microsystèmes pour les technologies spatiales
Programme doctoral en microsystèmes et microélectronique

pour l'obtention du grade de Docteur ès Sciences

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École polytechnique fédérale de Lausanne

2021

Omnia quae nunc vetustissima creduntur, nova fuere.

– Publio Cornelio Tacito

Acknowledgements

I would like to express my most sincere gratitude to Dr. Danick Briand, who gave me the precious opportunity to be a member of his research group and to be involved in this challenging yet stimulating topic. I really appreciated your passion for science, your suggestions for improvement, and the scientific discussion we had in these four years. Thank you for your availability, your guidance throughout my doctoral study, and your continued support.

I am grateful to the members of my Ph.D. jury, Prof. Jürgen Brugger, Prof. Guillermo Villanueva, Dr. Edsger Smits, and Dr. Nenad Marjanovic, for having accepted to read and evaluate this thesis.

I would like to thank all the colleagues of the FOxIP project, especially Dr. Sami Bolat and Dr. Yaroslav Romanyuk, for their collaboration and the proficient talks we had these years.

Special thanks go to Saleem Khan and Alexis Marette, who helped me at the beginning of this journey with their guidance and their friendship.

A mention for my office mates Ryan van Dommelen and Silvia Demuru, it was great to spend the time in the office between scientific discussions and laugh, it really made this journey easier and noisier.

A huge thanks go to Jaemin Kim, a great colleague, always available and ready to help. I'm really grateful for our scientific discussions and your support, it really allowed me to reach this goal.

Working at LMTS, Microcity, EPFL has been a great experience, mainly thanks to the lab's people and their spirit. I would like to thank Juan Zarate, Christine de Saint-Aubin, Samuel Schlatter, Xiaobin Ji, Francesca Sorba, Mathias Imboden, Alexandre Poulin, Ulas Adiyan, Rubaiyet Haque, Vito Cacucciolo, Edouard Leroy, Jean-Baptiste Chossat, Krishna Manaswi Digumarti, Robert Marius Hennig, Ronan Julien Hinchet, Djen Timo Kühnel, Brince Paul Kunnel, Michael James Henry Smith, Fabio Beco Albuquerque, Valentin Py, Sylvain Thomas Schaller, Giulio Grasso, James Alec Pierce Bourely, Nicolas Francis Fumeaux, Min Gao and Morgan Monroe. (I hope I didn't forget anyone)

I would also like to thank Prof. Herbert Shea that made such an ideal working environment possible. Moreover, a special thank goes to the best-secretary-ever Myriam Poliero, for her kindness and availability.

Thanks to all my friends, scattered all over Italy and the globe, Matteo, Luca, Andrea, Tommaso, Flavio, Giuseppe, Gianmarco, Paolo, Giovanni, Ilario, Marco….(I would never finish) Thanks to Leandro for the long talks and the support during these years. Grazie Champ.

I'm really grateful to my family, my parents Fabrizio and Michelina, that always supported me, and my sisters, Giulia and Barbara. Thanks also to my grandma, my grandpa, all my uncles, cousins, to Papzzoland… Thank you all for your love.

Last but not least, my wife Elena, thank you. I feel really blessed to have you always on my side.

Grazie a tutti,

Alessio

Neuchâtel, 24 September 2021

Abstract

Novel metal-oxides (MO_x) semiconductors for thin-film transistors (TFTs) are being developed as they can offer superior electric performances over organic-based counterparts. MO_x TFTs processed on foil could be exploited in smart labels as RFID and NFC tags, flexible wearable devices, interfaced with or like sensors for personalized healthcare, fulfilling the demand for device integration in daily life products. However, their current processing conditions do not enable large-area manufacturing on commonly used substrates in printed electronics, such as thermosensitive polyethylene-based foils, preventing their cost-effective diffusion in consumer and logistic products. This thesis addresses the solution processing at low temperature (<200°C), via deep-UV enhanced synthesis, of metal-oxide-based TFTs and their additive manufacturing, including ink development and printing, and TFT fabrication and characterization.

First, we present bottom gated TFTs made from a novel, fully solution-processed IZO/AlO_x-based stack. On silicon, we studied how thermally annealed IZO (200–450°C) interacts with high-k AlO_x-based spin-coated and vacuum-deposited dielectrics by evaluating TFT performances and IZO chemical composition. The optimal material match in the sol-gel-based stack processed at 450°C resulted in superior interface and TFTs overperforming their ALD counterparts, μ~26cm^2/Vs, I_{on}/I_{off}~10^6 versus μ~4cm^2/Vs, I_{on}/I_{off}~10^4. Finally, fully solution-processed metal-oxide TFTs at high temperature were achieved by implementing photolithography, resulting in high-performance devices with μ~68cm^2/Vs and I_{on}/I_{off} ratio>10^9, comparable with state-of-the-art sputtered devices.

Then, we implemented a DUV-enhanced protocol for the synthesis of spin-coated IZO semiconductor and printed AlO_x/$YAlO_x$ dielectric at a low temperature of 200°C. Prolonged DUV exposure (1h) and thermal annealing (3h) yielded TFTs with μ as high as ~40cm^2/Vs. By studying the effects of the process parameters on IZO chemical composition and TFTs characteristics, the IZO synthesis time was shortened to ~1h while maintaining excellent performances such as μ~16cm^2/Vs, I_{on}/I_{off}>10^8, and SS<100mV/dec. Ultimately, we demonstrated a protocol as short as 10min at 200°C capable of yielding TFTs with mobility of ~3cm^2/Vs, I_{on}/I_{off}>10^8, and SS<100mV/dec, stable after one year without passivation.

Aiming at further reducing the thermal budget, we explored an in-situ DUV excimer synthesis approach and inkjet printing of the MO_x functional layers. First, DUV excimer was implemented on the AlO_x/$YAlO_x$ dielectric, demonstrating at a very low processing temperature of 130°C, capacitors (MIM) exhibiting leakage currents of about 10^{-7}A/cm at 1MV/cm. We proposed and validated a process flow to integrate these MIMs on flexible foil, resulting in operative MIMs with a printed AlO_x/$YAlO_x$ dielectric on PEI foil. We developed an IZO ink and studied composition influences on printability and TFT performance when synthesized at temperatures below 200°C. The combination of DUV excimer treatment at 180°C with an optimized IZO ink formulation and printing process resulted in TFTs with μ>1cm^2/Vs. Finally, thermally annealed TFTs with printed MO_x functional stack exhibiting μ>4cm^2/Vs were proven. Process tuning is still required to achieve fully printed IZO-AlO_x/$YAlO_x$ TFTs on foil, but the preliminary results proved the suitability of both printing and synthesis approaches with cost-effective polymeric substrates.

Keywords

deep-UV, indium zinc oxide, low temperature, metal oxide, printing, solution processing, thin-film transistor, flexible substrate

Sommario

Nuovi semiconduttori a ossidi metallici (MO_x) per transistor a film sottile (TFT),vengono oggigiorno sviluppati grazie alle superiori prestazioni elettriche rispetto alle controparti a base organica. I MO_x TFT fabricati su pellicola potrebbero essere sfruttati in etichette intelligenti come tag RFID e NFC, in dispositivi indossabili flessibili, come sensori personalizzati, soddisfacendo la domanda di funzionalità extra nei prodotti della vita quotidiana. Tuttavia, le loro attuali condizioni di fabbricazione non consentono la produzione in grande scala e a basso costo su substrati comunemente usati nell'elettronica stampata, come le plastiche termosensibili a base di polietilene, impedendone la diffusione nei prodotti di consumo e logistici. Questa tesi tratta la fabbricazione di TFT a base di ossido di metallo con tecniche additive a bassa temperatura (<200°C) tramite sintesi basata su UV profondo (DUV), compreso lo sviluppo di inchiostro e la stampa, fabbricazione e caratterizzazione dei dispositivi.

In primo luogo, presentiamo i TFT realizzati, basati su strati di IZO/AlO_x processati in soluzione. Su silicio, abbiamo studiato come IZO trattato termicamente (200-450°C) interagisce con dielectrico ad alto k basato su alumina,depositato con spin-coating e con tecniche sotto vuoto (ALD), valutando le prestazioni dei TFT e composizione chimica dell'IZO. Rispetto alle controparti con dielectrico ALD, l'abbinamento ottimale dei materiali nello stack basato su sol-gel ha portato a un'interfaccia superiore e a TFT piu performanti, μ~26cm^2/Vs, I_{on}/I_{off}~10^6 rispetto a μ~4cm^2/Vs, I_{on}/I_{off}~10^4. Infine, aplplicando fotolitografia, i TFT ad ossido di metallo completamente lavorati in soluzione ad alta temperatura hanno raggiunto alte prestazioni con μ~68cm^2/Vs e I_{on}/I_{off}>10^9, paragonabili allo stato dell'arte di dispositivi standard.

Poi, abbiamo realizzato un protocollo per la sintesi dell' IZO rivestito per rotazione e del dielettrico AlO_x/$YAlO_x$ stampato, ad una bassa temperatura di 200°C grazie alla sintesi con DUV a bassa temperatura. Prolungate esposizione DUV (1h) e ricottura termica (3h) hanno ottenuto TFT con μ fino a ~40cm^2/Vs. Studiando gli effetti dei parametri di processo sulla composizione chimica IZO e le caratteristiche TFTs, il tempo di sintesi IZO è stato ridotto a ~1h mantenendo eccellenti prestazioni come μ~16cm^2/Vs, I_{on}/I_{off}>10^8, e SS<100mV/dec. In definitiva, abbiamo dimostrato un protocollo breve come 10min a 200°C in grado di produrre TFT, stabili oltre un anno anche senza passivazione, con mobilità di ~3cm^2/Vs, I_{on}/I_{off}>10^8, e SS<100mV/dec.

Al fine di ridurre ulteriormente l'impatto termico della sintesi, abbiamo implementato un approccio di sintesi con DUV excimer e temperature applicate simultanemente ("in-situ"), con MO_x stampati ad inchiostro. In primo luogo, DUV in-situ è stato applicato sul dielettrico AlO_x/$YAlO_x$, realizzando a bassa temperature (130°C), condensatori (MIM) con basse correnti di perdita, circa 10^{-7}A/cm a 1MV/cm. Abbiamo proposto e convalidato un processo produttivo per integrare questi MIM su un foglio flessibile, ottenendo MIM operativi con un dielettrico AlO_x/$YAlO_x$ stampato su foglio di PEI. Abbiamo sviluppato un inchiostro IZO e studiato come la sua composizione influisce sulla stampabilità e sullele prestazioni dei transitor quando sintetizzati a temperature inferiori a 200°C. La combinazione del trattamento DUV excimer a 180°C con una formulazione ottimizzata di inchiostro IZO ha portato a TFT stampati con μ>1cm^2/Vs. Infine, sono stati dimostrati TFT con ossidi metallici entrambi stampati, trattati termicamente, con μ>4cm^2/Vs. Una messa a punto del processo è ancora necessaria per ottenere TFT IZO-AlO_x/$YAlO_x$ completamente stampati su lamina, ma i risultati preliminari hanno dimostrato l'idoneità di entrambi gli approcci di stampa e di sintesi con i convenienti substrati polimerici.

Parole chiave

UV profondo, transistor a film sottile, processi a bassa temperatura, stampa, ossido di indio e zinco, substrati flessibili

Résumé

De nouveaux semi-conducteurs à oxyde métallique (MO_x) pour les transistors à couche mince (TFT) sont actuellement développés en raison de leurs performances électriques supérieures à celles de leurs homologues à base organique. Les TFTs MO_x fabriqués sur substrats souples pourraient être exploités dans des étiquettes intelligentes comme les tags RFID et NFC, ou interfacés avec ou comme capteur appliqués aux soins de santé personalisés, répondant ainsi une demande pour une intégration de fonctionnalités supplémentaires dans les produits quotidiens. Toutefois, leurs conditions de fabrication actuelles ne permettent pas leur production à grande échelle et à faible coût sur des substrats couramment utilisés en électronique imprimée, tels que les plastiques thermosensibles à base de polyéthylène, ce qui empêche leur utilisation généralisée dans les produits de consommation et dans la logistique. Cette thèse traite de la fabrication et de la caractérisation de TFTs à base d'oxydes métalliques à basse température (<200°C) en employant des techniques additives de mise en forme et une synthèse des basée sur une exposition à des UV profonds (DUV).

Premièrement, nous présentons des TFTs fabriqués à partir d'un empilement original de couches d'IZO/AlO_x synthétisés par un procédé sol-gel. Sur silicium, nous avons étudié comment le semiconducteur IZO traité thermiquement (200-450°C) interagit avec des diélectriques de grille à base d'alumine à constante diélectrique élevée, déposés par dépôt à la tournette et en phase vapeur sous vide (ALD). Par rapport au diélectrique formé par ALD, l'empilement des oxydes fonctionnels synthétisés que par sol-gel à 450°C a induit une qualité d'interface résultant en des TFT plus performants, μ~26cm^2/Vs, I_{on}/I_{off}~10^6 par rapport à μ~4cm^2/Vs, I_{on}/I_{off}~10^4. Enfin, avec une structuration par photolithographie, les TFTs composés de ces mêmes oxydes métalliques synthétisés à haute température ont présenté des performances élevées avec une mobilité ~68cm^2/Vs et un ratio I_{on}/I_{off}>10^9, comparables à l'état de l'art.

Ensuite, nous avons développé un protocole pour la synthèse à une température minimale de 200°C par exposition aux UV profonds du semiconducteur IZO et des diélectriques AlO_x/$YAlO_x$. Une exposition aux DUV (1h) et un traitement thermique (3h) prolongés ont permis d'obtenir des TFTs avec une mobilité atteignant ~40cm^2/Vs. Suite à une étude de l'effet des différents paramètres sur la composition chimique de l'IZO et les caractéristiques des TFTs, le temps de synthèse de l'IZO a été réduit à ~1h tout en maintenant d'excellentes performances telles que μ ~16cm^2/Vs, I_{on}/I_{off}>10^8, et SS <100mV/dec. Finalement, nous avons démontré un protocole réduit à 10min permettant la production à 200°C de TFTs stables sur une année, cela même sans passivation, présentant une mobilité de ~3cm^2/Vs, un ratio I_{on}/I_{off}>10^8, et un SS<100mV/dec.

Afin de réduire davantage le budget thermique de la synthèse, nous avons mis en œuvre une approche in-situ, combinant DUV excimère et chauffage, appliquées à des couches MO_x imprimées par jet d'encre. Tout d'abord, ce procédé a été appliqué sur le diélectrique AlO_x/$YAlO_x$, permettant la fabrication à basse température (130°C) de condensateurs (MIM) ayant de faibles courants de fuite, environ 10^{-7}A/cm à 1MV/cm. Nous avons proposé et validé un procédé de fabrication de ces MIMs sur un substrate souple (PEI), avec la réalisation de MIMs composés d'un empilement AlO_x/$YAlO_x$ imprimé. Nous avons développé une encre IZO et étudié comment sa composition affecte son impression et les performances du transistor pour une synthèse d'IZO à des températures inférieures à 200°C. La combinaison du traitement DUV excimère avec une formulation d'encre IZO optimisée a permis d'imprimer des TFTs présentant une mobilité >1cm^2/Vs. Enfin, des TFTs à base d'IZO imprimé et traité thermiquement à 180°C ont été démontrés avec une mobilité >4cm^2/Vs. Une optimization du procédé est encore nécessaire pour obtenir des TFTs faits d'IZO-AlO_x/$YAlO_x$ entièrement imprimés sur feuille, mais les résultats préliminaires ont démontré l'adéquation de l'approche avec les substrats polymèriques.

Mots-clés

UV profond, oxyde d'indium et de zinc, oxyde métallique, impression, procédés en solution à basse température, transistor à couche mince, substrat flexible

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Chapter 1 Introduction

1.1 Background and motivation

The diffusion of the internet of things (IoT) created a strong market pull for low-end electronics such as smart labels like RFID and NFC tags that provide communication and interactivity with the user once integrated within a product. Requirements such as mechanical flexibility and transparency created increasing attention on electronics on foil because it enables many novel applications concerning multiple areas such as flexible circuits, chemical sensors, and transparent and conformable wearable devices.[1–3] However, the current processing conditions, such as vacuum-based fabrication and the aggressive chemicals involved in the production, have restrained their diffusion to high-end applications onto rigid or relatively expensive and non-transparent substrates. Alternative methods have to be explored to involve cost-effective foils, like polyethylene naphthalate (PEN) or polyethylene terephthalate (PET) and paper, which will enable the ultimate diffusion of flexible electronics in consumer and logistic products. Printed electronics present a valid option as it can be cost-efficient with less material usage and less demanding infrastructures. It is a versatile approach with many parameters that can be easily varied for fast prototyping; it does not necessarily require aggressive chemistry and can be scaled for large-area manufacturing at a low cost. However, scientific and technological challenges have thus far prevented the exploitation of such manufacturing techniques for the direct processing of low-end electronics onto inexpensive substrates.

As basic blocks for many electronic applications, thin-film transistors (TFT) are employed in a broad range of emerging fields like smart labels, RFID and NFC tags, or like sensors for personalized healthcare embedded in wearable.[4] Among the different semiconducting materials used for their active channels, only organic materials and metal oxides (MO_x) can be solution-processed and printed. Organic-based TFTs (OTFTs) received some attention in the past years because of the large number of semiconductors available (among others pentacene, P3HT,[1] and fullerenes), the flexibility in semiconductor chemistry (molecular weight, composition, possible functionalization), and their processability at low temperatures, even at room temperature. However, these materials exhibit poor electrical performances, notably low mobility (~1 cm^2/Vs) and possible device instabilities, correlated to the interactions of the semiconducting channel with the environment (e.g., moisture) and its intrinsic limited charge transfer capability. MO_x materials instead are chemically stable: the quality of the charge transfer in the semiconductors, depending mainly on the purity of the metal oxide network, is less affected by the external environment. The MO_x TFTs suffer much less from device instabilities and outperform the organic counterparts in electrical performances with average mobility one order of magnitude higher.[5] This aspect, in combination with favorable features like transparency and high operational frequencies, allowed MO_x TFTs to become a cornerstone of the flat panel display technology. High-end applications like displays for smartphones demand high device reliability and performance. TFTs employing semiconductors like sputtered indium gallium zinc oxide (IGZO) can nowadays fulfill these requirements. However, this is not always the case when the semiconductor is manufactured via solution processes like printing because these methods are still technologically immature. Several technical challenges related to the achievement of uniform depositions, the rheological constraints, and complex ink chemistry have restrained thus far their wide diffusion at an industrial scale. Precursor-based metal oxides, in comparison with physically deposited ones, may present lower electrical performances (low stability and poor mobility) and require a high process temperature (> 350 °C) to remove solution residuals forming a proper MO_x network. This high thermal requirement restrained the field of applications to rigid substrates, like silicon or glass, or specific and rather expensive materials such as flexible glass or high-performance polymers, like polyimide (PI), while excluding inexpensive and sustainable substrates like polyethylene naphthalate (PEN) or polyethylene terephthalate (PET) and "green" materials such as paper and biopolymers. The study and development of alternative low-temperature curing methods for high-quality films have been the subject of intense research in the past years. Chemistry modifications like adding fuel to the solution, and alternatives to thermal curing such as microwave annealing and other photonic methods, have been tested. Nonetheless, the incomplete comprehension of these curing methods and the technological challenges related to the printing of the functional oxides have thus far restricted the achievement of fully printed MO_x TFTs on the flexible PI, with a process temperature of 300 °C and mobility < 0.05 cm^2/Vs,[6] or to glass/silicon substrates[7].

[1] P3HT = Poly(3-hexylthiophene-2,5-diyl)

The manufacturing could happen on heat-tolerant carriers and then successively transfer the devices onto the final thermosensitive substrates. Companies such as *PragmatIC* involve cleanroom techniques, such as spin-coating and chemical etching, to realize their devices on the thermal resistant PI and then transfer them onto the final substrate. This strategy would avoid thermal limitations linked to the thermosensitive substrates but is not cost-efficient and environmental oriented. Developing a curing process for high-performance but cost-effective electronics like printed MO_x TFTs, suitable for versatile and inexpensive substrate materials, could pave the way for a broader diffusion of daily life objects with embedded electronic capabilities (object-human interfacing, personalized healthcare, or sensing).

The project "Functional OXides Printed on Polymers and Paper (*FOiXP)*", part of the Strategic Focus Area (SFA) Advanced Manufacturing program of the Swiss Federal Institute of Technology (ETH) domain, has addressed the main challenges which are restraining a broader development of metal-oxide electronics:

- the MO_x synthesis with a limited thermal budget;
- the manufacturing of MO_x TFTs directly on these thermosensitive substrates;
- the implementation of additive fabrication techniques like printing.

The consortium of the project was composed of different laboratories, from institutions part of the ETH domain, being: the *Laboratory for Thin Films and Photovoltaics (TFPV)* and the *Laboratory for Functional Polymers (FP)* from the *Swiss Federal Laboratories for Materials Science and Technology (EMPA)*, the *Polymer Nanotechnology Group (INKA)* from *Paul Scherrer Institute (PSI)*, and the *Soft Transducers Laboratory (LMTS)* of the *Swiss Federal Institute of Technology in Lausanne (EPFL)*. The different partners addressed the various research aspects required to achieve low-temperature solution-processed MO_x TFTs:

- substrate selection and functionalization (i.e., substrate characterization and investigation of possible planarization layer);
- ink preparation for the metal oxide functional layers (i.e., development of inks for dielectric and semiconductor layers suitable for low-temperature processing);
- establishing curing approaches compatible with the addressed substrates (i.e., examination and selection of promising approaches, study, and optimization of the synthesis protocols);
- device manufacturing (i.e., TFT design and characterization, process flow development and optimization, integration on the flexible substrates).

In the frame of this project, this thesis provided a scientific contribution on the aspects related to the manufacturing and low-temperature synthesis of the semiconductor metal-oxide layer of the printed transistors. The task required developing a suitable ink formulation, studying and optimizing low-temperature photonic synthesis methods, and manufacturing the devices on rigid and flexible substrates. The challenges faced, the objectives, and the contributions of the thesis are defined in the following sections.

1.2 Objectives and challenges

As stated above, the technological maturity of MO_x TFTs enabled the diffusion of such devices in our daily life. However, regardless of their potential fields of application, they are mainly employed in high-end devices like displays. The use of printing techniques, coupled with inexpensive and flexible substrates, could broaden their range of application, but many issues remain to be resolved. Several challenges have not been extensively undertaken or have not adequately addressed. The majority of the studies conducted so far investigated singular aspects of the problem, like the printing/curing of only one layer, while contemporary using materials not suitable for flexible applications, like thermal SiO_2, since developed on silicon substrates. These approaches often neglect several factors related to the component as a whole. The interactions between printed semiconductor/dielectric, the constraints linked to thermal instability of the final substrates, and their low-temperature processing are among these.

The overview of the main challenges and constraints faced during this Ph.D. work, also depicted in Figure 1.1, is provided hereafter. Foremost, solution processing at low temperatures requires studying and selecting the materials and the chemistry involved. The solution formulation consists of the choice of solvent types (aqueous versus non-aqueous, single versus multiple), metal-oxides precursors (chloride, nitrate, alkoxides, acetates), and eventual extra components (fuels, co-solvents, surfactants). A chemical design of the functional films is also mandatory to obtain the desired electrical performance. It involves an investigation of chemical composition (In, Ga, Zn, Al, Y), the ratio between elements (In:Zn, Al:Y), and the possible introduction of additional materials to functionalize the layers (Al, Y).

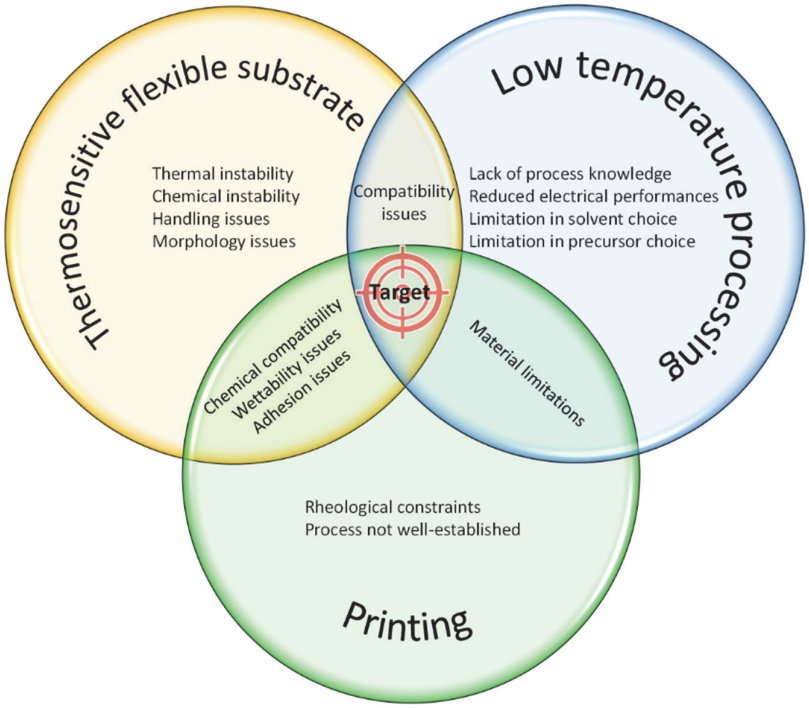


Figure 1.1 Challenges & constraints related to the selected processing methods and their interactions.

An alternative methodology to the standard high-temperature annealing of the deposited films, such as photonic synthesis or chemically engineered synthesis, must be implemented to reduce the processing temperature. The possible approaches need to be evaluated considering their effectiveness in relation to the inks involved and their compatibility with the substrates, especially regarding possible damages to their chemical structure. A deep investigation of the process and the effects of the process parameters on the chemical and electrical characteristics of the MO_x layers is mandatory. High-quality films with high density and few impurities are essential to yield performing TFTs. Low-temperature thermally synthesis may require additional energy sources such as light or chemical (i.e., combustion). In this frame, the choice of the chemical compounds and parameters like the type of light source, the presence or not of an external heat source, the environmental exposure conditions, the temperature applied, and the processing times influence the outcome. Therefore, parametric studies are necessary to understand and optimize the process.

Compared to conventional approaches such as spin coating, inkjet printing as an alternative method for the deposition of the MO_x layers presents additional obstacles. Ink preparation needs to consider the rheological requirements for proper jetting, which may necessitate ink adjustments, like the need for co-solvent. However, it also has to account for the impact of the selected chemistry on the low-temperature processing: for example, compounds with high boiling points are not suitable. Achieving uniform deposition, mandatory for proper device functionality, necessitates process optimization. Different parameters such as jetting waveforms, printing speed, and the number of nozzles can influence the outcome. In this frame, physical phenomena like the coffee ring effect can be present and therefore considered. Moreover, the stacking of different printing layers is even more challenging because of the possible ink incompatibilities and the strict requirements layer morphology, such as the low roughness required at the dielectric/semiconductor interface.

Utilizing flexible substrates instead of rigid substrates, like glass or silicon wafers, presents several technical challenges. Intrinsic higher surface roughness negatively impacts on electrical performances of the TFTs. Possible flexural stresses, which may damage the devices, have to be considered. Specific handling procedures may be required to maintain the substrate flatness and ensuring mechanical stability during the processing. In thermal and chemical stability, polymeric substrates like PEN and PEI underperform standard materials, such as silicon. The higher thermal expansion coefficients (CTE) and the tendency to absorb moisture from the external environment cause dimensional instabilities. An excessive mismatch between the thermal coefficients of the metal oxide and substrates generates stress states in the deposited films, and the more rigid MO_x layers may experience crack formation, resulting in device failure.

We have aimed at fulfilling some of these technological and scientific gaps present in literature regarding the low-temperature processing of metal oxide printed TFTs applied on thermosensitive flexible substrates. The main objectives of the thesis consist in:

- Developing a process requiring temperatures compatible with the targeted substrates: ~200 °C and below;
- Formulating of a MO_x semiconductor solution for sol-gel process, consisting in the investigation of solutions with different chemical compositions towards the achievement of TFTs with high electrical performances while respecting a material selection suitable for low-temperature processing;
- Applying deep-UV-based methods for the reduction of the process temperature required in the semiconductor synthesis, while comparing two deep-UV light sources: low-pressure Hg-based and excimer-based (Xe_2);
- Study of the effects of process parameters on the chemical composition of the MO_x films to estimate the impact on the electrical characteristics of the resultant TFTs and eventually minimize the thermal budget;
- Manufacturing by printing of the different functional components constituting the MO_x TFTs;
- Evaluating the influence of various ink formulations on the effectiveness of the previously developed annealing protocols and optimizing the ink formulation;
- Transferring the proposed process flow onto a thermosensitive substrate.

1.3 Contributions and thesis outline

We have established deep-UV (DUV)-enhanced methods for annealing IZO thin films at low temperatures (≤ 200 °C), highlighting the efficacy of the process, even after 5 minutes of DUV exposure and 5 minutes of thermal annealing. As an outcome, the resulting TFTs have yielded mobility up to ~40 cm^2/Vs, I_{on}/I_{off} ratio > 10^7, and stability under bias stress. We generated knowledge on the role and importance of the treatment steps on the IZO composition and final TFT performances, which is crucial to minimize the thermal budget required for the process and ensure the compatibility of the approach with thermosensitive substrates. We yielded TFTs with better performances than those achieved with comparable synthesis methods (i.e., duration time and process temperature), proving that the DUV-enhanced approach can be effective with a significantly reduced duration, which is potentially appealing for its industrialization. Moreover, the proposed synthesis method is versatile and was applied to synthesize an AlO_x based MO_x gate dielectric at a low temperature of 130 °C. Using this process, we demonstrated an original achievement by manufacturing onto commercially available PEI foils (T_g= 217 °C) capacitors made of inkjet-printed $AlO_x/YAlO_x$ stack, exhibiting a current leakage of ~10^7 A/cm^2 at 1 MV/cm.

The thesis structure includes first a review of the scientific and technological background, followed by some aspects related to metal-oxide-semiconductor engineering and the solution processing of TFTs made of the selected IZO semiconductor at high temperatures. Then, the DUV-based approaches for the low-temperature synthesis of the IZO channel are presented, and the characteristics of the processed TFTs are described. Finally, the additive manufacturing of the MO_x TFT devices using inkjet printing and the transfer of the process onto thermosensitive substrates are addressed.

Chapter 2 aims at providing a general introduction to the scientific and technological fundamentals related to this work. First, we introduce the TFTs, the relevant theory regarding their working principle, and the general requirements for a proper device operation. Then the representative semiconducting channel technologies are presented, with a focus on the metal oxides. We address the different aspects of their solution processing, such as the chemistry involved and the deposition methods. In this frame, the possible approaches to achieve a reduction of the synthesis temperature are examined. We critically analyze the available literature and show how DUV is the most promising method to reduce the thermal budget required yet maintaining good electrical performances. Finally, we illustrate the main difficulties linked to the processing of MO_x TFTs on substrates with a low glass transition temperature (T_g), discussing the limitations of the actual state of the art and presenting the approaches used in this thesis to overcome these challenges.

Chapter 3 addresses the chemical composition of the semiconductor employed in the TFTs. Here, we study the formulation of the precursor solution in relation to the electrical characteristics of the final devices and the low temperatures targeted. We initially examined potential solvents, exploiting the thermalgravimetric analysis (TGA) to characterize the solutions and determine the most promising one for processing at low temperatures. Afterward, we tuned the composition of the film by varying the cations ratio (In:Zn) in the precursor ink, evaluating the electrical characteristics of the resulting TFTs, and selecting the proper formulation. To further improve the electrical characteristics of the IZO based TFTs, we investigated the possibility of adding in the chemical formulation of the solutions a third cation as a dopant. After studying the existing literature, we selected aluminum as a complementary element for the IZO semiconductor, which acts as an oxygen getter and can improve the switching capabilities of the TFTs. We tested it in different concentrations inside the precursor solutions and evaluated the respective electrical performances.

Chapter 4 concerns the characterization of our solution-processed MO_x TFTs processed with standard thermal treatments at high temperatures. To evaluate the efficacy of the low-temperature approaches described in the following chapters, we studied the performances of the selected semiconductor when thermally treated with standard curing methods. We investigated how the IZO semiconductor interacts with solution-processed and atomic layer deposited (ALD) AlO_x-based dielectrics in this context. The material characteristics and the electrical performances of the TFT have been evaluated and compared. Owing to a superior interface between the solution-processed dielectric and semiconductor, the TFTs with MO_x sol-gel active stack have overperformed their counterparts. Ultimately, implementing photolithographic steps, the TFTs thermally annealed at 350 °C demonstrated mobility of ~68 cm^2/Vs and an extremely high $I_{on}/I_{off} > 10^9$, comparable with state-of-the-art sputtered devices, confirming the quality of the MO_x semiconductor and its proper matching with the selected $AlO_x/YAlO_x$ dielectric.

Chapter 5 presents the successful synthesis of solution-processed IZO TFTs at low temperatures via a DUV-based approach. We preliminary evaluated the conversion capability of the DUV light emitted from a Hg-based source, performing Fourier transform infrared (FTIR) analysis on exposed MO_x films, which was revealed to be efficacious already after 5 minutes of exposure. We then manufactured sol-gel MO_x TFTs cured using the DUV-enhanced approach. We performed a parametric study of DUV exposure and post-annealing time applied during the IZO annealing process to evaluate the role of each step and eventually minimize the total curing duration. Moreover, we integrated the solution-processed IZO with a printed high-k $AlO_x/YAlO_x$ dielectric cured with a similar methodology. Despite a process temperature of only 200 °C, the TFTs yielded mobility up to ~16 cm^2/Vs and a high I_{on}/I_{off} ratio of 10^8. We chemically characterized the MO_x films using X-ray photoelectron spectroscopy (XPS) and energy-dispersive X-ray (EDX) analysis. We then correlated these results with those obtained from the electrical characterization, establishing the role and effect of the curing parameters on the electrical performances. This knowledge allowed us to reduce the curing process to 10 minutes (5 min DUV + 5 min @ 200 °C) while maintaining functional devices. Aiming for a further thermal budget reduction, we also reduced the post-annealing temperature to 180 °C, which unfortunately resulted in a drastic decrease in electrical performance. The alternative approach proposed to overcome these limitations is described in the following chapter.

Chapter 6 addresses the technological transfer of the TFTs onto low T_g substrate and their printing. Three main subjects are covered in this chapter: the minimization of the thermal budget required for the MO_x synthesis of both dielectric and semiconductor, the printing of the MO_x layers, and aspects related to the use of low T_g flexible substrate. We propose an alternative excimer DUV light source combined with thermal treatment (i.e., in-situ) as a potential method to overcome the performance limitations at temperatures below 200 °C of the Hg-based DUV. We transferred on our technological platform the dielectric printing process, initially elaborated from our partners at EMPA, and developed a printable IZO semiconductor. In this frame, we optimized the process by studying the ink composition (e.g., co-solvent percentage) and the process parameters, such as drop spacing and the number of printed layers. By doing so, we successfully proven TFTs manufactured with a reduced process temperature ≤ 180 °C with mobility > 1 cm^2/Vs and I_{on}/I_{off} ratio > 10^5. We also exploited the in-situ DUV excimer approach to reduce the thermal budget required to synthesize the printed MO_x dielectric. With a short in-situ DUV excimer treatment of 20 minutes, we demonstrated capacitors with printed MO_x dielectric and current leakages ~10^7 A/cm^2 at 1 MV/cm, even at temperatures as low as 130 °C. Finally, we address the replacement of rigid substrate with the low T_g PEI foil, demonstrating capacitors with inkjet-printed MO_x dielectric, with performances comparable to those achieved on rigid substrates, thus suitable for future implementation in more complex devices such as TFTs.

Concluding remarks and the perspectives related to the results achieved during this thesis work are given in **Chapter 7**.

Chapter 2 Metal-oxide thin-film transistors: fundamentals and technology

This chapter covers the fundamentals of solution-processed metal-oxide-based thin-film transistors.

First, we introduce the thin-film transistors (TFT) technology and its working principle, comparing it with standard metal oxide semiconductor field-effect transistors (MOSFET) used in CMOS silicon electronics. After describing the possible configurations of a TFT related to the stacking order of the functional layers, semiconductor, and dielectric, we present the figures of merit used to evaluate the performance of a TFT: the mobility, the I_{on}/I_{off} current ratio, the threshold voltage, and the subthreshold swing. Then, we compare the primary four categories of semiconducting channels used in TFTs: amorphous silicon (a-Si), polycrystalline silicon (poly-Si), organic polymers, and metal oxides (MO_x). Among them, MO_x emerged over their counterparts for superior performances, notably high carrier mobility (> 70 cm^2/Vs)[8], transparency, and large-area uniformity. Moreover, functional MO_x semiconductor layers can be manufactured via solution processing at a relatively low temperature (< 350 °C).

The deposition methods for MO_x thin films are introduced. After providing an overview of the standard cleanroom-based fabrication processes, like sputtering, we compare these conventional methodologies with the solution-based ones, such as sol-gel. Here we analyze the advantages and drawbacks of the two approaches, especially concerning the final film quality and the process constraints. We then focalize on the solution processing of the semiconductor: lowering the temperature required for the synthesis of a MO_x is a challenging task. It requires the investigation and study of all the process aspects, starting from the chemistry involved to the proper selection of the annealing method. We describe the possible options and the relevant state-of-the-art regarding the ink formulation and the approaches for their curing at a relatively low temperature of ≤ 200 °C. In this frame, we will discuss the techniques based on deep-ultraviolet (DUV) exposure that were investigated during this thesis.

We then report on the printing methods: after a general introduction, we highlight the techniques capable of depositing thin films with a suitable uniformity, a mandatory requirement for the functional active layers targeted, and describe the actual status of printing MO_x semiconductors. Afterward, we introduce the solution-processed MO_x dielectric film applied in combination with the low-temperature solution-processed MO_x semiconductor developed in this work. We discuss the possible interactions between the active layers and the methods utilized to characterize the behavior of the fully solution-processed MO_x active stack.

Finally, we highlight the challenges and limitations of manufacturing sol-gel-based MO_x TFTs on thermosensitive substrates. To conclude, by looking at the available literature on solution-processed/printed MO_x TFTs manufactured on this type of substrates, we discuss the technological and scientific gap present and introduce the approaches selected in this thesis to overcome it.

2.1 Introduction to TFT technology

The field-effect transistors (FET) are three-terminal devices that exploit the electrical field generated from a change in potential at one of the electrodes, the gate, to modulate the conductance in the semiconducting channel between the other two electrodes, the source and the drain. The thin-film transistors (TFTs) can be considered as a subgroup of the field-effect transistors. In these transistors, all the passive and active layers of the devices are thin films, in the range of hundreds of nm thick, deposited on a substrate made of electrically inert material. First invented by Weimer in 1962[9], their technological dissemination was initially restrained from technical limitations, namely the poor control of material properties in the thin-film semiconductor and the inadequate device reliability over large-area processing. Only after the demonstration of performing TFTs (mobility ~1 cm^2/Vs) in 1979, integrating as semiconductor channel hydrogenated amorphous silicon (a-Si:H) deposited by via plasma-enhanced chemical vapor deposition, the TFTs became of interest as switching elements for the pixels of the first liquid crystal displays (LCDs).[10] They are nowadays widely implemented consumer electronics, especially as driving elements for the mentioned LCDs. However, they have also been demonstrated and exploited in a wide range of other areas, such as in microelectronics as non-volatile memories[11], in digital radiography as X-ray detectors[12], and applied as transducers in physical and (bio)chemical sensors[2,13].

In this section, we give an overview of the TFT technology. Firstly, we provide a basic description of the TFT working principle and classification of the devices according to the layer stacking. Then, the relevant figures of merit for this type of device are introduced by looking at the typical output and transfer characteristics curves. Lastly, we describe and compare the most frequently used semiconducting channel technologies according to the mentioned figures of merit and other relevant parameters.

2.1.1 TFTs and MOSFET: working principle and comparison

As depicted in Figure 2.1, the field-effect transistors are three-terminal devices, with the semiconductor layer in physical contact with the source and the drain electrodes while being separated from the gate electrode by an insulating layer. The electrical field generated from a change in potential on the gate can modify the density of charges at the interface between the dielectric and the semiconductor layers. Ultimately, the control of the electrical operation in the channel between the source and the drain is obtained via a conductivity modulation in the semiconductor, forming a conduction channel close to the semiconductor/dielectric interface, where the carriers can flow depending on the nature of the charge carriers, either electrons or holes, the semiconductors can be respectively n-type or p-type.

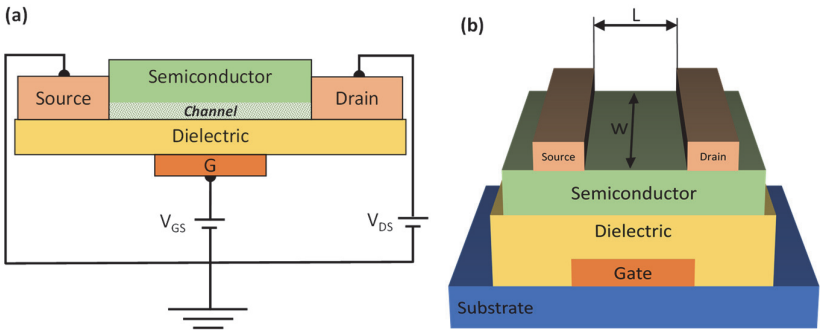


Figure 2.1 Schematic representation of a three-terminal field-effect transistor. (a) Shows the biases applied to the electrodes and (b) represents a TFT architecture with the relevant geometrical dimensions.

Today, metal oxide semiconductor field-effect transistors (MOSFETs) are the basic building blocks of complementary-metal-oxide-semiconductor (CMOS) electronics in standard silicon-based microprocessors. Their semiconducting channel, along with the source and drain electrodes, is part of the rigid single-crystal Si wafer employed as substrate (as depicted in Figure 2.2a). The channel is created with the inversion of the majority carriers at the interface, which occurs when a potential is applied to the gate. The electronic characteristics of the silicon wafer, such as the type of the majority charge carriers and its resistivity, can be locally modified via ion implantation techniques. To do so, different complex processes requiring specific conditions, like high temperature (>1000 °C) or high vacuum, are necessary: oxidation, lithography, ions implantation, thin-film deposition, and etching. They exploit the intrinsic high electron mobility of the crystalline silicon (c-Si) channel to reach excellent performances (> 1000 cm^2/Vs)[14]. However, the rigid c-Si substrate is fundamental as it plays an active role in the device.

In TFTs, all the passive and active layers of the devices are deposited on the substrate, which is typically electrically inert (Figure 2.2b). The channel is created with the accumulation of the majority carriers. For example, an n-type semiconductor will accumulate

electrons when a positive voltage is applied to the gate, thus allowing conduction between source and drain electrodes. In terms of electron mobility, the highest values reported for TFTs are ~100 cm^2/Vs.[5] Nevertheless, the channel is not made in the substrate but deposited as thin film, and therefore TFTs can be processed on a large variety of substrates. This freedom in the choice of the substrate allows the realization of transistors onto insulating substrates, like glass or polymers, which may present physical characteristics like optical transparency or mechanical flexibility, which is unattainable with silicon electronics. Moreover, their deposition processes may not require high temperatures or heavy infrastructures. By employing solution processes like spin-coating and printing, the functional layers and electrical connections can be deposited without vacuum equipment and at a lower temperature (< 500 °C) on large-area surfaces. Table 2.1 summarizes the main differences between TFTs and MOSFETs.

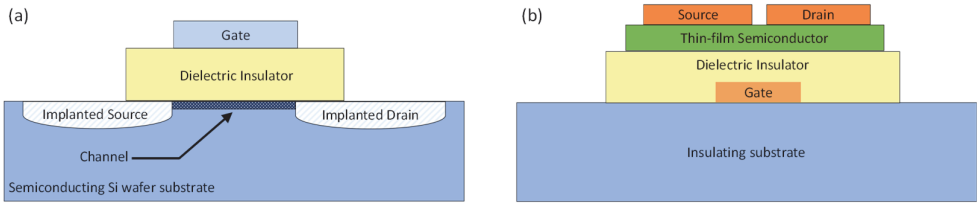


Figure 2.2 Cross-section and structure comparison between (a) MOSFET and (b) TFT.

Table 2.1 Comparison between MOSFET and TFT technology. Adapted from [15]

	MOSFETs (CMOS)	**TFTs**
Layer formation technology	Implantation, thin film deposition, growth from the substrate	Deposition (sputtering, PECVD, spin-coating, printing)
Process temperature [°C]	High temperature (> 500 °C)	Low temperature (< 500 °C)
Quality of the layers	Highly crystalline	Amorphous or polycrystalline
Carrier mobility in the channel [cm^2/Vs]	450 up to > 1000	0.1 up to ~100
Carrier type	Both p-type and n-type	Mainly one type, depending on the semiconductor material (poly-Si both)
Type of substrate	Silicon opaque and mainly rigid	Any kind of substrate including glass or plastic: transparent, flexible
Substrate dimensions	Up to 12 inches in diameter silicon wafers	Centimeters to meter size

2.1.2 Configurations and characteristics of TFTs

A difference between TFTs over the MOSFETs is the possibility to vary their configuration accordingly with the requirements of the targeted application. A TFT can be classified according to the order used to stack its different functional layers.

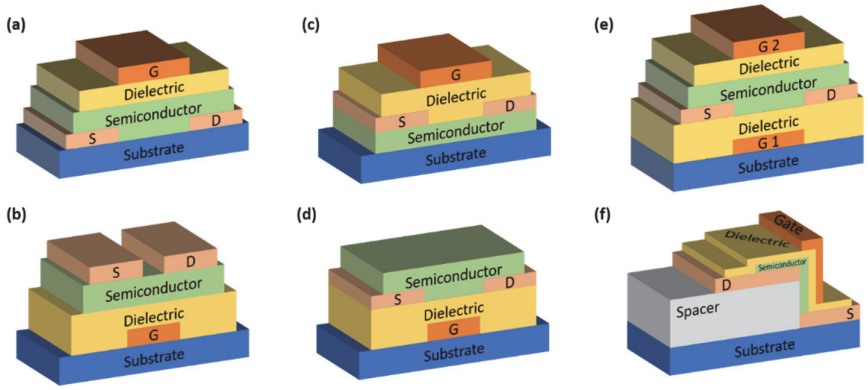


Figure 2.3 The most common TFT configurations: (a) top gate (TG) staggered TFT, (b) bottom gate (BG) staggered TFT, (c) TG coplanar TFT, (d) BG coplanar TFT, (e) double gate (DG) TFT, and (f) vertical TFT (VTFT).

The most common configurations are associated with the position of the gate electrode relative to the active semiconductor layer: top-gate (TG) (Figure 2.3a and Figure 2.3c) and bottom-gate (BG) (Figure 2.3b and Figure 2.3d). Top- and bottom-gated architectures can be further grouped in two sub-categories, depending on the position of the interface where the carrier transport occurs to source and drain electrodes: coplanar if on the same plane and staggered if not. Each configuration presents advantages and disadvantages from the fabrication and performance point of view. The selection of the best structure depends on the selected application and materials used.[16] BG configuration is widely used in display technology because the active channel, which may suffer from light-induced instability, is shielded from the gate beneath. However, the active layer is exposed to the atmosphere, which could cause electrical instability and performance degradation, demanding an extra fabrication step to passivate the semiconductor.[5] In TG architecture instead, the semiconductor is covered by the gate dielectric and gate electrode layers and does not necessarily require passivation. Nevertheless, the fabrication steps following the active layer deposition, involving vacuum, high temperature, or reacting chemicals, may influence the electrical characteristics of the semiconductor. In addition to these standard structures, alternative layouts have been employed to further improve the performances. In double-gate (DG) TFTs (Figure 2.3e), an additional gate is deposited to increase the portion of the semiconducting channel experiencing the field-effect, providing better channel modulation and higher currents.[17] Alternatively to these planar geometries, driven by the need for devices miniaturization and higher performances, vertical TFTs (VTFTs) or quasi-vertical TFTs (QVTFTs) (Figure 2.3f) have been recently investigated. In this configuration, shorter channel lengths can be achieved without photolithography, resulting in high on-currents. Source and drain electrodes are stacked parallelly with a dielectric film in between, which acts as a spacer with its thickness defining the dimension of the channel.[18,19] This last configuration requires excellent step coverage from the layers deposited.

2.1.3 Figures of merit

The most used figures of merits can be extracted from the current-voltage (I-V) characteristics measured in static conditions (direct current (DC)). Considering the device depicted in Figure 2.4 a and choosing for simplicity the case of an n-type TFT working in enhancement mode, with the source grounded (V_S = 0 V) and applying a positive voltage to the gate electrode (V_{GS}), there will be an accumulation of negative carrier charges (i.e., electrons) at the dielectric/semiconductor interface. Once the drain electrode V_{DS} is also biased and reaches a specific value of V_{GS}, called threshold voltage (V_{Th}), an electrical current I_{DS} can flow between the source and drain electrodes. The two typical I-V characteristics employed to describe the electrical behavior of these devices are the transfer characteristic (I_{DS}-V_{GS} Figure 2.4a) and the output characteristic (I_{DS}-V_{DS} Figure 2.4b).

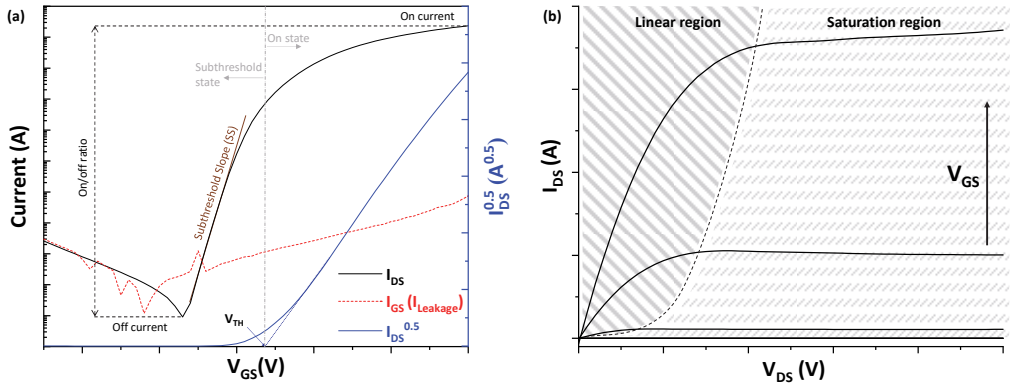


Figure 2.4 Typical I-V characteristics of a TFT: the transfer (a), obtained at varying V_{GS} and fixed V_{DS}, and the output (b), extracted by varying V_{DS} at determined V_{GS} values.

As shown in the output curve, two different working regimes can be identified: the linear and the saturation regime. The two working regimes are related to the physical formation, between source and drain, of a conductive path in the semiconductor layer. The completion of the channel formation occurs typically when a minimum value of V_{GS}, V_{Th}, is applied. For small values of V_{DS} ($V_{DS} << V_{GS} - V_{Th}$), the charge-carrying channel is still incomplete, and the current I_{DS} is varying as a function of both V_{DS} and V_{GS}. Its approximated value can be calculated from the simplified Shichman–Hodges model[20]:

$$I_{DS,lin} = \frac{W\, C_{ox}\, \mu}{L} (V_{GS} - V_{Th}) V_{DS}$$

Equation 2.1 Drain current in the linear regime.

where W is the channel width [m], L is the channel length [m], and μ is the carrier mobility [cm^2/Vs]. C_{ox}, which is the dielectric capacitance per unit of area [nF/cm^2], is defined as:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}}$$

Equation 2.2 Dielectric capacitance per unit of area.

where t_{ox} is the thickness of the dielectric film, ε_0[2] is the vacuum permittivity, and ε_r is the relative permittivity.

Once $V_{DS} \geq V_{GS} - V_{Th}$, the completed conductive channel is formed, and the device is in saturation regime: the current I_{DS} is only a function of the applied V_{GS}. I_{DS} is calculated according to the following quadratic expression:

$$I_{DS,sat} = \frac{W\ C_{ox}\ \mu}{2L}\ (V_{GS} - V_{Th})^2$$

Equation 2.3 Drain current in saturation regime.

From the above-mentioned equations (Equation 2.1, Equation 2.2, Equation 2.3) and the curves depicted in Figure 2.4a and Figure 2.4b, we can extract the main parameters used to describe a TFT in DC mode of operation: carrier mobility, I_{on}/I_{off} ratio, threshold voltage, and subthreshold swing.

2.1.3.1 Carrier Mobility

This parameter evaluates the efficiency of charge transport in a material. In TFTs, together with geometrical factors and capacitive coupling, it directly influences the maximum drain current achievable. Physically, it describes how quickly the charges can move when subjected to an electric field. It is mainly influenced by the presence of scattering sources in the material (e.g., lattice imperfections, impurities, grain boundaries).[21]The charge-transporting channel is localized in a confined area in the proximity of the interface between semiconductor and dielectric, additional sources of scattering, like the interfacial surface roughness between the two layers, have to be also accounted for. Notably, MOSFETs possess a smooth interface as the dielectric oxide is grown directly from the Si substrate, whereas interface quality could be more problematic for TFTs.

The carrier mobility is a characteristic of the material, ideally independent of the method used to calculate it. However, in real applications, the extracted mobility values and the V_{Th} strictly depend on the model used to describe and predict the TFT behavior.[22] The most common mobility values extracted, which depend on the working regime of the TFT, are the linear mobility μ_{lin} (also known as Field-effect mobility μ_{FE}) and the saturation mobility μ_{sat}:

$$\mu_{lin} = \mu_{FE} = \frac{L}{W\ C_{ox} V_{DS}} \frac{dI_{DS}}{dV_{GS}}$$

Equation 2.4 Linear mobility.

and

$$\mu_{sat} = \frac{2L}{W\ C_{ox}} \frac{d^2 I_{DS}}{dV_{GS}^2} = \frac{2L}{W\ C_{ox}} \left(\frac{d^2 \sqrt{I_{DS}}}{dV_{GS}} \right)^2$$

Equation 2.5 Saturation mobility.

where $\left(\frac{d^2 \sqrt{I_{DS}}}{dV_{GS}} \right)^2$ can be extracted as the slope of $(I_{DS})^{1/2}$ versus V_{GS} plot in saturation regime. The values obtained from linear mobility tend to be incorrect and overestimated because of the voltage dependence and the possible influence of high gate leakage and contact resistance.[5] To provide values closer to the actual performance of the realized TFTs, in this work of thesis μ_{sat} has been used to evaluate the mobility of the devices. The extraction method for the capacitance of the gate dielectric, C_{ox}, and the effects of its frequency dependence on the mobility values will be discussed in Section 2.5.2.

[2] $\varepsilon_0 = 8.85 \cdot 10^{-12}\ \frac{F}{m}$

2.1.3.2 I_{on}/I_{off} ratio

Another important parameter to characterize the operation for a TFT, which can be extracted from the transfer curve, is the I_{on}/I_{off} current ratio, defined as:

$$\frac{I_{on}}{I_{off}} = \frac{\left|I_{DS}(V_{GS,max}, V_{DS,max})\right|}{min\left|I_{DS}(V_{GS,max})\right|}$$

Equation 2.6 I_{on}/I_{off} current ratio.

It describes the switching ability of the device. Values of 10^6 or higher are generally desirable for high-end digital circuits[23], but values > 10^4 are typically acceptable for other applications.

2.1.3.3 Threshold voltage and subthreshold swing

The threshold voltage V_{Th} is defined as the minimum value of V_{GS} to apply in order to form a conductive channel in the semiconductor layer. Once reached this voltage value, the transistor can be considered as in "ON" state. Instead, at a value below, the device works in the so-called subthreshold region. Once again, the experimental values corresponding to V_{Th} depend on the modeling of the electrical behavior of the TFT.[22] Among the different ones, we selected the extrapolation of the value from the $(I_{DS})^{1/2}$ versus V_{GS} plot in saturation mode, as shown in Figure 2.4a.

The subthreshold swing SS is a parameter that describes how efficiently the device can work as a switch. It defines the gate voltage required to increase by one decade the drain current in the subthreshold region, indicating how fast a device can be turned on. It can be extrapolated from the transfer plot and is expressed as follows:

$$SS = max\left(\frac{d\log_{10}\left|I_{DS}(V_{DS,max})\right|}{dV_{GS}}\right)^{-1}$$

Equation 2.7 Subthreshold slope.

2.1.3.4 TFTs performances quantification

The electrical performance of a TFT can be evaluated using the figures of merit presented above. Independently from the geometrical form factors, W and L, a semiconductor showing good mobility (μ >1 cm^2/Vs) is necessary to achieve high-performing devices. However, to achieve high I_{on}/I_{off} ratios (> 10^6) is also important to limit off-current to low values (pA range or less), which ultimately reduces the power consumption of the device in an "OFF" state. Moreover, low subthreshold swing (< 100 mV/dec) and a threshold voltage close to 0 V are desirable to reduce the power consumption and the operating voltage in circuit applications.

2.1.3.5 TFT general requirements

To obtain a suitable level in performance, a TFT exhibiting only one satisfactory single characteristic like high mobility is not enough. Each component of a performing TFT needs to respect some design guidelines, independently from the type of materials and manufacturing processes used. The essential requirements for the components of a single TFT device and their interfaces, addressed in detail in the following paragraphs, are depicted in Figure 2.5.

In this work, we aimed to manufacture metal-oxide TFTs with the best electrical characteristics possible. Therefore, we based ourselves on these criteria when selecting the functional materials, such as a semiconductor ensuring high electrical performances, e.g., mobility and switching capabilities, or low leakage for the dielectric material, while also considering other aspects like the interactions between the different layers and material printability.

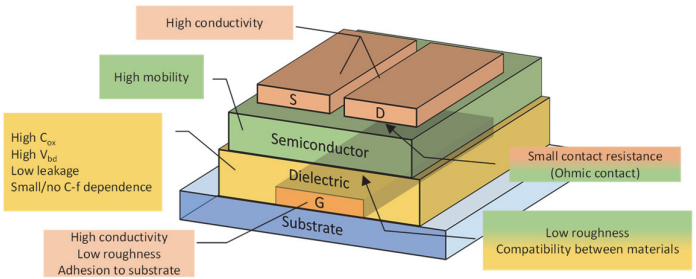


Figure 2.5 General requirements for each TFT component and their interfaces.

2.1.4 Comparison between semiconducting channels

TFTs can also be classified as a function of the material composing its semiconducting channel. Four technologies have emerged as most common and diffused: amorphous silicon (a-Si), low-temperature polycrystalline silicon (LTPS), organic semiconductors, and metal oxide semiconductors (MO_x). Alternatives based on nanomaterials such as carbon nanotubes[24] or 2D materials (nanosheets of MoS_2 or WSe_2, and graphene)[25] have also been investigated. However, due to the repeatability issues of the devices and process complexity, they are still at the research phase.

In covalent semiconductors such as Si-based ones, the charge transport is related to the overlap between the sp^3 orbitals, which are highly directional; therefore, their mean free path[3] is strongly dependent on the material structural order. As a direct consequence, the randomness of these overlaps in amorphous silicon limits the mobility of the resulting TFTs to $\mu < 1$ cm^2/Vs, whereas ordered crystalline silicon, like low-temperature polycrystalline silicon (LTPS), yields mobility up to 100 cm^2/Vs, and is preferred for high-end commercial applications, e.g., high-resolution displays[26].

The diffusion of organic-based TFTs (OTFTs) has been limited for a long time from the low mobility achievable (μ <1 cm^2/Vs). They also suffer from device instability and poor uniformity over a large area caused by the influence on the charges transport of several variables, such as ambient atmosphere and crystallinity.[27]To improve their electrical performance and reduce the instabilities, an encapsulation layer is usually necessary for OTFTs. Different materials, like poly(3-hexylthiophene-2,5-diyl) (P3HT) and pentacene, have been investigated as semiconductors, and thanks to the increased interest in the field, OTFTs reaching mobilities as high as 43 cm^2/Vs have been reported[28] however, such good performances are still hard to consistently reproduce.

In terms of charge transport, MO_x based TFTs exhibit mobility comparable to the LTPS technology and can be optically transparent. As a unique characteristic of metal-oxide semiconductors containing post-transition metals, the electron transport occurs among the isotropic *s* orbitals[4] via direct overlap, independently from their structural order. Therefore, these materials are preferentially n-type. Among the various MO_x employed as semiconductors, zinc oxide-based, such as zinc tin oxide (ZTO) and indium oxide-based ones, are the most common. Indium oxide-based materials such as indium oxide (InO_x) and indium zinc oxide (IZO) can offer high mobility and are widely diffused. Indium gallium zinc oxide (IGZO) is the most diffused MO_x in industrial applications (e.g., displays) because it owns good carrier modulation (i.e., high I_{on}/I_{off}) and optimal operational stability. High mobility values have been demonstrated using both amorphous MO_x, like IGZO with $\mu \sim 76$ cm^2/Vs[8], and crystalline MO_x like (InO_x) or ZTO with mobility exceeding 35 cm^2/Vs [29,30]. The carrier transport in the metal-oxide semiconductors and their chemical composition (i.e., the role and the choice of the cations) will be discussed in detail in Chapter 3.

Mobility is one of the several parameters summarized in Table 2.2 that needs to be considered for a proper comparison of the nature of the semiconductor channel. Each technology presents pros and cons in terms of electrical characteristics achievable, and the use of a particular film is related to the final application targeted. Moreover, when considering their processing, only organic and MO_x materials can be solution-processed and printed to cost-effectively produce TFTs on large area substrates. Finally, MO_x-based TFTs exhibit superior stability, switching behavior, and outperform their organic counterparts in electrical performance, making them strong candidates for future ubiquitous electronics.

Table 2.2 Comparison between the characteristics of the different channel materials for TFTs.

	a-Si	**LTPS**	**Organic**	**MO_x**
Microstructure	Amorphous	Polycrystalline	Mainly polycrystalline	Mainly amorphous
Carrier Mobility [cm^2/Vs]	1	50-100	0.1-10	10-100
Process Temperature [°C]	150-300	350-500	RT to 250	RT to 450
Semiconductor stability	High	High	Low	High
Transparency	Null	Null	Medium	High
Printability	Low	Low	High	High
Flexibility	Low	Low	High	High
Conduction type	N-type	N and P-type	Mainly P-type	Mainly N-type

[3] The *mean free path* is defined as the average distance that an electron travels before it scatters.

[4] Condition valid for post-transition metal cations with an electronic configuration $(n-1)d^{10}ns^0$, where *n*, which is the principal quantum number, is ≥4.

2.2 Solution processing of MO_x based TFTs

This section gives a specific focus on the MO_x based TFTs: providing an overview of the usual techniques used for their manufacturing and an introduction to their solution processing. After comparing standard deposition approaches like sputtering and solution-based ones, we provide a more detailed description of the chemical reactions occurring during the metal oxide layer formation in a sol-gel process, the method used in this thesis to synthesize the selected indium zinc oxide layers. The chemistry involved in the synthesis of the IZO semiconductor, such as the precursor concentrations, the role of the chemical elements, and their proportions (In:Zn ratio), will be discussed in more detail in Chapter 3.

2.2.1 Process fundamentals and comparison with standard methods

In the previous section, we have already mentioned the advantages of metal oxide thin-film semiconductors over their counterparts, especially organics. In particular, device stability and process repeatability have significantly helped their diffusion in commercial applications. It is also worth mentioning that all these technological advancements in the field have been possible thanks to well-established manufacturing processes. The principal deposition technique for MO_x semiconductors is sputtering. The availability of different sputtering methods, such as RF[5], RF-magnetron, and DC, combined with the possible tuning of several process parameters, like pressure and sputtering power and the use or not of a reactive atmosphere, provides a good process-tunability. With the large availability of target materials, which can also be sputtered simultaneously at different rates, the fine-tuning of the material composition can be achieved, with layers having a typical thickness around tens – hundreds of nanometers. The process is usually carried out at room temperature, but the final MO_x films may necessitate thermal post-treatments at relatively low temperatures (generally up to 150 °C) to ensure proper semiconducting characteristics. Sputtered IGZO TFTs are characterized by high I_{on}/I_{off} ratios (~10^6), electrical stability, and mobility values as high as 76 cm^2/Vs.[8] Owing to these characteristics, they are considered the standard reference for MO_x TFTs. The IGZO TFTs are present in most commercial rigid displays that utilize glass as a transparent substrate[23] or in the last generation of flexible displays exploiting thermo-resistant but opaque substrates like polyimide (PI).[31] Alternative standard processes, like pulsed laser deposition (PLD)[32], atomic layer deposition (ALD)[33], and Plasma-enhanced-ALD (PEALD)[29], can also be used to manufacture indium-based semiconductors InO_x, IZO, and IGZO,[5] or other semiconductors like zinc tin oxide (ZTO).[33] However, these techniques that yield highly conformal and dense layers are more common for dielectric deposition.[34] However, all the mentioned techniques present a drawback: they are vacuum-based. Moreover, many fabrication steps require patterning by photolithography, which necessitate a cleanroom environment, increasing their fabrication costs and limiting the process throughput.

Thanks to their scalability and lower cost, solution processes for MO_x semiconductors are being considered for the large-area manufacturing of TFTs. Their additive manufacturing would greatly interest the cost-effective production of a new generation of IoT applications, like disposable electronics and sensors. By simplifying and achieving localized materials patterning and using less demanding equipment, printing can reduce materials losses and infrastructure costs yet maintaining good process flexibility and resulting in the manufacturing of performing devices. However, solution-based approaches are relatively new compared to the standard thin-film patterning processes used in CMOS foundries and involve liquid chemistry, resulting, therefore, in quality of the functional materials that are generally lower than those processed using vacuum-based techniques. Hence, solution-processed TFTs usually display lower electrical performances and can suffer from unstable behaviors.[20]

Several methods have been demonstrated to obtain a MO_x film starting from a solution, [35] but two are generally preferred, especially when targeting low-temperature processing: the use of MO_x nanoparticles and the "sol-gel" method. In the first approach, MO_x nanoparticles maintained in suspension are exploited: once the solution is deposited, the chemicals, like the solvent and the surfactants that ensure the stability of the suspension, are taken away typically using heat, leading to the creation of a semiconducting path through a necking process between the nanoparticles. This approach requires reduced heat and can be carried out at temperatures as low as room temperature.[36] *Dasgupta et al.* in 2011 reported TFTs with printed InO_x and ion-gel dielectric processed at room temperature but with low mobility 0.2 – 0.8 cm^2/Vs (depending on the model employed to extract it).[37] Some promising results have also been achieved with this approach: notably, *Garlapati et al.* reported photonically annealed nanoparticle-based printed InO_x semiconductor, with polymeric dielectric on PEN substrate achieving mobility of ~12 cm^2/Vs.[38] However, this method may limit the electrical performance of the resulting devices: the discrete nature of the particles can create an excessive roughness at the semiconductor/dielectric interface, requiring liquid-based dielectrics (i.e., electrolytes) and causing film porosity. Poor ink stability can also limit the uniformity of the devices over a large area.

[5] RF = Radio frequency.

On the other side, the sol-gel approach involves the chemical synthesis of metal-oxides starting from a precursor solution. The process can be reproducible, notably by proper control of the synthesis environment, and the quality of the resulting films is higher than the one achieved with nanoparticles. The interest in this approach grew exponentially since the first solution-processed IGZO TFT was published by *Kim et al.*[39]. They reported TFTs fabricated on a glass substrate and made of an IGZO film annealed at 450 °C for 1 hour, which yielded mobility close to 1 cm^2/Vs. Nowadays, thanks to advancements in the field, mobilities such as 20 cm^2/Vs or more employing IGZO semiconductors are more commonly reported.[40,41] As a possible drawback, depending on the precursors and solvent used, they may require long processes or high temperatures to promote their conversion into functional MO_x films. Generally, the formation via solution processing of MO_x semiconductor films, like IGZO, IZO, or ZTO, involves temperatures between 350 °C and 500 °C, with a variable process duration (up to 1 hour or more).[42–44] Moreover, due to the potential presence of solvent residuals and unconverted compounds in the films, they can present porosity and a lower quality MO_x network than those manufactured via standard sputtering technology.

In this thesis work, we have preferred a sol-gel process over the nanoparticle-based approach because of the better performances achievable and its process stability and repeatability. We now provide in the following paragraph a description of the chemical reactions involved.

2.2.2 Sol-gel chemistry

The sol-gel process is a well-established methodology used to form a material network called “gel”, starting from a colloidal solution called “sol”. In the case of MO_x, the colloidal solution is composed of the precursors, which are usually a coordinated complex where the metal cations are surrounded by ligands, and the solvent, which is usually water or alcohol-based. Some extra components, like surfactants, can be added to the mixture to maintain its colloidal nature and avoid precursors agglomeration/sedimentation. The chemical process that leads from the sol to the final gel, which in our case is a dense MO_x film, is quite complex and involves different simultaneous reactions and different intermediate products. However, it can be schematically described as a five-step process: (i) precursor decomposition via solvation, (ii) solvolysis, (iii) condensation, (iv) film densification via residuals removal, and (v) crystallization.

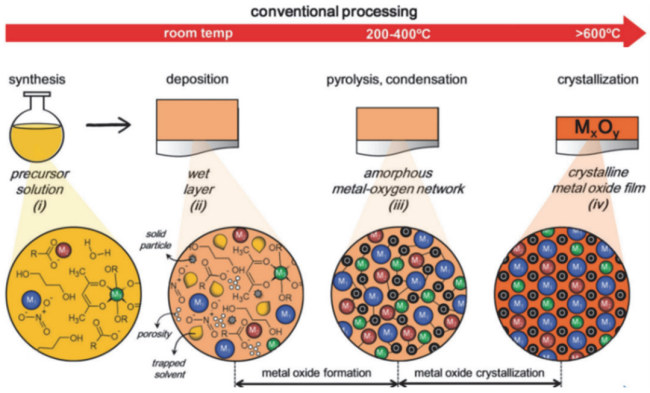


Figure 2.6 Representation of the chemical steps occurring during the heat treatment of a sol-gel processed MO_x layer. Adapted from [35].

The initial precursors are dissociated during the solvation step (i), releasing free cations (M) that get coordinated with water molecules forming solvation complexes, like hexaaqua complex.[45] During the solvolysis (ii), some of the weak bonds in the complexes are replaced to form hydroxides (M-OH) or alkoxides (M-OR), which will ultimately create the M-O-M network. In the condensation step (iii), there is the formation of oxo-bridges (M-O-M) between the cations with a simultaneous release of either H_2O or alcohol (R-OH). It is worth mentioning that the chemical reactions in (i), (ii), and (iii) can partially occur already after the solution preparation: in the sol-gel processing of MO_x TFTs, this solution “aging” needs to be accounted for since it may influence the final film structure.[46] The reaction conditions in which the reactions occur are also essential: the ultimate microstructure of the material is also dependent on the equilibrium between the alcoholysis reaction in (ii) and the oxolation in (iii), which is dependent on the pH of the solution.[47] *Jun et al.* demonstrated that depending on the solvent chosen, resulting in extremely acidic (4.7) or extremely basic (~14) solutions, their ZnO was either inactive or performing (max mobility 14.7 cm^2/Vs at 450 °C).[48] For this reason, additives such as citrate and urea can be included to control the reactions (change the pH or facilitate the formation of intermediate complexes) and obtain the desired result.[49]

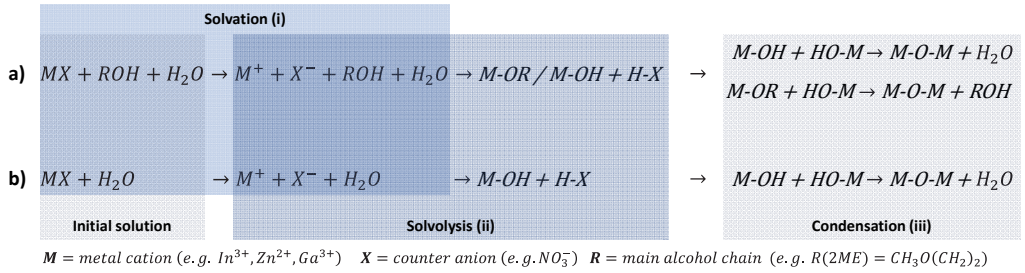


Figure 2.7 The chemical reactions occurring during the sol-gel process. Depending on the solvents involved: a) represents the alcohol route while b) represents the water route. As an example, are reported the elements involved in the sol-gel process of IGZO using nitrate precursors and 2-methoxyethanol as solvent.

After the deposition of the solution, a drying step is performed to remove the solvent in excess, obtaining a dried film with a partial MO_x networking. The presence of unconverted precursors, hydroxides, and solvent residuals, hinders the proper MO_x networking and affects the electronic transport in the film. An improvement in the quality of the film is achieved in step (iv), when impurities, solvent, and precursors residuals are removed thanks to the energy provided during further annealing steps. This energy is also exploited to rearrange the MO_x network and remove eventual lattice imperfections, reducing the film porosity related to the gases previously trapped and enhancing the film densification.[50] Finally, if the energy provided is sufficient, the film structure can further rearrange, obtaining partial or total crystallization (v).

As mentioned previously, the energy required for these reactions to occur is usually provided via thermal treatments performed at relatively high temperatures. In Section 2.4, we will describe the alternative approaches that can replace the standard thermal procedures and be exploited to synthesize metal-oxide thin films at a lower temperature.

2.3 Deposition methods for solution-processed metal-oxide TFTs

In the following section, we introduce the standard coating methods used to manufacture solution-processed MO_x TFTs. In thin-film transistors, the deposition of the semiconductive material should be limited to the area of the active channel: unnecessary conductive paths can increase the electrical losses and compromise the device performance. For this reason, the semiconductor layer necessitates to be locally patterned. The deposition methods for metal-oxide thin films can be divided into two main categories: full-area deposition and local-area deposition. The first category, which yields un-patterned surfaces and may require additional processes like photolithographic steps to pattern the layer, includes techniques such as dip coating,[51] bar coating,[52] spray coating,[53] and spin coating. The second category, which results in layers already patterned, is mainly constituted by additive manufacturing techniques, i.e., printing.

The printing methods can be separated into two categories: those requiring a physical printing plate and those reproducing a pattern from a digital file. Some of these technologies require contact between the system and the substrate, like gravure and flexography, while others, also called jetting techniques like inkjet, do not involve contact. The rheological properties of the inks, like viscosity, surface tension, and density, determine the suitability of specific printing technology, ultimately influencing the resolution achievable and the thickness of the layers. In this frame, each technique has advantages and limitations that determine its appropriateness for a specific application. Concerning the deposition of MO_x active layers, the methods that could be interesting for future implementation on an industrial scale need to manufacture very thin films with a precise thickness control while maintaining uniformity on a large area. Inkjet printing is a digital technique, ideal for quick prototyping since plateless but potentially scalable for industrial applications, which does not suffer from possible contact-related cross-contamination, and possesses high process flexibility. Therefore, it is being considered as one of the most promising for large-area manufacturing of solution-processed MO_x TFTs. After a brief overview of the deposition methods, we will focus on the printing techniques, addressing their working principles and highlighting the relevant state-of-the-art. We will concentrate on inkjet and aerosol jet that have been studied and utilized during this Ph.D. research.

2.3.1 Coating techniques

Among the classic coating methods, spin coating (Figure 2.8) is the most established method in academia for solution-based MO_x thin-film deposition with several hundred publications in the literature.[54] The main reasons for its wide diffusion are its process versatility, easiness, and reproducibility. The working principle is based on the equilibrium between centrifugal forces and viscous forces of the solutions. Cast on rotating support that holds the substrate, the solution spreads due to the angular speed and forms a thin film on the substrate while the excessive solution is removed. Once defined the solution composition and its rheology known,

primarily related to the molar concentration, by varying some process variables like spin speed and acceleration, uniform layers can be deposited. Finally, the deposited layer undergoes drying and annealing steps to remove the solvents and form the film, and via process repetition, the desired final film thickness is achieved.

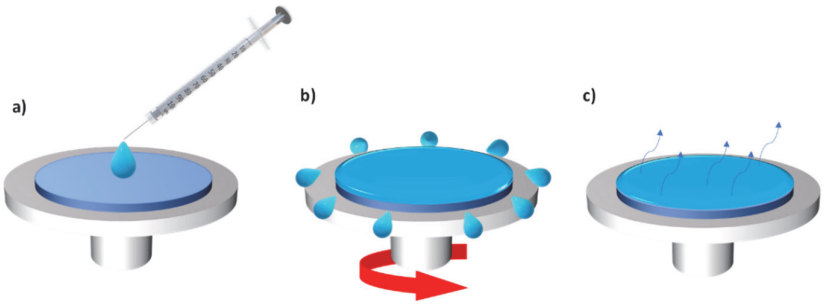


Figure 2.8 Schematic working principle of spin-coating deposition. a) Solution deposition, b) solution spreading to form a uniform thin layer, and c) solvent evaporation.

However, this technique presents some limitations related to the topography of the surface to be coated. A clean surface is required to ensure layer uniformity: the presence of surface inhomogeneity like dust or structures too thick ($\gtrsim$ 100 nm) results in an unregular deposition. Flexible substrates are challenging because of their intrinsic waviness: a carrier substrate may be necessary to ensure their flatness during the deposition step. Moreover, the drying of the solution occurring during the deposition limits the size of the area that can be coated homogeneously and consequently processable the substrates, ideally circular, with a limited size, ~30 cm (12 in wafers) in diameter.

Spin-coating is a well-established method to deposit photoresist required in the photolithographic steps used by the CMOS industry. Recently companies like PragmatIC (UK) have implemented spin-coating in their process-flow for the industrial production of flexible integrated metal-oxide TFT-based circuits. Nonetheless, the process requires the patterning of the metal-oxide films and is limited in size to wafer substrates. The relatively low throughput, the limited scalability, and the excessive solution waste relegate its utilization for the MO_x deposition in TFT manufacturing mainly to the R&D scale.

2.3.2 Printing methods

Among the printing processes, screen, flexographic, and gravure printing have been known and used for a long time, especially for newspapers and books. These technologies require a printing plate to transfer the pattern onto the substrate, like a metal engraved cylinder for gravure or a mesh for screen printing. Those techniques are well suited for high volume production such as roll-to-roll but may not be suited for all electronic components due to limitations in feature resolution (flexographic) or because of excessively thick layers (screen). Moreover, the need for a permanent printing plate or cylinder imposes some limitations: material compatibility between ink and plate limits the choice of solvents, and the unsuitability for rapid prototyping, since changing the design requires a brand-new plate to be made with a significant cost. In printed electronics, these techniques are often utilized for passive elements like PCBs or antennas[55] but also complex structures like OTFTs[56], diodes[57], and organic light-emitting diodes (OLEDs)[58]. Concerning MO_x-based TFTs manufacturing, the literature is relatively narrow. Notably, *Carlos et al.*[59] have recently demonstrated for the first time flexographic printing for AlO_x dielectric in their TFTs on PI, while *Leppäniemi et al.*[60] exploited reverse offset printing for both InO_x semiconductor and silver electrodes, yielding TFTs on PI with μ = 1.4 cm^2/Vs.

Non-contact methods usually do not require a fixed mask and therefore provide higher design flexibility. Moreover, their intrinsic non-contact nature avoids possible contamination or eventual damage. These so-called digital methods can reproduce a pattern from a CAD file that can be quickly modified, allowing cost-effective and rapid prototyping. Furthermore, different digital techniques, like inkjet, can ensure uniform thin layers with relatively fine features and therefore are adapted for MO_x thin-film transistors manufacturing. We will discuss them in detail in the next section.

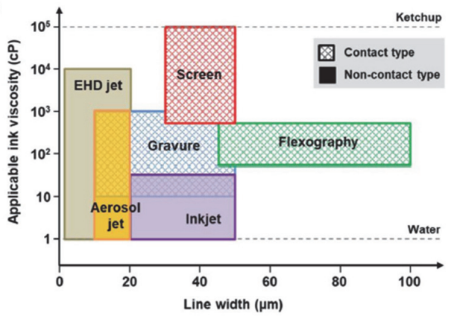


Figure 2.9 Feature resolution and viscosity operational windows of the different printing methodologies.[54]

2.3.2.1 Digital printing

Among the digital methods, we can make a distinction relative to the way jetting is performed. In a drop-on-demand (DoD) system like inkjet, the ink is ejected discretely: pushed through the small opening of the nozzle, generally, via thermal or piezoelectric actuation, the formation of the single droplets can be achieved. The quality of the printed drops is dependent on the rheology of the ink: knowing parameters like surface tension, density, and viscosity, one can predict and evaluate the shape of the resulting droplet. For inkjet, the ink formulation requires fine-tuning due to a jetting window (viscosity = 2 – 30 cP) being much narrower when compared to other techniques like aerosol jet. Substrate-ink interactions (e.g., wettability, linked to the surface energy) and the volume of the droplets, which is typically 1-10 pl for piezo-based commercial printers from Dimatix, Microfab, Xaar, define the minimum feature achievable using inkjet, which is usually in the order of tens of microns. The theory, the physics, and the challenges behind inkjet printing will be further discussed in Chapter 6.

Digital printing combines the advantages already mentioned (e.g., process flexibility, design freedom, cost-effectiveness), a low material consumption, a suitable thickness range, and resolution could be exploited in manufacturing the next generation of cheap, disposable, and more sustainable electronics. Nowadays, it is employed to produce different complex electronic components like OLEDs, [61] organic photovoltaics (OPV),[62,63], or OTFTs[64]. Appealing also to the manufacturing of metal-oxide TFTs, different reports on TFTs implementing inkjet-printed MO_x semiconductors can be found in the literature.[65] In 2007, TFTs made of a printed IZO film were for the first time fabricated using a commercial printer.[66] Since then, the number of scientific publications has rapidly increased. However, manufacturing complex devices like TFTs presents several challenges that can be even more significant when using inkjet.[67] The preparation of different and stable jettable inks, resulting in layers with a good film thickness uniformity, low roughness, and chemically orthogonal, is a challenging task. Due to the difficulties linked to multilayer stacking, most of the existing studies on the application of printing to realize metal-oxide TFTs are limited to only a single functional layer printed, with typically the MO_x semiconductor deposited on a thermal SiO_2 dielectric film.[66,68–72] As shown in Table 2.3, which summarizes the state-of-the-art regarding inkjet printed MO_x TFTs, the inkjet printing of semiconductor and dielectric layers has rarely been reported. These reports, in which the printed metal-oxide functional semiconductor is combined with printed electrodes, always involve annealing at high temperature and fabrication on rigid glass/Si substrates and a unique case on thermo-resistant PI foil.

Table 2.3 SoA of TFTs with at least two components ink jet printed. (SC= semiconductor G= gate S/D= source drain DIE= dielectric)

SC	Printed G	Printed SC	Printed DIE	Printed S/D	Max $T_{annealing}$ [°C]	Sub-strate	μ [cm^2/Vs]	Ref.
SnO_2	ATO[6]	SnO_2	ZrO_2	ATO	500	Glass	11	[73]
IGO	ITO	IGO	ZrO_x	ITO	450	Glass	7.5	[74]
ISO[7]	/	ISO	/	ITO	400	Si	10.5	[75]
IGO	ITO	IGO	$ScZrO_x$	ITO	350	Glass	12	[7]
IGTO	/	IGTO	AlO_x	ITO	350	Glass	3	[76]
ZTO	FTO[8]	ZTO	ZrO_x	FTO	300	PI	0.04	[6]
InO_x	/	InO_x	/	Ag	300	Si	3	[77]
InO_x	/	InO_x	AlO_x	ACO[9]	250	Si	19	[78]
InO_x	/	InO_x	AlO_x	ACO	250	Si	11	[79]

[6] Antimony-doped tin oxide.

[7] Indium strontium oxide.

[8] Fluoride-doped tin oxide.

[9] Aluminium-doped cadmium oxide.

Despite its versatility, inkjet printing presents a resolution limited to ~30 µm. The need for tinier features promoted the development of alternative techniques, notably electrohydrodynamic (EHD) jet. EHD is a non-contact printing that exploits an electric field, applied between the nozzle and substrate to shape and control the ejecting ink, allowing printed features with a high resolution in the sub-micron scale.[80] The technique was recently applied in the fabrication of MO_x TFTs: *Hong et al.* printed thin AlO_x dielectric films, with features down to 20 µm, on an ITO layer sputtered on SiO_2/Si to modify its conductive nature locally, converting it into a semiconducting material with thermal processes (200 – 400 °C) while simultaneously passivate the TFTs, which ultimately yielded mobility of ~6 cm^2/Vs. [81]. *Liang et al.* demonstrated instead how the technique could be employed to print MO_x TFTs fully. Their devices, manufactured on a glass substrate, necessitated a curing step over 350°C to sinter the IGZO and InO_x semiconductors, ultimately reaching mobility over 80 cm^2/Vs.[41] Despite its potential, especially for printed TFTs with a short channel, the low throughput and the practical limitations related to the need for an electric field (e.g., printing on an insulating or uneven substrate) restrict its diffusion.

Another printing method capable of overcoming the limitation in the resolution of the inkjet technique is the aerosol jet printing method. Alternatively to the methods mentioned above, in the aerosol jet process, an ink-mist is continuously ejected. This aerosol is selectively stopped by a mechanical shutter, preventing the ink from reaching the substrate where not needed to form the desired pattern. The process involves first the mist formation from the initial ink, by pneumatic or ultrasound actuation, then the aerosol is transported into the nozzle where it gets collimated by an annular ring of sheath gas. As a result of the aerodynamic focusing, the deposited features can resolve ~10 µm. The different possible actuation used to form the aerosol also provides a wide operating window in ink viscosity, ranging between 1 and 1000 cP, making it suitable for jetting a wide range of functional liquids, including ink with metallic nanoparticles and precursor inks for semiconductors and dielectrics. In printed electronics, this technique is generally employed to print metallic interconnections and contacts, where it can profit from the high-resolution and realize, by tilting the nozzle, interconnections on surfaces presenting steps requiring coverage (i.e., 2.5D printing) or on 3D structures.[82] Due to the narrowness of the deposited structures and their uneven morphology, the aerosol jet is not suited for the full-printing of roughness-sensitive devices like MO_x TFTs, requiring a very smooth interface between dielectric and semiconductor. A handful number of reports of aerosol jetted MO_x semiconductors are available requiring the implementation of ion gels dielectrics to achieve acceptable interfaces despite the excessive layer roughness.[83–85] This method will be further discussed in Chapter 6 as a possible way to print fine metal features to maximize the W/L of the printed TFTs. An overview of the ink requirements and capability per each technique is reported in Table 2.4.

Table 2.4 Comparison of characteristic features of common printing methods used in printed electronics. (Low<0.01, Medium 0.01-1, High >1) Adapted from [86].

Method/ feature	Inkjet	Aerosol jet	EHD jet	Gravure	Flexography	Screen
Printing form	Digital	Digital	Digital	Mask	Mask	Mask
Feature width [µm]	~30	10	~1	~20	~75	100
Ink viscosity [cP]	2-30	1-1000	1-10000	100-12000	50-500	500-12000
Film thickness [nm]	10-500	30-150	20-180	10-400	5-50	14000-25000
Thickness control	Ok	Good	Good	Ok	Ok	Poor
Throughput [m^2/s]	Low-medium	Low	Low	High	Medium-High	Medium-High
Printing speed [mm/s]	1.25-7000	0.1-10	0.2-8	5-1000	200-830	50-300

2.4 Reduction of the synthesis temperature for sol-gel metal-oxides

As discussed in Section 2.2, the electronic transport in the MO_x materials is highly affected by impurities and defects in the films. Therefore, during the MO_x synthesis, it is required that the impurities are removed conjointly with the precursor conversion. In the sol-gel process, the annealing via thermal treatment necessitates high temperatures (350 °C-500 °C) to yield complete precursor conversion and proper film densification. This section aims to provide an overview of the methods considered for lowering the maximum temperature required to synthesize solution-processed metal oxides. We will describe the main aspects of the different approaches and focus on their state of the art concerning the synthesis of metal-oxide semiconductors.

Throughout the development of solution-based MO_x TFTs, the excessive temperature requirements for semiconductor annealing have always been a limiting factor, restraining the range of suitable substrates to glass, silicon, and polyimide (PI), as temperature-resistant polymer. Two main pathways can be taken to minimize the energy required to synthesize a functional MO_x network: optimization and modification of chemical processes and the exploitation of alternative curing processes. After briefly introducing the frequently used methods and their respective state-of-the-art, we will focus on the core approach investigated in this thesis work, deep-UV enhanced photoactivation.

2.4.1 Chemical process optimization

Since the first reports on solution-processed MO_x TFTs, the chemistry behind the sol-gel process has been intensely investigated, leading to some interesting progress. As introduced in the previous sub-section, in MO_x sol-gel chemistry, the starting sol is composed of solvent, solute, and additives. To achieve a lower annealing temperature, one approach is to optimize the chemical formulation of the sol by a proper selection of those chemical compounds entering in its composition.

Metal salts such as metal acetates, metal halides (M-Cl[87] and M-F[88]), and metal nitrates are the typical precursors employed in sol-gel. If the reactions of the process are known, one can determine the range of temperature required, per each reaction, by measuring via thermal gravimetric analysis (TGA) the mass loss as a function of the temperature applied. We have previously described in Section 2.2.2 the reactions involved and seen that the formation of metal oxide thin-films from chemical precursors is achieved via an endothermic reaction. The steps involved, such as the precursor conversion, the film densification, and the crystalline rearrangement, can be recognized in the weight loss versus temperature graph depicted in Figure 2.10, where each weight drop identifies a loss in mass related to the steps occurring in the sol-gel process. It has been demonstrated, via TGA, that among the types of precursors, nitrates are less demanding in terms of energy and consequently the most suited for low-temperature processes.[89,90] Parallelly, other types of precursors have also been investigated and reported as effective for low-temperature approaches. However, these procedures involving alternative chemical reactions or use for the chemical doping of the MO_x films often resulted in variable results. We summarize in Table 2.5 the representative works involving nitrates and alternative precursors like metal alkoxides[91], metal ammine-hydroxo complex[48], and aqueous metal complex[45].

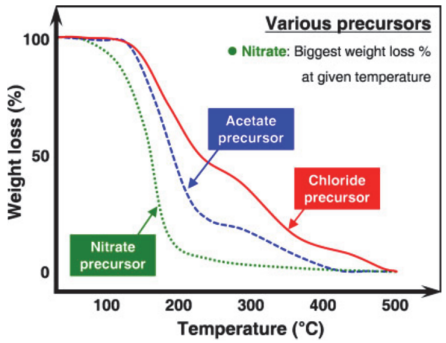


Figure 2.10 Thermal gravimetric analysis (TGA) obtained from solutions composed by different initial precursors.[89]

As previously mentioned, once synthesized, the number of chemical residuals left in the semiconductor films should be minimized as it negatively affects the quality of their MO_x network and the resulting TFT performances. This aspect is crucial when low-temperature synthesis processes are involved as the amount of energy available is limited. Notably, the nature of the solvent plays a critical role in the number of trapped residuals. The amount and type of byproducts formed during the reactions, combined with the ease in evaporating the trapped solvent molecules, influences the final energy required for the metal oxide synthesis. These aspects are strongly related to the boiling temperature (T_b) of the solution. Excessively volatile solvents may not provide process stability over time due to uncontrolled solvent evaporation and uncontrolled rheology. A high boiling temperature increases the solution stability during the processing, but also the energy demand when the final layer is deposited and the residuals removed. The solvents, which primarily have to ensure a stable and uniform dispersion of the precursors, can be divided into aqueous and organic. Organic solvents such as 2-Methoxyethanol (2ME) can successfully dissolve the nitrate precursor and ensure a homogenous dispersion. It presents a boiling point (T_b = 124 °C) that allows stable processing while ensuring the evaporation of most of the solvent low-temperature drying (i.e., > 130 °C). Those solvents can be employed alone or combined with others like ethylene glycol (EG) or ethanolamine, improving the ink stability over time while providing the possibility of modulating the rheological characteristics of the solutions (e.g., viscosity). Aqueous solvents like de-ionized water are generally less toxic than their counterparts, can dissolve nitrate precursors, and also produce fewer byproducts. However, drawbacks such as the high reactivity between the precursors and the water[92], combined with excessively low viscosity, do not make water a strong candidate for MO_x solution processing with techniques such as inkjet printing. Even if *Scheideler et al.*[78] recently demonstrated printing from aqueous inks InO_x TFTs exhibiting linear mobility up to 19 cm^2/Vs after curing the semiconductor for several hours at 250 °C on silicon, the solvents with organic chemistry are still preferred.

Additional components have been added to the standard solvent-precursors mixtures to boost the final electrical performances and lower the synthesis temperature of the metal-oxides. In the last years, different types of fuel additives have been investigated.[93,94] A combustion reaction can be initiated when fuels such as acetylacetone, sugar, and urea are added to oxidizer elements such as

nitrates. This energy, generated locally from the exothermic reaction, is then exploited for the endothermic MO_x synthesis, reducing the need for an external energy source and resulting in lower processing temperatures. [95] However, it has also been hypothesized that some solvents, such as 2ME, do not require additional combustible as they may also act as fuel themselves.[96] We will further discuss the chemical formulation of the solutions used in this work in Chapter 3.

Table 2.5 Summary of representative chemical formulation approaches applied to lower the processing temperature required to form metal-oxide-semiconductor films.

Semicon-ductor	Precursors type	Solvent type	Approach	Additives	Annealing, T_{max} [°C]	μ [cm^2/Vs]	Ref.
InO_x	Nitrate	DI water	Aqueous	Null	Thermal, 250	Up to 19	[78]
IZO	Fluoride	DI water	Chemical doping	Null	Thermal, 200	4.1	[88]
IGZO	Nitrate	2ME + NH_3	Combustion	3-Nitroacetylacetone (NAcAcH)	Thermal, 300	5.7	[94]
InO_x	Nitrate	2ME + NH_3	Combustion	Acetylacetone (AcAcH)	Thermal, 250	11.1	[97]
InGaO	Nitrate	2ME + NH_3	Combustion	Acetylacetone (AcAcH)	Thermal, 300	Up to~17.6	[32]
ZTO IZO InO_x	Nitrate (chloride for Sn)	2ME+ NH_4NO_3	Combustion	Acetylacetone (AcAcH) Urea	Thermal, 200	6	[93]
IGZO	Nitrate	2ME + NH_3	Combustion	Acetylacetone (AcAcH)+ Sugar	Thermal, 300	Up to 7.5	[98]
InO_x	Nitrate, Fluoride, Chloride, Acetate	DI water	Precursor	Null	Thermal, 250	Up to 36.3 (nitrate)	[45]
IZO	Alkoxide cluster	2ME + methoxy- iso-propanol	Precursor	Null	Thermal, 230	~10	[91]
ZnO	Ammine-hydroxo complex	NH_3	Precursor + pH control	Tetramethylammonium hydroxide	Thermal, 150	0.42	[48]

2.4.2 Alternative curing approaches

As mentioned previously, conventional thermal approaches for MO_x TFTs manufacturing necessitate high temperatures (> 350 °C) to achieve functional and performing devices. This condition is related to the energy required to convert the solution containing the precursors into a dense MO_x semiconductor film. Numerous studies adopting different approaches have been carried out to overcome the thermal constraints associated with their synthesis: notably, the exploitation of different thermodynamic conditions during the annealing, such as the atmospheric pressure, by controlling the gaseous composition during the treatments and the exploitation of alternatives to thermal sources of energy. In this sub-section, we present the relevant state-of-the-art on the topic, which is summarized in Table 2.6 and Table 2.7, and describe the different methods applied.

Thermal annealing performed under different gas pressures, like high-pressure annealing in O_2 and inert atmosphere [99] or vacuum post-treatments[100], have been reported operative TFTs at relatively low temperatures of 200 – 250 °C. These methods influence the thermodynamics of the conversion process, lowering the temperatures required for the oxide synthesis and enhancing the control of the final density of the film. *Tak et al.* used a high-pressure post-treatment at 5 atm in H_2 followed by second treatment in O_2 atmosphere at a variable pressure (5 – 20 atm), to increase the density of their IZO semiconductor films thermally treated at 280 °C in air and achieve a μ~4.5 cm^2/Vs.[99] A vacuum-facilitated condensation post-annealing, obtained via a vacuum byproduct-evaporation, was applied by *Hwang et al.* to convert their MO_x solution into InO_x at a low temperature of 125 °C resulting in mobility of about 2.43 cm^2/Vs.[101] *Oh et al.* further explored the approach and integrated a preliminary phase into a humid environment to the vacuum annealing process to fabricate spin-coated InO_x TFTs at 140°C having mobility of ~2 cm^2/Vs on PEN[10] substrate.[102] Other forms of assisted annealing involving plasma have been demonstrated as well. *Jeong et al.* exploited a cold H_2 plasma to remove hydroxides and passivate their ZnO films, reaching μ~1.4 cm^2/Vs for a processing temperature of 140 °C.[103] *Li et al.* reported similar results: their process with an NH_3 plasma promoted the chemical reactions and their InO_x TFTs showed μ~1.3 cm^2/Vs as well for an annealing temperature of 140 °C.[104] However, these methods require additional equipment like pressurized chambers, vacuum pumps, or specific gas atmosphere (H_2 or NH_3 for the plasma), thus reducing their cost-effectiveness due to their implementation complexity in a printing process line.

The use of alternative electromagnetic sources to replace or assist thermal annealing has been widely investigated. As the interaction of the radiations is dependent on the nature of the materials involved, the effectiveness of these methods relies on the optical

[10] PEN = Polyethylene napthalate.

window of adsorption of both the substrate and layers composing the device. Also, their working principle differs according to the type of radiation involved. The microwave range was exploited by *Jun et al.* to excite the aqueous solvent molecules of their ZnO solutions and achieve μ~0.7 cm^2/Vs at 140 °C.[47] *Xia et al.* instead integrated the infrared radiations into the thermal process to improve the impurities removal in their IGZO films and reach mobility up to ~68 cm^2/Vs at 230 °C.[105]

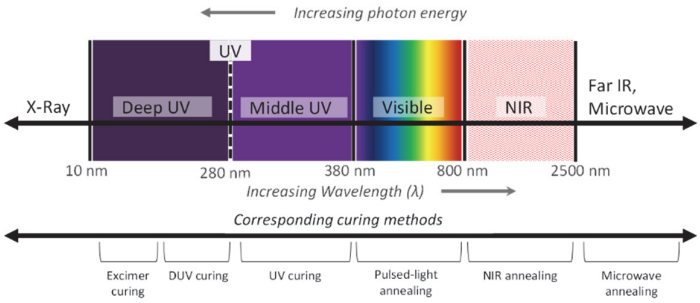


Figure 2.11 Electromagnetic spectrum and the correlated curing techniques described in the literature, applied to solution-processed MO_x films.

Another method that attracted the attention of the researcher is the so-called *pulse light annealing*, where a light source emits energetic impulses for a short time (milliseconds range). The method was developed for the sintering at low-temperature of metal conductors deposited on optically transparent sensitive foils.[106] The light source very quickly raises the temperature (several hundred degrees Celsius) of those absorbing metallic structures present on the exposed surface but, the short duration of the exposure (milliseconds) preserves the transparent substrate from thermal damages. This method, which is appealing for industrial applications thanks to its rapidity, presents a fundamental limitation: the light, generally emitted from a xenon lamp, is mainly generated in the visible spectrum and is therefore ineffective on transparent materials. It works well for metals but requires some adjustments to be effective on metal oxides that do not absorb in the visible spectrum. Few strategies to overcome this limitation have recently been reported: *Gilshtein et al.*[107] added an organic dye to improve the light adsorption of their ITO conductors, while *Yarali et al.*[108] yielded on PEN foils TFTs with a maximum process temperature of 130 °C and mobility ~ 2.3 cm^2/Vs, employing spin-coated InO_x/ZnO as semiconductor and exploiting the metal gate of their bottom-gate structure as light-absorbing elements. *Moon et al*. instead combined different sources: they integrated pulsed-light annealing with near-infrared (NIR) to convert the IGZO precursors; nonetheless, it necessitated extra deep-ultraviolet (DUV) annealing to yield mobility 7.7 cm^2/Vs and I_{on}/I_{off} ratio >10^6.[109] In the context of MO_x synthesis, the part of the electromagnetic spectrum below the visible (λ < 380 nm) is of high interest since the majority of the precursor solutions are opaque only in that range. The approaches that involve light sources in this wavelength window will be discussed in detail in the next section.

Table 2.6 State-of-the-art curing approaches applied to metal-oxide semiconductors involving energy sources emitting in the visible range or above (λ > 380 nm).

Semiconductor	Substrate	Annealing method	T_{max} [°C]	μ [cm^2/Vs]	Ref.
IZO	Si	High Pressure	280	4.5	[99]
IGZO	Si	IR	230	68	[105]
IGZO	Si	Microwave	180	6.7	[110]
ZnO	Si	Plasma H_2	140	1.4	[103]
InO_x	Si	Plasma NH_3	140	1.3	[104]
InO_x	PEN	Vacuum	140	2	[102]
ZnO	Si	Microwave	140	0.7	[47]
InO_x/ZnO	PEN	Pulsed-light annealing	130	2.3	[108]
InO_x	Si	Vacuum	125	2.4	[101]
IGZO	Glass	Pulsed-light annealing	100	8.8	[111]
ZnO	Si	Pulsed-light annealing	90	0.05	[112]
IGZO	Si	Pulsed-light annealing	N.A	10.5	[113]
IGZO	Si	NIR+Pulsed-light annealing+DUV	N.A	7.7	[109]

2.4.3 Photoactivation via deep-ultraviolet (DUV) treatment

The different types of radiation aforementioned can increase the temperature locally, like pulsed-light annealing, or address selectively some molecules, like microwaves. However, the photons can also dissociate molecular bonds and trigger chemical reactions. The energy of a single photon is only dependent on its wavelength: it can be derived from the following equation $E = \frac{hc}{\lambda}$ where h is the Plank constant, c is the speed of light, and λ is the wavelength.[11] By knowing the energy level required to achieve the bond cleavage[12] and the chemical composition of the elements involved in the process, one can identify the minimal energy required for successful photoactivation and select accordingly the light sources that can be applied. Examples of chemical bonds and the corresponding wavelength necessary to break them apart are provided in Figure 2.12.

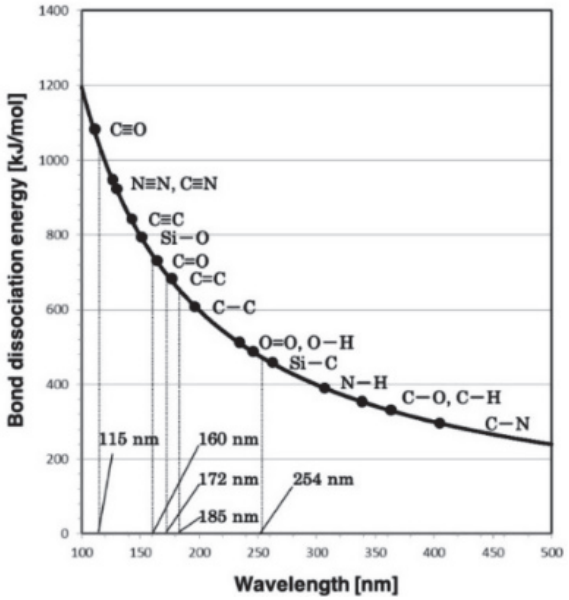


Figure 2.12 Energy level, and correspondent wavelength, required to break the typical chemical bonds present in the various molecules.[114]

For metal-oxide films manufactured via a sol-gel process, the chemical bonds of the molecules present in the solvents and precursors determine the energy levels required for photoactivation. For a solution involving 2ME as solvent and nitrate compounds as precursors, the bonds involved are nitric bonds (N–O ~ 350 kJ/mol due to the resonant bond present in the nitrate ion) and organic bonds (C–H = 413 kJ/mol, C–C = 347 kJ/mol, and C–O = 358 kJ/mol).[115] The light sources capable of emitting photons with a sufficient energy level to dissociate these bonds are those possessing wavelengths below the middle-UV range (λ < 280 nm). The optical adsorption range was also confirmed via UV-vis spectroscopy of the precursor solution.[116] The effectiveness of this type of UV light for the MO_x sol-gel process has been known since 1995 when *Van de Leest* applied it on metalorganic compounds like TEOTi[13] using a deep-ultraviolet (DUV) source.[117] However, only in 2012, *Kim et al.* demonstrated for the first time the effectiveness of DUV photoactivation for a spin-coated IGZO film: the process resulted in TFTs manufactured on a transparent polyarylate (PAR) foil with mobility of 3.77 cm^2/Vs after 120 minutes of treatment at 150 °C.[118]

We will now describe some of the mechanisms associated with the photoactivation via DUV of metal-oxide precursors involved in a sol-gel reaction process. The precursor conversion and the enhanced impurities removal result from different chemical reactions taking place during the DUV irradiation. The energetic photons can decompose via photolysis of those bonds with lower energy, such as the N–O of the nitrate precursors, leading to the photoinitiation of the M–O–M networking. Simultaneously, the organic bonds of the residuals, like C–H, C–C, and C–O, are also cleaved; this photodecomposition of the impurities results in smaller molecules that are easier to remove.[119] As a byproduct of these reactions, radicals like hydroxyl radicals (HO*) are produced; this in-situ radical formation catalyzes the mentioned reactions and enhances the condensation reaction of the precursors, improving the film densification.[120] Concerning the radical formation, the nature of the gaseous atmosphere involved during the exposure plays a role. When

[11] $h = 6.626 \times 10^{-34}$ [J s] $c = 2.998 \times 10^{8}$ [m/s].
[12] It is expressed in eV or in [kJ/mol].
[13] TEOTi= Tetra-ethyl-ortho-titanate.

the light exposure is performed in an oxygen-rich environment, due to ozone (O_3) creation, there is a loss in terms of delivered energy to the surface. However, the presence of such reactive species increases the number of radicals, thus improving the sol-gel synthesis.[35]

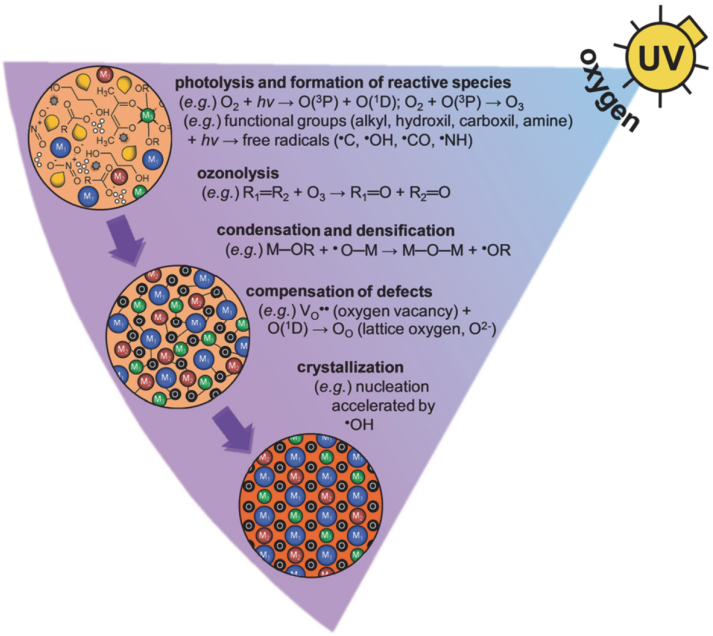


Figure 2.13 Summary of the chemical reactions triggered from exposure to a DUV light in an O_2-rich environment.[35]

A large variety of UV sources is nowadays available, with different light, radiation intensities, and emission spectra according to the nature of the emitting gas used. Few works report on UV sources having a limited emission in the middle UV range (λ<280 nm) but still capable of converting the MO_x precursor thanks to their high intensity. *Scheidler et al.* exploited a powerful lamp delivering a light intensity of 1 W/cm^2 to manufacture by printing InO_x TFTs on Si at 250 °C. Implementing a MO_x gate dielectric synthesized with the same method, they reported linear mobility as high as 12 cm^2/Vs. [79] *Garlapati et al.* implemented a laser curing (He-Cd laser) to anneal their nanoparticle-based printed InO_x semiconductor on PEN substrate achieving mobility of ~12 cm^2/Vs.[38]

One of the most popular DUV sources is the low-pressure Hg lamp which presents two prominent emission peaks at 253.7 nm and 184.9 nm, corresponding respectively to 90 % and 10 % of the optical output.[121]Using this type of lamp (UV253H from Filngen, intensity of ~28 mW/cm^2), the group from professor *Sung Kyu Park* at Chung-Ang University in Korea established a synthesis protocol for IGZO films at 150 °C, which is the lowest temperature reported with this approach, and exploited it to investigate other aspects of TFT solution processing.[111,118,122–125] They required a 120 min long process in an N_2 environment to avoid energy dissipation due to ozone formation in an O_2-rich environment, which inhibited converting their precursor solution into operational IGZO. Even if partially successful after 60 minutes, their protocol required 120 minutes to ensure film densification. They also pointed out how DUV alone may not be effective and highlighted the necessity of supplying some heat during the DUV treatment, generated by the lamp or provided externally to ensure a proper precursor conversion.[118] *Park et al.* synthesized an InO_x semiconductor film to form TFTs on PI that achieved mobility ~8 cm^2/Vs by using the same type of UV lamp (UV253H) and similar processing conditions but with an intentional substrate heating at 150 °C during the 30 min long UV exposure in an N_2 environment.[120]

Another type of source that has been considered for photoactivation is the excimer lamps, in which a gas of dimers in the excited state can generate an emission spectrum with almost a single peak emission. The confined emission spectrum and the higher level of energy achievable can increase the irradiance[14] of the source and its effectiveness. Depending on the type of dimer, different parts of the electromagnetic spectrum can be covered, with wavelengths ranging from λ =351 nm to λ=108 nm, when using with XeF and NeF, respectively.[35] Among them, sources (both in laser and lamp form) utilizing Xe_2 or deuterium (D_2), λ=172 nm and λ=160 nm respectively, have been recently reported for processing at low-temperature MO_x TFTs. *Carlos et al.* recently reported a similar "in-situ" protocol applied to printed InO_x films on PI, which yielded after 90 min of exposure at 180 °C TFTs with a mobility of ~2.9 cm^2/Vs.

[14] Expressed as the radiant power per unit of area [W/m^2].

[59] Table 2.7 collects the relevant literature regarding those reports involving DUV photoactivation of metal-oxide-semiconductor films, considering a maximum temperature processing, $T_{process}$, ≤ 200 °C.

The large variety of UV source types available, having different intensities and emission spectra, combined with a flexibility in processing parameters, like exposure in different gaseous atmospheres or the possibility to couple the irradiation with thermal treatments, pushed the interest of the researchers for this DUV photoactivation approach. The DUV annealing method, which could be implemented in industrial process-flow with limited capital investment, is currently one of the best candidates for the future mass production of solution-processed MO_x devices on flexible polymeric substrates. However, some challenges still need to be addressed adequately while considering the few limitations of the approach.

- Due to limited light penetration in the materials, complete photoactivation occurs only when the film treated is thin (< 20–30 nm). DUV is ineffective when applied to thicker films and will result in low MO_x networking due to excessive impurities or unconverted compounds. A deposition process yielding uniform thin layers is essential to ensure the functionality of the MO_x active layers.
- Most of the reported annealing procedures require relatively rigorous environmental conditions (mainly inert environment to avoid ozone formation) and a rather long annealing time (> 60 min). A further investigation of the underlying mechanisms, with a possible optimization of the protocols, is still required to minimize the process duration and thermal budget of the MO_x synthesis.
- The majority of publications reported thus far on sol-gel-based TFTs involve spin-coated semiconductors. These are often deposited on Si wafers or combined with vacuum-based gate dielectric layers. The few examples of printed and photoactivated metal-oxide semiconductors were processed only on thermo-resistant substrates like PI and Si. TFTs involving both printed MO_x semiconductor and dielectric films and successfully photoactivated at low temperature on any thermo-sensitive substrate have not been reported yet.

Table 2.7 Literature summary regarding approaches involving DUV photoactivation to manufacture sol-gel-based MO_x TFTs, considering a maximum processing temperature ≤ 200 °C. (Semiconductor was obtained via sol-gel and spin-coated if not mentioned otherwise.) (PVP= poly(4-vinylphenol) NP= nanoparticles)

Substrate	Semiconductor	Dielectric	UV lamp	Annealing conditions	T_{max} [°C]	Process duration [min]	μ [cm^2/Vs]	Ref.
Si	IZO	SiO_2	Excimer D_2	N_2	200	30	1.3	[126]
PEN	ZnO NP	ZrO/AlO_x	Metal Halide lamp	N_2	180	90	4-5	[127]
Si	IGZO	AlO_x	Excimer D_2	N_2	180	30	6.3	[128]
PI	Printed InO_x	Printed AlO_x	Excimer D_2	N_2	180	90	~2.9	[59]
PI	IGZO	AlO_x	DUV	N_2	150	120	5.9	[123]
PI	IGZO	AlO_x/ZrO	DUV	N_2	150	120	~8.5	[129]
PEN	Printed InO_x	ALD Al_2O_3	Excimer D_2	N_2	150	180	~1	[34]
Si	IZO InO_x	SiO_2	UV	Air	150	15	>30	[116]
PI	IGZO	AlO_x	DUV	N_2	150	120	~8	[120]
PI	IGZO	Zr:AlO_x	DUV	N_2	150	120	~8.6	[130]
Si	IGZO	AlO_x	DUV	N_2 + humid treatment	150	120	~6.9	[122]
PAR	IGZO	AlO_x	DUV	N_2	150	120	~3.8	[118]
Si	IZO	Solution processed SiO_2	DUV	N_2	150	150	16.2	[131]
Si	InO_x	SiO_2	Excimer Xe_2	N_2	140	15	4.4	[132]
PEN	Printed IGZO	PVP +ALD Al_2O_3	Laser	NA	120	NA	~4.2	[133]
PET	ZnO NP	Organic-inorganic composite	UV	NA	115	NA	0.5	[134]
PEN	Printed InO_x NP	Organic dielectric	He-Cd laser	NA	NA	<1	12	[38]

2.5 Combining solution-processed MO_x dielectric and semiconductor

High-k inorganic gate dielectrics like MO_x are an essential component for actual and future high-performance silicon and printed TFTs. Thanks to the large pool of possible materials (single/multiple components, ion doping), their enhanced dielectric characteristics (high-k, large bandgap >5 eV), and the wide range of deposition methods (gas-phase, solution processing), MO_x dielectrics emerged as a valid alternative to the traditional SiO_2 dielectric. In the past years, parallelly to the MO_x semiconductors, low-temperature approaches for solution-processed MO_x gate dielectric have also been investigated. In this context, aluminum-oxide-based insulators have been identified as one of the most promising materials.

In the frame of the SFA FOxIP project and with the final goal of pursuing fully solution-processed devices via printing, we aimed at combining the semiconductor and dielectric layers, both made of metal-oxides and solution-processed. While we focused on developing the semiconductor ink, Sami Bolat through his Ph.D. work, and the collaborators at Empa, developed yttrium-doped aluminum oxide ($YAlO_x$) and aluminum oxide (AlO_x) dielectric inks. Starting from the recipe for the ink-jettable $YAlO_x$ reported in their publication [135], an adapted AlO_x/$YAlO_x$ printed dielectric stack was implemented in the architecture of the TFTs researched in this thesis. In Chapters 4, 5, and 6, we will discuss in detail the implementation of these inks and the improvements made in their processing at low temperatures.

The goal of this section is to introduce metal-oxide dielectrics, to explain their role as gate dielectric in TFTs, and to precise some of the interactions occurring between the semiconductor and dielectric layers. Then, to better analyze the performances of the solution-processed metal-oxide TFTs developed in the following chapters of the thesis, we will address specific phenomena occurring, such as dielectric-induced instability (i.e., frequency dependence), when integrating by solution processing a metal-oxide gate dielectric with a metal-oxide semiconductor.

2.5.1 Basics of MO_x dielectric

Silicon dioxide has been employed for decades in CMOS technology for its excellent insulating characteristics. However, the continuous need for device miniaturization exposed its limits as an insulator.[136] When SiO_2 is utilized as a dielectric layer in TFTs, these devices require relatively high operation voltages to reach the saturation regime due to a small capacitive coupling. On the contrary, high-k materials provide high capacitances without excessive leakage related to a diminished film thickness.

Different classes of inorganic dielectrics with high relative permittivity ε_r (or k) > 3.9[15], like nitrides (SiN_x, AlN_x), metal-oxides, perovskites, and hybrid combinations, have been investigated. The dielectric film is a layer that aims at insulating the gate electrode from the other TFT electrical components. It has a crucial role in TFTs since it provides capacitive coupling with the active layer and enables the field effect. According to Equation 2.3, for fixed semiconductor and geometrical parameters, increasing the areal capacitance of the dielectric results in TFTs with higher on-currents. The stronger capacitive coupling also improves the subthreshold swing (SS) and reduces the operating voltages (i.e., saturation voltage).

Parameters like the leakage current or the breakdown voltage ultimately characterize the quality of an insulator. Insulators inevitably allow some charges to flow from the source/drain electrodes to the gate electrode. This amount of current is measured at the gate (I_{GS}) and is defined as leakage current $I_{leakage}$. The number of undesired charges flowing depends on the material bandgap, which should be > 5 eV for insulating material.[137] The magnitude of this current loss is dependent on the applied electric field. When the voltage applied exceeds a specific value called breakdown voltage V_{BK}, an electrical breakdown occurs in the film, and the insulator becomes electrically conductive. By measuring the value J_{leak} (current flow per area) as a function of the applied electric field, the maximum applicable gate voltage at a given film thickness can be evaluated. This value should ideally be 1.5x higher than the TFT maximum operating voltage before breakdown. Therefore, a dielectric with high breakdown strength and leakage densities lower than 10^{-6} A/cm^2 at 1MV/cm is highly desirable to minimize the current losses. Decreasing the thickness of the layer is a method to increase the capacitance C_{ox}, but lowering the thicknesses also increases the breakdown probability due to film defects like pinholes and the leakage due to tunneling currents.[138]

[15] The relative permittivity of SiO_2.

2.5.1.1 The selected dielectric stack: $AlO_x/YAlO_x$

Among the different metal-oxides that demonstrated high-k and low leakage currents, aluminum oxide (AlO_x, k~9) is probably the most diffused. Well-established in the conventional semiconductor industry, it can be deposited in a wide range of temperatures (down to room temperature), this using various standard deposition methods, like sputtering and especially ALD, forming high-quality, dense films. Moreover, the amorphous nature of the AlO_x films, even when processed at high temperatures (~600 °C), reduces the number of possible leakage pathways compared to their crystalline counterparts.[138] Parallelly, methods for the solution processing of AlO_x were also explored. As it happened for the MO_x semiconductors, different precursors have been used, e.g., aluminum chloride[139] and aluminum nitrates[78]. Following the trend in lowering the processing temperature of metal-oxide TFTs, solution-processing of AlO_x films at temperatures ranging from 250 °C to 150 °C [138], and even down to 60 °C [123], have been demonstrated via DUV synthesis.

The continuous research aiming at low-power consumption transistors led to the exploration of different approaches to improving the characteristics of the gate dielectric, e.g., reduction of the leakage and increase of the areal capacitance. In this frame, the doping of AlO_x with compounds that can increase its total permittivity, yet maintaining an adequate bandgap, was investigated. Among the possible materials, yttria (Y_2O_3, k~15), already employed as a dielectric in TFTs [140], was applied as a doping compound for aluminum oxide. The successful use of spin-coated dielectrics composed of yttrium-doped-aluminum oxide ($YAlO_x$) in TFTs was reported by *Lee et al.*, yielding high mobility ~53 cm^2/Vs and a low leakage current density of ~ 10^{-8} A/cm^2.[141] However, in this work, a process temperature up to 400 °C was required. *Koslowisky et al.* reported promising results with similar materials but requiring a minimum processing temperature of 350 °C.[142] The project partners at Empa succeeded in realizing performing devices with inkjet-printed $YAlO_x$ processed at 150 °C. The layers, cured via DUV annealing in combination with thermal treatment, were deposited on a PI substrate and integrated with a sputtered IGZO to eventually yield TFTs with mobility up to 4.3 cm^2/Vs.[135]

Intending to achieve fully solution-processed MO_x TFTs at low temperature, most of the TFTs realized and studied during this thesis employ a solution-processed dielectric stack composed by AlO_x and $YAlO_x$, which was developed in collaboration with the project partners, as it can provide lower leakage levels and less frequency dispersion than AlO_x alone. We will now discuss how the MO_x dielectric and semiconductor layers interact during the device operation and how the stack can be characterized.

2.5.2 Semiconductor-Dielectric interactions in MO_x TFTs

It is clear by now that a TFT is a complex electrical device where each component has a role and presents peculiar electrical characteristics. The semiconductor assures a charge-transport in the active channel, the dielectric ensures low leakage and good capacitive coupling, source and drain contacts inject and extract the charges from the semiconductor, whereas the gate electrode modulates charges density in the channel. However, these characteristics taken singularly do not guarantee the performance of a device. In this frame, the interface between dielectric and semiconductor layers plays a fundamental role in the electrical performance of the final device. In bottom gated TFTs, corresponding to the architecture investigated in this work, the morphology of the dielectric film, located underneath the semiconductor layer, can strongly influence the whole system: a surface with low roughness, < 1 nm ideally, minimizes the charges scattering in the active channel. High surface energy and high hydrophilicity, which simplify the subsequent semiconductor deposition, are as well desirable. The presence of charge-trapping sites at the interface also impacts the behavior of a transistor: deep traps can immobilize part of the charges generated during the subthreshold state, resulting in higher SS values and reduced switching capability.[143] An abrupt transition between the two layers may result in dangling bonds and other defects, increasing the number of traps.[144] Therefore, an interfacial region with a sleek transition between the layers is beneficial.

Among the different possible electrical characterizations, capacitive measurements as a function of the voltage or the frequency (respectively C-f and C-V) can provide information regarding the quality of the deposited dielectric and the quality of the interface of the metal-oxide double layer stack. From the investigation of C-V curves obtained from metal-insulator-semiconductor-metal (MOS) structures (example in Figure 2.14), one can examine the switching performance of the device and identify non-ideal behavior, like hysteresis and the presence of traps at the interface. Depending on the frequency applied in the C-V measurements, different parameters like threshold voltage can be extracted. Notably, the trapping/de-trapping phenomenon cannot be observed at high frequency, requiring specific characterization techniques operating at low frequency (almost DC), such as quasi-static C-V (QSCV) or very low-frequency C-V (VLFCV) analysis.

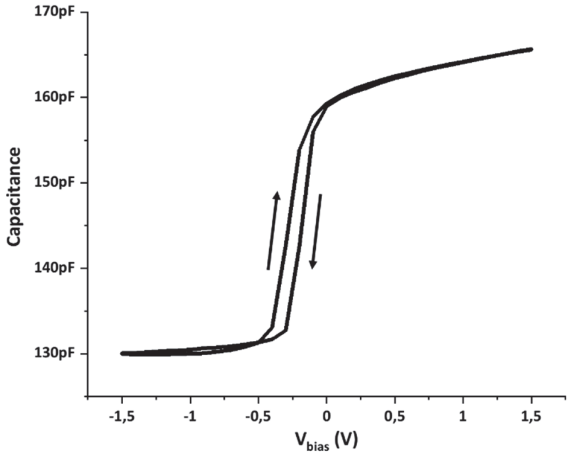


Figure 2.14 Example of C-V characteristic extracted from a MOS structure made of the typical material stack employed in this thesis: Au/Ti/IZO/AlO_x/$YAlO_x$/Cr. (frequency= 1 kHz)

2.5.2.1 Influence on TFTs performance due to solution processing of the metal-oxide dielectric

In the last years, with the diffusion of solution-processed dielectrics, the number of TFTs reporting remarkable performances, notably high mobility, has been rapidly increasing. This phenomenon is even more intriguing considering that, in many reports where the same semiconductor is processed in parallel on both standard (e.g., thermal SiO_2) and solution-processed dielectrics (e.g., spin-coated AlO_x), this performance enhancement (up to 10 times of difference) is present only in the solution-processed ones.[145] Many studies have been carried out about the topic, but an unequivocal explanation has not been found yet. This, and other aspects related to the use of solution-processed metal-oxide dielectric, will now be discussed.

The dielectric material is an insulator that, once subjected to an electric field, can be polarized. The polarization phenomenon is not instantaneous and depends on the molecules involved and on the nature of their polarization. Different types of polarization, like electronic, ionic, or orientational polarization, occur only in specific frequency ranges, and each ultimately contributes to the capacitance of the material, as depicted in Figure 2.15.

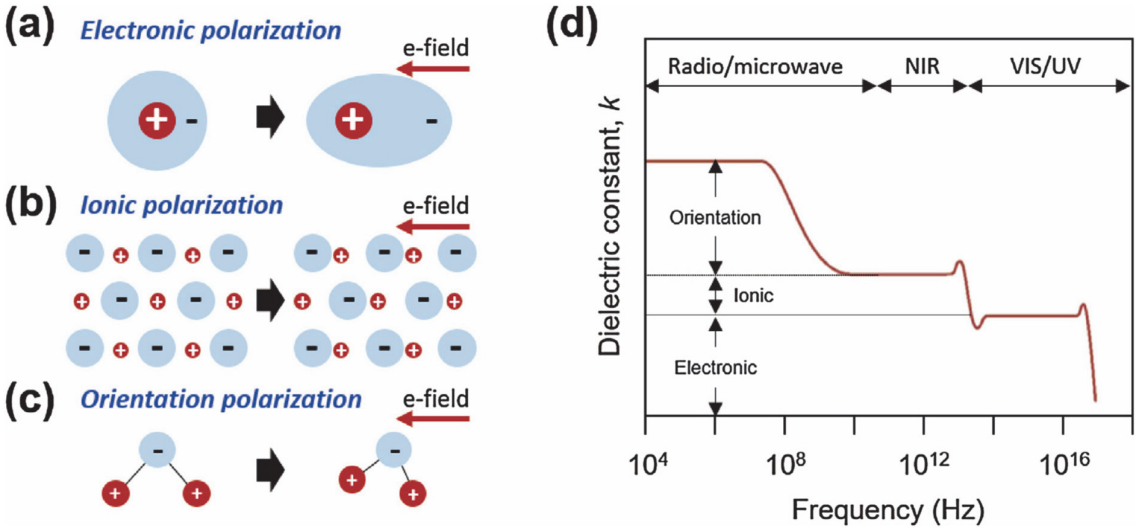


Figure 2.15 The basic mechanisms of dielectric polarization. Schematics of (a) electronic polarization, (b) ionic polarization, (c) orientation polarization. (d) Electronic, ionic, and orientation polarization contribute to the overall dielectric constant as a function of the frequency applied.[146]

For a TFT, the correct characterization of the dielectric layer with the proper estimation of its dielectric constant and the eventual dependence on the frequency is essential. As seen in Equation 2.3, the mobility is a function of the capacitance per area C_{ox}, which

can be obtained by measuring the capacitance in a simple parallel plate structure MIM (metal-insulator-metal), as depicted in Figure 2.16.

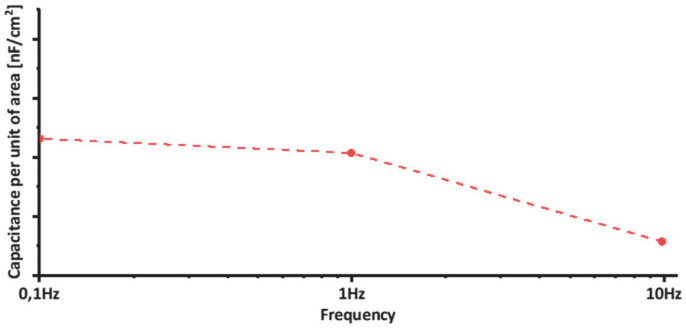


Figure 2.16 Example of C-f characteristic at low frequency, extracted from a MIM structure made of the typical material stack employed in this thesis: Al/AlO_x/$YAlO_x$/Cr.

However, in a frequency-dependent dielectric, a measurement at low-frequency (< 1 Hz) needs to be performed to account for possible contributions from slow responsive polarizations and minimize the eventual overestimation of the mobility. Considering that the transfer characteristic used to evaluate the mobility is obtained in DC, the actual capacitance of the TFT could be significantly higher than the one measured at high frequency, resulting in extraordinarily high (μ > 100 cm^2/Vs) but unrealistic mobility values.[21] For the design of devices working in AC, notably high-end applications like LCD panels, an accurate mobility estimation is crucial. The figure of merit called *transit frequency* (f_T), which represents the highest operation frequency for the transistor, is mobility-dependent. Therefore, a mobility miscalculation may lead to a wrong geometrical design of the TFTs, compromising the correct operation of the final devices. High-quality dielectrics do not present a strong frequency-dependency: high-k materials, which cannot follow the variation of electric field changes at high frequency, usually exhibit only a significant capacitance change in the megahertz range, while low-k materials show constant values independently from the frequency. Such behavior is typical for those layers manufactured via standard vacuum-based processes, like ALD AlO_x or thermal SiO_2. However, the capacitance of solution-processed dielectrics, especially if cured at low temperature, is likely affected by impurities such as residuals hydroxides trapped in the layer, resulting in frequency dependence of their behavior.[147]

For most metal oxides, water adsorption is thermodynamically favored (Figure 2.17). The adsorption is usually limited to the surface, but it may affect the whole layer in a film porous/not sufficiently dense.[53] *Daunis et al.* demonstrated that some metal oxide dielectrics, such as AlO_x, are more inclined to moisture adsorption and explained how this affects the electrical characteristics. They identified water molecules in the film as the source of counter-clockwise hysteresis, suggesting that, when the portion of dielectric in contact with the gate contains water, an electron donation from dielectric to the gate occurs, increasing the electric field and the electron concentration in the active channel.[147] A similar electron donation mechanism was suggested by *Zeumault et al.*: the mobility boost is attributable to the presence of donor-like traps in their ZrO_2 dielectric, acting as a source of electrons donation towards the semiconductor layer.[148]

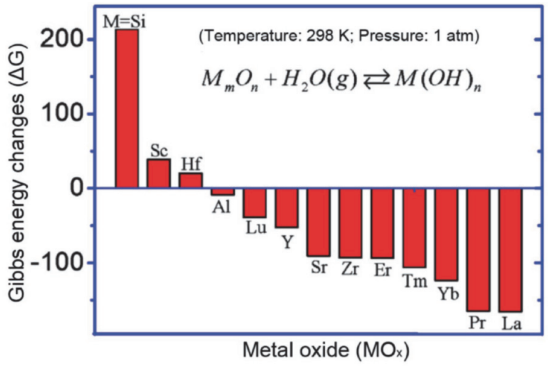


Figure 2.17 Gibbs energy changes required for moisture adsorption, under standard conditions, for some high-k oxide dielectrics.[149]

Alternatively, *Heo et al.*[150] attributed the increase of areal capacitance to the presence of mobile ions in the film, which resulted in the formation of an electric double layer (EDL) at the interface between their AlO_x dielectric and InO_x semiconductor, thus enhancing the electron accumulation in the active channel. Recently, *Liang et al.*[151] further expanded this theory, adding to the EDL formed by electrostatic accumulation, a pseudo-capacitance caused by Faradaic charge transfer. They also theorize additional doping, voltage-dependent, of their InO_x semiconductor by the residual hydrogen ions in their alumina dielectric, resulting in a higher carrier density in the active channel but likely unsaturated TFTs. However, from their results, it is not clear if the mechanism involves mobile hydroxyl ions.

Different characterizations can be carried out to investigate the presence or not of the phenomena described above and better understand the electrical behavior of solution-processed metal-oxide TFTs. Among them, the investigation of the C-f characteristics at a very low-frequency range (down to 10 mHz) is of interest. These curves can be obtained from MIM structures and employed to correctly estimate the extracted channel mobility and identify eventual interdependence between capacitance and frequency/voltage, as recently shown by *Zhuang et al.*.[97]

2.5.2.2 Synaptic behavior

Among the possible attractive applications in future electronics, neuromorphic computing is one of the most fascinating. With the goal of mimicking the chemical interconnections between the synapsis, different types of two-terminal electronics, like organic-based memristors (with conducting polymers like PEDOT:PSS) and optoelectronic memristors, have been reported.[152,153] Three-terminal devices, which can combine signal processing and memory functions, are usually preferred to their two-terminals counterparts. The so-called synaptic (or neuromorphic) TFTs have been demonstrated using different classes of dielectrics, such as electrolytes,[154], ionic liquid,[155], and metal oxides[156]. Solution-processed MO_x dielectric layers can naturally present the characteristics required to obtain a memory behavior, such as charge trapping and hysteresis. This behavior was exploited in IZO/AlO_x TFTs developed in the frame of the SFA FOxIP project. (Figure 2.18) The combination of the spin-coated IZO film developed in this thesis with a printed AlO_x dielectric on a silicon substrate successfully exhibited the synaptic behavior. The potential for neuromorphic applications has been further demonstrated by integrating such devices into an acoustic system capable of replicating the whole audio range (up to 50 kHz).[157]

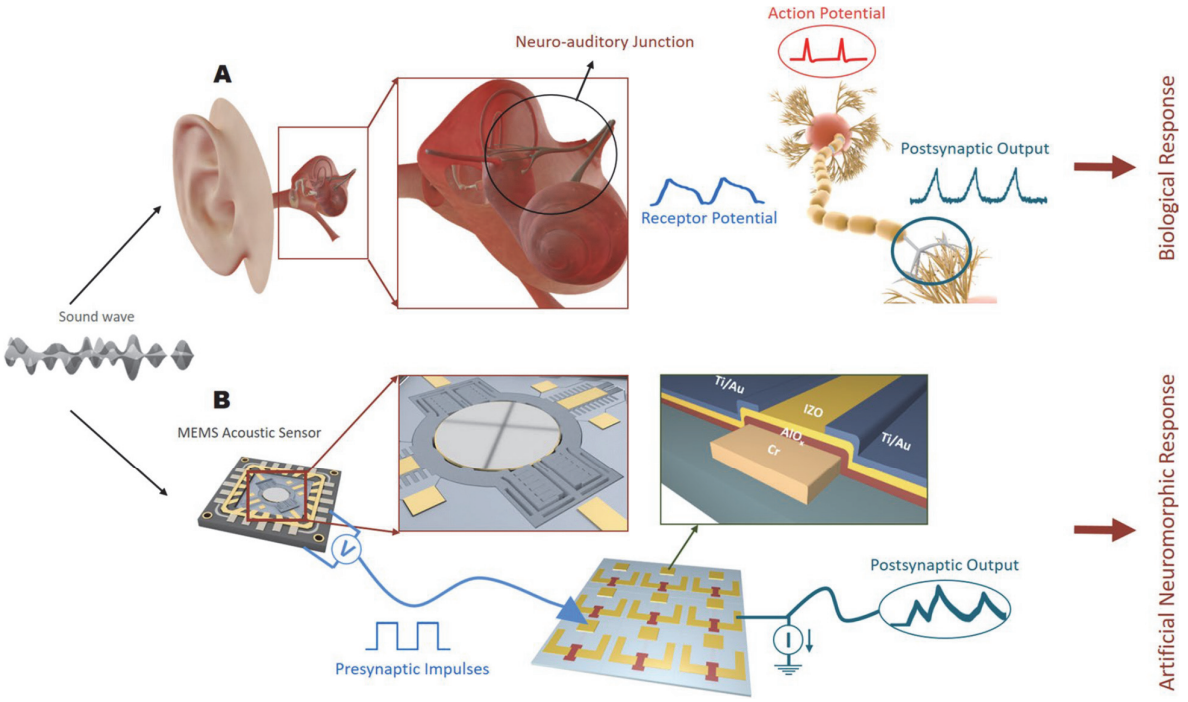


Figure 2.18 Example of solution-processed MO_x TFTs acting as synaptic transistors in neuromorphic applications.[157]

2.6 Printing MO_x TFTs on flexible and temperature-sensitive substrates

The ultimate goal of this thesis was to establish methods to manufacture by printing MO_x TFTs onto flexible and thermosensitive substrates. Compared to conventional substrates, like glass and silicon, their flexible nature and inferior mechanical/chemical/temperature stability pose technical challenges. The chemical and temperature compatibility of the methods used to synthesize the MO_x active layers and other aspects, like the potential need for a planarizing buffer layer or specific methods for handling, have to be considered. This section summarizes the limitations of employing this type of substrates and correlates them with the state-of-the-art on printed MO_x TFTs.

2.6.1 Flexible and thermosensitive substrates characteristics

Aiming for the future generation of environmental-friendly and disposable electronics for applications like sensors for personal healthcare and smart-packaging, flexible but cheap and transparent substrates have to be utilized. The targeted materials (like paper, polyetherimide (PEI), polyethylene terephthalate (PET), and PEN) are characterized by inferior thermal stability: nominally high thermal expansion coefficient (CTE) and low glass transition temperature (T_g). High CTE can create a mismatch with materials with lower CTEs, like metal-oxides, resulting in thermo-mechanical stress, leading to substrate warping and possible crack formation in the layers. Once surpassed the T_g, the substrate material experience softening. Polymers applied to printed electronics have been engineered to overcome this limitation: for example, heat-stabilized PET can sustain higher process temperature for a longer time than bare PET (78 °C versus 110 °C in T_g). Despite the advancement in the substrate domain, their processing window remains very narrow (typically < 200 °C) compared to rigid substrates (T_{max} for glass > 550 °C) or the specific and expensive thermal resistant polyimide (up to ~400 °C). Moreover, they can suffer from poor chemical resistance and changes in surface morphology if not employed within their operating temperature range, posing additional challenges for printed electronics, particularly for the solution processing of performing solution MO_x TFTs. Table 2.8 summarizes the characteristics of some substrate materials which are relevant for printed electronics.

Table 2.8 Summary of the most relevant parameters for the substrates more commonly used in printed electronics. In the table are included materials that are of interest but not targeted during this work, such as paper, and helpful reference materials, such as flexible glass and Si.

Substrate	**T_g [°C]**	**T_{max} [°C]**	**CTE [ppm/°C]**	**Roughness**	**Transparency**
Paper	NA	200	Large	Poor	Opaque
PET (Melinex)	110	150	~10	Ok	Good
PEN (Teonex)	155	180	~10 – 30	Ok	Good
PEI (Ultem)	217	220	~50	Ok	Light amber
PES (Solvay)	220	/	~50	Ok	Good
PI (Kapton)	354	<400	10-45	Ok	Amber orange
PI (Upilex)	354	>400	10-20	Good	Amber orange
Flexible glass	>600	~700	3	Good	Good
Si	~700	>1000	2.5	Good	Opaque

These materials are generally:

- less chemically stable: moisture/solvent adsorption, limited compatibility with solvents;
- less thermally stable: expansion coefficient mismatch, limited process temperatures;
- dimensionally unstable: high CTE, misalignments in multilayer printing;
- may present poor surface morphology: high roughness, low initial flatness.

Implementing methodologies initially designed for rigid substrates, like glass and silicon, on flexible substrates poses technical challenges. Aspects like foil mechanical stability and the need for methods that ensure the substrate flatness during the different processing steps have to be considered.

Due to their flexible nature:

- flexural stress needs to be considered (high risk of device damaging);
- specific handling is required (rigid carrier substrates, minimum mechanical stability mandatory).

2.6.2 Printing MO_x TFTs on flexible and thermosensitive substrates

As a consequence of these limitations, the literature regarding printed MO_x TFT on flexible substrates, as reported in Table 2.9, is modest and often limited to high-performance polymers such as polyimide (PI), used notably for addressing transistors in the display and IoT (i.e., RFID by PragmatIC) industries, which exhibit relatively high chemical and thermal resistance (up to 450 °C).

Table 2.9 State-of-the-art summary on printed MO_x TFT on flexible substrates. (NP = nanoparticles)

SC	Printed G	Printed SC	Printed DIE	Printed S/D	Max $T_{annealing}$ [°C]	Substrate	μ [cm^2/Vs]	Ref.
ZTO	FTO	ZTO	ZrO_x	FTO	300	PI	0.04	[6]
ZnO	/	ZnO	Organic	/	250	PI	1.6	[83]
InO_x	/	InO_x	AlO_x	/	180	PI	2.8	[59]
InO_x	/	InO_x	/	/	150	PEN	1	[34]
ZnO	Ag	ZnO NP	Organic	Carbon	150	Cellulose	0.07	[158]
IGZO	/	IGZO	/	/	120	PEN	4.2	[133]
InO_x	/	InO_x NP	Organic	/	60	PEN	8	[38]
InO_x	/	InO_x NP	Organic	/	25	PEN	<1	[37]

The few examples reported in the literature regarding using thermosensitive substrates, such as PEN or even cellulose, employ layers not printed or not metal-oxide-based, such as an organic dielectric. These cost-effective and possibly transparent films are currently tricky to involve in the manufacturing process due to incompatibility with standard MO_x thermal synthesis and the lack of chemical and mechanical stability of such foils. The PI instead can be conveniently spin-coated to form homogeneous thin films on carrier substrates that can be detached at the end of the manufacturing process, circumventing the technical difficulties related to the solution processing on stand-alone foils.[159] Nonetheless, PI is a relatively expensive and opaque (yellow) material, thus not ideally suited for transparent and cheap applications, like disposable smart labels.

As an alternative route to avoid the thermal limitations, the manufacturing could take place on heat-tolerant carriers and then successively transfer the devices onto the final thermosensitive substrates.[160] However, such approaches would diminish the potential of the printing methods as a cost-effective solution. Using digital additive manufacturing techniques to directly print active electronic components and systems on a cost-effective large-area substrate or the final applicative foil, such as PET or cellulose-based packaging materials, without the need for rigid carriers or complex photolithographic processes, would broaden the diffusion of printed MO_x based electronics in daily life and consumer applications.

2.7 State-of-the-art summary on low-temperature processed and printed MO_x TFT: status and challenges

In this section, we provide a complete overview of the available literature regarding the low-temperature processing of MO_x TFTs, implementing both non-printed and printed functional metal-oxide layers. From this summary, we have pointed out the remaining open challenges and the aspects that can deserve more investigations, identifying the technological and scientific gap to be fulfilled to reach to achieve fully printed MO_x TFTs onto thermosensitive substrates. We will ultimately illustrate the approaches investigated during this thesis as contributions towards filling this gap.

2.7.1 Status on low-temperature processed and printed MO_x TFTs

As described in the previous paragraphs, many different approaches have been explored aiming at manufacturing low-temperature solution-processed MO_x TFTs. Several combinations of semiconducting metal oxides have been investigated, with those based on indium representing the large majority of the work performed because of the high mobility achievable and the relatively low process temperatures for this material. However, InO_x can suffer from operational instability and poor current modulation capability, therefore not ideal for performing MO_x TFTs. Diminishing the temperature required for the synthesis of metal oxides is still a focal point of the research community. Different chemistries, including the implementation of specific precursors and the integration of fuels in the mixture, have been examined. Generally, chemical optimization is combined with curing techniques that allow minimizing the temperature required during processing. Among them, methods like DUV, based on electromagnetic sources, are usually preferred because of their process flexibility and their possible combination with thermal treatments. As a result of efforts dedicated by the community, annealing temperatures like 200 °C or less are nowadays not exceptional for solution-processed MO_x electronic films. Solution-processed IGZO at such low temperatures often requires prolonged treatments to be adequately synthesized. Valuable alternatives such as IZO, more stable than InO_x and potentially requiring shorter treatment durations than IGZO, have not been investigated sufficiently. Table 2.10, reports the relevant literature about solution-processed IZO-based TFTs with process temperature ≤ 200 °C.

Table 2.10 Literature regarding solution-processed IZO treated at a temperature ≤ 200 °C.

Ref.	Dielectric material	Energy source	T_{max} process (°C)	Total curing time (min)	Mobility (cm^2/Vs)
[161]	ALD Al_2O_3	Thermal	200	120	4.1
[126]	Thermal SiO_2	DUV	200	30	1.3
[116]	Thermal SiO_2	UV	150	15	33.1
[162]	Spin coated SiO_2	DUV+Thermal	150	150	16.2
[118]	ALD Al_2O_3	DUV	N/A	120	4.4

Nonetheless, looking at the publications on solution-processed/printed MO_x TFTs summarized in Table 2.11, it can be noted that fully printed MO_x TFTs on a flexible substrate have been only demonstrated so far on thermo-resistant PI foil. Except *Zeumault et al.*[6], who reported fully printed ZTO based TFTs cured at 300 °C on PI, but with poor performances (mobility ~0.04 cm^2/Vs), no other record is available. The increasing number of publications, and the consequent advancements in the field, have resulted in progress towards this objective. The fact that the main publications are reporting fully printed MO_x TFTs on rigid substrates tells us that achieving this goal of printing them on foil, temperature-sensitive or not, can be considered a very challenging task. We will now describe some of the relevant achievements on this topic.

Scheideler et al. have shown mobility of ~11 cm^2/Vs with fully printed MO_x TFTs on highly doped Si used as gate/substrate. All components: InO_x as semiconductor, AlO_x as dielectric, ACO as source/drain electrodes were printed, except for the gate, with a processing temperature of 250 °C remaining above the limit for thermosensitive substrates.[78]

Leppäniemi et al. demonstrated printed InO_x TFTs on PEN, photocured with a deuterium lamp applying an "in-situ" process, combining light exposure and heat, limiting the processing temperature to 150 °C, but required 180 min of treatment to reach mobility of ~1 cm^2/Vs.[34]

Carlos et al. recently reported on TFTs implementing a printed InO_x/AlO_x semiconductor/dielectric stack processed at 180 °C, which yielded a mobility ~2.9 cm^2/Vs. The latter was manufactured on a flexible PI and required a DUV exposure of up to 90 min, but the method could be potentially replicated on more appealing substrates.[59]

Addressing temperature sensitive foils, *Yarali et al.* yielded on transparent PEN foils TFTs with mobility of ~ 2.3 cm^2/Vs.[108] They employed a multilayer spin-coated InO_x/ZnO as semiconductor and spin-coated ZrO_2/AlO_x dielectric, cured via pulsed light annealing. They demonstrated that both MO_x active layers could be synthesized on substrates like PEN, but their methodology requires the passage from spin-coating to the printing process.

Table 2.11 State-of-the-art on low temperature processed & printed MO_x TFTs. Here, we provide an overview of the actual state of the art of solution-processed/printed MO_x TFTs at low temperature, reporting relevant examples per each of the most common MO_x semiconductor materials. We included as references publications reporting TFTs on rigid substrates.

		IGZO			**IZO**			**InO_x**				**Others** [16]	
	Sputtered IGZO	***Rigid Substrate***	***Low T_g Foil***	***Fully printed***	***Rigid Substrate***	***Low T_g Foil***	***Fully printed***	***Rigid Substrate***	***Low T_g Foil***	***Almost Fully Printed***		***Low T_g Foil***	***Fully printed on foil***
Substrate	Foil and Si	Si	PAR	Glass	Si	PEN	/	Si	PEN	Si	PI	PEN	PI
T process [°C]	Up to 150	300	150	350	150	200	/	250	150	250	180	60	300
Printed S/D	No	No	No	Yes	No	No	/	No	No	Yes	No	No	Yes
Printed MO_x Dielectric	No	No	No	Yes	No	No	/	No	No	Yes	Yes	No	Yes
Printed MO_x Semiconductor	No	Yes	No	Yes	No	No	/	No	Yes	Yes	Yes	No (In_2O_3/ZnO_2)	Yes (ZTO)
Printed Gate	No	No	No	Yes	No	No	/	No	No	No	No	No	Yes
DUV Approach	No	No	Yes	No	Yes	No	/	No	Yes	Yes	Yes	No	No
I_{on}/I_{off} ratio	10^5 - 10^9	$1.3*10^7$	10^8	~10^6	10^6	$4.1*10^8$	/	10^5	10^7	10^6	10^6 - 10^7	10^5	~10^3
Mobility [cm^2/Vs]	Avg: 10-25 Max: 76	20	3.77	81	>30	4.1	/	36.3	~1	~11	>1 Max: 2.8	2.3	0.04
Reference	[20,163,164]	[40]	[118]	[41]	[116]	[88]	/	[45]	[34]	[78]	[59]	[108]	[6]

[16] Few other examples of fully printed MO_x TFT, using alternative semiconductor combinations, such as InGaO, have also been reported. However, these TFTs are all onto rigid substrates and processed at high T (450 °C or more), therefore not relevant for our state of the art.

By looking at the literature (summarized in Table 2.11) emerges that some fundamental aspects of the topic have not been addressed thoroughly, and more investigations are required to fill the technological and scientific gap still present.

- InO_x is the primary MO_x semiconductor investigated for low-temperature applications, but it suffers from operational instability and therefore is not suited for implementation at an industrial scale.
- The solution-processed MO_x semiconductors are often combined with insulators different from the preferable MO_x dielectrics or are deposited with vacuum-based processes. These types of dielectrics ultimately will need to be replaced with solution-processed ones, thus requiring additional studies to investigate important aspects of the devices, like the dielectric-semiconductor material compatibility and the quality of the interface.
- Many publications deal with glass or Si substrates for practical reasons, while the aspects of processing onto thermosensitive foils are often overlooked. In this frame, curing protocols often involve prolonged exposures suitable for rigid and stable materials like glass but may not be compatible with polymeric foils. Optimization of the annealing process may be necessary to establish a manufacturing process compatible with more sensitive substrates.
- The preferred deposition method for MO_x thin films remains spin-coating. However, a process developed using spin-coating may not be transferable to printing, necessitating changes in chemistry and process optimizations to get notably uniform films, which would be even more challenging if stacking printed layers together.

A manufacturing process based on printing methods, combined with a synthesis methodology compatible with the thermosensitive substrates, capable of yielding performing TFTs has not been proven yet.

2.7.2 Challenges and research approaches addressed in this thesis

We have addressed the challenges related to semiconductor chemistry, the low-temperature synthesis via DUV-enhanced methods, the development of a manufacturing protocol based on inkjet printing, and the implementation of the process onto the targeted substrates with the ultimate goal of achieving printed MO_x TFTs onto thermosensitive substrates.

Envisioning the complete printing of our MO_x stack, we carried our studies integrating both solution-processed/printed performing MO_x dielectric and semiconductor, investigating the interaction between the two layers and evaluating their behavior while optimizing the performances of the devices.

We identified IZO as a semiconductor: compared to InO_x, it can provide better electrical performances, notably higher operational stability and V_{th} ~0 V, yet yielding satisfactory mobility. We have also implemented a high-k AlO_x/$YAlO_x$ dielectric which ensures good electrical performances (i.e., low leakage) and provides an optimal match with the IZO semiconductor (i.e., good semiconductor/dielectric interface).

We investigated different combinations of chemical solvents and additives to obtain chemistry favorable for a low-temperature approach. We ultimately selected nitrate as precursors and 2-methoxyethanol as a solvent because, in comparison to the other combinations, it required the lowest amount of energy to convert the ink into functional MO_x film. We explored the MO_x synthesis via DUV processes because it demonstrated its effectivity on the selected MO_x inks based on nitrate precursors. The method is highly flexible thanks to the considerable number of possible process variables (wavelength, power, gas atmosphere, heat supply). Moreover, contrarily to others like the pulsed light annealing, the UV emission range fits the optical absorption spectral range of the MO_x sol-gel does not require specific arrangements such as non-transparent light-absorbent elements.

Intending to target substrates different from Si wafers, we implemented parametric studies to optimize the curing process and minimize the thermal budget. We investigated two types of DUV sources and ultimately reduced the time required to sinter the IZO to only 10 min at 200 °C. A further reduction of the process temperature was achieved exploiting a more powerful DUV source, resulting in TFTs processed at a maximum temperature of 160°C were ultimately demonstrated.

We upgraded our process from the initial spin-coating to a printing process by modifying the ink composition and evaluating the effectiveness of the DUV annealing on the new ink. We developed a manufacturing protocol compatible with thermosensitive and transparent substrates, like PEI. In doing so, we integrated a buffering layer capable of preventing substrate damages and ensuring the processability of the metal-oxide functional films on this type of flexible foil, which was further demonstrated by manufacturing printed AlO_x/$YAlO_x$ capacitors on PEI.

Each of these aspects will be addressed in the following chapters.

2.7.2.1 TFT requirements

According to the objectives and the challenges of the thesis, we present here the main requirements for the MO_x TFTs, which will be helpful to evaluate the performances of the devices presented throughout the chapters.

Table 2.12 Summary of the requirements for the MO_x TFTs investigated in this thesis.

	Minimum	**Optimal**
Substrate	Rigid	Foil (low T_g)
$T_{process}$ (°C)	≤ 200	< 180
Printed Source/Drain	No	Yes
Printed MO_x Dielectric	No	Yes
Printed MO_x Semiconductor	No	Yes
Printed Gate	No	Yes
DUV Approach	Yes	Yes
I_{on}/I_{off} ratio	> 10^4	> 10^6
Mobility (cm^2/Vs)	> 1	> 4

2.8 Conclusions

In this chapter, as a promising basic building block for future electronic systems, we introduced the MO_x-based thin-film transistors: their fundamentals, design, realization, and characterization, highlighting their important figures of merit. These devices are often manufactured via costly cleanroom-based processes, which demands infrastructures and resources. The pool of possible applications further enlarges if these devices could be realized using sustainable processing techniques applicable in mass-scale production, such as additive manufacturing methods, i.e., printing.

We described the different deposition methodologies, focusing on those printing methods that could be exploited to realize the thin and uniform MO_x functional films required to achieve performing TFTs. However, to be impactful and attractive for emerging applications, like smart packaging and wearable sensors for personalized healthcare, it would be interesting to manufacture these TFTs on environmental-friendly and cost-effective flexible substrates. However, these materials suffer from mechanical and thermal limitations that have prevented their use with solution-processed MO_x-based devices since they require a relatively high processing temperature for the sol-gel formation.

We described the different approaches that can be exploited to synthesize at lower temperatures MO_x electronic films to overcome the thermal constraints of the substrates. In this frame, particular attention was given to the methods based on electromagnetic sources like DUV that, thanks to their process versatility, can be effective with quick processes or in a range of temperatures potentially compatible with the thermosensitive substrates addressed.

We then focused on the semiconductor behavior when combined with solution-processed MO_x dielectric and how the devices can be characterized to evaluate the dielectric quality. We reviewed the limitations and the challenges related to the implementation of thermosensitive flexible substrates. Ultimately we provided a complete overview of the state-of-the-art regarding low-temperature solution-processed MO_x: by analyzing the literature and the previous approaches to the problems, we exposed the technological and scientific gaps remaining. Finally, we briefly introduced the challenges addressed and the methodology applied in this thesis in relation to the following coming chapters.

Chapter 3 Concept and design of solution-processed MO_X semiconductor

This chapter aims to describe the concept and design of MO_x semiconductor thin films based on sol-gel processes.

First, we provide an overview of the carrier transport mechanism involved in a MO_x thin-film semiconductor and compare it with the one occurring in amorphous silicon films. We then introduce and compare amorphous MO_x with their crystalline counterparts, showing how their crystallinity is related to the nature of the cations composing the film and to the film stoichiometry. In this frame, we provide some insights on the chemical composition necessary to obtain films with the desired electrical performances and briefly discuss the influence of different cations on electronic transport. We describe the two main classes of multi-component metal oxides employed in semiconductor layers: zinc oxide-based and indium oxide-based. We show the characteristics and the state-of-art of the most relevant compositions, such as ZTO, IGZO, and IZO. Among them, in the perspective of lowering the synthesis temperature, IZO was selected because of its interesting electronic performances and its relatively convenient chemistry.

Then, we discuss in detail the chemical design of the semiconductor. We start from the solvent selection by comparing the widely diffused 2-methoxyethanol and a less toxic alternative, 1-methoxy-2-propanol. The solutions made of the two different solvents were characterized via thermal gravimetric analysis (TGA) to identify the temperature range required to trigger the chemical reactions. Afterward, we studied how different stoichiometry could influence the electrical characteristics and the morphology of the synthesized films. By analyzing the crystalline nature of the deposited layers via Grazing Incidence X-ray diffraction (GIXRD), we could identify those cationic ratios ensuring that the IZO layers were in an amorphous state. By combining this microstructural characterization with the electrical characteristics of TFTs made of these films, the cationic In:Zn ratio was determined to be 7:3.

Finally, we explored the possibility of further improving the electrical characteristics of our TFTs by doping the IZO semiconductor with aluminum. Al has been of interest as a possible alternative to Ga as it is cheaper and widely available in nature. Al doping can lead to films with a stable amorphous phase and, since it is a strong oxygen binder, it can act as a carrier suppressor that ultimately reduces the off-currents and stabilizes the TFT operation. The better control of oxygen defects in the film could also lead to improved carrier mobility. We investigated the effects that introducing small concentrations of Al in the IZO metal-oxide layer has on the electrical performances of IZO TFTs. We confirmed the role of carrier suppressor of the Al ions, which in small percentages (< 3%) slightly improved the switching capabilities of the devices, but we did not observe a significant influence on the carrier mobility. Ultimately, we decided to maintain the stoichiometry initially identified and not implement any Al doping in the IZO.

3.1 Material design towards performing amorphous oxide semiconductor channel

In this section, we describe in detail the charge transport occurring in a thin film metal-oxide semiconductor. First, we will describe the transport mechanism and explain why the amorphous MO_x semiconductors have superior electrical characteristics to their crystalline counterparts. Then, we provide the requirements with respect to the chemical composition necessary to obtain functional films and briefly discuss the influence of different cations on their electronic transport. In this frame, we will examine some of the classes of binary and multi-component oxides used as semiconductors like ZnO-based and InO_x-based oxides, components of the mainly used IGZO. Their advantages and limitations in the context of low-temperature solution processing will also be discussed.

3.1.1 Amorphous metal oxide semiconductors

We mentioned that in the previous chapter that in Si-based semiconductors, the conduction occurs mainly via the covalent bonds in the sp^3 hybridized orbitals. These strongly oriented bonds are sensitive to lattice distortions that may create dangling bonds. Consequently, the charge transport is also affected by the crystalline order: in single-crystal silicon, the conduction path is undisturbed, resulting in extremely high electron mobility (1000 cm^2/Vs), in polycrystalline-silicon the lattice still presents a long-range order, but the grain boundaries in the material are a source of scattering which cause a partial decrease in mobility (~100 cm^2/Vs), whereas the randomly oriented bonds of the amorphous-Si strongly limit the charges conduction (~1 cm^2/Vs).

The electronic conduction in metal-oxide semiconductors, with mainly n-type materials being used in TFTs, is instead almost independent of crystalline order and lattice distortion. The conduction occurs via the spherical s-orbitals of the heavy post-transition metal cations, particularly for those elements with electronic structure $(n-1)d^{10}ns^0$ where $n \geq 4$, like in Sn^{4+}, Zn^{2+}, Cd^{2+}, In^{3+}.[165] As depicted in Figure 3.1, when these isotropic orbitals can overlap, the conductive path is created regardless of the spatial orientation. When $n \geq 5$: the size of the s orbitals allows a sufficient overlap that enables a strong electron delocalization.[166] In parallel, defects in the M–O–M network like substitutional/interstitial hydrogen, cation interstitials, and oxygen vacancies[17] can also contribute to total charges available by injecting electrons and increasing the conductivity of the layer.

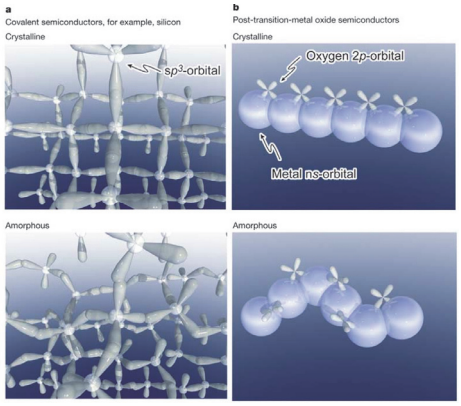


Figure 3.1 Charge transport in covalent semiconductors and post-transition metal-oxide semiconductors.[26]

Performing n-type MO_x semiconductors necessitate elements that can provide an adequate number of charge carriers. These constituents represent the basis for each conductive/semiconductive MO_x and possess the previously mentioned ideal electronic configuration, like In^{3+} and Sn^{4+} ($[Kr](4d)^{10}(5s)^0$, n=5). Additionally, Zn^{+2} that owns a similar electronic structure ($[Ar](3d)^{10}(4s)^0$, n=4), is also exploited as a carrier supplier. Binary oxides obtained from these elements, like In_2O_3, ZnO, and SnO_2, have been considered the base components for MO_x semiconductors. Indium oxide-based and tin oxide-based transistors can yield mobilities up to 100 cm^2/Vs, but undesired high off-currents often limit their application as semiconductors.[5] An excessive number of charges, over ~10^{18} cm^{-3}, causes degenerated conduction, ultimately resulting in transistors with poor switching capabilities and negative threshold voltages not adapted for practical applications. Instead, ZnO-based TFTs can maintain reasonable mobility values (~1 cm^2/Vs) and a higher I_{on}/I_{off} ratio. Moreover, these layers often require passivation films as they are sensitive to the ambient atmosphere, such as humidity,

[17] Oxygen vacancy acting as shallow donor $O_O^x \rightarrow V_O^{\circ\circ} + \frac{1}{2}O_2(g) + 2e^-$.

oxygen, and other gases present in the air, which eventually causes electrical modifications and instabilities. Additionally, most of these binary oxides, especially ZnO, tend to be arranged in polycrystalline/nanocrystalline structures. (Figure 3.2c) Their crystalline nature partially hinders charge mobility; the grain boundaries cause electrical inhomogeneities and limit the electrical uniformity over a large area. These boundaries are also structural defects that can initiate and promote crack formation in the MO_x films, which is a drawback for TFTs manufactured on flexible substrates.

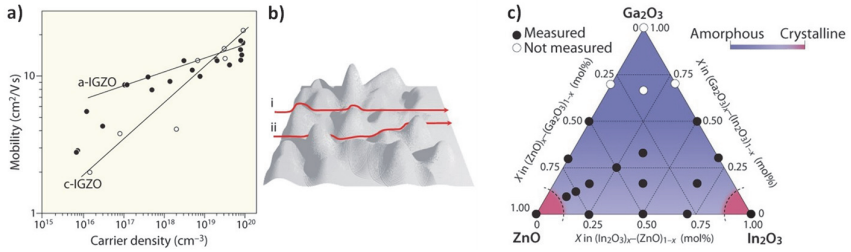


Figure 3.2 Comparison between crystalline and amorphous MO_x. a) Relationship between Hall mobility and carrier density for c-IGZO and a-IGZO. b) Illustration of percolation conduction showing examples of (i) a shorter and (ii) a longer path. c) Relation between film morphology and chemical composition. (Adapted from[167])

To overcome these limitations, multi-component oxides comprising different cations can ensure an amorphous nature. These amorphous oxides can provide superior TFT performance than binary compounds. A stable amorphous phase can be achieved when the film contains two or more metal cations, like indium and zinc, presenting different ionic charges and crystal structures since the different geometries disrupt the crystalline order. Moreover, adding elements with varied electrical characteristics provides much higher flexibility in the electrical design of the films. Compounds operating as carrier suppressors are often added to these operating as mobility enhancers, providing a better modulation of the charge transport in the oxides. Cations such as gallium (Ga) possess a stronger oxygen affinity than In or Zn. Incorporating these elements, also called "oxygen getters", suppresses the formation of oxygen deficiencies, diminishing the background carrier concentration associated with the electron donation from the oxygen vacancies. As a result, the off-currents can be sensibly reduced, thus improving the switching capabilities of the transistor. However, this effect intensifies as the percentages of such elements in the film increments, ultimately lessening the on-currents. Therefore, the proper amount balance between these elements needs to be found.

We will now provide an overview of the standard multi-component metal oxides applied as an active semiconductive layer in TFTs.

3.1.2 ZnO-based multi-component oxides semiconductors

In the early 2000s, zinc oxide-based semiconductors were of interest owing to their transparency and electrical performances similar to those achieved with a-Si. However, as mentioned earlier, ZnO is mostly polycrystalline and possesses a high concentration of traps that partially limit its performance.[5] Amorphous ZnO was also reported but generally is not employed as a semiconductor.[168] Therefore, several alloys have been investigated to ensure films, starting from a ZnO base, with an amorphous phase. Among them, zinc tin oxide (ZTO) is the most relevant; it has an amorphous phase due to the different crystalline nature of the ZnO and SnO_2 oxides (Figure 3.3), respectively wurtzite and rutile structure, and is capable of yielding mobility up to 4.3 cm^2/Vs depending on the ratio of the cations.[169] Quaternary compounds, such as aluminium-doped ZTO or zirconium-doped ZTO, have also been studied with variable outcomes.[42,169]

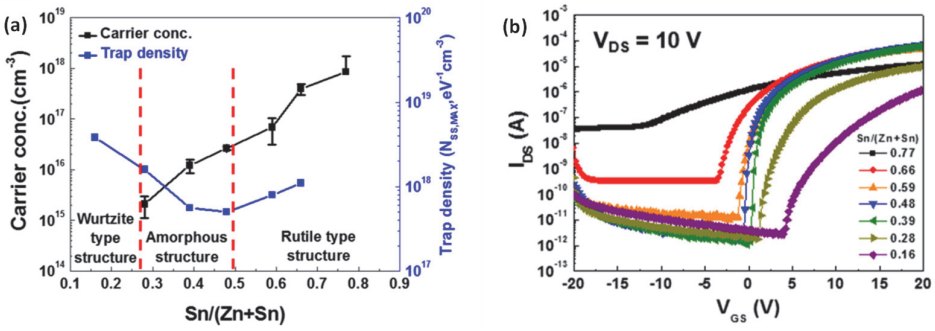


Figure 3.3 Morphological and electrical characteristics of ZTO-based transistors with different Zn:Sn ratios.[169]

Zn-based materials are considered more accessible than In-based ones: indium is relatively scarce and more expensive than Zn, potentially at risk as a future bottleneck in the manufacturing supply. Moreover, Zn and ZnO are environmental-friendly and biocompatible, which is advantageous for possible future applications like disposable electronics or wearable and implanted devices.

Nonetheless, solution-processing at a low temperature of Zn-based oxide materials, such as ZTO, remains a challenge: tin precursors are mainly chloride-based and therefore, as seen in Section 2.4, require elevated temperatures (> 300 °C) to be converted into a MO_x network and to remove the impurities from the films.[6,170] Appealing alternatives for eco-friendly electronics, such as magnesium doped ZnO, have been demonstrated via sol-gel processing but still require investigations since processing temperatures as high as 400 °C are still necessary.[171,172]

3.1.3 InO_x-based multi-component oxides semiconductors

As mentioned, indium is relatively expensive and not biodegradable. However, it is also reported as processable at low temperature via solution-processing with suitable electrical performance. Therefore, it is still considered the most promising base material for applications on thermosensitive foils. As previously described, it presents the best electronic configuration among the post-transition metals, is a weak oxygen binder, thus possessing many free carriers. Solution-processed InO_x semiconductors can be manufactured at low-temperature using nitrate precursors (< 200 °C) and yield amorphous films with high mobility.[132] However, the resulting TFTs suffer from poor operational stability, low I_{on}/I_{off} ratios, and negative threshold voltages.[173,174] Several binding elements have been exploited to improve their electrical characteristics and ensure reliable switching operation.

3.1.3.1 IZO

Zn-doped indium oxide (IZO) is one of the most diffused multi-component oxides. In_2O_3 presents a bixbyite structure, while ZnO has a wurtzite structure. As a result, the IZO films can present an amorphous state over a large range of the cationic ratio between In and Zn (80:20 – 20:80 in %).[91] It is also possible to tune its resistivity by varying its composition[175] or changing the process parameters.[176] By doing so, sputtered IZO can act as transparent electrodes or as the active layer in TFTs, as shown in Figure 3.4. Sputtered films are generally characterized by many carriers and light instability that cause elevated off-currents. For this reason, thanks to transparency and low electrical resistance, typically 10-100 Ω/Sq, IZO is commonly used in the display industry as an alternative to TCOs like ITO. Instead, combining IZO with gallium (Ga) has been favored to reach performing semiconductors, as it neutralizes part of the vacancies and stabilizes the electrical behavior of the resulting TFTs.

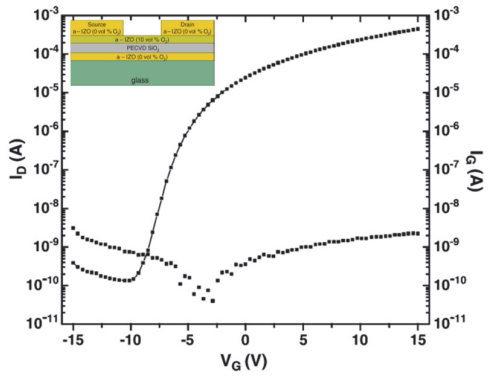


Figure 3.4 Example of sputtered IZO films exploited as conductors and as a semiconductor in the same TFT. (Adapted from [176])

On the other hand, solution-processed IZO films do not necessarily exhibit excessive conductive behaviors because of an inferior metal-oxide quality reached with respect to their vacuum-based counterpart due to the involvement of liquid chemistry and possible residuals in the films. Among the ternary oxides used as semiconductors, the IZO has been widely studied, and many parameters have been investigated for its optimization. This large number of process variables, such as solution composition and formulation, process conditions, and post-annealing treatments, allows a flexible tuning of its semiconductor characteristics, resulting in TFTs exhibiting high mobility (> 30 cm^2/Vs) and a good I_{on}/I_{off} ratio (> 10^6).[116,177]

Banger et al. showed the importance of the film stoichiometry to control both structural and electronic properties of IZO TFTs (Figure 3.5), ultimately reaching performing devices, processed at 230 °C on Si, with field-effect mobility of 10 cm^2/Vs.[91]

Seo et al. instead demonstrated that it was possible to form by sol-gel IZO films on flexible foil, limiting the process temperature to 200 °C and still achieving, after a two hours thermal treatment, a mobility > 4 cm^2/Vs.[88]

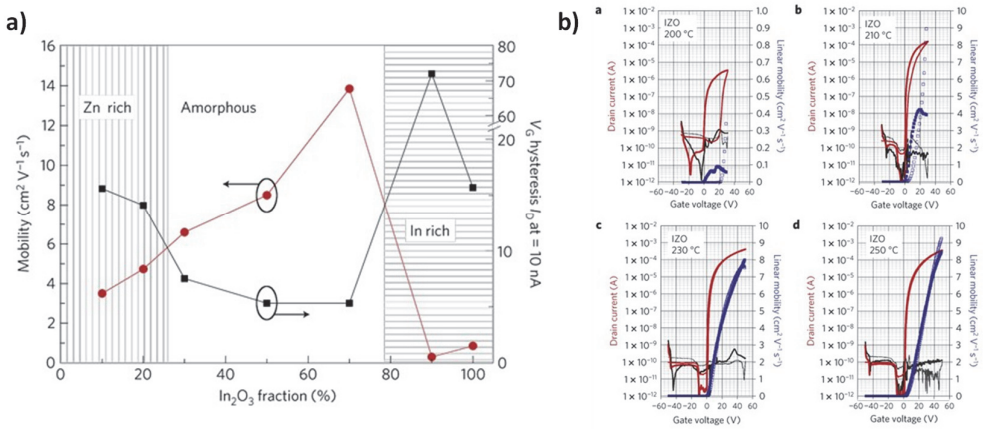


Figure 3.5 Structural and electrical characteristics of IZO TFTs. a) Plot of mobility and hysteresis of IZO TFTs as a function of the stoichiometry. b) Transfer curves obtained from TFTs cured at various temperatures. (Adapted from [91])

The chemical formulation for solution-processed IZO is favorable since only two cations need to be tuned. Moreover, both cations have nitrate precursors, which are suitable when considering low-temperature synthesis approaches like the DUV annealing applied in this work.

3.1.3.2 IGZO

The IGZO is the most diffused amorphous oxide semiconductor for TFTs as the sputtered IGZO is nowadays the cornerstone of the TFTs employed in liquid crystal display (LCD) technology. It was demonstrated for the first time in 2004 by *Nomura et al.* when they deposited it at low temperature on PET via pulsed lased deposition to form transparent and performing TFTs with mobility over 5 cm^2/Vs.[26] Until that moment, other metal oxides such as crystalline ZnO or ITO were scarcely utilized as semiconductors because their electrical characteristics were difficult to control and not suited for reliable switching applications. However, by adding elements like gallium, which forms a stronger Ga–O bond than In–O and Zn–O, it is possible to decrease the background carriers related to the vacancies, reducing the off-current and shifting the threshold voltages towards neutral values. As depicted in Figure 3.6, the electrical characteristics of the devices are strongly related to the ratios between the different chemical elements: unbalanced mobility enhancers (In, Zn) leads to uncontrolled switching. At the same time, excessive gallium can depress the on-current and mobility. *Fortunato et al.* compared several ratios and concluded that a 4:2:2 (In: Ga: Zn) ratio would be optimal, granting an I_{on}/I_{off} ratio over 10^7 and a suitable on-current level.[5] They also pointed out that the electrical performances are related to many deposition parameters, such as the target composition and the oxygen pressure, the thickness of the layer deposited, or the thermal post-treatment performed.

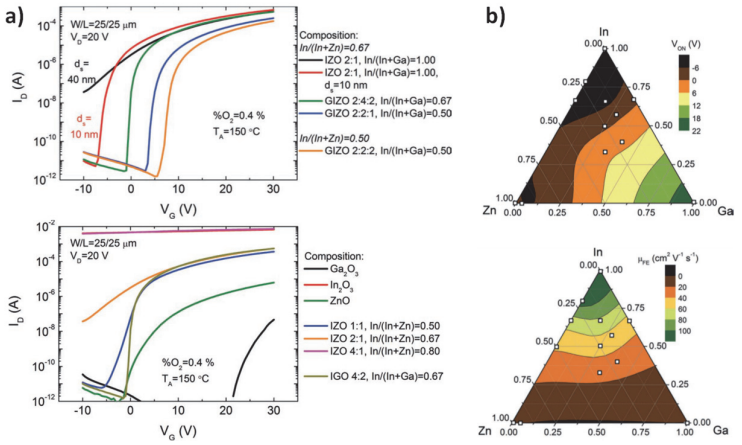


Figure 3.6 Effect of cation tuning on sputtered IGZO TFTs. a) IGZO transfer characteristics for different cation stoichiometry. b) Effect of cation stoichiometry on mobility and threshold voltage. (Adapted from [5])

During a sputtering deposition, the elemental composition of the film can be precisely tuned, resulting in a reliable and repeatable process. Solution-processing presents instead challenges related to the chemistry, especially regarding the balance between the different cations. Moreover, when considering low-temperature annealing, multiple components in the solution can influence the amount of heat necessary to decompose the precursors. For example, *Banger et al.* could achieve functional solution-processed TFTs with IZO semiconductors processed at temperatures as low as 230 °C. However, when they added gallium, their IGZO film required a higher synthesis temperature of 275 °C.[91] The MO_x synthesis at low temperatures can be facilitated by photonic sources, such as DUV, but may necessitate prolonged exposures to be effective (up to 120 min).[118] Simplified chemistry is desirable to reduce both the temperature and processing time required to synthesize these oxide semiconductors.

3.1.3.3 Other In-based alloys

Several combinations of materials have been explored in the past years to find alternatives to quaternary IGZO and ternary IZO. Novel combinations have been proposed to ease the chemistry of the channel, lowering the annealing temperatures or improving the electrical performances (higher mobility, better stability, and switching capabilities). The majority of them have been grouped and analyzed in review papers such as the one from *Parthiban et al.*[178]. Since the number of possible alloying permutations is remarkable, for the sake of time, we will only report few relevant examples.

Kumomi et al. investigated a large set of sputtered indium-based ternary oxides doping the layers with elements such as Mg, Al, Si, Ge, Ti, and others. They selected the dopants according to their electronic affinities and ionic radii. In Figure 3.7 are reported the transfer characteristics extracted from the various TFTs. They concluded that among the tested combinations, both indium germanium oxide (InGeO) and IZO were showing satisfactory performances, comparable with IGZO.[179]

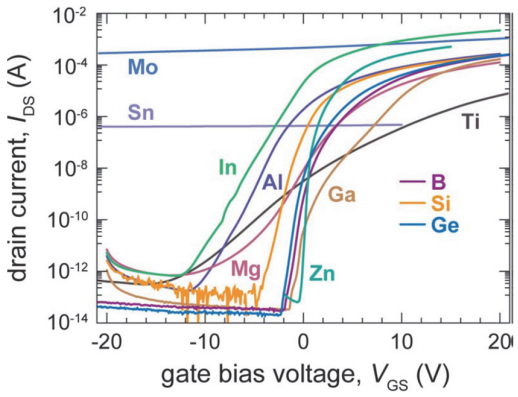


Figure 3.7 Transfer characteristics obtained from various sputtered In-X-O TFTs.[176]

Kim et al. instead demonstrated that, by adding the proper amount of gallium to indium, it was possible to induce the crystalline phase in the film while controlling the trapping site density and the number of vacancies. Their TFTs on Si, employing solution-processed gallium-doped indium oxide (InGaO) cured at 400 °C, could reach linear mobility as high as 52.6 cm^2/Vs while maintaining I_{on}/I_{off} ratios > 10^8.[174]

3.1.4 The selected sol-gel based IZO semiconductor for low-temperature processing

We have identified IZO as a promising semiconductor candidate for sol-gel processing at a low temperature of metal-oxide TFTs reported in this work. This material composition was preferred over others, like IGZO and InO_x, because it presents a good compromise between performance (amorphous phase, high mobility, high I_{on}/I_{off} ratio, operational stability) and the possibility to be processed at low temperature via sol-gel chemistry, thanks to its simple chemistry involving only two cations. The details regarding the formulation of the ink are described in the following section.

3.2 Ink design for the IZO solution

Here, we present the IZO system utilized in this thesis. We characterized the sol-gel process via thermal gravimetric analysis (TGA) to identify the temperature range necessary to trigger the reactions involved in the MO_x synthesis. We describe the study carried out on different IZO solutions and the effects caused by different compositions on the electrical characteristics of the deposited films. We tested two solvents to identify the most suitable one for a low-temperature processing approach. Then we also varied the ratio between the cations, evaluating its effect on the electrical performances of the TFTs, and we analyzed the crystalline nature of the

films via Grazing Incidence X-ray diffraction (GIXRD). This process led us to select 2ME as a solvent and determine the optimum cationic ratio between In and Zn precursors that ensured an amorphous structure and provided desirable electrical behavior, In:Zn = 7:3.

3.2.1 Characterization of the sol-gel reaction by TGA

A TGA measures the mass variation as a function of the temperature applied to the sample. The events during the sol-gel processes, such as solvent evaporation and the expected chemical reactions, can be determined and correlated to the mass loss, ultimately identifying the minimum temperature required to trigger each chemical reaction step. Thereby we can determine the range of temperatures required from the reactions involved in the MO_x synthesis via sol-gel, ultimately revealing the temperature range for the formation of the oxide films via a thermo-chemical process. In this work, we exploited it to preliminary compare different ink formulations.

The precursors utilized were commercial zinc nitrate hexahydrate ($Zn(NO_3)_2{\cdot}6H_2O$) and indium nitrate hydrate ($In(NO_3)_3{\cdot}xH_2O$). The solvent selected for the inks was the 2-methoxyethanol (2ME), a typical solvent used in MO_x sol-gel processing, especially in combination with nitrate precursors for low-temperature processing. It has a relatively low boiling temperature (T_B = 124 °C) and ensures optimal solvation of the precursors resulting in a homogenous solution stable over time. As a comparison, we also tested a solvent that has a similar chemical formulation but less toxicity than 2ME: 1-methoxy-2-propanol (1M2P). As discussed in Section 2.4.1, we did not consider water as a solvent for our sol-gel process. All the solvents and the precursors were purchased from *Sigma-Aldrich*. For the investigation, we kept a constant ratio between In and Zn precursors, 7:3.

The TGA samples were prepared as follows. We dissolved the proper amount of precursors in a vial containing 2 ml of solvent. The inks were stirred for 12 h at 60 °C to obtain homogeneous solutions. Finally, a drying process, 8 h at 100 °C, was performed to evaporate most of the solvents and obtain a dried paste. The paste was transferred into the crucible of the TGA where, after weighing the sample, the temperature was raised from 30 °C to 400 °C with a speed of 10 °C/min. The system used was a TGA 4000 from *Perkin Elmer*.

In Figure 3.8a is reported the TGA curve obtained from a 0.2 M IZO solution in 2ME where we can identify four areas and three mass drops, signs of possible events:

1. From 50 °C to ~150 °C that could represent a solvent and moisture evaporation;
2. From 150 °C to ~300 °C represents the solvolysis reaction with partial removal of the organic species;
3. From 300 °C to ~350 °C condensation reaction occurs, with M–O–M networking and final evaporation of the remaining precursor impurities/solvent trapped;
4. ≥ ~350°C a plateau is reached because all the reactions have already occurred. A further heat supply will lead to lattice rearrangement and crystallization.

Figure 3.8b shows a comparison between two IZO solutions with different solvents, 2ME and 1M2P. What can be extrapolated from these curves is that the temperature required to complete the MO_x networking is a function of the used solvent. It can be seen that, in the case of 1M2P, the mass continues to diminish until T = 400 °C, an indication that impurities were still present and, therefore, that the MO_x networking is incomplete. In parity of conditions, the 1M2P-based IZO solution necessitates higher temperatures to complete the conversion/impurity removal than the 2ME-based one, ~50 °C more.

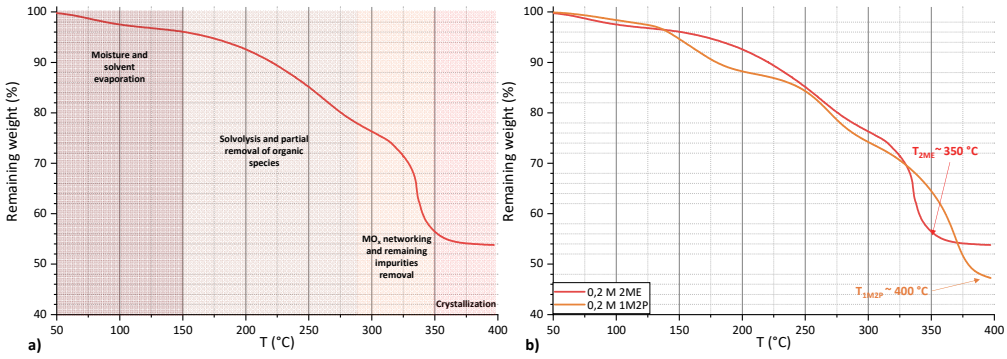


Figure 3.8 Thermogravimetric analysis of nitrate-based IZO solutions. a) Depicts the typical curve obtained from a 2ME-based solution where we can identify the different moments of the sol-gel reaction. b) Shows the comparison between two IZO solutions employing different solvents.

As mentioned, the TGA predicts the range of temperatures required for the MO_x synthesis. The conditions in real applications are dissimilar from the test conditions applied during the TGA: the surface area in a thin film is different from the one in a paste, and different results could be achieved utilizing faster or slower temperature increasing rates. Nevertheless, this method is very beneficial for the initial screening of the solution components to define its composition in terms of solvents and precursors. We finally excluded the 1M2P as a solvent candidate in the perspective of low-temperature processing and identified the 2ME as the most promising one.

3.2.2 Variation of In:Zn ratio in the IZO semiconductor

The electrical characteristics of the produced transistors are dependent on channel chemistry. As discussed above, proper cation tuning is necessary to achieve TFTs with the desired high mobility and switching capability. Moreover, we know from the literature that the morphology of the deposited films depends on the cationic ratio. Therefore, we fabricated TFTs where the active IZO channel presented diverse chemical compositions. We studied how different cation ratios can influence both electrical and morphological characteristics. We identified a ratio window where the cation combination yields IZO metal oxide films with an amorphous phase, choosing the composition that leads to TFTs with satisfactory performances.

We will first describe the fabrication of these transistors with the relative process flow and then discuss the results obtained from the various characterizations.

3.2.2.1 Substrate and dielectric layer

For the study regarding the semiconductor composition, as substrate, we employed highly conductive silicon (resistivity < 0.005 Ω·cm), which also acted as the gate electrode. After a standard RCA cleaning, the wafers have been thermally oxidized using the *Centroterm* furnace at EPFL-CMi to form a high quality 200 nm thick dry SiO_2 oxide layer employed as the gate dielectric. The wafers were afterward diced in chips of 1.8 cm x 1.8 cm.

3.2.2.2 Semiconductor deposition and MO_x synthesis

The semiconductor layer was deposited via spin-coating and thermally annealed. The precursor solution for the synthesis of IZO was prepared by dissolving zinc and indium nitrate hydrate precursors in 2ME. The concentration of these precursors for spin coating was chosen as 0.2 M, typically reported in the literature[126], and different In:Zn ratios were tested, from pure InO_x to pure ZnO with the following variation in the ratio: 9:1, 7:3, 5:5, 3:7, 1:9.

The solutions were stirred at 60 °C for more than 12 h and filtered with 0.2 µm (PTFE) filters before use. Before deposition, the Si/SiO_2 chips were subjected to O_2 plasma treatment (Low-pressure Plasma Cleaner Atto from *Denier*, power of 0–300 W at 13.56 MHz) for 5 min at 100 % power that improved the solution wettability. Then, the film formation occurred via spin-coating (WS-650Mz-23NPPB from *Laurell Technologies*): 0,6 ml of solution was poured on the substrate, and then a rotation at 2000 rpm for 30 seconds was applied. The coated substrate was then immediately transferred on a heated hot plate for a drying step at 150 °C for 1 hour in air ambient. Then, the final annealing was carried at 350 °C for 30 min to trigger the MO_x networking.

3.2.2.3 Electrodes deposition and final devices architecture

The aluminum electrodes, ~100 nm thick, were deposited by e-beam evaporation through a magnetic shadow-mask, which adhered well to the substrate and minimized the shadow effect. As depicted in Figure 3.9b, the electrodes patterned had constant width (W) and comprehended four different channel lengths (L), providing the following W/L ratio: 7.5, 10, 15, and 30, repeated four times to have some statistics.

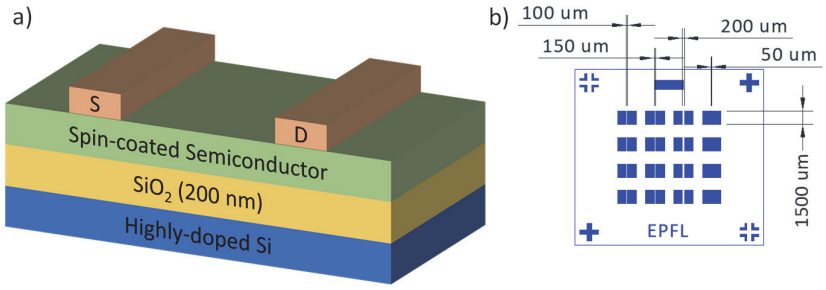


Figure 3.9 TFT cross-section and electrodes dimensions. a) shows the TFT cross-section while b) depicts the four different W/L present on the mask. Each device for a given W/L is repeated four times to ensure statistical results.

3.2.3 Electrical characterization

We extracted the relevant figures of merit from the manufactured TFTs to evaluate the electrical performances as a function of the different IZO stoichiometry evaluated. The representative electrical values extracted are summarized in Table 3.1. In Figure 3.10 are reported the typical transfer curves obtained from devices presenting the same geometry but varying cation ratios.

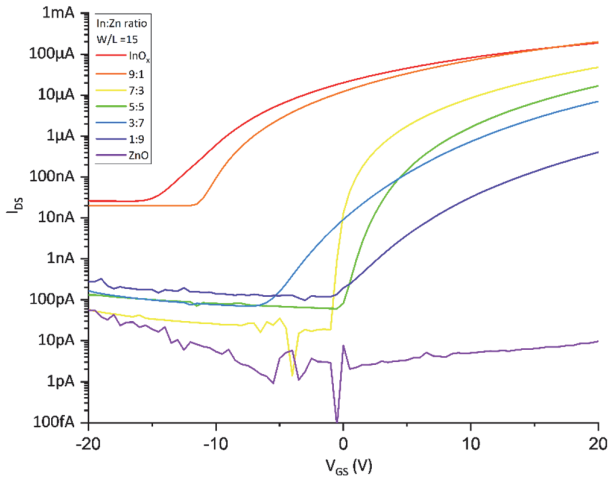


Figure 3.10 Comparison between typical transfer curves obtained from TFTs with a variable indium-zinc ratio in the active channel.

From Figure 3.10, we can observe how the increase in the zinc percentage in the IZO films diminishes the on-currents and ultimately leads to not operative devices.

As expected, an excess of charges dominates the transfer characteristics of the pure InO_x and 9:1 IZO layers. These devices possess the highest on-currents, provided by a large number of indium cations. However, the elevated off-current observed, related to the high number of background charges, depresses their I_{on}/I_{off} ratio, limiting it to a value in the order of 10^3. They are also characterized by negative threshold voltages that are not ideal for switching applications from a practical point of view.

The indium fraction needs to be higher than zinc to maintain an adequate level of on-current. In this frame, the 7:3 IZO presents a current level approximately an order of magnitude lower than the films with a 9:1 ratio, but the increased fraction of zinc stabilizes the switching behavior of the devices. The threshold value shifted to almost neutral voltages, strongly reducing the off-currents and increasing the I_{on}/I_{off} ratio over 10^6. Similar behavior was found in 5:5 IZO films but with lower values of the on-current. Comparing these two different types of active channels composition, we report in Figure 3.11 the typical transfer curves obtained from devices with different W/L.

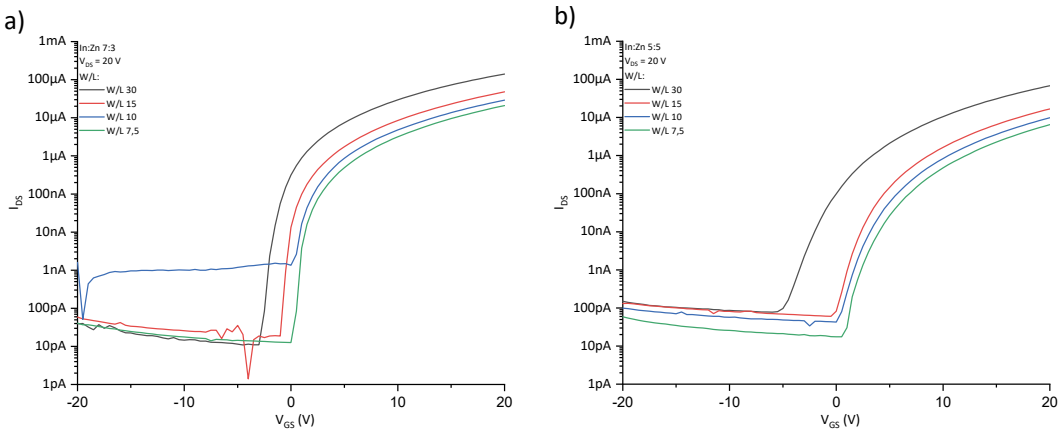


Figure 3.11 Comparison between transfer characteristics of TFTs with different active channel composition: a) 7:3 IZO and b) 5:5 IZO. The curves were obtained from TFTs with various W/L.

A further increase of the Zn percentage (3:7 IZO and 1:9 IZO) did not improve the electrical behavior of the TFTs, as already reported elsewhere[5], the relatively moderate performances are related to a diminished number of charge carriers and large unfilled trap densities. Moreover, zinc tends to arrange in crystals, limiting the movement of charges in the MO_x film.[180] Finally, the pure ZnO films did not yield working devices.

Table 3.1 Typical electrical values obtained from IZO TFTs with various In:Zn channel chemistry. (indium percentage decreasing from left to right)

	InO_x	9:1	7:3	5:5	3:7	1:9	ZnO
V_{Th} (V)	-9.8	-5.3	2.0	5.6	5.5	6.4	/
On-current (A)	2.0×10^{-4}	1.9×10^{-4}	4.8×10^{-5}	1.6×10^{-5}	7.0×10^{-6}	0.4×10^{-6}	/
Off-current (A)	2.6×10^{-8}	2.0×10^{-8}	2.7×10^{-11}	7.3×10^{-11}	7.0×10^{-11}	1.3×10^{-10}	/
I_{on}/I_{off} ratio	7.7×10^{3}	9.5×10^{3}	1.7×10^{6}	2.2×10^{5}	1.0×10^{5}	3.1×10^{3}	/

3.2.4 Characterization of film morphology by optical microscopy and XRD analysis

The electrical characteristics can also be correlated with the morphology of the IZO films. Maintaining an amorphous state is fundamental to the charge conduction as the grain boundaries are a source of scattering and are associated with depletion regions with high potential barriers that affect the movement of the carriers. [5] In Figure 3.12, the images of the MO_x active channels obtained from the optical microscopy (digital microscope from Keyence digital) are presented. The increasing fraction of zinc in the IZO films causes the formation of crystallites in the film that can explain the poor characteristics of the resulting TFTs. Starting from the 3:7 ratio, crystallites of small dimensions (few microns) begin to form in the film, whereas the size increases to tens of microns for pure ZnO.

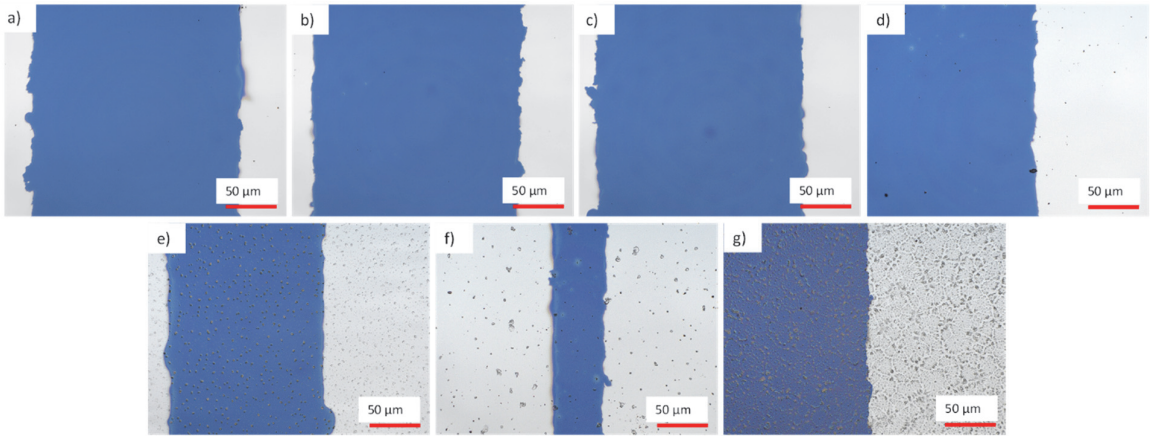


Figure 3.12 Optical images of the deposited films with variable In:Zn. The indium percentage in the film increases from a) to g). Respectively a) InO_x, b) 9:1 IZO, c) 7:3 IZO, d) 5:5 IZO, e) 3:7 IZO, f) 1:9 IZO, and g) ZnO.

The crystalline nature of the films was analyzed via Grazing Incidence XRD (GIXRD) analysis. As indicative samples, we selected In:Zn ratios of 7:3, 3:7, and 1:9, and bare SiO_2 was included as a reference. A MalvernPANalytical MRD diffractometer using Cu Kα radiation and 1° grazing incident configuration was utilized for the analysis. The curves depicted in Figure 3.13 show that all the tested films seem amorphous, as the only peak visible at ~56° is associated with the Si (311) signal coming from the substrate. The apparently amorphous nature of the samples containing high fractions of Zn could be related to the chosen analysis method and the inhomogeneous morphology of the films.

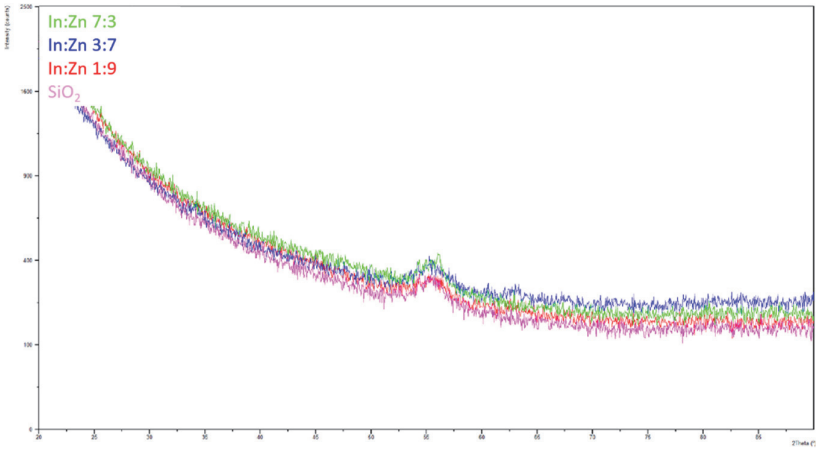


Figure 3.13 GIXRD patterns obtained from the IZO films with different chemical compositions (In:Zn= 7:3, 3:7, and 1:9, plus SiO_2 reference).

3.2.5 Conclusions on the formulation of IZO solutions

We investigated the main components of the IZO sol-gel solution: solvent and stoichiometry. We went for nitrate-based precursors since recognized as less demanding in terms of heat necessary to their decomposition, as previously discussed in Section 2.4. As solution-processing of performing TFTs at low temperatures requires chemical optimization of the precursor solution, we examined via TGA two different organic solvents and selected the one that necessitated less heat to convert the precursors in IZO, the 2ME. Then, we manufactured TFTs containing IZO with variable cationic ratios and characterized their electrical and morphological characteristics. From these results, we identified the most promising solution-precursors combination and the cationic ratio. Ultimately we decided to employ 2ME solvent and an In to Zn ratio of 7:3.

As a possible method to further enhance the performances of the semiconductor (higher mobility/ improved switching characteristics), we considered the possibility of further alloying the metal oxide IZO with an additional aluminum cation. The latter will be discussed in the following section.

3.3 Doped-IZO as semiconductor

The tuning process of the electrical characteristics can be achieved by doping the initial MO_x network with other cations. As mentioned earlier, the cations can contribute to the electrical behavior of the films by providing charge carriers or suppressing them. The ternary IZO possesses an ideal number of electrical charges to achieve performing semiconductor properties ($\gtrsim 10^{17}$). The IZO may suffer from high off-currents and negative threshold voltages that are not desirable in practical applications. Incorporating elements like tin will increase the charge number and could compromise their switching capabilities. However, cations, such as gallium, that act as carrier suppressors, lessening the off-currents and stabilizing the operational voltage close to a neutral position, are of interest.

Gallium, introduced in the IZO system by Nomura et al. in 2004, has been widely investigated. As of now, it remains the preferred doping element for sputtered IZO-based MO_x semiconductors, especially for those applications like LCD that do not necessarily need high mobility values (≥ 1 cm^2/Vs) but good electrical stability and switching capability. For sol-gel processing, alternatives to gallium have been explored in the past years as it does not necessarily match the requirements to achieve low-temperature processing and, like indium, is a relatively rare and expensive material.[181]

Henneck et al. compared various dopants, yttrium (Y), scandium (Sc), lanthanum (La), and gallium, by adding them to the composition of IZO based semiconductor films synthesized via a combustion process. The electrical characteristics of their TFTs, fabricated involving an annealing step at 300 °C for MO_x film synthesis, showed that only Ga doping improved operational stability and did not depress mobility.[182]

Benwadit et al. have systematically studied the material and electrical characteristics of solution-processed doped-IZO semiconductors. They tested over ten different cations, chosen according to their ionic radii and electron negativity, keeping a constant composition and curing the layers at 450 °C. They highlighted some trends in the electrical behaviors, such as interface defect density versus electronegativity, but they could not find a universal rule to select the cation.[166]

Univocal results are difficult to achieve as each studied system differs from the others (layer stoichiometry, precursors type, doping concentration, annealing temperature). On our side, we explored the possibility of improving the electrical characteristics of the solution-processed IZO semiconductor films by doping them with aluminum.

3.3.1 Al as doping element for MO_x semiconductor

Among the various dopants studied in the past years, aluminum has been considered a cost-effective alternative to gallium. Like gallium, it is characterized by a strong affinity to oxygen that can be exploited to suppress the formation of oxygen vacancies and ultimately improving the I_{on}/I_{off} ratio by lowering the off-current. The integration of Al ions in the composition of metal-oxides tends to stabilize the amorphous phase of the films.

Gao et al. integrated 10 at% Al in their solution-processed IZO layers and demonstrated better control of the electrical characteristics of their TFTs by reducing the defect density and suppressing the charge trapping at the semiconductor/dielectric interface.[183] Recently, *Hong et al.* modified the electrical behavior of sputtered ITO by locally doping it with Al, and as a result, their TFTs yielded mobility as high as 6.4 cm^2/Vs.[81]

The role of oxygen vacancy and amorphous phase stabilizer is exploited to form performing transparent electrodes: in Al:ZnO aluminum ions, which have smaller ionic radii than Zn (0.54 Å and 0.74 Å, respectively), disrupt the lattice orientation, forming an amorphous film and improving its electrical conductivity.[184] In other reports has been hypothesized that an increased presence of Al could lead to a surge of carrier concentrations due to an increasing number of donor level defects. They also highlighted that the increase of Al concentration in these films does not necessarily correspond to a monotonous resistivity decrease.[185] Similarly, *Scheideler et al.* reported a solution-processed Al-doped cadmium oxide (Al:CdO) used as S/D electrodes in low-temperature InO_x-based TFTs: a limited amount of Al-doping (3%) resulted in decreased resistivity, but higher fractions (up to 8%) ultimately depressed the film conductivity.[78] The numerous Al-O bonds significantly diminish the number of oxygen vacancies at high concentrations of Al and ultimately reduce the number of available carriers.

3.3.2 Effect of Al doping in the IZO system

We want to investigate how the electrical performances of our TFTs can be affected by the introduction of variable Al fractions in the IZO semiconductor. The possibility of increasing the carrier mobility by reducing the number of defects in the film while maintaining good switching characteristics is attractive. Moreover, the nitrate-based Al precursors are suitable for their eventual sol-gel processing at low temperatures. The experimental methodology used and the characterization of the realized devices are discussed in the following sections.

3.3.2.1 Substrate and dielectric layer

As similarly described for the In:Zn study, we employed highly conductive Si as substrate and gate contact, thermally oxidized to form a 200 nm thick SiO_2 gate dielectric layer.

3.3.2.2 Semiconductor deposition and synthesis

The semiconductor was deposited via spin-coating. The precursor solution for the synthesis of IZO was prepared by dissolving zinc nitrate hexahydrate and indium nitrate hydrate precursors in 2-methoxyethanol. The concentration of these precursors was chosen as 0.2 M, and the In:Zn ratio (7:3) was selected as previously discussed in Section 3.2.2. Similarly, an AlO_x solution was prepared by dissolving aluminum nitrate nonahydrate ($Al(NO_3)_3{\cdot}9H_2O$) in 2-methoxyethanol, with a final solution concentration of 0.05 M. All the solutions were stirred at 60 °C for more than 12 h and filtered with 0.2 µm (PTFE) filters before deposition. Solutions containing Al-doped-IZO in different percentages, from 0.5 % to 10 %, have been prepared by adding a variable amount of the AlO_x solution to an initial volume of 2 ml of IZO: 0.5 %, 1 %, 3 %, 5 %, and 10 %. We also included a non-doped sample as a reference. The deposition of the Al:IZO occurred as previously described: O_2 plasma 5 min at 100 % power, then spin-coating at 2000 rpm and solvent drying for 1 hour at 150 °C in air ambient. The final annealing necessary to synthesize the MO_x semiconductor was carried at 400 °C for 30 min. We selected a temperature of 50 °C higher than the one used in the previous study, expecting higher off- currents, to enhance the possible effects of Al on the electrical characteristics, especially on the off-current control.

3.3.2.3 Electrodes deposition and devices architecture

The aluminum electrodes, ~100 nm thick, composing the source and the drain were deposited by e-beam evaporation through the same magnetic shadow-mask previously described. , is depicted the cross-section of the realized devices.

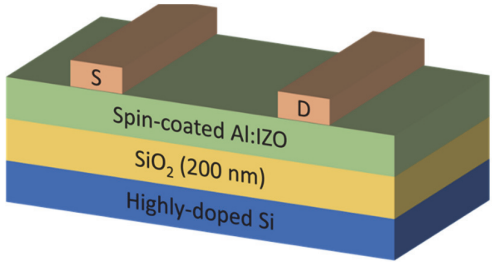


Figure 3.14 Cross-section schematic of the fabricated TFTs with Al-doped IZO.

3.3.3 Electrical characterization

We characterized the output and transfer characteristics of the TFTs obtained from a non-doped IZO and compared them with those from the Al-doped IZO semiconductors. We focused on these electrical parameters that can be affected by the variation of aluminum concentration in the film: the on and off currents, the carrier mobility, the subthreshold slope, and the threshold voltage. We analyzed multiple devices from each sample (n≥3), and in Figure 3.15 are reported the typical transfer a) and b) output curves obtained from the devices as a function of the Al doping percentage.

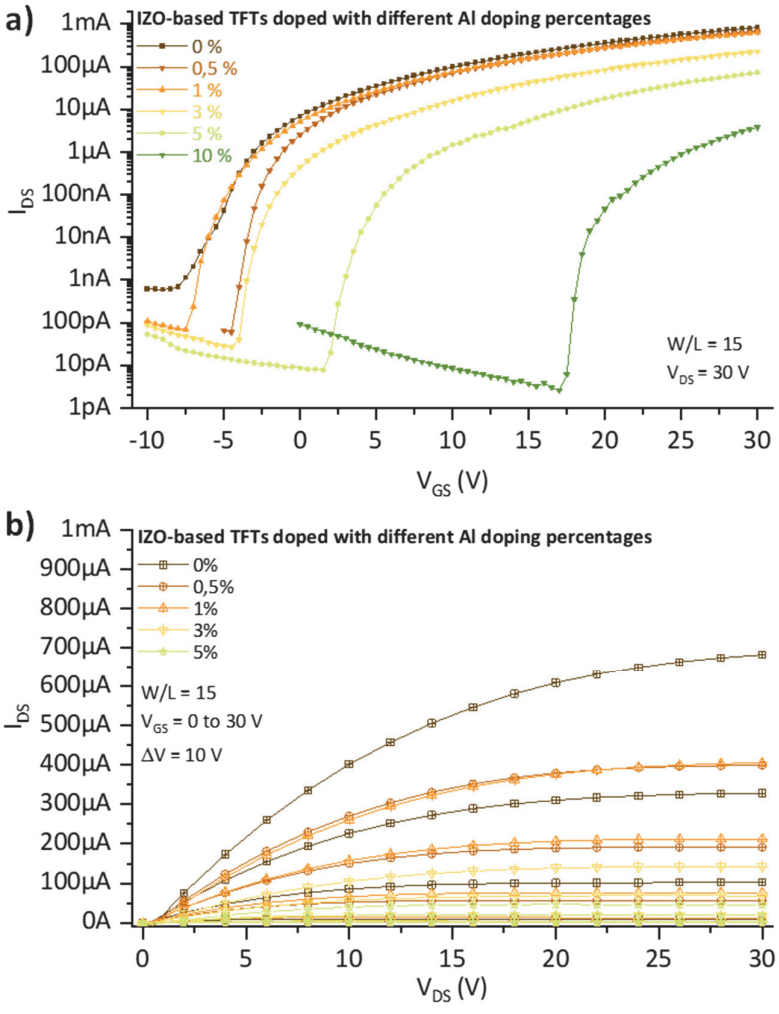


Figure 3.15 Typical a) transfer and b) output curves obtained from IZO TFTs with different Al %.

TFTs with pure IZO present the highest off-current level, 163±150 pA, and the highest on-current levels, 0.73±0.17 mA, which corresponds to the I_{on}/I_{off} ratio > 10^7 and to saturation mobility of 3.25±0.6 cm^2/Vs. The threshold voltage of the TFTs is 0.98±0.33 V, but the devices start to turn on at negative voltages, ~-10 V resulting in a sub-threshold swing of 0.65±0.32 V/dec.

From the comparison between the transfer curves, we can observe a general trend related to the nature of the Al as a strong oxygen binder: the off-currents tend to decrease, and the TFTs switching voltage moves toward positive values. The I_{on}/I_{off} ratio of the various devices does not degrade excessively, as both on- and off-currents are reduced in parallel.

The on-currents of the devices doped with 0.5 % and 1 % of aluminum are not sensibly affected by the presence of Al, remaining in the same order of magnitude (~550 µA and ~720 µA, respectively); we can observe a similar trend on the saturation mobility and off-currents. Implementing a small fraction of aluminum causes an improvement in the switching speed, which decreases from 0.65 to 0.4 V/dec. This decrease in SS indicates a reduction of interface trap density at the semiconductor/dielectric interface.[186]

As shown in Figure 3.16, the first signs of performance degradation can be observed for Al >3 %; as a consequence of the drop in on-current, the extracted mobility 1.2 cm^2/Vs is reduced by ~60 % compared with the undoped devices. The increasing fraction of Al in the layer disrupted the charge transport in the film. This behavior can be explained by an excessively reduced number of donor vacancies and available carriers.

Higher percentages, 5 % and 10 %, further increase the current depressing effect of aluminum. This damage in the transistor performances is also visible from the remarked shift toward positive voltages of the threshold voltages, ~10 V and 20 V, respectively.

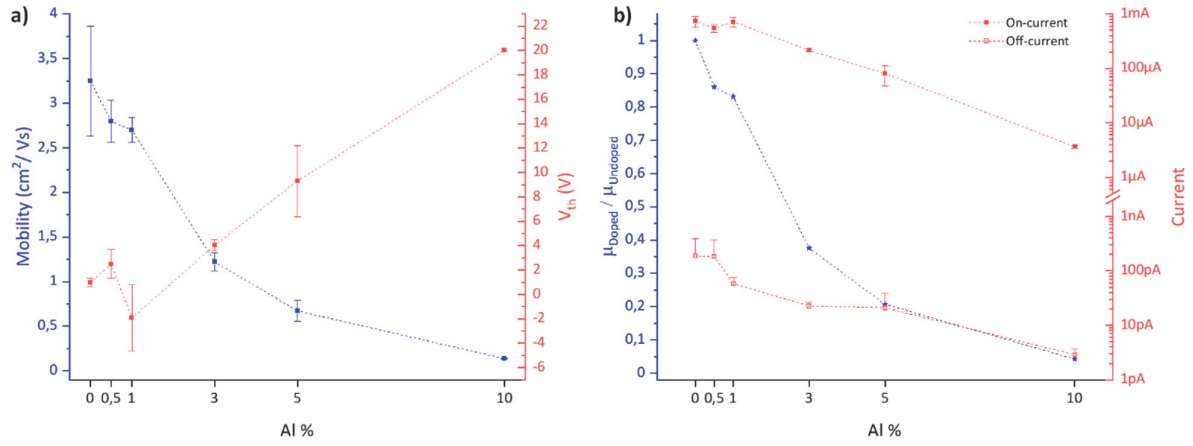


Figure 3.16 Electrical characteristics of the Al-doped IZO-based TFTs. a) Saturation mobility and threshold voltage versus Al % and b) on- and off-currents on the right axis, left axis depicts the ratio between the average measured mobility over the mobility value of the undoped IZO film versus Al %.

All the electrical performances extracted from the TFTs with a variable percentage of Al doping are summarized in Table 3.1.

Table 3.2 Statistics regarding the electrical characteristics of TFTs employing Al-doped IZO as a semiconductor. (n≥4)

Al doping	**0 %**	**0.5 %**	**1 %**	**3 %**	**5 %**	**10 %**
Mobility (cm^2/Vs)	3.2±0.6	2.8±0.2	2.7±0.1	1.2±0.1	0.7±0.1	0.1±0.1
V_{Th} (V)	1.0±0.3	2.5±1.2	-1.9±2.7	4.0±0.5	9.3±2.9	20±0.1
SS (V/dec)	0.6±0.3	0.4±0.1	0.4±0.1	0.4±0.1	0.6±0.2	0.3±0.1
On-current (µA)	731±169	549±87.0	718±152	214±147	81.0±33.0	3.60±0.20
Off-current (pA)	163±153	159±140	58.0±17.0	23.0±3.00	20.0±17.0	2.90±0.80
I_{on}/I_{off} ratio ($x10^6$)	10.3±10.1	6.57±5.45	13.0±2.80	9.53±1.45	4.70±4.30	1.35±0.43

3.3.4 Al-doped IZO: discussion

We investigated the effect of different Al doping concentrations on the IZO semiconductor characteristics when implemented in a TFT architecture. Aluminum was demonstrated to be a potential alternative to the mainstream gallium used as a dopant for IZO semiconductors. It is confirmed that Al acts as a carrier suppressor for the oxygen defects. Such effect is visible from the improvement in switching characteristics of these TFTs with an Al-doping ranging between 0.5 % and 3 %. The presence of the cations stabilized the transfer characteristics shifting the curves towards more positive voltages and reduced the level of the off-current, probably due to an increase in the channel resistance direct consequence of a stronger oxygen-binding obtained from the Al ions. The electrical behavior of the devices showed to be sensitive to small variations in the Al fraction. Above 1 %, a drop in on-current and mobility degradation is already noticeable. According to the results, the limit to maintain acceptable electrical performances is around 3 %. Above this value, the increased fraction of AlO_x in the IZO matrix tends to excessively reduce the electrical carriers available in the semiconducting layer and TFTs performances. From our results, the Al inclusion in the composition of IZO films does not enhance the carrier mobility, as demonstrated for ZnO-based semiconductors.[187,188]

The TFTs manufactured with the bare IZO as semiconductors do not suffer from excessively high off-currents while exhibiting good switching behavior and mobility, as will also be shown in the following chapters. In the perspective of their low-temperature processing, Al doping is an approach that will not bring a significant added value to the electrical characteristics of the devices as it does not increase the mobility. Furthermore, its presence could increase the heat required to convert the films, as similarly reported for Ga.[91] For these reasons, an IZO semiconductor will be employed in the following chapters.

3.4 Conclusions

In this chapter, we have presented the concept and a chemical formulation for a solution-processed IZO semiconductor. First, we introduced the carrier transport working principle for amorphous MO_x thin films and the state-of-the-art regarding the common ZnO-based and InO_x-based semiconductors. Then, we discussed the formulation of our semiconductor solution required for the IZO synthesis via sol-gel, from the solvent to the cationic composition. We first compared two organic solvents and, exploiting a thermal-gravimetric analysis, selected the one that provided MO_x precursor conversion at a lower temperature, the 2-methoxyethanol (~350 °C). Then, we examined different stoichiometries involving ternary compositions based on In and Zn. From the study, we selected the IZO formulation with 7 to 3 of In:Zn ratio as it provided an optimal compromise between switching capabilities (I_{on}/I_{off} ~10^6, V_{Th}~0 V) and on-current levels (> 40 µA). We investigated via GIXRD the amorphous window of the In:Zn MO_x system and confirmed that the selected stoichiometry provides the desired amorphous phase. Finally, we studied the possibility of exploiting a further alloying of the IZO with aluminum to tune the TFT electrical characteristics. No significative differences in transfer and output curves have been noticed for a concentration of Al below 1 %, while for percentages above 3 %, a substantial drop in mobility, linked to on-current reduction, was observed (from a ~60 % loss in mobility at 3 % Al to ~95 % loss at 10 % Al, in comparison to undoped IZO). We attributed such reduction in currents to a stronger oxygen-cation binding, linked to the increased number of Al-O bonds that reduce the oxygen vacancies and the number of available carriers in the MO_x. We will further discuss the role of Al doping for IZO semiconductors in Chapter 4 concerning TFTs with a fully solution-processed MO_x active stack processed at high temperatures. Since no mobility enhancements have been observed following the Al doping, we decided not to implement any voluntary Al-doping in our precursor solution, continuing with a 7:3 In:Zn IZO formulation in the work reported in the following chapters on pairing IZO with an AlO_x based dielectric and on reducing its synthesis temperature.

Chapter 4 Thermal synthesis of solution-processed IZO-based TFTs

In this chapter, we present the performances of the TFTs with metal-oxide active layers fully solution-processed, annealed via standard high-temperature protocols.

Employing temperatures relatively elevated, such as 350 °C or more, the synthesis of the functional MO_x films can be achieved. However, differently from TFTs employing standard vacuum-based dielectrics like thermally grown SiO_2, physical phenomena like atomic interdiffusion could be more easily promoted between the solution-processed semiconductor and dielectric layers when using a sol-gel-based dielectric. Moreover, aspects such as the quality of the semiconductor/dielectric interface and the possible dielectric constant dependence with the frequency need to be accounted for as they can affect the TFT electrical performances. To investigate these possible effects, we studied two different metal-oxide dielectrics and simultaneously evaluated how the annealing protocol applied on the IZO semiconductor modifies the electrical characteristics of the resulting TFTs. Two types of AlO_x based high-k gate dielectrics were examined: a vacuum-based ALD Al_2O_3 dielectric versus a spin-coated AlO_x/$YAlO_x$ dielectric. We compared the electrical performances and analyzed the chemical compositions of the two types of devices via X-ray photoelectron spectroscopy (XPS).

Afterward, we implemented photolithographic steps to manufacture TFTs with optimized electrical performances that included a thermally annealed fully solution-processed MO_x active stack composed of printed AlO_x/$YAlO_x$ dielectric and spin-coated IZO. Such devices will also be considered a reference in terms of characteristics and performances for these TFTs annealed at low temperatures presented in the following chapters. We describe the architecture, the layout of the TFTs, and the process flow used to fabricate them. We have thoroughly characterized the electrical performances of the devices, including classic output and transfer curves combined with capacitance measurements and stability tests. We investigated the morphology of the layers and their chemical composition exploiting techniques as high-resolution transmission electron microscopy, energy-dispersive X-ray spectroscopy (EDX), and XPS. Due to the high temperature (up to 450 °C) process applied, we manufactured the TFTs on silicon wafers. The solution-based devices demonstrated performances that are comparable with state-of-the-art sputtered MO_x semiconductors. The TFTs yielded a high I_{on}/I_{off} ratio $>10^9$, a subthreshold slope (SS) of <200 mV/dec, and threshold voltages (V_{th}) ~ 0.6 V. To extract an accurate mobility value of ~ 68 cm^2/Vs, we exploited specific low-frequency capacitance measurements to estimate the dielectric constant calculated at a low frequency of 10 mHz. To complement the characterization, we investigated the operational stability of the TFTs subjected to bias stress and verified the durability of the devices one year after their fabrication.

These remarkable performances, obtained via thermal annealing, present an encouraging starting point that confirms the selected dielectric/semiconductor metal-oxide stack quality. We will exploit these results in the following chapters to compare the performance and evaluate the effectiveness of the low-temperature synthesis approaches.

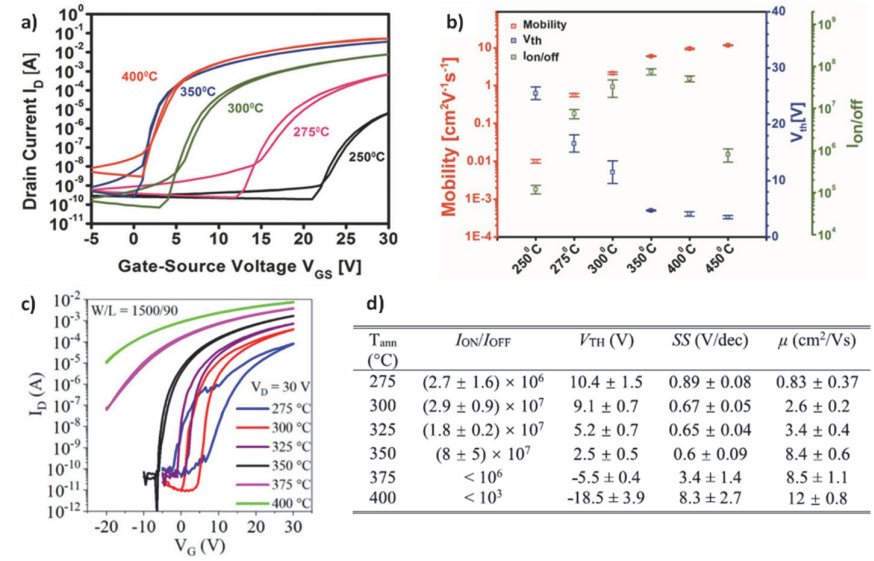
4.1 Thermal annealing of indium zinc oxide-based MO_x TFTs

In this section, we report the results of the investigation carried out on the effects of different annealing protocols on the IZO semiconductor during the MO_x synthesis via thermal processes.

State of the art regarding the effects of thermal annealing on solution-processed semiconductors is scarce. In the past years, few studies have been carried out on the effects that various annealing temperatures have on the characteristics of the resulting TFTs. These investigations mainly focused on the semiconductor layer itself, involving vacuum grown or deposited gate dielectric such as thermal SiO_2, thus not addressing the interactions between the two active layers, notably when both solution-processed, and how the thermal treatment conditions can affect their properties.

Sanctis et al. investigated the effects of variable temperature on the electrical characteristics of IZO based TFTs with dimethyl 2-hydroxyimino- and 2-nitromalonato ligands based precursors. The devices obtained via IZO spin-coating on SiO_2/Si substrate were treated via thermal annealing with temperature ranging from 250 °C to 450 °C[18], which ultimately yielded mobility as high as 11.6 cm^2/Vs at 450 °C. As shown in Figure 4.1a and Figure 4.1b, they observed a monotonical increase of the mobility as a function of the annealing temperature of the semiconductor, correlated with increasing MO_x alloying. They also attributed the increase in carrier concentration to an augmented number of oxygen vacancies, which finally caused, at 450 °C, an increase in off-current and lessened I_{on}/I_{off} ratio.[189]

Recently, *Cai et al.* performed a similar study, exploiting nitrate-based precursors, on the effects of annealing temperature on IZO based TFTs. Employing spin-coated IZO on SiO_2/Si structure, they tested the effects of thermal annealing at temperatures varying from 275 °C to 400 °C for 1 hour, as shown in Figure 4.1c and Figure 4.1d, highlighting how synthesis temperatures > 350 °C led to excessively conductive semiconductor channels and TFTs with poor switching characteristics. Afterward, they identified 350 °C as the optimal temperature for the IZO synthesis and manufactured TFTs with spin-coated AlO_x, cured at 350 °C for 1 hour as dielectric that yielded mobility ~9 cm^2/Vs.[190]



d)

T_{ann} (°C)	I_{ON}/I_{OFF}	V_{TH} (V)	*SS* (V/dec)	μ (cm^2/Vs)
275	$(2.7 \pm 1.6) \times 10^6$	10.4 ± 1.5	0.89 ± 0.08	0.83 ± 0.37
300	$(2.9 \pm 0.9) \times 10^7$	9.1 ± 0.7	0.67 ± 0.05	2.6 ± 0.2
325	$(1.8 \pm 0.2) \times 10^7$	5.2 ± 0.7	0.65 ± 0.04	3.4 ± 0.4
350	$(8 \pm 5) \times 10^7$	2.5 ± 0.5	0.6 ± 0.09	8.4 ± 0.6
375	$< 10^6$	-5.5 ± 0.4	3.4 ± 1.4	8.5 ± 1.1
400	$< 10^3$	-18.5 ± 3.9	8.3 ± 2.7	12 ± 0.8

Figure 4.1 Effect of annealing temperatures on IZO based TFTs: a) transfer characteristics comparison and b) comparative statistics. Adapted from [189]. c) Transfer curves and d) electrical performances reported by Cai et al.. Adapted from[190].

The research about the thermal annealing for the sol-gel synthesis of IZO involved thus far standard SiO_2 as gate dielectric without considering these effects related to using a high-k solution-processed MO_x dielectric. For example, the devices manufactured by *Cai et al.* showed improved mobility and subthreshold slope when the spin-coated AlO_x dielectric was employed instead of thermal SiO_2, with mobility increasing from 8.4±0.6 cm^2/Vs to 9.2±1.3 cm^2/Vs and subthreshold slope reducing from ~0.6 V/dec to ~0.09 V/dec.[190]

[18] The treatment duration is not reported in the article.

To better understand the MO_x system of our sol-gel IZO-based TFTs, it is essential to examine their performances when synthesized via thermal annealing. On our side, as we aim for fully solution-processed MO_x TFTs, we are also interested in studying the interactions between solution-processed active metal-oxide layers and how they influence the electrical characteristics of the TFTs. To investigate how the electrical performances change with the IZO synthesis temperature and compare the use of different dielectrics, we manufactured TFTs with two different dielectric/IZO semiconductor stacks comprising both spin-coated and vacuum-deposited AlO_x-based gate insulators. The selected spin-coated dielectric, composed of a double layer of yttrium-doped AlO_x ($YAlO_x$) and AlO_x, was developed by Sami Bolat in the frame of the SFA FOxIP project and was based on a $YAlO_x$ dielectric reported in an earlier publication from the same group.[135]

The solution-processed IZO was cured for 30 min at a temperature varying from 200 °C to 450 °C, which resulted in operative transistors for temperatures higher than 300 °C. We analyzed the electrical behavior of the TFTs, which reached mobility over 15 cm^2/Vs, up to ~26 cm^2/Vs, with both MO_x layer solution-processed and compared them as a function of the two types of AlO_x-based dielectrics. The fully solution-processed stack outperformed the hybrid ALD/spin-coated stack, with an order of magnitude difference in mobility and switching capabilities, both I_{on}/I_{off} ratio and subthreshold slope. This difference in performance was attributed mainly to a superior interface formed thanks to the synergy between the layers and a good material match.

During the comparison process, we identified two different trends in electrical performance as a function of the annealing temperatures depending on the dielectric/semiconductor stacks, with a not monotonically increase in mobility for the fully solution-processed stack at temperatures over 400 °C. We looked into the chemical composition of the IZO films exploiting XPS analysis, assessing the precursor conversion and the quality of the MO_x networking to correlate them with the electrical characteristics of the IZO TFTs. Ultimately, we discussed the hypothesis of possible doping of the semiconductor film, caused by thermal diffusion of aluminum from the solution-processed dielectric, as an explanation for the positive shift in transfer characteristics and the lowering in on- and off-currents observed in the TFTs annealed at 450 °C.

4.1.1 Thermally annealed sol-gel IZO: comparison between solution-processed and ALD metal-oxide gate dielectric

We selected bottom gated TFTs structures with highly doped silicon wafers as substrate/gate for the study. Two different gate dielectrics with a high dielectric constant replace the standard thermal SiO_2 dielectric: a vacuum-based ALD Al_2O_3 and a sol-gel spin-coated $AlO_x/YAlO_x$. As we employ a full gate architecture with a non-patterned semiconductor, the TFT electrical performances will be influenced by the leakage, leading to higher off-current levels. Devices realized via photolithographic processes, with optimized architecture for enhanced electrical performances, will be described in Section 4.2. Here we wanted to evaluate the effects of thermal annealing, with temperature ranging from 200 °C to 450 °C, on the chemical composition of the IZO film and how different dielectric types can affect the electrical characteristics of the TFTs.

The devices described hereafter have been manufactured in Microcity, Neuchâtel, which do not possess strictly controlled environmental conditions, notably with the humidity level fluctuating from 40 % to 60 % (±10 %). The process flow is summarized in Figure 4.2 and then described in detail in the coming sub-sections.

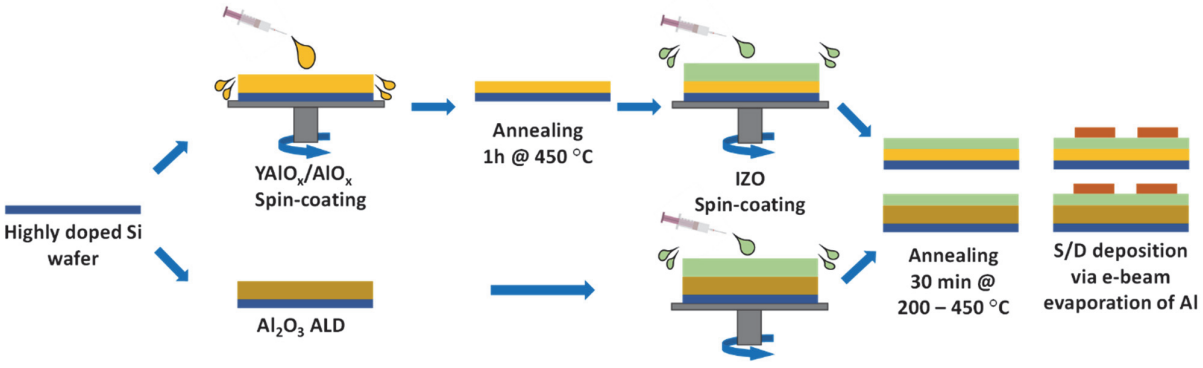


Figure 4.2 Schematic of the manufacturing process flow employed to realize the IZO/AlO_x-based TFTs.

4.1.1.1 Dielectric deposition and synthesis

Starting from a highly doped (0.001–0.005 Ω/cm) Si wafer employed as the gate contact, we deposited the two different dielectric layers as follows.

For ALD dielectric:

We deposited on the Si wafer a 200 nm-thick Al_2O_3 by ALD. The ALD is performed under vacuum at 200 °C in a *Beneq TFS200* reactor using TMA[19] and H_2O as the precursors. The deposition, consisting of approximately 900 cycles, was repeated twice to avoid possible imperfections in the film, such as pinholes, to reach the desired thickness of 200 nm, confirmed by ellipsometry.

For spin-coated dielectric:

The precursor solution for the $YAlO_x$ film was prepared by dissolving yttrium nitrate hexahydrate ($Y(NO_3)_3{\cdot}6H_2O$) and aluminum nitrate nonahydrate ($Al(NO_3)_3{\cdot}9H_2O$), with a Y/Al ratio of 1:9, in 10 mL of 2-methoxyethanol. For the AlO_x layer, aluminum nitrate nonahydrate was dissolved in the same solvent. The precursor concentration was set to 0.2 M for $YAlO_x$ and 0.4 M for AlO_x. The solutions were stirred at 70 °C for more than 12 h and filtered with 0.2 µm poly(tetrafluoroethylene) (PTFE) filters before deposition. The deposition method is based on the IZO deposition process described in the previous chapter: prior deposition, we applied a short O_2 plasma[20] treatment of 5 min at 300 W (13.56 MHz) on the wafers to improve their wettability, then the spin-coating process was carried at 2000 rpm, with the two layers ($YAlO_x$ first) deposited sequentially and then dried on a hot plate in air for 1 hour at 150 °C. The final curing to convert the precursors and synthesize the MO_x dielectric stack was carried in an oven at 450 °C for 1 hour.

4.1.1.2 Semiconductor deposition and synthesis

The semiconductor was deposited as well via spin-coating. The precursor solution for the synthesis of IZO was prepared by dissolving zinc nitrate hexahydrate ($Zn(NO_3)_2{\cdot}6H_2O$) and indium nitrate hydrate ($In(NO_3)_3{\cdot}xH2O$) precursors in 2-methoxyethanol. The concentration of these precursors for spin coating was chosen as 0.2 M, and the In/Zn ratio of 7:3 was selected as described in Chapter 3. The solutions were stirred at 60 °C for more than 12 h and filtered with 0.2 µm (PTFE) filters before deposition. The deposition of the IZO film occurred with the same process described for the dielectric layers: 5 min O_2 plasma (300 W, 13.56 MHz), spin-coating at 2000 rpm, and solvent drying in air for 1 hour at 150 °C on a hot plate.

The dried wafers, both with ALD and spin-coated dielectric films, were cleaved with a diamond pen after drying and subjected simultaneously to a curing protocol for 30 min at the following temperatures: 200 °C, 250 °C, 300 °C, 350 °C, 400 °C, and 450 °C.

We performed each annealing step in air condition on a hot plate, except for the one at 450 °C that we completed in the oven as 450 °C it was above the limit temperature of the employed hot plate. The upper-temperature limit of 450 °C was set to ensure the amorphous phase of the IZO layer, as shown in previous papers for sol-gel IZO.[189,191]

4.1.1.3 Electrodes deposition and devices architecture

The aluminum electrodes, ~100 nm thick, were deposited by e-beam evaporation through a magnetic shadow-mask, which adheres to the substrate and minimizes the shadow effect. As depicted in Figure 4.3, the electrodes patterned have constant width (W) of 1500 µm and comprehend four different channel lengths (L), providing the following W/L ratio: 7.5, 10, 15, and 30.

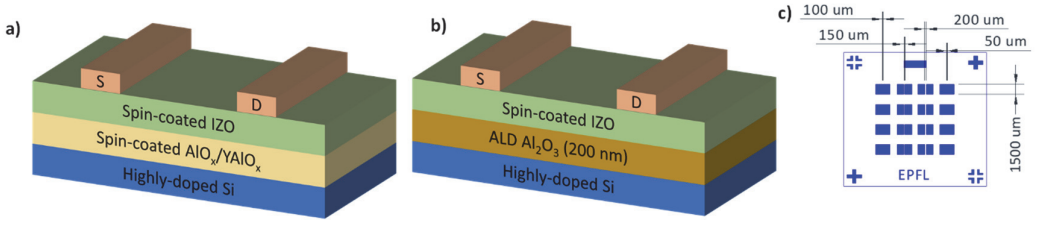


Figure 4.3 Devices cross-section. a) and b) Depict the TFT cross-sections while c) the layout of the shadow mask for the source and drain electrodes illustrating the four different W/L are present in the mask.

[19]TMA= Trimethylaluminium.

[20] Atto plasma cleaner from *Denier* (frequency: 13.56 MHz, power: 0 – 300 W).

4.1.2 Characterization methodology

The methodology used for the electrical characterization of the manufactured TFTs and the chemical analysis of the IZO semiconductor layer is described in the following paragraphs.

4.1.2.1 Electrical characterization

We measured the transfer characteristics from devices made with an IZO semiconductor film cured at different temperatures onto Al_2O_3-based dielectrics to investigate the effects of annealing conditions on electrical performances. In doing so, we examined multiple devices with different W/L and confronted their figure of merit. We first evaluated the devices with the same dielectric, then confronted the results between ALD Al_2O_3 and spin-coated AlO_x/$YAlO_x$ by comparing their behavior. We extracted the transfer curves with a 4155A semiconductor parameter analyzer from *Hewlett-Packard* in ambient air. As the mask used for this process did not include any capacitive structures, to calculate the mobility, we extracted the areal capacitance of the spin-coated dielectric at 1 kHz from the C-V curves obtained from the MOS capacitors intrinsically present, with a stack formed by the Si gate, the spin-coated layers, and the evaporated Al electrodes. For the ALD dielectric, instead, we assumed a dielectric constant ε_r= 9 characteristic of ALD deposited Al_2O_3 films; value confirmed when measured with the same methodology employed for the spin-coated dielectric.

4.1.2.2 X-ray photoelectron spectroscopy (XPS)

We exploited XPS measurements to investigate the chemical composition of our MO_x films to evaluate and compare the quality of the conversion process as a function of the annealing temperature.

The elemental identity, chemical state, and quantity of a detected element can be identified from the binding energy and the intensity of a photoelectron peak emitted by a surface exposed to X-rays. The XPS is a technique used to characterize only the superficial layer, but information about chemical distribution in depth can be obtained by combining the XPS measurement with ion milling, like Ar ion sputtering. To better evaluate the composition of the film, avoiding possible surface contamination, we performed an in-depth study and selected these spectra obtained in the bulk of the material for the analysis. However, in-depth XPS does not provide precise information enough to define the composition of the film at the interface semiconductor/dielectric.

For MO_x films, the peak relative to oxygen bears information regarding the quality of the alloying process. We can fit the O1s spectrum with three prominent components[192]:

- M–O covalent bonds, 529.5–530.2 eV;
- Oxygen vacancies (O_{vac}), ~531.2 eV;
- M–OH bonds, ~532.2 eV.

High percentages of covalent bonds indicate an excellent conversion of the precursors and few weakly bonded oxygens that could potentially act as electron traps. At the same time, the high number of hydroxides indicates the presence of non-converted compounds and not proper alloying.[193] The role of oxygen vacancies in metal oxide films is not fully understood yet. It appears that a certain fraction of vacancies is necessary to achieve high mobility, but excessively high fractions may not be beneficial as they increase the off-currents. Depending on the size of the vacancy, they can act as mobility enhancers providing carriers as shallow donors or mobility depressors acting as electron traps.[194,195]

The XPS measurements were carried out using a PHI VersaProbe II scanning XPS microprobe (*Physical Instruments AG*) using a monochromatic Al Kα X-ray source of 47.2 W power with a beam size of 100 µm. The spherical capacitor analyzer was set at a 45° take-off angle with respect to the sample surface. The pass energy was 46.95 eV, yielding a full-width at half-maximum (FWHM) of 0.91 eV for the Ag $3d_{5/2}$ peak. A surface sputter depth profile was analyzed by Ar^+ sputtering at 2 keV and a sputtering rate of ~6 nm/min; the different measurements were performed each for 30 s. We performed the curve analysis and peaks deconvolutions using the PHI Multipak software after calibrating the peaks with the C1s position (284.8 eV). We exploited the structures already present on the wafer to produce the samples for the XPS analysis and evaluate the quality of the deposited films and relative devices.

Pierre Mettraux from the Molecular and Hybrid Materials Characterization Center (MHMC) at EPFL performed the XPS characterization and provided support during the data analysis.

4.1.3 Results for IZO on spin-coated $AlO_x/YAlO_x$ dielectric

Here we discuss the results achieved from the electrical and material characterization of the TFTs with spin-coated AlO_x-based dielectric.

4.1.3.1 Electrical results

Figure 4.4 reports the typical transfer curves extracted from the TFTs manufactured with the $AlO_x/YAlO_x$ spin-coated dielectric. Table 4.1 summarizes the extracted electrical performances.

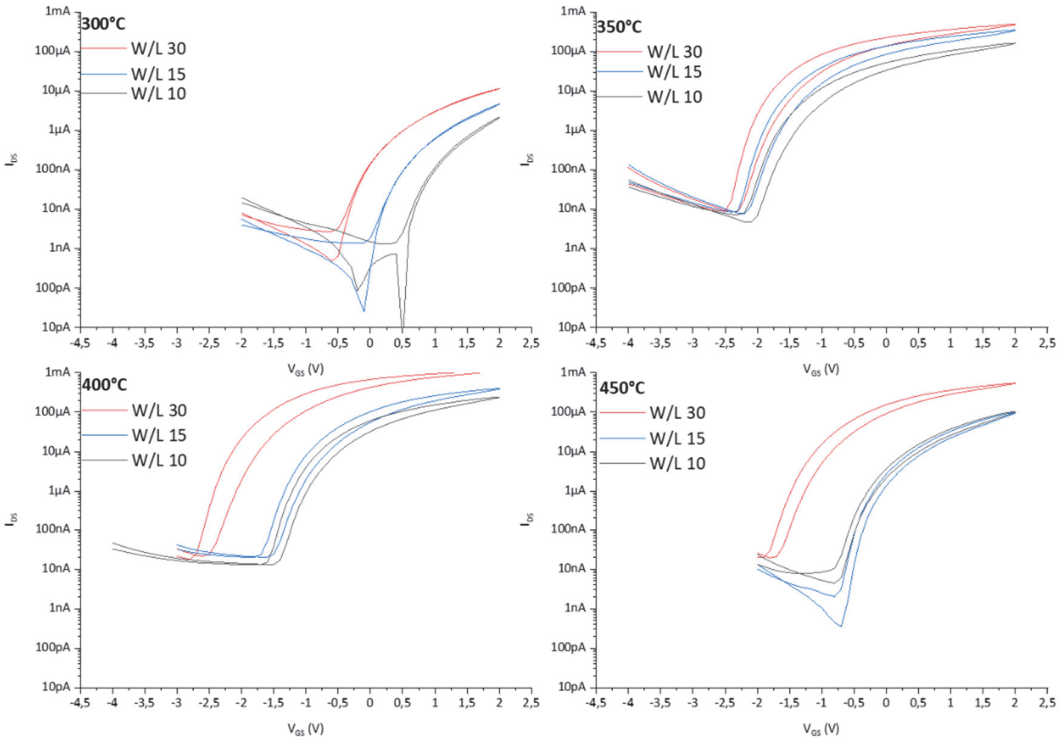


Figure 4.4 TFTs with spin-coated IZO and spin-coated $AlO_x/YAlO_x$ dielectric. Representative transfer curves extracted from TFTs cured with different annealing temperatures from devices with different W/L. The drain voltage V_{DS} for all the curves was 2 V. The devices cured at 200°C and 250°C were not active.

Despite the thermal annealing at 450 °C of the high-k dielectric, the off-current levels in the range of tens of nanoamps, measured from most of the devices, are relatively elevated and partially hinders the switching capabilities of the TFTs. Since we are not employing patterned gate or defined semiconductor areas, the TFTs intrinsically suffer from leakage currents that cause a rise in the off-current levels and reduce the mobility values reached.

We did not observe working devices for curing temperatures below 300 °C. The devices with IZO annealed at 300 °C for 30 min show modest performance with mobility ~1 cm^2/Vs and I_{on}/I_{off} ratio over 10^5. A relatively mild thermal annealing at 300 °C for 30 min seems not to ensure a proper precursor conversion and the complete removal of the residuals, to be confirmed by the XPS measurements. We observed a significant improvement in electrical characteristics once 350 °C was reached. Notably, when we applied the thermal protocol at 400 °C, the TFTs achieved on-currents up to ~0.6 mA, which ultimately yielded high mobility over 26 cm^2/Vs. Finally, the samples cured at the highest temperature of 450 °C showed good mobility and on-currents, respectively ~18 cm^2/Vs and ~0.2 mA, similar to those obtained for TFTs with the IZO cured at 350 °C. Compared to the devices with IZO processed at 400 °C, a ~40 % reduction in both on- and off-currents, combined with a threshold voltage shift towards more positive values, from -1.5 V to -0.3 V, were observed.

Table 4.1 Comparison of the electrical results for the TFTs (n≥3) with IZO cured at various temperatures and spin-coated dielectric.

	Spin-coated $AlO_x/YAlO_x$ 300 °C	Spin-coated $AlO_x/YAlO_x$ 350 °C	Spin-coated $AlO_x/YAlO_x$ 400 °C	Spin-coated $AlO_x/YAlO_x$ 450 °C
Mobility (cm^2/Vs)	1.13±0.24	15.3±7.33	26.6±3.86	18.3±5.66
On-current (A)	$6.10±4.90 \times 10^{-6}$	$2.67±1.80 \times 10^{-4}$	$5.76±4.59 \times 10^{-4}$	$1.98±2.20 \times 10^{-4}$
Off-current (A)	$1.80±2.70 \times 10^{-10}$	$5.50±3.15 \times 10^{-9}$	$1.80±0.40 \times 10^{-8}$	$6.60±9.10 \times 10^{-9}$
I_{on}/I_{off} ratio	$9.70±8.40 \times 10^{5}$	$4.80±0.90 \times 10^{5}$	$3.10±1.90 \times 10^{5}$	$9.00±12.0 \times 10^{5}$
SS (V/dec)	0.13±0.04	0.20±0.01	0.21±0.01	0.17±0.06
V_{Th} (V)	0.39±0.44	-1.36±0.99	-1.50±0.52	-0.35±0.67

4.1.3.2 Material characterization

We performed XPS analysis on some selected samples made with solution-processed MO_x gate dielectric to evaluate the effect of processing temperature on the IZO semiconductor chemical composition. We studied the O1s peak measured from samples cured at 200 °C, 350 °C, and 450 °C to evaluate the material composition and correlate it with the electrical performances. Figure 4.5 depicts the fitting of the curves obtained from these samples.

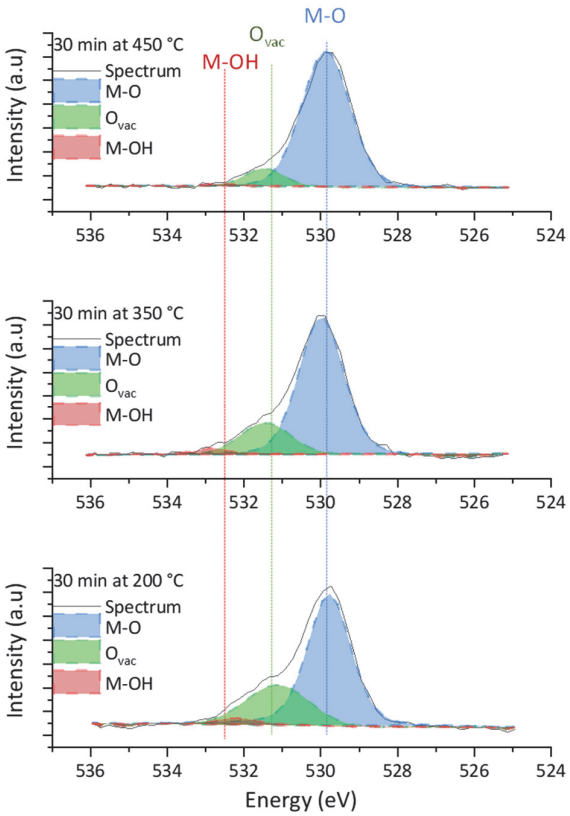


Figure 4.5 Comparison of the O1s peaks extracted from the IZO layers cured with different annealing protocols with relative deconvolution.

We summarized the component fractions obtained from the deconvolution of the spectra in Table 4.2.

Table 4.2 Summary of component fractions obtained from the deconvoluted O1s peaks.

	M-O (%)	O_{vac} (%)	M-OH (%)	Fitting parameter (χ^2)
200 °C	70.7	26.6	2.6	0.70
350 °C	78.3	18.6	3.1	0.90
450 °C	90.3	8.8	0.9	1.08

Even though we observed a relatively high MO_x conversion rate (~70 %) after an annealing process at 200 °C, the transistors manufactured with this protocol did not yield any working device. This electrical behavior can be justified notably by the amount of carbon in the film localized in the proximity of the interface (~4 at%), visible from the in-depth XPS profile in Figure 4.6, indicating undissolved residuals that interfere with the charge transport. The level of carbon at the interface was instead negligible (< 1 at%) when we applied higher synthesis temperatures.

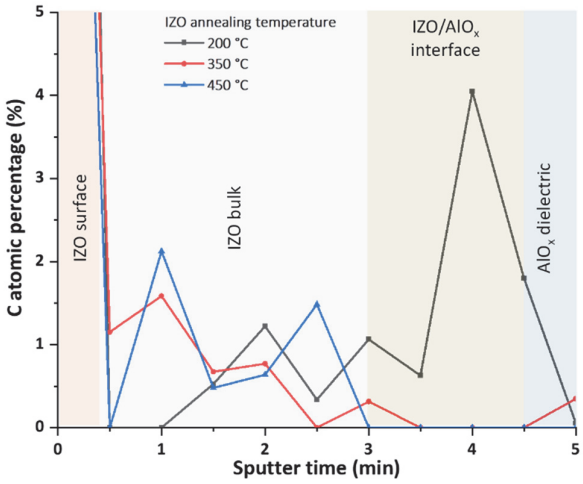


Figure 4.6 Carbon atomic distribution over semiconductor thickness in the TFTs with spin-coated IZO/AlO_x/$YAlO_x$ stack as a function of the IZO annealing temperature, obtained from the in-depth XPS analysis.

The intermediate synthesis temperature of 350 °C showed a better conversion rate (~78 %) and a vacancy fraction of ~19 %. As expected, we measured the highest conversion rate (~90 %) for the films synthesized at 450 °C, with a low vacancy fraction (~9 %) and minimal traces of hydroxides (~1 %). The drop in vacancies percentage, from ~19 % to ~ 9 %, could justify the slight decrease in on-current from 350 °C to 450 °C as less shallow donors are available.[196] However, as the formation of oxygen vacancies is thermodynamically favored at a higher temperature, we expected an increase in the measured vacancy fraction.[197] Various reports involving IGZO and IZO as semiconductors and variable processing temperatures confirmed this increasing trend in vacancies, which was identified as the ultimate cause of the degraded switching capabilities of the TFTs at high temperatures.[189,190,198] The different thermal treatments could also influence the interface between the two active layers. According to the low values in subthreshold swing measured (~200 mV/dec), the increase in temperature did not affect the interface negatively, which instead benefitted potentially from the lower number of defects present at 450 °C, showing a slight decrease to ~170 mV/dec.

As an alternative explanation for the positive shift in the transfer characteristics, the reduction in on- and off-currents, and the low amount of oxygen vacancies in the film, we considered the possible Al diffusion in the IZO film as a cause. Recently, *Hong et al.* exploited this phenomenon to modulate the electrical characteristics of a conductive ITO film to manufacture TFTs eventually. They printed AlO_x on the film and triggered an Al diffusion with a thermal process, up to 400 °C, highlighting how the phenomenon is correlated to the annealing conditions and how different diffusion rates can influence the TFT performances. Ultimately, the Al diffused in the ITO acted as an oxygen getter, decreasing the number of vacancies and stabilizing the switching capabilities of their devices.[81] We have seen similar results in Chapter 3, in which we demonstrated that by incorporating a minimal Al fraction (>1 %) in the IZO semiconductor, a shift towards positive threshold values and the decrease in both on- and off-currents could be achieved.

To validate this hypothesis, we analyzed further the results obtained from the XPS to identify any sign of Al presence in the film. Indium and aluminum present two peaks in their emission spectra at low energy: In4p and In4s, respectively at ~78 eV and ~123 eV, while for the aluminum, Al2p and Al2s at ~74 eV and 118 eV.[192] In Figure 4.7, we can see the XPS spectra obtained from different depths of the MO_x stack, showing in red the strong Al peak coming from the high aluminum percentages in the dielectric, opposed to the black profiles extracted from the semiconductor bulk where indium is predominant.

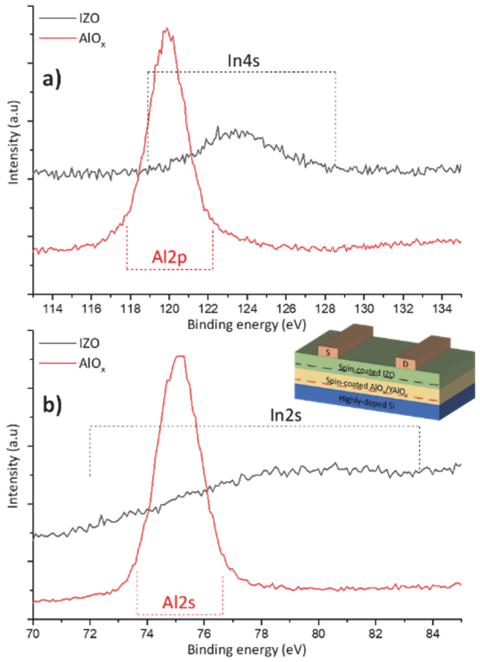


Figure 4.7 XPS signal overlap from Al and In. The curves obtained from the semiconductor layer (in black) and the dielectric layer (in red) show the spectra analysis in the two emission windows a) ~120 eV and b) ~74 eV.

We investigated the emission spectra extracted from the bulk of the IZO layers, treated with different annealing temperatures. We could not identify the presence of Al due to the In4p emission around 78 eV with large FWHM. We suspect that the Al fractions involved in the diffusion can be minimal, and the signal from the Al2p at ~74 eV could be masked from the In4p. Figure 4.8 depicts the comparison of extracted curves from the different samples at energy ~74 eV, for which we included the spectrum obtained from the IZO/AlO_x interface, where the Al signal starts to emerge as the Al percentage increases and the intensity of the In signal decreases.

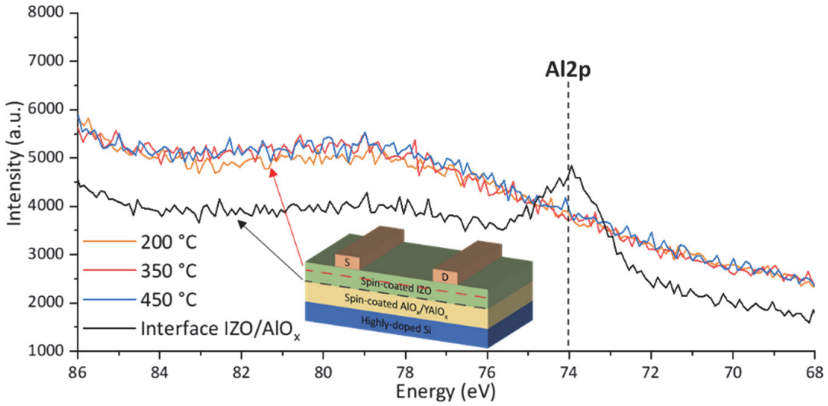


Figure 4.8 XPS spectra from the samples with spin-coated dielectric registered at ~74 eV. We can see an overlap between the In4p peak and the Al2p peak: as the percentages possibly involved are minimal, the Al peak is not visible in the IZO films cured at the various temperatures. Instead, it becomes more evident when the same analysis is performed at the semiconductor/dielectric interface where the Al fractions are higher, and the In signal is less predominant.

4.1.4 Results for IZO on ALD Al_2O_3 dielectric

Here are reported the results obtained from the IZO-TFTs manufactured with the ALD Al_2O_3 dielectric. Figure 4.9 depicts the transfer curves of the TFT cured following the different annealing protocols, while Table 4.3 reports the electrical performances per each type of device.

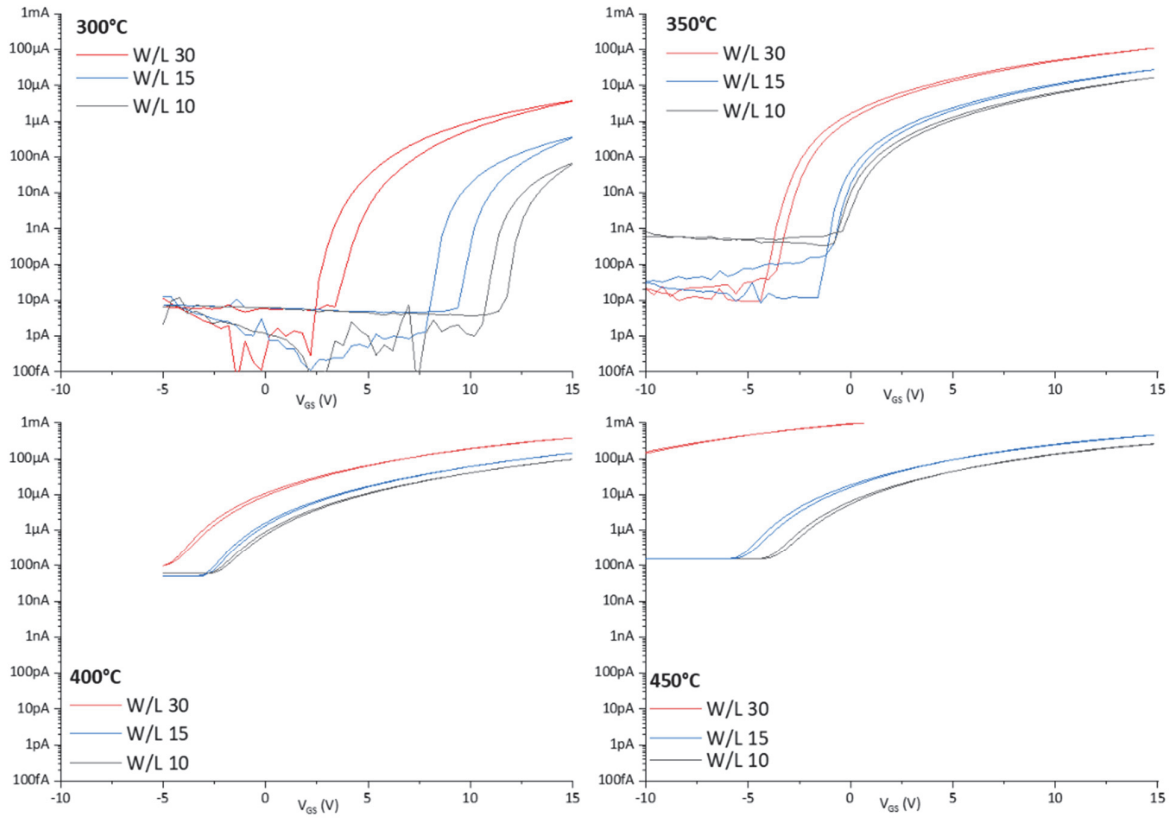


Figure 4.9 TFTs with spin-coated IZO and ALD dielectric. Representative transfer curves extracted from TFTs cured at different annealing temperatures from devices with variable W/L. The drain voltage V_{DS} used during the measurements was 15 V. The devices cured at 200°C and 250°C were not active.

As similarly occurred for the samples with sol-gel dielectric, the thermal annealing of the IZO at a temperature below 300 °C did not yield working devices. We saw how the increase in annealing temperature corresponded to an increase in the on-currents of the devices. The TFTs cured at 350 °C demonstrated the best switching characteristics with an I_{on}/I_{off} ratio of 3.5±5 × 10^6, low off-currents ~ 100 pA, and a threshold voltage of ~0.9 V. A further increase in temperature resulted in a degradation of the switching characteristics as the devices suffered from higher off-currents, over hundreds nA, and a marked shift of threshold voltage towards negative values. As discussed in the previous sub-section, this aspect could be correlated to the formation of oxygen vacancies at high temperatures, which increase the number of background charges in the film and also cause a degradation of the subthreshold swing, from 0.29±0.27 V/dec at 350 °C to 4.17±4.11 V/dec at 450 °C.

We excluded the effects of thermal treatments on the ALD Al_2O_3 dielectric, manufactured at 200 °C, as a possible cause of the different switching behavior of the TFTs at high temperatures. A previous study on Al_2O_3 deposited via ALD on Si reports that no significant changes, notably in thickness and capacitance, were observed in the layer after thermal treatment at 450 °C for 30 min.[199]

Table 4.3 Comparison of the electrical results for the TFTs with ALD dielectric and IZO cured at various temperatures.

	ALD Al_2O_3 300°C	**ALD Al_2O_3 350°C**	**ALD Al_2O_3 400°C**	**ALD Al_2O_3 450°C**
Mobility (cm^2/Vs)	0.03±0.02	0.56±0.13	2.10±0.70	4.17±0.80
On-current (A)	1.04±1.80 × 10^{-6}	4.00±4.30 × 10^{-5}	1.75±1.45 × 10^{-4}	1.10±1.30 × 10^{-3}
Off-current (A)	1.10±0.60 × 10^{-12}	1.10±1.90 × 10^{-10}	7.75±2.60 × 10^{-8}	6.20±8.10 × 10^{-7}
I_{on}/I_{off} ratio	1.15±1.23 × 10^5	3.50±5.00 × 10^6	2.30±0.14 × 10^4	2.10±0.70 × 10^4
SS (V/dec)	0.22±0.05	0.29±0.27	1.64±0.19	4.17±4.11
V_{Th} (V)	8.70±2.82	0.89±1.50	-5.40±10.5	-9.20±11.0

We have also analyzed the chemical composition of the IZO layer annealed at 350 °C to compare it with the analogous sample deposited on the solution-processed dielectric. From the O1s deconvolution in Figure 4.10, we observed a chemical composition consistent with the one measured from the fully solution-processed counterpart, suggesting that at 350 °C, MO_x composition does not depend on the nature of the layer onto which the precursor solution is deposited.

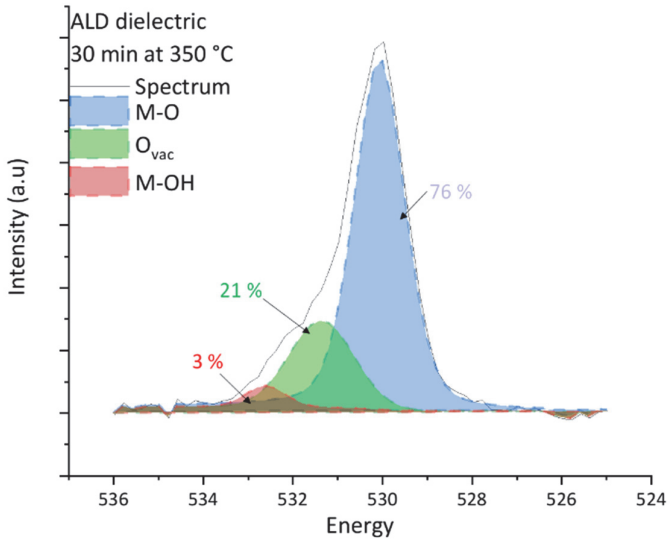


Figure 4.10 O1s curve of the IZO deposited on ALD Al2O3 with the relative deconvolution and the atomic fractions calculated, with a fitting parameter (χ^2) equal to 0.61. The values 76 %, 21 %, and 3 %, respectively M-O, O_{vac}, and M-OH, are comparable to those obtained from the IZO on spin-coated dielectric, cured with the same protocol: 78.3 %, 18.6 %, and 3.1 %.

4.1.5 Comparison and discussion

Here we summarize and discuss the results obtained for the IZO TFTs with solution-processed and ALD AlO_x-based dielectrics. We compared two AlO_x-based dielectrics fabricated with a standard vacuum process and via sol-gel processing to evaluate how the nature of the dielectric could influence the performances of the TFTs. Figure 4.11 depicts typical transfer curves obtained from the two types of MO_x stacks as a function of the annealing temperature of the IZO semiconductor layer.

From Figure 4.11a, we can see that samples with ALD dielectric yielded operative devices for IZO synthesis temperatures > 300 °C, showing increased mobility and higher on- and off- currents as the temperature raised from 300 °C to 450 °C. We also observed a threshold shift towards negative voltages combined with reduced switching capability, indicating increased film conductivity corresponding to excessive curing. Such behavior is coherent with the formation of oxygen vacancies, thermodynamically more favorable at high temperatures, which ultimately contribute to the number of background carriers available in the film.[197]

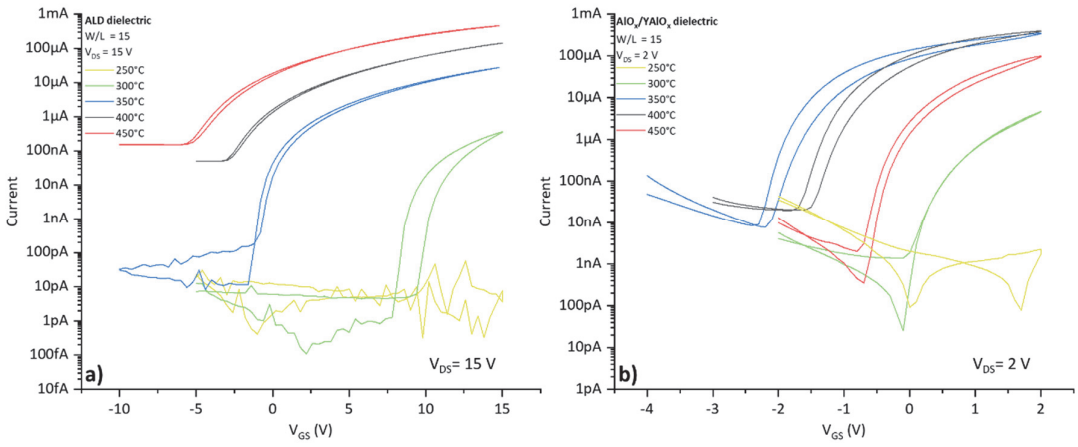


Figure 4.11 Comparison of transfer curves from devices cured at different temperatures: a) ALD dielectric and b) solution-processed dielectric.

From Figure 4.11b, we observed a similar trend for the sol-gel dielectric, where increased IZO annealing temperature resulted in enhanced on-currents and mobility. However, in contrast with what was measured with ALD dielectric, we noticed that the trend was not maintained in the whole tested temperature range. Figure 4.12, reporting a) the measured currents and b) the extracted TFT mobility as a function of the curing temperature, shows a change in this behavior from 400 °C to 450 °C. A positive shift of the transfer curves, combined with mobility and currents decrease at 450 °C, was noted. We attributed this electrical behavior to the reduced number of oxygen vacancies present in the IZO film, as shown in the deconvolution of the O1s peak obtained from the XPS analysis in Figure 4.5.

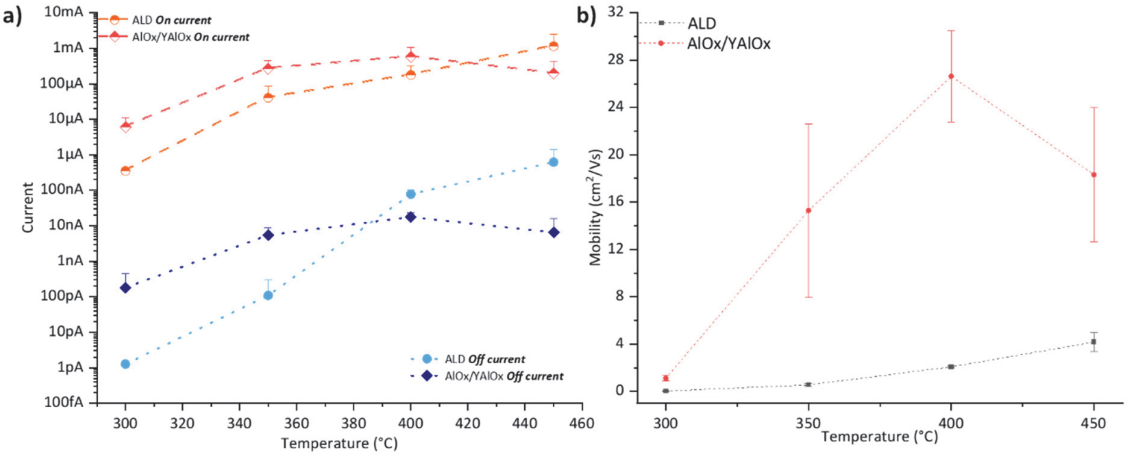


Figure 4.12 Comparison of the electrical characteristic between the two types of TFT. a) Depicts the tendency for on-current and off-current as a function of the annealing temperature. b) Shows the calculated mobility as a function of the temperature.

Despite a similar MO_x composition (at 350 °C), the samples cured with the same protocol showed different electrical behavior depending on the dielectric employed. Both types of TFTs demonstrated a good I_{on}/I_{off} ratio >10^5, but the fully solution-processed stack outperformed their ALD counterpart in terms of mobility, ~15 cm^2/Vs versus ~0.5 cm^2/Vs, and in terms of on-current levels, with an order of magnitude difference. This result suggests that the IZO semiconductor forms a better interface with the $AlO_x/YAlO_x$ dielectric than ALD Al_2O_3, facilitating the charge transport in the channel. A similar difference in performance was similarly reported by *Xu et al.* when they confronted TFTs with active stacks formed by solution-processed IZO/solution-processed AlO_x and solution-processed IZO/thermal SiO_2: they described devices, thermally treated at 300 °C, which yielded ~11 cm^2/Vs of mobility using AlO_x dielectric and ~0.5 cm^2/Vs with SiO_2 dielectric. They also hypothesized a reduced interfacial trap density for the fully solution-processed stack, demonstrating the formation of a better interface between the two solution-processed metal-oxides, which ultimately enabled the improvement in transistor performance.[145] The lower subthreshold swings obtained with the $AlO_x/YAlO_x$ dielectric suggest a lower interfacial trap density. Further investigations on the quality of the interface, such as capacitive measurements (C-V) at low-frequency on MOS capacitors for proper interface trap estimation, could be exploited to confirm this hypothesis. It would be interesting to analyze and compare the material composition of the two interfaces (IZO/ALD AlO_x versus IZO/spin-coated AlO_x) to shed more knowledge on the origin of the difference in interface quality.

The high off-currents and the lessened switching capabilities of the devices with ALD dielectric, annealed at 450 °C, suggest a high fraction of oxygen vacancies, which complies with the literature[189,190] but diverges from the results obtained from the devices, treated at 450 °C, with solution-processed dielectric (O_{vac} ~9 %). We considered a possible Al diffusion from the solution-processed dielectric in the IZO to explain the trend inversion for mobility and both on- and off-currents when going for a higher annealing temperature from 400 °C to 450 °C. Moreover, Al possesses a stronger oxygen affinity than In and Zn, acting as an oxygen getter, and could explain the small number of vacancies measured at 450 °C. As discussed in Chapter 3 for Al-doped IZO TFTs annealed at 400 °C, the doping of the IZO semiconductor with minor Al fractions (> 1 %) causes current level reduction and transfer curves shifts towards more positive voltages similar to those observed here. We tried to verify this hypothesis by exploiting the XPS analysis but with inconclusive results. Alternative types of analysis with higher sensitivity, such as secondary ion mass spectrometry (SIMS) and Auger electron spectroscopy (AES), would be necessary to characterize the small fractions possibly involved in this phenomenon and ultimately identify or not aluminum in the IZO semiconductor.

4.2 Manufacturing of TFTs with fully solution-processed MO_x active stack at high temperature

This section describes the process flow and the characterization of devices with fully-solution, processed MO_x active layers, treated via standard thermal annealing at high-temperature and realized exploiting photolithographic processes.

We used bottom gated TFTs that present both AlO_x/$YAlO_x$ dielectric and IZO semiconductor solution-processed and thermally cured. To better evaluate the performance of the MO_x layers and the electrical characteristics of the resulting TFTs, we implemented photolithographic steps, such as wet etching to pattern the IZO film and the use of a lift-off process for the electrodes that helped to reduce sources of leakage such as the unpatterned gate and semiconductor. The manufacturing process described hereafter is similar to the one used to fabricate the devices described in Chapter 5, addressing the low-temperature curing approach. We thoroughly characterized the resulting TFT electrical performances by combining capacitive measurements at low frequency (< 1 Hz) with I-V characteristics like the transfer and output curves. The TFTs yielded remarkable performances with I_{on}/I_{off} ratio > 10^8 and mobility exceeding 68 cm^2/Vs. We also evaluated the operational stability of the devices performing positive and negative bias stress tests, which resulted in minimal threshold voltage shifts. We looked at the microstructural nature and chemical composition of the sol-gel films, focusing on the IZO semiconductor, with transmission electron microscopy (TEM), XPS, and EDX. The nano diffraction analysis confirmed the amorphous nature of the deposited IZO.

Interestingly, from the curve fitting of the oxygen peak measured by XPS, we observed in the IZO unexpectedly low MO_x (~54 %) and high O_{vac} (~45 %) fractions, which do not match with the results reported in the previous section on the combination of IZO with different dielectrics (MO_x ~78 % O_{vac} ~18 %). We interpreted this relatively low MO_x and high vacancy fractions in the semiconductor as slight intermixing of dielectric and semiconductor films constituents, with Al interdiffusion and oxidation in the semiconductor when curing IZO at relatively high temperature. In the XPS spectrum, the oxygen peak from AlO_x overlaps with the one from oxygen vacancies, therefore adding up and resulting in the high vacancies values measured. We also observed the Al presence in IZO from the Al2s peak in the XPS performed on the samples. The following sections describe the process flow, the different characterizations performed, and the results obtained.

4.2.1 TFTs and test structure layouts

We employ a photolithographic process consisting of three steps involving three photomasks described in the following sections.

A schematic process flow is summarized in Figure 4.13a. The process involves the definition via lift-off of gate and capacitor bottom electrodes with the first photomask, “Gate mask”. After deposition and annealing of the active MO_x films, the semiconductor layer is patterned using the second photomask, “Semiconductor mask”, to maximize the TFT performance and avoid sources of leakage current. Finally, the top electrodes (source, drain, and capacitor top electrodes) are realized exploiting the patterns present in the third photomask, “S/D mask”. A cross-section of the final structure is provided in Figure 4.13b.

The cell unit, which is then replicated over 60 times on a 100 mm wide silicon wafer, includes many different bottom-gated TFTs and complementary structures, like inductors or capacitors, to characterize specific electrical aspects and better comprehend the origins of electrical behaviors in the TFTs. Figure 4.13c depicts a unit cell present on the mask layout. We will now describe the structures exploited to obtain the electrical characterization discussed in the following paragraphs.

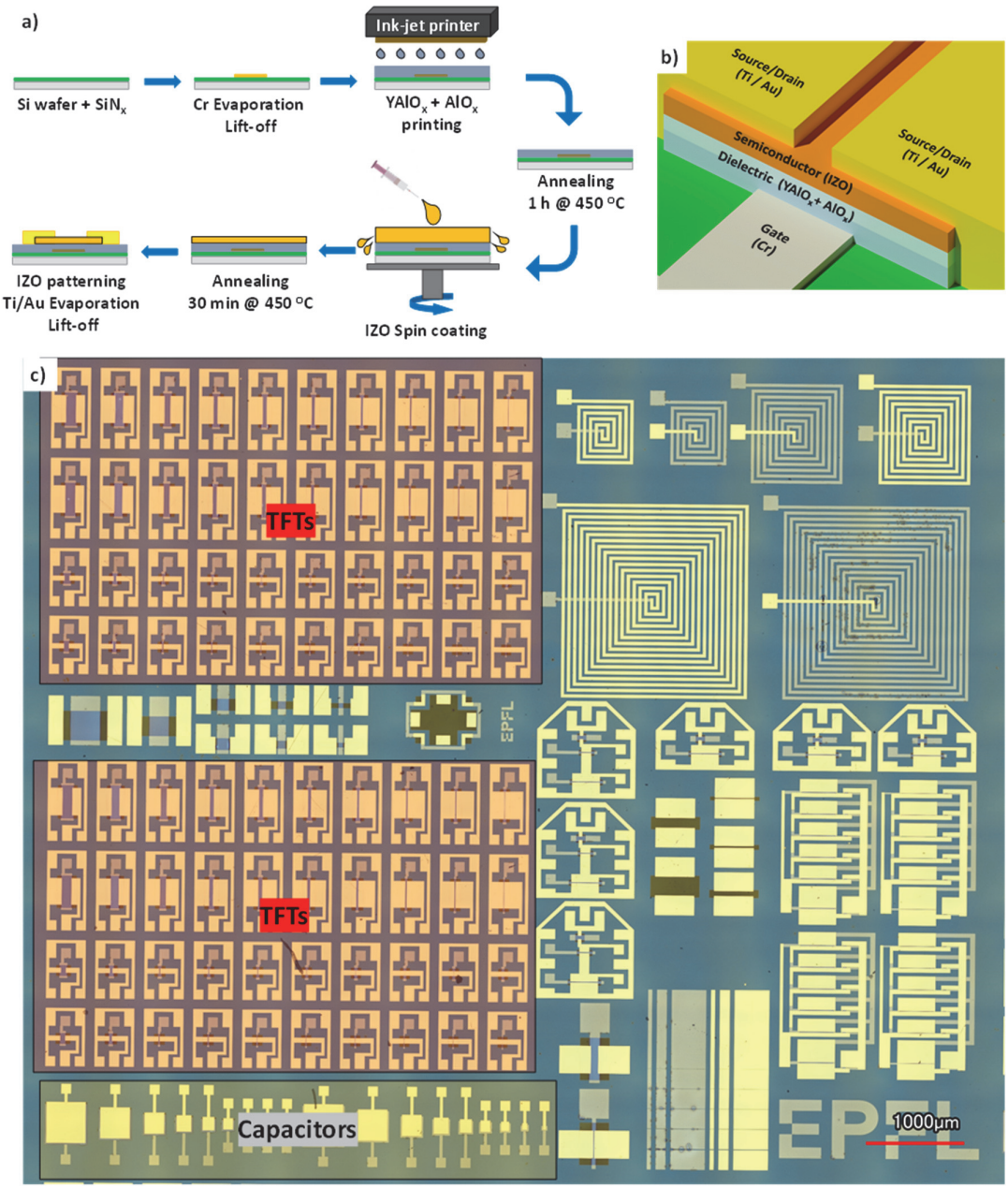


Figure 4.13 Layout and process flow of the photolithographically patterned structures. a) Schematic process flow and b) cross-section of the final stack. c) Optical image of the layout of a unit cell after fabrication.

4.2.1.1 TFTs and capacitors

Each unit cell includes 40 TFTs with different variations of the geometrical parameters, each of them repeated twice. In Figure 4.14, it can be seen that rows 1-2 and rows 3-4 maintains the same electrode width (W), 280 µm and 50 µm respectively, whereas, along the other axis, there is a variation of the channel length (L), with an increase from 5 µm to 100 µm from right to left. The difference between rows 1 and 3 to rows 2 and 4 is a different overlap between the source and drain electrodes with the gate, a parameter that influences the amount of parasitic capacitance and is particularly relevant for devices working at high frequency. The overlap between the gate and the source/drain electrodes is respectively 15 µm and 5 µm. The overlap is not a critical parameter for our TFTs fabricated here, but we characterize the TFTs with the smaller overlap of the two types available to place ourselves in the best conditions by limiting the parasitic capacitances.

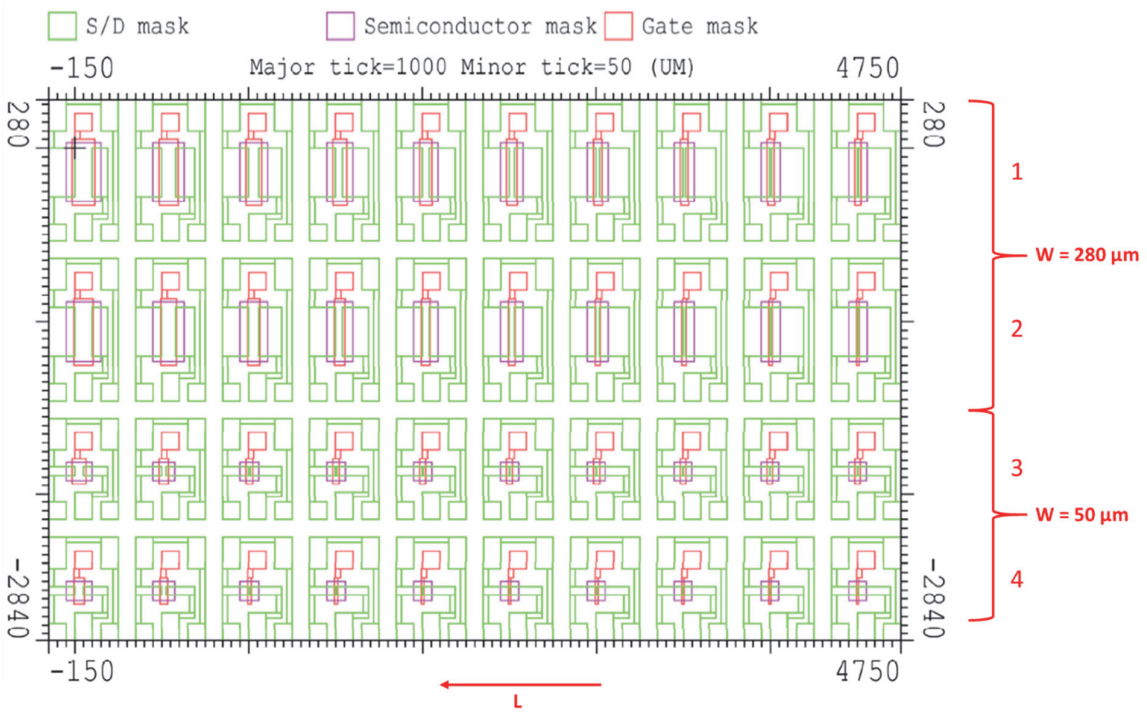


Figure 4.14 Digital file representing all the 40 different TFT types available in a unit cell. Here are reported all the designs contained in the layout of the three masks necessary to fabricate the TFTs.

The mask includes two types of parallel plate capacitive structures exploited for the active layers characterization: metal-insulator-metal (MIM) and metal-insulator-semiconductor-metal (MOS). We can evaluate the electrical performances of the gate dielectric layer performing C-V and C-f characterizations with the MIM structures. To better understand the operation and the characteristics of a TFT, the knowledge of the dielectric layer behavior is as necessary as the knowledge of the semiconductor film. Similar analysis can be performed with MOS structures to evaluate the quality of the semiconductor-dielectric system, for instance, by investigating the presence of traps at the interface, visible with C-V characteristics at low frequency. These analyses, beneficial to understand the behavior of the final devices, will be then discussed later from Section 4.2.5.3.

As for the TFTs, various geometries are available, as depicted in Figure 4.15, resulting in different capacitor areas ranging from 1.2×10^{-9} m^2 to 1.6×10^{-7} m^2.

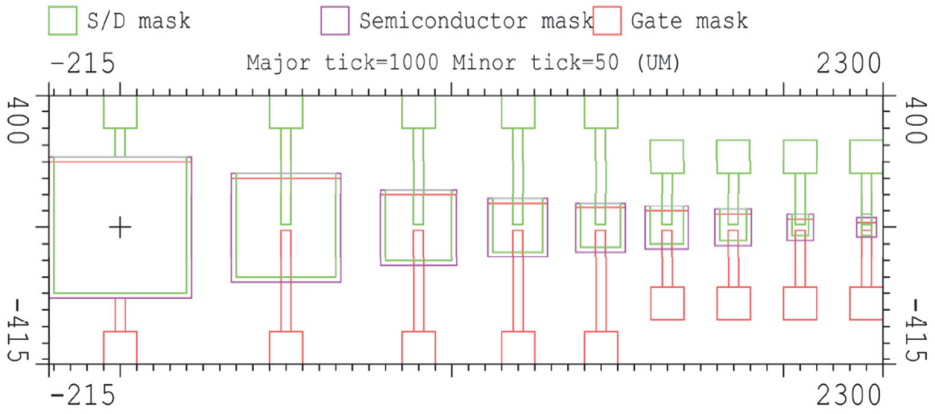


Figure 4.15 Digital file representing the dimensions of the different capacitors. Here are reported all the designs contained in the masks to fabricate the capacitors. The image depicts the MOS capacitors.

4.2.2 Process flow

The manufacturing process of these devices has been performed between the CMi cleanroom located in Lausanne for all the photolithographic processes and the Coating Competence Center (CCC) of EMPA in Dubendorf for the deposition and curing of the MO_x layers. The atmospheric conditions, temperature (T) and humidity (RH), are strictly controlled in these two environments and do not experience particular fluctuations. (CMi: RH: 38-48 %, T: 21±2 °C; CCC: RH: 35±10 %, T: 22±2 °C)

As a substrate, we utilized 100 mm wide, 525 µm-thick Si wafers coated with a low-pressure chemical vapor deposition (LPCVD) low-stress silicon nitride layer of 100 nm acting as a buffer insulating layer.

4.2.2.1 Gate electrode deposition and patterning

We utilized a 35 nm-thick chromium layer, deposited via e-beam and patterned via photolithography and lift-off to form contemporary gate and capacitor bottom electrodes.

The digital file shown in Figure 4.16 represents the first lithographic mask used to pattern the gate electrodes of the TFT structures.

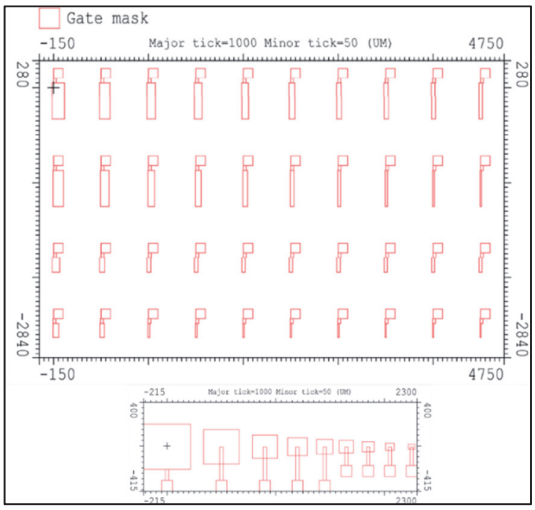


Figure 4.16 Section of a digital file, referred to the TFT and capacitive structures, exploited to fabricate the gate mask.

The photolithographic process is based on a bi-layer lift-off technique available at CMi. After quick preliminary dehydration at 120 °C, the two resists are spun and baked (190 °C for 250 s and 100 °C for 90 s respectively) sequentially. The first resist (LOR from *Microchem*) is not photosensitive, unlike the second one (AZ 1512 from *Microchem*). The stacked resists are then exposed to UV light through a photolithographic mask. During the development, the top layer behaves as a standard positive-tone photoresist, while the underlying LOR film can be isotropically dissolved in the developer, creating an undercut of a few hundred nanometers by controlling the development time.

The steps involved are the following and represented in Figure 4.17:

1. Substrate coating with a double layer photoresist (LOR + AZ 1512), exposure to UV light, and development;
2. Chromium evaporation via e-beam using the *Alliance-Concept EVA 760* evaporator;
3. Resist stripping, obtained by immersing the wafers in a remover solution (Remover 1165 from *Dow*) to reveal the patterned layers.

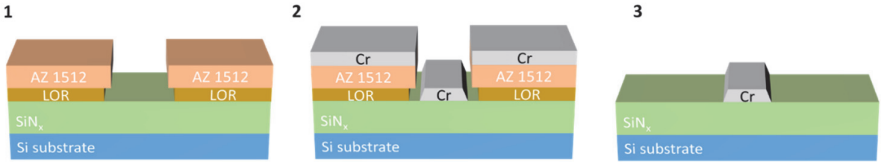


Figure 4.17 Schematic of the double layer lift-off process used to pattern the chromium gate electrodes.

4.2.2.2 Dielectric deposition and synthesis

The dielectric layer was deposited via printing at Empa with the collaboration of Dr. Sami Bolat. We utilized an $AlO_x/YAlO_x$ dielectric stack like the one presented in the previous section. The ink viscosity was adapted to match the rheological requirements of the printer and ensure stable jetting. For this purpose, we implemented a mixture of solvents, 50 % 2ME / 50 % Ethylene Glycol.

We employed a *Meyer Burger* PixDRO LP50 inkjet printer equipped with ten pL *Dimatix* DMP cartridges. Before the deposition, we performed O_2 plasma treatment for 5 min (225 W, 13.56 MHz) to improve the solution wettability. Then, the two dielectric layers have been printed sequentially deposited with a printing resolution of 300 DPI and 400 DPI[21], respectively. Between the two depositions, the samples are subjected to a drying step on the hot plate (temperature ramping from 75 °C to 200 °C, then plateau at 200 °C for 1 min) and a short plasma treatment (1 min at 225 W, 13.56 MHz). After the printing, the layers are dried on the hot plate for 1 hour at 200 °C under ambient atmosphere, and then ultimately annealed at 450 °C for 1 hour to ensure the MO_x synthesis.

4.2.2.3 Semiconductor deposition, synthesis, and patterning

The semiconductor was deposited via spin-coating using the same semiconductor solution described before in Section 4.1.1.2: IZO 0,2 M in 2ME. Before the deposition, a 10 min DUV treatment (low-pressure mercury lamp UV253HR from *Filgen*; output power intensity of 25–28 mW/cm^2) was performed to improve the layer wettability, then we spin-coated the solution as previously described (2000 rpm for 30 seconds). We implemented two spin-coated layers[22] with intermediate drying between the depositions (3 min on a hot plate at 150 °C + 3 min DUV treatment [23]. Afterward, the layers are first dried on the hot plate for 1 hour at 150 °C in air condition, then sintered at 350 °C for 30 min on the same tool. We selected 350 °C as in the previous Section 4.1 since it showed a good trade-off between mobility and switching performance for both types of dielectric employed.

The day after the deposition, the wafers were processed in the cleanroom at CMi to pattern the semiconductor channels via wet etching. First, the channel areas are covered with AZ 1512 patterned using a standard photolithographic process, then the samples are dipped into a 0,12 M hydrochloric acid solution for less than 60 sec to perform the etching, and finally, the resist is stripped away in the remover solution. This patterning step also involves the semiconductor structures included in the MOS capacitors. Figure 4.18 shows the wet etching process performed.

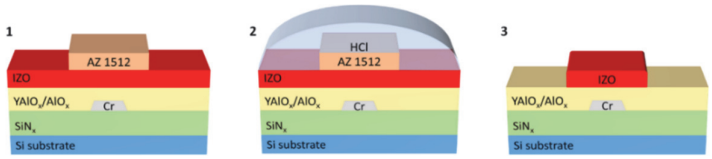


Figure 4.18 Schematic description of the wet etching process necessary to pattern the IZO structures.1) Photoresist deposition and patterning, followed in 2) by the wet etching in HCl and resist stripping in 3), which releases the patterned IZO structures.

Here is presented the digital file representing the second lithographic mask used to pattern the semiconductor channel (Figure 4.19).

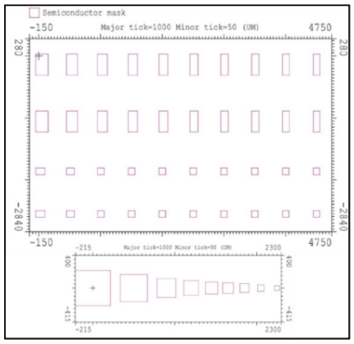


Figure 4.19 Section of the digital mask file, referred to the TFT and MOS structures, exploited to pattern the semiconductor channel.

[21] DPI= Drops per inch.

[22] We performed a two layer deposition to avoid inhomogeneities in the final layer.

[23] DUV exposure improves the wettability as similarly done by O_2 plasma. However, DUV is preferred for the surface treatment of semiconductor layers to not alter the characteristics of the films.

4.2.2.4 Source and drain electrodes deposition and patterning

We employed a double metal layer composed of titanium for better adhesion and gold, respectively 10 nm and 70 nm, to form source and drain electrodes for the TFTs and the top electrodes for the capacitors. We exploited the same process described for the gate electrodes for patterning the structures. The metal deposition was carried out via e-beam using the EVA 760.

The digital file shown below represents the last lithographic mask used to pattern the top capacitor electrodes and source/drain electrodes (Figure 4.20).

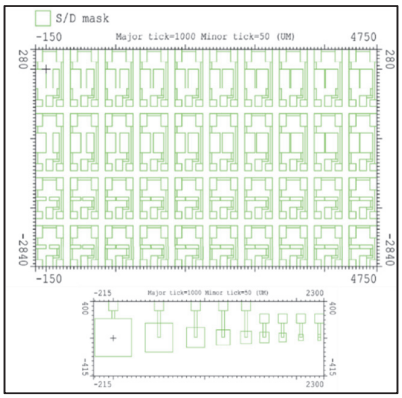


Figure 4.20 Section of a digital file, referred to the TFT and capacitive structures, exploited to pattern the source/drain and top electrodes.

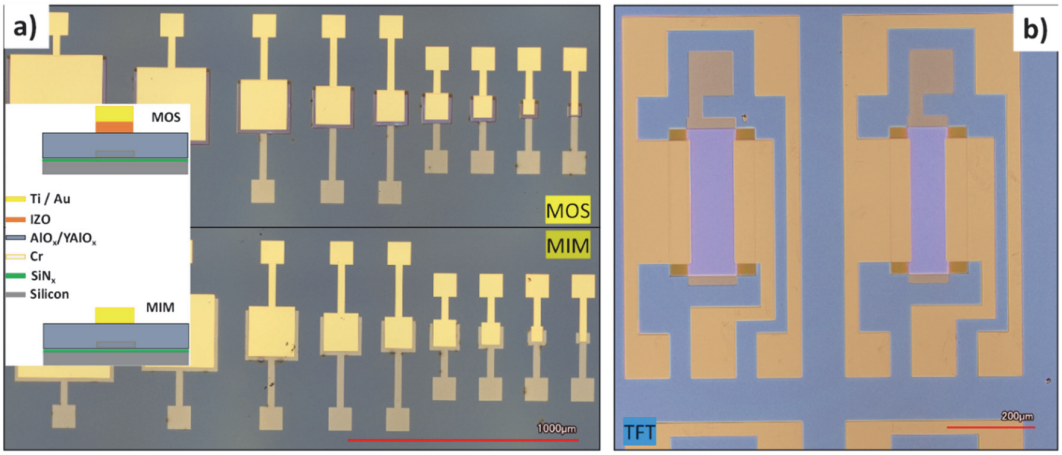


Figure 4.21 Optical image of the a) MIM and MOS capacitors and relative cross-sections, and b) TFTs.

4.2.3 Material characterization

We investigated the morphology and chemical composition of the manufactured TFT devices from the morphological point of view to the composition of the deposited MO_X films.

We studied the cross-section of a TFT exploiting high-resolution transmission electron microscopy (TEM) imaging. We confirmed the thickness of all the deposited layers, observed the interfaces between the active layers, and evaluated the crystallinity of the IZO with a punctual nano diffraction technique. We also analyzed, in scanning TEM mode, the composition of all layers via energy-dispersive X-ray spectroscopy (EDX).

We verified the synthesis of the IZO at 350 °C for 30 min by in-depth XPS, which provides a semiquantitative analysis of the materials present in the films and the type of bonds involved. Combining the XPS with ion milling, we performed analysis over the entire thickness of the device: as a result, we obtained the profile of the different elements contained in the TFT.

We will now discuss in detail the results obtained from the characterizations performed.

4.2.3.1 Transmission electron microscopy

Transmission electron microscopy is an imaging technique that exploits a beam of electrons transmitted through a specimen to compose an image. It is a high-resolution technique that can resolve structures in tens of nm and operate in different modes, such as scanning mode and diffraction imaging.

The sample preparation is a fundamental step as it has to be less than 100 nm thick to allow the electrons to pass through: the specimen, called "lamella", is prepared by a focus ion beam (FIB). First, the selected area is covered with a protective carbon layer, then the material around the area is removed via ion milling, as shown in Figure 4.22a and Figure 4.22b. Afterward, the unpolished lamella is extracted and attached to the TEM sample-holder via carbon deposition. Ultimately, the lamella is thinned with the FIB to reach the desired thickness. (Figure 4.22c)

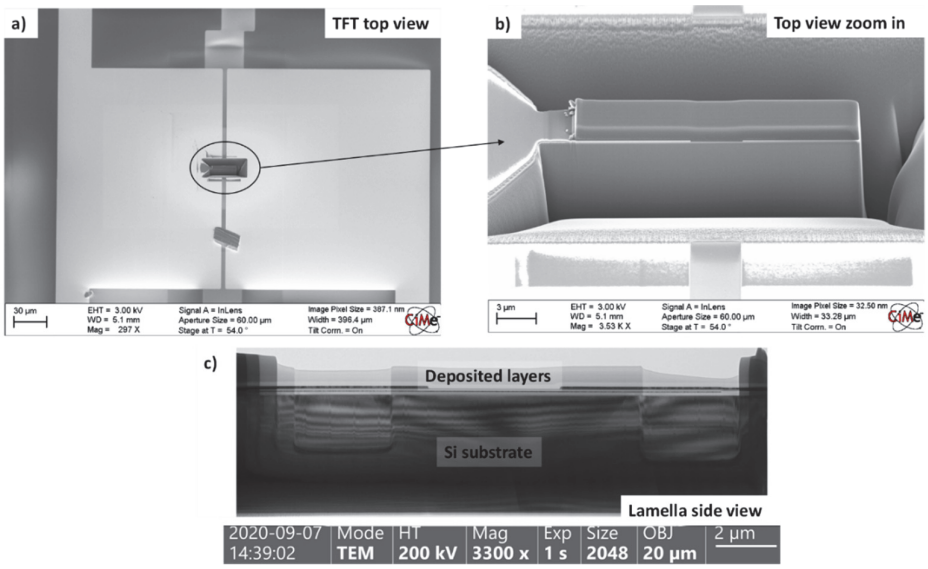


Figure 4.22 Lamella preparation. a) Location selected for the lamella and b) a close-up image of the process. c) Depicts the final lamella already fixed to the holder.

Dr. Lucie Navratilova of the Interdisciplinary Centre for Electron Microscopy of EPFL (CIME) performed the lamella preparation. Dr. Victor Boureau operated the TEM and gathered the images. TEM imaging and scanning TEM (STEM) cross-section analyses were performed using a FEI Talos F200S, operated at 200 kV.

We measured the thickness of all the layers deposited from different positions in the TEM cross-section (Figure 4.23a). We characterized the crystallinity of the IZO cured at 350 °C for 30 min: as depicted in Figure 4.23b, we exploited a nano diffraction technique to measure the structural order of the IZO locally, confirming that the semiconducting oxide is in an amorphous phase.

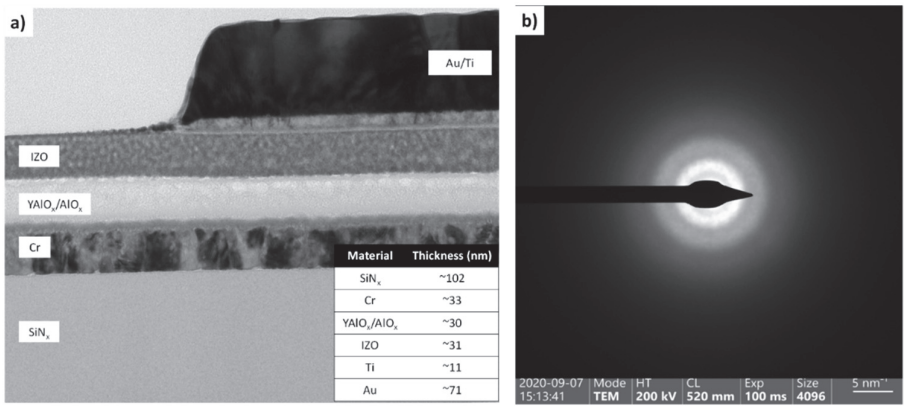


Figure 4.23 a) High-resolution TEM image of the TFT cross-section. b) Diffraction pattern of the IZO film, which does not show signs of crystalline orientation.

An EDX hyperspectral mapping was performed in STEM mode to investigate the chemical composition of the films. The technique measures the X-ray spectrum and identifies the sample composition with a sensitivity of 0.5-1 at%.[200] Analyzing the active layers using a high-resolution HAADF[24] image (Figure 4.24a), we observed the interdiffusion between the IZO and AlO_x/$YAlO_x$ films, highlighted in the red box. The thickness of this region was estimated to be approximately 10 nm, where a continuous transition in the atomic concentration of the chemical elements involved: Al, In, and Zn (Figure 4.24b). This swift interfacial transition is ultimately desirable to achieve performing TFTs with small SS.

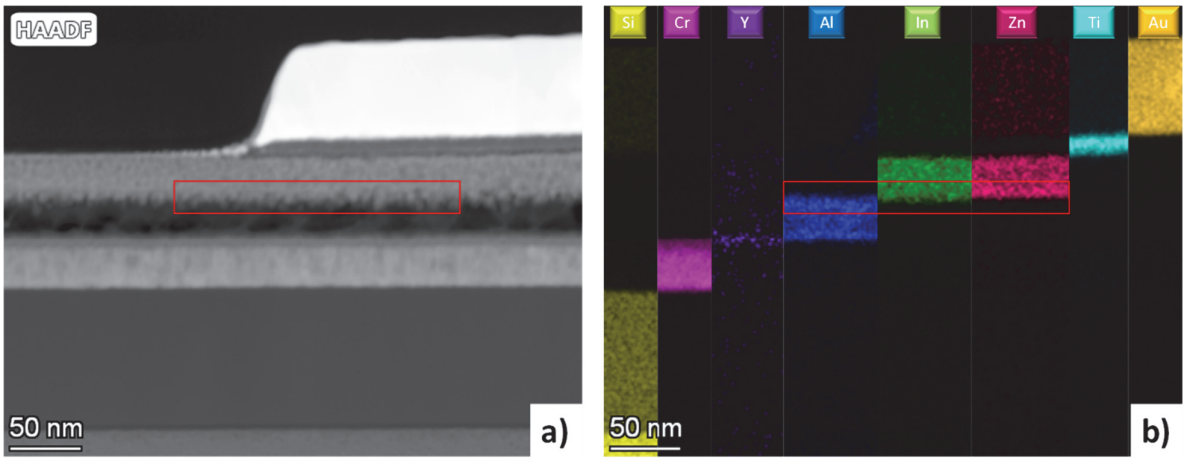


Figure 4.24 STEM pictures of the cross-section. a) High-resolution HAADF image of the cross-section. b) Chemical elements distribution in the layers obtained via EDX.

The analysis of the interface composition in Figure 4.25 and of the material distribution profile exposed two phenomena, indicated from the pink and blue arrows in Figure 4.25b:

1. There is a pile-up of Zn at the interface. It signifies that indium ions can diffuse more easily into the aluminum oxide dielectric than zinc. This analysis shows the excellent material match between the indium-based semiconductor and aluminum-based dielectric, resulting in a high-quality interface.
2. There is a non-zero signal from the aluminum in the IZO. This signal of ~1.5 % in the atomic fraction can indicate an aluminum diffusion into the IZO layer. This phenomenon needs to be confirmed from other analyses as the value measured is close to the detection limit of the system (~0.5-1 %).[200]

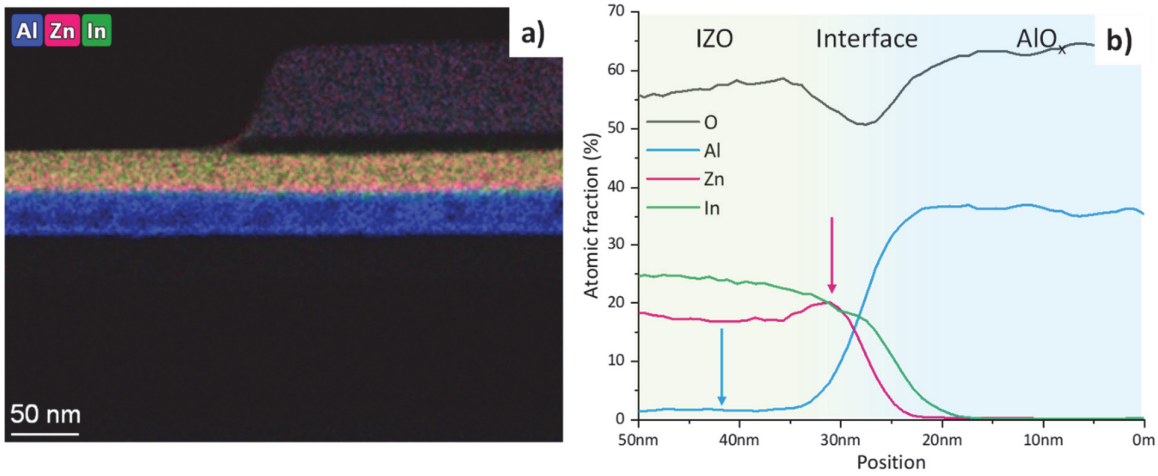


Figure 4.25 Chemical analysis of the active layers with a) HAADF image and b) relative atomic fraction profile.

[24] HAADF = High-angle annular dark-field.

4.2.3.2 XPS

We performed an in-depth XPS analysis on the samples to evaluate the chemical composition of the deposited film and the quality of the semiconductor layer.

We confirmed a proper MO_x conversion as there is a minimal signal (< 2 %) from nitrogen and carbon, respectively, signs of unconverted precursors and trapped solvent. (Figure 4.26)

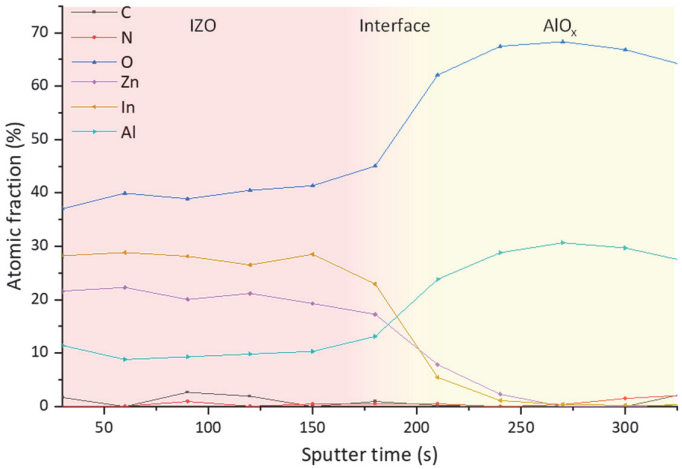


Figure 4.26 Profile of the chemical composition extracted from the in-depth XPS measurements.

Figure 4.27 depicts the curve fitting from the spectrum of the O1s curve, extracted from the bulk of the IZO layer, measured during the in-depth analysis.

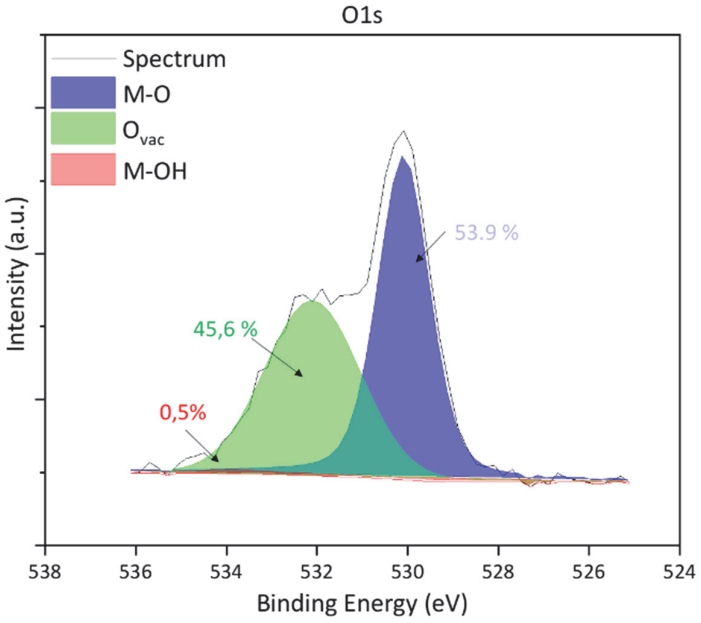


Figure 4.27 O1s deconvolution obtained from the bulk of the IZO layer, with a fitting parameter (χ^2) equal to 0.65.

We analyzed the total signal and processed it using the PHI Multipak software. We could quantify the three contributions as follows:

- M–O (530.06 eV) = **53.9 %**;
- O_{vac} (532.07 eV) = **45.6 %**;
- M–OH (533.8 eV) = **0.5 %**.

From the data analysis, two aspects attracted our attention: the composition of oxygen peak obtained from the curve fitting and the O_{vac} peak positioning.

We noticed a low percentage of covalent bonds (~54 %) for a thermally cured IZO layer compared to the ones observed in the previous Section 4.1 (~ 78 %). Moreover, the surprisingly high vacancy fraction ($\gtrsim$ 45 %) may identify a not fully converted MO_x layer with a high number of defects. However, this hypothesis contradicts the evidence of low carbon and nitrogen residuals in the film, visible in Figure 4.26.

We also observed a shift (~0.8 eV) in the O_{vac} peak at ~531.2 eV. We excluded it as an artifact relative to the deconvolution process as the fitting parameter (χ^2) shows almost a perfect match χ^2=0.65.

An alternative explanation for the unexpected results needs to be found elsewhere. From the elemental analysis of the IZO film, as shown in Figure 4.28, we detected a signal at ~74 eV associated with aluminum in the film. Unfortunately, as already discussed in the previous Section 4.1, precise quantification is impossible as the Al2p signal overlaps with the In4p located at ~78 eV. As we calculate the atomic fraction from the integral of the area below the curve, the value of ~10 % obtained from the XPS and visible in the profile shown in Figure 4.28 is overestimated.

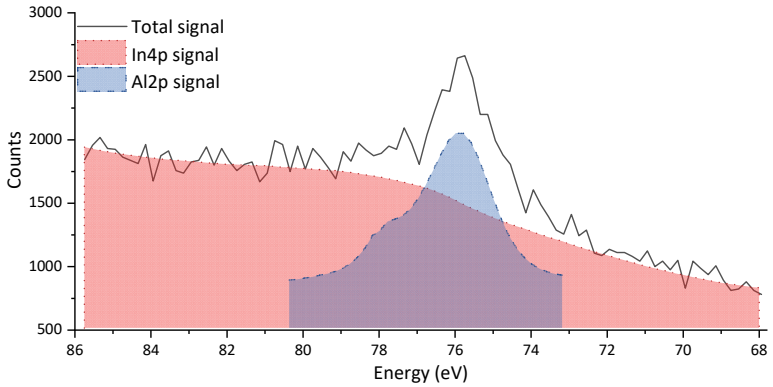


Figure 4.28 The total signal registered around 75 eV. The signal can be deconvoluted in two contributions related to the In4p located at 78 eV characterized from a large FWHM and the Al2p located at ~75 eV.

The presence of Al explains the elevated signal measured at ~531.9 eV in Figure 4.29 since the O1s spectrum emitted from an AlO_x compound generally presents a peak between 531 eV and 532 eV.[192] From the Al2p and O1s signals profiles, depicted in Figure 4.29, we can notice how the relatively small signals attributed to AlO_x and Al present throughout the whole depth of the IZO layer and increase without significant energy shifts once they reach the dielectric layer. Therefore, we can now attribute the significant signal measured at ~531.9 eV as a combination of O_{vac} and AlO_x.

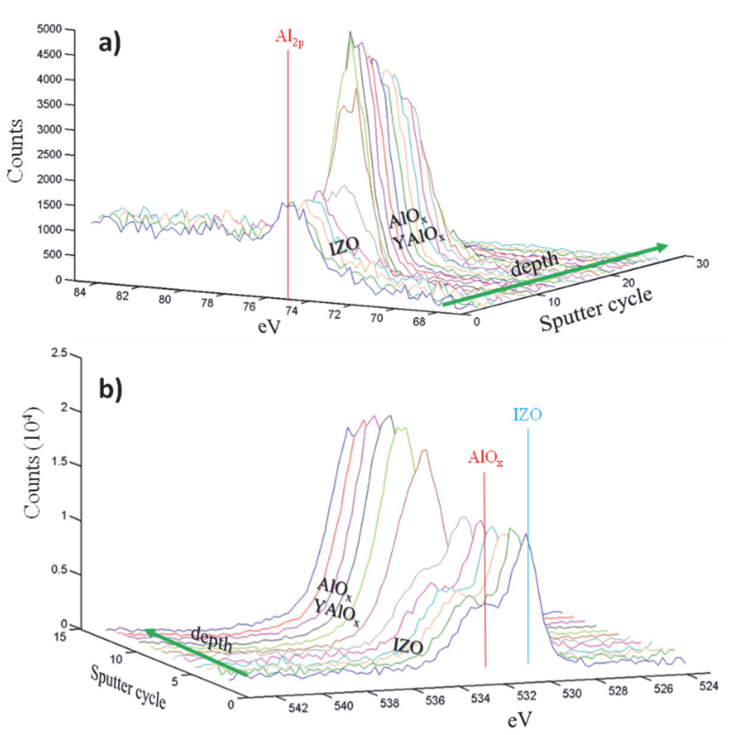


Figure 4.29 Profile distribution of a) Al and b) O1s over the whole active layers thicknesses.

We successively repeated the XPS measurements to confirm the initial measurements. We observed the same Al signal previously described from the surface analysis gathered in a different sample spot, confirming that the original readings were not caused by artifacts or possible dielectric pinholes in the semiconductor.

We can summarize the results obtained from the chemical analysis of the IZO films as follows:

- Results from XPS data regarding Al signal and O1s curve fitting suggest a minimal Al doping inside the whole thickness of the IZO. Due to signal overlap in the Al and In spectra, we cannot correctly estimate the entity of this phenomenon. We repeated the measurement twice and verified that the readings were correct.
- The compositional analysis performed via EDX confirms the presence of ~ 1.5 at% over the thickness of the IZO layer. However, since the value is close to the resolution limit of the technique (0.5-1 %), we cannot exclude that the reading is affected by artifacts.

We will now discuss the electrical characteristics extracted from the transistors and from the capacitor structures.

4.2.4 TFT characterization

We extracted various sets of I-V characteristics from the realized TFT devices to evaluate their electrical performances. Exploiting semiconductor parameter analyzers such as the *Keithley 4200A-SCS Parameter Analyzer and the HP 4155,* we measured the output and transfer characteristics of the devices and extracted the figures of merit. Then we evaluated the operational stability and durability of the TFT by performing bias stress tests and confronting their electrical performance one year after their manufacturing. The results about the operational stability are discussed in Section 4.2.6.1.

Among the available TFT geometries, we characterized those with a W = 280 µm and a channel length L = 100 µm, resulting in a W/L= 2.8, the smallest W/L available in our layout. Figure 4.30 depicts the typical transfer and output characteristics obtained from the measured TFTs.

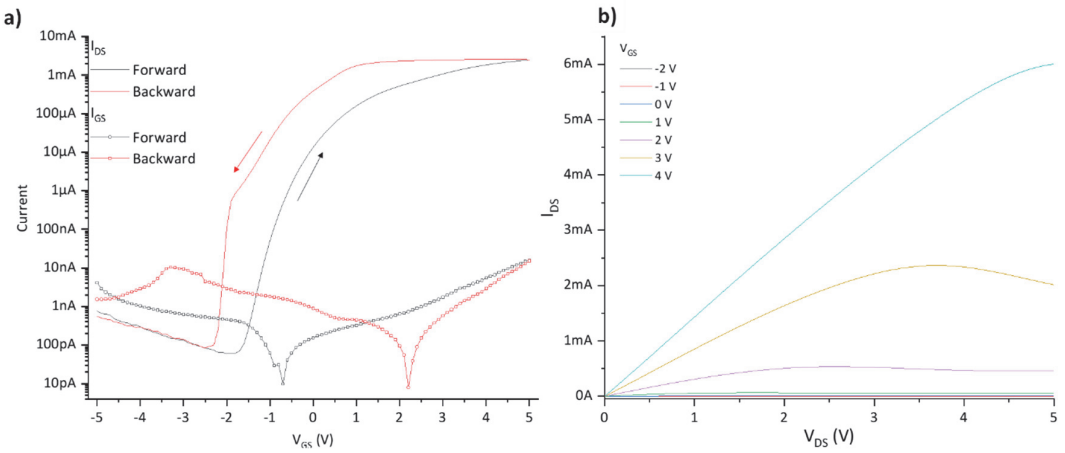


Figure 4.30 Typical a) transfer and b) output characteristics measured from the TFTs. The voltage applied during the measurement of the transfer characteristics was V_{DS} = 1.5 V.

The transistors exhibited remarkable electrical performances, such as an exceptional mobility ~70 cm^2/Vs, with a threshold voltage ~0.6 V and an extremely high I_{on}/I_{off} ratio >10^9. The mobility was extracted using the dielectric constant evaluated with low-frequency capacitive measures described in Section 4.2.5.1. We observed a slight dependence of the saturation current from the applied drain voltage from the output characteristics. Such behavior could be correlated to movable ions inside the dielectric film the ions trapped in the dielectric,[201,202] aspect discussed in Section 4.2.5. We confirmed the quality of the interface and the material matching between dielectric and semiconductor, reporting low subthreshold swing values < 200 mV/dec. We measured the TFT characteristics from different wafer positions: the consistency in the electrical behavior, as visible in Figure 4.31, demonstrates the uniformity of the layers over the sample area. These electrical characteristics align with state-of-the-art TFTs with vacuum-processed IGZO with mobilities over 70 cm^2/Vs and I_{on}/I_{off} ratio > 10^9.[20,203]

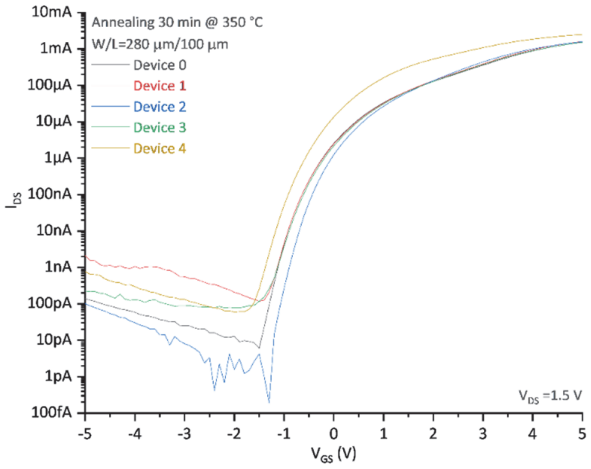


Figure 4.31 Transfer curves obtained from several devices. (n=5)

We can observe a small counter-clockwise hysteresis from the transfer characteristics (Figure 4.30a), typical of the devices containing solution-processed AlO_x dielectrics and probably due to some adsorbed moisture from the dielectric, as discussed previously. We calculated the hysteresis as the difference in threshold voltages for the forward and backward sweeps. The TFTs did not suffer from severe hysteretic instability as the hysteresis calculated was below 0.7 V, which can be considered acceptable. Table 4.4 summarizes the statistics regarding the electrical performances calculated from the TFTs.

Table 4.4 Summary of the figure of merit extracted from the electrical characteristics of the devices. We obtained the statistics from n≥5 TFTs.

μ (cm^2/Vs)	V_{Th} (V)	I_{on}/I_{off} ratio	S.S (mV/dec)	Hysteresis (V)
68.2±3.48	0.61±0.46	1.49±3.35 × 10^9	180±60	0.67±0.16

4.2.5 Dielectric characterization

To better understand the electrical behavior of the realized TFTs and properly characterize them, we performed C-V capacitive and I-V measurements on the MIMs and MOS present on the wafer.

We investigated the electrical performances of the deposited dielectric and its behavior as a function of the measurement frequency. As discussed in Section 2.5, the solution-processed dielectric may suffer from instability related to frequency dispersion. The possible presence of movable ions could influence the electrical performances of the devices with possible ion injections, pseudocapacitance phenomena, or causing hysteresis.[147,151] Measurements were carried out at different frequencies, reaching low frequency (< 1 Hz) and emulating the DC conditions for extracting the output and transfer characteristics. Moreover, some slow trapping and de-trapping phenomena are visible only at low-frequency. Properly evaluating the capacitance at low frequency is necessary to assess the TFT performance better and calculate the mobility value correctly. From the extracted capacitance, knowing the thickness of the gate dielectric film and the capacitor area, we calculated its dielectric constant using Equation 2.2.

We performed the low-frequency capacitive measurements with a *Keithley 4200A-SCS Parameter Analyzer* exploiting the "Very Low Frequency C-V Technique" (VLF C-V) included in the machine. The system allows the measurement of capacitances between 1 pF and 10 nF, in a frequency range from 10 Hz down to 10 mHz. The system models the tested device as a capacitor with a resistor in parallel, where the parallel resistance is mainly regulated from the leakage current. The leakage strongly influences the measurement quality as the additional DC signal modifies the accuracy of the readings. Figure 4.32 shows the measure working principle. To overcome the measurement reliability problem, the manufacturer provides the accuracy range for the measurements as a function of the current level measured and the dissipation factor D[25], automatically calculated from the system.[204] We respected these guidelines to evaluate the accuracy of our measurements. All the graphs shown in the following sections met the reliability criteria.

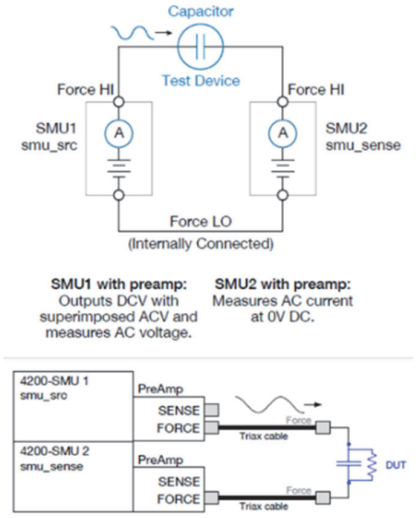


Figure 4.32 VLF C-V measurement working principle. Adapted from [204].

4.2.5.1 Low-frequency C-f measurement

As mentioned above, we characterized the dielectric layer performing VLF C-V analysis on MIM capacitors. We exploited the capacitors with the smallest area: 30x40 μm^2 and 50x50 μm^2 to minimize leakage interference with the measurements. We measured the capacitance values of the MIMs while sweeping the applied frequency from 10 Hz to 10 mHz. From this analysis performed on n>5 devices, we extracted a dielectric constant for the printed $AlO_x/YAlO_x$ cured at 450 °C of 32.8, measured at 10 mHz. We can use this value to precisely estimate the carrier mobility of the TFTs, mitigating overestimations related to capacitance miscalculations. Figure 4.33 depicts the calculated dielectric constant of the printed $AlO_x/YAlO_x$ dielectric, cured at 450 °C, as a function of the frequency. The dielectric constant shows a slight variation as a function of the frequency. The dependence of the dielectric constant from the whole range of frequency tested will be further discussed in the following sections.

[25] D = Reactance/Resistance = $1/\omega RC = 1/2\pi fRC$

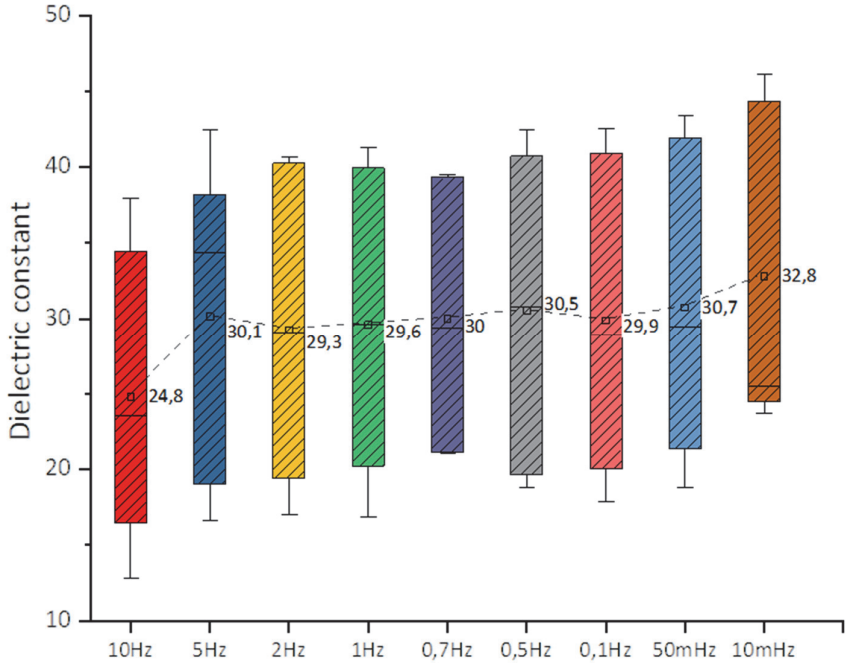


Figure 4.33 Box plot of the dielectric constant values calculated from VLF C-V measurements at 0 V. The dotted line connects the mean values, also numerically reported on the right of the relative bar. We obtained the statistics from a minimum of n>5 devices.

The VLF measures are not reliable when the leakage current between the electrodes increases. The accuracy of the measurements is high (< 3% error) when the current measured remains in the range between 100 pA to 1 nA. However, as visible in Figure 4.34a, increasing the applied voltage over 1 V can produce leakage currents of a magnitude comparable with the measuring range, thus increasing the dissipation factor and resulting in unreliable results. Figure 4.34b shows the typical curve obtained when we performed a C-V measure at low frequency with MIMs: the capacitance that should not depend on the voltage applied decreases in correspondence an increase of voltage and D factor. It was impossible to mitigate this artifact during measures, thus preventing reliable results with this approach.

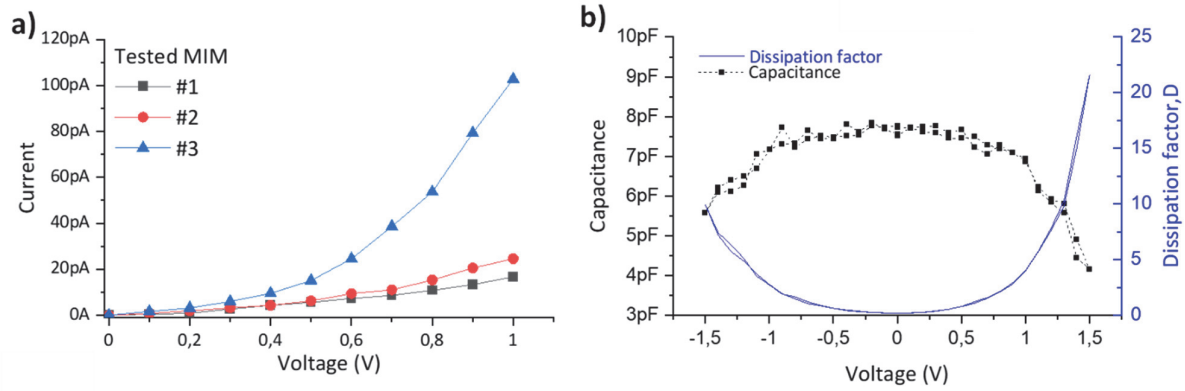


Figure 4.34 VLF analysis limits. a) typical I-V leakage curves obtained from 30x40 µm MIM. b) Capacitance measure at 0.1 Hz: the dissipation factor grows as a function of the applied voltage due to the increase of leakage currents.

To overcome the limitation, we decided to perform the C-V measurements at a low frequency on the MOS structures that are less affected by the parasitic currents. The results are presented in Section 4.2.5.3 regarding the C-V.

4.2.5.2 Medium-high frequency C-f measurement

For the medium-high frequency C-f measurements, between 100 Hz and 1 MHz, we employed a precision LCR meter (*Agilent E4980*). In Figure 4.35 is reported the variation of the measured dielectric constant for frequency varying between 100 Hz and 1 MHz. We could observe the typical trend of a high-k gate dielectric,[137] with an initial increase from 1 MHz (~10.5) to 100kHz (~13.4), then stabilization at lower frequencies around 13-14.

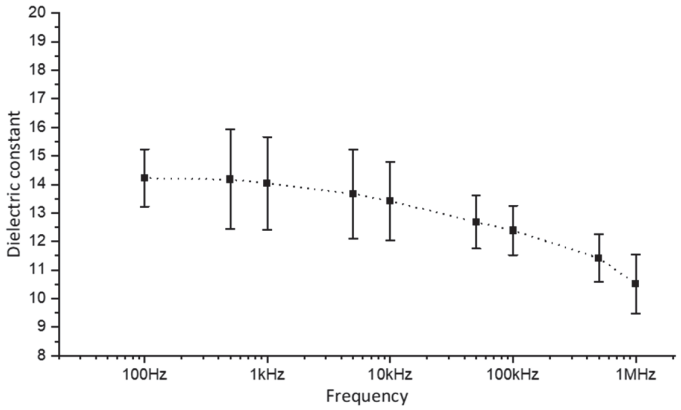


Figure 4.35 Dielectric constant variation at medium-high frequencies.

Ultimately, we report in Figure 4.36 the calculated dielectric constant as a function of the frequency in the range 0.01 Hz to 1 MHz. The dielectric constant shows a slight variation as a function of the frequency, as the value measured at 10 mHz is approximately two times higher than the one measured at kHz levels. Even if frequency dependence is not desirable, an increase of a factor two is still low compared to other solution-processed AlO_x-based dielectrics reported in the literature with factor ten.[97,205] We suspect that this behavior could be related to a small number of hydroxides probably adsorbed from the dielectric layer during the processing, as suggested in previous works.[147] Pieces of evidence of the possible presence of such slow polar molecules trapped in the gate dielectric are discussed in the next paragraph.

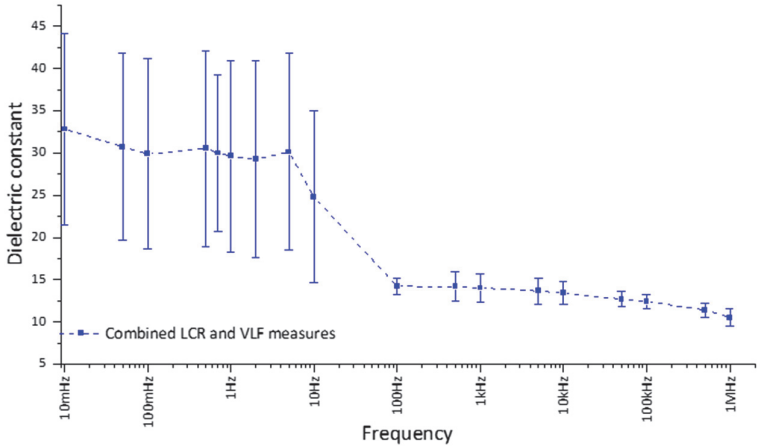


Figure 4.36 The dielectric constant of the printed $YAlO_x/AlO_x$ dielectric as a function of the frequency over the whole range measured from 0.01 Hz to 1MHz (C-f).

4.2.5.3 Capacitance-voltage characterization

Another type of structure that can be studied to evaluate the TFT performance is the MOS capacitor. It is a sandwich structure, depicted in Figure 4.21, formed by the active layers between two electrodes, exploited to evaluate the electrical behavior of a combination of both metal-oxide active layers. Capacitance-voltage curves are obtained by applying a bias voltage to the capacitor. Since it contains a semiconductor working in accumulation mode, it increases its total capacitance until the flat band condition is reached, then the capacitance value experiences a plateau. Such measuring techniques can be performed at different frequencies, and low frequencies can be utilized to characterize the charge movement between the layers, typically not visible at high frequency in kHz-MHz range, and estimate the presence of traps at the interface or some charge injection. These defects in the dielectric layer

eventually can cause gate bias instability and hysteretic behavior.[22] Figure 4.37 depicts the typical curve obtained performing a C-V analysis on these devices at 1 Hz.

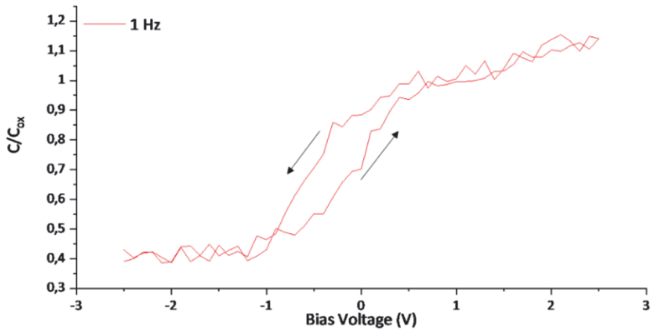


Figure 4.37 Typical C-V curve of a MOS capacitor measured at 1 Hz.

In the C-V curve, we can observe a small hysteresis: this counter-clockwise hysteresis is probably attributable to mobile ions such as residual OH^- which have a slow polarization response and, as described by *Daunis et al.*, act as a source of trap states in the dielectric.[147] Unfortunately, as previously described for the MIMs, the gate leakage also affects the MOS: the influence, visible at higher applied voltage as an increase of capacitance, did not allow a correct evaluation of the capacitance voltages higher than 2 V. Due to limited time available, we did not deepen this type of analysis as is mainly related to the dielectric behavior, focusing more on the TFT I-V characteristics, such as transfer and output, and the semiconductor characterization.

We will now discuss the methodology and the measurements performed to evaluate the performances of our TFTs from the stability point of view.

4.2.6 Characterization of TFTs stability and reliability

Establishing the TFT quality requires evaluating figures of merit, like mobility or I_{on}/I_{off} ratio, and the characterization of its operational stability and reliability. In Figure 4.38, the primary sources of instabilities are summarized.

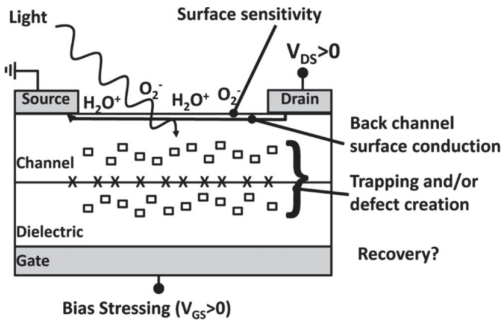


Figure 4.38 Schematic summary of potential instabilities in bottom-gate amorphous metal oxide transistors.[202]

MO_x films, like other semiconductors like organics, can be subjected to instabilities caused by interactions with the external environment and the materials and manufacturing process used. The bottom-gate configuration leaves the TFTs with the semiconductor layer exposed to the external environment: in ambient conditions, moisture and other gas, like oxygen, can interact with the active film and modify the device operation. Generally, those problems can be mitigated by depositing an extra layer acting as a passivating layer that shields the semiconductor from the external environment. Defects caused by the manufacturing process, such as remaining hydroxides trapped in the dielectric layer or a poor interface between the dielectric and the semiconductor, can also generate trapping states and device instability. As shown previously, some of these defects can also be examined by studying the low-frequency C-V characteristics of a MOS capacitor.

We performed bias stress to evaluate the stability of the TFTs and investigated the durability of our devices by checking the electrical performances one year after the manufacturing.

4.2.6.1 Positive bias stress (PBS) and negative bias stress (NBS)

An important aspect to investigate and evaluate the performance of a TFT is operational stability. The TFTs employed in high-end applications such as LCDs necessitate durability and consistent operation over time, especially concerning the threshold voltage. Due to the different sources of stress such as temperature, humidity, and voltage bias, the electrical characteristics of the device tend to be modified over time. Notably, bias stress can cause shifts in the transfer curve of the TFT, changing the threshold voltage and altering the operating voltage conditions. As operational stability is desirable in any TFT, we performed tests like positive and negative bias stress to evaluate the performance of our solution-processed metal-oxide-based TFTs annealed at high temperature.

We investigated the operational stability of the TFTs by applying a gate bias stress and measuring the resulting shift in V_{Th} (ΔV_{Th}). Figure 4.39 shows the typical curves obtained during the test and the trend relative to the ΔV_{Th} as a function of the stress time. We extracted the transfer characteristics before and after the applied stress, calculated the $V_{Th,}$ and evaluated the consequent ΔV_{Th}. A positive stress voltage of 2 V was used on the gate to accumulate carriers at the semiconductor/dielectric interface. We similarly assessed the negative bias stress was by applying a voltage of −2 V under dark conditions.

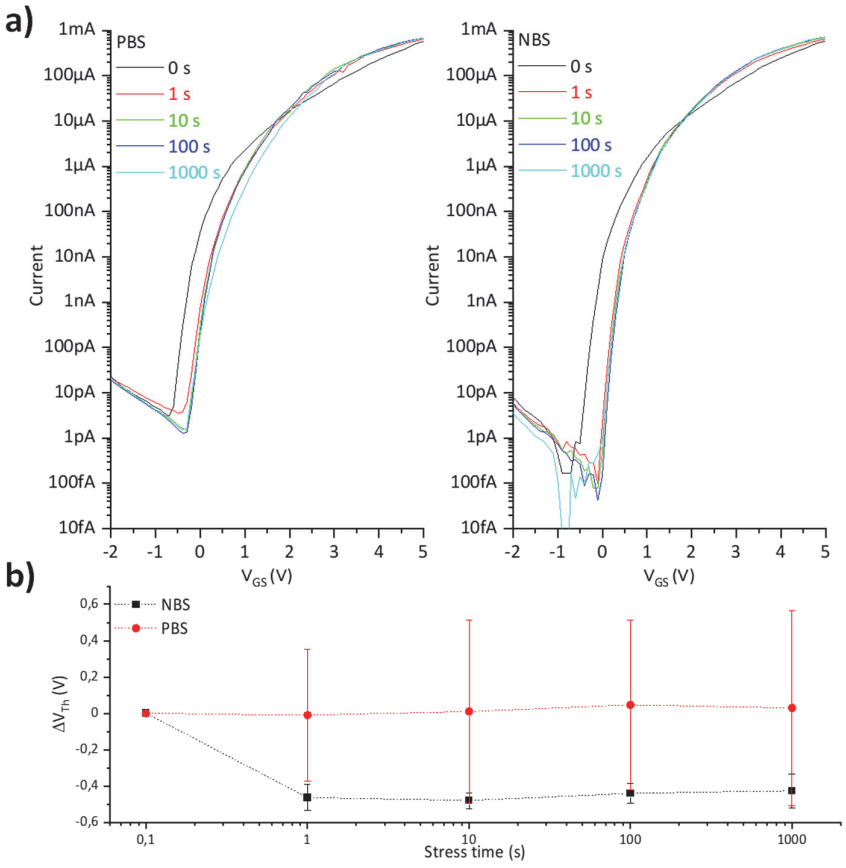


Figure 4.39 Bias stress. a) Typical transfer characteristics obtained after 1000 s of positive and negative bias stress. (V_{DS} = 1.5 V) b) Statistical distribution regarding the V_{Th} shift as a function of the stressing period. (n≥3)

The application of constant positive voltage for 10^3 s in air ambient conditions resulted in a minimal positive shift of 0.03 V. The negative bias instead showed a shift in the negative direction of -0.43 V, which is consistent with the expected behavior of an n-type TFTs subjected to negative bias under dark conditions.[202]

Ultimately, the TFTs demonstrated remarkable stability in both stress conditions, ΔV_{Th} < 0.5 V shifts after 1000 s stress and did not show signs of performance degradation.

4.2.6.2 Durability over time

Solution-processed metal oxides may suffer from exposure to the external environment. As described previously, they often tend to interact with the humidity present in the air, which ultimately can result in performance degradation and possible TFT failure.[206]

We decided to examine how aging affected the manufactured solution-based transistors by measuring the transfer characteristics one year after fabrication. During this period, we kept the samples on a shelf without any particular storage conditions. We performed an annealing at 120 °C for 10 min prior to characterization to remove water molecules adsorbed on the surface, potentially influencing the behavior of the devices. Figure 4.40 depicts the transfer characteristics collected from these devices.

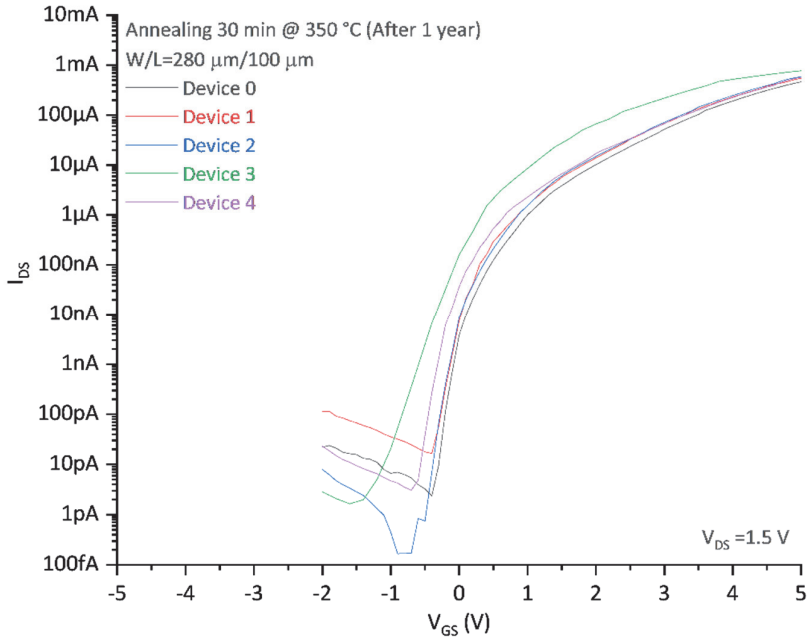


Figure 4.40 Transfer characteristics obtained from five non-encapsulated TFTs measured after one year resting under ambient air conditions.

It can be noticed that the electrical behavior was not modified from the prolonged exposure to the environment. All the tested devices maintained I_{on}/I_{off} ratios > 10^8 while showing a slight degradation in mobility, passing from the initial 68.2±3.5 cm^2/Vs to 41.1±3.8 cm^2/Vs. These results demonstrate the stability of the deposited IZO to the external environment and the remarkable durability of the TFTs, which could even be enhanced with proper encapsulation.

4.2.7 Discussion

We presented TFTs with a printed $AlO_x/YAlO_x$ gate dielectric and spin-coated IZO semiconductor, synthesized using thermally activated sol-gel processes at high temperatures. The devices demonstrated remarkable electrical performance, with mobility ~70 cm^2/Vs, I_{on}/I_{off} ratio in the order of 10^9, and stability even after one year from the fabrication. The excellent stability demonstrated over time and under bias stress was achieved without an encapsulation layer. Compared with the devices described in Section 4.1.3, the superior electrical characteristics, notably lower off-currents, can be attributed to the photolithographic process that reduces the sources of leakages by patterning components like the gate electrode and the semiconductor.

We observed from both XPS and EDX analysis indications of a tiny fraction of Al in the IZO semiconductor. Due to the small amount involved (~1 at%), it was impossible to quantify it precisely with these methods. Alternative analysis, such as SIMS or Auger spectroscopy, should be performed to confirm the results. We cannot correlate the presence of Al in the film with the high mobility achieved as it does not seem to act as a mobility enhancer. However, the presence of Al could play a role as a switching enhancer since it lowers the off-currents and prevents the shift of the transfer curves toward negative voltages, as shown in the previous paragraphs and discussed in Chapter 3.

To better position the performances of our devices, we compared them with state-of-the-art TFTs with solution-processed MO_x stacks composed of AlO_x based dielectrics and IZO semiconductors, thermally annealed at 350 °C. From Table 4.5, we can see that our non-

patterned TFTs present better performances than their counterparts, whereas the photolithographically patterned transistors displayed superior performances to the state-of-the-art.

Table 4.5 SoA regarding TFTs with fully solution-processed MO_x dielectric/semiconductor stack. If not mentioned otherwise, the films are deposited via spin-coating, and all the devices employed IZO as a semiconductor, thermally annealed at 350 °C.

Dielectric material	μ (cm^2/Vs)	I_{on}/I_{off} ratio	S.S (mV/dec)	Ref.
$YAlO_x$	2.6	1.8×10^7	N.A.	[142]
AlO_x	9.2	$>10^5$	89	[190]
$LaAlO_x$	11.9	10^4-10^5	380	[207]
$LiAlO_x$	13.5	10^4	150	[208]
$AlO_x/YAlO_x$	15.3	4.8×10^5	201	This work
Printed $AlO_x/YAlO_x$	68.2	1.5×10^9	180	This work

From the information gathered, the excellent electrical performances of the TFTs can be attributed to the exploitation of standard photolithographic processes, the quality of the semiconductor, and the synergy between printed AlO_x-based dielectric and spin-coated IZO. Despite the need for additional fabrication steps, the development of an encapsulation layer could be envisioned for practical applications. The use of passivation layers made of high-k Al_2O_3[209] or polymeric resins, like SU-8[210] or CYTOP[211], should be considered as it could improve the TFTs performances and further enhance the device stability.[202]

4.3 Conclusions

This chapter presented some relevant aspects related to the thermal annealing of solution-processed based TFTs at high temperatures.

For the first time employing a fully solution-processed MO_x stack with IZO as a semiconductor, we investigated how different dielectrics can affect the electrical performance and material characteristics of the sol-gel IZO semiconductor when treated at a high temperature. We involved high-k AlO_x-based ALD and sol-gel dielectrics for this comparison and tested temperatures ranging from 200 °C and 450 °C. The TFTs with ALD dielectric showed an incremental trend in the measured mobility as a function of the IZO annealing temperature, combined with a decrease in switching capabilities for temperatures over 350 °C, with I_{on}/I_{off} ratio decreased from 10^6 to 10^4 from 350 °C to 450 °C, and SS degraded from 0.29 V/dec to 4.1 V/dec. The TFTs with solution-processed dielectric maintained good switching performances over 300 °C, with an I_{on}/I_{off} ratio > 10^5, but mobility and current levels diminished from 400 °C to 450 °C, while the switching speed slightly improved, from ~210 mV/dec to ~170 mV/dec in SS.

We hypothesized a possible aluminum diffusion from the insulator to the semiconductor to explain some differences in the electrical results achieved, notably sub-threshold slopes and off-currents. Unfortunately, the material analysis carried via XPS could not confirm this hypothesis due to low material fractions probably involved (~1 at%), which are not easily detectable due to a signal overlap between indium and aluminum. The substantial difference in performance (maximum mobility ~28 cm^2/Vs versus ~4 cm^2/Vs) was attributed to a better interface formed between the fully solution-processed semiconductor/dielectric stack. From the EDX analysis performed on the photolithographically patterned sample with the fully solution-based stack, we observed a smooth material transition between semiconductor and dielectric.

Ultimately, we implemented a standard photolithographic process to manufacture the thermally annealed IZO-TFT devices to limit the possible sources of leakage. We realized the TFTs with a printed $AlO_x/YAlO_x$ dielectric integrated with the developed IZO semiconductor, cured at 450 °C and 350 °C, respectively. Implementing this process, we have demonstrated TFTs with performances comparable with state-of-the-art TFTs with sputtered IGZO semiconductors, like high I_{on}/I_{off} ratio ~10^9 and high mobility ~70 cm^2/Vs. We investigated the dielectric dependence from the frequency, measuring it at a very low frequency of 10 mHz, which resulted in a dielectric constant of 32.8, providing the dielectric dependence over a wide range of frequencies (1MHz to 10 mHz) and a more precise estimation of mobility values. The operational stability of the TFTs was tested via bias stress, demonstrating threshold voltage shifts below 0.5 V after 1000 s stress. The durability of the devices was proven by measuring the samples not encapsulated after one year, and the TFTs demonstrated minimal signs of degradation despite no passivation layers.

The results obtained from the thermally annealed solution-processed $IZO/AlO_x/YAlO_x$ stack confirm the suitability of the material combination to realize performing TFTs. The following chapters will report on the low-temperature synthesis methods investigated based on a DUV approach and their effectiveness assessed by comparing the results obtained with those achieved at high temperature in this chapter.

Chapter 5 Low thermal budget synthesis of IZO semiconductor through DUV-enhanced approach

This chapter addresses the reduction, via a DUV-enhanced approach, of the synthesis temperature and thermal budget for fabrication of IZO based TFTs.

We first describe the possibility of modifying the chemical composition of the semiconductor solution by introducing urea in the mixture and trigger a self-combustion synthesis. Using the fuel to oxidizer ratio (ϕ), we calculated the amount of additive for a combustion reaction that should not leave uncombusted products. We exploited the TGA analysis to evaluate the effects on the solution and compared it with the ones previously obtained from the exact solution without an additive. The curves show that incorporating the fuel does not lower the temperature to achieve the final M–O–M conversion. Since further chemical optimization would have been required to successfully establish a self-combustion reaction, we decided to maintain the IZO solutions chemistry unaltered.

We then focused on DUV-based synthesis, which appears to be a more promising approach to lower the MO_x synthesis temperature. Despite the large availability of publications on this annealing method, the lack of parametric optimization often resulted in excessively long light exposure/thermal post-treatment. We introduced a DUV-enhanced approach where the light exposure is complemented with a thermal post-treatment, demonstrating its effectiveness at a temperature as low as 200 °C, without the need for exceedingly prolonged treatments. We initially investigated the effects of the DUV light exposure and the subsequent post-annealing parameters on the chemical composition of the IZO films via Fourier-transform infrared spectroscopy. Afterward, we implemented the protocols for a TFT structure in which the semiconductor layer was combined with a high-k aluminum oxide/ yttrium aluminum oxide (AlO_x/$YAlO_x$) dielectric film to realize fully solution-processed MO_x TFTs at low temperature. We thoroughly characterized the electrical performances of the devices and the material characteristics of the MO_x layers via X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM). The TFTs treated for a long time (> 3 hours) demonstrated strong current modulation capabilities with $I_{on}/I_{off} > 10^7$ and mobility (μ_{sat}) over 35 cm^2/Vs. We also verified that shorter protocols could be highly effective on the IZO synthesis. For example, the TFTs with IZO treated with 20 min DUV followed by 60 min at 200 °C yielded $I_{on}/I_{off} > 10^8$, a subthreshold slope (SS) < 100 mV/dec, and μ_{sat} of 15.6 ± 4 cm^2/Vs. Ultimately, we demonstrated the real potential of this approach by manufacturing, with a synthesis protocol including only 5 min DUV and 5 min at 200 °C, performing devices with an $I_{on}/I_{off} > 10^8$, a SS < 100 mV/dec, and mobility ~3 cm^2/Vs.

Lastly, to investigate the viability of this approach for the IZO synthesis at a temperature lower than 200 °C, we diminished the post-treatment temperature to 180 °C. We selected a curing protocol (20 min DUV + 60 min post-annealing) and compared the electrical performances of the TFTs treated with the same protocol but at a slightly higher temperature of 200°C. The results showed a sensible drop in electrical performance, notably a mobility decrease from ~16 cm^2/Vs to ~1 cm^2/Vs. Pursuing this approach to reach lower temperatures would necessarily require undesirable long process durations. Therefore, we decided instead to implement a more powerful DUV lamp based on an excimer light source to overcome this limitation. The use of the excimer lamp and related findings will be discussed in Chapter 6.

The results presented in this chapter were included in a scientific article published in *ACS Applied Electronic Materials* [212].

5.1 Lowering the IZO synthesis temperature

This section discusses the two approaches tested during this thesis to lower the synthesis temperature and the relative thermal budget required from the IZO semiconductor.

Initially, we explored the possibility of modifying the chemistry of our semiconductor solution by adding fuel and trigger a combustion reaction. Such exothermic reaction could provide energy to the precursor conversion and reduce the need for external energy sources, thus decreasing processing temperature and time. We selected urea as is one of the most common additives employed in the low-temperature fabrication of MO_x TFTs.[95,213] We exploited the thermal gravimetric analysis (TGA) to verify the effects of the addition of this chemical compound on the chemistry involved. The results did not show the expected improvement as the temperature required in the final reaction remained unvaried. As *Salgueiro et al.*[214] previously observed during the synthesis of their sol-gel ZTO-based TFTs, the 2ME solvent may have a dual role acting as fuel as well. Its contribution as an oxidizer to the combustion chemical reactions triggered by additional fuel may ultimately disrupt their equilibrium, leading to a wrong balance between components and unsatisfying conversion or uncombusted residuals. Despite the interest in the combustion-synthesis topic, the working principle is still not understood fully. When applied to semiconductor metal oxides, it still requires relatively high temperatures (≥ 225 °C) to yield acceptable performances ($\mu > 1$ cm^2/Vs).[93] On our side, we decided to focus instead on more promising physical methods based on photosynthesis via DUV light exposure.

We then introduced the annealing protocol selected for our metal-oxide layers, consisting of variable DUV exposure followed by a thermal post-treatment at low temperature. We treated our IZO films with different combinations of DUV exposure and post-treatment duration to evaluate the effectiveness of the protocols. We investigated the chemical composition of the deposited films via Fourier-transform infrared spectroscopy (FTIR), looking for solvent and precursors residuals, and assessed the efficacy of the different protocols. Section 5.2 will further describe the effects of the annealing protocols applied to the synthesis of the IZO semiconductor film on the electrical performances and chemical composition of the realized TFTs.

5.1.1 Combustion process with urea as fuel

Among the methods explored to lower the synthesis temperature for the MO_x thin films, the exploitation of self-generated energy from a combustion reaction has frequently been reported.[95,213] A combustion reaction can be initiated when reducing compounds such as acetylacetone or urea are introduced into systems that include oxidizing elements such as nitrates. This energy, locally generated from the exothermic reaction, is then exploited for the endothermic MO_x synthesis, reducing the need for an external energy source, resulting in lower processing temperatures. In a recent review, *Carlos et al.*[95] described how parameters like type of cation, type of fuel, and pH of the solution influence reaction outcome and potentially modify the morphology of the final oxide. The fuel to oxidizer ratio (ϕ) plays a crucial role in calculating the ratio between the oxidizing and reducing components to reach a stoichiometric proportion. The approach, introduced in 1981 by *Jain et al.*[215], considers oxygen (O) and nitrogen (N) as an oxidizer, with a valence -2 and 0, respectively. Instead, carbon (C), hydrogen (H), and metal ions (M^+) act as reducing elements, respectively, with a valence of +4, +1, and their metal valence. The fuel to oxidizer ratio (ϕ) is defined as:

$$\Phi = \frac{(-1)RV}{OV} n$$

Equation 5.1 Fuel to oxidizer ratio in a combustion reaction.

RV and *OV* are the reducing and oxidizing valence, and *n* is the molar ratio between reducing and oxidizing compounds. When $\phi = 1$, no atmospheric oxygen is required for the reaction, resulting in the combustion of the precursor materials and the conversion into MO_x and gaseous byproducts, like H_2O, N_2 and CO_2. Instead, $\phi > 1$ and $\phi < 1$ indicate a fuel-rich and a fuel-deficient mixture: in these conditions, the excessive fuel and uncombusted compounds may remain trapped in the final MO_x films, damaging the electron transport and the device performances.[214,216]

Many organic compounds, such as glucose, sucrose, urea, and acetylacetone, have been studied to reduce the synthesis temperature of MO_x films. This approach has been exploited to realize both active and passive MO_x-based components at a relatively low temperature, such as ITO conductors, AlO_x dielectrics, and IGZO semiconductors.[93] The lowest temperature values have been achieved on the AlO_x dielectric manufacturing, demonstrated at temperatures as low as 150 °C.[95,213] Other components required higher temperatures to provide satisfactory performances: at 200 °C, the InO_x based TFTs reported by *Kim et al.* yielded only 0.81 cm^2/Vs, while other types of MO_x semiconductors tested (ZTO and IZO) required temperatures over 250 °C to achieve $\mu > 1$ cm^2/Vs.[93] Successive studies on MO_x semiconductors processed at low temperatures have been reported, exploiting mainly acetylacetone and urea as fuel.[213] However, process temperatures around 250 °C remained necessary to achieve acceptable performances.[50,213] We

selected the urea (U) as a fuel for our solutions, as it is a relatively cheap and available compound with a low ignition temperature that causes a strongly exothermic reaction and possesses good coordination with nitrate-based metal precursors.

We started by calculating the amount of urea to add to our mixture from equation (1) and the chemical reactions involved in the IZO formation from nitrate precursors in a 2-methoxyethanol solution, described in Equation 5.2, to ultimately achieve a stoichiometric reaction. The reducing valence of urea is +6, while the oxidizing valence of zinc nitrate and indium nitrate are -10 and -15, respectively, as the hydrated water does not contribute to the valence. From the calculations, we required a molar ratio of Zn:U = 1:1.66 and a In:U = 1:2.5.

$$2In(NO_3)_3 \cdot 2H_2O + CH_3OC_2H_4OH \rightarrow In_2O_3 + 3\,N_2 + 6\,H_2O + 3\,CO_2 + \frac{7}{2}O_2$$

$$Zn(NO_3)_2 \cdot 6H_2O + CH_3OC_2H_4OH \rightarrow ZnO + N_2 + 10\,H_2O + 3\,CO_2$$

Equation 5.2 Overall chemical reactions of MO_x formation from metal nitrate precursors (In and Zn nitrate) in 2ME solvent.

We then prepared the IZO+U precursor solution (0.2 M) and preliminary tested it via thermalgravimetric analysis (TGA). Similarly to what is shown in Chapter 3 regarding the effect of the use of different solvents, we analyzed the weight loss as a function of the temperature applied to determine the temperature range required to convert the precursor solutions. We compared the curves extracted with and without the presence of the fuel, depicted in Figure 5.1, and we could conclude:

- A significant mass drop, related to the combustion of the urea, is noticeable between ~125 °C and ~175 °C;[217]
- A higher weight loss is recorded for the sample containing urea (~55 % versus ~32 %). However, due to an initially greater amount of material (urea + precursors), we cannot univocally interpret it as a sign of better densification of the final material;
- The presence of the fuel does not lessen the temperature required to achieve the final MO_x conversion as both required over 350 °C.

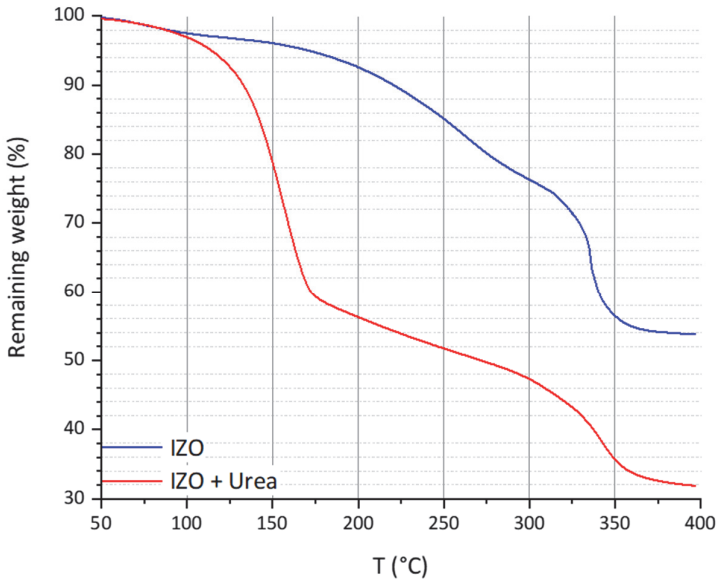


Figure 5.1 Precursors solutions thermogravimetric analysis: Comparison between two identical IZO solutions with and without urea.

We are attributing the unexpected negative outcome to an improper chemical design of the reaction. As suggested by *Salgueiro et al.*[96], it is possible that the 2ME used as a solvent to disperse the nitrate precursors may partially act as fuel as well. If it is the case, adding fuel to a mixture in which some oxidizer compound is already available shifts the fuel to oxidizer ratio ϕ ratio towards positive values, resulting in an extremely fuel-rich mixture. Figure 5.2 shows the theoretical and experimental trend of a combustion reaction as a function of the ϕ.[95] We can observe that the optimum in reaction efficiency and released heat is obtained when ϕ is 1. For ϕ>1, despite a more significant fuel availability, the reaction is slowed down by the excessive fuel present, negatively impacting the amount of heat produced during the reaction, resulting in experimental values lower than the theoretical ones. Moreover, the presence of uncombusted products will also diminish the M–O–M networking quality.

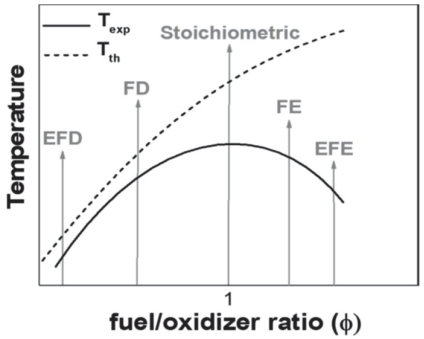


Figure 5.2 The theoretical and the experimental trend of temperature versus the fuel oxidizer ratio (extremely fuel-deficient (EFD), fuel-deficient (FD), stochiometric, fuel-excess (FE), and extremely fuel-excess (EFE)).[95]

Reducing the synthesis temperature of our MO_x layers via a combustion process approach would have required further optimization of the precursor solution chemical composition. Moreover, even with a chemical composition perfectly balanced, this approach can provide a limited amount of energy to the conversion reactions. By looking at the literature, this energy level does not seem sufficient to yield proper semiconductor layers at temperatures ~200 °C or below. We focused instead on synthesizing the IZO films via physical methods based on DUV treatments, which offer more process flexibility, especially when combined with thermal treatments and have been already demonstrated as effective for MO_x semiconductor synthesis at the temperature range of interest.

5.1.2 IZO synthesis via DUV annealing

A consistent M–O–M networking and low precursor-related impurities in the semiconductor metal-oxide film are distinguished features of performing solution-processed TFTs. Such MO_x layers can be synthesized from metal precursors that will convert into oxides through alcoholysis and condensation reactions once provided with thermal or photonic energy.[218] As discussed in Section 2.4, DUV curing has been identified as a promising candidate for low-temperature synthesis since the combination nitrate precursors-2ME solvent shows an optical absorption for wavelengths < 300 nm and photons emitted in the DUV spectrum are energetic enough to break the organic chemical bonding in the precursor.

Previous studies in the literature, summarized in Table 5.1, indicated that IZO semiconductors could be successfully manufactured by exploiting DUV based synthesis at temperatures lower than the ones reached via combustion synthesis. At a temperature of 150 °C, DUV alone or in combination with thermal treatments requires prolonged periods (≥ 120 min) to convert the MO_x precursors and remove the reaction residuals successfully. Instead, for processing temperatures of 200 °C or more, some reports show that suitable electrical performances could be achieved within reasonable processing times, such as 30 min as reported by *Leppäniemi et al.*[126]

Table 5.1 Literature regarding spin-coated IZO-based TFTs annealed via DUV methods.

Dielectric material	Energy source	T_{max} process (°C)	Total curing time (min)	Annealing conditions	μ_{sat} (cm^2/Vs)	Ref.
Thermal SiO_2	DUV+Thermal	250 – 400	120	N/A	0.4 – 11.1	[219]
Thermal SiO_2	DUV	250	240	Vapor medium	1.2	[220]
Thermal SiO_2	DUV	200	30	N_2	1.3	[126]
Thermal SiO_2	UV	150	15	Air ambient	33.1	[116]
Spin coated SiO_2	DUV+Thermal	150	150	N_2	16.2	[162]
ALD Al_2O_3	DUV	N/A	120	N_2	4.4	[118]

On our side, in the frame of this work, in collaboration with our partner at Empa, we demonstrated the feasibility of the synthesis method based on DUV exposure followed by thermal treatment at 250 °C for IZO-based solution-processed TFTs exploited for synaptic applications.[157] However, such a relatively high temperature would not be compatible with the thermosensitive substrates targeted, which necessitate process temperatures ~200 °C or below. Intending to explore the potential of the Hg-based DUV lamp, investigating a possible decrease of temperature (≤ 200 °C) and processing time, we proposed a synthesis protocol based on the combination of DUV exposure followed by thermal treatment at 200 °C.

For this study, we exploited as a DUV system depicted in Figure 5.3: a UV253HR Ozone cleaner from *Filgen*, located at EMPA, equipped with a low-pressure mercury light source, with main emission peaks at 253.7 nm (90 %) and 184.9 nm (10 %), and an output power intensity of 25−28 mW/cm^2. The samples can be located on a metallic plate positioned at 2.7 cm from the lamp, and no heat can be internally supplied (e.g., from a hot plate) during the exposure.

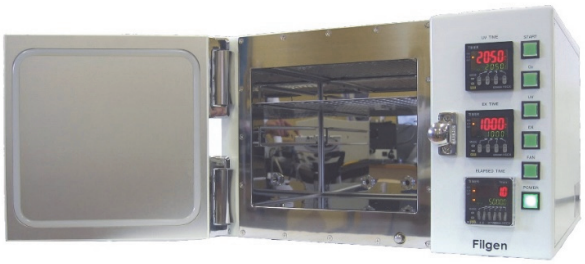


Figure 5.3 Image of the low-pressure mercury DUV lamp used for the parametric study (UV253HR from *Filgen*).

5.1.2.1 Assessment on the DUV curing protocol via Fourier Transform Infrared (FTIR) analysis

We investigated the effectiveness of the DUV-enhanced approach through the analysis of IZO films treated with different protocols. We prepared the samples by spin-coating and curing the IZO solutions on glass substrates. After a drying step of one hour at 150 °C in an ambient atmosphere, we processed the samples with different curing protocols, comprising DUV alone, thermal treatments, and combinations of the two, and finally compared the absorption spectra of the samples obtained by Fourier-transform infrared spectroscopy (FTIR). By doing so, we can identify and partially quantify the presence of given chemical species, thus evaluating the quality of the deposited films.

The FTIR measurements were conducted with a *BRUKER* single reflection attenuated total reflection (ATR) unit (diamond ATR crystal) incorporated in a *BRUKER Tensor 27* spectrometer in the wavenumber range 400–4000 cm^{-1} on samples spin-coated on soda-lime glass substrates.

To understand the effects of some of the variables involved, we analyzed and compared relevant curing conditions such as dried layers only (1 h at 150°C), thermal treatments (1 h at 200 °C or 400 °C), DUV exposure alone, and DUV followed by a post-thermal treatment. The results obtained for these different treatments are presented in Figure 4. In the case of nitrate-based solutions, the absorbance spectrum from 1300 to 1550 cm^{-1} indicates the chemical composition of the deposited films.

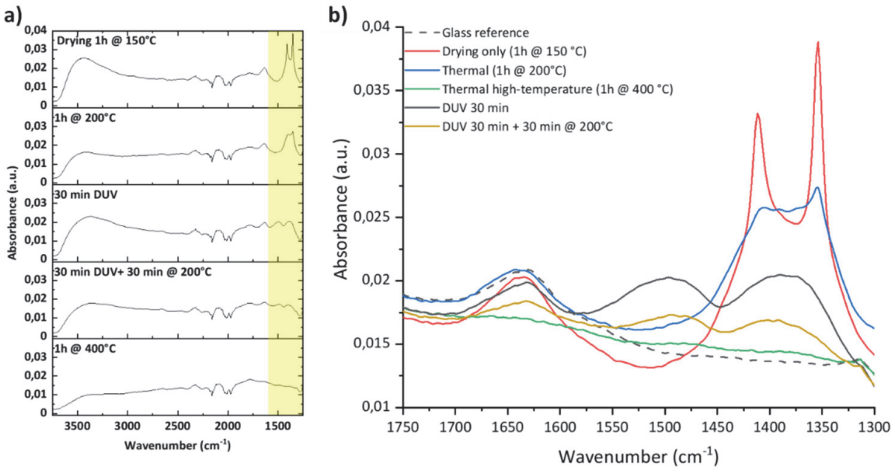


Figure 5.4 Absorption spectra extracted during the FTIR spectroscopy. a) Spectra obtained from samples treated with different annealing procedures. b) Comparison of the curves, emphasizing the section 1300 – 1750 cm^{-1} where the nitrate-related and precursor-related peaks are visible.

As expected, larger thermal budgets yielded higher quality films with fewer residuals, as displayed in the profile of the high-temperature reference. The exposure to DUV light drastically changes the adsorption spectrum of the layers, whereas the combination with post thermal treatment at 200 °C lowers the curves, thus indicating a further reduction of undesired residuals compounds in the film.

The peaks at 1650 cm^{-1} and 3000–3600 cm^{-1} are attributed to H_2O bonds vibration, bending, and stretching modes.[221] Two sharp peaks at 1353 cm^{-1} and 1410 cm^{-1}, present in the samples without DUV treatment, are linked to unconverted precursors and solvent residuals trapped in the films. The low-pressure mercury UV source presents two prominent emission peaks at 253.7 nm (90 %) and 184.9 nm (10 %), which in terms of delivered energy correspond to 472 kJ/mol and 647 kJ/mol. These energetic photons can decompose compounds with lower binding energy, such as nitrates (N–O ~ 350 kJ/mol due to the resonant bond present in the nitrate ion) and organic compounds (C–H = 413 kJ/mol, C–C = 347 kJ/mol, and C–O = 358 kJ/mol).[222] The presence of free radicals caused by the ozone produced during light exposure in an oxygen-rich environment can further enhance the residuals removal and film densification.[223] The two peaks visible between 1300 cm^{-1} and 1550 cm^{-1} are attributed to the existence of carbonates on the surface after the DUV exposure, while no nitrate residuals are detected (sharp peak at 1384 cm^{-1}).[224]

This analysis demonstrates the effectiveness of the selected method for the conversion of the MO_x precursors. We then further explored the role of variable durations for the DUV and post-thermal treatments. Implementing a parametric study, as shown in Figure 5.5, we observed that DUV exposure appears to convert the precursor solution already after 5 min. Post-annealing treatments, effective after 5 min, did not change the shape of the spectra but lowered their absolute value, which denotes a decreased concentration of impurities in the film. Both prolonged thermal treatment and DUV exposure yielded similar effects, decreasing the overall presence of impurities. These results demonstrated that MO_x synthesis via DUV does not necessarily require long exposure times of at least 15-30 minutes as reported until now. Such results suggest that, by implementing the proposed synthesis approach, it could be possible to reduce the processing time sensibly yet maintaining a maximum processing temperature relatively low, 200 °C and potentially even below.

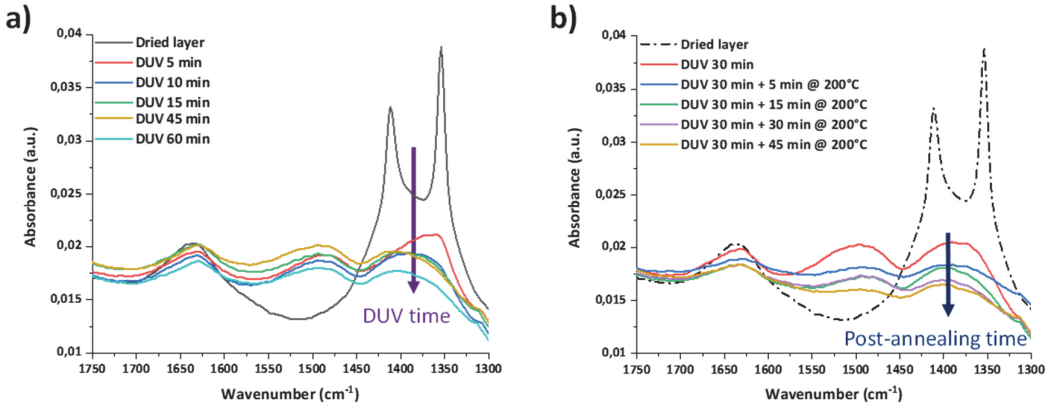


Figure 5.5 Absorption spectra extracted during the FTIR spectroscopy for different annealing protocols, comparing different a) DUV exposure time and b) post-annealing duration.

We will now implement the described IZO synthesis protocols to realize TFTs structures and evaluate their effects on the device characteristics.

5.2 DUV-enhanced approach for low-temperature synthesis of IZO based TFTs

This section describes the process flow and the characterization of the TFTs based on printed MO_x dielectric and spin-coated IZO, synthesized via a DUV-enhanced approach at a maximum temperature of 200 °C.

The synthesis approach involves various combinations of DUV curing followed by post-annealing at 200 °C. (Figure 5.6) The effects of different DUV light exposure times and several post-annealing on the chemical composition of the IZO film were studied exploiting techniques like FTIR, XPS, and EDX. We characterized the electrical performances of the TFTs and correlated the results to the different curing protocols. We investigated and identified the role of the two curing steps in the synthesis process of the semiconducting layer: the DUV exposure triggers the photochemical reaction and is required to achieve functional layers, while the following thermal post-treatment improves the quality of the films with its densification and impurity removal.

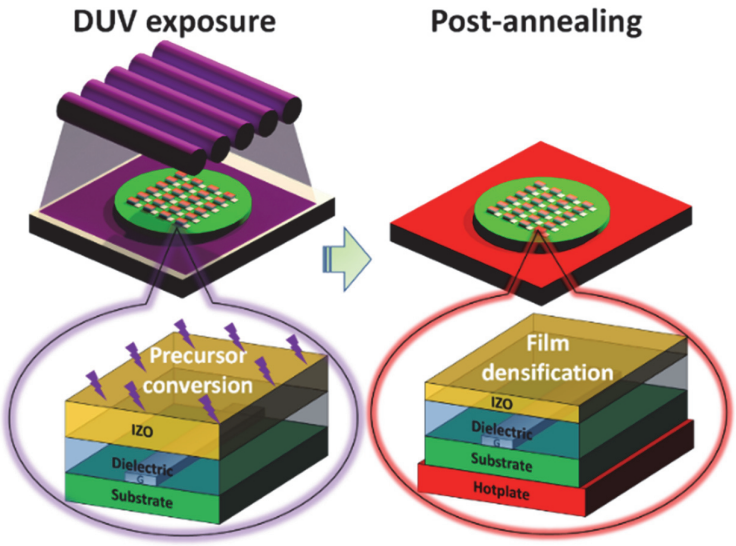


Figure 5.6 DUV-enhanced approach working principle. The DUV light triggers the precursor conversion while the successive thermal treatment at a low temperature ensures the film densification and the impurities removal.

We also highlighted that the two steps are mandatory as the samples cured separately with only DUV or thermal treatment at 200 °C did not yield performing devices. Implementing these curing protocols, we successfully obtained TFTs with mobility up to ~40 cm^2/Vs, I_{on}/I_{off} ratio $>10^7$, and subthreshold slope (SS) < 150 mV/dec. As an outcome, we have been able to shrink down the time required from the curing process and demonstrate a synthesis protocol lasting only 10 min (5 min DUV + 5 min at 200 °C), which yielded TFTs with mobility of 2.83 ± 1.4 cm^2/Vs, I_{on}/I_{off} ratio > 5×10^8, and SS of 82 ± 26 mV/dec.

Among the different characterizations performed, we ensured the stability and durability of the TFTs with bias stress tests and measurements over time. The devices treated with the shortest protocol showed threshold shifts (< 1 V) comparable to the devices cured for a longer time, demonstrating the effectiveness of the synthesis process even for such short annealing. Despite the absence of an encapsulation layer, the samples exposed to the air environment also demonstrated contained performance degradation more than twelve months after their manufacturing.

Ultimately, we investigated further the potential of the DUV-enhanced approach diminishing the post-treatment temperature to 180 °C. To supply the necessary energy at a lower post-annealing temperature, we increased the treatment duration and ultimately compared the TFT performances with those achieved when 200 °C is applied in the post-annealing temperature. Working devices with a high I_{on}/I_{off} ratio of 10^8 have been successfully achieved. Despite the relatively small decrease in the thermal treatment temperature (20 °C), we observed a decrease in mobility, suggesting that at this temperature, prolonged treatment times over 90 min are necessary to yield performances similar to those demonstrated with the same approach but at 200 °C.

5.2.1 Designs and process flow

The manufacturing process employed in this study is based on the same one presented in Section 4.2, which we exploited to realize bottom-gate TFTs with variable dimensions (W/L varying from 56 to 2.8) and the capacitive MIM structures necessary to characterize the device performances. The photolithographic masks and the lift-off process involved are the same as described in the previous chapter in Section 4.2. The differences in the processing lie in the synthesis protocols exploited to cure the deposited MO_x layers: owing to DUV-enhanced synthesis, we could successfully limit the maximum temperature of the fabrication steps to 200°C. For the sake of time, in the following paragraphs, we will report only a schematic description of the steps while providing details of the annealing protocols. Figure 5.7 summarizes the process flow of the fabrication, with the lithographic steps, the printing deposition of the dielectric film and spin coating of the IZO layer, and their DUV synthesis described in detail afterward.

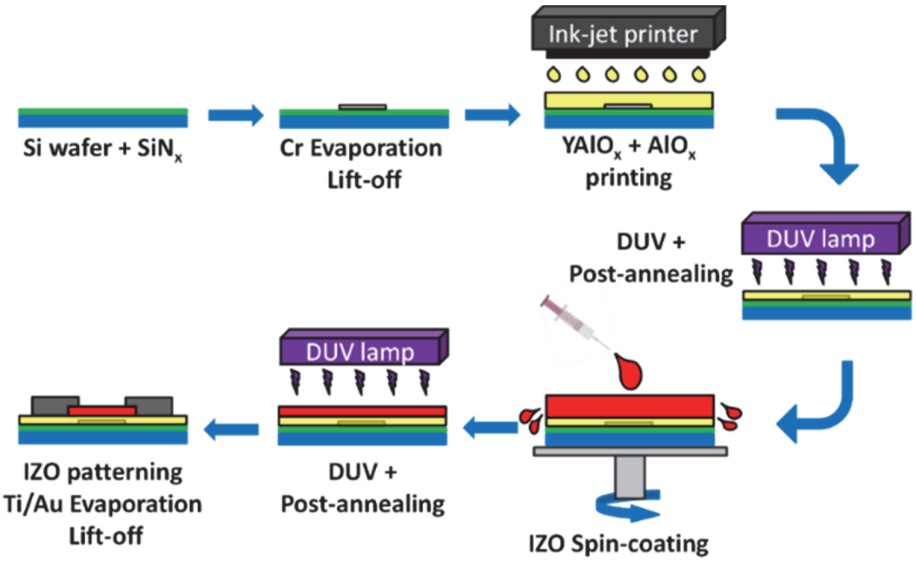


Figure 5.7 Synthetic scheme of the manufacturing process flow of the solution-processed IZO-TFTs at low temperature exploiting the DUV-enhanced approach.

As similarly described for the high-temperature thermally processed samples in Section 4.2, the processing of these devices has been performed between the CMi cleanroom located in Lausanne and the Coating Competence Center (CCC) of EMPA in Dubendorf.

As a substrate, we utilized 100 mm-wide Si wafers coated via low-pressure chemical vapor deposition (LPCVD) with a low-stress silicon nitride layer of 100 nm in thickness acting as a buffer insulator.

5.2.1.1 *Gate electrode deposition*

As gate electrodes, we used a 35 nm-thick chromium layer, deposited via e-beam and patterned via photolithography and lift-off. We patterned the structures following the methodology previously described in Section 4.2.2.1.

5.2.1.2 *Dielectric deposition and synthesis*

The preparation of the dielectric inks and the deposition methodology for the printed bi-layer $AlO_x/YAlO_x$ dielectric is the same as the ones described in Section 4.2.2.2.

For the deposition, we employed the PixDRO LP50 inkjet printer equipped with ten pL *Dimatix* DMP cartridges. Before the deposition, we performed an O_2 plasma treatment, then the two dielectric layers were printed sequentially and, after printing, dried on the hot plate for 1 hour at 200 °C in air condition. For the MO_x synthesis, we implemented a protocol developed by Dr. Sami Bolat, similar to one previously reported from the same group.[135] It comprises a DUV treatment of 45 min in a nitrogen atmosphere with the UV253HR lamp followed by a final post-annealing of 60 min at 200 °C on a hotplate in an air atmosphere. The process ultimately yielded a dielectric layer of ~30 nm, as confirmed from the TEM pictures of the device cross-section.

5.2.1.3 *Semiconductor deposition and synthesis*

We deposited the semiconductor with the same precursor solution and the methodology described previously in Section 4.2.2.4.

Before deposition, a 10 min DUV treatment was performed, and then we spin-coated the IZO solution twice to avoid layer inhomogeneities as previously described (2000 rpm for 30 seconds). Afterward, the layers are first dried on the hot plate for 1 hour at 150 °C in air condition, then subjected to a combination of DUV exposure in ozone atmosphere and post-treatment at 200 °C, both steps with variable duration, ranging between 0–60 min for the DUV and 0–180 min for the thermal step. Afterward, the layer was patterned by combining photolithography and wet etching steps.

5.2.1.4 Source and drain electrodes deposition

As a source and drain electrodes, we employed a double metal layer composed of e-beam evaporated titanium and gold, respectively 10 nm and 70 nm thick, patterned by lift-off.

5.2.2 Characterization methodology

In this section, we will describe the methodology employed to characterize the chemical and electrical characteristics of the devices.

5.2.2.1 *Material characterization*

We investigated the chemical composition of the layers via X-ray photoelectron spectroscopy (XPS) and energy-dispersive X-ray spectroscopy (EDX), whereas the crystallinity of the layers was studied via grazing incident X-ray diffraction (GIXRD) and local nano-diffraction during the TEM.

The XPS measurements were carried out using a PHI VersaProbe II scanning XPS microprobe (*Physical Instruments AG, Germany*) using a monochromatic Al Kα X-ray source of 47.2 W power with a beam size of 100 µm. The spherical capacitor analyzer was set at a 45° take-off angle with respect to the sample surface. The pass energy was 46.95 eV yielding a full width at half maximum of 0.91 eV for the Ag $3d_{5/2}$ peak. A surface sputter depth profile was conducted by Ar^+ sputtering at 2 keV and a sputtering rate of ~6 nm/min. The measurements were performed each 30 sec along with the sputtering depth. We calibrated the peaks using the C1s position (284.8 eV). We used the PHI Multipak software to obtain the curve fitting of the O1s peaks. Pierre Mettraux from the Molecular and Hybrid Materials Characterization Center (MHMC) at EPFL performed the XPS characterization and provided support during the data analysis.

For the GIXRD measurement, a *Malvern PANalytical MRD* diffractometer using Cu K-alpha radiation and a 1° grazing incident configuration was utilized. Dr. Vaclav Pejchal from CSEM performed the analysis.

Transmission electron microscopy (TEM) and scanning TEM (STEM) cross-sections analysis were performed using a FEI Talos F200S, operated at 200 kV. The EDX hyperspectral mapping was performed in STEM mode. Dr. Lucie Navratilova of the Interdisciplinary Centre for Electron Microscopy (CIME) at EPFL performed the lamella preparation. Dr. Victor Boureau operated the TEM and gathered the images.

5.2.2.2 *Electrical characterization*

We carried out the electrical characterization of the layers and the performances of TFTs (n≥5) from the various electrical active and test structures present on the wafers.

We exploited the Metal-Insulator-Metal (MIM) capacitors integrated on the wafer to measure the dielectric constant from capacitance versus frequency (C−f) measurements using a precision LCR meter (*Agilent E4980*). To compare the TFTs devices operation, we calculated the figures of merit like the saturation mobility (μ_{Sat}), the threshold voltage (V_{Th}), I_{on}/I_{off} ratio, and the subthreshold slope (SS), using the equations given in Chapter 2. The transfer and output characteristics were recorded in an ambient atmosphere at room temperature with a semiconductor parameter analyzer (*HP 4155A*). The curves were extracted from TFTs with a W = 280 µm and a channel length L = 5 µm, resulting in a W/L= 56, as shown in Figure 5.8.

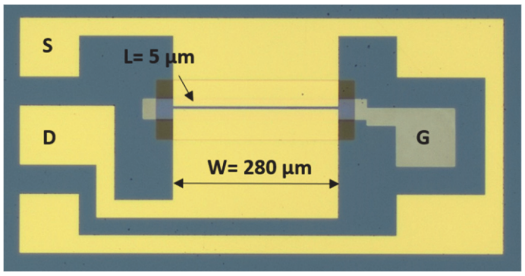


Figure 5.8 Digital optical image of a TFT fabricated and characterized in this study, including its channel dimensions.

Positive and negative gate bias stress tests were performed on the same TFT type with the *HP 4155A* by applying a constant gate voltage of +3 V and -3 V in dark conditions.

5.2.3 Influence of DUV exposure and post-annealing time on TFT characteristics

The formation of an M–O–M network in the semiconductor layer is fundamental to achieve working TFTs but is not the only condition to satisfy. Film densification and impurity elimination, as well as the quality of the semiconductor/dielectric interface, are as crucial as the conversion of the precursors: defects in the amorphous oxide semiconductor, such as residual carbon impurities, structural distortions, and incomplete M–O–M lattice formation, can lower the electron mobility and cause device instability. To analyze the contribution of DUV and post-annealing (PA) duration on the electrical performances of IZO TFT devices, we tested different

combinations of these parameters. We started from protocols involving relatively long treatments, with 20 – 60 min DUV followed by a 20 – 180 min thermal step at 200 °C. The goal here was to establish the role and the importance of each step and when combined during the IZO synthesis. Afterward, aiming for a shorter protocol duration, we performed a fine parametric study involving durations of 5 – 20 min of DUV and 5 – 20 min of thermal treatment, ultimately demonstrating operational TFTs processed with only 5 min DUV + 5 min at 200 °C. Along with the electrical measurements, using XPS, we studied the oxide conversion rate (M–O percentage, obtained from the deconvolution of O1s curves) and the chemical composition of the treated IZO layers, focusing on the presence of unconverted precursors and undesirable elements, such as nitrates, hydroxides, and carbonates.

5.2.3.1 *DUV exposure effects*

We started our investigation by assessing the effect of the DUV exposure duration, preparing and characterizing a set of TFTs exposed to DUV light for a variable time duration, 0, 20, 45, and 60 min, and a fixed post-annealing at 200 °C for one hour in air.

The devices cured using thermal treatment only did not show a stable transistor behavior (Figure 5.9a). The semi-quantitative analysis of the film composition revealed a partial MO_x conversion (M–O ~ 66 %) and residual carbon inside the IZO film (Figure 5.9b and Figure 5.9c), which may cause the improper TFT behavior. As anticipated from the analysis of the FTIR spectrum, the existence of these undesirable components can be imputable to solvent molecules trapped and possible carbonates that have not been removed by DUV light or from the ozone generated during the treatment.

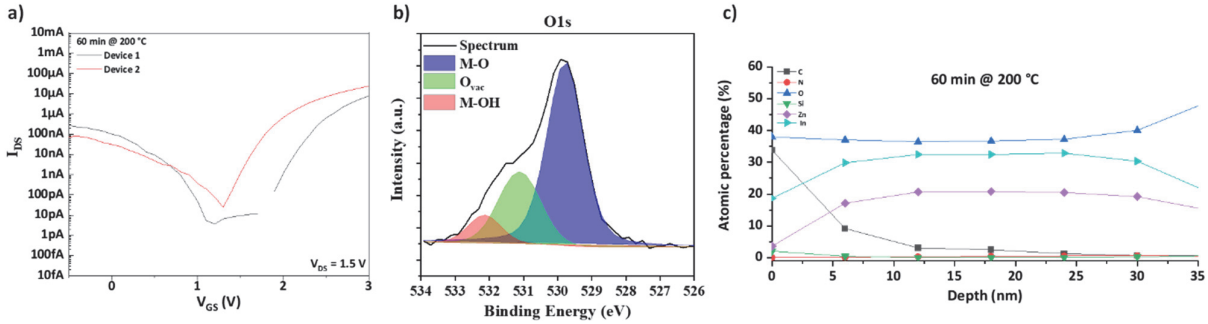


Figure 5.9 TFTs with IZO cured via a thermal treatment at 200 °C for 60 min: electrical and chemical analysis. a) Depicts the transfer curves obtained from the few working TFTs measured. b) and c) show, respectively, the deconvolution of the O1s peak and the in-depth chemical structure obtained from the XPS analysis of the IZO film.

When comparing to the characteristics obtained from IZO treated only with thermal annealing at 200 °C, presented in Figure 5.9a, a significant enhancement of the characteristics of the device has been observed already for the minimum duration of the DUV exposure of 20 min, as shown in Figure 5.10. TFTs yielded mobility of 15.6 ± 4.03 cm^2/Vs, I_{on}/I_{off} ratio 2 ± 3.4 × 10^8 and SS of 91 ± 17 mV/dec.

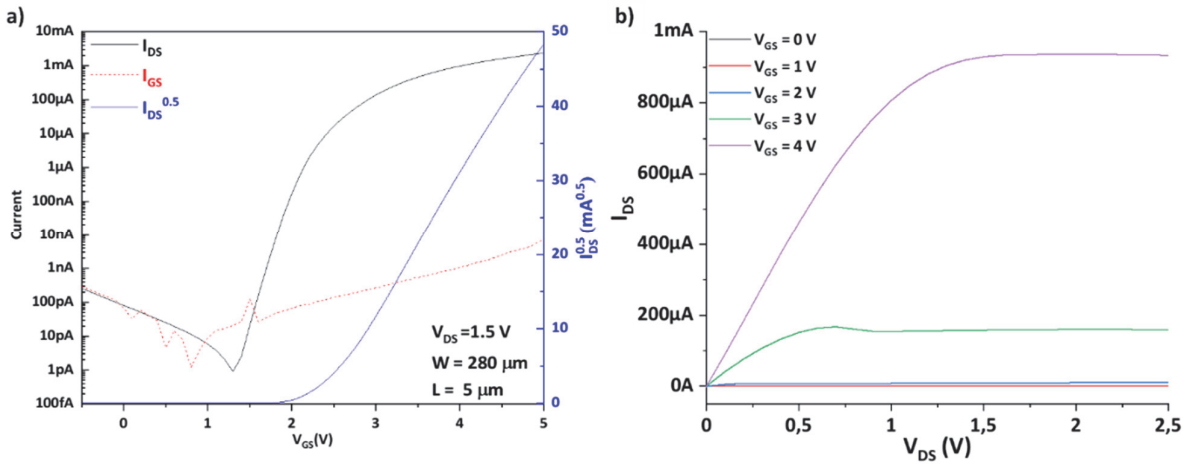


Figure 5.10 TFTs annealed with 20 min DUV + 60 min at 200 °C. Typical transfer a) and output b) curves extracted from the devices.

The XPS analysis has shown, as depicted in Figure 5.11 and summarized in Table 5.2, that the application of DUV exposure for 20 min improved the conversion of the film and resulted in a higher fraction of fully coordinated M–O bonds (70.8 %) and in decreased M–OH bonding states (2.4 %). A prolonged DUV treatment of 45 min, followed by 60 min at 200 °C, did not change the chemical structure of the film, resulting in minor fluctuations in the composition extracted from the XPS spectra.

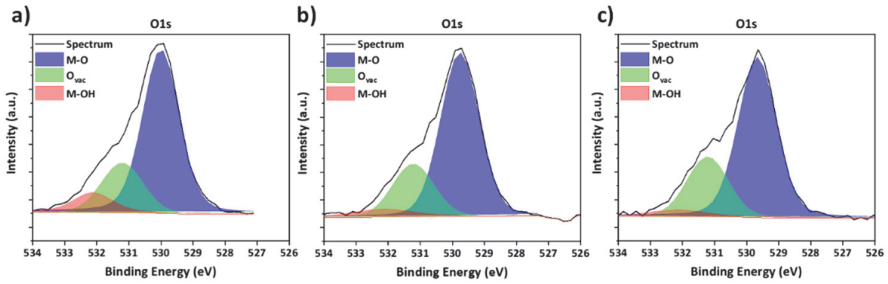


Figure 5.11 XPS spectra from different IZO layers. Deconvolution of the O1s peaks of IZO films treated with different DUV exposure time a) 0 min, b) 20 min, and c) 45 min followed by 60 min post-annealing at 200°C.

Table 5.2 Summary of component fractions obtained from the deconvoluted O1s peaks for variable DUV duration.

	M-O (%)	O_{vac} (%)	M-OH (%)	Fitting parameter (χ^2)
60 min @ 200 °C only	66.60	25.76	7.64	1.46
20 min DUV + 60 min @ 200 °C	70.76	26.83	2.40	1.14
45 min DUV + 60 min @ 200 °C	70.74	25.97	3.39	1.68

Figure 5.12 reviews the effects of the DUV exposure time on a) the chemical composition and b) the typical electrical characteristics. Figure 5.12c instead reports the whisker plots of the figures of merit extracted from the various TFTs. We can observe that the best performances in terms of switching and mobility are achieved with the relatively short DUV exposure of 20 min. Extended DUV exposures for 45 min and 60 min caused a slight decrease in mobility (15.6 cm^2/Vs at 20 min DUV + 60 min PA versus 11.8 cm^2/Vs at 60 min DUV + 60 min PA) and an increase of the subthreshold slope (91 mV/dec versus 149 mV/dec). These findings suggest that relatively long DUV exposures (> 20 min) can cause damages to the semiconductor/dielectric interface by increasing the number of traps, as indicated by the increase in SS, and negatively affecting the carrier transport demonstrated by the lowered mobility. Table 5.3 reports the statistics regarding the electrical performances of TFTs described in the section.

Table 5.3 Electrical performances extracted from TFTs treated with 0/20/45/60 min DUV and 60 min at 200 °C.

DUV time (min)	Post-annealing time (min)	μ_{sat} (cm^2/Vs)	V_{Th} (V)	I_{on}/I_{off} ratio	SS (mV/dec)
0	60	-	-	-	-
20	60	15.6 ± 4.03	1.64 ± 0.12	$2.01 \pm 3.40 \times 10^8$	91 ± 17
45	60	12.3 ± 6.91	3.11 ± 0.37	$2.25 \pm 1.10 \times 10^7$	135 ± 42
60	60	11.8 ± 8.35	2.71 ± 0.52	$8.26 \pm 5.76 \times 10^7$	148 ± 85

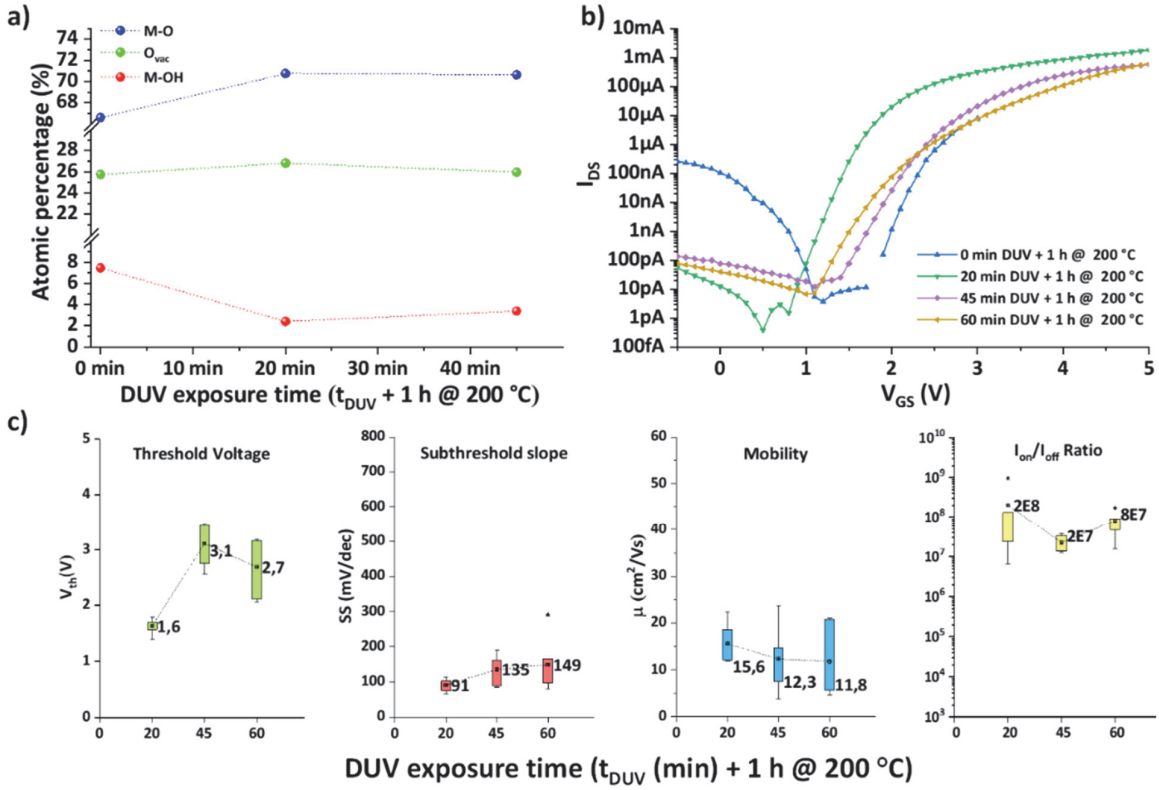


Figure 5.12 Effects of DUV exposure on the electrical performance of the TFTs and chemical composition of the IZO layers after a variable DUV exposure time (0, 20, 45, 60 min) and constant post-annealing for 60 min @ 200 °C. a) Semi-quantitative analysis of the oxygen components in the IZO films, derived from the O1s curve obtained by XPS, as a function of the DUV exposure time. (M–O ~ 530 eV, O_{vac} ~531.2 eV, M–OH ~ 532.1 eV) b) Typical transfer curves for IZO-TFTs made using different durations of the DUV exposure. c) Statistics (n>5) regarding V_{th}, SS, mobility, and I_{on}/I_{off} ratio.

5.2.3.2 Effects of post-annealing duration

As done for DUV exposure time, the role of the post-annealing time has been investigated through the characterization of TFTs exposed for 45 min to DUV light and subsequently treated with variable post-annealing periods (0–180 min at 200 °C in air).

In the TFTs exposed to DUV light only, the treatment resulted in converted precursors, as demonstrated from the FTIR spectra and further confirmed by the XPS analysis (M–O fraction in the film = 70 %) (Figure 5.13). Nevertheless, the devices (Figure 5.13a) presented inconstant poor switching characteristics and low mobility (μ_{sat} ~ 10^{-3} cm^2/Vs), confirming that DUV exposure alone, if not applied for a long time, does not supply enough energy to the semiconductor film, resulting in an incomplete conversion and densification of the IZO.[225]

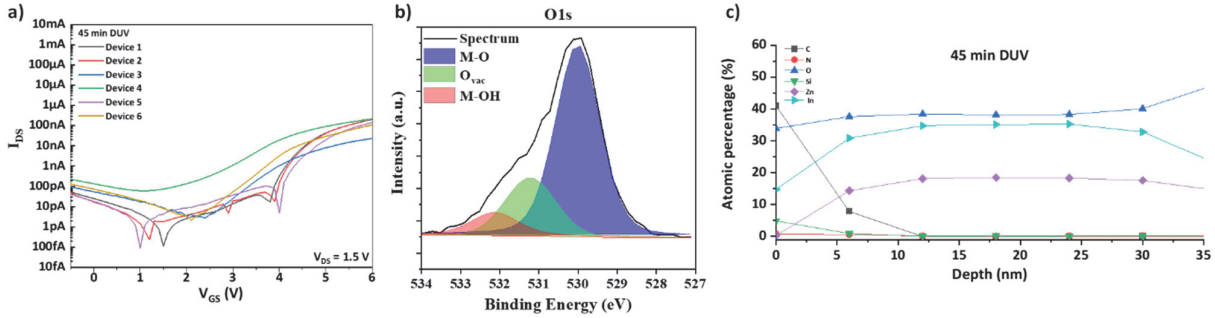


Figure 5.13 Electrical and chemical analysis of the reference samples with IZO cured via DUV only (45 min). a) Depicts the transfer curves obtained from several TFTs, b) shows the deconvolution of the O1s signal obtained from the XPS analysis of the IZO film, while c) displays the in-depth composition of the film.

We observed a sharp improvement in the electrical characteristics when treatment of 20 min on the hotplate was applied. The devices exhibited an increase of four orders of magnitude in the I_{on}/I_{off} ratio (10^8) coherent with the higher on-currents yielded (> 100 µA), a decreased SS (~ 100 mV/dec), and the mobility reached values > 10 cm^2/Vs. This mobility enhancement results from a higher MO_x structural order, associated with fewer hydroxides presented in the film and a reduced trap density. The XPS analysis, summarized in Table 5.4 and depicted in Figure 5.14, reports that prolonged post-annealing does not significantly modify the percentage of fully-coordinated M–O bonds (~ 71 %). Hydroxide content is lowered after 60 min at 200 °C from 8.9 % to 3.4 %, while the percentage of vacancies increased from 21 % to ~26 %.

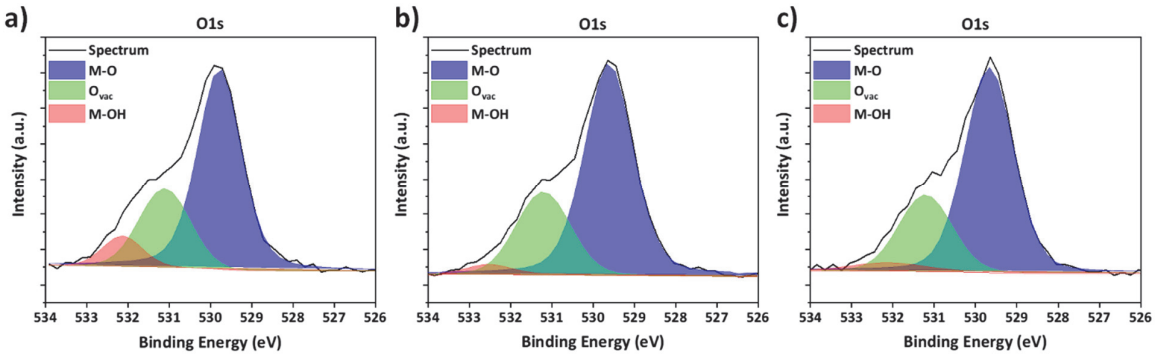


Figure 5.14 Compositional analysis, by XPS, of IZO layers exposed for 45 min DUV followed by a) 0 min, b) 20 min, and c) 60 min post-annealing time at 200 °C.

Table 5.4 MO_x composition of IZO films exposed to a fixed DUV and variable post-annealing (45 min + 0/20/60 min @ 200 °C) obtained from the deconvoluted O1s peaks.

	M-O (%)	O_{vac} (%)	M-OH (%)	Fitting parameter (χ^2)
45 min DUV only	70.08	21.05	8.87	1.08
45 min DUV + 20 min @ 200 °C	71.51	23.03	5.46	0.99
45 min DUV + 60 min @ 200 °C	70.74	25.97	3.39	1.68

The chemical analysis and the statistics regarding these devices are shown in Figure 5.15, where Figure 5.15a shows the MO_x composition as a function of the PA time and Figure 5.15b depicts the typical transfer characteristics of the devices. As can be seen from the statistics reported in Figure 5.15c, the devices treated with 45 min DUV and a PA duration of 20 – 120 minutes reported very similar performances in terms of SS, ~110 mV/dec, and I_{on}/I_{off} ratio ~10^7. In terms of mobility, 45 min DUV + 120 minutes of PA resulted in a slight increase of 1 – 2 cm^2/Vs compared to the devices treated for 45 min DUV + 20 min PA. The prolonged treatment of 180 min instead resulted in better mobility of ~40 cm^2/Vs. The simultaneous rise in subthreshold slope suggests that the channel is becoming more conductive, and more extended annealing protocols could probably result in a very conductive IZO layer. The detailed statistics on the electrical performance of the TFTs described in this section are reported inTable 5.5.

Table 5.5 Electrical performances extracted from TFTs treated with 45 min DUV and 0/20/60/120/180 min at 200 °C.

DUV time (min)	Post-annealing time (min)	μ_{sat} (cm^2/Vs)	V_{Th} (V)	I_{on}/I_{off} ratio	SS (mV/dec)
45	**0**	0.005 ± 0.002	3.86 ± 0.45	$2.03 \pm 0.16 \times 10^4$	310 ± 30
45	**20**	11.4 ± 3.94	2.76 ± 0.21	$3.88 \pm 4.25 \times 10^8$	108 ± 63
45	**60**	12.3 ± 6.91	3.11 ± 0.37	$2.25 \pm 1.10 \times 10^7$	135 ± 42
45	**120**	13.6 ± 8.75	3.20 ± 0.49	$7.74 \pm 7.00 \times 10^7$	120 ± 55
45	**180**	40.1 ± 15.5	3.11 ± 0.33	$6.83 \pm 5.22 \times 10^7$	204 ± 76

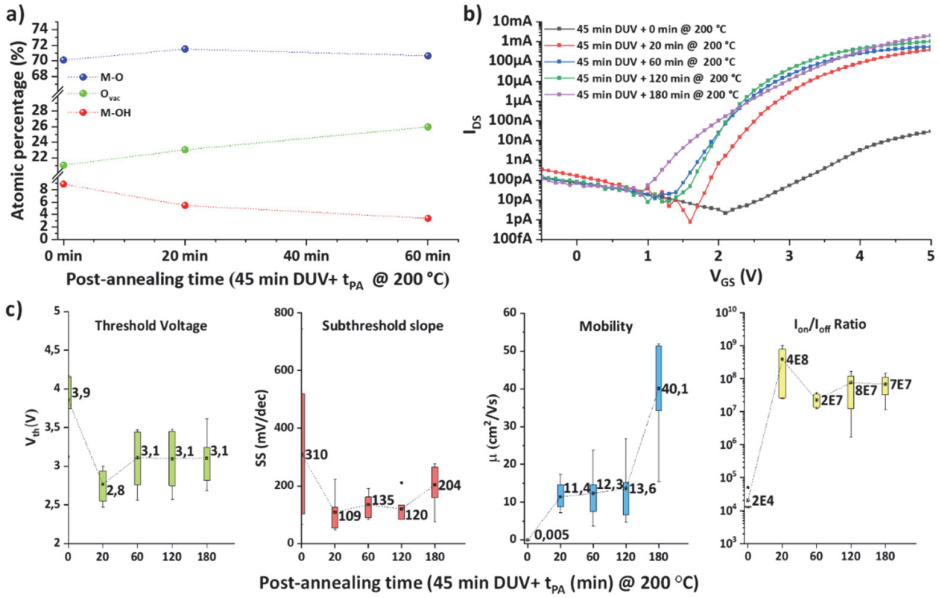


Figure 5.15 Effects of post-annealing duration at 200°C on the electrical performance of IZO-based TFTs and chemical composition of the IZO layers for a 45 min DUV exposure. a) Semi-quantitative analysis of the oxygen components in the IZO films, derived from the O1s curve obtained by XPS, as a function of the post-treatment time. (M–O ~ 530 eV, O_{vac} ~531.2 eV, M–OH ~ 532.1 eV) b) Influence of prolonged thermal annealing on the transfer curves of TFTs. c) Statistics (n>5) regarding V_{th}, SS, mobility, and I_{on}/I_{off} ratio.

The study on the effect of DUV and thermal treatment time confirmed the initial hypothesis that both DUV and post-annealing are simultaneously necessary to achieve working TFTs. Moreover, the screening performed on the effects of the protocol parameters revealed that neither excessively long (> 20 min) DUV exposures and thermal treatments are necessary to yield operational devices.

We will now discuss the results of the parametric study carried on short-duration protocols.

5.2.4 Shortening of the protocol duration

As the data previously collected suggested that prolonged treatments may not be compulsory to achieve working devices, we decided to shorten the protocol steps to explore the limits of the DUV-enhanced approach. To evaluate how a reduced thermal budget would affect the TFT performances, we explored different sets of short curing times, starting with 20 min DUV + 20 min PA, 10 min DUV + 20 min PA, and 10 min DUV + 10 PA, to conclude with the shortest protocol of 5 min DUV + 5 min PA.

In comparison to devices cured for more extended periods (20 min DUV + 60 min @ 200 °C), the decreased curing times (20 min DUV + 20 min @ 200 °C) resulted inevitably in a lessening of TFT performances; as depicted in Figure 5.16, we observed a drop in the saturation currents (~ 100 µA), which originated the lowering in mobility (μ_{sat} ~ 3 cm^2/Vs versus 15.6 cm^2/Vs). Nevertheless, the switching characteristics of the TFTs have not been particularly affected, maintaining I_{on}/I_{off} ratios higher than 10^7.

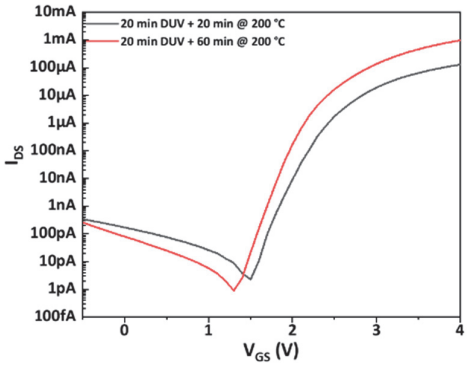


Figure 5.16 Comparison between typical transfer curves obtained from TFTs treated with 20 min DUV + 20 min @ 200 °C and 20 min + 60 @ 200 °C.

Surprisingly, annealing protocols with different combinations of shorter steps (< 20 min) yielded TFTs with similar electrical performances. Reducing the thermal budget for the IZO curing did not affect the uniformity of the TFT properties all over the substrate: as depicted in Figure 5.17, the devices showed a consistent switching behavior independently from the annealing protocol. Despite a good switching (I_{on}/I_{off} ~10^8), the TFTs cured with 10 min DUV + 10 min @ 200 °C showed unexpected low on-currents (< 40 µA) and consequently low mobility of approximately 0.4 cm^2/Vs. As this particular processing condition was the only one that resulted in such low performance, we suspect that the behavior is related to problems during the fabrication and, therefore, should be reproduced.

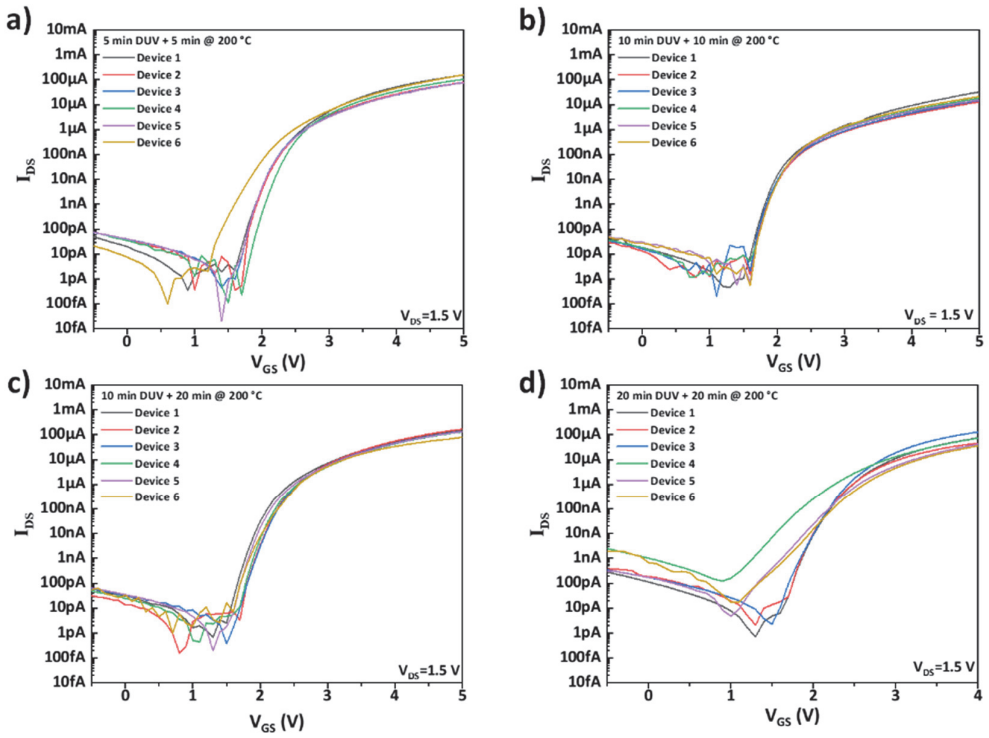


Figure 5.17 Transfer curves of various TFTs with IZO semiconductor synthetized with short protocols. a) 5 min DUV + 5 min @ 200 °C, b) 10 min DUV + 10 min @ 200 °C, c) 10 min DUV + 20 min @ 200 °C, and d) 20 min DUV + 20 min @ 200 °C .

Table 5.6 summarizes the electrical statistics obtained from the TFTs treated with short protocol duration. Figure 5.18 depicts a mobility map obtained from the experimental results (the black dots). This map, which may require additional data points to be more accurate, could be potentially exploited to roughly predict the TFTs performance (mobility) as a function of the treatment protocol duration (0–60 min).

Table 5.6 Summary of the electrical characteristics extracted from the IZO-TFT devices cured with DUV and thermal step at 200 °C shorter than 20 min. (n ≥ 6) Statistics on TFTs annealed with 20 min DUV + 1 h at 200 °C are also included as a comparison.

DUV time (min)	Post-annealing time (min)	μ_{sat} (cm^2/Vs)	V_{Th} (V)	I_{on}/I_{off} ratio	SS (mV/dec)
5	5	2.83 ± 1.44	2.68 ± 0.26	0.58 ± 1.30 × 10^9	82 ± 26
10	10	0.38 ± 0.27	2.57 ± 0.23	0.72 ± 1.59 × 10^8	72 ± 15
10	20	2.78 ± 0.82	2.57 ± 0.22	1.15 ±1.20 × 10^8	78 ± 22
20	20	2.63 ± 1.58	2.33 ± 0.10	1.17 ± 2.20 × 10^7	168 ± 81
20	60	15.6 ± 4.03	1.64 ± 0.12	2.01 ± 3.40 × 10^8	91 ± 17

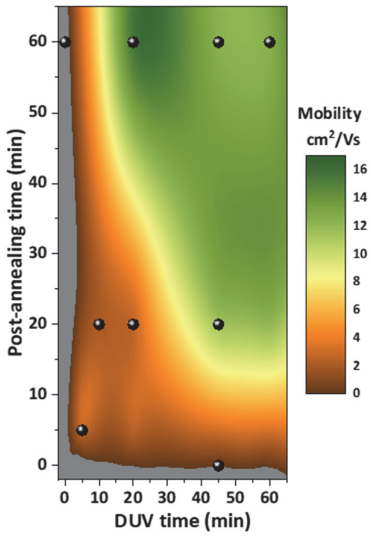


Figure 5.18 Mobility map, as a function of DUV exposure and post-annealing (0–60 min), obtained with the experimental results (black dots).

Then, we focused on the promising samples achieved with the shortest protocol of 5 min DUV + 5 min at 200 °C; the typical electrical curves and chemical analysis are depicted in Figure 5.19. The semi-quantitative analysis of the film, obtained by XPS, confirmed the conversion of precursors (67.5 %) and the complete absence of nitrate and carbonates in the layer. It also revealed a relatively high number of hydroxides (~ 14.5 %) (Figure 5.19c). The presence of these compounds affects the M–O network negatively by reducing the number of coordinate bonds between the cations and degrading the charge transport, which results in lower electron mobility (μ_{sat} = 2.83 cm²/Vs). Despite those hydroxides inside the layer, the TFTs exhibited I_{on}/I_{off} of 0.58 ± 1.30 × 10^9, a subthreshold swing of 82 ± 26 mV/dec, and a V_{Th} 2.68 ± 0.26 V.

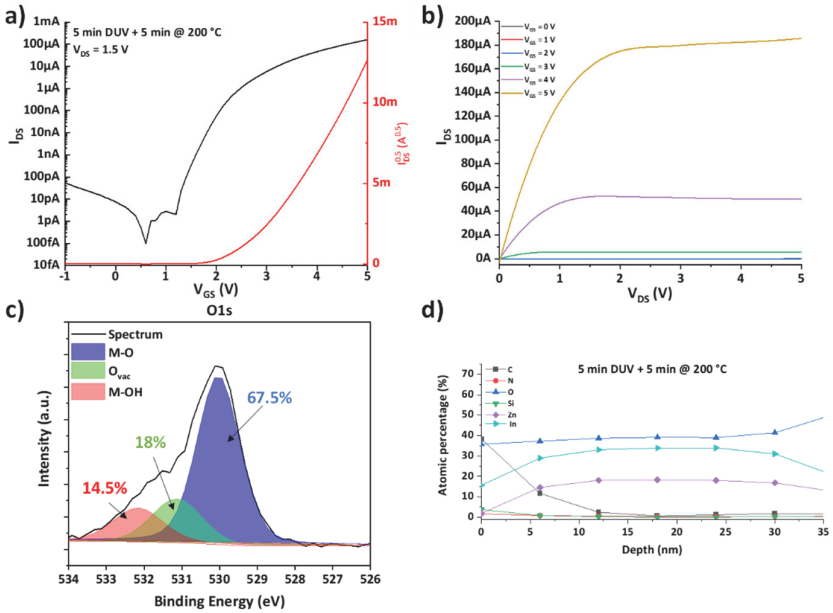


Figure 5.19 Electrical characteristics and material analysis of the IZO-TFTs cured with a short protocol of 5 min DUV + 5 min at 200 °C. a) and b) depict the typical transfer and output curves, while c) shows the O1s deconvolution and d) the chemical composition of the IZO film, obtained with the XPS.

According to the results obtained from the different combinations tested, shortening both DUV and post-annealing steps from 20 to 5 min does not significantly affect the electrical characteristics of the devices, and the MO_x synthesis can be as effective as it is with more extended protocols.

5.2.5 Complementary characterizations

Here we report in detail the results of the complementary material and electrical characterization performed on the samples. First, GIXRD and high-resolution TEM images of TFTs cross-sections are reported with material composition, layer morphology, and semiconductor/dielectric interface analysis. Then is presented the characterization of the dielectric constant performed on MIM structures, beneficial to understand the behavior of the devices and assess mobility values properly. Ultimately, the studies on device durability and stability, comprising bias stress and hysteresis evaluation, are presented.

5.2.5.1 Cross-section analysis

High-resolution TEM imaging was carried out to analyze the morphology of the deposited layers with the results presented in Figure 5.20. Samples exemplifying both the shortest and the most prolonged curing protocols, 5 min DUV + 5 min @ 200 °C and 60 min DUV + 180 min @ 200 °C, respectively, were selected to evaluate the layers of the system.

From these cross-sections, the thickness and the crystalline phase of the IZO layers were evaluated. For the shortest annealing protocol (5 min DUV + 5 min @ 200 °C), layer thickness was about 36 nm, while the layer thickness of the sample with prolonged treatment was about 30 nm. As expected, the prolonged post-treatment improved layer densification, reaching values comparable to those of samples processed with thermal annealing at 350 °C (31 nm). The measurements also showed that the dielectric layer is not affected by successive treatments, as the thickness was ~32 nm for both samples.

We investigated the crystalline nature of the IZO films exploiting a nano diffraction technique to measure the structural order of the IZO locally, confirming that the oxide is in an amorphous phase independent of treatment protocol duration.

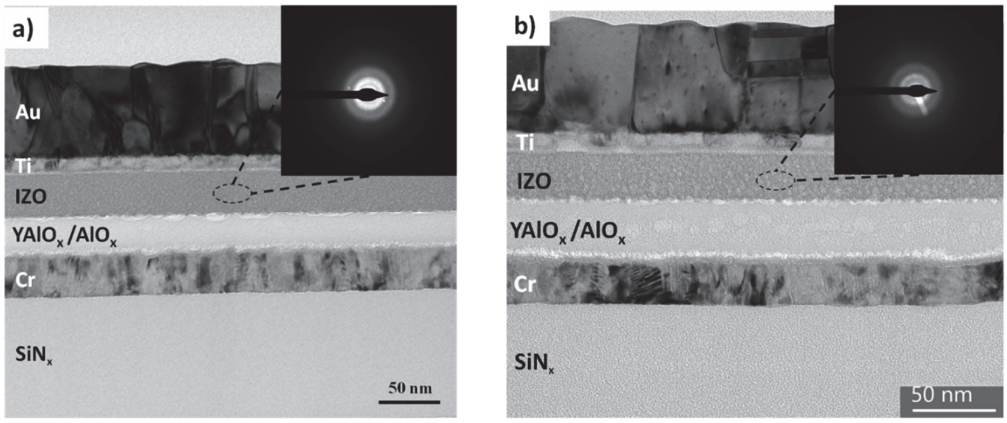


Figure 5.20 High-resolution TEM cross-sectional images of the solution-processed IZO/AlO$_x$/YAlO$_x$ TFTs. Images referred to samples annealed with a) the shortest protocol (5 min DUV + 5 min @ 200 °C) and b) longest protocol (60 min DUV + 180 min @ 200 °C). In the top corner of each image are reported the respective nano-diffraction analysis of the IZO film.

We also confirmed the crystalline nature of the IZO film via grazing incident XRD (Figure 5.21). We deposited IZO on a glass slide to perform the test and cured it with an intermediate protocol, 30 min DUV followed by 60 min at 200 °C. The X-ray diffraction pattern clearly shows the amorphous nature film. No particular diffraction peaks corresponding to a crystalline phase were observed, while the amorphous halo present between 2θ angle 20°–30° originates from the glass substrate.

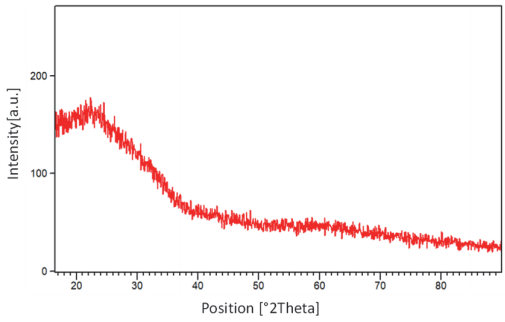


Figure 5.21 Grazing incident XRD spectrum of an IZO film synthesized with 30 min DUV + 60 min at 200 °C.

As discussed in Chapter 4, such remarkable performances achieved by the reported TFTs, even with very short curing, can also be attributed to the positive synergy between the spin-coated IZO and the printed AlO_x/$YAlO_x$. The fabricated film stack, analyzed via scanning transmission electron microscopy (Figure 5.22), revealed at the interface between dielectric and semiconductor a thin layer characterized by an atomic interdiffusion between IZO and AlO_x, independent from the curing conditions. The compositional gradient in this interlayer of approximately 10 nm in thickness, also observed in the thermally sintered devices, ensures the smooth transition between the films. The low SS values yielded by most devices confirm the presence of a high-quality interface between the two active layers, ultimately resulting in high-performance transistors.

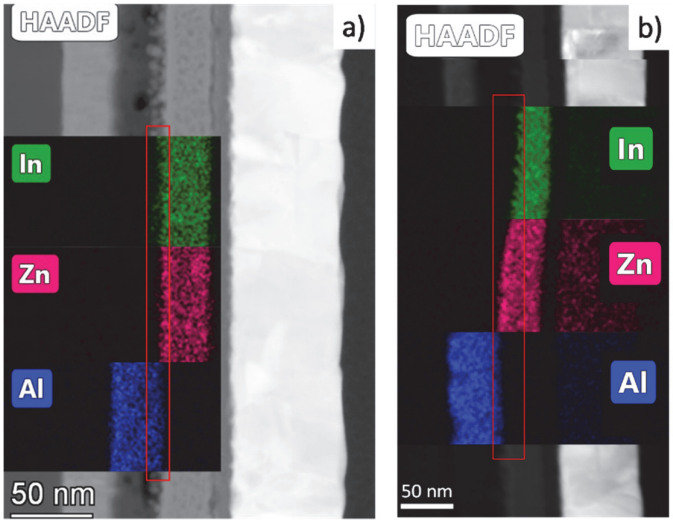


Figure 5.22 HAADF images of two TFT cross-sections recorded with TEM. Chemical composition, obtained via EDX analysis, of the dielectric/semi-conductor interface of the IZO-TFTs, treated with a) the quickest (5 min DUV + 5 min @ 200°C) and b) the most prolonged protocol (60 min DUV + 180 min @ 200°C).

5.2.5.2 Calculation of the dielectric constant

To minimize the mobility overestimation due to frequency dispersion in the dielectric layer, we evaluated the dielectric constant of the high-k MO_x dielectric at low frequency (20 Hz). Figure 5.23a shows the value extracted as a function of the frequency, while Figure 5.23b contains an optical image of the MIM capacitors exploited to extract the values. From the measurements at 20 Hz, we extracted an aerial capacitance value C_{Ox} = 295 nF/cm^2, corresponding to a k = 10, consistent with results reported in the literature with similar gate dielectrics.[135,142] During the period of the measurements, the *Keithley 4200A-SCS Parameter Analyzer* exploited in Chapter 4 for capacitive measurements at very low frequencies was not yet available. Therefore, 20 Hz was the minimum frequency testable with the available high-precision LCR meter.

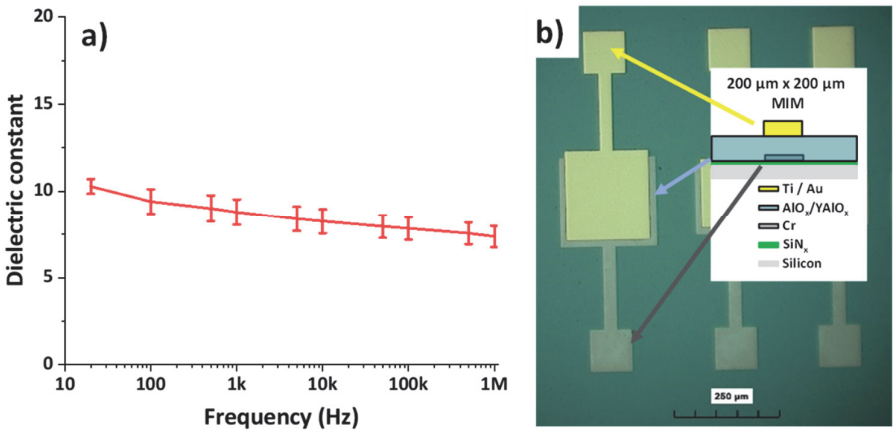


Figure 5.23 $YAlO_x$/AlO_x dielectric characterization. a) Dielectric constant as a function of the frequency, obtained from the Metal-Insulator-Metal (MIM) capacitors present on the wafers. b) Top view optical image of the realized MIM structures with schematics of its cross-section.

5.2.5.3 Transfer characteristics as a function of W/L

As the photolithographic masks contained a large variety of TFTs, we characterized the transfer characteristics of the TFTs with variable geometry. In this context, we selected devices cured with the protocol of 20 min DUV and 60 min at 200 °C, and we tested TFTs with a W/L ranging from 56 to 2.8. Figure 5.24a shows the extracted transfer curves, while Figure 5.24b depicts the mobility value extracted as a function of the geometrical parameters. From the graph in Figure 5.24b, we can see that the mobility does not depend on the geometry of the TFTs as the average calculated from the extracted values is 16.2 ± 3.19 cm^2/Vs. Such results align with the mobility data extracted from samples with the single geometry W/L = 56, 15.6 ± 4.03 cm^2/Vs.

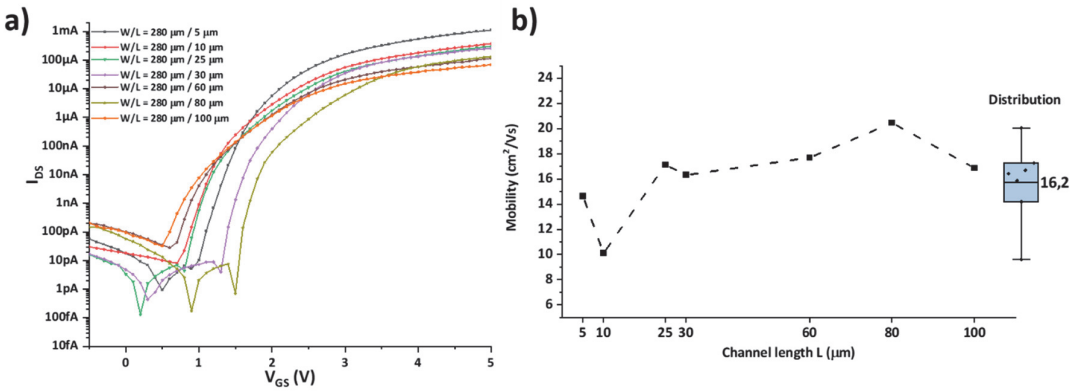


Figure 5.24 TFTs with variable geometry. a) Transfer curves obtained from TFTs with variable W/L and b) the calculated mobility as a function of the channel length.

5.2.5.4 Durability and operational stability

In previous sections, we discussed the most relevant figures of merit, such as I_{on}/I_{off} and mobility, needed to evaluate the TFT performances. However, examining the stability and the durability of the devices is also required to provide a complete assessment of their performances. To study the operational stability of the realized TFTs, we characterized aspects like hysteresis and bias stress as a function of the DUV annealing protocol applied and compared these with the characteristics obtained for the thermally annealed devices presented in Chapter 4. We evaluated how the low-temperature processing and the duration of the curing protocols affect the stability and the durability of the TFTs, especially for these devices sintered with the shortest protocol (5 min DUV + 5 min at 200 °C).

5.2.5.5 Hysteresis

Concerning operational stability, devices should not suffer from excessive hysteresis. Several mechanisms, namely dielectric mobile charges, electrical dipoles near the interface, or charge traps, can be responsible for this aspect.[11] However, the semiconductor quality resulting from the different curing protocols applied may influence these phenomena due to the remaining impurities. By scanning the gate voltage V_{GS} back and forth, the transfer characteristic of TFTs annealed with different protocols have been acquired, and the hysteresis, measured as the difference between the two threshold voltages, was evaluated. Figure 5.25 presents the typical transfer curves for TFTs processed with the shortest protocol (5 min DUV + 5 min at 200 °C) and a longer one (20 min DUV + 60 min at 200 °C) obtained when forward and backward gate voltage sweeps are performed.

The TFTs cured with the minimal thermal budget (5 min DUV + 5 min at 200 °C) exhibited a small counter-clockwise hysteresis of 0.37 ± 0.17 V, while the one measured from the TFTs annealed for a longer time (20 min DUV + 60 min at 200 °C) was slightly higher (0.77 ± 0.20 V). The counter-clockwise hysteresis as discussed in 4.2.4 is attributed to moisture adsorbed from the dielectric layer, and the values are in the same range as those measured from the high temperature thermally annealed TFTs (350 °C) reported in Chapter 4, at 0.67 ± 0.16 V. These results demonstrate that the solution-based TFTs annealed at a maximum temperature of 200 °C do not suffer from severe hysteretic instability independently of the curing protocols applied.

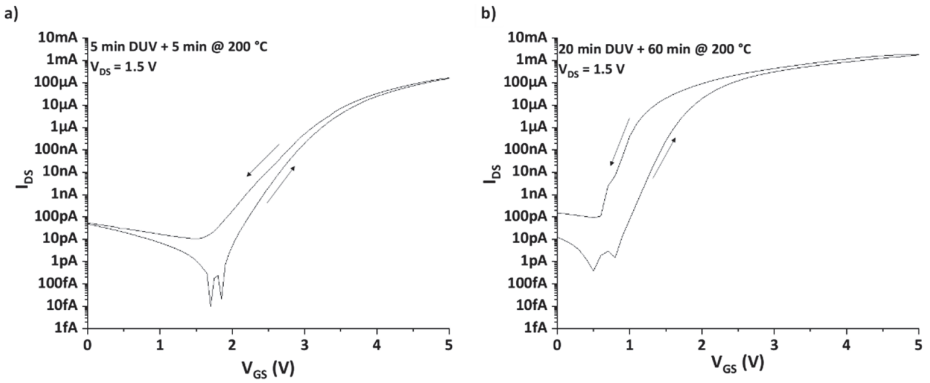


Figure 5.25 Typical hysteresis, observed during a sweep back and forth, in the transfer characteristics of IZO-TFT devices cured with a) 5 min DUV + 5 min @ 200 °C and b) 20 min DUV + 60 min @ 200 °C.

5.2.5.6 PBS and NBS

We investigated the operational stability of the TFTs by applying a gate bias stress and measuring the resulting shift in V_{Th} (ΔV_{Th}). The transfer characteristics, acquired before and after the applied stress, were used to extract the V_{Th} and evaluate the consequent ΔV_{Th}. A positive stress voltage of 3 V was applied on the gate to accumulate many carriers at the semiconductor/dielectric interface. Similarly, negative bias stress was evaluated by using a voltage of -3 V under dark conditions.

The application of constant positive voltage for 10^3 seconds in air ambient conditions resulted in a positive shift, consistent with a screening effect caused by the trapped charges in the insulator.[226] The threshold voltage shift under negative gate bias stress after 10^3 seconds shows a reduced change in the negative direction, which is frequently reported for n-type TFTs when subjected to this kind of stress in dark conditions.[202] To understand how the stability could be influenced by the IZO curing, TFTs realized using different thermal budgets (minimal = 5 min DUV + 5 min @ 200 °C, medium = 20 min DUV + 60 min @ 200 °C, and high = 45 min DUV + 60 min @ 200 °C) were evaluated. We then compared the results to quantify the operational stability according to the applied curing time. Figure 5.26a and Figure 5.26b show the positively and negatively stressed transfer curves obtained from a sample annealed with 5 min DUV + 5 min @ 200 °C; despite the use of the mildest curing conditions, the voltage shift ΔV_{Th} resulting from the stress has been relatively low (< +0.9 V and < -0.3 V after 10^3 seconds). In terms of PBS, no significant difference was observed between the samples despite the different process duration (Figure 5.26). However, in comparison with thermally annealed devices reported in 4.2, the value ΔV_{th} ~0.9 V is relatively higher (ΔV_{Th} ~0 V). This difference in stability suggests that low-temperature processed active channels may be more susceptible to interactions with the external environment than high-temperature processed ones.[202] Regarding NBS, the devices reported a negative ΔV_{Th} ~0.2 V, with the devices with the medium budget showing ~0.5 V. Such values are in line with these reported in Section 4.2.6 for thermally annealed TFTs, ΔV_{th} ~0.4 V. Both bias stress instabilities and the device durability, discussed in the next paragraph, could be improved by implementing an encapsulation layer, thus reducing the interaction with the external environment.

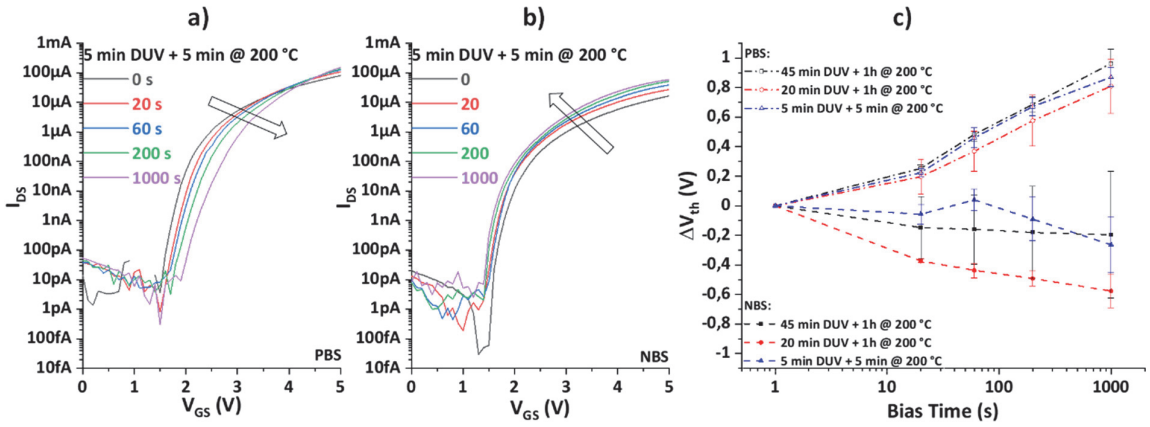


Figure 5.26 Effect of different gate bias stress time, respectively positive a) and negative b) stress, on the transfer characteristics of IZO-TFTs treated using the minimal curing treatment (5 min DUV + 5 min @ 200 °C) (V_{DS}= 1.5 V; V_{GS}= ±3 V) and c) on threshold voltage shifts of TFTs (n ≥3) cured using different protocols.

5.2.5.7 Durability over time

The durability of solution-processed metal-oxide is often questioned. The tendency of ambient air humidity to interact with the MO_x surface frequently leads to performance degradation and TFTs failure.[206] The encapsulation of the devices with a passivation layer is commonly required to mitigate this issue. To assess an eventual correlation between curing protocol and stability over time, we examined the behavior of TFTs treated using different annealing protocols. Figure 5.27 depicts the transfer curves obtained 0, 6, and 12 months after the fabrication.

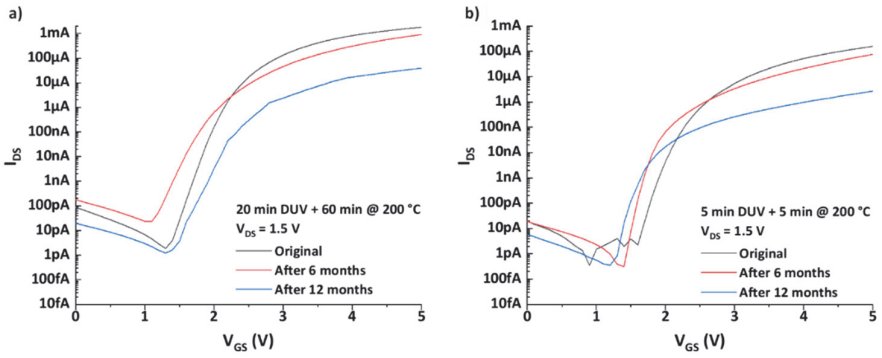


Figure 5.27 Effects of aging on the transfer characteristics of IZO-based TFTs cured with different annealing protocols: a) TFT cured with the shortest thermal protocol (5 min DUV + 5 min @ 200 °C) and b) TFT cured with a more extended annealing protocol (20 min DUV + 60 min @ 200 °C).

Despite the absence of a passivation layer, after six months of air ambient exposure, the electrical characteristics showed a minimal performance degradation independent from the curing protocol. After twelve months, the TFTs maintained a proper switching behavior with an I_{on}/I_{off} ratio >10^6 but suffered from diminished mobility for both types of curing protocols. It is worth mentioning that the performance degradation rate was similar independently from the duration of the IZO synthesis protocol, further validating the effectiveness of our quick annealing protocol of 5 min DUV + 5 min @ 200°C.

5.2.5.8 Summary of fabricated TFT performances

Here we summarize the electrical characteristics from all the various TFTs examined. Figure 5.28 shows the transfer curves (not shown previously in the paragraph) obtained from TFTs cured at different conditions. Except for samples synthesized with only DUV or thermal treatment, all tested protocols yielded working devices. Moreover, despite being extracted from TFTs distributed all over the substrate, the curves presented a relatively small variability in all tested protocols. This aspect is remarkable considering that we are implementing an active stack based on printed and spin-coated metal oxides synthesized at a maximum temperature of 200 °C. Table 5.7 reports the overall picture of the figures of merit calculated from all the devices.

Table 5.7 Electrical parameters of IZO-TFTs (n ≥ 5) processed under different curing conditions: saturation mobility (μ_{sat}), threshold voltage (V_{th}), I_{on}/I_{off} ratio, and subthreshold slope (SS).

DUV time (min)	Post-annealing time (min)	μ_{sat} (cm^2/Vs)	V_{Th} (V)	I_{on}/I_{off} ratio	SS (mV/dec)
0	60	-	-	-	-
5	5	2.83 ± 1.44	2.68 ± 0.26	0.58 ± 1.30 × 10^9	82 ± 26
10	10	0.38 ± 0.27	2.57 ± 0.23	0.72 ± 1.59 × 10^8	72 ± 15
10	20	2.78 ± 0.82	2.57 ± 0.22	1.15 ±1.20 × 10^8	78 ± 22
20	20	2.63 ± 1.58	2.33 ± 0.10	1.17 ± 2.20 × 10^7	168 ± 81
20	60	15.6 ± 4.03	1.64 ± 0.12	2.01 ± 3.40 × 10^8	91 ± 17
45	0	0.005 ± 0.002	3.86 ± 0.45	2.03 ± 0.16 × 10^4	310 ± 30
45	20	11.4 ± 3.94	2.76 ± 0.21	3.88 ± 4.25 × 10^8	108 ± 63
45	60	12.3 ± 6.91	3.11 ± 0.37	2.25 ± 1.10 × 10^7	135 ± 42
45	120	13.6 ± 8.75	3.20 ± 0.49	7.74 ± 7.00 × 10^7	120 ± 55
45	180	40.1 ± 15.5	3.11 ± 0.33	6.83 ± 5.22 × 10^7	204 ± 76
60	60	11.8 ± 8.35	2.71 ± 0.52	8.26 ± 5.76 × 10^7	148 ± 85
60	120	38.5 ± 18.9	2.81 ± 0.43	3.72 ± 2.60 × 10^7	141 ± 33
60	180	35.1 ± 16.4	2.75 ± 0.52	2.23 ± 1.49 × 10^7	134 ± 63

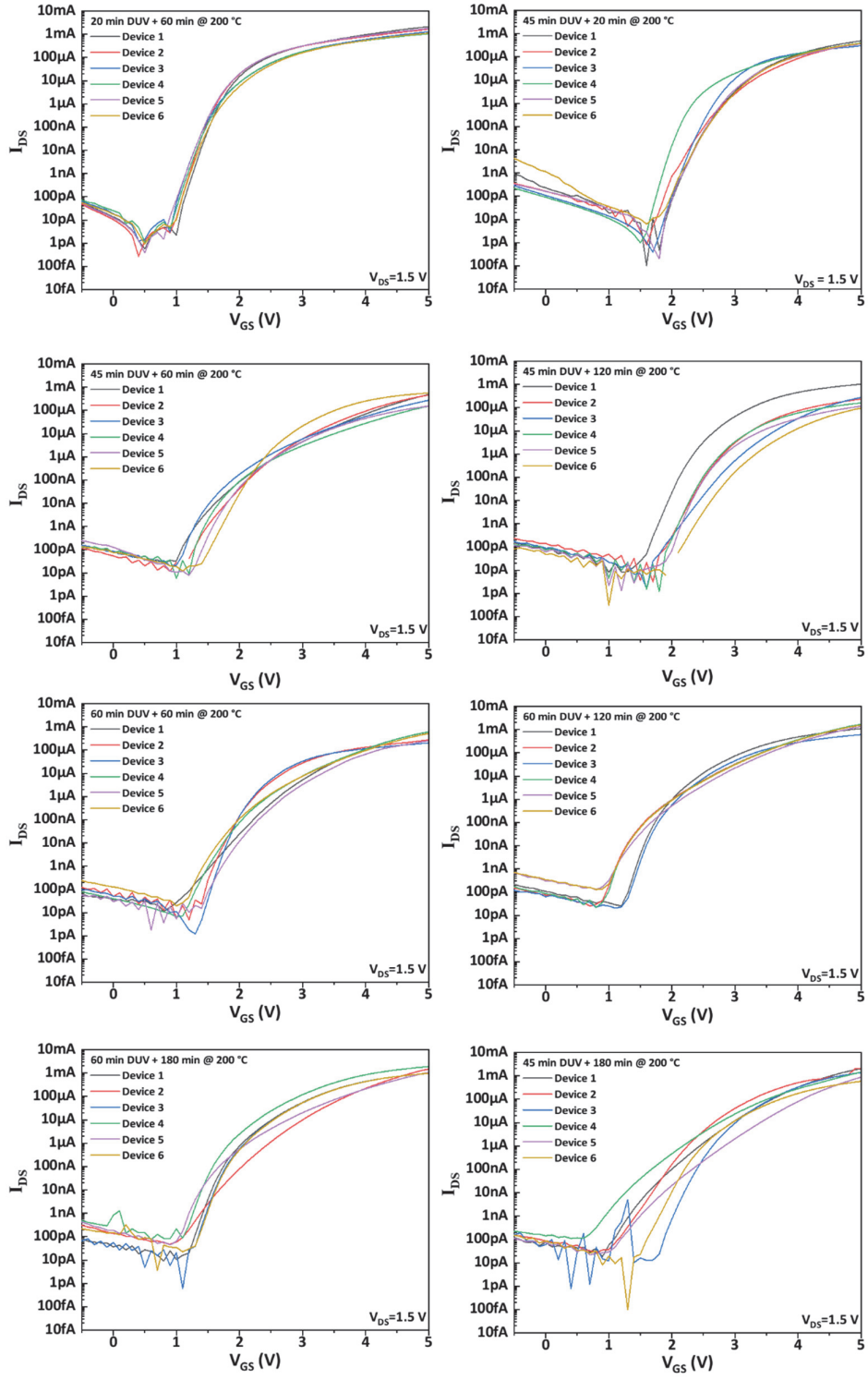


Figure 5.28 Transfer curves acquired from IZO-TFTs treated with different DUV synthesis protocols. (W = 280 µm, L = 5 µm)

5.2.6 Lowering the maximum process temperature

In the previous paragraphs, we investigated the DUV enhanced approach, studying the role of both DUV light exposure and post-annealing time on the properties of IZO films and the resulting TFTs characteristics. We verified that a minimal DUV exposure is mandatory to trigger the synthesis of the MO_x semiconductor layer. Meanwhile, we confirmed the critical role played by the thermal post-treatment that provided the proper film densification and improved the carrier transport quality in the semiconductor channel. The study enabled us to successfully reduce the thermal budget of the process by shortening its duration down to 10 min.

We then decided to reduce the temperature applied during the post-treatment to 180 °C, further diminishing the thermal budget and investigating the limits of the synthesis approach towards reaching processing conditions more compatible with thermosensitive substrates such as PEN. For the processes comparison, we selected a protocol of medium duration that yielded performing devices: 20 min DUV + 60 min post-annealing. We manufactured TFTs following the same process flow described in the previous section, but we changed the post-treatment temperature to be 180 °C and then compared the electrical performances with the ones annealed at 200 °C. In this frame, we did not change the protocol used to synthesize the dielectric layer to properly compare the TFT characteristics as a function of the IZO annealing protocol.

Figure 5.29 shows the electrical characteristics of the TFTs with IZO cured with 20 min DUV + 60 min at 180 °C. Table 5.8 reports the statistics regarding the figures of merit calculated from the samples.

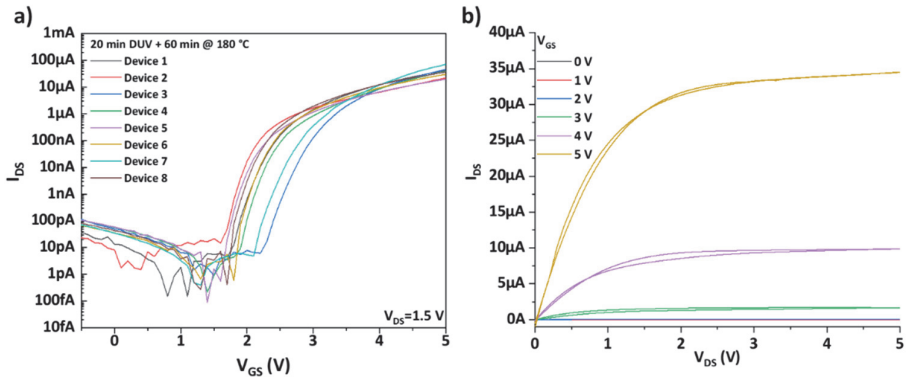


Figure 5.29 Electrical characteristics of TFTs with IZO semiconductor synthesized with a protocol of 20 min DUV + 60 min at 180 °C. a) Transfer curves acquired from various devices, and b) a typical output curve.

As visible from Figure 5.29a, the devices presented an excellent current modulation quantified in an I_{on}/I_{off} ratio of 0.58 ± 1.29 × 10^9, similar to the one achieved at 200 °C, and a suitable device-to-device uniformity. The TFTs demonstrated decent saturation mobility of 0.95 ± 0.70 cm^2/Vs and a low subthreshold slope of 91 ± 10 mV/dec. Unfortunately, compared to the devices cured with a process temperature of 200 °C, the TFTs sensibly underperformed in mobility. Compared to the shortest protocol of 5 min DUV + 5 min at 200 °C mobility levels three times lower are yielded, whereas using the same protocol are more severely decreased from ~16 cm^2/Vs to ~1 cm^2/Vs.

Table 5.8 Summary of the electrical performances of the devices with an IZO semiconductor cured with a maximum process temperature of 180 °C (n>8). As a comparison, we reported the results obtained with the same protocol but at 200 °C and the shortest protocol (5 min DUV + 5 min at 200 °C).

	μ_{sat} (cm^2/Vs)	V_{th} (V)	I_{on}/I_{off} ratio	SS (mV/dec)
20 min DUV + 60 min @ 180 °C	0.95 ± 0.70	2.83 ± 0.32	0.58 ± 1.29 × 10^9	91 ± 10
20 min DUV + 60 min @ 200 °C	15.6 ± 4.03	1.64 ± 0.12	2.01 ± 3.40 × 10^8	91 ± 17
5 min DUV + 5 min @ 200 °C	2.83 ± 1.44	2.68 ± 0.26	0.58 ± 1.30 × 10^9	82 ± 26

This drop in performance exposed the technical limitations of this approach. From the results, we can conclude that at 180 °C, to achieve electrical mobility similar to the one shown previously for devices annealed at 200 °C, an extended post-annealing time is compulsory to remove the residuals from the MO_x films and ensure a satisfactory M–O–M networking. As excessively long treatments are ultimately not practical, especially as we target substrates that are not very thermally stable, we decided to explore alternative methods to diminish the synthesis temperature while containing the process durations. In this context and in the next chapter, the use of a more powerful excimer-lamp will be introduced.

5.2.7 Discussion

This chapter explored two potential approaches to generate energy and minimize the need for thermal energy, thus lowering the synthesis temperature of solution-processed IZO semiconductors: a chemical one, linked to the insertion of fuel in the precursor solution to trigger a combustion reaction, and a physical one, exploiting a DUV-based synthesis.

The first approach is relatively limited in process variables and resulting extra energy provided to the conversion reaction. The amount of energy available is determined by the nature of the fuel and from the balance between oxidizing and reducing elements.[95] Different fuels have been investigated to lower the processing temperature in sol-gel MO_x-based TFTs in this frame. However, requirements such as low ignition temperature and compatibility with precursor solution have narrowed down the number of suitable chemicals, such as urea and acetylacetone. Moreover, the possible reducing nature of the 2ME solvent complicates the correct balancing of the reaction, potentially leading to a poor M–O–M networking and the remaining of some residuals. By looking at the literature, the energy level provided by the fuel alone does not seem sufficient to yield proper semiconductor layers at the temperature range of our interest, 200 °C or below. After a preliminary study on the precursor solutions carried via TGA, we decided to pursue another approach.

Synthesizing the IZO films via physical methods based on DUV treatments, on the other hand, offer more process flexibility (lamp type, exposure environment, process duration), especially when combined with thermal treatments (heat supply for a certain amount of time, during or after the DUV) and have been previously demonstrated as effective for the semiconductor synthesis at the temperature range of interest. We proposed an approach composed of a DUV exposure followed by thermal treatment. FTIR results showed that DUV exposures require exposure ≥ 5 minutes to convert the precursors. The effectivity of the DUV photosynthesis for MO_x precursor conversion after such a short exposure was never proven before as it was previously reported that at least 15 – 30 min were necessary.[116,118] The thermal treatment (200 °C) instead appeared to be effective for the residual removal as the absorption signal measured with FTIR was reduced after 5 min of treatment. Using the proposed approach, we achieved performing TFTs employing minimal protocol durations of 5 min DUV + 5 min post-annealing at 200 °C. We have also manufactured TFTs at a maximum temperature of 180 °C, which yielded an excellent current modulation capability, with an I_{on}/I_{off} ratio > 10^8. However, mobility values ~ 1 cm^2/Vs were sensibly lower than those achieved with the protocols at 200 °C and can also be reached from TFTs with organic semiconductors. We have demonstrated that 180 °C is the limit in process temperature reachable with this method, within a reasonable processing time. It is possible that very long (> 90 min) thermal treatment would have improved the electrical characteristics. However, it would have been unpractical, and prolonged treatments may not successfully compensate for the energy provided at higher temperatures. In Table 5.9, the representative results of the study are positioned with respect to the state-of-the-art regarding IZO based TFTs.

Table 5.9 State-of-the-art about IZO based TFTs treated via DUV or processed at T≤ 200°C, including representative results presented in this chapter. All IZO films have been deposited via spin-coating.

Ref.	*Dielectric material*	*Energy source*	*T_{max} process (°C)*	*Total curing time (min)*	*Annealing conditions*	*Mobility (cm^2/ Vs)*
[219]	Thermal SiO_2	DUV+Thermal	250 – 400	120	N/A	0.4 – 11.1
[220]	Thermal SiO_2	DUV	250	240	Vapor medium	1.2
This work	**Printed AlO_x/$YAlO_x$**	**DUV+Thermal**	**200**	**225**	**Air ambient**	**40.1**
[161]	ALD Al_2O_3	Thermal	200	120	Air ambient	4.1
This work	**Printed AlO_x/$YAlO_x$**	**DUV+Thermal**	**200**	**80**	**Air ambient**	**15.6**
[126]	Thermal SiO_2	DUV	200	30	N_2	1.3
This work	**Printed AlO_x/$YAlO_x$**	**DUV+Thermal**	**200**	**10**	**Air ambient**	**2.8**
This work	**Printed AlO_x/$YAlO_x$**	**DUV+Thermal**	**180**	**80**	**Air ambient**	**0.95**
[116]	Thermal SiO_2	UV	150	15	Air ambient	33.1
[162]	Spin coated SiO_2	DUV+Thermal	150	150	N_2	16.2
[118]	ALD Al_2O_3	DUV	N/A	120	N_2	4.4

The parametric study provided new information on the effect of DUV exposure and thermal post-annealing on the IZO networking and the TFT performances. For the first time, such a study has been performed on a low-temperature DUV-processed sol-gel MO_x active stack with printed dielectric and spin-coated semiconductors. By doing so, we demonstrated the feasibility of the DUV-enhanced approach for different MO_x materials combined together. This methodology is fundamental to understand the TFT system for the future development of fully printed IZO-based TFTs.

To maintain the desirable electrical performances while lowering the process temperature, we could envision a synergic combination of the combustion process and DUV annealing, which so far has been demonstrated effective only for gate dielectric synthesis at temperatures as low as 150 °C.[95] However, a not easy fine-tuning of the chemistry would be compulsory, and an investigation of the semiconductor MO_x quality and the electrical performances of the resulting TFTs would be necessary to establish the viability of the method at temperatures ≤ 200 °C.

On our side, we are proposing in the next chapter a synthesis approach based on a more powerful DUV exposure with simultaneous heating that could increase the efficacy of the DUV photosynthesis and help in decreasing both time and processing temperatures. This method will be discussed in the next chapter.

5.3 Conclusions

In this chapter, we proposed a low-temperature synthesis method for manufacturing our IZO-TFTs based on DUV exposure followed by thermal treatment at temperatures as low as 180 °C. We studied how different treatment times influence the IZO MO_x composition and the performances of the resulting TFTs, ultimately demonstrating that the approach could be effective even with exposure protocols as quick as 10 minutes.

We studied via FTIR the chemical composition of the IZO layers for different combinations of variable DUV exposures and post-treatments we applied. We investigated the role of DUV exposure and the effect of the successive post-annealing on the IZO properties and the TFT characteristics, demonstrating that DUV treatment is required to ignite the conversion of nitrate precursors into a MO_x network. The FTIR analysis performed on IZO treated for a variable time suggested that a DUV exposure time as short as 5 minutes could trigger the photosynthesis of the MO_x.

Then, we implemented the approach to manufacture TFT with solution-processed high-quality IZO semiconductor films and printed high-k MO_x dielectric and limited the processing temperature to 200 °C. We verified that the DUV exposure and the thermal treatment at 200 °C alone were insufficient to achieve working devices while the combination of the two treatments could enable mobility ranging from over 40 cm^2/Vs, for prolonged treatments (45 min DUV + 180 min at 200 °C), to ~10 cm^2/Vs for shorter protocols (45 min DUV + 20 min at 200 °C). Even if the TFTs achieved lower performances than those obtained via thermal processing at 350 °C (~68 cm^2/Vs), these treatments demonstrated capable of yielding devices that are superior to those reported in the literature, annealed with a similar approach and temperature range.

We showed that a drastic reduction of the treatment time and the thermal budget was possible via a thorough parametric investigation of the DUV exposure and post-annealing time, demonstrating that excessively prolonged treatments may be superfluous. The curing process of the semiconductor film can be as short as 10 min (5 min DUV + 5 min at 200 °C), resulting in TFTs with I_{on}/I_{off} of 10^8, a SS = 82 ± 26 mV/dec, and a μ_{sat} of 2.83 ± 1.4 cm^2/Vs. We characterized the stability of the devices via bias stress and their durability, monitoring their behavior over time. The results showed that despite the rapid synthesis protocol, the devices did not suffer from severe instabilities compared to TFTs cured at the same temperature for a longer time and to those processed thermally at 350 °C, confirming the effectiveness of the synthesis method.

Envisioning a possible implementation of the method for the synthesis of metal-oxides by sol-gel on thermosensitive substrates like PEN, the post-annealing temperature was further reduced to 180 °C, at the cost of extended exposure duration. Despite the diminished processing temperature, the TFTs yielded I_{on}/I_{off} over 10^8 and μ_{sat} of 0.95 ± 0.70 cm^2/Vs. Unfortunately, the mobility was over an order of magnitude lower compared to the value achieved from TFTs treated with the same protocol at 200 °C. To maintain proper TFT performances, even at temperatures lower than 200 °C, we decided not to pursue this method further and replace the DUV source with a more powerful one, based on excimer emission, which will be discussed in the next chapter.

Chapter 6 Towards fully printed MO_X TFTs at low temperature

This chapter presents the results regarding the printing of the metal oxide functional layers and reducing the thermal budget required for their synthesis to ultimately achieve fully printed TFTs on polymeric foils. The results in this chapter have been achieved with the support of Dr. Jaemin Kim from EPFL-LMTS, whom manufactured and characterized part of the reported samples.

First, we introduce the DUV excimer system exploited to further decrease the thermal budget required for the MO_x synthesis. This system, equipped with an excimer light source and a heating stage, can provide higher photonic energy while exploiting the application of heat during the DUV exposure to improve the precursor conversion process. Such an "in-situ" approach is often exploited to achieve solution-processed InO_x-based TFTs at temperatures below 200 °C. However, it is a relatively new approach for IZO-based TFTs as only one report is available in the literature, in which IZO was processed at 200 °C.[126]

Then we focus on the inkjet printing of our functional metal-oxides layers. We first introduce the printing method addressing the theory necessary to understand the relative ink requirements and expose the challenges linked to the deposition methodology. Then, the established process and the studies on the various printing parameters necessary to optimize the quality of the deposited AlO_x/$YAlO_x$ dielectric and the IZO semiconductor films are reported. In this frame, we started from the dielectric MO_x stack as our partner at Empa had already established the ink formulation. We transferred the printing process to our inkjet platform, and to ensure uniform coffee ring effect-free layers, some process parameters, such as the duration of the O_2 plasma used to pre-treat the substrate and the stage temperature during printing, were tuned. Finally, we verified the effectivity of the in-situ DUV excimer treatment on the dielectric stack and studied how temperature could affect its electrical performance, ultimately achieving functional AlO_x/$YAlO_x$ layers even at synthesis temperatures lower than 150 °C.

Following the work on the metal-oxide dielectric, we address the printing by inkjet of the IZO precursors solution starting from equal ethylene glycol (EG)/2-methoxyethanol (2ME) co-solvent/solvent composition. Since having a high boiling point of 197 °C, we investigated the effect of EG concentration on the DUV assisted synthesis of IZO films at low temperature, evaluating how TFTs with IZO semiconductor, printed using different solvent/co-solvent formulations (5 %vol to 50 %vol of EG in 2ME), perform when treated with in-situ DUV excimer at variable temperatures (160 °C to 180 °C). The results confirmed that electrical performances are indeed affected by the amount of co-solvent. We chose an ink formulation with 10 % co-solvent as it provides a suitable trade-off between jetting stability and electrical performance. Afterward, we further investigated how the ink concentration and layer stacking affect the final IZO film thickness and uniformity and the related TFT behavior. We observed how a sufficiently thick semiconductor is essential for satisfactory electrical performance and identified an optimal condition for one IZO layer printed with a 0.5 M ink and 10 % EG.

Ultimately, we combined the two printed metal-oxides films to achieve TFTs with a fully printed active metal-oxide stack. We proved that it was possible to achieve satisfying switching characteristics and mobility in the range of 4 cm^2/Vs with a fully printed dielectric and semiconductor stack thermally synthesized at high temperature. By implementing the in-situ DUV excimer approach at low temperature (< 200°C), unsatisfactory electrical performances were obtained, notably high leakage currents and poor yield, showing that processing a high-quality dielectric/semiconductor metal-oxide interface by printing and DUV treatment is tricky, involving many influential factors, which require broader and deeper investigations for better identification of the critical parameters to optimize, eventually supporting an optimum adaptation of the process flow.

Finally, envisioning fully printed TFTs, we present the preliminary work performed on the printing source and drain electrodes. In this frame, we demonstrated the possibility of integrating printed silver and gold thin films as top electrodes over the semiconductor layer by exploiting aerosol jet printing capable of reaching a line resolution of tens of µm. We also addressed the transfer onto thermosensitive foil of the manufacturing process. Preliminary studies on two potential substrates have been performed, identifying polyetherimide (PEI) as the most promising. We successfully realized the printed dielectric stack, annealed via in-situ DUV excimer treatment for 20 min at 170 °C, and leakage levels below 10^{-7} A/cm^2 at 1 MV/cm. Such results demonstrated the feasibility of the

proposed approach for low-temperature synthesis of functional MO_x layers on PEI, paving the way, following some tuning of the process, for the manufacturing of more complex structures such as TFTs.

A scientific article is under preparation, including some of the achievements presented in this chapter on the DUV-excimer synthesis of printed metal-oxide electronic films at low temperatures.

6.1 Synthesis of metal-oxide dielectric and semiconductor films via an excimer DUV system

In this section, we introduce the excimer-based DUV system exploited in the last part of this thesis to further reduce the thermal budget required to synthesize the functional metal-oxide films investigated in this work.

We previously explored a MO_x synthesis method based on a DUV light exposure, using a low-pressure mercury (Hg) source (UV253HR from *Filngen*), combined with a thermal post-treatment at 200 °C. We studied various curing parameters achieving good electrical TFT performances even after a short processing time of 5 min DUV plus 5 min at 200 °C. Then, we verified that when going below 200 °C for the post-treatment, longer processing times (> 90 min) are required to obtain satisfactory enough MO_x synthesis and yield performing TFTs. Therefore, we investigated an alternative DUV approach based on excimer light source and simultaneous substrate heating during the exposure, which could potentially enhance the effectivity of DUV treatment and therefore lead to a reduction of the thermal budget required.

Employing a Hg-based light source, in 2012 *Kim et al.* reported the necessity to provide heat during the UV exposure to trigger the photochemical reactions, highlighting that when heat is generated by the DUV exposure itself, the synthesis process requires prolonged exposure times.[118] The strong beneficial effect on the MO_x synthesis process of in-situ heating during DUV exposure was proven by *Park et al.*, using a Hg-based UV source combined with a hotplate, achieving AlO_x synthesis with a process as fast as 5 min at 150 °C.[120]

The same concept was applied later, involving excimer-based DUV sources for manufacturing semiconductor films in TFTs structures, mostly InO_x-based.[34,126,128,132] Notably, *Chae et al.* synthetized their InO_x on SiO_2 dielectric with in situ temperature of 140 °C, yielding after 15 min exposure mobility over 4 cm^2/Vs.[132] Instead, a limited number of publications regarding sol-gel IZO-TFTs treated via DUV excimer is available. *Leppaniemi et al.* reported spin-coated IZO cured via in-situ excimer treatment at 200 °C for 30 min, which yielded relatively low mobility of 1.3 cm^2/Vs.[126] Looking at the results achieved in the SoA and aiming for a further decrease of the thermal budget, we changed the DUV source for a more powerful excimer one (Xe_2 source) and integrated in-situ heat transfer in our DUV process approach. Conveniently, the excimer-based approach can be exploited to reduce the synthesis temperature for both MO_x-based semiconductors and dielectric.

The main differences between the systems are the emission spectrum and the relative irradiance. Figure 6.1 depicts the spectra of the two lamps exploited during our studies: the single peak emission of the Xe_2 at 172 nm limits the photonic dissipation and provides an irradiance of 65 mW/cm^2, whereas the Hg-based source, with a predominant peak at 253,9 nm but also various other minor emissions, can deliver an irradiance of 28-32 mW/cm^2. Interestingly, these photons with higher energy produced by the excimer can decompose the precursors and ease the undesirable removal by cleaving the organic bonds and reducing complex residuals in components that are simpler to remove.

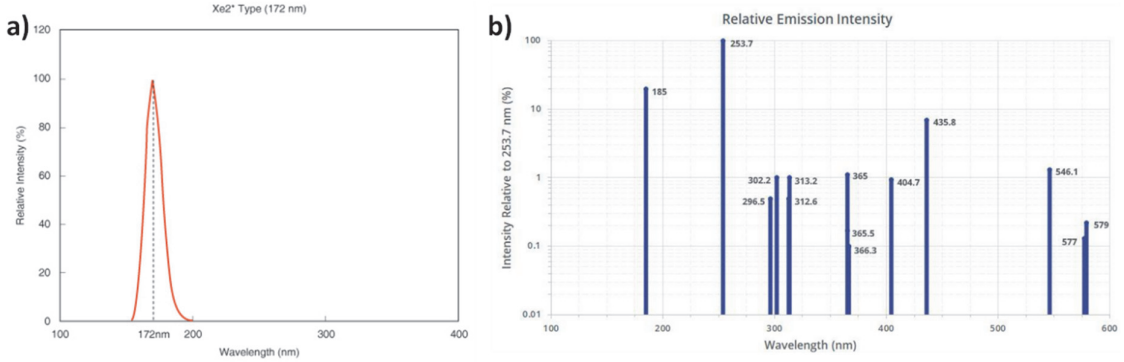


Figure 6.1 Emission spectra comparison between a) excimer Xe_2 source and b) low-pressure Hg source.

We built a setup (Figure 6.2) comprising an *L13129-C3* lamp from *Hamamatsu Photonics* with a Xe_2 excimer source, enclosed in a glove box. As the sample stage, we employed a movable hotplate with a heating capability up to 200 °C[26] that allowed a minimum

[26] The in-situ temperature of 200 °C was set as limit to preserve the lamp integrity.

distance for the exposure of 3 mm. The exposure occurred in an N_2 environment to preserve the equipment from damage due to possible ozone formation.

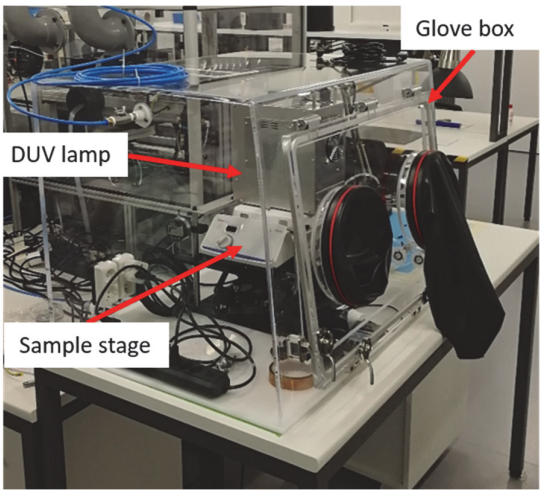


Figure 6.2 The excimer DUV system exploited for the in-situ synthesis of the metal-oxide dielectric and semiconductor films.

6.2 Inkjet printing of the metal-oxide functional layers

Chapter 2 provided a general introduction of the printing methods, whereas here, we focus on inkjet printing that was selected as deposition method for our MO_x semiconductor and dielectric, introducing its working principle and defining the relevant parameters necessary to deposit uniform layers with this technique. In this context, we will focus on aspects of the deposition of MO_x layers and the constraints on the chemical ink formulation linked to achieving performant TFTs synthesized at low temperatures are involved.

6.2.1 Inkjet printing fundamentals

Inkjet printing is a method based on a drop-on-demand (DoD) ink ejection process in which the ink is pushed through the small opening of the nozzle to form single droplets. It is a digital printing technique involving a large pool of adjustable parameters, like ink formulation and jetting waveform it owns design freedom and is cost-effective since it involves minimal material consumption and no printing plates. Moreover, the digital and non-contact nature of the method, the reasonable printing resolution (~30-40 µm), and the capability to deposit thin films make it a suitable candidate for the custom manufacturing of the next generation of cheap, disposable, and more sustainable electronics.

The digital image is converted into an electrical signal and sent to an actuator, ultimately generating the drops. Nowadays, different actuating systems for drop formation are available, such as piezoelectric, thermal, acoustic, and electrostatic. However, piezoelectric actuation is mainly used in printed electronics since it does not demand ink heating (up to the boiling point) and chemical additives as for the thermal actuation, commonly applied for printing colors.[227] The piezo-actuation applied to a vibration plate (i.e., a membrane) exploits the inverse piezoelectric effect to create pressure waves and form the drops. The drop formation occurs in three phases:

1. The piezo moves upward, the ink is sucked from the reservoir;
2. The piezo moves downward, pushing out the ink;
3. The piezo returns in a standby position, causing the liquid to break off and form the drop.

The shape of the drop can be tuned by modifying the shape and the voltage of the electrical signal (waveform) sent to the piezoelectric actuator. In Figure 6.3 is described the working principle for the drop formation for the piezo actuation system and a typical waveform employed.

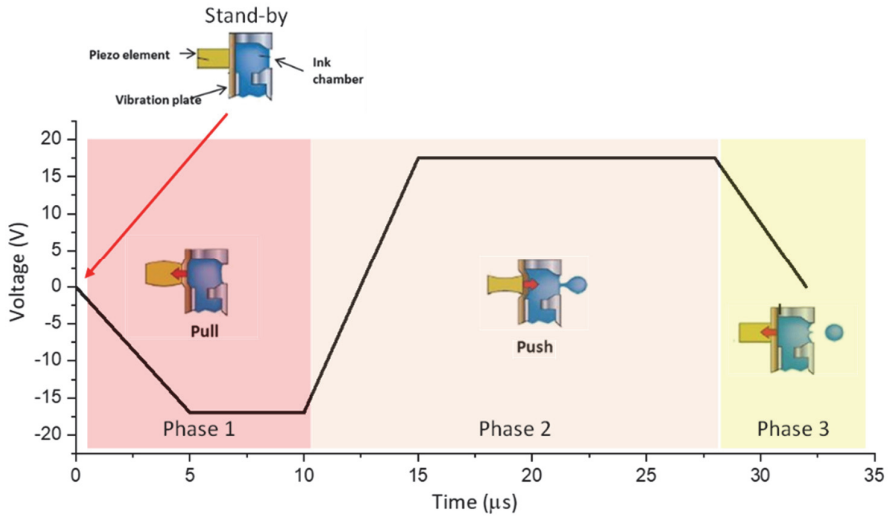


Figure 6.3 Drop formation principle for piezo actuators with the three phases and a typical waveform used. Adapted from [228].

Constraints in ink viscosity and surface tension are mainly related to the chosen system: inkjet systems have a relatively narrow viscosity window, generally 2 – 30 cP, due to the limited power generated from the actuator and a surface tension generally above ~20 mN/m. In this work, we employed a printing system based on Dimatix DMC disposable cartridges (DMC-11610, 1.5 mL reservoir, 10 pL drop volume, based on piezo actuation) from *Fujifilm.* The recommended ink rheological parameters for the DMC cartridges are 10-12 cP and 30-40 mN/m.

Ink chemistry has a primary role in inkjet printing. Ink properties define the drop formation and printing quality, not only the characteristics of the drops and the repeatability of the process but also the final layer morphology and, as we will discuss later, can influence the conversion of the metal-oxide precursor ink at low temperature. The ink comprises two main components: the base, with two main types of solvent used, aqueous and non-aqueous, and the additives. The base is the primary component of the ink, and in the case of metal-oxide precursors inks, the selected solvent has to ensure homogeneous dispersion of the precursors. As discussed in Section 2.4.1, we did not consider aqueous-based solvents as they can be highly reactive with the precursors[92] and present excessively low viscosity, which is not convenient for inkjet printing. Additives are also a crucial ink constituent: they can stabilize the inks, adjusting their physical properties to achieve desirable jetting or increase the shelf life. Among the various types of additives, we can find viscosity modifiers, surfactants, dispersants, pH modifiers, and chelating agents.

The proper drop ejection, interaction with the surface, and final printing quality are determined by two main rheological parameters: viscosity and surface tension.[229] Non-newtonian liquids can be printed but are generally not preferred due to the fluctuations in ink viscosity.[230] The viscosity of the ink can be modulated by modifying the ink concentration or adding modifiers like glycerol and ethylene glycol as co-solvents. Viscosity is also temperature-dependent; for this reason, most of the available printheads can operate at a variable temperature (up to 70 °C for disposable *Dimatix DMC* cartridges), which enables to tune the ink rheological characteristics. Surface tension has an influence on droplet formation and jetting. Values above 20 mN/m are generally necessary to achieve proper drop formation. High values (60 mN/m) prevent undesired ink flow from the nozzle but can cause its clogging; meanwhile, low surface tension ($\gtrsim$20 mN/m) results in inappropriate ink release forming a continuous ink flow or unstable drops.[65] Moreover, the ink could spread on the printing plate, creating a wet layer that could solidify, affect the drop trajectory or clog the nozzles.[229] The surface tension can be tuned by adding surfactants additives to the ink mixture.[231] Lastly, the surface tension of the ink will also influence the spreading of the ink on the substrate. However, ink spreading can be controlled by modifying the wettability of the substrate surface with the surface treatment processes involving notably oxygen plasma and DUV treatments.

Additional parameters, such as the nozzle diameter, the jetting waveform design, the printhead-to-stage distance, and humidity, have to be also considered as they can influence the final quality of the printing. Nozzle size influences the amount of ejected liquid, and the final drop dimension (typically ~30 µm for 10 pL DMC cartridges) ultimately affects the printing resolution while jetting voltage affects the drop speed, and the nozzle-stage distance can change the drop time-of-flight. Humidity instead can affect the ink composition, process repeatability, and in MO_x printing, influence the final material composition.

An ink printability can be evaluated by knowing its rheological parameters with the use of three dimensionless numbers: Reynolds (Re), Weber (We), and Ohnesorge (Oh). These dimensionless numbers represent the flow characteristics in terms of inertial forces and viscous forces (Re), inertial forces and surface tension (We), and viscous forces and surface tension (Oh). They can be calculated as follows:

$$Re = \frac{\rho u L}{\mu} = \frac{uL}{v}$$

Equation 6.1 Reynolds number.

$$We = \frac{\rho v^2 L}{\gamma}$$

Equation 6.2 Weber number.

$$Oh = \frac{\mu}{\sqrt{L\gamma\rho}} = \frac{\sqrt{We}}{Re} = \frac{1}{Z}$$

Equation 6.3 Ohnesorge number.

Where ρ= density of the ink [kg/m^3], γ = surface tension of the ink [N/m], μ= dynamic viscosity of the ink [Pa·s][27], u = speed of the droplet [m/s], L = characteristic length [m], and v = kinematic viscosity of the ink [m^2/s]. The characteristic length *L,* in the case of inkjetting with Dimatix disposable cartridges, is generally reported as 20 µm, close to the nozzle diameter (21.5 µm for *DMC* cartridges).

Z-number is a dimensionless number, reciprocal of Oh, which is often used to evaluate the printability of an ink. In previous studies, the ink printability was analyzed according to the Z-number and the range that provides the optimal printing conditions identified, generally being $1 \leq Z \leq 10$.[232–234] For $Z < 1$, the viscosity of the ink is generally too high for jetting, while when $Z > 10$, it results in unstable satellite drop formation. In Figure 6.4, the inkjet operating window is reported as a function of Oh and Re. In the graph is represented the influence on drop formation of several combinations of rheological parameters, while are also provided two examples of drop formation for inks with different Z-number.

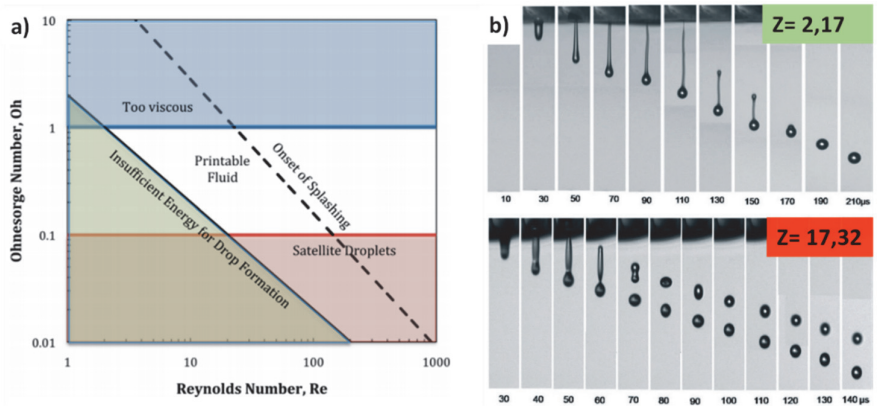


Figure 6.4 a) A schematic diagram showing the operating regime for stable operation of inkjet printing.[235] b) Representative photo sequence of the drop formation from two fluids with a suitable (in green) and improper Z-number (in red).[232]

6.2.2 Low-temperature processing of printed MO_x layers: challenges and requirements

Selecting the correct ink formulation is a process that considers ink rheology and ink compatibility according to the chosen printhead and the nature of the substrate/layer onto which the material will be deposited. Besides these general guidelines, printing metal-oxide films to be integrated into a TFT architecture presents additional challenges and requirements.

[27] It is often reported in centipoise (cP), a unit of the CGS system, where a 1 cP = 1 mPa·s.

6.2.2.1 Challenges in MO_x layer deposition for TFTs

In TFTs, the thickness and the uniformity of the deposited functional layers are crucial parameters. For example, a dielectric that does not present uniform thickness affects the operational uniformity of the devices and may cause failures (V_{Th} and $V_{breakdown}$ are thickness dependent). Moreover, these films have to be thin (tens of nanometers) to achieve high electrical performances, notably low sub-threshold swings for fast switching. The concentration of the precursor ink is the main parameter to control the final thickness of a MO_x film. At the same time, the optimization of the printing process can provide a uniform deposition and help in tuning the layer thickness (notably, number of jetting nozzles, drop spacing, number of layers deposited). Once printed, the deposited layer undergoes thermal processes, drying and annealing, converting the liquid ink into a solid layer. The single drops and the final dry layer may experience an inconstant thickness caused by a not uniform distribution of materials over the extent of the deposited film, resulting in a higher concentration on the edges. This inhomogeneity in the dry layer is known as the "coffee ring" effect. In solutions with suspended particles, a higher evaporation rate at the edge of a drop leads to a convective flow from the center to the edge, ultimately accumulating the particles in that area.[236] An ink engineering needs to be performed in order to control and prevent this effect. A solution to this problem is the exploitation of the so-called Marangoni effect: it creates fluid flows in the opposite direction of the outward flow driven by the differential drying, thus uniforming the particle distribution in the drop/layer preventing local accumulation. The Marangoni effect can be achieved by using a solvent mixture composed of solvents with different vapor pressures and surface tension: the component with high vapor pressure evaporates preferentially at the drop edge, with a localized decrease of surface tension that generates a gradient to the center of the drop, ultimately generating an inward convective flow that homogenizes the concentration of the particles.[237–239] Parameters such as the printing stage temperature can also influence coffee ring shapes. *Dou et al.* reported that despite the presence of co-solvent in the water-based mixture, if the plate temperature is high enough (in their case was > 35 °C), it can induce diffusion phenomena in the drops that reduce the concentration gradients in the liquid responsible for the Marangoni flow, thus provoking coffee ring.[240] Therefore, depending on the solvent system involved, a proper stage temperature must be found to minimize coffee ring formation and achieve uniform layers. Figure 6.5 depicts the Marangoni flow principle and the effect of plate temperature on the drop shape.

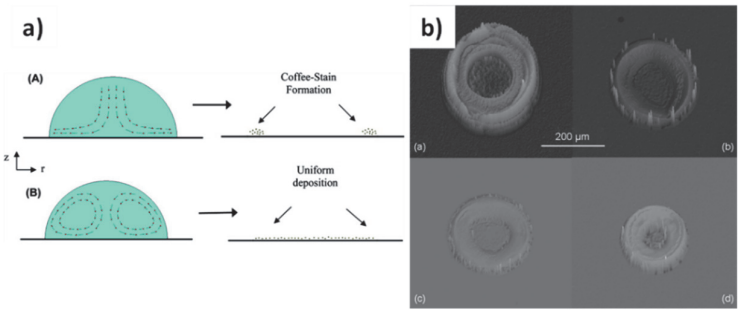


Figure 6.5 Coffee ring effect. a) Exploitation of Marangoni flows to overcome it.[239] b) Inkjet-printed drops of a ZrO_2 ink (water-based ink with 10% of ethanol) printed onto a glass surface heated to (a) 25 °C, (b) 35 °C, (c) 50 °C, and (d) 100 °C.[240]

Multiple layer stacking is another major challenge for printed MO_x TFTs. Achieving an interface between semiconductor and dielectric with minimal roughness that limits scattering events is mandatory to ensure the performing devices. Moreover, chemical compatibility between the materials composing the layers and the solvents in the inks employed must also be ensured. Table 6.1 reports the literature involving TFTs with printed semiconductors processed at temperatures ≤ 200 °C. Most of the reported papers on printed MO_x TFTs involve one printed layer, often the semiconductor deposited on classic Si/SiO_2 substrate-gate/dielectric system. To the best of our knowledge, only a report about printed dielectric and semiconductor annealed at temperatures below 250 °C was published in 2020 by *Carlos et al.*. They showed TFTs on PI substrate with inkjet-printed InO_x/ flexographically-printed AlO_x semiconductor/dielectric stack processed at 180 °C via excimer DUV, which yielded mobility ~2.9 cm^2/Vs after exposing the InO_x semiconductor for 90 min.[59]

Table 6.1 Literature on TFTs with printed MO_x semiconductor, processed at T ≤ 200 °C.

Semiconductor material	Dielectric material	T_{max} (°C)	Process duration (min)	μ (cm^2/Vs)	Ref.
IGZO	SiO_2	200	N.A.	1.5	[69]
IZO	SiO_2	200	60	0.4	[70]
InO_x	AlO_x	180	90	2.8	[59]
InO_x	ALD Al_2O_3	150	180	~1	[34]
ZnO	SiO_2	150	N.A	< 10^{-3}	[241]
IGZO	Polymer+ALD	120	N.A	4.2	[133]

6.2.2.2 Ink requirements for printed MO_x processed at low-temperature

The low thermal budget approaches, such as DUV or excimer DUV, provide a limited amount of energy to the deposited precursor inks, and the quality of the final layer can be affected by the amount of high boiling point co-solvent in the layer. For these reasons, during the tuning of the ink formulation to obtain the proper rheological characteristics, the requirements related to the low-temperature processing should be accounted, and the fraction of co-solvents with high boiling points kept as low as possible to ease the solvent removal.

Therefore, to achieve uniform MO_x printed layers synthesized at low temperature, avoiding the coffee ring effect and yielding suitable precursor conversion, the ink formulation should be:

- chemically compatible with printing system and previously deposited materials;
- satisfy the rheological requirements for a stable jetting;
- limit to the minimum the amount of high boiling point compounds that may compromise the low-temperature synthesis.

This combination of requirements, together with the challenges related to the manufacturing process, has restrained the amount of literature regarding printed MO_x TFTs at low temperatures.

6.2.3 Approach to the solvent formulation for MO_x inkjet ink

We have seen that mono-solvent inks generally suffer from the coffee ring effect, preventing the deposition of uniform layers. Moreover, the solvent applied in this work, 2ME, presents rheological characteristics not suited for stable and repeatable jetting, owing to the low viscosity of ~1.6 cP. The ink formulation can be adjusted in two ways: increasing the solute concentration or modifying the solvent mixture by choosing co-solvents with higher viscosity.

Solvent modification with more viscous co-solvents is commonly employed as a successful method to tune the ink rheology and limit the coffee ring effect. Regarding printing metal-oxide films, *Matavž et al.* studied a combination of glycerol and 1-3-propanediol as co-solvent for 2ME that ultimately resulted in stable jetting and allowed them to print tantalum oxide dielectric layers successfully.[242] A similar approach involving 2ME and co-solvents such as ethanol, ethanolamine, and ethylene glycol, was described by *Dang et al.* to improve the printability of their inkjet-printed silver structures.[243]

Among the various co-solvent available, ethylene glycol (EG) is frequently reported. *Jeong et al.* studied in 2011 the role of EG fractions (up to 30 %) in a 2ME-based IGZO semiconductor ink: their printed IGZO on SiO_2/Si was annealed thermally at 400 °C for 30 min, and they observed a correlation between TFT performances and EG fractions. Notably, their best mobility of ~4.9 cm^2/Vs, reported for 20 % in EG, was attributed to a reduced amount of hydroxides and oxygen vacancies in comparison to TFTs with EG fractions lower than 20 %.[244] More recently, *Leppäniemi et al.* studied the role of the EG (up to 30 %) in a mix with 2ME for the printed InO_x semiconductor. They deposited the InO_x ink onto SiO_2/Si substrates and annealed it at 300 °C for 30 min and reported their best performances for 5 % EG instead, with mobility ~4 cm^2/Vs that ultimately decreased for higher percentages of co-solvent, ~0.3 cm^2/Vs at 30 % EG. They eventually chose a 10 %/90 % EG/2ME composition, which provided a good compromise of printability and electrical performance.[34]

On our side, ethylene glycol as co-solvent was a natural choice (viscosity = 16 cP) as already employed in the dielectric ink and thus compatible with our 2ME-based semiconductor solution. The role of EG fractions in IZO based semiconductors 2ME/EG inks has never been studied, and the few studies involving MO_x semiconductors exploited thermal processes at relatively high temperatures, such as 300 °C or 400 °C. Such temperatures are higher than the boiling point of the mixtures ($T_{B,\,EG}$= 197 °C; $T_{B,\,2ME}$= 124 °C), ensuring the evaporation of the solvents involved and generally providing sufficient energy to remove the reaction residuals and convert the precursors, thus yielding operative TFTs. However, since we are targeting approaches below 200 °C, close to the mixture boiling temperature, solvent removal, and MO_x conversion can be highly affected by the ink chemical composition. Considering the same amount of the two solvents, as EG possesses higher T_B than the 2ME, it requires more energy to be evaporated.

The following sections will describe the investigated aspects and our work on manufacturing printed MO_x TFTs via a low-temperature approach.

6.3 Printing of active layers for MO_x TFTs

This section describes the aspects of printing via inkjet of the MO_x semiconductor and dielectric addressing their synthesis applying an in-situ excimer/heat protocol at low temperature (< 200 °C).

As stated in Chapter 5, the AlO_x/$YAlO_x$ dielectric developed at EMPA was successfully printed, and their synthesis process was based on a DUV-enhanced approach at 200 °C (45 min DUV + 60 min at 200 °C). Targeting a reduction of the thermal budget required for the whole processing of the TFTs, we studied the implementation of a DUV excimer protocol to the synthesis of this dielectric layer as well as to the IZO semiconductor film. First, we focused on the transfer of the printing process of the MO_x dielectric stack to our Ceraprinter inkjet platform, optimizing the printing process and studying the effects of various parameters, such as printing geometry, printing direction, and nozzle number on the morphology and dielectric characteristics of the printed layers. Afterward, we investigated the effectiveness of the excimer synthesis protocol on the dielectric layer and tested on MIM capacitors variable in-situ temperatures, from 130 °C to 180 °C for a constant duration of 20 min. The leakage I-V tests demonstrated that an in situ DUV excimer could synthesize the MO_x dielectric even at temperatures below 150 °C.

We then focused on the IZO layer: differently from the dielectric, we observed that the presence of ethylene glycol (EG) as a co-solvent in the precursor ink negatively impacted the synthesis at a low temperature of the MO_x and the electrical performance of the resulting TFTs. The experiments showed that employing an ink similar to the one exploited for the dielectric, 50 %/50 % EG/2ME, results in a drop of TFTs performance when annealed via DUV excimer at 180 °C with respect to TFTs treated with the thermal process (30 min at 350 °C). The EG has a higher boiling point than 2ME ($T_{B,\,EG}$= 197 °C; $T_{B,\,2ME}$= 124 °C) and consequently requires more energy to be removed. Therefore, we studied the printability of different solvent/co-solvent combinations by varying the EG fraction, mainly linked to a viscosity variation as a function of the ink composition. Then, we exploited these inks to manufacture TFTs and investigated different synthesis temperatures, from 190 °C down to 160 °C, to correlate the EG percentage with the electrical parameters of the TFTs. As an outcome, we identified 10 % EG as the best concentration to use with 2ME in terms of printability and final electrical performance. As a further step, we investigated multiple methods to improve the quality of the printed layers, modifying the printing parameters, such as the number of printed layers, drop spacing, and printing direction. In this context, we also explored the possibility of increasing the ink viscosity by raising the precursor concentration to 0.5 M, improving the jetting stability.

Ultimately, we combined the two printed functional MO_x films layers to manufacture TFTs on a silicon substrate. We manufactured TFTs with a thermally annealed printed stack that exhibited satisfying electrical performances comparable to previously reported TFTs with thermally annealed printed IZO semiconductors and both MO_x layers printed. Afterward, we synthesized the printed MO_x layers stack via the in-situ DUV excimer treatments developed to fabricate printed TFTs at a lower temperature. However, the electrical performances did not meet the expectations, notably high leakage and relatively low yield, suggesting that further process optimization is still required. As the low-temperature processed TFTs with fully printed active stack suffered from low yield and excessive leakages, we investigated some of the possible causes of this behavior: the role of the intermediate wetting enhancer step performed before semiconductor deposition (O_2 plasma at 300 W for 5 min), and the effect of different humidity levels during the fabrication process. We compared various treatments and verified that it does not negatively influence the performance of the dielectric layer and its interface with the semiconductor.

6.3.1 Printing system: Ceraprinter F-serie

Here we introduce the printing system used to print the metal-oxide films by inkjet. We employed the *CeraPrinter F-Serie* from *Ceradrop* located at EPFL-LMTS in Microcity, Neuchâtel, depicted in Figure 6.6. It is an “all-in-one” deposition platform designed to develop printed electronics and equipped with both deposition and curing accessories. IR and UV lamps are integrated for post-processing treatments. The printing stage has a 305 mm x 305 mm area, which can be heated up to 60 °C, and possesses a motion accuracy of $\lesssim$1.5 µm that allows a printing resolution of less than 5 µm x 5 µm.

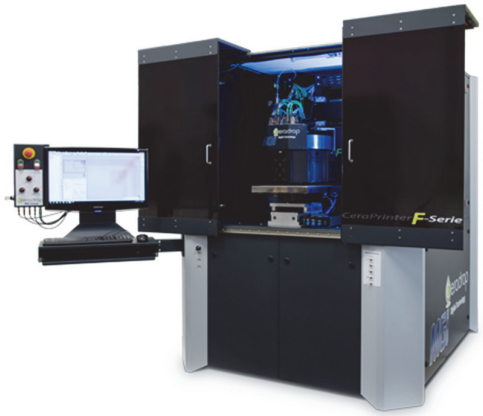


Figure 6.6 Ceraprinter F-serie.

The system presents three different interchangeable print-heads for deposition of a wide range of functional inks via inkjet and aerosol jet, for the latter with an ultrasonic or a pneumatic atomizer and shutter below the nozzle to control the deposition location.

- The inkjet module is equipped with disposable *DMC* Dimatix cartridges (1-16 nozzles, 10 pL) with a maximum printing resolution of ~30 µm, depending on the drop volume.
- The ultrasonic aerosol module can jet solutions with a viscosity below ~10 cP, exploiting circular nozzles with dimensions varying from 100 µm to 300 µm, thus enabling a printing resolution down to ~10 µm for by ultrasonic aerosol jet with an optimized process and ink.
- For a large-area coating, the pneumatic aerosol module can jet inks with a viscosity ranging from 1 to 1000 cP, wide circular and rectangular nozzles, with orifice sizes varying from 1000 µm to 3000 µm.

The printer software is composed of three modules: Ceraslice, Dropanalyser, and Fabanalyser.

6.3.1.1 Ceraslice

Ceraslice is the Ceradrop printer CAD software used to import external digital files, draw objects and design the filling patterns. The software is valid for all the different printing systems, with minor changes between aerosol jet and inkjet related to the nature of their jetting, continuous and drop-on-demand jetting, respectively. Here we will discuss only the aspects related to inkjet. Ceraslice offers a wide range of possible parameters that can be exploited to optimize the printing quality, from the filling pattern (lattice type, printing direction, filling strategy) to the printing direction (x-axis or y-axis, in both positive or negative directions). The system includes the possibility to print with a various range of lattices, depicted in Figure 6.7: square, square centered, centered DECA hexagon, centered FAB hexagon, rectangular, and centered rectangular. While “efab” and “eshift” are fixed parameters defined by the lattice selected, two main parameters have to be selected to ultimately define the drop density (DPI) of the pattern: drop splat (D_s) and drop overlap (D_o). The DPI, which eventually is determined from the drop-to-drop distance (D_d), is a primary parameter to define the thickness of a printed layer as it defines the amount of material deposited.

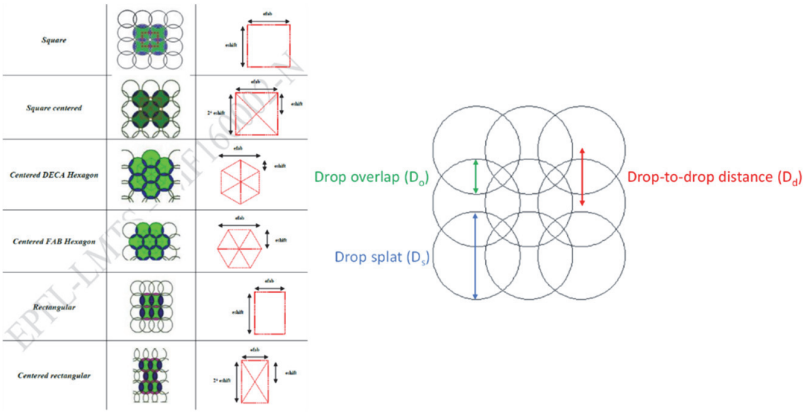


Figure 6.7 Printing lattices and relevant parameters for inkjet printing with the Ceraprinter.

As depicted in Figure 6.7, the drop splat represents the dimension of the drop on the surface, while drop overlap is the overlap between two adjacent drops. Therefore, once identified D_s (depending on ink formulation and surface treatment), one can implement the desired DPI by choosing the corresponding D_o with the following formula:

$$D_s - D_o = D_d$$

Equation 6.4 Drop-to-drop distance calculation for DPI evaluation.

We report some D_d examples and in parenthesis, the relative DPI: 256 µm (100 DPI), 128 µm (200 DPI), 80 µm (300 DPI), and 63 µm (400 DPI).

6.3.1.2 Dropanalyser

Dropanalyser is an advanced analysis software for droplet jetting. It is exploited during the waveform design to evaluate how different waveform affects the jetting quality and the shape of the drops. The software allows to address the nozzles of the printhead singularly and modify their waveform to achieve uniform jetting with multiple nozzles. The embedded tool called "ejection report" can automatically analyze all the relevant parameters of the jetting, such as drop speed, drop volume, or drop tilt angle.

In the frame of waveform design for optimal jetting, we targeted waveforms capable of producing:

- well defined single drops;
- with no satellites;
- drop speed of 6-7 m/s;
- minimal ejection angle for straight drops.

6.3.1.3 Fabanalyser

Fabanalyser is the part of the software related to the fabrication: it is employed to verify and analyze the quality of a deposited pattern. After printing, we exploited it to preliminary observe the pattern, to identify possible defects or non-uniformities in the wet layers. The pictures of the wet layers are collected during this step. Figure 6.8 depicts an image collected via Fabanalyser: here, we can observe an example of a wetting issue during the successive deposition of the two dielectric layers.

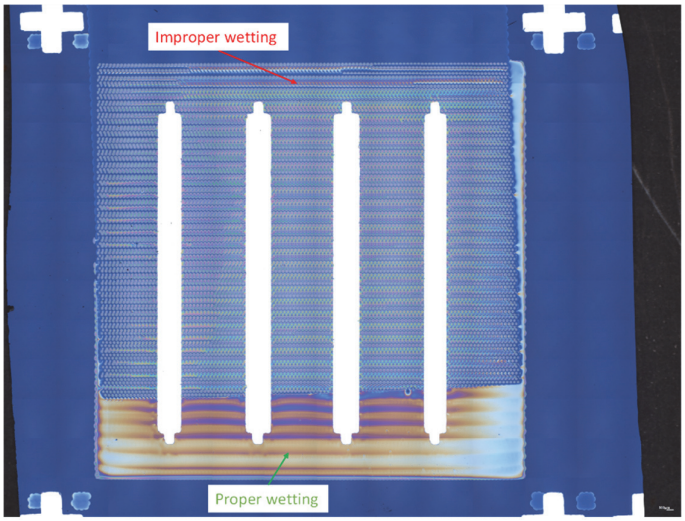


Figure 6.8 Image collected via Fabanalyser. An example of an observed issue related to the non-uniform wettability of the layer.

6.3.2 Printing of $AlO_x/YAlO_x$ dielectric stack

For the $AlO_x/YAlO_x$ printing process, we decided not to modify the ink formulation, developed by our partners at Empa, a 0.2M $YAlO_x$ and a 0.4 M AlO_x, based on yttrium nitrate ($Y(NO_3)_3{\cdot}6H_2O$) and aluminum nitrate ($Al(NO_3)_3{\cdot}9H_2O$) precursors, dissolved in equal fractions of EG and 2ME for the $AlO_x/YAlO_x$ printing process, since they demonstrated its satisfactory inkjetability. Starting from this formulation, we developed a jetting waveform and then optimized the printing by exploring the capabilities of the printer and investigating the effects of parameters such as stage temperature and duration of the surface treatment by plasma on ink printability. We employed SiO_2/Si chips as the substrate for these studies exploited as substrate in most of the TFTs reported in the following sections.

(The different colors of the substrate, like blue and yellow, are due to SiO_2 layers with different thicknesses used for printing tests.) For the TFTs with a fully printed stack with patterned gates, SiO_2 is used as the insulating passivation layer of the Si substrate. The thin evaporated metal (35 nm), used as a gate, does not influence the morphology of the printed layers.

We used a "test pattern" (Figure 6.9) composed of two lines of single drops (15 mm), exploited to measure the size of the drops D_s and adjust the drop overlap D_o, and four different squares (5 x 5 mm) characterized from a varying resolution: 100, 200, 300, and 400 DPI. This pattern was used in various experiments to evaluate the quality of the printed structures as a function of the tested parameter.

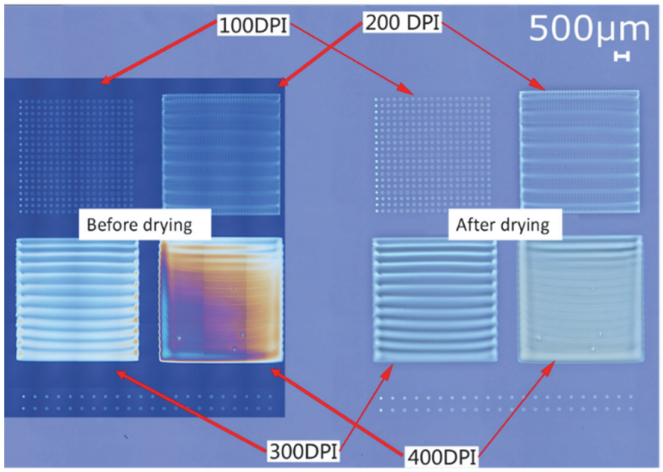


Figure 6.9 Example of test pattern exploited to evaluate the quality of the printed layers as a function of the tested parameters.

We started by developing jetting waveform suitable for the two dielectric $YAlO_x$ and AlO_x inks. This step was performed employing the Dropanalyser software and the ejection report. The images collected using Dropanalyser bear valuable information on the drops, such as their position, volume, and diameter, which help evaluate the jetting quality. Starting from waveforms reported elsewhere using the same printing platform,[79] we developed our waveform valid for $YAlO_x$, then adapted it for the other dielectric ink. Figure 6.10 reports the waveform used to print both dielectric inks and images of the drops formed while printing. The nozzle temperature was kept at 28 °C during the ejection, and despite the different ink concentrations of precursors in the dielectric inks, 0.2 M and 0.4 M, no change in the jetting waveform was required.

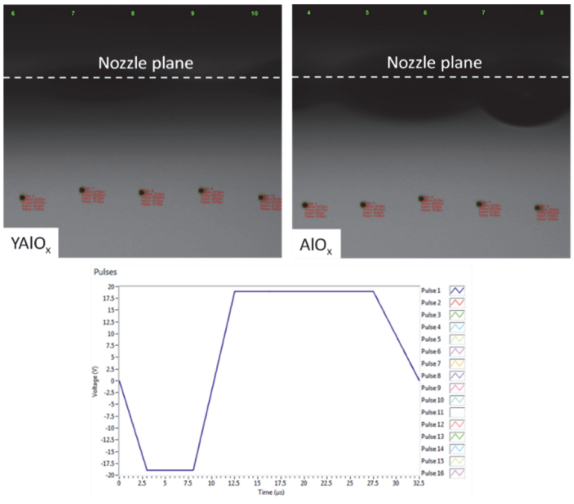


Figure 6.10 $YAlO_x$ and AlO_x inks printing: typical jetting waveform and drop appearance.

As the first step before printing, a surface treatment via O_2 plasma is performed to modify the surface energy and improve the substrate wettability. To optimize the printing, we first studied the effect of different O_2 plasma durations on the wettability of our ink. Figure 6.11 shows the wettability of the ink as a function of variable O_2 plasma (13.56 MHz, power of 300 W) treatment time

from 0 to 6 minutes, maintaining constant the stage temperature at 35 °C. In Figure 6.11a, we can see how the surface, if not treated with O_2 plasma, is predominantly hydrophobic, and the single drops cannot correctly coalesce even at a high drop density. Similar behavior is visible in Figure 6.11b, for which a short treatment of 2 minutes was applied. High-density patterns (300 and 400 DPI) show drop coalescence already after 4 minutes of treatment and a slight ink overflow, whereas after 6 minutes of treatment, the 200 DPI square shows a uniform layer. It is worth mentioning that the pictures in Figure 6.11 are collected just after the printing with Fabanalyser, and the solvent in excess (e.g., 400 DPI in Figure 6.11d) is removed during the annealing step without particular consequences on the layer morphology. As a result of the study, we identified a minimum plasma treatment (300 W, 13.56 MHz) of 5 minutes to ensure the proper surface wettability.

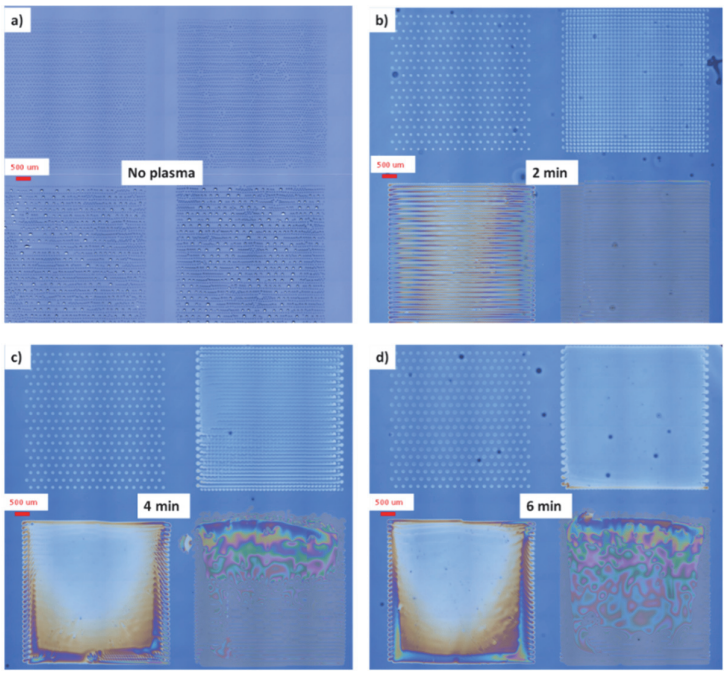


Figure 6.11 Effect of variable duration of the O_2 plasma treatment on printed structures. 0.2 M $YAlO_x$ printed on SiO_2/Si substrate treated, prior printing with variable O_2 plasma (300 W, 13.56 MHz) duration: a) 0 min, b) 2 min, c) 4 min, and d) 6 min. Images were acquired with Fabanalyser immediately after printing.

Then we investigated the effect of stage temperature on the morphology of the printed layers. Since the drops start drying when they touch the surface, this is an important parameter to control, ensuring that the desired uniform layer can be formed and that the stage temperature is appropriately set to not induce coffee ring formation. As discussed previously, higher temperatures can create diffusion fluxes in the single droplets, ultimately counterbalancing the ones generated by the Marangoni effect and leading to coffee ring formation. To find the optimum stage temperature, we varied it from 35 °C to 60 °C and compared the effects on the printed layers. Figure 6.12 shows the testing pattern printed at different stage temperatures. Despite prolonged plasma treatment, due to fast evaporation rates at temperatures ≥ 45 °C, the ink spreading is reduced, resulting in non-uniform layers composed of stripes.

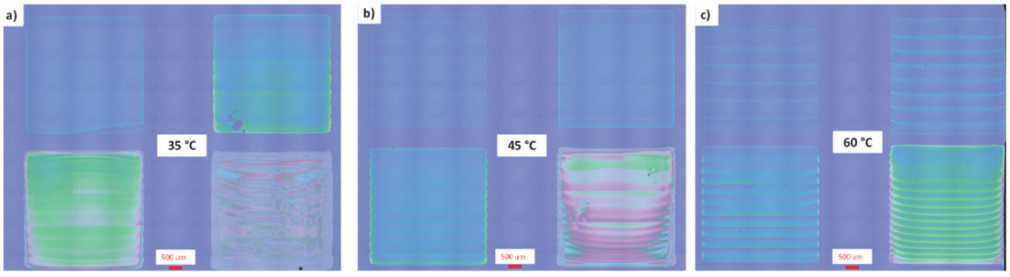


Figure 6.12 Effect of printing stage temperature on layer formation. 0.2 M $YAlO_x$ printed on SiO_2/Si substrate treated, for 5 min with O_2 plasma (300 W, 13.56 MHz), with the stage temperature increasing from left to right, respectively a) 35 °C, b) 45 °C, and c) 60 °C. Images were acquired with Fabanalyser immediately after printing.

As expected, the temperature of the stage impacts the formation of the coffee ring on the single drops. In Figure 6.13, we can observe AFM profiles of single drops of $YAlO_x$ deposited on SiO_2 substrates at different temperatures. The samples are afterward dried for 10 min at 90 °C. The highest temperature resulted in an approximately 15 um-wide coffee ring on the drop edge, whereas the drops deposited on a stage heated at 45 °C and 35 °C showed fewer thickness non-homogeneities. From the shape of the different drops and layers manufactured, we decided to implement a $T_{stage} \leq 35$ °C as it presents coffee ring-free drops and results in uniform layers.

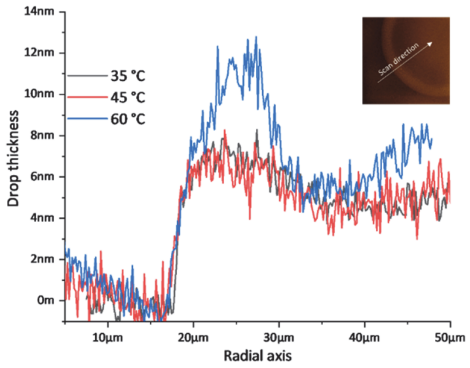


Figure 6.13 $YAlO_x$ drop profile as a function of T_{stage}. The profiles have been obtained via AFM. The concentration of the ink was 0.2 M (50 % EG,50 % 2ME).

The possibility of addressing each nozzle of the printhead singularly and modifying its waveform allows us to obtain uniform jetting from multiple nozzles. *Scheideler et al.* previously reported differences in the quality of the layer, notably drops not coalescing, when only one nozzle was employed in comparison with multiple nozzles.[79] Therefore, the effects of this parameter were verified by evaluating the quality of printed layers obtained with single and multiple nozzles. Figure 6.14 depicts four squares with a drop density of 200 DPI and the same printing parameters like waveform, ejection frequency (2 kHz), and stage temperature (35 °C) with a different number of nozzles. We did not observe significant differences when a single nozzle or multiple nozzles were employed; therefore, we chose to print using multiple nozzles to diminish the total processing time.

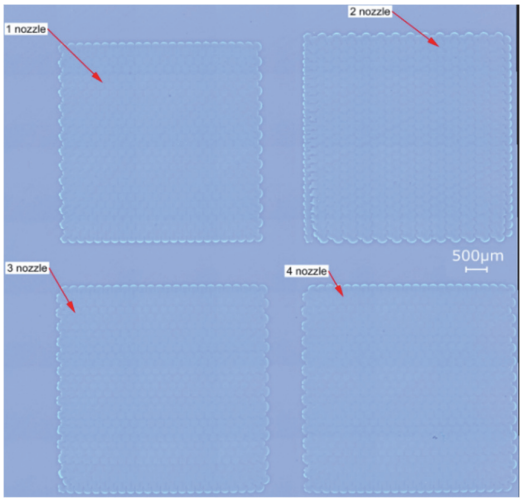


Figure 6.14 Evaluation of single and multiple nozzle printing. The image, taken with an optical microscope, provides a qualitative idea of the layer morphology variation as a function of the # of nozzles. No significant differences were visible.

As mentioned earlier, the Ceraslice software offers considerable process flexibility in pattern designing. Among the possible parameters, we have evaluated how the printing direction affects layer uniformity. In this frame, we tested positive and negative x-direction and positive y-direction, as depicted in Figure 6.15. The main difference in printing on the x- or y-direction is the printer section that moves: when we print on the x-direction, the printhead moves and the stage is fixed, while it is opposite when the printing occurs in the y-direction. We did not observe relevant differences using the three different methodologies, demonstrating that the printing stage and printhead possess precise motion. In the squares printed at 400 DPI, it is noticeable an ink overflow and relative

accumulation. However, it does not affect the devices as their fabrication will be located in the middle area of the printed structure that is instead uniform.

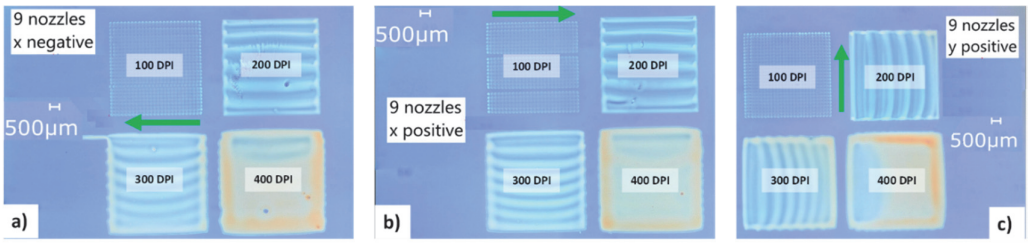


Figure 6.15 Study on the printing direction. Optical images of dried squares where a), b), and c) represent, respectively, patterns printed (single pass, 100–400 DPI, with # nozzles = 9 in the negative x-direction, positive x-direction, and positive y-direction. The green arrows in the pictures show the printing direction. (0.2 M $YAlO_x$ printed on SiO_2/Si substrate)

As an outcome of the optimization process, we identified optimum printing parameters for the dielectric inks with 50%/50 % EG/2ME:

- $YAlO_x$ 0.2 M and AlO_x 0.4 M;
- 28 °C nozzle temperature, stage temperature of 35 °C
- # nozzles ≥4, square lattice, printing along the positive x-direction.

Whereas the process flow for the printed dielectric AlO_x/$YAlO_x$ stack on SiO_2/Si substrates, exploited in most of the structures described afterward, is as follows:

- 5 minutes of O_2 plasma at 300 W,13.56 MHz;
- printing at 400 DPI;
- Drying (10 min at 90 °C on a hot plate in an air ambient);
- Intermediate annealing (20 min in-situ DUV excimer treatment at the same temperature as the final annealing);
- 5 minutes O_2 plasma at 300 W,13.56 MHz;
- AlO_x printing at 400 DPI;
- Drying (10 min at 90 °C on a hot plate in an air ambient);
- 10–30 min in-situ DUV excimer treatment at a variable temperature (130–180 °C).

Using these parameters and process flow, it was possible to achieve uniform printing of the double dielectric layer over a relatively large area. Figure 6.16 shows an example of a 25 mm x 25 mm square of printed AlO_x/$YAlO_x$ dielectric. The layers, both printed with 400 DPI, are deposited over a SiO_2 substrate presenting patterned metal lines exploited as a bottom electrode for the printed structures. The Al metal gates (35 nm thick) do not influence the printing quality. In Figure 6.16a is reported the $YAlO_x$ after drying and soft baking, while in Figure 6.16b is represented the final dual-layer stack after being dried. We examined via AFM the roughness of the printed dielectric stack (Figure 6.17) and verified that smooth layers with a root mean square roughness of < 1 nm could be obtained.

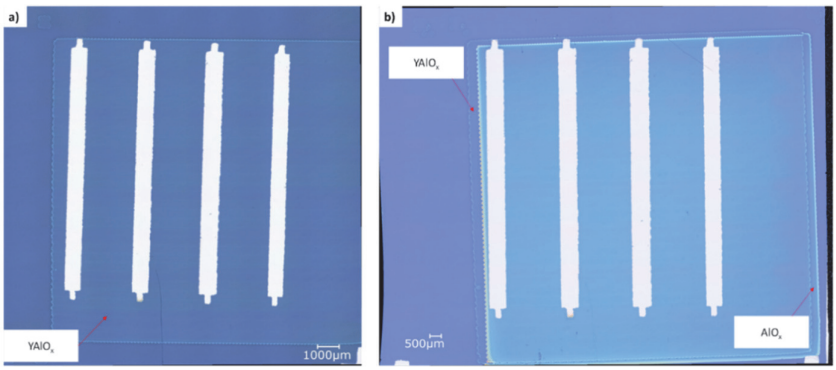


Figure 6.16 Example of a printed dielectric stack after process optimization: a) $YAlO_x$ and b) AlO_x/$YAlO_x$ stacked on SiO_2/Si substrate with patterned Al structures exploited as gate contacts.

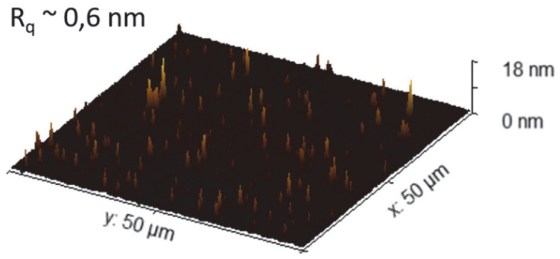


Figure 6.17 Surface analysis via AFM of the AlO_x on top of the printed dielectric stack after in-situ DUV exposure. (R_q~ 0.6 nm)

Via AFM, we also have checked the typical thickness of the layers, which resulted in ~10 nm for the $YAlO_x$ and ~30 nm for the AlO_x, ultimately yielding a total thickness of 40 nm, similar to the one reported in Chapters 4 and 5 with dielectric layers printed with the *Meyer Burger* PixDRO LP50 printer at EMPA.

6.3.2.1 Excimer curing of the dielectric layers

Once established the printing protocol, we focused on the dielectric synthesis via DUV excimer treatment. For this purpose, we manufactured MIM capacitors with a printed AlO_x/$YAlO_x$ treated with in situ DUV excimer at a variable temperature and tested the dielectric performance. Since a minimized electrical leakage is essential for performing TFTs, we measured the leakage current density and compared the statistical results (n≥4) obtained at an electric field of 1 MV/cm. We used aluminum-coated glass as a substrate and deposited the layers following the process flow described in the previous section. The proper printing quality was maintained despite passing from Si substrate to Al-coated glass. As final annealing, the samples were subjected to DUV excimer exposure for 20 minutes at temperatures varying from 130 °C to 180 °C. Afterward, aluminum pads were evaporated using a magnetic shadow mask, resulting in capacitors with an area of 0.01425 cm^2. Figure 6.18 depicts the leakage measurements obtained from different samples at a variable in-situ temperature.

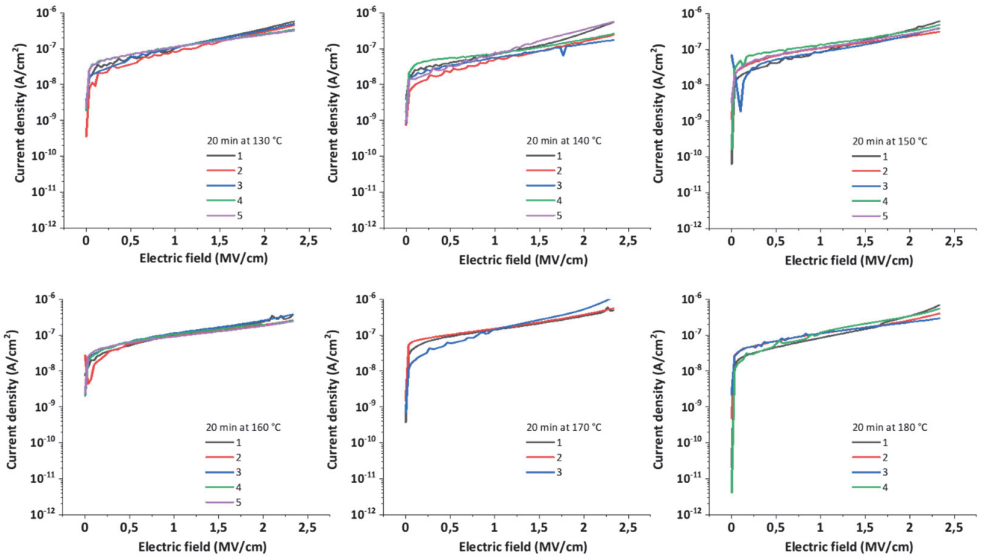


Figure 6.18 Leakage current measured from various MIM structures on glass (Al electrode/ Printed AlO_x-$YAlO_x$/ Al electrode) with an area of 0.01425 cm^2, as a function of the applied in-situ temperature during excimer exposure.

Figure 6.19 shows an optical image of the realized devices with relative cross-section and the statistical results of the leakage density at 1 MV/cm. The behavior of the current leakage density is relatively uniform for each curing protocol showing a current level in the order of 10^{-7} A/cm^2, which is only one order of magnitude higher than the one reported by *Bolat et al.* using a similar printed dielectric and a DUV curing protocol at 150 °C.[135] Surprisingly, no significant differences were observed in the behavior of the MIMs excimer treated at different temperatures, suggesting that with the selected protocol of 20 min and no post-treatment, the temperature applied during the in-situ treatment did not influence the process outcome. A deeper investigation on the effect of process parameters, like treatment duration, on the material, such as XPS or density measures, would help in understanding the role of the synthesis parameters on the final MO_x dielectric. Moreover, possible post-treatments (i.e., thermal post-annealing on a hotplate) could further

improve the quality of the dielectric layer. The results show the effectiveness of the DUV excimer synthesis protocol for this double layer $AlO_x/YAlO_x$, which lasts only 20 minutes and can be efficacious at temperatures as low as 130 °C.

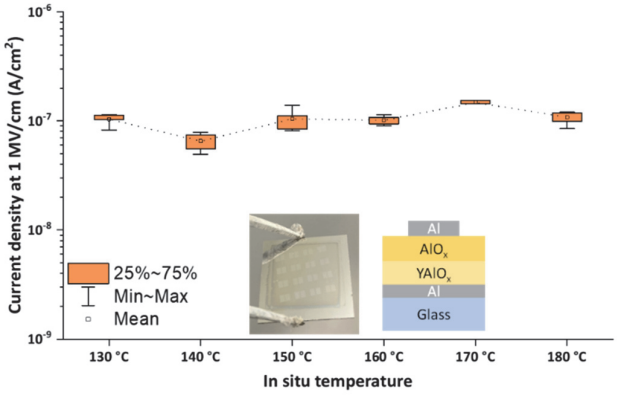


Figure 6.19 MIMs on glass with printed dielectric synthesized via in-situ excimer (20 min at 130 – 180 °C). Statistical analysis (n≥4) of the leakage current levels, at 1MV/cm, as a function of the in-situ temperature. (Box representing the 25 – 75 % of the results achieved, the error bars are linked to the minimum and maximum values measured, the dotted line connects the mean values)

6.3.3 IZO semiconductor printing

For the printing of the IZO semiconductor, we modified the initial precursor solution based on 2ME, designed for the spin coating, and, in the same way, as for the dielectric, we integrated an equal fraction of EG into the ink as a co-solvent. Employing the exact solvent composition of the dielectric films, we ensured the chemical compatibility between the layers. As the rheology of the ink remains unaltered, we could exploit a similar waveform and the optimized process developed for the previous dielectric inks. In Figure 6.20, we can see an image of the jetting (2 kHz, # nozzles= 5, T_{nozzle}= 28 °C) and the waveform employed (same as dielectric ink).

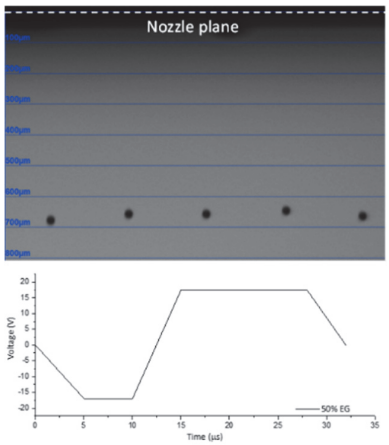


Figure 6.20 Jetting of IZO ink with 50 % EG/ 50 % 2ME: an optical image of the drops formed using the waveform depicted.

We first verified that the transition from spin-coating to printing for the IZO deposition did not negatively impact the electrical performances of the TFTs. We did not add any EG in the solution for spin-coating (same as previous chapters), while for printing was employed a 50%/50% EG/2ME solvent formulation. As a testing structure, we used IZO on SiO_2/Si chips similar to those described in Chapter 3. The highly conductive Si acts as substrate/gate contact, and a 200 nm thick thermal SiO_2 works as the gate dielectric. After an O_2 plasma treatment of 5 minutes (300 W, 13.56 MHz), we deposited one IZO layer via inkjet printing at 400 DPI (2 kHz, # nozzles= 5, T_{nozzle}= 28 °C, T_{stage} 35 °C), or spin-coating, 30 seconds at 2000 rpm. The films were dried at 150 °C for 10 minutes and then subjected to thermal treatment on a hot plate in ambient air at 350 °C for 30 minutes. Then we evaporated aluminum via a magnetic shadow mask to form the source and drain electrodes (W/L= 15). Figure 6.21 reports the typical curves extracted from the two types of samples. For the TFTs with printed IZO, we did not observe a drop in performance compared to the spin-coated ones. Instead, we extracted better mobility due to a slightly higher on-current (~1 cm^2/Vs versus ~4 cm^2/Vs). As similarly reported by *Jeong et al.* for

their thermally annealed (400 °C) printed IGZO TFTs,[244] where their performances were improved from ~1 cm^2/Vs to ~4 cm^2/Vs with the incorporation of 20 % EG, the EG presence may have played a role in the final composition of the MO_x layer, increasing the number of oxygen vacancies and consequently the number of carriers available.

The result demonstrates that when the IZO is thermally cured at a high temperature, the deposition method and the variation in solvent formulation (pure 2ME for spin-coating versus 50%/50% 2ME/EG for printing) do not negatively influence the electrical performance of the devices.

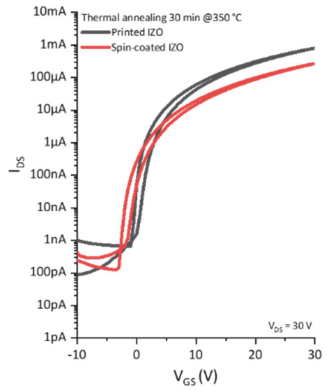


Figure 6.21 Typical transfer curves obtained from thermally annealed (30 min 350 °C) TFTs with printed (50% EG as co-solvent) and spin-coated IZO (pure 2ME as solvent) semiconductors on SiO_2/Si chips.

6.3.3.1 Effect of co-solvent on low-temperature processed IZO via in-situ DUV excimer

We modified the ink composition by adding ethylene glycol with a higher boiling point than the initial solution. Therefore, we increased the heat required to evaporate the remaining solvent and possibly modified the nature of the residuals trapped in the printed layer. This change in chemistry does not significantly affect the IZO synthesis and the quality of the MO_x film, as the annealing at elevated temperatures possesses sufficient energy to remove undesirable compounds. However, this may not be the case with low-temperature approaches, such as the in situ DUV excimer at temperatures below 200 °C.

To verify this hypothesis about the influence of EG in the excimer curing process, we treated via in-situ DUV excimer TFTs with spin-coated IZO (no EG) and printed IZO (50% EG) as semiconductors. As a testing structure, we used printed IZO on Si/SiO_2 chips similar to those described in Chapter 3. The highly conductive Si acts as substrate/gate contact, and a 200 nm thick thermal SiO_2 works as the gate dielectric. After an O_2 plasma treatment of 5 minutes (300 W, 13.56 MHz), we deposited by printing (400 DPI, 2 kHz, # nozzles= 5, T_{nozzle}= 28 °C, T_{stage} 35 °C) or by spin-coating (2000 rpm for 30 s) an IZO layer, which was dried at 150 °C for 10 min and then subjected to the in-situ DUV excimer treatment at 180 °C for 15 min. Figure 6.22 shows the comparison between two typical transfer curves extracted from the realized devices. Despite the same synthesis treatment, the addition of EG in the ink for printing, in comparison to the solution without EG used for spin-coating, resulted in sensible performance degradation, confirming our hypothesis that for the in-situ DUV excimer low-temperature approach, the solvent composition of the ink may play a role in the conversion process.

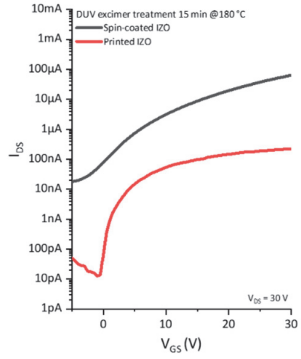


Figure 6.22 Comparison between typical transfer characteristics obtained from TFTs with printed (50% EG) and spin-coated IZO (no EG), synthesized via in-situ excimer treatment (15 min at 180 °C), on SiO_2/Si chips.

Afterward, we preliminary evaluated the effect of the treatment time for the IZO synthesis when the 50 % EG co-solvent is present in the ink by testing an in-situ protocol at 180 °C for different exposure times up to 30 minutes. As a reference, we prepared samples with printed IZO thermally cured at 350 °C for 30 min and compared the results. We used printed IZO on SiO_2/Si chips realized with the same protocol described above as a testing structure. After the drying, the printed layers were subjected to the in-situ DUV excimer treatment at 180 °C for a variable process duration (10–30 min). Figure 6.23 shows the realized devices, with a schematic cross-section and typical transfer characteristics obtained for the different protocol duration.

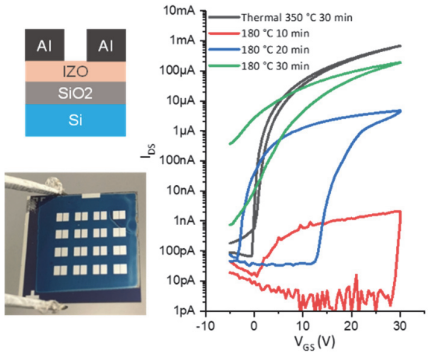


Figure 6.23 Typical transfer curves obtained from printed TFTs made of IZO semiconductor (50%/50% 2ME/EG) treated via in-situ DUV excimer for a variable duration, 10 min to 30 min, and constant temperature 180 °C. (V_{DS} = 30 V)

As depicted in Figure 6.23, the results showed the influence of excimer exposure duration on the MO_x synthesis and the TFT electrical characteristics. The shortest treatment resulted in poorly behaving devices, whereas 20 min and 30 min treatments significantly improved switching and on-current levels. A more significant clock-wise hysteresis was present compared to the thermal reference even after 30 minutes of exposure. This aspect could be related to an incomplete MO_x conversion or residuals in the IZO films caused by the amount of EG added as co-solvent.

6.3.3.2 Ink optimization and influence of co-solvent amount on the TFTs electrical behavior

We investigated the effects of variable solvent composition on the IZO printability and the efficacy of the in-situ treatment for the semiconductor synthesis.

The presence of varying EG fractions strongly influences the rheology of the inks since it modifies the ink viscosity, and consequently, its jetting behavior. The solvent combination 2ME/ EG presents a surface tension that is always suitable for inkjet printing with DMC cartridges (~30 – 40 mN/m) since it can vary from ~31 mN/m to ~48 mN/m, the two values for each solvent alone[28].[245,246] In this case, the main rheological parameter that can affect printability is the viscosity of the ink. We measured the viscosity variation as a 2ME/EG ratio function (0 –50% in volume of EG), as shown in Figure 6.24. The measures are carried at a temperature of 24±0.2 °C using a DV-II+Pro viscometer by *Brookfield.*

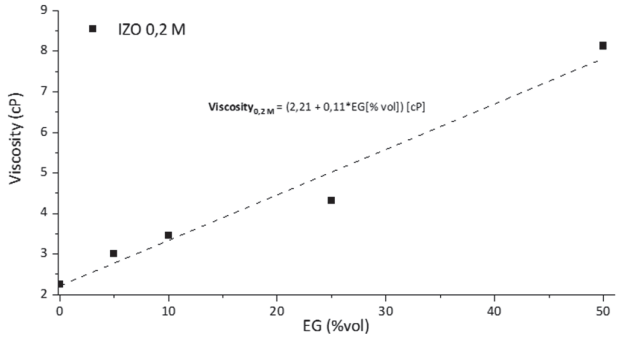


Figure 6.24 Variation of ink viscosity as a function of EG fractions present. 2ME is used as the primary solvent.

[28] Values calculated at 20 °C.

As predictable, the increase in EG fraction led to a monotonous increase in viscosity from 3.01 cP at 5 % EG to 8.13 cP at 50 % EG. The values extracted are in line with those previously reported from Leppäniemi et al. using similar ink for printed InO_x semiconductors.[34] This change in viscosity has a significant impact on the ink-jetting. The typical viscosity range for inkjet is 2-30 cP, while the window recommended from the nozzle supplier is 10- 12 cP.[247] We exploited the analysis software available in the Ceraprinter to evaluate the drop characteristics and jetting stability per each type of ink. Starting from the waveform developed for the metal-oxide inks with an equal proportion of 2ME and EG, we designed and optimized waveforms per each ink formulation to achieve drops with an approximate speed of 7 m/s.

Drop generation and layer formation

First, we assessed the capability of printing ink that does not contain any co-solvent. From theoretical calculations involving Equation 6.3, we can preliminarily calculate the Ohnsurge number for pure 2ME as follows:

$$Oh_{2ME} = \frac{2.26}{\sqrt{20 * 10^{-6} * 965 * 31.8 * 10^{-3}}} = 0.091$$

Such a low value, < 0.1, will likely result in satellite drop formation, as shown in the Oh versus Re graph in Figure 6.4. Figure 6.25 depicts the jetting behavior of the ink with pure 2ME as solvent. The mosaic picture shows the unstable jetting, with the different nozzles having erratic behavior, such as satellite drops generation, uncontrolled jetting, and deflected drops.

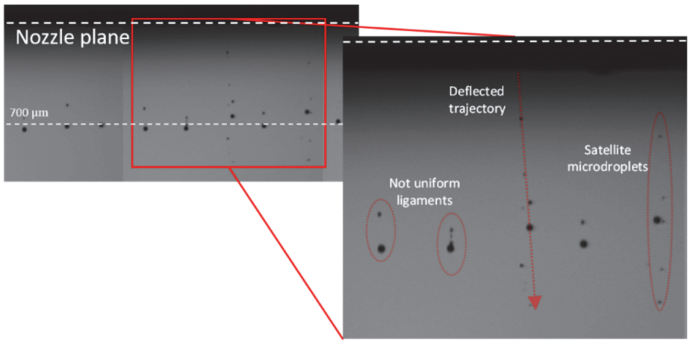


Figure 6.25 Jetting for an IZO ink based on pure 2ME, In detail, the type of non-uniformities observed for this type of ink gathered from Dropanalyser.

As the percentage of EG increases, the ink jettability improves, and more stable drops are formed. Adding 5 % of EG to the ink, the increase in viscosity of almost one cP with respect to pure 2ME (2.26 cP versus 3.01 cP) provides a better drop formation, with a more stable shape and reduced probability of uncontrolled satellite drops. For EG percentages of 10 % or more, the increased viscosity (~3.5 cP) ensures the formation of well-defined single drops and provides a better drop fidelity. In Figure 6.26, we can see the jetting behavior of the different inks according to their EG content (5–25 %). We also reported the waveform used per each ink composition where minor adaptations were employed starting from the one developed for equal EG/2ME fractions, notably lower voltages applied in the filling phase linked to lower viscosities due to minor EG fractions.

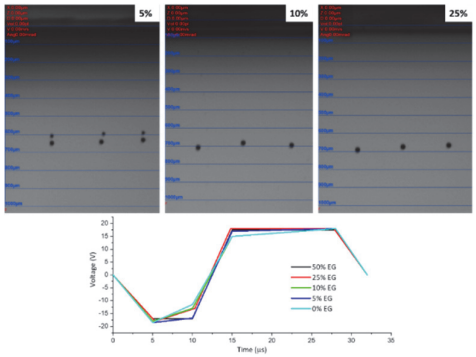


Figure 6.26 Drop formation obtained from inks with variable EG % in 2ME (5, 10, 25 %). We can observe that the ink with the lowest EG percentage, 5 %, may suffer from satellite drops. A comparison of all the waveforms used as a function of the EG % (0 – 50 %) is also reported.

We then examined the layer formation obtained from the inks with different EG concentrations. On Si/SiO_2 chips, treated with O_2 plasma for 5 min at 300 W (13.56 MHz), we identified the parameters for the layer formation (drop splat and drop overlap as a function of the DPI) per solvent composition ($D_{s,50\%EG}$= 270µm, $D_{s,25\%EG}$= 220µm, $D_{s,10\%EG}$= 205µm, $D_{s,5\%EG}$= 200µm). Afterward, we exploited the structure formed by the four squares with variable DPI, as done earlier for the dielectric. (Figure 6.27) Independently from the EG fraction in the ink, 100 DPI was not sufficient to form a uniform layer, whereas a density higher than 200 DPI leads to continuous films. The ink composition influences the printing quality: the higher evaporation rates in the inks with 5 % and 10 % EG result in material accumulation on the edges of the stripes that form the layers after each printing passage, ultimately causing the formation of uneven striped pattern in the layers. At high drop density, the phenomena caused random accumulation of ink and films with inhomogeneous morphology, while the increase of EG % ameliorated the issue and provided a more uniformly distributed ink and better printability.

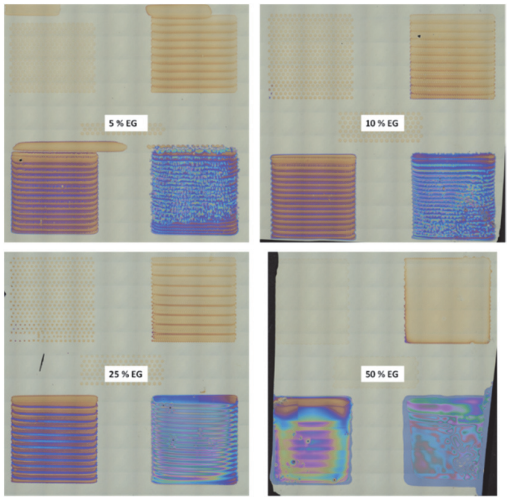


Figure 6.27 Inkjet test patterns realized per each type of IZO ink containing a variable EG percentage, 5, 10, 25, and 50 %, in 2ME on SiO_2/Si substrate. (The yellow color is due to the SiO_2 thickness, 200 nm)

TFT electrical performances as a function of the EG percentage

Once we verified the printability of the inks, we manufactured TFTs by printing IZO onto SiO_2/Si chips, synthesizing the MO_x via an in-situ DUV excimer treatment, and looked at their electrical performances. We have chosen IZO inks with EG percentages of 5, 10, 25, and 50 %. We employed the same process flow described in the previous Section 6.3.3.1. As final IZO annealing treatment, we fixed a process duration of 20 minutes and investigated the effects of variable temperature (160 °C to 180 °C) during the treatment as a function of the volumetric fraction of EG in ink. The substrates were initially subjected to O_2 plasma treatment for 5 min to improve the wettability, then an IZO layer at 400 DPI was printed and subjected to drying at 150 °C for 10 min and then treated via in situ DUV excimer. Per each annealing procedure, we treated the four types of samples simultaneously. Finally, source and drain electrodes were deposited via Al evaporation through a magnetic shadow mask. The transfer curves extracted from various TFTs (n≥3) are summarized in Figure 6.28 and Figure 6.29, devices presenting switching characteristics have been extracted from most samples.

High EG percentages (50 % and 25 %)

The TFTs employing IZO ink with an equal fraction of 2ME and EG resulted in poor or utterly absent transistor behavior. For samples with 50 % of EG, except for the sample treated at 170 °C, which unexpectedly yielded short-circuited devices as visible in Figure 6.28a, both treatments at 180 °C and 160 °C for 20 minutes resulted in poor or inactive TFTs. These poor electrical results align with the previous tests mentioned earlier that employed the 50% EG ink.

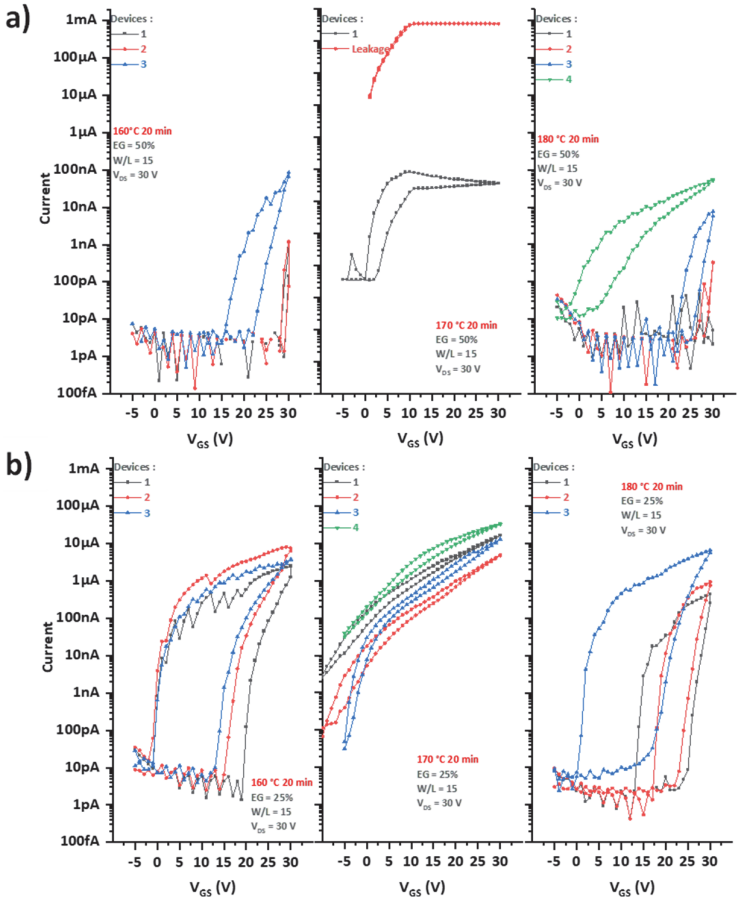


Figure 6.28 Transfer characteristics of IZO TFTs on SiO_2/Si chips made by inkjet with a) 50 % EG and b) 25 % EG in 2ME, processed at a variable in-situ temperature during the excimer treatment. The applied temperature increases from the left (160 °C) to the right (180 °C).

In Figure 6.28b instead, are reported the transfer curves extracted from the TFTs with 25 % EG. The ink with 25 % of EG showed unsatisfactory electrical performances, notably with on-currents lower than the counterparts with a lower EG concentration inside the ink, a large clock-wise hysteresis, and mobility in the range of 0.1 cm^2/Vs or below even at 180 °C. This behavior can be associated with improper MO_x synthesis and the possible presence of impurities and remaining hydroxides that hinder the charge transport and act as traps causing the hysteretic behavior.[244]

Low EG percentages (10 % and 5 %)

The use of ink formulation with the lowest amount of co-solvent, 5 % and 10 %, yielded the best electrical characteristics: mobility in the range of 1 cm^2/Vs or higher have been extracted from the devices treated at 180 °C, with on-current levels in the order of hundreds of microamps and negligible hysteresis. The relative transfer curves are depicted in Figure 6.29. At 180 °C, we observed that most TFTs did not show optimal switching characteristics, with I_{on}/I_{off} values around 100 – 1000 related to high off-currents. However, the presence on both 5 % and 10 % EG samples treated at 180 °C, of a device with optimal switching characteristics, $I_{on}/I_{off} > 10^6$, suggests that this behavior seems to be correlated with the variable layer thickness, with local material accumulation caused by non-optimal printing, that alters the characteristics of the TFTs.

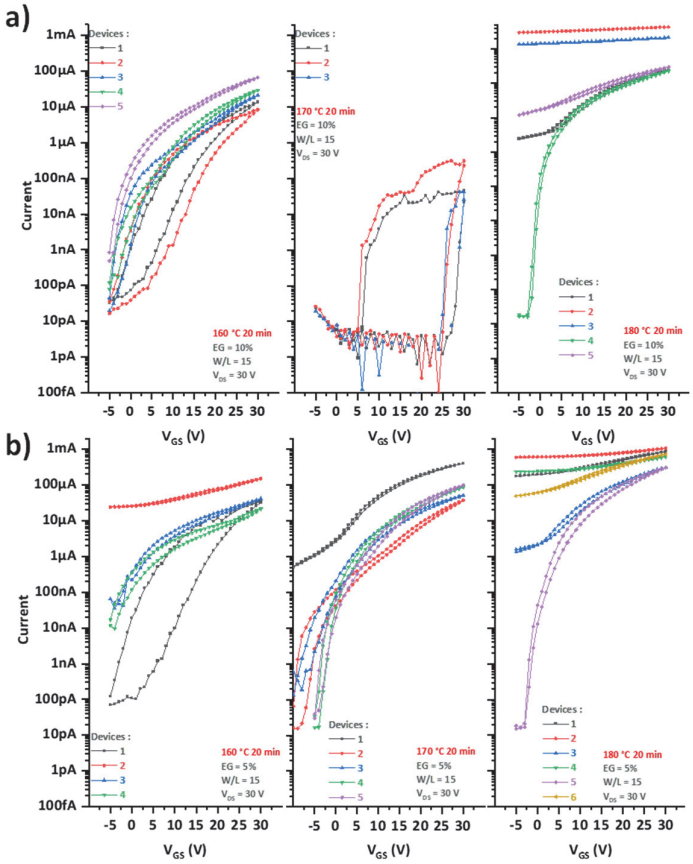


Figure 6.29 Transfer characteristics of inkjet IZO-TFT on SiO_2/Si chips with a) 10 % EG and b) 5 % EG, in 2ME, processed at a variable in-situ temperature during the excimer treatment. The applied temperature is increasing from the left (160 °C) to the right (180 °C).

As expected, the performances of the TFTs sensibly decrease when the in-situ temperature is lowered to 170 °C and 160 °C. Switching characteristics improved. Notably, devices with 5 % EG and treatment at 170 °C reported an overall good switching behavior with $I_{on}/I_{off} > 10^6$. The devices with 10 % EG treated at 170 °C showed unexpected bad electrical characteristics. However, it seems related to problems within the manufacturing of that specific sample more than a synthesis-related problem. Devices synthesized at the lowest temperature of 160 °C, especially those with 10 % EG, reported signs of hysteresis, which suggest an incomplete conversion. Nonetheless, these TFTs had acceptable switching capabilities, I_{on}/I_{off} ~10^5, and on-currents over the µA range despite the low temperature of 160 °C applied and the short treatment time of 20 min.

Summary and discussion

Figure 6.30 summarizes the mobility value calculated per co-solvent/solvent composition as a function of the temperature applied during the 20 min in-situ DUV excimer treatment.

a)

$T_{in-situ}$ / EG %	180 °C	170 °C	160 °C
5 %	1,26±0,56	0,62± 0,55	0,17±0,09
10 %	0,77±0,34	>0,005	0,16±0,11
25 %	0,03±0,02	0,08±0,04	0,02±0,01
50 %	-	-	-

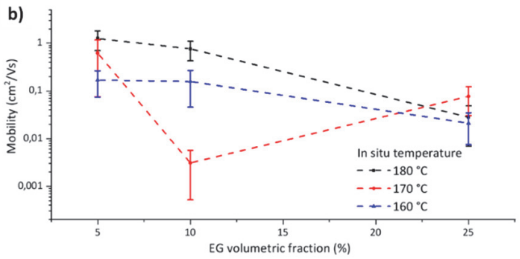
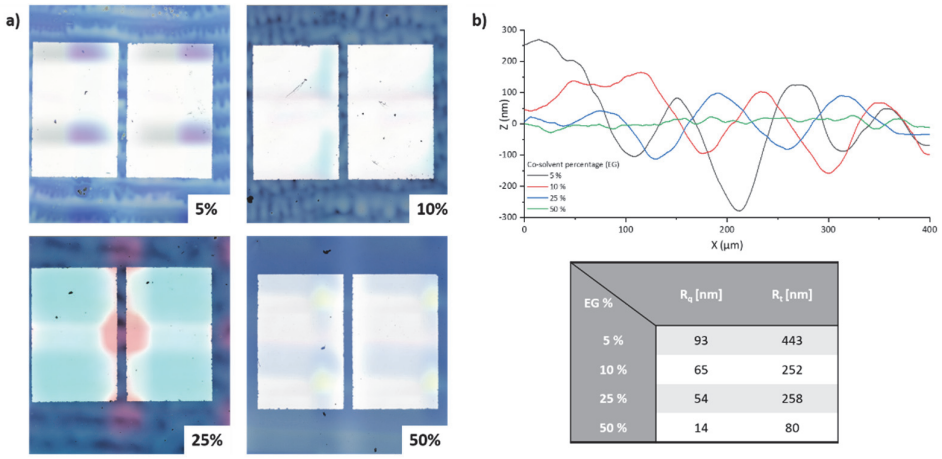


Figure 6.30 Electrical characteristics of TFTs with printed IZO, with variable EG% in 2ME, on SiO_2/Si chips. a) Numerical and b) graphical summary of mobility values as a function of EG %.

Inks with high fractions of EG, 50 % and 25 %, yielded poor or no TFT characteristics, with mobility < 0.1 cm^2/Vs. Better electrical characteristics have been achieved instead for low percentages of EG co-solvent, 10 % and 5 %. As expected, lowering the treatment temperature resulted in reduced performance, notably lower mobility. Devices with 5 % EG in the IZO ink showed a reduction from ~1.26 cm^2/Vs at 180 °C to ~0.17 cm^2/Vs at 160 °C, similarly occurring for those with 10 % EG, from ~0.76 cm^2/Vs to ~0.15 cm^2/Vs. Moreover, the transfer curves of the TFTs treated at 160 °C showed some hysteresis, probably linked to a not complete conversion or the presence of hydroxides.

Comparing the transfer curves obtained from different devices on the same sample with both 5 % and 10 % EG in 2ME, we observed relatively not uniform switching characteristics and variable performances. We suspect that this variability in TFT performance is linked to the improper morphology of the printed IZO layers. A non-uniform printing result in layers where the ink concentration is not well distributed, as depicted in Figure 6.31a and visible from their thickness profiles in Figure 6.31b. In these conditions, the printed structure experiences fluctuations in thickness caused by the variation in the amount of material deposited, which ultimately causes an uneven distribution of electrical performances in the manufactured devices. This aspect can be related to the different availability of electric charges, linked to the amount of MO_x atoms available, and the inconstant effectivity of the DUV excimer treatment influenced by the local fluctuation in thicknesses. The dependence of performances from the semiconductor thickness was also reported by *Leppäniemi et al.*[34] with printed InO_x TFTs thermally annealed at 300 °C. In that frame, they also studied variable EG fractions. However, they ultimately assumed that the presence of co-solvent did not sensibly affect the quality of the MO_x networking and attributed the difference in performance only to a thickness variation in the semiconductor film as a function of the co-solvent.



EG %	R_q [nm]	R_t [nm]
5 %	93	443
10 %	65	252
25 %	54	258
50 %	14	80

Figure 6.31 Effects of variable EG percentages (5 –50 %) on the semiconductor surface of TFTs printed IZO on SiO_2/Si chips. a) Optical images of devices and b) surface profile + roughness values, as a function of the EG %. Both images and profiles have been obtained with a confocal microscope.

This investigation proved that the addition in the initial 2ME ink of variable amounts of EG as a co-solvent with a boiling point higher than the maximum process temperature influences the conversion of the MO_x IZO ink. We consider the presence of EG in the ink as the leading cause of the difference in electrical performances due to a negative impact on the MO_x conversion and residual removal at the low temperatures tested. We cannot exclude that the final film thickness has a role in the performances. However, we believe that alone it cannot justify the complete absence of switching characteristics in the devices with an equal amount of EG and 2ME. A material composition analysis via XPS or other techniques could be helpful to verify the number of precursors and solvent residuals trapped in the MO_x network as a function of the volumetric co-solvent fraction.

Despite non-optimal TFT electrical characteristics, this study demonstrated the potential of the in-situ excimer synthesis to reduce the thermal budget of the printed IZO annealing process, yielding working devices at temperatures as low as 160 °C. These results are promising since we fixed a relatively short processing time and did not include any post-thermal treatment. Therefore, the electrical characteristics could be improved by tuning the in-situ process parameters, as did the DUV-enhanced approach discussed in 0.

Although capable of jetting, inks with EG percentages below 10 % did not ensure sufficient drop fidelity. Therefore, even if 5 % of EG provided the highest mobility, we opted for a compromise between performances and process stability, choosing for the IZO semiconductor ink employed in the following sections a composition of 10 % EG and 90 % 2ME.

6.3.3.3 TFTs with all printed IZO - AlO_x/$YAlO_x$ layers thermally annealed at high temperature

After developing the printing process for the MO_x dielectric and semiconductor, we integrated the printed layers to realize TFTs with a fully printed metal-oxide active stack. To validate the new process flow with both printed layers, we manufactured TFTs with thermally annealed MO_x layers following the process conditions described in Section 4.2.

As a substrate, we utilized 100 mm wide, 525 µm-thick Si wafers coated with a low-pressure chemical vapor deposition (LPCVD) low-stress silicon nitride layer of 100 nm acting as a buffer insulating layer. Afterward, we thermally evaporated Cr (~35 nm) to form, via shadow mask, the metal structures exploited as gate electrodes. The wafer has been then cleaved with a diamond pen to form silicon chips that could be exploited in multiple experiments. We then applied an O_2 plasma treatment (5 min, 300 W,13.56 MHz) to improve the wettability before printing the AlO_x/$YAlO_x$ layers. The printing parameters for the dielectric layers are described in Section 6.3.2 as no difference in printing quality was observed between printing on SiO_2 and SiN_x. We proceed with sequential printing of $YAlO_x$ and AlO_x, between the two depositions, the samples are subjected to a drying step on the hot plate (temperature ramping from 90 °C to 200 °C, then plateau at 200 °C for 1 min) and plasma treatment (5 min at 300 W, 13.56 MHz). After the printing, the layers are dried on the hot plate for 1 hour at 200 °C under ambient atmosphere, and then thermally annealed in an oven in ambient air for 1 hour at 450 °C to ensure the MO_x synthesis. After an O_2 plasma (5 min, 300 W, 13.56 MHz), the IZO (0.2 M, 10 % EG) semiconductor has been printed (1 layer, 400 DPI) using following the protocol described in the previous section. Then the IZO film was first dried for 30 min at 150 °C and then annealed at 350 °C for 30 min on a hot plate in air condition. We evaporated 100 nm-thick Al to form source and drain electrode via shadow mask.

At this stage, we introduced an additional post-annealing step of 30 min at 150 °C after electrodes deposition. We noticed that this additional step was helping in obtaining more uniform switching characteristics by increasing the quality of the interface between S/D electrodes and the semiconductor, as also reported by *Leppäniemi et al.*.[248,249]

Figure 6.32a reports optical pictures of each printing step and the final device, while Figure 6.32b shows the transfer curves extracted from the TFTs.

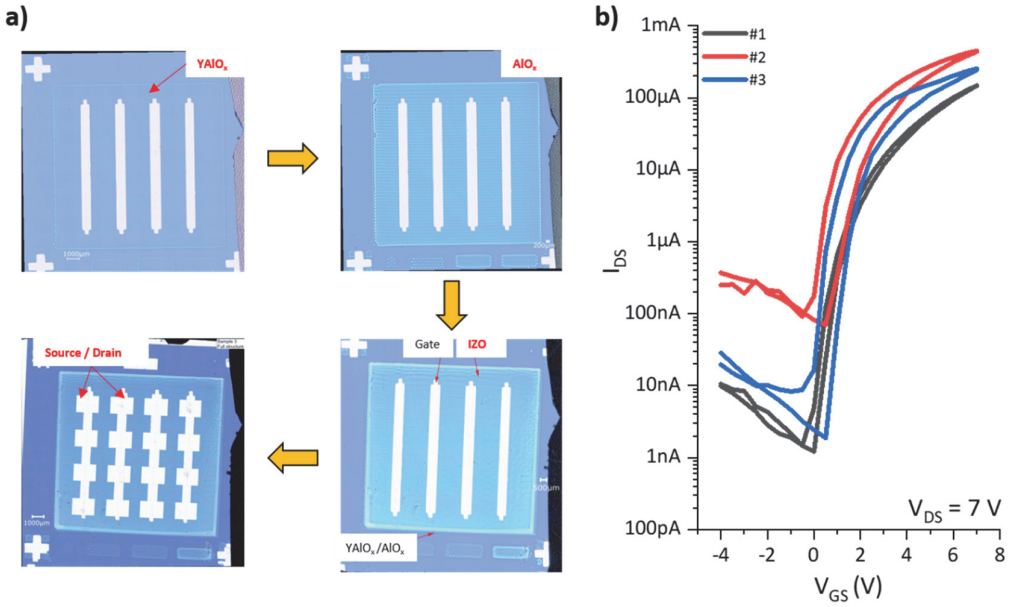


Figure 6.32 TFTs with IZO and AlO_x/$YAlO_x$ printed and thermally annealed at high-temperature on Si substrate: a) optical images of the process steps and b) transfer curves obtained from the samples. . For the layer printing, we used a 0.2 M IZO ink in 10 %/90 % EG/2ME, 0.4 M AlO_x and 0.2 M $YAlO_x$ in a 50 %/50 % EG/2ME medium. Curing parameters: 30 min at 350 °C and one hour at 450 °C for semiconductor and dielectric, respectively. Full TFT stack: Al/IZO/AlO_x/$YAlO_x$/Cr/SiN_x/Si (SiN_x as an insulating buffer).

The devices showed sufficient switching characteristics, with an I_{on}/I_{off} ratio of 8.8±7.1 × 10^4, mainly due to the relatively high off-currents. As seen in Chapter 4, this aspect could be ameliorated by patterning the semiconductor film, which reduces the leakage current. On-current levels were instead satisfactory as they could reach values over 100 µA, which finally yielded mobility value of 4.2±2 cm^2/Vs. These TFT performances are satisfying but lower than those reported in Section 4.1 achieved by the same MO_x active stack treated with the same thermal process but deposited by a spin-coating process (~15 cm^2/Vs). These results indicate that further improvement could be attained by implementing IZO ink formulation and printing strategy optimizations, notably involving IZO patterned structures.

We analyzed the available literature regarding TFTs with printed IZO as semiconductors to compare the electrical performances of our devices. The few reports available are all exploiting thermal SiO_2 dielectric,[70,250,251] or, in one case, vacuum-deposited hafnium oxide gate dielectric.[252] Except for *Lee et al.* that tested thermal annealing at a variable temperature from 200 °C to 400 °C,[70] the annealing temperature required was between 425 °C and 500 °C, a relatively high thermal requirement that could be justified by non-optimized ink formulation or printing processes. Ultimately, mobilities in the range ~8 cm^2/Vs are reported despite the higher temperatures involved in the IZO synthesis. Our devices, which possess both active layers printed and composed of metal-oxides, have shown promising performances despite the lower annealing temperature of 350 °C, thus demonstrating that performing TFTs could be achieved using printed patterned structures for our MO_x functional stack. Looking for the optimal conditions necessary to achieve performing TFTs when low-temperature processing is involved, we decided to further investigate some printing parameters, such as ink concentration and the number of printed layers, which can influence the IZO thickness TFT performances.

6.3.3.4 Printed IZO layer quality improvement

During our experiments, we observed some fluctuation in the printing quality when using a drop density of 400 DPI and a 10 % EG in the IZO ink, with layer morphology not always optimal. To address this aspect, we investigated ways to improve the uniformity of the printed IZO films while aiming for TFTs with the best electrical performances. We decided to deposit them with a drop density of 200 DPI instead of 400 DPI, as providing more repeatable and uniform layers, and check that, despite thinner layers being deposited, we could obtain more uniform layers in thickness and possibly compensate for the reduction in thickness by printing two of them. Therefore, we verified the effect of thickness on the electrical characteristics by manufacturing TFTs with one and two printed IZO layers. The samples were manufactured on SiO_2/Si following the process flow previously exploited for the printed IZO: after the O_2 plasma surface treatment of 5 minutes (300 W, 13.56 MHz), we deposited the IZO layer via printing at 200 DPI. For the two-layer deposition, the films were deposited subsequently without drying in between, as reported in the literature to avoid pinhole formation in the film.[34] The films were dried at 150°C for 10 minutes and then subjected to in-situ excimer annealing for 30 min at 190 °C. Ultimately, Al was evaporated through a magnetic shadow mask to form the source and drain electrodes. The thickness of the printed layers has been measured via AFM, resulting respectively for one and two layers in 10 – 20 nm for 0.2 M ink and 22–43 nm for 0.5 M ink.

In Figure 6.33 are reported the transfer curves extracted by the two types of TFTs. Those with double IZO layers overperformed the TFTs with one-layer-only. These devices with one printed layer showed small mobility of 0.04±0.01 cm^2/Vs and a marked clock-wise hysteresis, whereas the ones with two layers yielded mobility of 0.37±0.05 cm^2/Vs and more negligible hysteresis. The difference in mobility of one order of magnitude confirmed that the thicker film probably possesses more charges available, yielding higher on-currents. Moreover, carrier scattering mechanisms can affect thin semiconductor layers and, in comparison with thicker films, may suffer higher traps at the interface, ultimately decreasing the mobility and increasing the hysteresis.[253] A similar conclusion about low thickness negatively impacting the electrical characteristics of solution-processed TFTs was reported by *Spiehl et al.* and by *Dilfer et al.* referred to their flexographically printed IZO TFTs.[250,251]

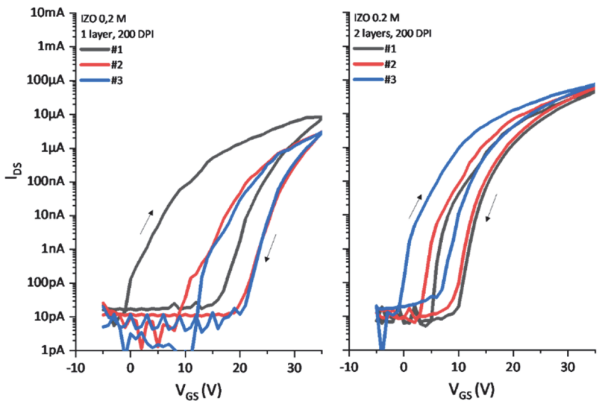


Figure 6.33 Effect of number of IZO printed layers 1, (left) and 2 (right), on electrical performances of in-situ excimer treated (30 min 190 °C) TFTs with SiO_2/Si and a 0.2 M IZO ink. V_{DS}=35 V. (Full TFT stack: Al/IZO/SiO_2/Si).

In the frame of achieving uniform layers that yield good TFTs, we decided to increase the concentration of our IZO ink to 0.5 M. This approach allows us to modify the viscosity of the ink, from 3.45 cP for 0.2 M ink to 4.45 cP for 0.5 M, without adding more co-solvent and further improve the printing stability. Simultaneously, the higher precursor load inside the ink will increase the thickness of the final IZO film, thus providing better electrical characteristics without suffering from the adverse electrical effects linked to thin layers.

Therefore, we manufactured TFTs with the same structure and process flow as discussed above, but we employed a 0.5 M IZO ink. In Figure 6.34 are reported the transfer characteristics of TFT devices made of one and two layers. In this case, we did not observe a significant difference in electrical performances as both types of devices had a satisfactory I_{on}/I_{off} ratio >10^5 and negligible hysteresis. Regarding the mobility, the TFTs with a double IZO layer showed slightly reduced mobility than the counterpart with one IZO layer, respectively 1.35±0.15 cm^2/Vs and 0.72±0.08 cm^2/Vs. The cause of this mobility reduction could be due to possible nanoporosity in the film linked to the double layer stacking, as previously reported by *Avis et al.* for their printed IZTO TFTs.[254]

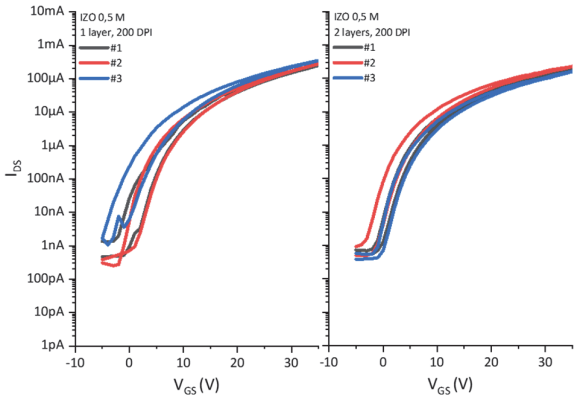


Figure 6.34 Effect of number of IZO printed layers 1, (left) and 2 (right), on electrical performances of in-situ excimer treated (30 min 190 °C) TFTs with SiO_2/Si and a 0.5 M IZO ink. V_{DS}=35 V. (Full TFT stack: Al/IZO/SiO_2/Si).

Figure 6.35 summarizes the various characterization performed on the printed layers and the electrical characteristics of the resulting TFTs. The performances of the TFTs exploited in this study were overall slightly lower than expected as we achieved, synthesizing the IZO at 190 °C mobility in the same range as we reported in the previous section with protocols at 180 °C. We suspect that the relatively high humidity level of ~50 % RH during the fabrication could have negatively impacted the performances. This aspect will be further discussed in Section 6.3.4.

We verified that the thickness of the IZO semiconductor has a role in the electrical performance of the TFT. We identified a suitable thickness range, which could be achieved by either increasing the initial precursor concentration in the ink or by stacking multiple layers. As an outcome of this study about different ink concentrations and the number of stacked printed IZO layers, we could identify the one with 0.5 M and a single layer as the most promising combination to achieve performing TFTs with uniformly printed IZO layers. Once an optimal printing strategy is established, we could optimize the in-situ DUV excimer synthesis curing approach by studying protocol duration and temperature, possibly reducing the process temperature below 180 °C, and ideally involving the low-temperature-treated printed dielectric developed in Section 6.3.2, envisioning the subsequent implementation of the MO_x active stack onto the thermosensitive substrates targeted.

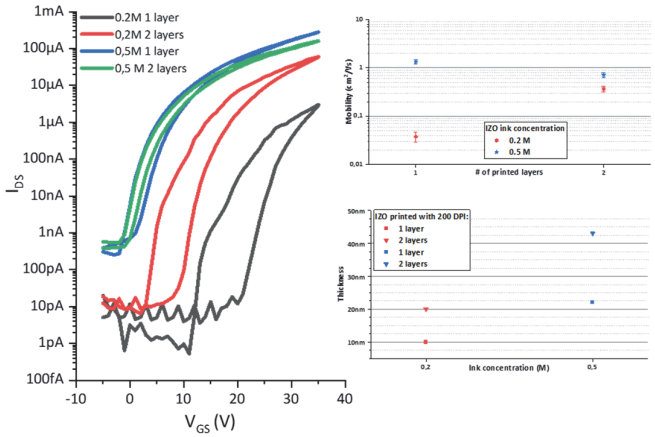


Figure 6.35 Graphic summaries of results obtained testing different ink concentrations and layer stacking. a) Comparison of typical transfer characteristics and b) mobility values as a function of ink concentration and # of layers (n≥3). c) Thickness variation as a function of the number of layers and ink concentration.

6.3.3.5 *In-situ DUV excimer treated TFTs with both printed IZO and $AlO_x/YAlO_x$ dielectric*

Here, we combined the manufacturing processes with synthesis done using the in-situ DUV excimer process developed for the printed $AlO_x/YAlO_x$ dielectric and the printed IZO semiconductors to achieve TFTs with a fully printed active stack at low temperature.

We utilized SiO_2/Si chips as a substrate, where the SiO_2 acted as a buffer insulating layer, then 35 nm-thick Al was evaporated through a shadow mask to form the gate electrode. The process flow for the printed dielectric is the one described in Section 6.3.2, and the final layer synthesis was performed with an in-situ DUV excimer of 20 min at the same temperature utilized to treat the semiconductor afterward, 180 °C or 190 °C. After an O_2 plasma treatment of 5 min (300 W,13.56 MHz) for wettability improvement, we printed an IZO layer (10 % EG, 0.5 M, and 200 DPI). Afterward, dried at 150 °C for 10 min on a hot plate in air condition, and finally synthesized with variable in-situ DUV excimer conditions: 30 min at 180 °C, 60 min at 180 °C, and 30 min at 190 °C. Unfortunately, the experiments did not yield working devices with poor yield due to excessive leakage currents and non-operative transistors. Figure 6.36 reports some examples of transfer curves obtained from TFTs treated with various in-situ DUV excimer parameters. We tested a range of temperatures and process duration that were proven to be sufficient to synthesize operational MO_x dielectric and semiconductor films. Nevertheless, it was not possible to achieve working devices, which indicated that during the combination of the two layers, some parameter/process-step was negatively affecting the operation of the final devices. We identified few possible causes for these manufacturing issues and discussed them in the following sections.

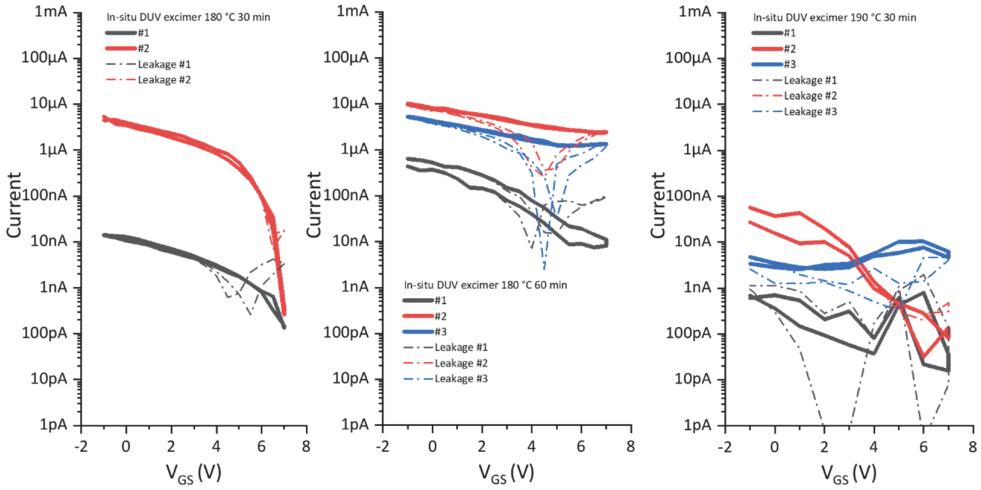


Figure 6.36 Transfer curves obtained from TFTs on Si substrate with IZO and $AlO_x/YAlO_x$ printed and treated with variable in-situ DUV excimer protocols (semiconductor protocols: 30 min at 180°C, 60 min at 180 °C, and 30 min at 190 °C). Full TFT stack: Al/IZO/$AlO_x/YAlO_x$/Al/SiO_2/Si (SiO_2 as an insulating buffer).

6.3.3.6 *Effect of wetting enhancing treatment on in-situ treated dielectric*

As we encountered issues in combining the two low-temperature synthesized MO_x layers, we investigated, as a possible cause for the improper electrical behavior of the TFTs, the effect of wetting-improvement treatment occurring on the dielectric film before the semiconductor deposition. Since we verified that when processed separately, the dielectric in the MIMs or printed IZO for TFTs with SiO_2/Si are correctly synthesized with a satisfactory operation, we suspected that a treatment on the dielectric stack before IZO deposition might have an influence on the interface state of the MO_x stack, thus resulting in nonoperative and leaky TFTs. Notably, Gillan et al. recently reported that their thermally annealed printed $YAlO_x$ dielectric was suffering from dielectric instabilities possibly related to the O_2 plasma treatment performed (1 min at 200 W) before the semiconductor deposition.[205]

To verify if the wettability enhancing process, carried via O_2 plasma treatment, is influencing the behavior of our dielectric film, we manufactured MIM structures on Si chips, with Al electrodes and our printed dielectric stack, synthesized via in-situ excimer at 190 °C for 30 min, and then subjected them to various treatments to identify possible changes in their working behavior. Then we measured the leakage current and confronted the results, establishing possible correlations between treatment and leakage values. In this frame, we tested processes that are typically exploited in solution-processed TFT manufacturing to improve surface wettability: O_2 plasma (5 min at 300 W, 13.56 MHz), DUV[29] in air ambient (10 min), and DUV excimer (in both N_2 and O_2-rich ambient for 10 min).

[29] For the DUV treatment we employed the PSDP-UV8T UV Ozone cleaner from *Novascan* available at Microcity.

The results have been confronted with non-treated samples as reference. Figure 6.37 reports the leakage curves obtained from the various samples.

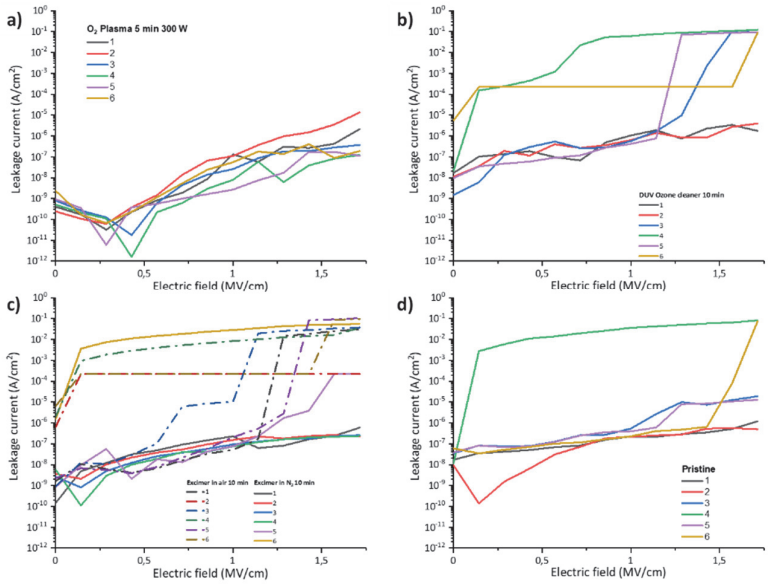


Figure 6.37 Leakage current measured from MIMs (Al/printed AlO_x-$YAlO_x$/Al on Si substrate) after various surface treatments. The dielectric after the in-situ DUV excimer treatment (30 min at 190 °C) was subjected to a) 5 min O_2 plasma, b) 10 min DUV, c) 10 min Excimer DUV in N_2 /air, and d) no treatment (pristine).

From the curves reported, we can observe that only in the case of O_2 plasma the MIM yield was 100 %, whereas all other types of samples tested, at least one broken MIM (current >10^{-4} A/cm^2 before reaching 1.5 MV/cm). The statistical results of the test on the leakage current are summarized in Figure 6.38, where the current level at 1MV/cm is reported. Overall, both DUV types of treatment in the oxygen-rich environment, creating ozone during the treatment, negatively influenced the leakage density, notably all MIM treated with DUV excimer broke after 1 MV/cm while this happens for more than 60 % of the MIMs treated with the ozone cleaner DUV. Compared with the pristine samples, which yielded leakage density values ~10^{-7} A/cm^2, similar to those reported in Section 6.3.2.1, both O_2 plasma and DUV excimer in N_2 yielded slightly lower current densities, respectively $\lesssim 10^{-7}$ A/cm^2 and ~5×10^{-8} A/cm^2.

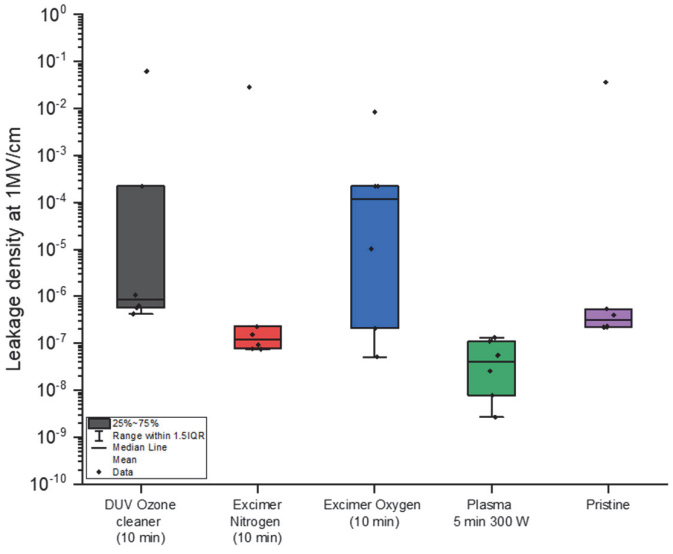


Figure 6.38 Dielectric behavior as a function of the surface treatments. The tests have been carried on MIM capacitors (Al/printed AlO_x-$YAlO_x$/Al on Si substrate) and the dielectric treated with in-situ DUV excimer for 30 min at 190 °C. Statistical values (n=6) of leakage current density at 1MV/cm.

We also checked the frequency dependence of the capacitance as a function of the treatments tested. Figure 6.39 reports the typical C-f curves at low-frequency extracted from samples treated with O_2 plasma, DUV excimer in N_2, and pristine MIMs. We can observe a slight improvement in frequency dispersion for the DUV excimer treated MIM in N_2, but no significant difference is observed between pristine and O_2 plasma-treated.

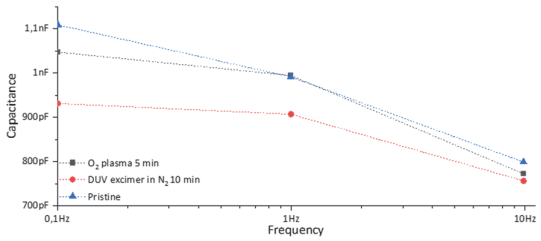


Figure 6.39 Frequency dependence as a function of the surface treatments. The tests have been carried on MIM capacitors (Al/printed AlO_x-YA-lO_x/Al on Si substrate) and the dielectric treated with in-situ DUV excimer for 30 min at 190 °C.

The results of this study demonstrated that O_2 plasma treatment does not seem to negatively affect the dielectric characteristics of the printed AlO_x/$YAlO_x$ stack. However, we cannot exclude that the intermediate treatment could influence the semiconductor/dielectric interface.

6.3.4 Effect of humidity during processing on the TFTs electrical characteristics

Environmental conditions during the processing are another factor that can potentially influence the electrical characteristics of the TFTs. These aspects are not particularly concerning for vacuum-based processes, likely performed in cleanrooms with controlled conditions, with depositions occurring primarily at very low humidity levels and precise temperatures. Metal-oxide solution-processing, which is not necessarily performed in such controlled conditions, may experience performance and yield fluctuation, as many process parameters, such as the printing conditions and sol-gel chemical reactions, can be influenced by humidity and temperature. These aspects are yet not well understood and not adequately investigated. Some studies highlighted the influence of the environmental conditions during the photonic synthesis of MO_x films and how they can influence the TFT performances.[122,147], nonetheless, each step of the manufacturing process should be equally controlled.

Some publications report on the relative humidity values (RH%) as an indicator of the environmental conditions during fabrication, but as it depends on the temperature, it does not represent a consistent parameter (e.g., 40 RH%[30] correspond to 9.2 g/m^3 at 25 °C and 7.3 g/m^3 at 21 °C[31]). *Lim et al.* consistently studied how manufacturing and performances of TFTs with spin-coated InO_x/AlO_x stack can be influenced by temperature and humidity conditions during fabrication, highlighting how at minimal humidity levels (~0 %), the best performances and highest process yields can be obtained.[255] Nonetheless, the temperatures involved were still relatively high (> 200 °C), and the results referred to relative humidity.

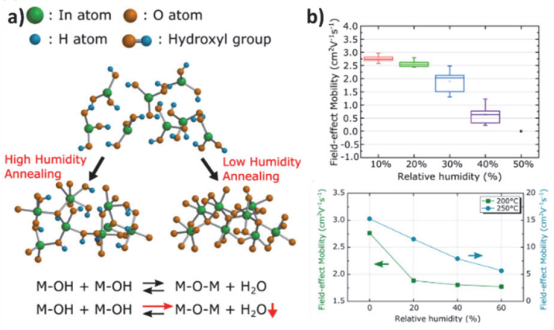


Figure 6.40 Effects of humidity on sol-gel MO_x TFTs. a) Dependence of chemical conversion in InO_x from on the humidity condition during the annealing process. b) Statistics on TFTs performances as a function of humidity and annealing temperature. Adapted from [255].

[30] RH% at a given pressure.

[31] Absolute humidity is measured as grams of water in a cubic meter.

On our side, we experienced variability in process yields and device performances, mainly when low-temperature (< 200 °C) processing was involved. As most of the fabrication steps are carried in a not fully controlled environment, with temperature and humidity level fluctuations (approximately 8.5 – 12 g/m^3), we suspected that this could be one of the causes of our low yield and variations in results. Starting from precursor inks preparation (moisture can be adsorbed from the highly hygroscopic precursors) to deposition (wettability and jetting can be altered) and ultimately MO_x synthesis (TFT performance fluctuations), each step should be controlled appropriately to ensure process reliability. We implemented a solution-preparation step in a glove box to ensure that inks were not affected by environmental conditions. We ideally would have performed all the processing in a ~0 % humidity environment to ensure best electrical performances and process repeatability, as suggested by *Lim et al.*[255]. However, it was practically not possible as the Ceraprinter is not gas-tight, and samples need to be carried out from one processing tool to another. Instead, we tried to control the process as much as possible by transferring all the manufacturing steps inside the printer hull (hot plate for drying and thermal annealing), trying to lower the humidity levels with the use of desiccant (silica gel), and monitoring the absolute humidity value during the processing (temperature and humidity sensor SHT4X Smart Gadget from *Sensirion*).

Since we encountered problems with the fabrication process at higher humidity levels, resulting in low yields that could even be null, we suspected this aspect as a possible cause of device failure. Therefore, we compared two different humidity conditions (8.9 and 11 g/m^3) and observed how humidity levels influence the processing and the final devices. We manufactured devices with printed IZO on SiO_2/Si chips following the process flow described before in Figure 6.3.3 and thermally annealed (30 min at 350 °C). The printability was not affected as jetting and drop size remained unvaried, but the TFT performances were slightly different. In Figure 6.41, we can observe that higher humidity leads to more significant hysteresis and lower on-current. Such performance lowering can be caused by a higher number of hydroxides residuals, either adsorbed during the processing or from less efficient precursor conversion.

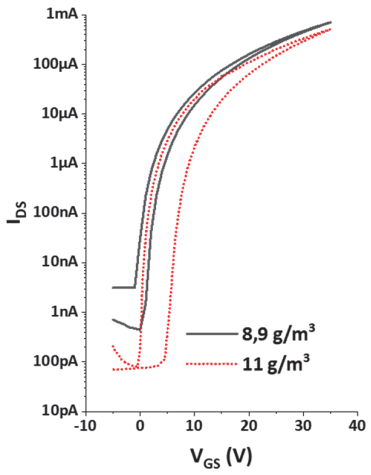


Figure 6.41 Typical transfer curves obtained from TFTs with printed IZO on SiO_2/Si, thermally annealed at 350 °C for 30 min, processed in different humidity environments.

We verified that processing conditions could play a significant role in TFT performances. We could not perform a complete study at more humidity levels and involving in-situ DUV excimer treated devices for time constrictions. Further investigations are required to understand better how much the humidity level affects the device characteristics and eventually identify a range that ensures repeatable processing. Such a study, performed on low-temperature processed MO_x layers, could help understand the required processing conditions and ultimately fill the gap in reliability between sol-gel processing and vacuum-based ones.

6.3.5 Discussion

This section discussed the inkjet printing process applied to the MO_x composing the active stack of our TFTs, oriented toward low-temperature synthesis approaches via in-situ DUV excimer treatments.

In this context, the main parameters that can influence printing quality, MO_x synthesis, and TFT performances have been investigated. We have seen that for the AlO_x/$YAlO_x$ dielectric, the ink chemical composition does not significantly have an influence when the layers are synthesized with the in-situ DUV treatment. After optimizing the printing parameters, like stage temperature and drop density, functional gate dielectrics can be achieved even at processing temperatures as low as 130 °C.

Ensuring a satisfying IZO semiconductor quality to yield performing TFT is more challenging as many parameters can influence the outcome. We showed that solvent/co-solvent ratio, ink concentration, and the number of deposited layers could affect the final performances and that optimization of all the parameters is required. By doing so, we demonstrated bottom gate TFTs with printed IZO on SiO_2/Si chips, synthesized at temperatures ≤ 180 °C and suitable performances ($\mu \gtrsim 1$ cm^2/Vs and I_{on}/I_{off} ratio > 10^5). Such performances are comparable with state-of-the-art TFTs with printed semiconductors annealed at a temperature below 200 °C, summarized in Table 6.2. Moreover, except for laser annealing [133], which can be fast but is not practical as is a localized synthesis approach, the TFTs treated here via in-situ excimer DUV reported the best performances at such low temperature (< 200 °C) and for relatively short treatments (down to 20 min), thus confirming the potential of the proposed low-temperature synthesis approach.

Table 6.2 State of the art regarding TFTs with sol-gel printed MO_x semiconductor treated at a temperature ≤ 200 °C. We also reported for comparison the results obtained in Chapter 5 but with a spin-coated IZO. ("Excimer DUV" in the annealing approach column implies using in-situ excimer DUV at the T_{Max} reported.)

Semiconductor material	Dielectric material	T_{max} (°C)	Annealing approach	Process duration (min)	μ (cm^2/Vs)	Ref.
IGZO	SiO_2	200	Laser	N.A.	1.5	[70]
IZO	SiO_2	200	Thermal	60	0.4	[69]
IZO	**SiO_2**	**190**	**Excimer DUV**	**20**	**1.3**	**This work**
InO_x	AlO_x	180	Excimer DUV	90	2.8	[59]
IZO	**SiO_2**	**180**	**Excimer DUV**	**20**	**1.2**	**This work**
Spin-coated IZO	**AlO_x/$YAlO_x$**	**180**	**DUV+Thermal**	**80**	**0.95**	**This work**
InO_x	ALD Al_2O_3	150	Excimer DUV	180	~1	[34]
IGZO	Polymer+ALD[32]	120	Laser	N.A	4.2	[133]

We also demonstrated TFT devices made of a fully printed MO_x active stack, thermally annealed at 350 °C, exhibiting ~4 cm^2/Vs mobility. Despite a relatively optimized processing protocol, with optimal ink formulation and parameters designed for the low-temperature in-situ DUV approach, inactive or poor transistors were achieved when the two printed layers were combined. We tested synthesis protocols, like in-situ DUV excimer at 180 °C or 190 °C for 30 min, capable of yielding both operational MO_x dielectric (working MIMs proven) and semiconductor films (TFTs on SiO_2/Si proven). This outcome indicates the need for further process optimization and investigation as some aspects of the protocol are not entirely understood.

We excluded that the wetting enhancing treatment, operated between the two depositions, degraded the gate dielectric layer itself. However, it cannot be neglected that this treatment may influence the resulting dielectric/semiconductor interface, impacting the TFTs characteristics.

We preliminary verified that humidity levels could affect the TFTs performances when thermally annealed at relatively high temperatures. However, we suspect that it may have a more adverse effect when low-temperature synthesis is involved. Moreover, the effects on printed gate dielectric and printed semiconductors may be diverse, from more considerable hysteresis to dielectric short-circuits to non-activated devices.

Literature suggests that significantly prolonged in-situ DUV treatments (> 90 min) at low-temperature (180 – 200 °C), applied to a similar sol-gel-based MO_x stack (InO_x/AlO_x), should not negatively affect the TFT electrical performance or degrade the dielectric.[59] Nonetheless, it could be interesting to investigate the effects of subsequent in-situ DUV treatments on the chemical composition of the printed dielectric by XPS to identify possible MO_x damages, notably at the interface, linked to consecutive dielectric and semiconductor synthesis.

The annealing protocol for both layers should be further studied and optimized. We demonstrated in 0 that DUV treatments with short protocols could ensure good electrical performances. However, the performances could be further improved by post-annealing steps. Once process repeatability is better controlled, a parametric study, similar to the one reported in 5.2, could be performed to identify the capability of the in-situ DUV excimer treatment to achieve working TFTs in terms of lower processing temperatures for a limited process duration (< 90 min). By doing so, the thermal process budget could be lowered even further. Afterward, to boost the electrical performances, one could envision a combination with thermal post-treatments or alternative photonic processes, like flash photonic sintering (i.e., Xenon lamp), as shown by *Moon et al.*.[109]

[32] Approach requiring as dielectric: thick PVP (720 nm) + thin ALD Al_2O_3 5 nm. Substrate coated with multi-layer TiO_2+Al_2O_3 by ALD.

6.4 Towards the fully printed MO_x TFTs on a thermosensitive substrate

This section reports the preliminary results obtained on TFTs with printed electric contacts and on implementing the manufacturing process onto a thermosensitive substrate.

We present a possible approach to potentially achieve TFTs with a fully printed structure. We exploited the know-how available at LMTS on printed metallic conductors and identified those that could be suitable as a source and drain electrodes for our MO_x TFTs. We investigated the possibility of using aerosol jet-printed silver and gold for this purpose. Integrating these printed contacts on the MO_x active stack developed, we demonstrated working devices with electrical characteristics similar to those achieved employing evaporated aluminum as a contact. Moreover, silver and gold could be potentially integrated into a low-temperature process flow as they can be sintered via flash sintering.

We also carried first studies on the feasibility for transferring the proposed low-temperature manufacturing and annealing protocols for low T_g substrates. We preliminary tested thermosensitive polymeric foils such as polyethylene naphthalate (PEN) and polyetherimide (PEI), which should be processable at temperatures up to 200 °C: we irradiated the bare samples with DUV for 1 hour to verify their chemical and morphological stability during the synthesis process proposed. Via AFM, we observed an increase in surface roughness and possible material instability due to the treatments; notably, PEN suffered from hillocks formation that could potentially penetrate the TFT devices and cause short circuits. Therefore, we implemented a planarization layer that acted as a barrier, thus increasing the process yield. PEI showed a slightly higher thermal resistance and fewer hillocks among the two materials and was proposed as the substrate for the printed devices. To demonstrate the viability of the process, we propose a protocol to manufacture, exploiting the in-situ DUV synthesis, MIM capacitors with a printed AlO_x/$YAlO_x$ dielectric stack on such polymeric substrates. We demonstrated working devices with leakage currents similar to these achieved on the rigid glass substrate, thus proving that printed MO_x devices could be manufactured with the proposed protocol, paving the way for more complex structures such as printed TFTs.

6.4.1 Source and drain printing

As one of the ultimate goals of the thesis is achieving MO_x based TFTs fully printed, in parallel with the inkjet printing of the active layers, we also carried some preliminary studies on the integration of printed electrodes for our TFTs. For this purpose, we exploited the know-how available at LMTS and the infrastructure at Microcity, particularly the aerosol-jet module of the Ceraprinter. For the printing of the source and drain electrodes, we selected the aerosol-jet technique instead of the inkjet as it enables resolutions in the range of ~10 μm, which can be exploited to increase the on-current levels of the TFTs thanks to the definition of electrodes with a smaller gap.

The material requirements for source and drain electrodes are: matching between metal and semiconductor work functions to achieve ohmic contact, high conductivity, and small contact resistance with the active layer. Moreover, they have to be printable and potentially sintered at low temperatures. Among the portfolio of conductive inks at EPFL-LMTS, we investigated silver and gold inks as a potential material for our printed source and drain electrodes.

Silver is probably the most common printable metal exploited in TFT. It is characterized by a low bulk resistivity of 1.59 μΩ·cm, and a work function of ~4.3 eV similar to the ones from Al (ϕ_{Al}~4.2 eV) and Ti (ϕ_{Ti}~4.3 eV), and generally close or lower than IZO based semiconductors work functions (ϕ_{IZO}~4.1-4.8 eV) [189,256], thus forming an ohmic contact. Few reports are available in the literature regarding inkjet-printed silver electrodes for MO_x-based TFTs, resulting in satisfying electrical performances.[257–259] Silver is often selected also because of the low temperature required to sinter. Depending on the type of ink employed, nanoparticle-based or precursor-based, temperature below 200 °C is generally sufficient to achieve conductivity levels close to bulk.[260] The other material tested is gold. Au possesses a slightly higher bulk resistivity 2.44 μΩ·cm and work function than silver, ϕ_{Au}~5.2 eV, which may cause a rectifying contact (Schottky) with the IZO semiconductor. Gold often requires sintering conditions more demanding in terms of temperature (~250 °C) and is more expensive than silver. However, in terms of long-term stability, gold is inert, while silver tends to oxidize and migrate in humid conditions[261]. Moreover, it is not a biocompatible material[262], whereas gold can be attractive for niche applications such as sensors for healthcare or in-vivo implants.[263–265].

Both inks used are nanoparticle-based: the silver ink was hydrocarbon-based with 40% in weight of silver from *UTDots*, UTDAg40; the gold ink was water-based, with 20% Au in weight, from *Fraunhofer IKTS*, Au-LT20. The inks were employed as received and subjected to sonication (5 min) before deposition. As a test structure, we used the fully solution-processed IZO-AlO_x/$YAlO_x$ stack on a highly doped Si wafer that worked as substrate and gate contact. After O_2 plasma treatment for wettability enhancement (5 min at 300 W, 13.56 MHz), the $YAlO_x$ and AlO_x solutions have been spin-coated, as described in Chapter 4, and cured 1 hour at 450 °C in the

oven. Afterward, a DUV treatment for 10 minutes was performed before depositing one layer of IZO via printing (50%/50% EG/2ME ink), following the procedure described in previous sections. After a drying step (1 hour at 150 °C), the latter was then annealed on a hotplate in air condition for 30 min at 350 °C.

For source and drain electrodes, we compared the two printed metals, printed Ag and printed Au, with e-beam evaporated Al acting as a reference. First, we deposited 100 nm-thick Al through a shadow mask designed to leave empty areas for printed electrodes. Then, we printed[33] the gold electrodes with geometrical parameters W = 1000 µm and L = 100 µm, similar to those realized via shadow masking, and annealed it at 250 °C for 60 min on a hotplate in air conditions. Ultimately we printed Ag electrodes with the same geometry and annealed the samples at 200 °C for 10 min on a hotplate in air condition.

In Figure 6.42 are depicted the optical images of the structures, with relative cross-section and thickness analysis via optical microscope.

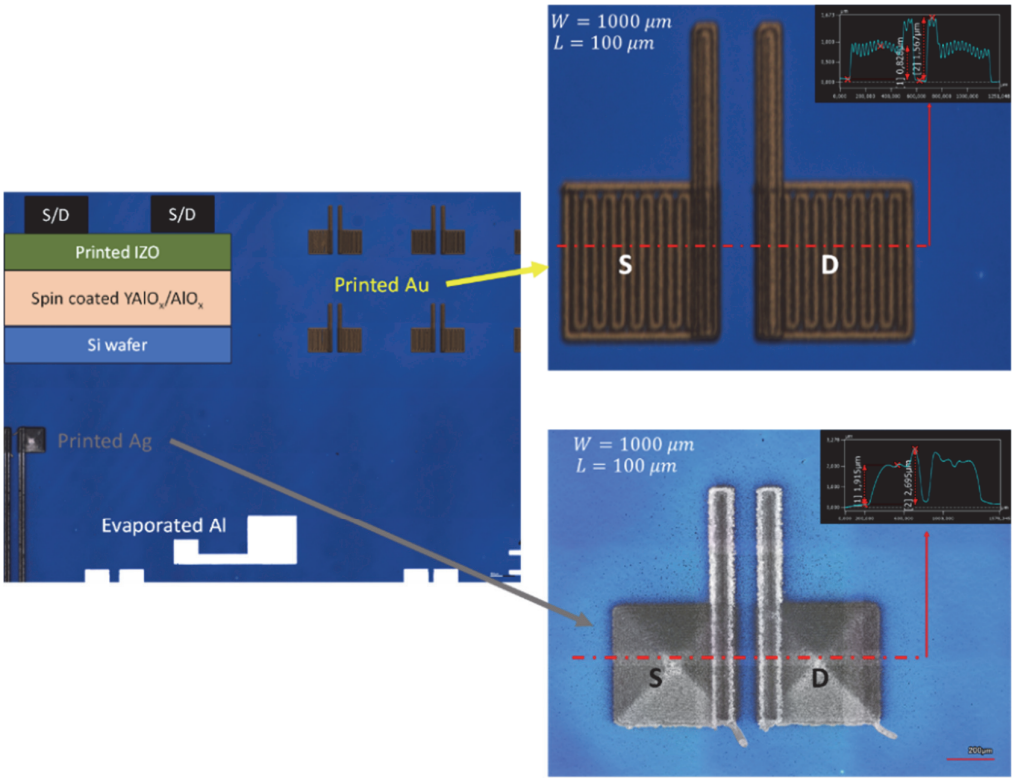


Figure 6.42 Aerosol jet printed Au and Ag electrodes on printed IZO. On the left an optical image of a sample; on the right, a zoom-in of the two types of printed electrodes and relative thickness profiles, obtained with the optical microscope. The typical thickness achieved is ~1 µm. The dimensions of the depicted electrodes are W = 1000 µm and L = 100 µm.

As depicted in Figure 6.43, typical transistor electrical characteristics have been extracted from all types of TFTs made. Relatively high off-current levels have been observed as expected from non-patterned devices. The TFT with Al-based electrodes showed the best performances, with I_{on}/I_{off} ratio over 10^4 and good on-current (~mA). A similar I_{on}/I_{off} ratio was achieved with silver electrodes but lower on-currents, approximately one-fold less. As predictable, gold electrodes have yielded the worst performances with an I_{on}/I_{off} ratio of only ~100 and on-current level in the same order of silver. From the output characteristics, we can observe that the devices reach a saturation condition with V_{DS} = 2-3 V. However, TFTs with Au electrodes present a less sharp curve in the linear regime and saturation regime at V_{DS} > 3 V, suggesting a higher contact resistance due to possible non-ohmic behavior.

[33] A 10 min DUV was performed before Au and Ag printing. The stage temperature was 35 °C. A nozzle size of 150 µm and a printing speed varying from 0.4 to 1 mm/s were employed. The printing parameters necessary to ensure a stable aerosol jetting were previously developed in the laboratory.
For silver: sheat gas flow = 0.32 psi, atomizer gas flow = 1.02 psi, and atomizing current 0.45 A.
For gold: sheat gas = 0.56 psi, atomizer gas = 1.26 psi, and current = 0.46 A.

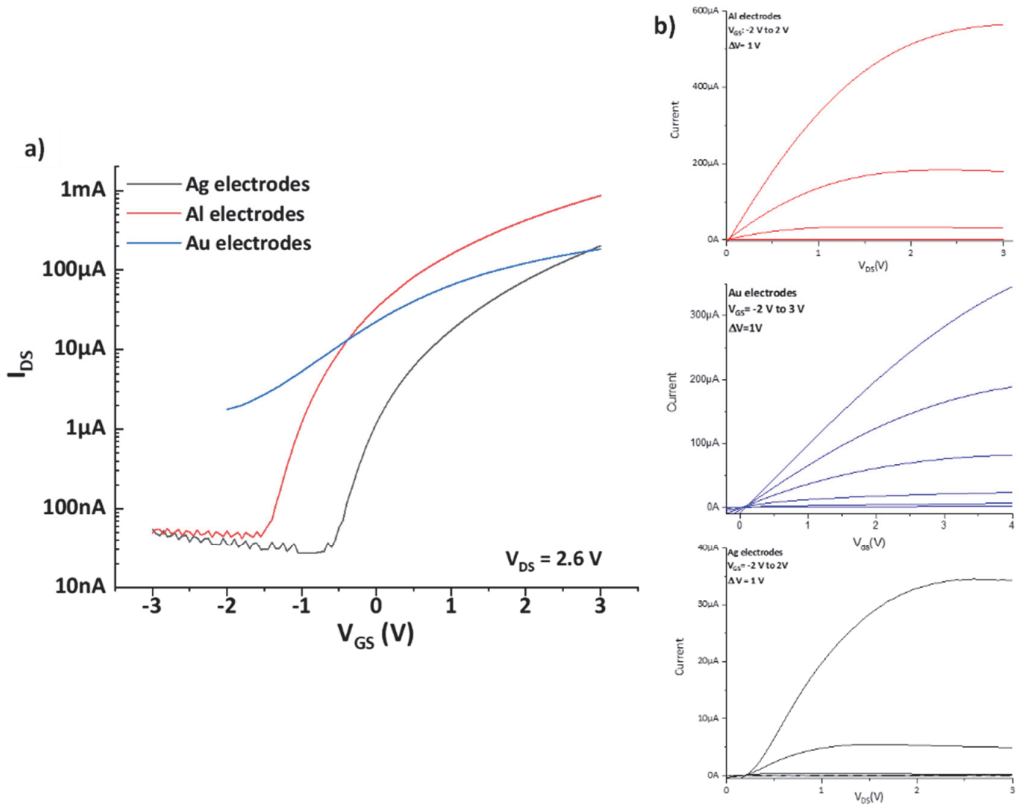


Figure 6.43 Typical electrical characteristics obtained from IZO-TFTs with printed Ag and Au electrodes compared to evaporated Al: a) transfer and b) output.

This preliminary study established the feasibility of aerosol printing as a deposition method for the source and drain electrodes. A relatively large channel length was tested here (L = 100 µm), but thanks to the high resolution achievable of the aerosol jet technique and Ceraprinter used, one can envision reduced electrode size, increasing W/L ratio, and achieving TFT with boosted on-current levels. Ag is the most promising among the two materials tested as it provides better electrical performances than Au. Moreover, it is suited for low-temperature processing as it can be sintered thermally at 140 °C for 60 min to reach 8 µΩ·cm[34]or photonically via flash sintering.[56,106]

6.4.2 Printed MO_x on a thermosensitive substrate

Ultimately aiming for printed TFTs on thermosensitive foils, we identified polyetherimide (PEI) and polyethylene naphthalate (PEN) as potential candidates. These foils are relatively transparent and can sustain temperatures up to 200 °C for a limited time, thus suitable for our purpose.

The resistance to excimer DUV treatments of the bare polymeric substrates has been tested by performing a 60 min in-situ DUV treatment and comparing the roughness of the samples via AFM before and after the treatments. As depicted in Figure 6.44, both PEI and PEN experienced damage caused by the treatment: the roughness R_q is slightly increased as well as the R_t.[35] Roughness R_q can influence the morphology of the deposited layer, leading to inferior charge transport in the semiconductor due to scattering phenomena. However, the increase in R_t is more concerning since it indicates the formation of hillocks from the polymer, which could potentially penetrate the thin film device and destroy it.

[34] From ink datasheet.

[35] R_q =Root mean square roughness R_t = Total height of roughness profile, representing difference in height between highest peak and deepest valley.

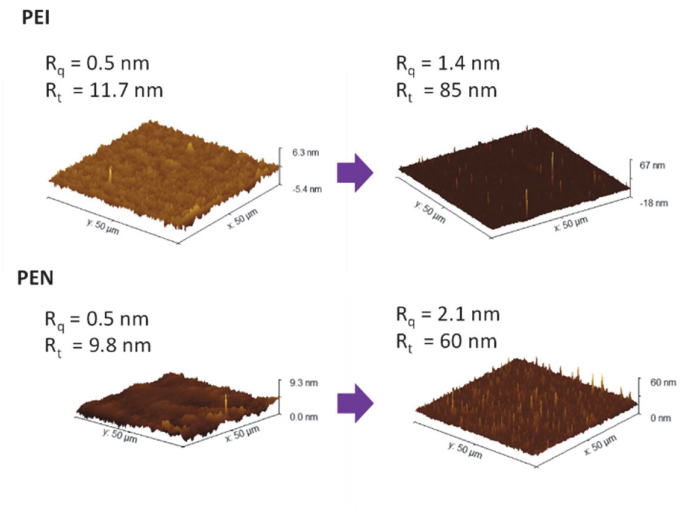


Figure 6.44 AFM analysis of bare PEN and PEI before and after one-hour in-situ excimer DUV treatment.

As a result, we identified PEI as a potential candidate as the DUV treatments resulted in a lower hillock density. Moreover, we decided to implement a planarization layer, acting as a barrier that reduces the risk of device failure due to some polymer punching through. Such an approach appears to be mandatory as most of the literature involving MO_x deposited onto low T_g substrates, like PEN, reports using ALD alumina barrier or relatively thick bottom electrodes.[34,88,266] In our case, we exploited a siloxane-epoxy-based resin, which can be conveniently spin-coated on the substrate and cured at low temperatures (100 °C).

Afterward, we implemented the manufacturing protocol developed for the printed MIMs capacitors on the selected PEI substrate. The complete protocol is described in Section 6.3.2.1. A final in-situ DUV excimer treatment of 20 min at 170 °C was performed to synthesize the printed MO_x dielectric layers. The devices, depicted in Figure 6.45, showed a low leakage current level (7±6 10^{-8} A/cm^2) at 1 MV/cm, measured over six devices) similar to the one achieved on a glass substrate (~10^{-7} A/cm^2). Such results are promising as no significant performance loss has been experienced after the transfer onto flexible foil.

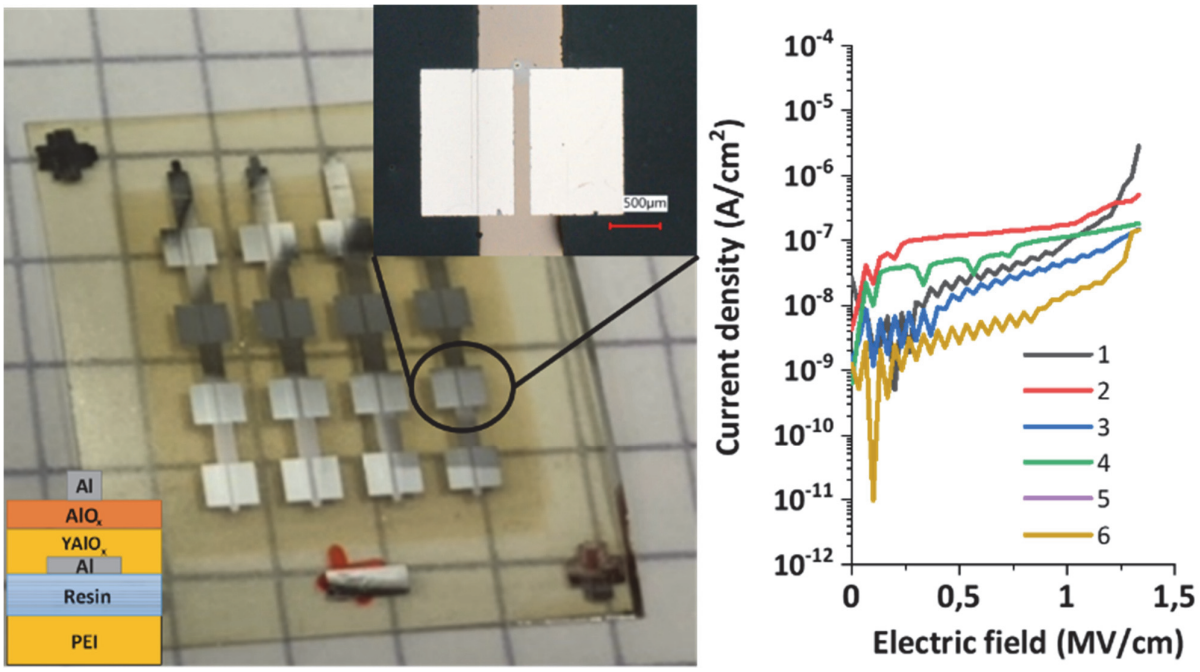


Figure 6.45 MIM realized on PEI. Optical image of the devices with extracted leakage currents.

As proof of concept, we demonstrated that synthesizing a printed MO_x dielectric via in-situ DUV excimer on PEI is possible. We also performed preliminary tests on TFTs structures with printed MO_x active stack on PEI by depositing ink-jet printed IZO on the layer stack employed for the MIMs. Figure 6.46 shows the proposed TFT stack architecture involving the siloxane-epoxy-based resin as a buffer layer on the PEI substrate. For these tests, we applied in-situ DUV curing conditions for the IZO layer similar to those exploited for the devices manufactured on Si in Section 6.3.3.5, such as 180 °C and 190 °C for 30 min.

Figure 6.46 Cross-section of the proposed printed MO_x TFT layer stack on PEI foil.

Predictably we did not achieve working devices, with results similar to the ones obtained from fully printed MO_x TFTs on Si substrate as discussed in Section 6.3.3.5. Once established the successful excimer DUV synthesis process for the fully printed MO_x stack on silicon, the proposed process flow for TFT manufacturing onto PEI could eventually be replicated. Nonetheless, integrating the total active stack on such substrate can present additional challenges that may require further investigations to achieve working devices. We showed that implementing a barrier layer reduces the risks of device failure due to hillock creation on the polymeric foil. However, another common source of device failure in TFTs deposited on foils is the formation of cracks in the metal oxides layers. The leading cause is the difference in the thermal expansion coefficients (CTE) between the polymeric substrate, dimensionally unstable, and the rigid inorganic MO_x layers deposited on top. An excessive mismatch between CTEs generates stress states in the deposited films during the thermal treatments, potentially causing failures in the MO_x layers. The manufactured MIMs structures did not suffer from this kind of problem, proving that the combination of materials (MO_x dielectric/Al/resin/PEI) can result in some relaxation of the thermomechanical stress generated during the dielectric curing. Nevertheless, the additional thermal treatments and the cyclic thermal stressing related to the successive IZO synthesis can potentially impact the deposited structures. No evidence of cracking was observed on the deposited layers during the preliminary attempts of manufacturing the fully printed MO_x stack on PEI, but further studies on the integrity of the in-situ DUV processed active layers may be required.

These results obtained on thermosensitive PEI substrates demonstrate that the in-situ DUV excimer process proposed could eventually be effective for the active MO_X layers printed on foil. Despite the possible substrate degradation due to the DUV exposure, the device integrity can be successfully maintained by employing a barrier layer, conveniently manufactured at low temperatures, without needing vacuum-based processed barrier layers. Our preliminary tests suggest that once solved the problems related to the DUV synthesis of the functional metal oxide stack, transferring the manufacturing process on the foil could be completed without significant changes in the process flow. These achievements represent a starting point for further investigations to reach the initial objective of this thesis: manufacturing fully printed IZO-based TFTs on thermosensitive substrates.

6.5 Conclusion

This chapter presented the aspects related to the exploitation of in-situ DUV excimer for MO_x synthesis at temperatures below 200 °C applied to printed layers toward the realization of fully printed TFTs.

We first introduced some theoretical aspects of inkjet printing, such as ink requirements for optimal jetting, and presented the printing platform exploited during this work. Then, we focused on implementing a printing protocol for both the dielectric and semiconductor metal-oxide films. We discussed the aspects related to MO_x printing for TFTs, such as ink formulation for layer-to-layer compatibility, rheology modification, and suitable layer thickness. In this context, we discussed the challenges of yielding uniform layers, particularly those related to the possible presence of the “coffee ring effect”, typical of precursor-based solutions. We considered the possibility of adding co-solvents in the ink mixture to ameliorate the issue and selected ethylene glycol, with a high boiling point and viscosity (T_B = 197 °C, viscosity = 16 cP), as co-solvent for the IZO ink.

Starting from the $YAlO_x$ and AlO_x inks, we proposed a printing protocol that, after evaluating parameters such as O_2 plasma substrate pre-treatment, stage temperature, and drop density, allowed to achieve uniformly printed layers without suffering from the coffee ring. Afterward, we investigated the effectivity of the proposed in-situ DUV excimer treatment on the MO_x dielectric stack. On MIM

structures manufactured on glass, we applied a 20 min long excimer DUV exposure at variable temperatures (130 – 180 °C), reaching even at the lowest processing temperature of 130 °C, leakage current levels at 1 MV/cm of ~10^{-7} A/cm^2, satisfactory to develop transistors.

After that, we developed an IZO semiconductor printable ink. First, we studied how different co-solvent fractions in ink affect both the jettability and quality of the deposited layer. In this context, we looked for a combination that ensured stable jetting and was favorable for a low-temperature synthesis by limiting the amount of high boiling point components in the ink. Then, we studied the electrical performances of TFTs with printed IZO semiconductors, obtained from inks with a variable EG fraction (5 – 50 % in volume) and treated via an in-situ DUV excimer performed at variable temperatures (160 – 180 °C). We confirmed that higher EG percentages lessened the electrical performances by decreasing the effectivity of the synthesis method. Simultaneously, we verified that, by tuning the ink formulation (EG% < 10 %), it was possible to achieve mobility over 1 cm^2/Vs even at a synthesis temperature of 180 °C. This kind of study on the impact of EG % on MO_x TFT characteristics was never performed for a low-temperature synthesis approach, highlighting the importance of a correct ink formulation. Further performance improvement was achieved by investigating how ink concentration and the number of printed layers affect the in-situ DUV synthesis. By doing so, we identified an optimal IZO printing protocol for low-temperature synthesis: a 0.5 M ink with 10 % in volume of EG as co-solvent and a single printed layer.

We then proposed a protocol to integrate the developed printable functional metal oxides and achieve a fully printed MO_x active stack on a silicon substrate. We demonstrated thermally annealed (350 °C) TFTs with inkjet-printed functional MO_x stack that yielded mobility ~4.2 cm^2/Vs and I_{on}/I_{off} ratio over 10^4. Ultimately, we integrated the low-temperature synthesis approach to the combined layers, which resulted in poor yields and excessive leakages. The future implementation of patterned structures, notably for the IZO semiconductor, could improve the TFT performances by limiting leakage sources and possibly increasing the process yield. We verified that the wetting enhancement treatment (O_2 plasma) performed on the dielectric layer before the semiconductor deposition did not degrade the dielectric. Consistent leakage levels (~10^{-7} A/cm^2 at 1 MV/cm) were maintained after the treatment, but possible effects on the dielectric surface influencing the state of the IZO channel interface, cannot be excluded. Humidity was shown to impact the electrical performances of high temperature thermally annealed TFTs, reducing the on-currents and increasing hysteresis when the manufacturing process happens in a higher humid ambient. We suspect that this parameter could play a role when the low-temperature DUV synthesis approach is involved. However, additional investigations would be necessary to establish the importance of the environmental conditions and other factors during device manufacturing to achieve a reliable process providing repeatable results. Further process tuning is therefore required to achieve TFTs with a fully printed IZO-AlO_x/$YAlO_x$ stack synthesized at lower temperatures than 200 °C.

Aiming to develop fully printed TFTs on thermosensitive substrates, we realized operative TFTs with aerosol jet printed source and drain Ag/Au electrodes, demonstrating the viability of this material combination for future fully printed devices. Ultimately, we implemented the printed MO_x layers and the synthesis method proposed on thermosensitive substrates such as PEI foils. We showed MIM structures with printed AlO_x/$YAlO_x$ excimer treated, achieving leakage levels in the dielectric similar to those on a rigid glass substrate (<10^{-7} A/cm^2 at 1 MV/cm). These results demonstrated that the in-situ DUV excimer approach described in this thesis is a strong candidate for the future development of fully printed MO_x-based electronics on thermosensitive foils.

Chapter 7 Conclusion and outlook

This thesis contributes to MO_x based TFTs field with a novel solution-processed IZO semiconductor / AlO_x-$YAlO_x$ dielectric stack, which can be manufactured via inkjet printing and, thanks to DUV-based synthesis techniques, processed at temperatures below 200 °C, compatible with thermosensitive substrates such as PEN and PEI. Here, we summarize the contributions and discuss the outlook on future work.

7.1 Conclusion

7.1.1 Solution-processed IZO-based TFTs

Thanks to operational stability and switching capability, IGZO-based semiconductors are the prevailing materials for commercial sputtered TFTs. However, via solution processing, they require relatively high synthesis temperatures. Instead, indium oxide (InO_x) semiconductors can be solution-processed at a relatively low temperature but own a poor current modulation and are often unstable. We presented a more stable yet performing sol-gel alternative to the mainstream InO_x for low-temperature processing. The sol-gel-based indium zinc oxide (IZO) semiconductor was designed to achieve TFTs with the best combination of performance in mobility and switching capabilities. We studied the cationic ratio and the effects of variable compositions of the IZO films on the TFTs characteristics. After selecting 7:3 In:Zn as an optimal compromise between switching capabilities (I_{on}/I_{off} ~10^6, V_{Th}~0 V) and on-currents, we further investigated its chemistry and the possibility of alloying the IZO with aluminum to improve electrical performances. In this frame, Al precursors, in concentration varying from 0 % to 10 %, was included in the IZO solutions as a dopant. The electrical characteristics of the resulting TFTs have been compared, and the effects of Al in the semiconductor assessed. Fractions below 1 % in Al did not show significant effects on the devices. Higher percentages, 3 % or more, lessened both on- and off-current, reducing mobility by ~95 % at 10 % Al doping. We attributed such lessening in currents to a stronger oxygen-cation binding, linked to the increased Al-O bonds in the Al-doped IZO, reducing the oxygen vacancies and the number of available carriers in the MO_x. As no significant performance improvements were observed, the initial IZO formulation 7:3 In:Zn was chosen for our semiconductor.

Then we studied how the sol-gel IZO interacts with two different types of high-k AlO_x-based dielectric: ALD Al_2O_3 and novel sol-gel AlO_x/$YAlO_x$ developed at Empa in Switzerland. In this context, we investigated the interaction of the different dielectrics with the sol-gel IZO semiconductor when treated at a high temperature. The study analyzed the electrical behavior and material characteristics of the IZO-based TFTs as a function of the annealing temperature (200 – 450 °C) and the nature of the dielectric implemented. Comparing the two types of devices, we observed a marked difference in performance, where the TFTs with sol-gel dielectric overperformed the ALD counterpart in mobility up to ~26 cm^2/Vs versus ~4 cm^2/Vs, and switching I_{on}/I_{off} 10^6 against 10^4 at 450 °C. This disparity was attributed to a better interface between the fully solution-processed semiconductor/dielectric stack than the solution-processed/vacuum-based one. Furthermore, the small subthreshold swings obtained with the AlO_x/$YAlO_x$ dielectric ($\lesssim$0.2 V/dec) suggest a desirable small interfacial trap density and confirm the excellent match between the IZO semiconductor film and the AlO_x/$YAlO_x$ dielectric layer. By implementing a standard photolithographic process to limit the possible sources of leakage, fully solution-processed TFTs were manufactured combining printed AlO_x/$YAlO_x$ dielectric and with spin-coated IZO, thermally annealed at 450 °C and 350 °C, respectively. Thanks to the patterned structure, the TFTs exhibited performances comparable with state-of-the-art TFTs made of sputtered IGZO semiconductors (max mobility reported ~76 cm^2/Vs), such as I_{on}/I_{off} ratio ~10^9 and high mobility ~68 cm^2/Vs. Such remarkable performances, achieved with an active stack composed of sol-gel-based metal-oxides, confirmed the excellent potential of the selected functional materials.

The MO_x system, annealed at high temperature, was thoroughly studied, providing valuable information on the behavior of the solution-processed devices, which can also be exploited for MO_x systems different from the one described in the thesis.

7.1.2 Low-temperature processing of MO_x TFTs via DUV

We studied a Hg-based DUV-enhanced low-temperature treatment for the sol-gel synthesis of IZO semiconductor films, reaching a maximum processing temperature of 200 °C. We demonstrated a prolonged synthesis protocol of 1 h DUV exposure and 3 h thermal treatment, applied on the original sol-gel-based MO_x TFT active stack composed of printed AlO_x/$YAlO_x$ dielectric and spin-coated IZO

semiconductor, that can yield TFTs with mobility over 40 cm^2/Vs. Combining the selected metal oxide stack with the synthesis protocol investigated, we achieved IZO-based TFTs with excellent electrical performances (μ~ 16 cm^2/Vs, I_{on}/I_{off} ratio > 10^8, subthreshold slope (SS) < 100mV/dec) even with process shorter synthesis protocols (20 min DUV + 1 h thermal treatment). Such TFT characteristics are superior to those reported in the literature for sol-gel IZO-based TFTs treated with similar synthesis methodology, meaning comparable DUV lamp and process duration. Furthermore, a parametric study on the effect of the exposure duration and post-annealing time on the IZO chemical characteristics and electrical performances of the TFTs allowed us to identify their role in the synthesis process and minimize the process duration. We demonstrated that 5 minutes short DUV exposure could trigger the sol-gel chemical reaction while a quick 5 minutes thermal post-annealing at 200 °C provides sufficient energy to remove residuals from the IZO film and ensure performing TFTs (μ ~3 cm^2/Vs, I_{on}/I_{off} ratio > 10^8, SS < 100mV/dec). Eventually, we established the critical role of the thermal treatment temperature by comparing the same treatment protocol, 20 min DUV + 1 h post-annealing, carried at 180 °C and 200 °C. The DUV exposure ensured working devices with good switching capabilities, but the insufficient thermal energy provided to the IZO film at 180 °C depressed the carrier mobility, lessening it to a value close to 1 (μ = 0.95 cm^2/Vs) versus the ~16 cm^2/Vs achieved at 200 °C.

The DUV-enhanced approach presents a thermal-efficient alternative to the prolonged DUV processes reported so far in the literature. The method, operative at low temperature (down to 180 °C), has been investigated, and its effectivity for the IZO synthesis explored. This study provided new information on the role and importance of the treatment steps on semiconductor conversion and final TFT performances. Such knowledge is crucial to minimize the thermal budget required for the process, thus increasing the compatibility of the approach with thermosensitive substrates. Moreover, we identified what appears to be the temperature limit of this approach as at 180 °C, to reach satisfactory TFTs operation, the MO_x synthesis necessitates undesirably prolonged treatments (> 90 min).

7.1.3 MO_x printing towards fully printed TFTs onto thermosensitive substrates

Aiming for a process capable of further reducing the thermal budget required for the IZO synthesis, we investigated an alternative, more powerful DUV excimer source with an adapted protocol involving both light and heat exposure, performing a so-called “in-situ treatment”. The approach first was applied to the printed $AlO_x/YAlO_x$ dielectric by manufacturing capacitive structures (MIMs) and in-situ treating by DUV excimer the dielectric layers for 20 min at variable temperatures (130–180 °C). The MIMs fabricated on glass substrates exhibited a leakage current level of ~10^{-7}A/cm at 1 MV/cm, satisfactory to develop transistors. With the proposed in-situ curing approach, we achieved performances similar to those reported on the same type of dielectric layers developed by our partners at Empa, but at a lower temperature and with a shorter processing time (20 min at 130 °C instead of 60 min at 150 °C). To prove the suitability of the selected materials and synthesis approach with thermosensitive substrates, we proposed a process flow to integrate these devices on polyetherimide (PEI) foil. First, a planarizing buffer layer was implemented, then the MIMs were manufactured by printing and DUV treating the dielectric with a protocol similar to the one employed for MIMs on glass, ultimately yielding leakage currents comparable to those obtained on a rigid substrate.

We developed an inkjet process for the IZO semiconductor envisioning the cost-effective large-area manufacturing of metal-oxide TFTs on temperature-sensitive substrates. In this context, the ink formulation was optimized to obtain a good compromise between printability and precursor conversion at low temperature (< 200 °C) with the in-situ treatment. We studied various parameters, such as solvent/co-solvent composition, ink concentration, and drop density, comparing printing quality and the electrical performances of the resulting TFTs. The outcome was an ink formulation and a printing process optimized for IZO synthesis using the proposed in-situ treatment at low temperature, which ultimately resulted in TFTs with printed IZO excimer-treated at 180 °C for 20 min exhibiting a mobility μ >1 cm^2/Vs. Finally, we manufactured TFTs with functional MO_x printed stack demonstrating μ > 4 cm^2/Vs when thermally annealed. We proposed a protocol for low-temperature processing of the fully printed MO_x stack for TFTs and conducted preliminary tests, but some process optimizations are still required.

The main scientific challenge for manufacturing sol-gel MO_x based TFTs on thermosensitive substrates is the MO_x synthesis at temperatures compatible with the low T_g substrate. We have proven that the in-situ DUV excimer presented is capable of this task and is a strong candidate for MO_x synthesis at processing temperatures even below 180 °C. Moreover, the relatively short processing time required is potentially appealing for industrial applications. In this context, cost-effective processing on a large area could be achieved via inkjet printing, but this approach, consisting in treating by in-situ DUV excimer ink-jetted MO_x films, requires further investigation as some aspects are still not well controlled. However, with further process optimization, the combination of the in-situ DUV-excimer treatment on inkjet printed metal-oxide electronic films developed in this thesis could potentially lead to printed MO_x TFTs at temperatures compatible with more eco-friendly and mainstream materials, such as PET or paper, which are currently out of reach.

7.2 Outlook

This PhD work provided a solid basis for the achievement of fully printed MO_xTFTs on the mainly used thermosensitive substrates, such as PEN and PET, in the field of printed electronics. The temperature reduction was achieved thanks to the investigations performed on two DUV-based synthesis approaches, which helped understand their working principle and optimizing their process. We proved the excellence of the material combination selected as the TFT devices, synthesized using various methodologies, showed state-of-the-art performances. MO_x active layers, with both semiconductor and dielectric printed, have been developed, and their synthesis at temperatures ≤ 180 °C demonstrated. We provided substantial advancements, implementing novel approaches to the challenges in focus with the final objective, notably developing ink formulation in the perspective of low-temperature applications and implementing parametric studies directly on the final sol-gel metal-oxide stack. However, few steps are still required to fulfill the final goal of fully printed MO_x TFT on cost-effective and temperature-sensitive substrates.

Further lowering of the thermal budget could enlarge the portfolio of substrates compatible with MO_x TFTs processing, including more eco-friendly and inexpensive polymers such as PET and eventually paper or bio-polymers. The in-situ DUV excimer method presented in the thesis is a strong candidate for the MO_x synthesis at temperatures in the range of 150 °C. Because of the wide range of protocol parameters, like exposure duration, temperature, and possible combination with post-treatments, studies are still required to identify the limits of the approach. Furthermore, one can envision that these limits can be afterword overcome by combining different photonic methods to synthesize metal-oxide electronic layers such as flash sintering and in-situ DUV. For flash sintering, process adaptations will be required to reach a higher light absorption efficiency for the transparent metal-oxides, like introducing dyes or ad-hoc metal gate structures.

Process repeatability and yield are still problematic, especially for sol-gel-based MO_xTFTs processed at low temperatures. Well-controlled laboratory conditions are mandatory as humidity can affect the chemical reactions (e.g., hydrolysis) and TFT characteristics. These aspects are still not well studied; identifying a suitable range in the manufacturing conditions (temperature and humidity) for repeatable processing at low temperatures would help fill the gap in process reliability between vacuum-based and solution-based approaches. Understanding how the treatments influence the layers and interfaces is also mandatory to improve the reliability of the process and the quality of the TFTs. In this frame, the influence of the MO_x stacking order (top-gate versus bottom-gate) and additional steps in the process flow (e.g., adding a passivation layer) could be further investigated.

To reach fully printed TFT devices, additional studies are still necessary to develop printable contact electrodes, which are processable at low-temperature, electrically compatible with metal-oxide semiconductors in terms of work function (i.e., providing ohmic contact), and eventually transparent. Sol-gel MO_x conductors such as ITO would be an ideal candidate. However, their processing at temperatures < 250 °C is still challenging. As shown in the last paragraphs of the thesis, metals like Au and Ag can be employed and, since non-transparent, be sintered exploiting techniques like flash sintering which preserve the integrity of the substrate. For applications that do not require transparency, it is a viable option. However, alternatives to Au and Ag, less costly and ideally forming ohmic contacts, would be preferred. Zinc could be an attractive printed alternative thanks to its adequate conductivity, suitable work function, and biodegradability. Nonetheless, the printing of conductive zinc structures is not straightforward as ZnO formation is thermodynamically favored. Therefore, non-conventional methods such as chemical sintering or complex photonic approaches (e.g., laser) may be required, and the compatibility of these approaches with MO_x manufacturing has to be proven.

From an environmental point of view, electronics in terms of material and process involved are not eco-sustainable. The research for novel materials, notably more respectful of the environment and ultimately bio-degradable, is rapidly increasing to contrast the surge in e-waste linked to consumer electronics diffusion. In this context, the methodologies presented in this thesis could be of help and applied to biodegradable metal-oxide functional layers. The DUV synthesis methods described in this thesis are potentially suited for all nitrate-based precursors in solution and could be exploited for the sol-gel processing at low-temperature of biodegradable high-k magnesium oxide (MgO) films. The same applies to ZnO-based semiconductors. The DUV approach is potentially exploitable to manufacture “green” metal-oxide-based electronics at low temperatures using more environmentally friendly, scalable, and cost-efficient printing methods. Moreover, by lowering the temperatures required by the processing of MO_x films, biodegradable substrates such as paper, silk, and other biopolymers could be potentially involved, paving the way for a new category of eco-friendly transistors.

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Curriculum vitae

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RESEARCH EXPERIENCE

Ph.D. candidate

Soft Transducers Laboratory, LMTS, Swiss Federal Institute of Technology Lausanne, EPFL

Advisor: Dr. Danick Briand

- Conception and manufacturing of printed metal-oxide-based thin-film devices (TFTs) at low temperature on flexible substrates, in the frame of a multi-partner funded project of the ETH domain (*FOxIP).*
- Design and development of semiconductor material composition correlated with its deposition via additive manufacturing techniques, such as ink-jet.
- Implementation of parametric studies for process optimization through ad hoc Design of Experiments.
- Contribution to developing a novel approach for integrating final prototypes onto thermosensitive substrates, such as paper and flexible polymers (PEN, PEI).

EDUCATION

- **Ph.D. in Microsystems and Microelectronics** *Aug. 2017-Present*

  Soft Transducer Laboratory, LMTS, Swiss Federal Institute of Technology Lausanne, EPFL

  Advisor: Dr. Danick Briand

  Thesis: *'Deep-UV approaches and printing of indium zinc oxide thin-film transistors targeting their processing on thermosensitive substrates'*
- **MCs in Nanotechnology Engineering** *Oct. 2013-July 2016*

  Università La Sapienza di Roma

  Advisor: Dr. Marco Balucani

  Thesis: '*New technology for production of MEMS through the use of Localized SOI Islands*'
- **BCs in Chemical Engineering, Materials and Environment** *Oct. 2009-Dec 2013*

  Università La Sapienza di Roma

  Advisor: Prof. Cecilia Bartuli

  Thesis: '*High-temperature corrosion phenomena in Waste-To-Energy plants*'

TECHNICAL SKILLS

- Material synthesis and characterization in a chemical laboratory environment (i.e., viscosity, thermal gravimetric analysis TGA)
- Electrical and material characterization (i.e., SEM, AFM, XPS, XRD, FTIR, C-V, C-f)
- Micro-fabrication with cleanroom equipment (i.e., photolithography, thermal evaporation)
- Additive manufacturing of thin-film electronics on a flexible substrate (i.e., inkjet and aerosol jet printing)
- Design and manufacturing of prototypes

PUBLICATIONS

Peer-reviewed articles

- Mancinelli A, Bolat S, Kim J, Romanyuk Y E and Briand D 2020 Deep-UV-Enhanced Approach for Low-Temperature Solution Processing of IZO Transistors with High-k AlOx/YAlOx Dielectric *ACS Appl. Electron. Mater.*

- Bolat S, Torres Sevilla G, Mancinelli A, Gilshtein E, Sastre J, Cabas Vidani A, Bachmann D, Shorubalko I, Briand D, Tiwari A N and Romanyuk Y E 2020 Synaptic transistors with aluminum oxide dielectrics enabling full audio frequency range signal processing *Scientific Reports* **10** 16664

Conference papers and presentations

- A. Mancinelli, S. Bolat, Y. E. Romanyuk and D. Briand; *Effect of DUV Curing on Low-Temperature Synthesis of IZO Semiconductor-Based TFTs*, 2020 Virtual MRS Spring/Fall Meeting & Exhibit, Nov 27-Dec 4,2020 (Virtual poster)

- A. Mancinelli, S. Bolat, Y. E. Romanyuk and D. Briand; *Solution Processed Metal Oxide TFTs for Thermosensitive Substrates*; Swiss@print, September 23-25, 2019, Fribourg (Poster)