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An IGCT Gate Unit for Zero-Voltage-Switching Resonant DC Transformer Applications

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An IGCT Gate Unit for Zero-Voltage-Switching Resonant DC Transformer Applications

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***Abstract*—Recently, IGCTs have shown a great potential for the soft-switching dc transformer applications based on LLC resonant converter. The zero-voltage switching that is present in this converter topology enables an operation of IGCTs without clamping circuit and with significantly higher switching frequencies, while maintaining the exceptionally low conduction losses. The high voltage and current ratings of the IGCTs make them a preferred choice for an efficient bulk power transmission. This paper shows how gate units for IGCTs can be optimized for this soft-switching application. It presents a simplification of the driving topology and the design process for high switching frequencies. This results in low power consumption and a very small size of the gate unit. The prototype of the gate unit is built and experimentally validated in a 2.5 kV 0.75 kA resonant operation of the IGCT.**

***Index Terms*—IGCT, gate unit, LLC converter, resonant, dc transformer, soft switching**

I. Introduction

A dc transformer is one of the key components to enable future medium-voltage dc grids. A promising topology for this emerging application is the resonant LLC converter operated in open loop near its resonant frequency [1]–[6]. Not only does this topology naturally offer a very stiff voltage ratio independent of the dc transformer loading, it also provides a galvanic isolation via a compact medium-frequency transformer (MFT) and high conversion efficiency due to zero-voltage switching (ZVS) operation.

To transfer sufficiently high power at medium-voltage levels, many researchers propose to integrate several LLC resonant converters into input series output parallel connected structures (e.g. [3]). While this approach offers some advantages, such as modularity and possible redundancy, the overall complexity is rather high, indicating lower reliability, increased volume, and, likely, even increased costs.

In contrast, the recent research [7]–[9] has proposed to utilize integrated gate-commutated thyristors (IGCTs) to enable the power conversion with a single LLC resonant converter stage. Such bulk power transfer is expected to achieve higher conversion efficiencies due to power-scaling rules applying to transformers and the lowest-in-class conduction losses of IGCTs. Moreover, the IGCTs proved to be highly reliable and provide a possibility for series-connected redundancy as they have a defined mode of failure as short-circuit. References [8], [9] have furthermore shown that the application with low turn-OFF currents and ZVS enables the operation of IGCTs at unusually high switching frequencies of up to several kHz and possibility to remove the clamp circuit that is otherwise required and used in all commercial products (typically variable speed drives). Moreover, the preflooding effect, prolonging the turn OFF in resonant application of IGBTs [10], has proved to be significantly less pronounced for IGCTs [9].

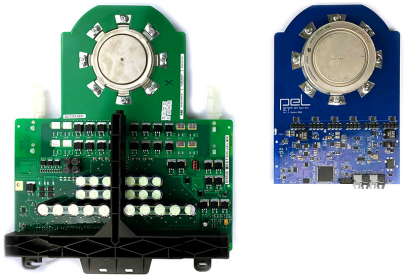

Fig. 1. Comparison of the size of the proposed gate unit for soft-switching applications (right) next to the commercial gate unit for hard-switching applications (left).

Although the aforementioned properties make IGCTs a preferable choice for the application in resonant medium-voltage dc transformers, the conventional gate units (commercial or prototypes) are far from optimized for this kind of high-frequency operation. As will be shown in this paper, the volume and the consumption of the designed gate unit can be reduced significantly by simplifying the driving topology. To demonstrate the size reduction, Fig. 1 shows a commercial gate unit next to the proposed one.

This paper shows the advantages of tailoring the IGCT gate unit for the LLC-converter-based dc transformer applications. It proposes a new driving topology that provides a high level of integration and demonstrates the possible optimization of the turn-OFF channel. Moreover, a protection scheme is implemented to prevent a shoot-through. The design and the functions of the proposed gate unit are validated experimentally, showing the key waveforms.

The rest of the paper is structured as follows: Section II presents the specifications given by the application which will be used as an input for the design. Section III shortly presents the operating principles of the state-of-the-art gate

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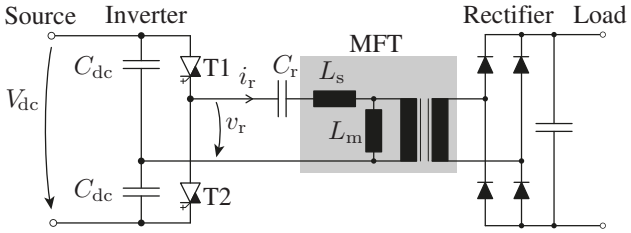

Fig. 2. Half-bridge LLC converter topology employing reverse-conducting IGCTs.

TABLE I
PARAMETERS OF THE EXAMPLE DC TRANSFORMER

Resonant frequency	f_0	1.6 kHz
Switching frequency	f_s	1.44 kHz
DC-link voltage	V_{dc}	2.5 kV
Turn-OFF current	I_{off}	140 A
Peak resonant current	$\hat{i}_r$	750 A
Dead time	T_{DT}	10 µs
Stray inductance	L_s	15 µH
Magnetizing inductance	L_m	1.5 mH
Resonant capacitance	C_r	680 µF

units from the literature. After, Section IV shows the details and considerations for the practical gate unit design for the resonant dc-transformer application. The developed gate unit prototype is tested in a target resonant operation in Section V and in a single-pulse high-current operation in Section VI. The conclusions are drawn in Section VII.

II. Application Specifications

The gate unit is developed for a 68 mm gate-commutated thyristor (GCT) applied in resonant dc transformers. A possible configuration of an LLC-converter-based dc transformer is depicted in Fig. 2. The converter parameters for validation of the gate unit, presented in Table I, are selected according to the design process from [9]. Note that although the LLC resonant converter is operated below the resonant frequency, the voltage ratio of the dc transformer is not impacted significantly. This is because the magnetizing-to-stray inductance ratio $m = 100$ is sufficiently high and the characteristic impedance $Z_0 = 0.15\,\Omega$ is sufficiently low. For more details on this topic, please refer to [1].

Fig. 3 shows the typical waveforms that were recorded in the no-load and full-load operation of the resonant test setup (presented later in Section V). As the switching frequency was selected below the resonant frequency, the turn-OFF current value I_{off} is 140 A independently of the current loading. This value can generally be set by a proper value of the magnetizing inductance of the MFT L_m. As the loading increases, an increasing resonant pulse is superimposed on the triangular current waveform. The limit for the maximum peak current value of the resonant pulse is the maximum allowed conduction losses and the condition for ZVS (as the increasing resonant pulse shortens the time when the integrated antiparallel diode is conducting). Note that the dc transformer application of the LLC converter covers only two operation modes of this converter often labeled as "O" and

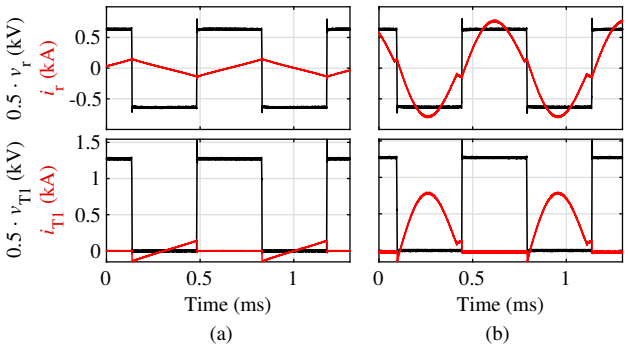

Fig. 3. Typical measured waveforms of an LLC resonant converter: (a) in no-load operation, (b) in full-load operation. v_r and i_r represent the voltage and current applied to the resonant tank, v_{T1} and i_{T1} represent the blocking voltage and the current of the upper IGCT T1.

"PO" (represented by Fig. 3a and Fig. 3b, respectively) in the literature (e.g. [11]). The other operation modes known for variable-voltage applications, such as "PON" or "PN", are not utilized.

Observing the waveforms in Fig. 3, several specifics of this IGCT application can be identified:

- the switching frequency is relatively high compared to a typical hard-switched IGCT operation (kHz range vs few hundreds of Hz)
- the turn-OFF current is constant for all operating points and is relatively low (it is a fraction of the rated GCT current)
- there is always a soft turn ON (typically, a zero-voltage turn ON while the antiparallel diode is conducting)
- the $\mathrm{d}i/\mathrm{d}t$ of the anode current during the IGCT turn ON or the retrigger is roughly two orders of magnitude lower compared to a typical hard-switched IGCT operation (below 8 A/µs vs. up to 1 kA/µs)

These observations will be further utilized to optimize the gate unit. Furthermore, the gate unit should be capable of a single-time high-current turn OFF of more than 1 kA for a case of emergency.

III. State of the Art of Gate Units

All gate units from the literature [12]–[17] provide the following basic functions, where each is typically implemented in its own dedicated hardware stage:

- *turn OFF* – to turn OFF the GCT and keep it OFF, negative voltage (−20 V) is applied between gate and cathode
- *turn ON (and retrigger) pulse* – to turn ON the GCT while ensuring that all thyristor cells are uniformly activated, a high-current short pulse is injected into the gate
- *backporch current* – to ensure that the device remains in an ON state, a relatively low current of several Amperes is continuously supplied into the gate after the turn ON

If the application requires that the GCT remains in the ON state while the antiparallel diode is conducting, a special attention needs to be paid to the gate unit design. The reason is that the negative voltage applied by the antiparallel diode forces the PN junction at the transparent anode to reverse

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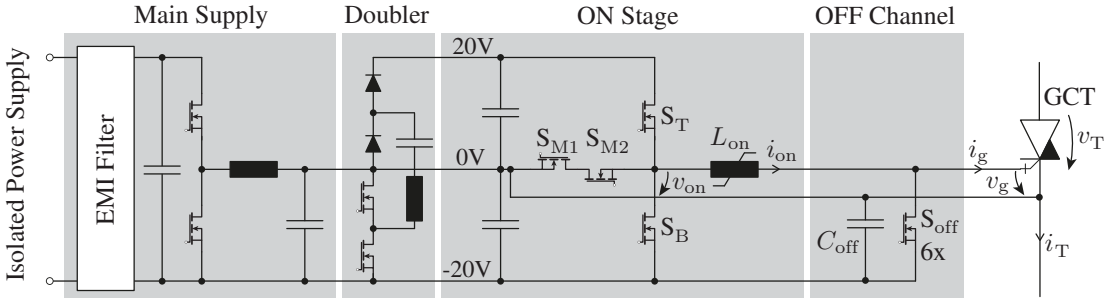

Fig. 4. Power-stage schematics of the gate unit designed for soft-switching application.

Fig. 5. Photo of the gate unit designed for soft-switching application.

avalanche and the intrinsic gate-to-anode diode opens, which in turn drives the gate-to-cathode voltage v_g negative. This effect has been considered and studied in e.g. [12], [13], [17]. In gate units, this occurrence is usually coped with by adding an additional stage that reduces the gate current by dissipating the energy in the gate unit [12], [17]. After the current of the antiparallel diode becomes lower (its voltage drop becomes lower), the PN junction near anode starts blocking and the voltage becomes positive. To ensure that the GCT is homogeneously ready to take over the current again a so-called retrigger pulse, similar to the turn-on pulse, is applied to the gate. Reference [13] proposes a different approach to cope with negative gate voltage without the necessity to dissipate the energy on the PCB. However, the ON channel is supplied by a dedicated floating power supply, which increases the complexity.

While the IGCT technology, including the gate units, proved to be robust and reliable in many field applications, the gate units are often criticized for their size, that poses practical restriction on the mechanical design of the stack, and their high power consumption (up to 130 W [18]) compared to that of IGBT drivers, that has to be covered by a floating power supply isolated for medium voltages.

IV. Gate Unit Improvement and Design

The central idea of the improvement for the gate unit is to utilize the advantageous properties of the LLC converter topology: Since the turn-OFF current is lower, the turn-OFF channel can be reduced in capability. Furthermore, since the application guarantees soft switching for the turn ON with a very low $\mathrm{d}i/\mathrm{d}t$, the turn-ON and retrigger pulses can be reduced in the magnitude. The feasible reduction depends on the exact GCT technology and should be discussed with the semiconductor manufacturer. In the developed gate unit, the turn-on pulse current peak was reduced four times and the retrigger pulse peak two times compared to typical values.

As a consequence, the turn-ON stage, retrigger stage, back-porch stage, and reduced backporch stage (for coping with negative gate voltage) can be merged into a single ON stage and the size-dominant OFF channel (typically covers the most of the PCB area) can be significantly reduced.

The resulting gate driver topology is depicted in Fig. 4. The particular stages are marked on the photo of the resulting gate unit in Fig. 5. The logic and the control are implemented on the low-cost *Xilinx Spartan 6 SLX4* FPGA. In the following subsections, the particular functionality of the stages is explained and their design is studied.

A. Turn-OFF Channel

The turn-OFF channel has a simple task to connect the gate to -20 V voltage potential to discard the charge from the gate in order to turn OFF the GCT. During the turn-OFF process, the load current is completely commutated into the gate driver for the GCT to restore its blocking capability. As a consequence, the -20 V bus has to be buffered by a sufficiently high capacitance C_{off}.

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There are two scenarios that have to be considered for the design of the turn-OFF channel: the typical low-current turn OFF applied at high frequency and the single-time emergency turn OFF.

The minimum required capacitance

$$C_{\mathrm{off,min}} = \frac{Q_{\mathrm{off}}}{\Delta U_{C\mathrm{off}}} \tag{1}$$

can be determined, as described in [16], by the worst-case electrical charge that is extracted from the gate during the turn OFF Q_{off} and by defining the maximum voltage decrease on the capacitors $\Delta U_{C\mathrm{off}}$ during the turn OFF. Assuming the worst-case charge to be $Q_{\mathrm{off}} = 5$ mC and the maximum allowed voltage decrease to be 10 % of the rated voltage ($\Delta U_{C\mathrm{off}} = 2$ V), the required capacitance is $C_{\mathrm{off,min}} = 2.5$ mF, which is used as a target for the design. The value of the worst-case electrical charge was selected by adding an additional margin to the value of 3.5 mC that was characterized from the measured gate current for a 2 kV 1.5 kA turn OFF of 5.5 kV GCT at 25 °C (the details and waveforms are presented later in Section VI).

Additionally, (1) can be transformed to determine that the voltage decrease at rated operation of the resonant dc transformer is $\Delta U_{C\mathrm{off}} = 0.2$ V ($Q_{\mathrm{off}} = 0.5$ mC characterized for 2.5 kV 140 A turn OFF and $C_{\mathrm{off}} = 2.5$ mF). This value is sufficiently low to ensure that the turn-OFF duration is not impacted and that the turn OFF at the rated operation is robust.

To select the capacitors for the turn-OFF channel, the rated rms current has to be determined (this is practically defined by the turn-OFF behavior). At the considered 1.44 kHz operation, the rms current caused by the turn OFF was characterized to be 11.5 A.

In the literature, the capacitor C_{off} is typically implemented using electrolyte aluminum capacitors [14], [17], [19] or the ceramic chip capacitors [13], [16], [19]. While the electrolyte aluminum capacitors have clear cost advantages, they are rather bulky, have high stray inductance, and allow for only low rms currents, which leads to typical high number of parallel-connected capacitors that populate large area of the gate unit. In contrast, the ceramic capacitors allow for very high rms currents but have typically lower values of capacitance that further decreases with applied direct voltage. As a consequence, the solutions based on this technology are often costly and target minimum possible capacitance [13], which might impact the turn-OFF capability of the gate unit. In this paper, the polymer tantalum capacitors are selected as the technology, since these pose a trade-off between the two aforementioned technologies, allowing for higher capacitances while remaining small in size. In practical realization, 25 of 100 µF 25 V 1.9 A capacitors *T55D107M025C0060* were used in parallel to achieve the required capacitance.

The switch $\mathrm{S_{off}}$ is realized as six parallel low-profile MOSFETs *Infineon BSC034N06NS* with worst-case ON resistance of 3.4 mΩ each, which leads to almost negligible losses in the rated operation (≈ 75 mW). This high number of switches was selected to reduce the stray inductance of the turn-OFF channel and to provide the single-time turn-OFF capability of high current as each of these MOSFETs can conduct up to 450 A for the duration of 10 µs. Despite the possibly nonuniform distribution of the gate current, this should guarantee a turn-OFF capability of the gate unit of at least 2 kA.

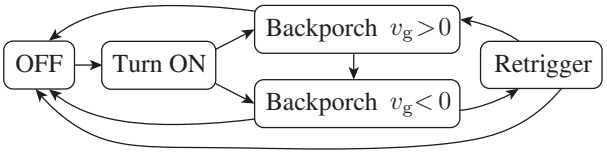

Fig. 6. Simplified finite state machine showing operation states of the gate unit.

In the photo of the gate unit in Fig. 5, it can be recognized that the MOSFETs and capacitors are placed in a close proximity of the GCT to minimize the stray inductance which is essential for the high-current turn-OFF capability [19]. The turn-OFF channel was not placed closer to comply with the existing mechanical constraints of the utilized stack. The lower part of the turn-OFF channel in the picture is the driving circuit for the MOSFETs.

B. ON Stage and Control Thereof

In order to be able to control the gate current for both positive and negative gate voltages in one converter stage, the ON stage has to be capable of generating both positive and negative voltages, leading to at-least two-level converter topology. However, since the gate voltage in the ON state of the GCT is typically around 1 V, the two-level converter topology would lead to a near 50 % duty-cycle operation during backporch current supply, which would in turn require relatively high switching frequency to keep the gate-current ripple low. Hence, we propose to implement a three-level T-Type NPC topology to provide three levels at the output and to utilize a nonlinear inductor to enable fast transients during the turn ON and slow transients during the backporch operation. The resulting topology of the ON stage is depicted in Fig. 4. Based on the voltage v_{on}, three switching states "-20V", "0V", and "+20V" are defined for the NPC stage, correspondingly.

To understand the functioning of the proposed gate unit (and the ON stage), the simplified finite state machine from Fig. 6 can be used. The complete control is implemented in the FPGA and the decisions are based on the comparator value of the gate voltage v_{g} (two states: positive or negative voltage) and a measurement of the ON-stage current i_{on} based on a shunt and a current-sense amplifier. Note that the current is not measured by an ADC but instead the amplifier output is connected to two comparators that are connected to two independent DAC channels. This way, the current crossings of values defined by the controller can be determined precisely and fast.

In the "OFF" state, the OFF channel is active (switch $\mathrm{S_{off}}$ is on) and thus the output of the ON stage is tied to -20 V potential to ensure that the current i_{on} does not increase. This state is held until the IGCT control signal does not request a turn ON via optical fibre (leading to a transition to "Turn ON" state in Fig. 6).

In the "Turn ON" state, the OFF channel is not deactivated immediately but first it is actively used to build up the current

in the inductor $L_{\rm on}$ together with the ON stage. By applying the "+20V" or "0V" switching state of the NPC stage, the voltage drop of 40 V and 20 V over the inductor $L_{\rm on}$ is generated, respectively [see Fig. 4]. The combination of these states within the turn-on delay of 3.5 µs is selected to build up a current $i_{\rm on} = 40$ A in the inductor. After the turn on delay is over, the turn-OFF channel is finally deactivated (switch $S_{\rm off}$ is OFF) and the inductor current is rapidly commutated into the gate, generating the turn-ON pulse. After that, the "0V" switching state is activated to decrease the gate current to its backporch value when the gate voltage $v_{\rm g}$ is measured positive. When the gate voltage is negative, the "-20V" switching state is applied to ensure that gate current decreases after the initial pulse (this is a sign that the antiparallel diode is conducting). After the gate current has reached the desired backporch current value, the backporch operation state is activated (transition from "Turn ON" to one of the "Backporch" states based on $v_{\rm g}$ polarity in Fig. 6).

In the backporch operation, the current is controlled by the fixed-ON-time hysteresis-control method utilizing one comparator to ensure the desired gate current level. When the gate voltage is positive, "+20V" switching state has a fixed period and the duration of "0V" switching state is determined by the comparator. Conversely, when the gate voltage is negative, "-20V" state has a fixed period and the duration of "0V" state is determined by the comparator. Note that during the positive gate voltage, the "fixed" ON-time period is slowly adaptively changed to track the desired switching frequency of 200 kHz.

When the gate voltage becomes negative during the "backporch $v_{\rm g} > 0$" state, the backporch operation is simply continued with different switching states. However, when the gate voltage becomes positive during the "backporch $v_{\rm g} < 0$" state, a transition via a retrigger pulse is made. This is generated by applying the "+20V" switching state until the gate current reaches roughly 38 A. After, the current is slowly decreased using the "0V" switching state. Once the gate current has dropped sufficiently, the backporch operation is continued.

The transition to the "OFF" state is initiated by the IGCT control signal.

One of the particular challenges in the design of the ON stage is to decide on the value of the inductance for the inductor $L_{\rm on}$. On the one hand, the inductance should be sufficiently high during the backporch operation to ensure that acceptable ripple can be achieved without too high switching frequency (at switching frequency of 200 kHz, the required inductance is around 5 µH to achieve acceptable gate current ripple). On the other hand, the inductance should be sufficiently low to ensure a fast ramp up of the gate current to generate the turn-ON pulse and the retrigger pulse. The solution to this problem is to utilize a nonlinear saturable inductor that decreases its inductance with increasing currents.

To simplify the gate unit production, numerous commercially available inductors were characterized outside of their designed operation area to find one with a desirable nonlinear characteristic:

- the inductance has to be near the target value of 5 µH up to approx. 8 A which is the highest backporch current,
- the inductance at high currents should be as low as possible to allow for fast increase of the current, while
- the inductance has to drop continuously to ensure similar turn-ON-pulse current peak for temperature variations and production tolerances.

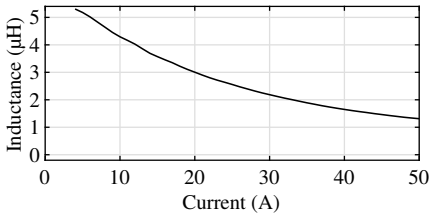

Fig. 7. Characteristic $L_{\rm on}(i_{\rm on})$ of the inductor selected for the ON channel.

Additionally, the inductor should have low winding resistance to omit hotspots on the PCB. Based on these requirements, inductor *Würth Elektronik 7443551470* was selected as a sufficiently good fit for the application (a better results would be possible only with a custom inductor design). The measured characteristic of this inductor is plotted in Fig. 7. The application of nonlinear inductor not only increases the dynamics of the current transients but also reduces the energy that is stored in the inductor, which is directly linked to the size of the inductor and to the loading of the voltage doubler stage.

Note that in contrast to the typical gate unit operation [12], [13], [17] where the backporch current is reduced when the gate voltage becomes negative, the backporch current is increased to 9 A in the proposed gate unit in order to accelerate the build up of the retrigger pulse. This is possible because the excessive energy during this kind of operation is not dissipated but it is recuperated into the capacitor $C_{\rm off}$.

C. Power Supplies

The gate unit is to be supplied from an isolating power supply with an input voltage range from 25 V to 40 V. Since the main power flow is expected to be via the turn-OFF channel, the main power supply is designed to directly supply the voltage bus for this channel. All other voltages on the gate unit are derived from this bus (that is buffered by a high capacitance $C_{\rm off}$).

As can be seen in Fig. 4, the main power supply is implemented as a simple buck converter that generates the voltage bus from 0 V potential to −20 V potential. The converter is controlled by a dedicated IC with an integrated overcurrent protection at switching frequency of 400 kHz.

Since the ON channel requires also +20 V bus, a resonant voltage doubler topology, as introduced in [20], is applied to generate it. The doubler is controlled by an FPGA in the open loop at 50 % duty cycle. The switching frequency of 350 kHz was selected to be sufficiently below the resonant frequency (ranging from 372 to 480 kHz due to tolerances) to ensure zero-current switching. The resonant voltage doubler is started up by an increasing frequency sweep.

Furthermore, there are several auxiliary power supplies implemented on the PCB to supply the MOSFET drivers, the FPGA, and the analog circuits.

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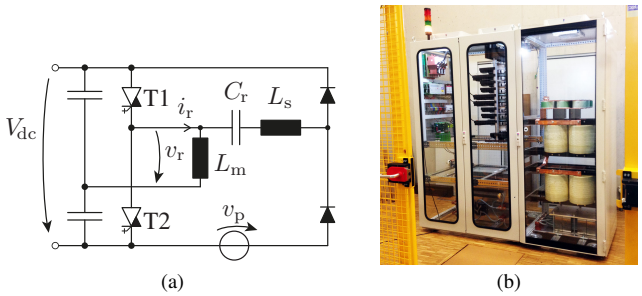

(a) (b)

Fig. 8. Experimental test setup for resonant testing of IGCTs: (a) schematic (b) photo.

D. Additional Functions and Safety Features

As mentioned before, the communication with the driver is realized via one bidirectional fibre-optic channel (for receiving the switching signal and sending internal status of the gate unit). Additionally, a second bidirectional fibre-optic channel is added to interlock the gate units in a case of an error or a failure.

The ensure a safe operation, all voltage buses are supervised by dedicated comparators and an anode-voltage measurement (via external 5 MΩ resistor connected via connector labeled as "Anode Connection" in Fig. 5) is implemented to detect an overvoltage. Moreover, it is detected whether the voltage has become high after the turn OFF. Since in the ZVS operation, the voltage becomes high after each turn OFF, an absence of the voltage likely signifies a failure of the GCT (this information is distributed by the second fibre-optic channel to protect the other GCT from shoot-through). This protection method is possible because IGCTs fail exclusively in short-circuit.

V. Validation in Resonant Operation

To validate the capability of the IGCT gate unit that was designed for the resonant dc transformer applications, a dedicated resonant IGCT test setup that was presented in [9] was utilized [see Fig. 8]. While this test setup does not process power, it forces the same working conditions on the IGCTs as the dc transformer based on LLC resonant converter that is depicted in Fig. 2 and can be used to perform the long-time continuous tests. In the setup, the low-current medium-voltage power supply generates voltage V_{dc} that determines the triangular magnetizing-current component together with the inductor L_{m}. A high-current low-voltage power-supply v_{p} excites the resonant tank in order to build up the required resonant peak current. The relevant parameters are summarized in Table I and the gate unit is fitted with a 5.5 kV 900 A reverse-conducting GCT *ABB 5SHX 1445H*.

The waveforms resulting from the resonant operation are plotted in Fig. 9, showing the gate voltage v_{g}, the ON stage voltage v_{on}, the gate current i_{g}, the anode-to-cathode voltage v_{T}, and the anode current i_{T} of the instrumented IGCT. Note that the gate voltage in the third graph is a detail view of the first graph. The gate current i_{g} was measured by four miniature Rogowski coils *PEM CWT Ultra-mini* positioned around the four gate connections of the GCT. For better readability of the graphs, all waveforms were filtered by a high-order 5 MHz low-pass filter in the post-processing. Furthermore, the offsets of the Rogowski coils were removed manually.

In Fig. 9b, the gate unit functioning during the full load operation can be observed. At the beginning, the driver keeps the GCT OFF by forcing gate voltage to $v_{\mathrm{g}} = -20$ V. Once the turn ON command is obtained, the ON stage voltage v_{on} is first increased to 20 V and later to 0 V to build up the current in the inductor L_{on}. After the turn-ON delay of 3.5 µs, the OFF-channel is deactivated, and the inductor current is commutated into the GCT's gate. After, the ON-stage voltage is kept as $v_{\mathrm{on}} = 0$ V until the gate current i_{g} naturally decays to ≈ 6 A. Subsequently, the backporch operation is activated to actively control the gate current at this current level with two voltage levels (v_{on} is either 20 V or 0 V) with an approximate switching frequency of 200 kHz. When the turn-OFF command comes, the negative voltage is applied again ($v_{\mathrm{g}} = v_{\mathrm{on}} = -20$ V) which transiently results into a high negative peak of the gate current until the GCT successfully turns OFF.

During the no-load operation, displayed in Fig. 9a, the situation is slightly more complex for the gate driver. While the initial steps during OFF state and the turn ON are identical to the full load operation in Fig. 9b, the negative current through the antiparallel diode in the no-load operation forces the PN junction near anode of the GCT to avalanche break which results into the negative gate voltage. As can be seen in Fig. 9a, once the gate unit recognizes that the gate voltage has become negative, the ON-stage voltage is set to $v_{\mathrm{on}} = -20$ V until the gate current decreases to the required backporch value of 9 A. After, the current is actively controlled by the ON stage by the two voltage levels -20 V or 0 V. When the gate unit recognizes that the gate voltage approaches zero, the retrigger gate-current pulse is generated by applying an ON-stage voltage of $v_{\mathrm{on}} = 40$ V until the required current value is reached. As can be seen, this pulse is sufficient to close the intrinsic gate-to-anode diode within the GCT and the gate voltage becomes $v_{\mathrm{g}} \approx 1$ V. After the current pulse has decayed, the backporch operation for $v_{\mathrm{g}} > 0$ is entered as in the full-load operation.

Fig. 10a and Fig. 10b show the detail of the turn-OFF transient for both no-load operation and full-load operation, respectively. The waveforms represent the zoomed in and unfiltered version of the waveforms from Fig. 9. These waveforms show that after a short reverse recovery peak of ≈ 400 A, the GCT current $i_{\mathrm{T}} = 140$ A is completely commutated into the gate unit before blocking voltage can be built up. Furthermore, a mild preflooding effect in the GCT can be observed, as the turn-OFF delay is slightly longer in the full-load operation than in the no-load operation.

To validate the thermal design of the proposed gate unit, a thermal picture of the stack, displayed in Fig. 11, was taken in a continuous operation. In Fig. 11, it can be recognized that the overall temperature of the driver is relatively low (around 35 to 50 °C) with only two hotspots of 66.4 °C at the inductor L_{on} (due to the relatively high winding resistance) and 70.6 °C at the current-measuring shunt. In summary, the temperatures can be described as safely low, considering that there is no forced

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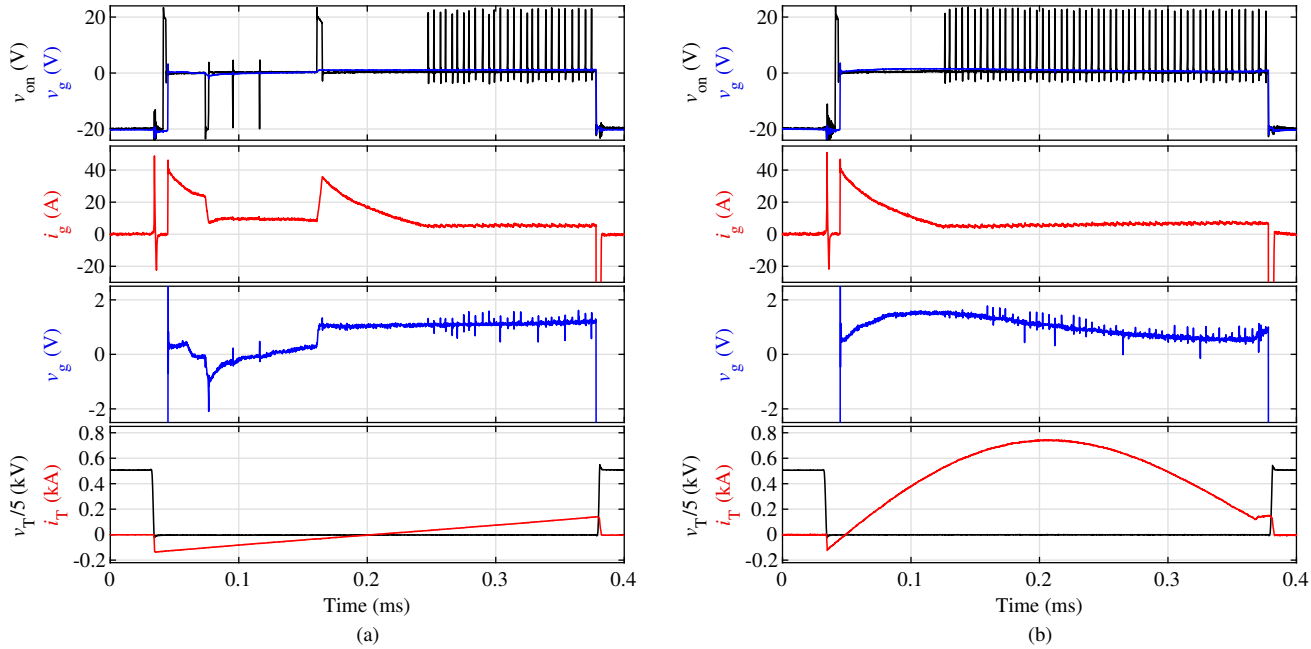

Fig. 9. Experimental validation of the gate driver in the resonant operation that emulates conditions of a dc transformer application: (a) no-load condition (b) full-load condition. All waveforms were filtered by a high-order 5 MHz low-pass filter in post-processing and the offsets of the Rogowski coils were removed manually. The gate voltage v_g in the third graph is the detail view of the gate voltage from the first graph.

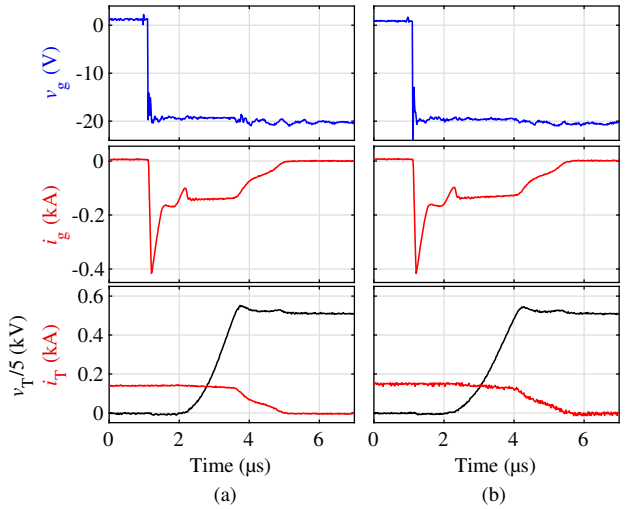

Fig. 10. Detail of the experimental waveforms from Fig. 9 showing the turn OFF detail: (a) no-load condition (b) full-load condition. The waveforms are unfiltered.

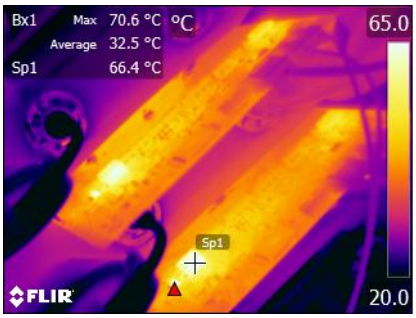

Fig. 11. Steady-state thermal picture of the gate units after 20 minutes of continuous operation at rated voltage and turn-off current.

cooling of the gate unit in the cabinet, the room temperature was ≈ 30 °C, and the case temperature of the GCT is 50 °C.

The long-time continuous operation of the test setup without any current-crowding failures further confirms that the decreased magnitude of turn-on and retrigger pulses is sufficient for the given application.

Finally, the consumption of the gate unit was measured to be ≈ 24 W, which is a fraction of the rated power of commercial drivers in hard-switched operation (consumption up to 130 W [18]). As a consequence, not only the gate unit size can be reduced but the size of the input power supply, providing isolation for medium voltage, as well. Furthermore, the consumption measurement was repeated also for the commercial gate unit, designed for hard-switched applications and depicted in Fig. 1 left. Under the same soft-switching operating conditions, the measured consumption was ≈ 31 W, which is significantly higher compared to the designed unit, despite the fact that the commercial unit has an external main supply (and thus, its consumption is expected to be even higher). Hence, it can be concluded that the designed gate unit, tailored for soft switching, is more efficient in the target operation than the commercial one.

VI. High-Current Turn-OFF Validation

To validate the single-time turn-OFF capability for high currents, a single-pulse setup was built around a hydraulic press (providing pressure to the stack), consisting of one IGCT, one diode, a 200 µF dc-link capacitor, and a 100 µH air-core inductor. Fig. 12 shows the schematic and the picture of the setup. Before each experiment, the capacitor is precharged

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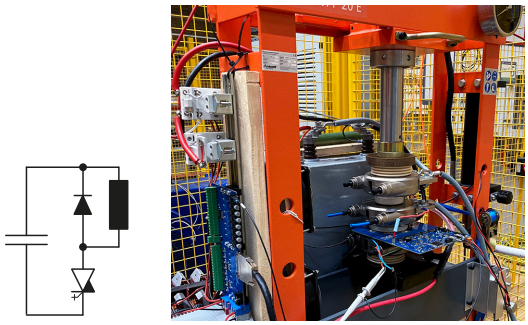

(a) (b)

Fig. 12. Utilized single pulse setup for high-current turn-OFF capability tests: (a) schematic (b) photo.

to the desired voltage level by a low-current medium-voltage power supply. To demonstrate high turn-OFF capability of the gate unit without risking a possible destruction of the GCT, the unit was fitted with a 5.5 kV 1.6 kA GCT from *ABB* (now *Hitachi Energy*) that allows for higher currents. (Since this GCT has generally higher switching losses, it is not suitable for the resonant operation.)

The results of the experiment can be seen in Fig. 13, showing the IGCT turn OFF at 2 kV and 1.5 kA. The waveforms clearly demonstrate the capability of the gate unit to provide the single-time emergency turn OFF for high currents (a sufficiently long period has to be applied to recharge the capacitors before the next turn ON can be applied). The observable discharge of the capacitor bank C_{off} is only $\Delta v_{C\text{off}} \approx 1$ V, which is in agreement with the expectations. Moreover, the stray inductance of the turn-OFF channel

$$L_{\text{stray}} \approx \frac{v_{C\text{off}} - v_{\text{g}}}{\mathrm{d}i_{\text{g}}/\mathrm{d}t} = \frac{6\ \text{V}}{5.05\ \text{kA/µs}} = 1.19\ \text{nH} \qquad (2)$$

could be identified as a function of the initial rate of rise of the gate current $\mathrm{d}i_{\text{g}}/\mathrm{d}t$ directly after turn OFF and by assuming that at the beginning, the voltage of the OFF-channel capacitor C_{off} stayed constant: $v_{C\text{off}} = 20$ V. This value can be considered as very low, when compared to the stray inductance of 1.1 nH of significantly larger commercial gate unit for 4 kA IGCTs [15].

VII. Conclusions

This paper has presented an IGCT gate unit design optimized for soft-switching dc-transformer application. The application specifics were presented together with the considerations during the design. The feasibility of the gate unit design was confirmed by an experimental validation with a GCT under resonant conditions.

The paper clearly demonstrates that in this application, several functions can be integrated into a single turn-ON stage with reduced turn-ON-pulse and retrigger-pulse capabilities. These pulses can be reduced in magnitude as the $\mathrm{d}i/\mathrm{d}t$ of the current after turn ON is limited by the application and thus, the thyristor cells have significantly more time to uniformly open. Furthermore, the turn-OFF channel can be reduced as well, since in the resonant operation, only very low currents are turned OFF. As a consequence, both the size of the proposed gate unit and its consumption can be reduced compared to the commercial gate units designed for hard-switching applications.

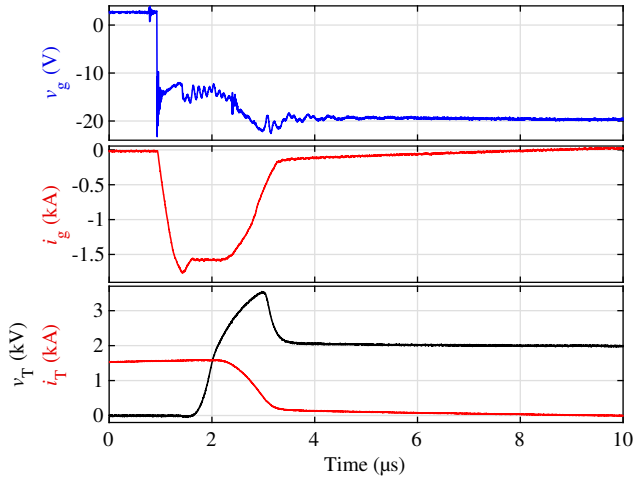

Fig. 13. Test of high-current turn-OFF capability of the gate unit measured at a single-pulse testbench, showing an IGCT turn OFF at 1.5 kA and 2 kV.

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References

[1] J. Kucka and D. Dujic, "Smooth power direction transition of a bidirectional LLC resonant converter for dc transformer applications," *IEEE Transactions on Power Electronics*, vol. 36, DOI 10.1109/TPEL.2020.3038467, no. 6, pp. 6265–6275, 2021.

[2] K. Tomas-Manez *et al.*, "Unregulated series resonant converter for interlinking dc nanogrids," in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, pp. 647–654, 2017.

[3] C. Zhao *et al.*, "Power electronic traction transformer—medium voltage prototype," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, 2014.

[4] J. Xu *et al.*, "PWM modulation and control strategy for LLC-DCX converter to achieve bidirectional power flow in facing with resonant parameters variation," *IEEE Access*, vol. 7, pp. 54 693–54 704, 2019.

[5] T. Guillod *et al.*, "Active magnetizing current splitting ZVS modulation of a 7 kV/400 V dc transformer," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1293–1305, 2020.

[6] W. Mei *et al.*, "A novel bidirectional control strategy for LLC resonant converter in high voltage application," in *2019 IEEE Vehicle Power and Propulsion Conference (VPPC)*, pp. 1–5, 2019.

[7] D. Stamenkovic *et al.*, "IGCT low-current switching – TCAD and experimental characterization," *IEEE Transactions on Industrial Electronics*, vol. 67, DOI 10.1109/TIE.2019.2939996, no. 8, pp. 6302–6311, 2020.

[8] D. Stamenkovic *et al.*, "Soft switching behavior of IGCT for resonant conversion," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, DOI 10.1109/APEC.2019.8722039, pp. 2714–2719, 2019.

[9] D. Stamenkovic and D. Dujic, "Soft-switching resonant conversion with IGCT," in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, DOI 10.23919/ICPE2019-ECCEAsia42246.2019.8796958, pp. 780–786, 2019.

[10] D. Dujic *et al.*, "Characterization of 6.5 kV IGBTs for high-power medium-frequency soft-switched applications," *IEEE Transactions on Power Electronics*, vol. 29, DOI 10.1109/TPEL.2013.2259264, no. 2, pp. 906–919, 2014.

[11] J. Deng *et al.*, "Design of llc resonant converters based on operation-mode analysis for level two phev battery chargers," *IEEE/ASME Transactions on Mechatronics*, vol. 20, DOI 10.1109/TMECH.2014.2349791, no. 4, pp. 1595–1606, 2015.
[12] H. Gruening *et al.*, "6 kV 5 kA RCGCT with advanced gate drive unit," in *Proceedings of the 13th International Symposium on Power Semiconductor Devices ICs. IPSD '01 (IEEE Cat. No.01CH37216)*, DOI 10.1109/ISPSD.2001.934574, pp. 133–136, 2001.
[13] H. Gruening and K. Koyanagi, "A modern low loss, high turn-off capability GCT gate drive concept," in *2005 European Conference on Power Electronics and Applications*, DOI 10.1109/EPE.2005.219695, pp. 10 pp.–P.10, 2005.
[14] Q. Chen and Q. Rui-chang, "Research on a novel gate drive circuit of integrated gate commutated thyristor," in *2008 International Conference on Electrical Machines and Systems*, pp. 2147–2149, 2008.
[15] B. Backlund and M. Luescher, "Recent developments in IGCT gate units," in *2007 European Conference on Power Electronics and Applications*, DOI 10.1109/EPE.2007.4417564, pp. 1–7, 2007.
[16] T. Butschen *et al.*, "Gate drive unit for a dual-GCT," in *8th International Conference on Power Electronics - ECCE Asia*, DOI 10.1109/ICPE.2011.5944717, pp. 2419–2426, 2011.
[17] L. Xie *et al.*, "The design of IGCT gate-unit equipped in the three-level NPC converter," in *2011 International Conference on Electrical Machines and Systems*, DOI 10.1109/ICEMS.2011.6073530, pp. 1–6, 2011.
[18] *Applying IGCT gate units, Application note 5SYA 2031-05*, ABB, 2017.
[19] Z. Chen *et al.*, "Stray impedance measurement and improvement of high-power IGCT gate driver units," *IEEE Transactions on Power Electronics*, vol. 34, DOI 10.1109/TPEL.2018.2826046, no. 7, pp. 6639–6647, 2019.
[20] J. Valdez-Reséndiz *et al.*, "Resonant switched capacitor voltage multiplier with interleaving capability," *Electric Power Systems Research*, vol. 133, DOI https://doi.org/10.1016/j.epsr.2015.12.037, pp. 365–372, 2016. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0378779615004149

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