IEEE Access, vol. 9, pp. 151 493–151 506, 2021

Hardware-in-the-Loop Modeling of an Actively Fed MVDC Railway Systems of the Future

S. Milovanović, S. Strobl, P. Ladoux, *et al.*

POWER ELECTRONICS LABORATORY
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received October 11, 2021, accepted October 29, 2021, date of publication November 2, 2021, date of current version November 15, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3125050

Hardware-in-the-Loop Modeling of an Actively Fed MVDC Railway Systems of the Future

STEFAN MILOVANOVIĆ[1], (Member, IEEE), SIMON STROBL[2], PHILIPPE LADOUX[3], (Member, IEEE), AND DRAŽEN DUJIĆ[1], (Senior Member, IEEE)

[1]Power Electronics Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
[2]Imperix, 1950 Sion, Switzerland
[3]Université de Toulouse, CNRS, INPT, UPS, LAPLACE, 31077 Toulouse, France

Corresponding author: Stefan Milovanović (stefan.milovanovic@epfl.ch)

This work was supported in part by the European Union's Horizon 2020 Research and Innovation Programme (Future Unified DC Railway Electrification System (FUNDRES) Project) under Grant 881772, and in part by the Swiss Innovation Agency—Innosuisse under Innovation Project 38041.1 IP-ENG.

ABSTRACT This paper presents an averaged real-time model of an arbitrary size MVDC railway system. In contrast to references already available in the literature, focusing mainly on specific parts of such a railway network (e.g. power converter installed in a locomotive), this paper offers a thorough insight into the modeling of every part belonging to it. Through a set of reasonable assumptions, the concept of a sector is presented allowing for a straightforward synthesis of any MVDC railway network. Thereafter, real-time models of catenaries, rails, trains, as well as power converters supplying the system are presented in a comprehensive manner. Without loss of generality, the system analyzed hereafter represents a 200 km section of a double-track EuroCity line powered by an actively fed electrification system with three transformer-rectifier groups and two modular multilevel converters. The proposed modeling approach was verified on a large-scale hardware-in-the-loop system comprising one RT Box 3, hosting the model of the exemplary railway network, and two modular multilevel converter digital twins relying on the use of industrial ABB PEC800 controllers.

INDEX TERMS Railway modeling, hardware-in-the-loop, RT Box, MVDC railway systems.

I. INTRODUCTION

For decades, the European Union (EU) has been making efforts towards the concept of a Single European Transport Area [1]. By unifying its transportation sector, the EU intends to improve the free movement of individuals, services and goods, which is at the heart of its single market. However, such a goal requires the ever extending transport infrastructure to cut ties with fossil fuel technologies due to concerns with pollution and sustainability. Consequently, extending its already large electric railway infrastructure and establishing a Single European Railway Area (SERA) represents one of the important ambitions of the EU.

Throughout Europe, railway systems are mainly differentiated by their voltage, with the most typical levels being 600 V_{DC}, 750 V_{DC}, 1.5 kV_{DC}, 3 kV_{DC}, 15 kV_{AC} (16.7 Hz) and 20 kV_{AC} (50 Hz) [2]. Such a wide variety of systems is a major hurdle for the creation of SERA as it limits the interoperability of rolling stocks. In this context, references [3], [4] introduced the potential of a new 9 kV_{DC} electrification system. Such a system is intended to replace the existing 1.5 kV_{DC} and 3 kV_{DC} railway lines, with the aim of improving the traffic capacity and overall system efficiency. In the existing 1.5 kV_{DC} and 3 kV_{DC} railway networks, the energy is usually delivered by Transformer-Rectifier Groups (TRGs) [4] (e.g. 6-, 12- or 24-pulse rectifiers). This technology is well known, efficient, robust and can be easily upscaled to support the need of the 9 kV_{DC} system. Notwithstanding the simplicity, efficiency and robustness of TRGs, the proposed voltage level opens the door for the use of Modular Multilevel Converters (MMCs) [5], which, in railway applications, offer potential advantages over Diode Rectifier (DR)-based configurations:

- In a TRG, the output voltage drops with an increase in the load current due to commutation caused by the transformer leakage inductance [6]. This drop affects the pantograph voltage, which can be considered a drawback given that the pantograph voltage is supposed to stay within a predefined range. The MMC, however, can control the voltage across its DC terminals [7],

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

irrespective of the load current. Thus, the minimum pantograph voltage is expected to be higher if some TRGs are replaced with MMCs.

- When a train decelerates, some of the braking energy can be recovered and injected back into the overhead lines. Unfortunately, TRGs are unidirectional. Therefore, if there is no train in the vicinity to consume this energy, the excess is dissipated in the Voltage Limiting Unit (VLU) installed on the roof of the locomotive. One way to prevent this waste is to install super-capacitors and/or batteries inside the locomotive [8] or at the railway stations [9]. The excess energy is temporarily stored and used later to accelerate the train when it leaves the station. Another method relies on the bidirectional nature of the MMC, which enables one to inject the excess energy into the AC grid and recover it later.
- DRs have no capability of reactive power control, while causing significant harmonic pollution on both AC and DC sides. As a result, reactive power compensators and filters are normally required. With the MMC, however, these are not needed as active and reactive power can be controlled independently, while ensuring an outstanding quality of AC currents due to its multilevel nature [7], [10], [11].
- In the case of a fault, an MMC realized with Full-Bridge (FB) cells can counter short-circuit currents by producing a negative voltage [12], [13].

Prior to deploying any technology in the field, especially if massive and expensive High Voltage (HV) or Medium Voltage (MV) systems are considered, control verification in a risk-free environment is more than recommended. For this reason a Hardware-in-the-Loop (HIL) replica of the MMC described in [14] was developed and presented in [15], [16]. Essentially, the converter power stage is emulated in the real-time simulator, while the actual control hardware is interfaced with the later using standard I/O connections. This way, the controller is never able to differentiate between the simulator and the real power hardware. In order to assess the performance of the MMC in railway applications, the digital twin of an MMC needs to be extended with a real-time model of an entire 9 kV_{DC} railway line, which is the main purpose of this work. At first glance, developing the real-time model of an Medium Voltage Direct Current (MVDC) railway system might seem a trivial task. Nonetheless, several technical challenges, listed below, can be associated to it:

- In general, hardware capabilities of an employed simulator impose a hard limit on the complexity of a network model. Railway systems are particularly demanding for two reasons. Firstly, the network topology varies over time depending on the number of trains and their positions within the network itself. Unfortunately, some real-time simulators cannot handle circuits with time-varying parameters (e.g. RT-Box [17]). Secondly, the switching behavior of train converters requires extremely small simulation step-sizes, which are quite often unrealistic in case a large-scale system is simulated. In other words, simulation speed/fidelity contradicts the requirement of simulating the system being as large as possible.
- Real-time simulation of TRGs and trains represents a demanding task for simulators solving the circuit equations in the state-space (e.g. RT-Box and TyphoonHIL) since the number of state-space matrices is directly tied with the number of switches in the system. What is more, in the circuit with N switching elements, the number of different state-space matrices equals 2^N. To avoid online calculation of system matrices, which happens to be time consuming, these are normally pre-computed and stored in the simulator memory. On these terms, a set of matrices, used in the upcoming simulation step, must be selected and loaded from memory, which is an inevitable time expense. From here, it can be concluded that the more TRGs and trains in the simulated network, the higher the simulation step-size requirements.

So far, modeling of railway systems, in a broader sense, has been addressed on multiple occasions. In [18], an analysis of rail potential and stray currents in an MVDC railway system was provided. However, such an analysis requires the rail model comprising a significant number of switches. According to the previous paragraph, such an approach is not suitable for real-time simulations. Reference [19] contains a detailed overview of MVDC railway systems, however, no modeling (neither offline nor real-time) is discussed. Similar conclusion stands for [20], where an MVDC railway system is proposed, however, no details on modeling are presented. Substantial amount of documentation on MVDC railway systems was published within *Shift2Rail* project [21]. Nonetheless, these studies are dedicated to potentials of MVDC technology in the railway domain and not to real-time modeling of systems they are proposing. In [22], offline model of an MVDC railway line containing two power stations and one train was proposed. The railway line was modeled in Simulink with a variable resistance block, which happens to be unavailable in some real-time simulators (e.g. RT Box) for the reasons falling outside of this paper's scope. Therefore, this modeling approach is not considered suitable for real-time simulations. Similar conclusion can be drawn in the case of [23], where offline modeling of an on-board hybrid energy storage systems for railway applications was discussed. Publication [24] provides an insight into real-time simulation of a converter/machine pair installed on the rolling stock. However, no other details were provided on modeling of the rest of the railway system. Identical conclusions can be made in the case of [25]–[28].

The work presented in [29] provides an information on real-time modeling of an AC railway network, where system admittance matrices are solved on dSPACE platform, which significantly differs from the simulator chosen for this work. Similarly, real-time model concerning mechanical parts of the train was introduced in [30], while the other system parts were tested by means of a reduced-power test bed. Similar idea was used in [31]. Once again, models mentioned

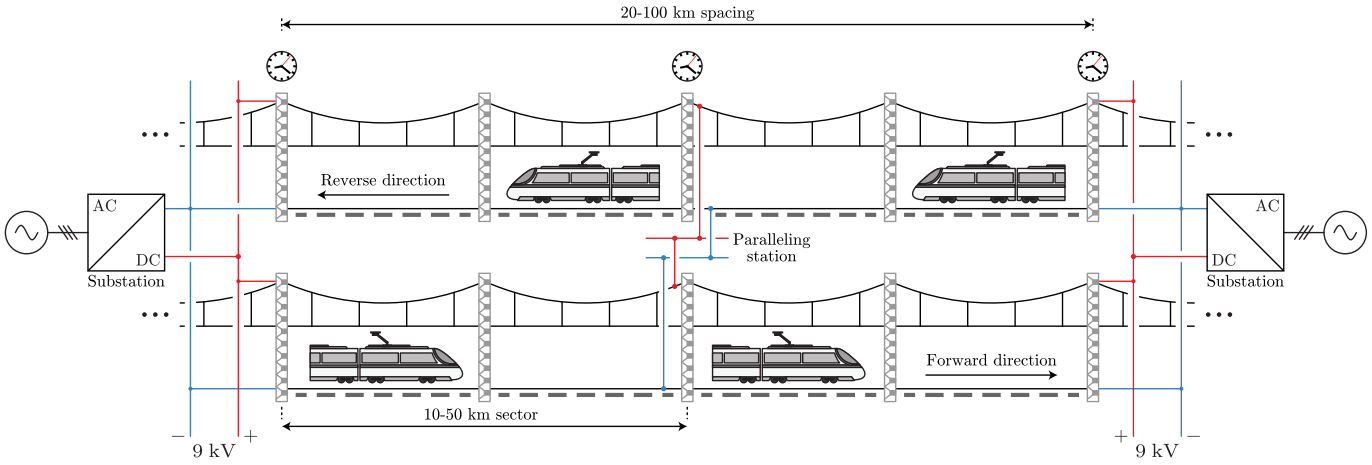


FIGURE 1. Double-track 9 kV_{DC} railway line. AC-DC converter block can designate either a TRG or an MMC.

in [30], [31] were implemented on dSPACE platform, making them different compared to ones discussed herewith. References [32], [33] touch on the topic of railway modeling, however, only on the converter level, while other parts existing in the railway system are not necessarily mentioned. In [32], device-level modeling of an MMC, operating as a 25 kV_{AC} traction feeder, was presented, while similar principles were discussed in [33] for the MMC operating as a rolling-stock converter.

As can be seen, most HIL models for railway applications focus on a specific part of the system, such as the traction system [24]–[28], [32]–[35] or the traffic management [36]. To the best knowledge of the authors, the only publication presenting the real-time model of a complete DC railway line considers a simple network with two substations, two trains and an ideal rail with no linear resistance [37]. What is more, it focuses on a peculiar topology with a superconductor wire in parallel with the catenary. The aim of the current work, however, is to propose a systematic way to deal with larger networks and all the parts comprising them, which is considered its most important contribution.

Forthcoming paragraphs provide a thorough insight into the real-time modeling of all the parts comprising an MVDC railway network - catenaries, rails, trains and converters supplying the network itself. The employed modeling techniques allow an essentially time-varying circuit to be replaced with a time-invariant counterpart, which enables the use of simulators incapable of operating with time-varying elements. Through a set of reasonable assumptions, averaging of the train and TRG models is introduced, leading to a significant reduction in the number of state-space matrices describing the considered system. In other words, the approach presented hereafter provides a model suitable for the system load flow studies, which comes in handy especially if the potential of a certain solution (e.g. MVDC railway network incorporating MMCs) is to be compared to its traditional counterparts (i.e. solutions relying on the use of mature technology such as TRG).

The rest of the paper is organized as follows. **Sec. II** includes a general system overview supported by a set of assumptions adopted in the upcoming paragraphs. **Sec. III** provides an in-detail model of the sector, including transmission line and rail models. **Sec. IV** deals with the train modeling, as well as relevant speed/power profiles of trains considered by this work. **Sec. V** covers the topic of the substations' modeling. Finally, **Sec. VI** contains the description of setup used to verify the modeling approach presented herewith along with the results obtained by means of it.

II. SYSTEM OVERVIEW AND GENERAL ASSUMPTIONS

The railway network under study is directly inspired by the double-track line proposed in [3] and it is illustrated in **Fig. 1**. Electric power facilities (substations) are either TRGs or MMCs and they are distributed at regular distances along the line. The power is then injected into a catenary system and shared between tracks by connecting them in parallel at the substations and half-way in-between paralleling stations. Finally, the current is collected by pantographs and circled back to the substations through the rails.

Since 9 kV_{DC} locomotives do not exist yet, the train used in this work is a modified EC 250 "Giruno" from the Schweizerische Bundesbahnen (SBB) [38], Switzerland. This is a high-speed train built by Stadler Rail operating between Frankfurt and Milan through the Gotthard Base Tunnel in Switzerland. Also, it is certified to operate in Austria. Since the electrification systems are not unified between these countries, the EC 250 must support multiple supply voltages: 15 kV_{AC}/16.7 Hz, 25 kV_{AC}/50 Hz and 3 kV_{DC} with the later being used in Italy. In this work, it is assumed that the EC 250 can be modified to support 9 kV_{DC} instead of 3 kV_{DC}. Characteristics of this train are summarized in **Tab. 1**.

In [3], the authors presented a method of sizing a DC railway network based on the load-flow analysis, the purpose of which was to ensure that the line respects the constraints related to temperature, voltage range and rail-to-ground voltage at all times. Once the choice of the rail and the overhead

TABLE 1. Parameters of the train [38] used for the case study.

Name	Cruise speed	Rated power	Traffic
EC 250 Giruno (RABe 501)	250 $\frac{\text{km}}{\text{h}}$	6 MW	EuroCity (EC)

TABLE 2. Overhead line electrical parameters.

Substation spacing	Cross-section	Resistivity	Linear resistance
50 km	250 mm^2	18.8 $\frac{\Omega\text{mm}^2}{\text{km}}$	0.0752 $\frac{\Omega}{\text{km}}$

TABLE 3. Rail parameters.

Density	Resistivity	Linear resistance	Linear conductance
60 $\frac{\text{kg}}{\text{m}}$	0.9 $\frac{\Omega\text{kg}}{\text{km m}}$	0.015 $\frac{\Omega}{\text{km}}$	0.075 $\frac{\text{S}}{\text{km}}$

TABLE 4. Voltage range for a 9 kV_{DC} line, scaled up from a widely used 1.5 kV_{DC} system.

Nominal voltage (V_{n})	Minimum voltage (V_{min})	Maximum voltage (V_{max})	Open-circuit voltage of substations (V_{oc})
9 kV	6 kV	10.8 kV	10.5 kV

cable is made, the railway line sizing is constrained mainly by two parameters - the catenary cross-section and the spacing between substations. In general, the cross-section should be large enough to ensure a satisfactory current density, while the spacing between two neighboring substations should be as small as possible to limit voltage drops along the line. In this work, rails and overhead cables are of the same type as in [4], however, instead of 230 mm^2 the cable cross-section is set as 250 mm^2, while the spacing between two substations is chosen as 50 km instead of 40 km. Parameters of the overhead lines and rails can be found in **Tabs. 2** and **3**, respectively. Further, following the European Standard EN 50163 [39], the voltage range of a DC line for traction applications is limited. Even though this standard does not cover 9 kV_{DC} lines, the specifications for 9 kV_{DC} can be scaled up, as explained in [3], according to **Tab. 4**.

To deal with arbitrarily large networks, one can introduce the concept of a sector. Henceforward, a segment of the line where only two trains can circulate at a time (one per direction) will be referred to as the sector. The complete line is then built by connecting multiple sectors in series and adding equally spaced substations at the terminations of some sectors, as shown in **Fig. 1**. Considering the substations spacing previously adopted in **Tab. 2**, a 250 $\frac{\text{km}}{\text{h}}$ train would need between 2 m 24 s and 6 m to cross a sector. Given that a train must be able to perform an emergency braking without any collision, it is safe to choose a sector length of 25 km. This also means that the spacing between two adjacent trains is 25 km, which corresponds to a very dense high-speed train traffic. Nonetheless, such a schedule represents a very convenient scenario for the system performance verification.

The following statement comes rather as a fact than an assumption - the dynamics of the mechanical system is multiple orders of magnitude slower compared to the electric time constant in the system. Nevertheless, such an obvious conclusion contributes to a significant simplification of the railway line modeling suitable for the upcoming studies, as will be seen shortly. Further, irrespective of the type of a TRG (i.e. 6-, 12-, 24-pulses, etc.), its output voltage contains a certain amount of higher order harmonics (e.g. 6th, 12th, etc.). However, the locomotives, as will be seen in **Sec. IV**, include an on-board inductive filter which allows for a straightforward control of their currents to almost pure DC waveform. In other words, higher order harmonics present in the system voltage take no part in power transfer. Therefore, they can easily be ignored, allowing for the averaging of the TRG real-time model. Similar conclusion can be applied to the MMC considering high quality of its AC and DC voltages, which renders higher order harmonics in the railway network current rather insignificant.

III. MODELING OF THE SECTOR

A. TRANSMISSION LINE MODEL

Considering the adopted sector length of 25 km, it is appropriate to use a transmission line model for the catenary and the rail. Generally speaking, an infinitesimal segment of a transmission line can be modeled as shown in **Fig. 2a**, as discussed in [40]. The linear resistance R' accounts for the Joule losses of the line, L' sums up both the self-inductance of the line and the mutual inductance with the neutral conductor, C' is the parasitic capacitance between the line and the neutral, and G' represents conductance of a space separating the line from the ground.

As the railway line is DC, while the switching behavior of converters is ignored according to the previous section, the linear inductance and capacitance can be neglected. Additionally, the distance between the catenary and the rail is large enough to assume that the air acts as a perfect insulator [8]. Thus, the transmission line model of the catenary is simplified to a linear resistance, as illustrated in **Fig. 2b**. For the rail, however, the conductor is close to the ground. As a result, the insulation is usually imperfect, which leads to leakage currents (called stray currents in [3]) between the rail and the ground. **Fig. 2c** presents the transmission line model of the rail including the rail-to-ground leakage.

As for the catenary, the resistivity σ [$\frac{\Omega\,\text{mm}^2}{\text{km}}$] of the cable is known from a manufacturer's datasheet, and parameter to size is the cross-section S_{c}[mm^2] of the cable. The linear resistance is then

$$R'_{\text{cat}}\left[\frac{\Omega}{\text{km}}\right] = \frac{\sigma}{S_{\text{c}}}. \tag{1}$$

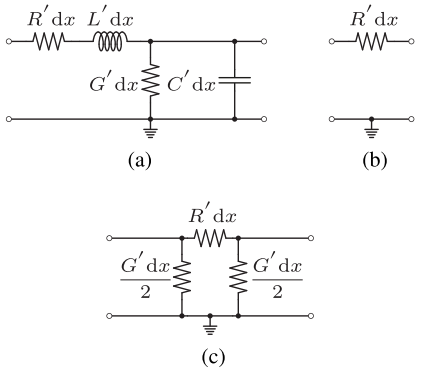


FIGURE 2. (a) Model of a generic transmission line; (b) Transmission line model of the catenary; (c) Transmission line model of the rail.

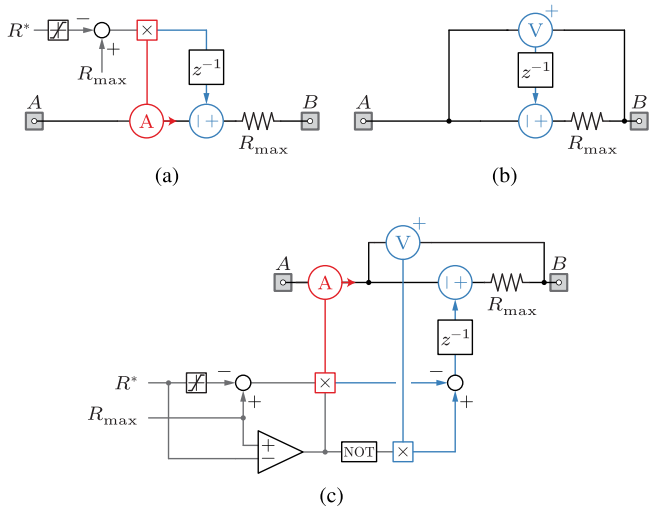


FIGURE 3. Implementation of a variable resistor suitable for real-time simulations: (a) Implementation based on current feedback; (b) Emulation of an infinite resistance; (c) Combination of the latter two.

Similarly, the resistivity $\sigma\,[\frac{\Omega\,\mathrm{mm}^2}{\mathrm{km\,m}}]$ of the rail is known from a manufacturer, and parameter to choose is the rail density $\rho\,[\frac{\mathrm{kg}}{\mathrm{m}}]$. The line resistance of the rail is then

$$R'_{\mathrm{rail}}\left[\frac{\Omega}{\mathrm{km}}\right] = \frac{\sigma}{\rho}. \tag{2}$$

Finally, the linear rail-to-ground conductance $G'_{\mathrm{rail}}\,[\frac{\mathrm{S}}{\mathrm{km}}]$ depends on materials used for the railway ties, the ballast and the rail insulators. It is fixed by the construction process. According to **Tab. 3**, this parameter equals $G'_{\mathrm{rail}} = 0.075\,\frac{\mathrm{S}}{\mathrm{km}}$.

As a train moves along the sector, catenary resistances left and right from it change. Consequently, the need for a variable resistor model becomes more than evident. While the majority of the offline simulators support the variable resistance model, circuit operation with variable parameters imposes a challenge for certain real-time simulators (e.g. RT Box [17]). Such a hurdle can be circumvented in by relying on the model depicted in **Fig. 3a**.

From here, one can establish the expression

$$v_{\mathrm{AB}}[k] = R^* i_{\mathrm{AB}}[k-1] + R_{\mathrm{max}}(i_{\mathrm{AB}}[k] - i_{\mathrm{AB}}[k-1]), \tag{3}$$

which can be further simplified based on the assumptions made in **Sec. II**. Namely, the dynamics of mechanical system happens to be several orders of magnitude slower compared to the electrical one. From the real-time simulator viewpoint, this means that there is barely any difference between two samples of current flowing through the analyzed block. Thus, one can assume that $i_{\mathrm{AB}}[k] \approx i_{\mathrm{AB}}[k-1]$, leading to

$$v_{\mathrm{AB}}[k] \approx R^* i_{\mathrm{AB}}[k], \tag{4}$$

which indicates that the structure from **Fig. 3a** behaves as a resistor with the resistance set externally as R^*. The lower and the upper saturation limits of R^* equal 0 and R_{max}, respectively.

In some cases, there is a need for an infinite resistance, however, including a resistor with a large resistance into the model can make matrices describing an analyzed system stiff. Therefore, another approach for modeling an infinite resistance was proposed in **Fig. 3b**. As can be seen, the current flowing between terminals labeled with A and B equals

$$i_{\mathrm{AB}}[k] = \frac{1}{R_{\mathrm{max}}}(v_{\mathrm{AB}}[k] - v_{\mathrm{AB}}[k-1]). \tag{5}$$

Since potentials of points A and B are supposed to stay unchanged over a few sampling periods of the real-time simulator, one can claim that $v_{\mathrm{AB}}[k] \approx v_{\mathrm{AB}}[k-1]$, leading to

$$i_{\mathrm{AB}}[k] \approx 0. \tag{6}$$

In other words, the circuit from **Fig. 3b** behaves as an open circuit, which is equivalent to an element having infinite resistance. Lastly, circuits from **Figs. 3a** and **3b** can be combined as depicted in **Fig. 3c**, which sets the framework for modeling of the double-track lines.

B. DOUBLE-TRACK LINE MODEL

Each train in the sector is moving along the line over time. Therefore, based on the transmission line model, the catenary is split into two variable resistances (left and right), as illustrated in **Fig. 4a**. However, when considering a double-track line, rails of both tracks are connected in parallel all along the line [3], [4]. The first consequence is that the rail is split into 3 sections (left, middle and right), since the distance between trains must also be considered. The second consequence is that the topology of the sector is different depending on whether or not the trains have crossed (please compare **Fig. 4a** and **Fig. 4b**).

A catenary resistance is computed from the position of the locomotive, length of the sector x_Σ and the linear resistance R'_{cat} as

$$R_{\mathrm{cat}}^{(\mathrm{left})} = R'_{\mathrm{cat}} x \tag{7}$$

$$R_{\mathrm{cat}}^{(\mathrm{rigth})} = R'_{\mathrm{cat}}(x_\Sigma - x). \tag{8}$$

The rail resistances depend on the position of the locomotives x_1 and x_2, the length of the sector x_Σ, linear resistance

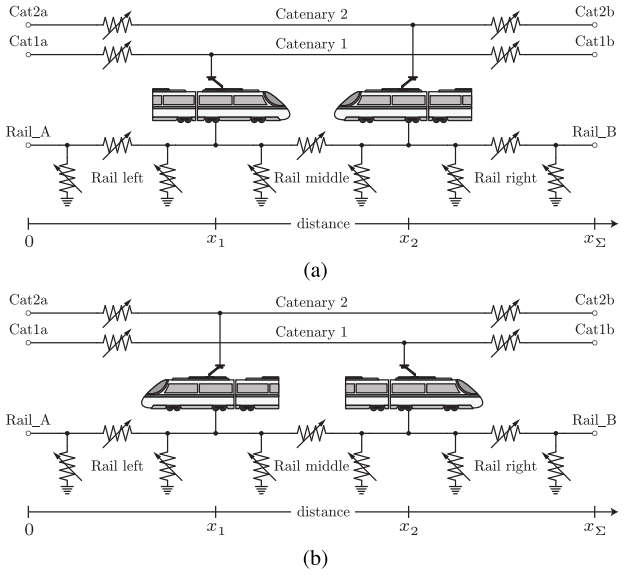


FIGURE 4. (a) Continuous model of a sector before the locomotives have crossed; (b) Continuous model of a sector after the locomotives have crossed.

R'_{rail} and the number of tracks in parallel (in this case two), denoted by N_t, according to the following expressions:

$$\forall\, x_2 > x_1 : \begin{cases} R_{\text{rail}}^{(\text{left})} = \dfrac{1}{N_\text{t}} R'_{\text{rail}}\, x_1 \\ R_{\text{rail}}^{(\text{middle})} = \dfrac{1}{N_\text{t}} R'_{\text{rail}}\, |x_2 - x_1| \\ R_{\text{rail}}^{(\text{rigth})} = \dfrac{1}{N_\text{t}} R'_{\text{rail}}\, (x_\Sigma - x_2) \end{cases} \tag{9}$$

$$\forall\, x_2 \leq x_1 : \begin{cases} R_{\text{rail}}^{(\text{left})} = \dfrac{1}{N_\text{t}} R'_{\text{rail}}\, x_2 \\ R_{\text{rail}}^{(\text{middle})} = \dfrac{1}{N_\text{t}} R'_{\text{rail}}\, |x_2 - x_1| \\ R_{\text{rail}}^{(\text{rigth})} = \dfrac{1}{N_\text{t}} R'_{\text{rail}}\, (x_\Sigma - x_1) \end{cases} \tag{10}$$

The rail-to-ground conductances are calculated in a similar way, as presented in (11) and (12). However, while implementing the model on an HIL simulator, one should be careful and recall that the rail conductance is split into two parts in the π-scheme, as illustrated in **Fig. 2c**.

$$\forall\, x_2 > x_1 : \begin{cases} G_{\text{rail}}^{(\text{left})} = N_\text{t}\, G'_{\text{rail}}\, x_1 \\ G_{\text{rail}}^{(\text{middle})} = N_\text{t}\, G'_{\text{rail}}\, |x_2 - x_1| \\ G_{\text{rail}}^{(\text{rigth})} = N_\text{t}\, G'_{\text{rail}}\, (x_\Sigma - x_2) \end{cases} \tag{11}$$

$$\forall\, x_2 \leq x_1 : \begin{cases} G_{\text{rail}}^{(\text{left})} = N_\text{t}\, G'_{\text{rail}}\, x_2 \\ G_{\text{rail}}^{(\text{middle})} = N_\text{t}\, G'_{\text{rail}}\, |x_2 - x_1| \\ G_{\text{rail}}^{(\text{rigth})} = N_\text{t}\, G'_{\text{rail}}\, (x_\Sigma - x_1) \end{cases} \tag{12}$$

What can be concluded is that the sector is actually to be represented with two circuits, the one of which is used depending on whether the trains have already met along the line or not. The switch-over between two circuits depicted in **Figs. 4a** and **4b** can be performed by extending the sector model by two ideal switches, however, such an idea contradicts the requirement of minimizing the number of switching components used in the model. As a result, another approach to the unification of circuits from **Figs. 4a** and **4b** must be relied upon.

In this particular case, it is not possible to use some averaged model of the sector as there is an interest to follow the displacement of trains as a function of time. Instead, the behavior of ideal switches can be emulated with variable resistances. By choosing parameters labeled with $R_{1\text{L}}$, $R_{2\text{L}}$, $R_{1\text{R}}$ and $R_{2\text{R}}$ according to (13) and (14), the circuit from **Fig. 5** can be made equivalent to either of those presented in **Figs. 4a** and **4b**.

$$\forall\, x_2 > x_1 : \begin{cases} R_{1\text{L}} = R_{\text{rail}}^{(\text{left})} \\ R_{2\text{R}} = R_{\text{rail}}^{(\text{right})} \\ R_{1\text{R}} = R_{2\text{L}} = \infty \end{cases} \tag{13}$$

$$\forall\, x_2 \leq x_1 : \begin{cases} R_{2\text{L}} = R_{\text{rail}}^{(\text{left})} \\ R_{1\text{R}} = R_{\text{rail}}^{(\text{right})} \\ R_{1\text{L}} = R_{2\text{R}} = \infty \end{cases} \tag{14}$$

The main advantage of the equivalent model from **Fig. 5** lies in the fact that a single electrical circuit represents the sector. Consequently, a railway line made of N sectors in a row is also described by a single circuit and a single set of state-space matrices. It is noteworthy that using infinite resistances does not make the system matrices stiff, thanks to the variable resistance implementation from **Fig. 3c**.

IV. TRAIN MODELING

A. LOCOMOTIVE

In 2021, locomotives supplied with 9 kV_DC do not exist yet. However, the conversion chain can be derived from existing locomotives supplied either with DC or AC voltage. The pantograph would likely be connected to an input filter, followed by a Power Electronic Traction Transformer (PETT) to isolate the traction unit from the catenary and step-down the voltage. At 9 kV_DC, PETT would rather imply a multilevel topology, where two main concepts, implying either partial (c.f. [41]) or bulk (c.f. [42]) power processing, depicted in **Figs. 6a** and **6b** are recognized. Thereafter, the rest of the propulsion chain would be the same as in existing locomotives [43]: a low voltage DC bus is protected by a VLU (typically, a non-isolated

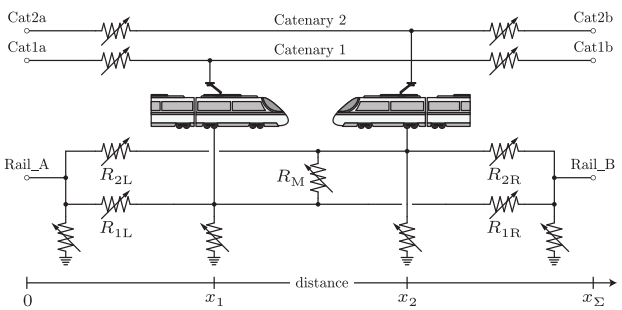


FIGURE 5. Sector model with non-ideal switches (variable resistors) intended to handle the crossing of the two trains. Parallel rail-to-ground shunts were merged together.

buck-type converter), and supplies multiple AC motors with their own inverters. Of course, several topologies are possible, and **Figs. 6a** and **6b** illustrate just a general idea. In either case, the conversion chain structure enables a high-bandwidth control of the current drawn from the pantograph. As a result, when observed from an overhead line, the train can be modeled with a controlled current source.

Obviously, the train current cannot take any arbitrary value since, in practice, power converter mounted on the train has a current limitation. According to [4], the locomotive should be able to operate at its nominal power until a certain lower threshold voltage is reached. For lower pantograph voltages, the converter enters the current limitation mode, leading to a linear drop of the maximal power. The effect of the current limitation is shown in **Fig. 7** with min/max pantograph voltages (c.f. **Tab. 4**) being labeled V_{min} and V_{max}, respectively. The threshold voltage is simply up-scaled from the 1.5 kV_{DC} locomotive presented in [4] as

$$V_{\text{lim}} = V_{\text{n}} \frac{1.3\,\text{kV}}{1.5\,\text{kV}} = 7.8\,\text{kV}. \tag{15}$$

When a locomotive brakes, the excess of energy flows back towards an overhead line the locomotive is connected to. Unless the braking energy is recuperated either by a train in the vicinity or returned to the AC grid the railway network is connected to, the pantograph voltage increases. Fortunately, the MMC substations are bi-directional. Therefore, the excess of braking energy could be retrieved and injected back into the AC grid. Nonetheless, if there is no MMC or no other train at proximity to absorb the braking energy, the pantograph overvoltage must be prevented by means of a VLU, as presented in **Fig. 8**.

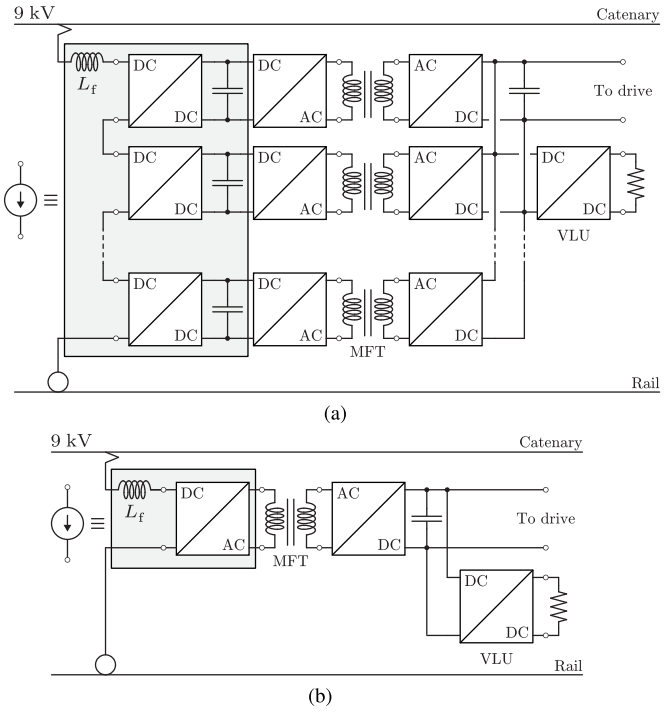


FIGURE 6. Two conversion concepts recognized in the MVDC domain; (a) Partial power processing; (b) Bulk power processing.

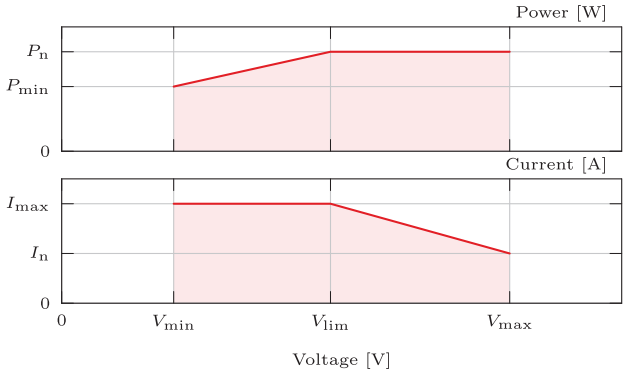


FIGURE 7. Power/Voltage and Current/Voltage safe operating areas of the train. In both cases, every point residing in the red transparent area can be safely reached, whereas the ones found above the red lines must be avoided.

As explained in the next section, train current depends on its power reference along with the available pantograph voltage. Let the train power reference be denoted by P^*. According to **Fig. 9**, the pantograph overvoltage can be avoided, during the braking phase, if the train power is corrected as

$$P_{\text{c}} = P^* + \frac{V - V_{\text{th,low}}}{V_{\text{th,up}} - V_{\text{th,low}}} P_{\text{n}}, \tag{16}$$

where threshold limits $V_{\text{th,low}}$ and $V_{\text{th,up}}$ were set as 10.6 kV and 10.7 kV respectively, while the nominal power of the train was denoted by P_{n}. Thereafter, the corrected power reference P_{c} gets compared with the train P/V characteristics from **Fig. 7** in order to obtain the reference which is subsequently converted in the train current. It must be emphasized that other voltage limiting strategies could have also been chosen, while the one provided **Fig. 9** represents only an example this work relies on.

B. SCHEDULER

According to [44], [45], a typical speed profile of a train is made of the following phases:

① Acceleration at maximum torque
② Cruising at constant speed
③ Coasting - the train slowly decelerates when approaching a railway station

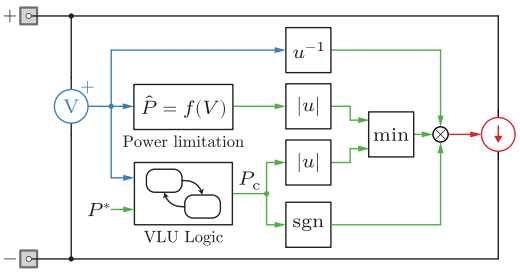


FIGURE 8. Real-time model of the train.

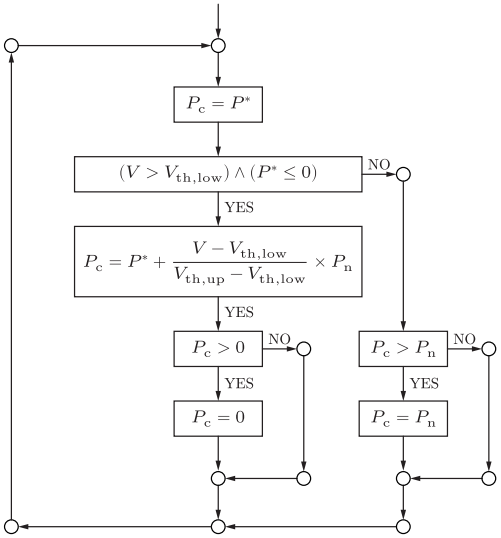


FIGURE 9. VLU logic adopted in this work.

④ Braking at maximum torque
⑤ Wait time at the station.

The upper plot in **Fig. 10** depicts the speed profile of the locomotive. The corresponding power consumption of the train was then deduced from the tractive and braking effort characteristics presented in [45], and is illustrated in the lower plot of the same figure. Sectors were envisioned in a way allowing only one train to circulate per sector and per track at a given time. This limitation makes sense from a traffic perspective as trains must maintain a minimal distance between them to prevent collision in case of an emergency braking. For this reason, a train cannot enter the next sector if the previous train has not left it yet. To respect this condition, two options are possible in terms of schedule:

- Trains wait at the end of their sector until they can pass to the next one
- All trains moving in the same direction have exactly the same speed at all times. If this is the case, they will all reach the end of their sector at the same time and they do not need to wait.

In a real-time simulation, the schedule can easily be handled by the use of Finite State Machines (FSMs), however, such a topic falls out of this paper's scope. Instead, it is worthy to note that speed and power profiles from **Fig. 10** are not convenient for an implementation in the FSM. Therefore, these are rather simplified (linearized) as presented in **Fig. 11**. From the system viewpoint, it does not truly matter what the speed profile is since it only affects the time needed for a train to pass through a sector. This, in turn, impacts how long the simulation lasts. However, the power profile is important from a load-flow perspective. When comparing the realistic and simplified power profiles, the later is less favorable because locomotives consume more power during the cruising and coasting phases. In fact, this is as if the trains were overloaded and needed to operate at full power to maintain their nominal speed. Additionally, the total braking

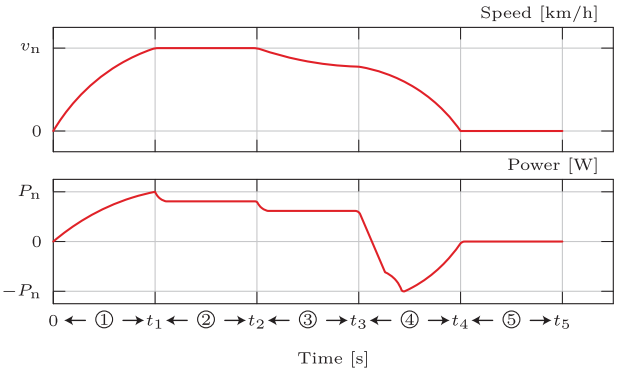


FIGURE 10. (a) Realistic speed profile of a train; (b) Corresponding power consumption.

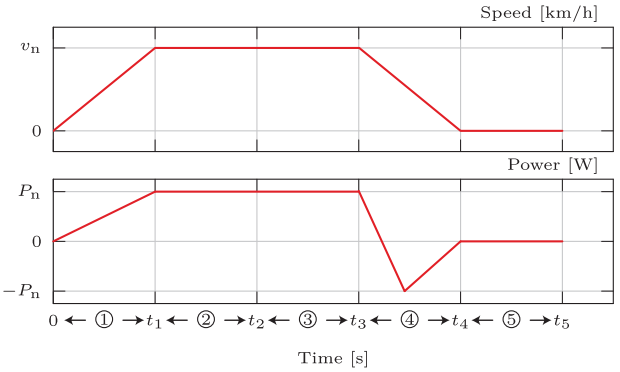


FIGURE 11. (a) Simplified (linearized) speed profile of a train; (b) Corresponding power consumption.

energy (area under the power curve during the braking phase) is also lower, which reduces the overall system efficiency. As such, the simplified model is more conservative.

V. MODELING OF SUBSTATIONS

A. TRGs

In a TRG, the DR performs AC-DC rectification, while the transformer modifies the AC voltage amplitude such that the DR open-circuit voltage, denoted by V_{R0}, matches the requirement from the EN 50163 standard. **Fig. 12a** depicts a 6-pulse DR connected to an AC grid by means of phase inductors labeled with L_g. It is noteworthy that identical schematics is to be used in case the DR is connected to the grid by means of a transformer. In this case, L_g denotes leakage inductance of the transformer.

Anyhow, commutation of the DR output current among phase inductors causes the average output voltage drop [46], which can be observed from (17).

$$V_R = \underbrace{\frac{3\sqrt{2}}{\pi} V_g}_{V_{R0}} - \underbrace{\frac{3}{\pi} \omega L_g}_{R_\sigma} I_R, \tag{17}$$

In the above expression, V_g represents the RMS value of the AC grid line-to-line voltage, whereas it was assumed that the DR output current is purely DC. However, something like that is not unrealistic, especially if all the trains can control the current drawn from their pantographs. What can be seen

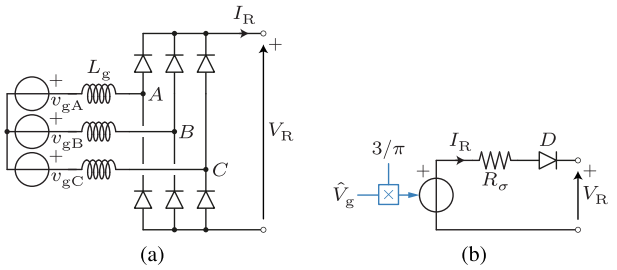


FIGURE 12. (a) 6-pulse DR connected to an AC grid by means of phase inductances labeled with L_g; (b) Averaged model of the DR.

from (17) is that the commutation voltage drop can actually be modeled with a resistor, labeled with R_σ, which allows one to derive the averaged TRG model depicted in **Fig. 12b**. The diode D preserves the unidirectional nature of the circuit.

The advantage of the proposed model lies in the reduction in the number of switching components used to model a TRG. Namely, in a circuit with M TRGs, the number of state-space matrices that an employed real-time simulator must handle equals $2^{(6\times M)}$ in case the model from **Fig. 12a** is used. If, however, the model from **Fig. 12b** is employed, the above mentioned number equals 2^M, which contributes to a significant reduction in the model computational requirements, and thus, the step-size used to run the simulation in real-time.

It must be stressed that 12-, 18- or even 24-pulse rectifiers are sometimes considered preferable in MV applications [47]. Notwithstanding, the proposed modeling approach does not change. Conversely, the expression (17) can be generalized as

$$V_R = k_1 \times \frac{3\sqrt{2}}{\pi} V_g - k_2 \times \frac{3}{\pi}\omega L_g I_R, \tag{18}$$

while values of coefficients k_1 and k_2 change depending on whether a group of DRs is connected in series or in parallel, as presented in **Tab. 5**. What can be seen from (18) and **Tab. 5** is that the nature of rectification system does not alter the structure of the model depicted in **Fig. 12b**. On the contrary, it only affects its multiplication constants, meaning that a single TRG model can be used for all the systems listed in **Tab. 5**.

B. MMCs

Fig. 13a present equivalent circuit of an MMC seen from its DC terminals [48]. In the case considered here, it is assumed that currents of the railway network are controlled by the trains. Therefore, as long as the MMC DC current is controlled by an external entity, the voltage component labeled with V_{DC} in **Fig. 13a** can be adjusted such that the voltage seen between the converter DC terminals corresponds to its reference value V^*_{MMC}. Consequently, in case the MMC is modeled in the same real-time simulator as the rest of the railway network, it can be approximated with a controlled voltage source, as illustrated in **Fig. 13b**.

In this work, however, real-time models of two MMCs are running on separate HIL units described in [15], [16] and

TABLE 5. Values of coefficients used to generalize (17).

	The number of pulses						
	6	12		18		24	
		series	parallel	series	parallel	series	parallel
k_1	1	2	1	3	1	4	1
k_2	1	2	$\frac{1}{2}$	3	$\frac{1}{3}$	4	$\frac{1}{4}$

referred to as MMC HIL 1 and 2. The model of the railway network discussed above runs on an independent HIL unit referred to as the Railway HIL. On these terms, the voltage across an MMC DC terminal should be measured and delivered to the Railway HIL, while current measurements from the Railway HIL should be sent back to the associated MMC HILs, as illustrated in **Fig. 14**. In other words, the model of the whole railway system is distributed (split) among several simulators.

When two parts of the model, created through the splitting procedure, must exchange the information on voltage, splitting the circuit at a place containing a capacitor is considered to be a good practice [17]. However, rather than having a concentrated DC link the MMC relies on the use of distributed DC links, making the voltage information exchange rather non-trivial. Nonetheless, the MMC real-time model can be extended by a small decoupling capacitor, labeled with C_d in **Fig. 14**, which circumvents the aforementioned challenge. As long as the capacitance C_d is selected sufficiently low, it does not alter the functionality of the circuit it is included in. In this work, the value $C_d = 50\,\mu$F was adopted.

VI. MODEL VERIFICATION

A. HIL PLATFORM DESCRIPTION

Fig. 15 presents the HIL system used for verification of results presented throughout this paper.

Real-time models of two MMCs run on two independent HIL units, a detailed description of which can be found in [15], [16]. In short, the employed MMC HILs rely on the use of the RT Box 1 from Plexim. Six RT Boxes are used for simulation of six MMC branches, each containing up to $N = 8$ cells. A seventh RT Box contains the model of an AC grid the MMC is connected to, along with an application the MMC is serving. On the back, an ABB PEC800 industrial controller was installed [15], [16]. In this way, the controller governing the real MMC prototype, described in [14], [49], [50], is used in this work, which adds a whole new level of reliability when compared with pure offline simulations.

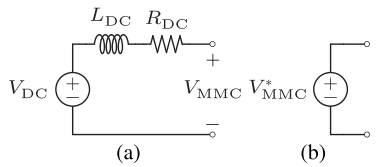


FIGURE 13. (a) Equivalent circuit of an MMC seen from its DC terminals; (b) Simplification of the circuit from (a) enabled by the fact that voltage component labeled with V_{DC} can be adjusted with high bandwidth.

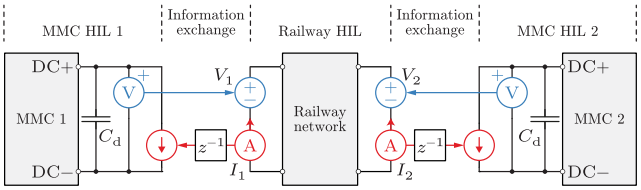


FIGURE 14. Distribution of the system model in case MMC real-time simulations take place in two independent HIL units.

Model of the railway network discussed above, contains eight sectors, meaning that sixteen trains circulate around it in accordance with the order provided by the block named Scheduler. As shown in **Fig. 15**, the model of the relevant railway network resides in the RT Box 3, which exchanges the information with two MMCs by means of two SFP links. In total, fifteen independent small-scale real-time simulators (2×7 RT Box 1 for two MMC HILs $+ 1 \times$ RT Box 3 for the Railway HIL) were connected together to emulate the behavior of an MVDC railway system. Scheduler controls the network traffic through the use of two FSMs, each controlling a group of trains moving in forward and reverse directions, respectively. By using the information on trains' speeds, and therefore positions, the Scheduler provides every sector with references for the overhead line and rail resistances/conductances. It is assumed that all the trains moving in the same direction have the same speed, however, such an organization of schedule does not affect the model generality.

Last but not least, the Railway HIL can send DC voltage references, labeled with V_1 and V_2 to both MMC HILs. In this way, the railway network power flow can be optimized with the aim of maximizing the system efficiency. However, this subject falls out of this paper's scope, meaning that both MMCs references were fixed at $V_1^* = V_2^* = 10.5\,\text{kV}$. Such a choice was made in accordance with **Tab. 4**, where TRG substations open-circuit voltage is defined as $V_{oc} = 10.5\,\text{kV}$. Parameters of simulated MMC and TRG substations can be found in **Tabs. 6** and **7**, respectively.

B. RESULTS

Fig. 16a contains results obtained by means of the previously described platform in case trains moving in both directions leave their platforms at the same time. In other words, no delay in schedules between two directions exists.

Instead of showing the waveforms for all sixteen trains, for clarity reasons, **Fig. 16a** includes the positions, pantograph voltages and powers of two trains moving in opposite directions and numbered with 4 and 12. It can be noticed that the pantograph voltages of both trains remain within the boundaries defined in **Tab. 4**, which confirms the validity of the design adopted for this study.

However, checking the accuracy of the presented modeling approach requires a comparison with offline simulations, given the unlikelihood of realizing the whole railway system in laboratory conditions. Thus, **Fig. 16b** provides relative errors in pantograph voltages, locomotive powers, substation

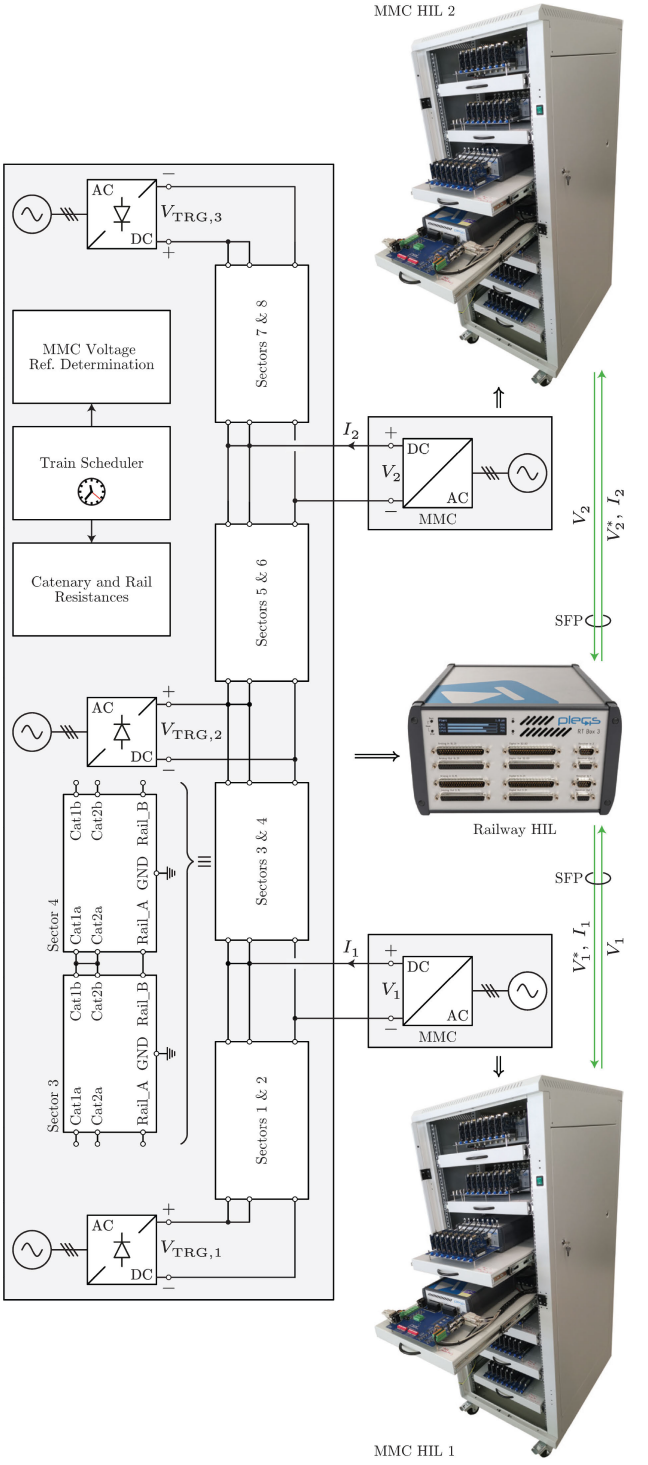
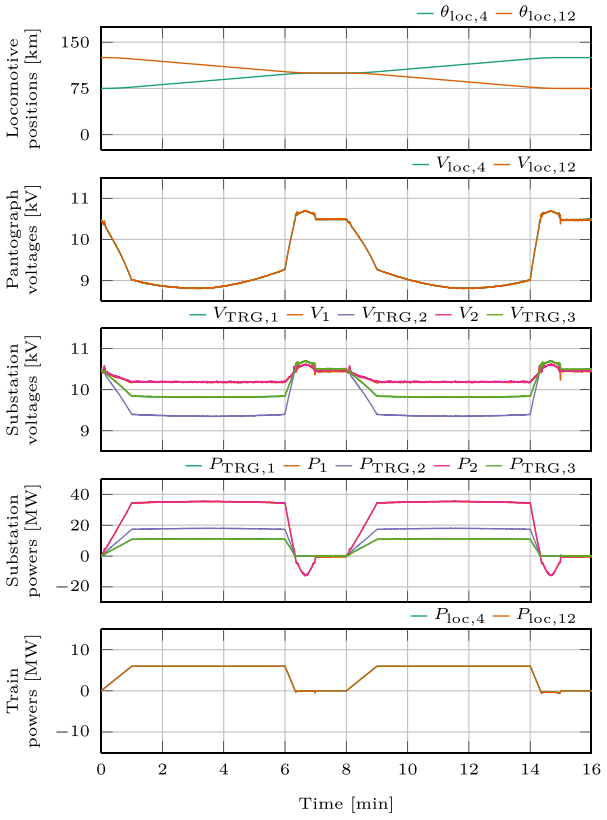
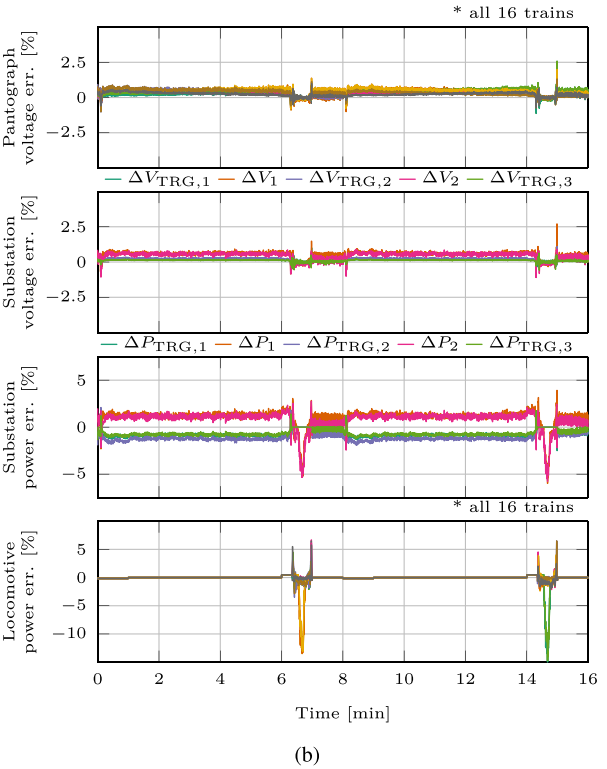


FIGURE 15. System used for verification of the approach presented in this work.

voltages and substation powers. In case voltage errors are observed, a normalization was performed with the substation open circuit voltage equal to $V_{oc} = 10.5\,\text{kV}$, while MMC and TRG power normalizations were performed with values of 40 MW and 30 MW, respectively. In the offline model, MMC substations were modeled as ideal voltage sources connected in series with a resistance equal to $R_{DC} = \frac{2}{3}R_{br} = 80\,\text{m}\Omega$.

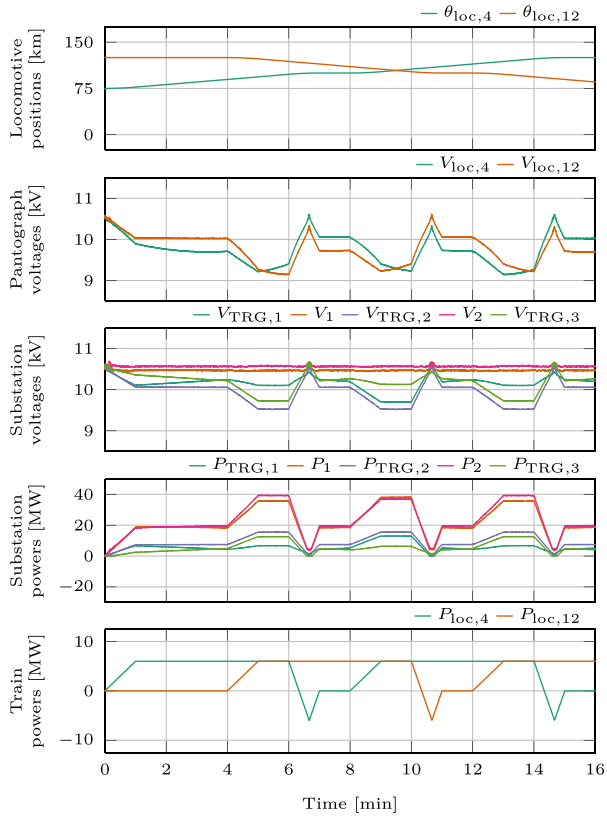


(a)

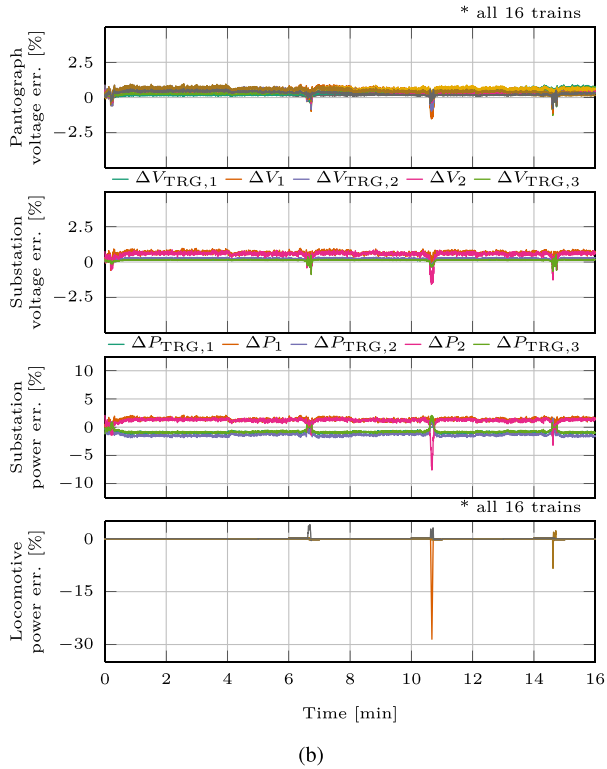


(b)

FIGURE 16. (a) Relevant system waveforms recorded in real-time. Trains moving in the reverse direction were not delayed with respect to ones moving in the forward direction; (b) Comparison between offline simulations and waveforms presented in (a).



(a)



(b)

FIGURE 17. (a) Relevant system waveforms recorded in real-time. Trains moving in the reverse direction were delayed with respect to ones moving in the forward direction by $T_d = 4$ min; (b) Comparison between offline simulations and waveforms presented in (a).

TABLE 6. Parameters of the MMC substations.

Rated DC voltage (V^*_{DC})	Rated power ($P_{\mathrm{n,MMC}}$)	No. of cells per branch (N)	Branch resistance (R_{br})	Branch inductance (L_{br})	Switching frequency (f_{sw})
11 kV	40 MW	8	120 mΩ	7.5 mH	1 kHz

TABLE 7. TRG substation parameters.

Rated DC voltage (V^*_{DC})	Rated power ($P_{\mathrm{n,TRG}}$)	Internal resistance (R_σ)
11 kV	30 MW	0.6Ω

Fig. 16b reveals an outstanding matching between the results obtained by means of real-time and offline simulations during periods excluding trains' braking. Around time instants equal to 6 min and 14 min, a slight mismatch between the two types of simulation can be observed and such an error can be attributed to the following reason. Namely, in the chosen railway network, node voltages are affected by the dynamics at which the MMCs can control their DC terminal voltages.

As already stated, in offline simulations, the adopted MMC model matches the one illustrated in **Fig. 13b**, with the reference being fixed to 10.5 kV. However, MMC HILs rely on detailed, switched, MMC models [16] governed by industrial controllers, which makes the MMC DC side dynamics slightly different compared to a stiff voltage source. As a results, a negligible error ($<$ 2.5% at all times) can be observed in substations' voltages.

Although of minor importance at first glance, even a 0.5 % voltage error causes the VLUs activation at different time instants. Consequently, powers demanded by the locomotives differ, resulting in the error displayed above. Notwithstanding, once the braking phase is over, the difference between the results from real-time and offline simulations nearly vanishes. It must be emphasized, however, that real-time simulations were performed with the MMC HILs using real industrial controllers, therefore, they are considered to be more realistic compared with the offline model considering the MMCs to be stiff voltage sources.

Figs. **17a** and **17b** contain similar analysis, however, with a delay of $T_{\mathrm{d}} = 4$ min introduced between schedules of trains moving in the opposite directions. As a result, two trains moving through the same sector do not brake at the same time, meaning that braking energy of one train can be used by its counterpart moving in the opposite direction. Conclusions identical to the ones related to **Figs. 16a** and **16b** can be made here - except during braking phases, results obtained from two models match to a very high extent. However, errors occurring during the above mentioned braking can be alleviated in case a more-detailed MMC offline simulation model is used for comparison purpose, which falls out of this work's interest.

VII. CONCLUSION

This paper provides an in-detail view of steps taken in modeling of all the parts belonging to an MVDC railway system of the future. Given that mechanical system dynamics can be neglected compared to the speed of real-time simulators, a set of simplifications was introduced allowing one to construct an efficient and fast simulation model, which is found extremely convenient in case system load-flow studies are to be carried out. In this way, the potential of replacing some of traditionally employed TRGs with MMCs can be examined, however, this subject can be considered a continuation of the work presented above. What is more, the presented modeling approach transforms a time-varying railway network into a time-invariant topology, which enables real-time simulations on simulators incapable of handling time-varying circuits. By introducing the concept of sector, which can be perceived as a main building block of the analyzed network, synthesis of an arbitrary size railway grid can be performed in an effortless manner. Model verification was performed on a large scale HIL system comprising fifteen small-scale real-time simulators, making the results presented above reliable and valuable from the system modeling standpoint.

REFERENCES

[1] *Transport in the European Union—Current Trends and Issues*, Directorate-General for Mobility and Transport of the European Commission, Brussels, Belgium, Apr. 2018.
[2] *Sector Overview and Competitiveness Survey of the Railway Supply Industry*, Ecorys, Rotterdam, The Netherlands, May 2012.
[3] A. Verdicchio, P. Ladoux, H. Caron, and C. Courtois, "New medium-voltage DC railway electrification system," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 2, pp. 591–604, Jun. 2018.
[4] A. Verdicchio, P. Ladoux, H. Caron, and S. Sanchez, "Future DC railway electrification system-go for 9 kV," in *Proc. IEEE Int. Conf. Electr. Syst. Aircr., Railway, Ship Propuls. Road Vehicles Int. Transp. Electrific. Conf.*, Nov. 2018, pp. 1–5.
[5] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech. Conf.*, vol. 3, Jun. 2003, p. 6.
[6] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Application, Design*. Hoboken, NJ, USA: Wiley, 2003.
[7] A. Christe and D. Dujic, "Modular multilevel converter control methods performance benchmark for medium voltage applications," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4967–4980, May 2019.
[8] B. Destraz, "Assistance énergétique base de supercondensateurs pour véhicules propulsion électrique et hybride," M.S. thesis, Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, Switzerland, May 2008. [Online]. Available: https://infoscience.epfl.ch/record/118661?ln=en
[9] *Enviline ESS—Energy Storage System*. Accessed: Mar. 19, 2021. [Online]. Available: https://new.abb.com/medium-voltage/switchgear/railway-switchgear/dc-traction-power-supply/energy-management/enviline-ess
[10] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. 13rd Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.
[11] L. Harnefors, A. Antonopoulos, S. Norrga, L. Ängquist, and H.-P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2526–2537, Jul. 2013.
[12] M. Steurer, F. Bogdan, M. Bosworth, O. Faruque, J. Hauer, K. Schoder, M. Sloderbeck, D. Soto, K. Sun, M. Winkelnkemper, L. Schwager, and P. Blaszczyk, "Multifunctional megawatt scale medium voltage DC test bed based on modular multilevel converter (MMC) technology," in *Proc. Int. Conf. Electr. Syst. Aircr., Railway, Ship Propuls. Road Vehicles (ESARS)*, 2015, pp. 1–6.

[13] M. M. Steurer, K. Schoder, O. Faruque, D. Soto, M. Bosworth, M. Sloderbeck, F. Bogdan, J. Hauer, M. Winkelnkemper, L. Schwager, and P. Blaszczyk, "Multifunctional megawatt-scale medium voltage DC test bed based on modular multilevel converter technology," *IEEE Trans. Transport. Electrific.*, vol. 2, no. 4, pp. 597–606, Dec. 2016.

[14] M. Utvic, I. P. Lobos, and D. Dujic, "Low voltage modular multilevel converter submodule for medium voltage applications," in *Proc. Int. Exhib. Conf. for Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2019, pp. 1–8.

[15] S. Milovanovic, I. Polanco, M. Utvic, and D. Dujic, "Flexible and efficient MMC digital twin realized with small-scale real-time simulators," *IEEE Power Electron. Mag.*, vol. 8, no. 2, pp. 24–33, Jun. 2021.

[16] S. Milovanovic, M. Luo, and D. Dujic, "Virtual capacitor concept for effective real-time MMC simulations," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Manage.*, 2021, pp. 1–8.

[17] *RT Box User Manual*, Plexim GmbH, Zürich, Switzerland, Jan. 2021.

[18] S. Aatif, H. Hu, F. Rafiq, and Z. He, "Analysis of rail potential and stray current in MVDC railway electrification system," *Railway Eng. Sci.*, pp. 1–14, Jul. 2021.

[19] P. Simiyu and I. E. Davidson, "MVDC railway traction power systems: State-of-the art, opportunities, and challenges," *Energies*, vol. 14, no. 14, p. 4156, Jul. 2021.

[20] A. Gómez-Expósito, J. M. Mauricio, and J. M. Maza-Ortega, "VSC-based MVDC railway electrification system," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 422–431, Feb. 2014.

[21] *Flexible Medium Voltage DC Electric Railway Systems*. Accessed: Oct. 6, 2021. [Online]. Available: https://projects.shift2rail.org/s2r_ipX_n.aspx?p=MVDC-ERS

[22] P. Simiyu and I. E. Davidson, "Modeling and simulation of MVDC traction power system for high-speed rail transportation," in *Proc. IEEE PES/IAS PowerAfrica*, Dec. 2021, pp. 1–5.

[23] P. Arboleya, I. El-Sayed, B. Mohamed, and C. Mayet, "Modeling, simulation and analysis of on-board hybrid energy storage systems for railway applications," *Energies*, vol. 12, no. 11, p. 2199, Jun. 2019.

[24] X. Guo, X. You, and Y. Song, "Real-time digital simulation of high-power electrical traction system," in *Proc. 15th Int. Power Electron. Motion Control Conf. (EPE/PEMC)*, Sep. 2012, pp. 1–5.

[25] G. Bianchi, F. C. Dezza, R. Manigrasso, and F. Mapelli, "Real-time test bench for traction drives controllers," in *Proc. Conf. Rec. Ind. Appl. Conf.*, vol. 3, 2000, pp. 1896–1900.

[26] L. Kovudhikulrungsri, K. Yuki, T. Arai, and A. Hirahara, "Real time simulator for railway traction and auxiliary power unit control applications," in *Proc. Int. Power Electron. Conf.*, Jun. 2010, pp. 244–247.

[27] H. Zhang, L. M. Shi, Y. Li, and K. Wang, "Real time simulation of high power converter for traction system," in *Proc. 15th Int. Power Electron. Motion Control Conf. (EPE/PEMC)*, Sep. 2012, pp. 306–310.

[28] C. Liu, R. Ma, B. Hao, H. Luo, F. Gao, and F. Gechter, "FPGA based hardware in the loop test of railway traction system," in *Proc. IEEE Int. Conf. Ind. Electron. for Sustain. Energy Syst. (IESES)*, Jan. 2018, pp. 206–211.

[29] R. Zhang, F. Lin, Z. Yang, H. Cao, and Y. Liu, "Hardware–in–the–loop real–time simulation experiment platform for traction power supply system based on dSPACE-Xsim," in *Proc. Int. Power Electron. Conf.*, May 2018, pp. 1816–1821.

[30] A. L. Allegre, A. Bouscayrol, J. N. Verhille, P. Delarue, E. Chattot, and S. El-Fassi, "Reduced-scale-power hardware-in-the-loop simulation of an innovative subway," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1175–1185, Apr. 2010.

[31] C. Mayet, P. Delarue, A. Bouscayrol, and E. Chattot, "Hardware-in-the-loop simulation of traction power supply for power flows analysis of multitrain subway lines," *IEEE Trans. Veh. Technol.*, vol. 66, no. 7, pp. 5564–5571, Jul. 2017.

[32] T. Liang and V. Dinavahi, "Real-time device-level simulation of MMC-based MVDC traction power system on MPSoC," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 2, pp. 626–641, Apr. 2018.

[33] T. Liang, Q. Liu, and V. R. Dinavahi, "Real-time hardware-in-the-loop emulation of high-speed rail power system with sic-based energy conversion," *IEEE Access*, vol. 8, pp. 122348–122359, 2020.

[34] *Need for Speed—Real-Time Simulation for Power Electronics in Railway Applications and Beyond*. Accessed: Oct. 11, 2021. [Online]. Available: https://search.abb.com/library/Download.aspx?DocumentID=9AKK106103A4045&LanguageCode=en&DocumentPartId=&Action=Launch

[35] T. Liang, Z. Huang, and V. Dinavahi, "Adaptive real-time hybrid neural network-based device-level modeling for DC traction HIL application," *IEEE Access*, vol. 8, pp. 69543–69556, 2020.

[36] E. Joelianto, D. Chaerani, and A. Setiawan, "Hardware in the loop simulation of railway traffic re-scheduling by means of MILP algorithm," in *Proc. 2nd Int. Conf. Instrum. Control Autom.*, Nov. 2011, pp. 119–124.

[37] K. Higashikawa, S. Urasaki, M. Inoue, M. Tomita, and T. Kiss, "Hardware-in-the-Loop simulation of superconducting devices for DC electric railway systems based on a real-time digital simulator," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 4, pp. 1–4, Jun. 2016.

[38] *Electric High-speed Multiple Unit—SMILE*. Accessed: Apr. 6, 2021. [Online]. Available: https://www.stadlerrail.com/media/pdf/smile_sbbe.pdf

[39] *Railway Applications—Supply Voltages of Traction Systems*, Standard EN 50163, 2004.

[40] C. Stackler, F. Morel, P. Ladoux, and P. Dworakowski, "25 kV–50 Hz railway supply modelling for medium frequencies (0–5 kHz)," in *Proc. Int. Conf. Electr. Syst. for Aircr., Railway, Ship Propuls. Road Vehicles Int. Transp. Electrific. Conf. (ESARS-ITEC)*, Nov. 2016, pp. 1–6.

[41] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer—Medium voltage Prototype," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3257–3268, Jul. 2014.

[42] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.

[43] Y. Hachicha, D. Cypers, M. Takuefou, S. Belin, P. Ladoux, and N. Roux, "Use of a HIL railway traction simulator for low frequency network stability studies," in *Proc. IEEE Int. Conf. Electr. Syst. Aircr., Railway, Ship Propuls. Road Vehicles Int. Transp. Electrific. Conf. (ESARS-ITEC)*, Nov. 2018, pp. 1–5.

[44] X. Liu, J. Xun, B. Ning, T. Liu, and X. Xiao, "Moving horizon optimization of train speed profile based on sequential quadratic proGramming," in *Proc. Int. Conf. Intell. Rail Transp. (ICIRT)*, 2018, pp. 1–5.

[45] Z. Bin, Y. Shijun, Z. Lanfang, L. Daming, and C. Yalan, "Energy-efficient speed profile optimization for high-speed railway considering neutral sections," *IEEE Access*, vol. 9, pp. 25090–25100, 2021.

[46] I. Batarseh and A. Harb, *Power Electronics: Circuit Analysis Design*. Springer, 2018.

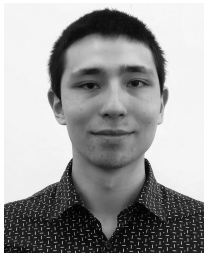
[47] A. Hernadi, Taufik, and M. Anwari, "Modeling and simulation of 6-pulse and 12-pulse rectifiers under balanced and unbalanced conditions with impacts to input current harmonics," in *Proc. 2nd Asia Int. Conf. Modeling Simulation (AMS)*, May 2008, pp. 1034–1038.

[48] S. Milovanovic and D. Dujic, "Comprehensive comparison of modular multilevel converter internal energy balancing methods," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8962–8977, Aug. 2021.

[49] E. Coulinge, A. Christe, and D. Dujic, "Electro-thermal design of a modular multilevel converter prototype," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2016, pp. 1–8.

[50] A. Christe, E. Coulinge, and D. Dujic, "Insulation coordination for a modular multilevel converter prototype," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Sep. 2016, pp. 1–9.

STEFAN MILOVANOVIĆ (Member, IEEE) received the B.Sc. and M.Sc. degrees from the School of Electrical Engineering, University of Belgrade, Serbia, in 2015 and 2016, respectively, and the Ph.D. degree from the École Polytechnique Fédérale de Lausanne, Switzerland, in 2020. From 2016 to 2017, he worked as a Research Assistant with the Department of Power Converters and Drive Systems, University of Belgrade. He is currently working as a Postdoctoral Researcher with the Power Electronics Laboratory, École Polytechnique Fédérale de Lausanne. His research interest includes medium/high voltage high power conversion.



SIMON STROBL received the B.Sc. and M.Sc. degrees in electrical and electronic engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 2018 and 2021, respectively. In August 2021, he joined Imperix Ltd., Sion, Switzerland, as a Development and Project Engineer. His main research interests include high performance variable speed drives and embedded programming for hard real-time applications.

PHILIPPE LADOUX (Member, IEEE) was born in 1963. He received the Engineering degree from the Institute of Engineering, ENSEEIHT, Toulouse, France, in 1987, and the Ph.D. degree in electrical engineering from the Institut National Polytechnique, Toulouse, in 1992. In 1994, he joined the Static Converters Research Group at the Laboratory of Plasma and Energy Conversion (LAPLACE), Toulouse, for which he was the Manager from 2001 to 2009. He is currently a Professor with the Institute of Engineering, ENSEEIHT, where he teaches power electronics. His research interest includes multilevel converters for high-power applications. The fields of application are railway electric traction as well as medium and high-voltage power systems. He has a strong experience of collaborative research with academic and industrial partners both at national and international levels. He is also involved in the steering committees of the international conferences SPEEDAM and ESARS and in the board of directors of PCIM Europe.

DRAŽEN DUJIĆ (Senior Member, IEEE) received the Dipl.-Ing. and M.Sc. degrees from the University of Novi Sad, Novi Sad, Serbia, in 2002 and 2005, respectively, and the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2008, all in electrical engineering. From 2002 to 2006, he was with the Department of Electrical Engineering, University of Novi Sad, as a Research Assistant. From 2006 to 2009, he was with Liverpool John Moores University, as a Research Associate. From 2009 to 2013, he was with the ABB Corporate Research Centre, Switzerland, as the Principal Scientist, working on the power electronics projects spanning the range from low-voltage/power SMPS in below kilowatt range to medium voltage high-power converters in a megawatt range. From 2010 to 2011, he was a member of a project team responsible for the development of the world's first power electronic traction transformer successfully commissioned on the locomotive. From 2013 to 2014, he was with ABB Medium Voltage Drives, Turgi, Switzerland, as a Research and Development Platform Manager, responsible for ABB's largest IGCT-based medium voltage drive ACS6000. He is currently with the École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, as an Associate Professor and the Director of the Power Electronics Laboratory. He has authored or coauthored more than 200 scientific publications and has led 18 patents. His current research interests include the areas of design and control of advanced high-power electronics systems for medium voltage applications. He has received the First Prize Paper Award from the Electric Machines Committee of the IEEE Industrial Electronics Society, in 2007. In 2014, he has received the Isao Takahashi Power Electronics Award for outstanding achievement in power electronics, and in 2018, the EPE Outstanding Service Award from the European Power Electronics and Drives Association. He is an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE TRANSACTIONS ON POWER ELECTRONICS, and the *IET Electric Power Applications*.