2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS) | 978-1-6654-3745-5/21/$31.00 ©2021 IEEE | DOI: 10.1109/EuroSOI-ULIS53016.2021.9560181

In-depth Cryogenic Characterization of 22 nm FDSOI Technology for Quantum Computation

Hung-Chi Han*, Farzan Jazaeri*, Antonio D'Amico*, Zhixing Zhao†,
Steffen Lehmann†, Claudia Kretzschmar†, Edoardo Charbon*, and Christian Enz*
*Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland
†GlobalFoundries, Germany
Email: hung.han@epfl.ch

***Abstract*—In this paper, the influence of temperature and back-gate bias is experimentally investigated on 22 nm FDSOI CMOS process. Cryogenic DC characterization was carried out under various back-gate voltages, V_{back}, from 2.95 K back to 300 K. An abrupt drop-off in drain current due to intersubband scattering is experienced in the transfer characteristic with a certain V_{back}. Moreover, resonant and source-to-drain tunneling transports are observed in devices with minimal channel length at cryogenic temperatures. The threshold voltage, V_T, and free carrier mobility, μ_{eff}, and their dependence on the back-gate voltage over a wide range of temperatures are extracted and discussed in detail. This work aims at investigating the impact of back gate potential on V_T and carrier transport at cryogenic temperatures, further paving the way towards up-scaling of quantum computers.**

***Index Terms*—FDSOI, Cryogenic CMOS, Quantum Computing**

I. Introduction

Silicon spin qubits have recently gained attention towards the up-scaling of quantum computers. They have remarkably proven their strength to achieve the so-called quantum integrated circuit by leveraging the well-established Complementary Metal-Oxide-Semiconductor (CMOS) technology [1, 2]. This is where the Fully-Depleted Silicon-On-Insulator (FDSOI) CMOS technology with electrostatically confined quantum dots holds the promise to reach the full monolithic integrated quantum processor [3]. Nevertheless, the lack of a cryogenic physics-based compact model of FDSOI is still a challenge to enable efficient circuit design at deep cryogenic temperatures. In light of recent efforts regarding the cryogenic DC characterization of a FDSOI technology [4]–[6]; the first study of such technology down to 4.3 K was reported in [4], further down to 20 mK in [5], and a design-oriented model was proposed in [6]. Moreover, [3, 7] revealed the carrier transport in an ultra-thin channel with respect to the intersubband scattering in a long device, and the resonant tunneling in a short channel, respectively. However, the effect of sweeping the back-gate voltage over a wide voltage range in short devices has not been reported yet. Additionally, the impact of the back-gate voltage on the free carrier transport at deep cryogenic temperatures is not well physically explained. Therefore, this paper aims at addressing the less-studied effects of the back-gate voltage on the DC performance for transistors of an up-to-date 22 nm FDSOI technology at deep cryogenic temperatures.

This work was supported in part by the EU H2020 RIA project SEQUENCE under Grant No. 871764.

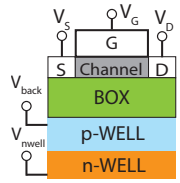

Fig. 1: The 2-D cross-section of 22 nm FDSOI technology.

Type	*W/L*
nMOS	wide / long
pMOS	wide / long
nMOS	wide / short
pMOS	wide / short

TABLE I: Measured devices (22 nm FDSOI process [8]).

II. Cryogenic DC Measurements

Table. I lists the measured devices with different types and geometries (nMOS/pMOS with long/short channels), fabricated on a 22 nm FDSOI process [8]. We assume the short channel effects are negligible in the long devices. On the contrary, short devices have the minimum length of such technology. Devices were probed on a LakeShore cryogenic probe station, CRX-4K, and characterized by the Keysight B1500A from ultra-low temperature, i.e., 2.95 K, back to room temperature, i.e., 300 K. The intermediate temperatures were taken at 20, 36, 77, 150, 210 K. A two-dimensional cross-section of a device is illustrated in Fig. 1. The p-WELL bias is represented by V_{back}. The p-WELL and n-WELL are reverse biased, and the device could operate either in forward back bias (FBB) or in reverse back bias (RBB). The FBB stands for the negative V_{back} for pMOS and positive V_{back} for nMOS, and vice versa for RBB. Hence, it allows a freedom to modulate V_T.

The transfer characteristics of devices in a linear mode, $|V_{DS}| = 10\,\text{mV}$, and $V_{back} = 0\,\text{V}$ are plotted in Fig. 2 over a wide range of temperatures. Nevertheless, the room-temperature data of long-channel nMOS (Fig. 2(a)) and short-channel pMOS (Fig. 2(d)) are missing due to electrostatic discharge during the abrupt warming up process. Nevertheless, Fig. 2 demonstrates the typical cryogenic behavior of CMOS technologies, i.e., subthreshold swing reduction, increasing V_T, and μ_{eff} enhancement, which provides a promising solution for low-power and high-performance modern electronics for quantum computations.

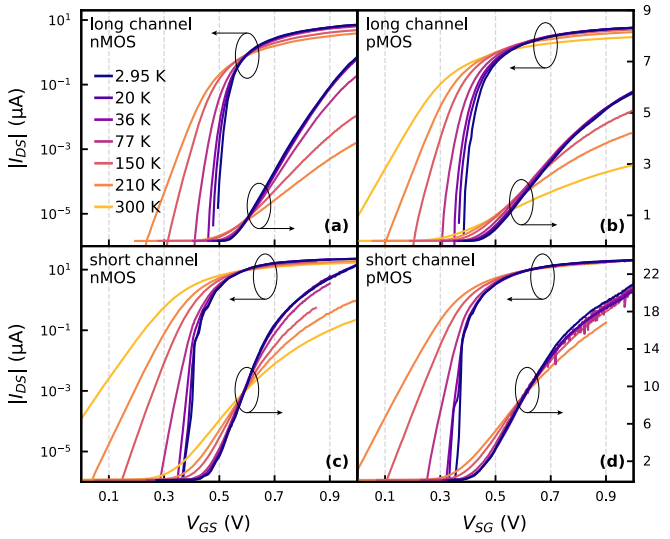

Fig. 2: Transfer characteristics of devices measured from 300 K and down to 2.95 K with $|V_{DS}| = 10\,\text{mV}$ and $V_{back} = 0\,\text{V}$, (a,b) correspond to the long-channel nMOS and pMOS, (c,d) are with respect to short-channel nMOS and pMOS.

The output characteristics in strong inversion ($|V_{GS}| = 0.9\,\text{V}$ for long devices and $|V_{GS}| = 0.7\,\text{V}$ for short devices) and $V_{back} = 0\,\text{V}$ are plotted in Fig. 3 over a wide range of temperatures. No kink effect is observed in this voltage range. The μ_{eff} was extracted from the linear and strong inversion regimes using g_{DS} function proposed by Jazaeri et al. [6, 9, 10]. This approach relies on the drift-diffusion transport model without any pre-assumption on the gate-voltage-dependent mobility. The results are detailed in Sec. IV.

III. Result and Discussion

A. Intersubband scattering

As demonstrated in Fig. 4(a,b), I_D-V_G of long-channel devices at 2.95 K is modulated by V_{back}, which ranges from -4 to 4 V with an interval of 2 V. The V_T is increased by RBB and decreased by FBB. It is worth noting that a sudden drop-off in drain current is experienced for long-channel nMOS with $V_{back} = 4\,\text{V}$ at around 400 mV above V_T, which is 0.22 V (see Fig. 4(a)), leading to a negative $\delta I_{DS}/\delta V_{GS}$. The phenomenon is attributed to the intersubband scattering for two-dimensional charge gas density [7], where the scattering rate follows such step-like density of states [11]. Hence, the drop of the current is due to the onset of the higher-order subbands. The relaxation time [11],

$$\frac{1}{\tau} = \sum_{p'} S(p,p') \left[1 - f(p')\right] \approx \sum_{p'} S(p,p'), \qquad (1)$$

is introduced to further explain why the intersubband scattering appears for this device at cryogenic temperatures and for some values of the back-gate voltage. The term of S in Eq. (1) is the scattering rate from the initial momentum p to the final momentum p' (Note that $f(p')$ is the occupancy rate of state at p' described by the Fermi-Dirac distribution, which is often equal to zero due to cryogenic temperatures). The scattering rate could be elaborated by *Fermi's Golden Rule*, the relaxation time, only considering the intersubband scattering between the first two subbands at cryogenic temperatures, is expressed by [11]

$$\frac{1}{\tau} = \sum_{p'} \frac{2\pi}{\hbar} |H_{p',p}|^2 \delta(E_2(p') - E_1(p) - \Delta E) \qquad (2)$$

with reduced Plank constant $\hbar$, matrix element $|H_{p',p}|$, and δ-function for energy conservation, in which, E_1 and E_2 stand for the eigenenergy of 1st and 2nd subbands, respectively, and ΔE is the energy change due to the scattering event. When $k_B T$ (Boltzmann constant k_B and temperature T) is large enough to cross numerous subbands, the abrupt drop-off in free carrier mobility is smoothed out. Additionally, subbands are split out in the strong vertical field due to potential confinement, where the δ-function in Eq. (2) is difficult to be satisfied at cryogenic temperatures because larger ΔE is required. Thus, the significant impact of intersubband scattering is only experienced for FBB at cryogenic temperature, but not for RBB conditions. Whereas, intersubband scattering is not experienced for pMOS device in the measured range since the smaller effective mass for holes leads to a wider gap between subbands. Moreover, intersubband scattering experienced in pMOS devices has not been reported yet. To observe the intersubband scattering for pMOS devices, a stronger FBB should be required.

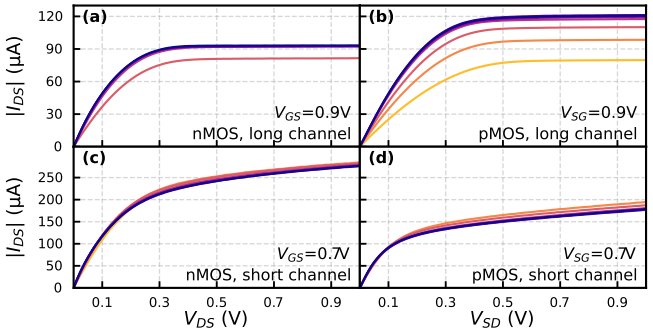

Fig. 3: Output characteristics of devices measured from 2.95 K back to 300 K with $V_{back} = 0\,\text{V}$ (the legend follows the one in Fig. 2).

B. Free Carrier Tunneling Transports

Fig. 4(c-f) emphasize the V_{back}-dependence of the measured subthreshold I_D-V_G at 2.95 K in linear and saturation regimes. The long-channel devices show the consistency in subthreshold regime between low and high horizontal fields (see Fig. 4(c,d)). However, the oscillatory drain current is pronounced for short-channel devices, especially in linear operation mode (see dashed lines in Fig. 4(e,f)). This is due to the resonant tunneling current, where free carriers tunnel the barrier via discrete energy levels of ionized quantum dots, and current flows in parallel to the drift-diffusion component (or even

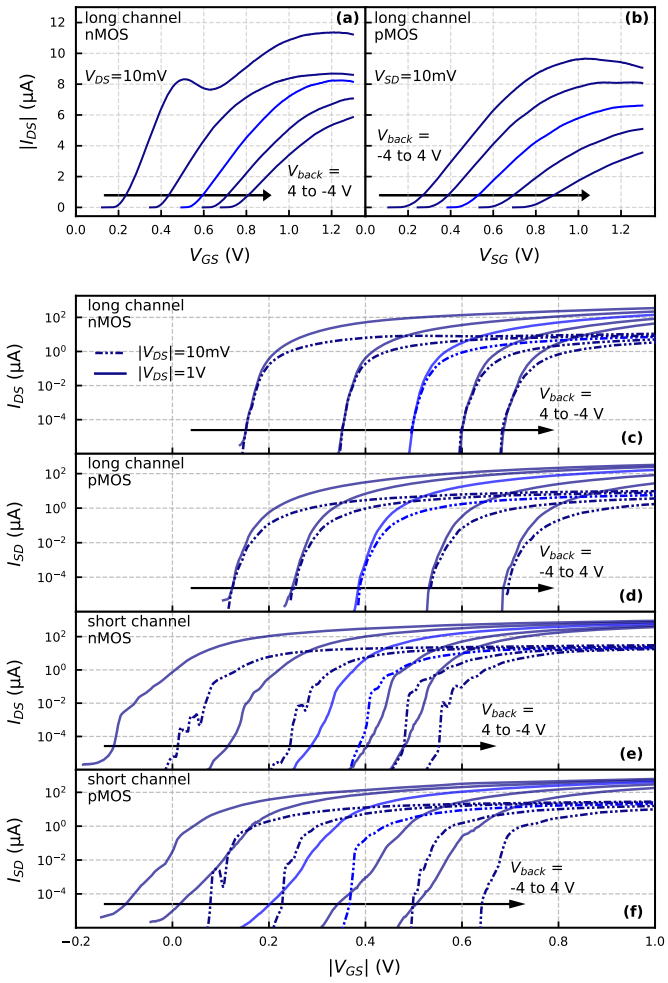

Fig. 4: Transfer characteristics of long/short nMOS/pMOS with V_{back} sweeping from -4 to 4 V at 2.95 K. The I_D-V_G curves with $V_{back} = 0$ V are highlighted by lighter blue. (a, b) I_D-V_G in linear scale for long-channel nMOS and pMOS devices, (c-f) logarithmic-scale I_D-V_G measured with $|V_{DS}| = 10$ mV (broken lines) and 1 V (solid lines) for long/short nMOS/pMOS, respectively.

the ballistic transport) [12]. Moreover, the resonant tunneling manifests differently with respect to V_{back}. It implies that the eigenvalue of a quantum dot is influenced by V_{back} as well. As evidenced by the solid lines in Fig. 4(e,f), the oscillatory behavior in I_D-V_G becomes less dominant in the saturation regime, which is due to the drain-induced barrier lowering (DIBL) and source-to-drain tunneling. The prior allows more free carriers following the drift-diffusion transport, and the latter is an additional current component that degrades the subthreshold performance owning to the drain-induced barrier thinning [13].

C. Summary of Oscillatory Drain Current

Two free carrier transport mechanisms, i.e., intersubband scattering and resonant tunneling, have been discussed previously. Although they both manifest as an oscillatory drain current in the transfer characteristic, they are due to different

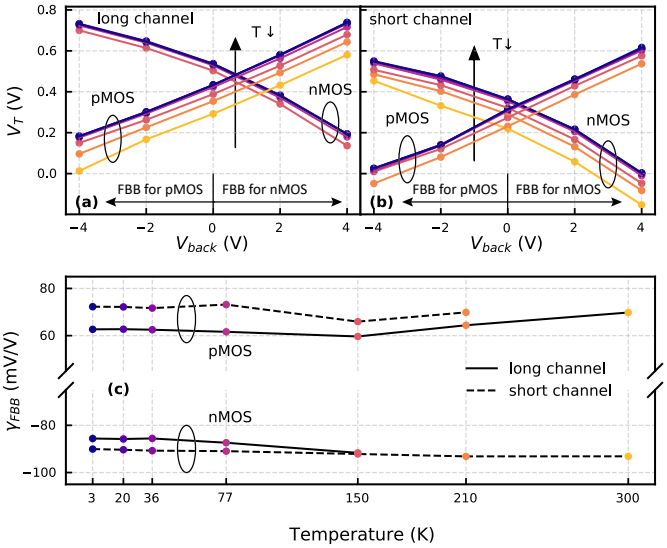

Fig. 5: (a,b) V_{back}-dependent threshold voltage at different temperatures, which is extracted from I_D-V_G with $|V_{DS}| = 1$ V (the legend of curves follows the one in Fig. 2), (c) back-body coefficient of FBB (γ_{FBB}) versus temperature.

	Intersubband scattering	Resonant tunneling
at cryogenic temperature	Yes	Yes
negative $\delta I_D/\delta V_G$	Yes	Yes
in subthreshold regime	No	Yes
above threshold	Yes	No
requires quantum confinement	Yes	No
experiences only in short channel	No	Yes

TABLE II: Summary of the properties of intersubband scattering and resonant tunneling, which experience in this study.

reasons. Hence, Table. II compares these two mechanisms in different conditions in terms of channel length, inversion status, device configuration, and etc.

IV. Back-gate Effects on V_T and μ_{eff}

The extracted V_T from I_D-V_G in saturation regime is plotted versus V_{back} in Fig. 5(a,b) for different temperatures. With the fixed V_{back} at 0 V, the increase in V_T at 2.95 K with respect to that at room temperature is around 150 mV for long-channel pMOS and short-channel nMOS, which is due to the shift of the quasi-Fermi level [14]. Although the comprehensive threshold voltage model for FDSOI technology, including the back-gate and low-temperature influence, has not been established yet, the consistency of the correlation between V_T and V_{back} at various temperatures implies that the front-to-back gate coupling does not lead to significant temperature dependence. Therefore, taking advantage of back-gate configuration, the increase in V_T could be compensated by FBB. Fig. 5(c) further elaborates the back-body coefficient for FBB, γ_{FBB}, with respect to different temperatures, describing how much V_T is modulated by 1 V of V_{back} while in FBB. The result suggests that room-temperature γ_{FBB} could sufficiently estimate the compensation for V_T at cryogenic temperatures.

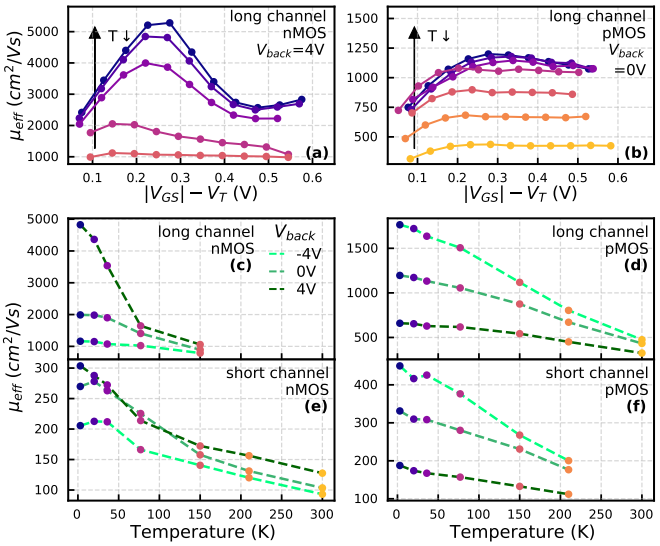

Fig. 6: Analysis of low field μ_{eff} with respect to various voltage conditions and temperatures, where μ_{eff} is extracted from I_D-V_D based on the method proposed in [9]. Low field μ_{eff} versus overdrive voltage at various temperatures for (a) long-channel nMOS at $V_{back} = 4\,\mathrm{V}$ and (b) long-channel pMOS at $V_{back} = 0\,\mathrm{V}$, (c-f) low field μ_{eff} as a function of temperature at $|V_{GS}| - V_T \approx 0.3\,\mathrm{V}$ with respect to various V_{back} (the legend of (a,b) follows to the one in Fig. 2).

The μ_{eff} is plotted in Fig. 6(a,b) versus the overdrive voltage, V_{ov}, for long-channel devices, where nMOS and pMOS are biased with $V_{back} = 4\,\mathrm{V}$ and $0\,\mathrm{V}$, respectively. At the same V_{ov}, it is clear that the μ_{eff} at cryogenic temperatures is enhanced in comparison to that at room temperature due to the reduced phonon scattering. The μ_{eff} trends in Fig. 6(b) show the universal mobility behavior [15]. For μ_{eff} at cryogenic temperatures, i.e., $T < 77\,\mathrm{K}$, decreases along the V_{ov} suggests that the surface roughness scattering has a relatively large impact on μ_{eff} due to less-dominant phonon scattering. Whereas, in Fig. 6(a), μ_{eff} at $T < 77\,\mathrm{K}$ dramatically drops off at $V_{ov} \approx 0.4\,\mathrm{V}$. It further verifies the substantial influence of intersubband scattering by I_D-V_D characterization, which has been already seen in Fig. 4(a).

Nevertheless, Fig. 6(c-f) demonstrate μ_{eff} as the function of temperature with respect to various V_{back}, while at $V_{ov} \approx 0.3\,\mathrm{V}$. The μ_{eff} overall shows the slight difference between each V_{back} at room temperature but diverges at cryogenic temperatures. It can be inferred from the vertical position of the mobile charge. In comparison to the back-gate inversion, i.e., strong FBB, mobility enhancement of the front-gate inversion is much limited by the remote Coulomb scattering from ionized charges in gate due to the ultra-thin gate dielectric [16]. Besides, it should be noted that mobility is enhanced less efficiently by the temperature and back gate in short-channel devices because of the neutral defects [17].

V. Conclusion

An experimental study is presented for a 22 nm FDSOI technology from 2.95 K back to 300 K for different device types and channel lengths. The transfer and output characteristics were accurately measured to investigate the influence of V_{back} on the DC performance in terms of I_D-V_G, V_T, and μ_{eff}. Quantum transports are pronounced in short-channel devices at cryogenic temperatures, i.e., resonant tunneling and source-to-drain tunneling. Additionally, the intersubband scattering significantly impacts the behavior of long-channel nMOS in strong FBB at cryogenic temperatures. The V_T versus a wide range of V_{back} is presented for various temperatures, which further suggests that the γ_{FBB} does not show the notable dependence on temperature. Furthermore, μ_{eff} with respect to temperature for different V_{back} is presented and reveals that μ_{eff} of front-gate inversion is enhanced less efficiently by temperature due to the remote Coulomb scattering.

References

[1] R. Maurand, X. Jehl *et al.*, "A CMOS silicon spin qubit," *Nat. Commun.*, vol. 7, no. 1, pp. 1–6, Nov. 2016.

[2] F. Jazaeri, A. Beckers *et al.*, "A review on quantum computing: From qubits to front-end electronics and cryogenic mosfet physics," in *2019 MIXDES - 26th International Conference "Mixed Design of Integrated Circuits and Systems"*, 2019, pp. 15–25.

[3] S. Bonen, U. Alakusu *et al.*, "Cryogenic characterization of 22-nm FDSOI CMOS technology for quantum computing ICs," *IEEE EDS*, vol. 40, no. 1, pp. 127–130, Jan. 2019.

[4] H. Bohuslavskyi, S. Barraud *et al.*, "28nm Fully-depleted SOI technology: Cryogenic control electronics for quantum computing," in *2017 Silicon Nanoelectronics Workshop (SNW)*, 2017, pp. 143–144.

[5] P. Galy, J. Camirand Lemyre *et al.*, "Cryogenic Temperature Characterization of a 28-nm FD-SOI Dedicated Structure for Advanced CMOS and Quantum Technologies Co-Integration," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 594–600, 2018.

[6] A. Beckers, F. Jazaeri *et al.*, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures," *Solid. State. Electron.*, vol. 159, no. 688539, pp. 106–115, 2019.

[7] M. Cassé, B. Cardoso Paz *et al.*, "Evidence of 2D intersubband scattering in thin film fully depleted silicon-on-insulator transistors operating at 4.2 K," *APL*, vol. 116, no. 24, 2020.

[8] R. Carter, J. Mazurier *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *IEDM*, Dec 2016, pp. 2.2.1–2.2.4.

[9] F. Jazaeri, A. Pezzotta, and C. Enz, "Free Carrier Mobility Extraction in FETs," *IEEE TED*, vol. 64, no. 12, pp. 5279–5283, Dec 2017.

[10] F. Jazaeri and J.-M. Sallese, *Modeling Nanowire and Double-Gate Junctionless Field-Effect Transistors*. Cambridge University Press, 2018.

[11] M. Lundstrom, *Fundamentals of Carrier Transport*. Cambridge University Press, 2010.

[12] R. Wacquez, M. Vinet *et al.*, "Single dopant impact on electrical characteristics of soi NMOSFETs with effective length down to 10nm," in *VLSIT*, Jun. 2010, pp. 193–194.

[13] J. Wang and M. Lundstrom, "Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?" in *IEDM*, Dec. 2002, pp. 707–710.

[14] A. Beckers, F. Jazaeri *et al.*, "Physical model of low-temperature to cryogenic threshold voltage in mosfets," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 780–788, 2020.

[15] S. Takagi, A. Toriumi *et al.*, "On the universality of inversion layer mobility in si mosfet's: Part i-effects of substrate impurity concentration," *IEEE Transactions on Electron Devices*, vol. 41, no. 12, pp. 2357–2362, 1994.

[16] J. Koga, T. Ishihara, and S. Takagi, "Effect of gate impurity concentration on inversion-layer mobility in mosfets with ultrathin gate oxide layer," *IEEE Electron Device Letters*, vol. 24, no. 5, pp. 354–356, 2003.

[17] M. Shin, M. Shi *et al.*, "Low temperature characterization of mobility in 14nm fd-soi cmos devices under interface coupling conditions," *Solid-State Electronics*, vol. 108, pp. 30–35, 2015, selected papers from the 15th Ultimate Integration on Silicon (ULIS) conference.