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Virtual Capacitor Concept for Computationally Efficient and Flexible Real-Time MMC Model

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ABSTRACT This paper demonstrates the splitting of the modular multilevel converter real-time simulation model into several independent parts through the use of the virtual capacitor concept. As a result, the number of state-space matrices the real-time solver needs to take into account gets significantly reduced, offering the possibility for substantial reduction of the simulation step size. Consequently, real-time simulation quality increases. The proposed concept was verified on a large-scale hardware-in-the-loop system comprising seven RT Boxes, where the model of the physical system is deployed, and ABB PEC800 industrial controller, where control algorithms of the real power hardware are deployed and executed.

INDEX TERMS Modular multilevel converter (MMC), circuit splitting, hardware-in-the-loop (HIL), virtual capacitor.

I. INTRODUCTION

Since a long time ago, Hardware-In-The-Loop (HIL) real-time simulations have been recognized as a reliable means for testing of control systems serving various purposes. General idea implies the connection of a tested controller to an HIL simulator through an appropriate interface. Thereafter, simulator inputs are read within a fixed time step and used subsequently to provide an output being as close as possible to the response observed in the real physical system. In other words, the controller being tested should never be able to differentiate between the simulator and the real power hardware. As a result, control system engineers can deploy and test new control algorithms in a risk-free environment, which is crucial if large and expensive systems are considered.

Power electronics systems, in a broader sense, rely on the use of switching devices found in one of two possible states: on or off. While various switch models (e.g. [1], [2]), adopted in the real-time simulation domain, can be considered, this work relies on the use of ideal switches. Therefore, in an electric network containing n switches, the number of distinct topologies (states) created through different combinations of devices being on/off equals 2^n. Furthermore, depending on the employed calculation approach, every valid configuration detected within the set of possible 2^n states can be associated with an appropriate state-space [3] or admittance matrix [4]. Due to frequent changes in the circuit states, guaranteeing high fidelity of the real-time simulation requires step sizes to fall within the boundaries of several microseconds or even hundreds of nanoseconds. To avoid time-consuming calculations of relevant system matrices (e.g. in the state-space [3]), these are normally pre-computed and stored in the simulator memory. On these terms, a set of pre-computed matrices, used in the upcoming simulation step, must be selected and loaded from memory, which is an inevitable time expense. However, the higher the number of switches, and simultaneously the matrices, the longer the time needed for the simulator to select the matrix being applied in the upcoming switching period. Thus, one can conclude that simulation speed and ability to address as many switching devices as possible represent two contradictory requirements. At first glance, modeling a structure with a high number of switching elements might seem irrelevant given that many basic topologies (e.g. [5]) can be represented with the same number of switches, irrespective of the operating voltage. Nevertheless, multilevel converters, widely used in medium and high voltage domain, comprise series connections of switching stages. On these terms, the number of switches employed within an observed topology increases with the operating voltage, leading to complex control structures. Consequently, the need for simulators, able

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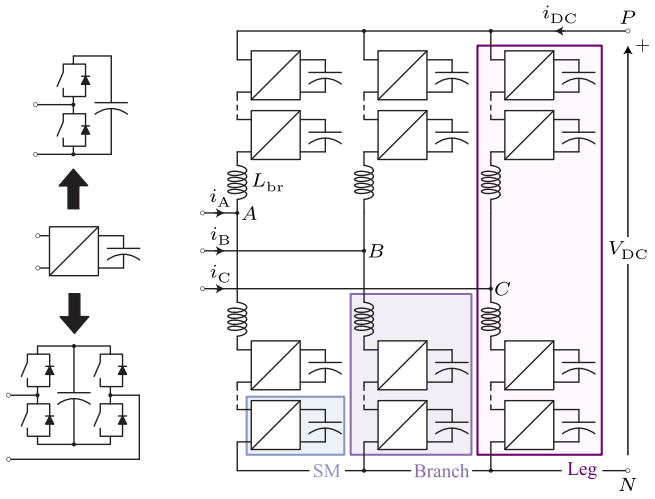


FIGURE 1. MMC along with the adopted naming convention.

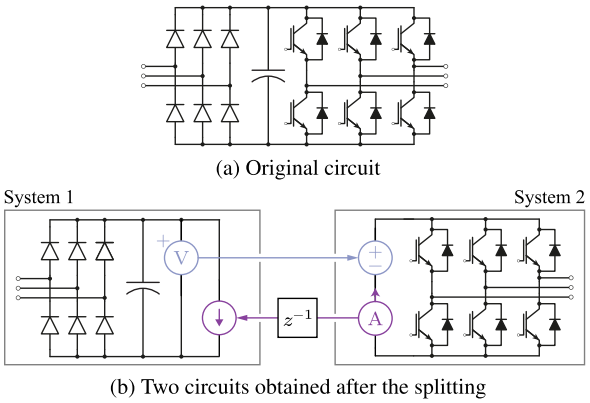


FIGURE 2. An example of possible circuit splitting.

to support real-time models of these converters, becomes evident.

MMC [6], depicted in **Fig. 1**, comprises a series connection of submodules (SMs), normally being in Half-Bridge (HB) or Full-Bridge (FB) configuration, while other choices have been listed in [7], [8]. According to **Fig. 1**, a series connection of an SM cluster and an inductor L_{br} is referred to as the branch, whereas two branches form the leg. By stacking SMs in series, theoretically unlimited voltage scalability is provided, while current capacity increase can be achieved in several ways [9], [10]. In spite of the advantages mentioned above, series connection of SMs comprises a high number of switching devices, making the MMC implementation challenging for any real-time simulator. Such a technological hurdle can be circumvented through an appropriate compression of the simulated circuit, meaning that sophisticated modeling approaches, putting the emphasis on minimization of the number of switching elements used in the model, need to be considered. Even if an appropriate modeling scheme is adopted, employed HIL simulator might not perform satisfactorily for various possible reasons:

- The number of physical inputs/outputs is insufficient, which is typical for small-scale HIL simulators (e.g. TyphonHIL, RT Box, SpeedGoat, StarSim) begin originally envisioned for systems not as massive as the MMC. It is noteworthy that large-scale simulators (e.g. RTDS, Opal RT, dSPACE) also exist, however, this paper focuses on the use of their small-scale counterparts.
- There are too many switching combinations resulting in an unacceptably large code used by the simulator.
- The computational effort happens to be too large requiring a reduction of the execution times.

In the first case, the MMC model must run on several simulators referred to as HIL units onward. To put it differently, splitting the model among different HIL units is required. In the last two cases, similar principle can be adopted, however, model separation takes place within a single HIL unit, as will be seen shortly. Namely, an artificial delay is included in the interaction between two or several parts of the circuit created through the splitting procedure. Consequently, separated parts of the circuit are treated independently, which reduces the number of state matrices describing the converter [11]. Moreover, different parts of the model are run on different hardware nodes, resulting in the step size reduction. **Fig. 2a** and **2b** illustrate such an example. To avoid forming of algebraic loops, one simulation step size delay must be introduced between newly formed circuit parts labeled with System 1 and 2, respectively. However, as long as the simulation step size is small enough, fidelity of the simulation should not be severely hindered.

Whenever a circuit splitting is required, performing so at a point containing capacitor or inductor can be considered a good practice, as explained in [11]. In contrast to the circuit depicted in **Fig. 2a**, the MMC does not contain a concentrated DC link where the circuit splitting can be performed. Conversely, the modular concept implies that DC links are distributed all over the converter, making the model separation rather non-trivial.

To eliminate this shortcoming, this paper proposes, presents and exploits the concept of virtual capacitor. By means of the proposed method, MMC real-time model can be decoupled into several independent parts, which leads to a significant reduction in the number of state matrices describing the converter - which can be considered the most important contribution of this work. As a result, with respect to the model chosen as a starting point, significant simulation step size reduction was achieved, while preserving all of its physical properties. Lastly, similar principle of the model splitting can be applied to any other MMC-based structure (e.g. Matrix MMC [12]), making it extremely versatile, flexible and extendable. In this work, seven RT Box 1 units were employed to run the real-time model of a 3.3kVac/5kVdc, 250kW MMC comprising 48 FB SMs in total. The proposed model was tested against the real industrial ABB PEC800 controller, where MMC control algorithm was deployed, making the presented results credible and valuable.

The rest of this paper is organized as follows. **Sec. II** contains a summary of the approaches used to model the MMC in real-time. Considering the pros and cons of the analyzed modeling approaches, the choice of the model being subject to splitting was justified. In **Sec. III**, the need for the MMC model splitting was thoroughly analyzed and followed by an in-detail explanation of the virtual capacitor concept. **Sec. IV** contains a step-by-step procedure for the virtual capacitor determination. Finally, **Sec. V** contains results obtained on the developed HIL simulator.

II. MMC REAL-TIME MODELING PERSPECTIVES

Conventional MMC modeling perspective assumes that an SM cluster can be replaced with a controlled voltage source [13], which was the reasoning followed in [14], [15]. While these, also referred to as the averaged, MMC models find their use if the steady state operation is considered, operating modes requiring the converter to be in the blocked state (i.e. charging or faulty operation) cannot be simulated in this way. Extension of the averaged MMC model, aiming to allow the blocked state emulation, was provided in [16]. However, the number of additional switches, required for the fulfillment of such a goal, was not considered acceptable from the real-time simulations aspect. In [17] the use of dynamic phasors was proposed, however, the behavior of individual SMs was not explicitly modeled, rendering this modeling approach unrealistic. A similar assumption was adopted in [18], [19], resulting in the need for different modeling schemes.

Modeling of a switch with an equivalent on-/off- resistance, combined with Dommel's capacitor model [20], allows for an SM cluster to be modeled with either Thevenin or Norton equivalent [4], [21]–[23]. Although convenient at first glance, such an approach prevents the blocked state to be modeled to the full extent. Moreover, modeling the switch being in the off state with a high value resistance might lead to stiff system matrices. Finally, changing the number of inserted SMs within a branch, makes the Thevenin or Norton equivalent circuit time-varying, which might not be supported by some real-time simulation platforms (e.g. RT Box [11]).

In [24], the MMC branch was modeled with the so-called surrogate network. Every SM is initially modeled with a parallel connection of capacitor, resistor and upward-directed diode, which prevents the SM capacitor from becoming negatively charged. Subsequently, an SM is associated with one group depending on whether it is inserted, blocked or bypassed. Similarly to the case mentioned above, an employed simulator needs to solve time-varying circuits.

Modeling of an MMC branch with a controlled voltage source and three switching elements, such as diodes, switches and transistors, was proposed on a few occasions [25]–[28]. Even though all of the operating modes can be emulated by such a combination, a solution, depicted in **Fig. 3**, ensuring the same performance with two diodes and two controlled voltage sources was proposed in [29]–[32]. In this way, a versatile model of the branch allowing for emulation of both

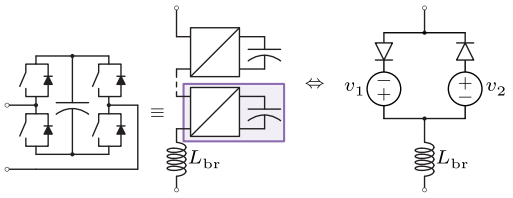


FIGURE 3. Branch model provided in [32] and adopted in the following discussions. Irrespective of the SM type (HB or FB), the branch model remains the same, which was found quite convenient from the HIL development standpoint.

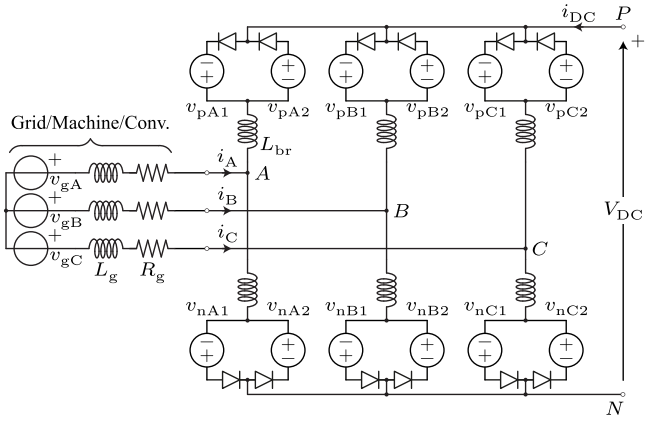


FIGURE 4. MMC model formed by means of methodology discussed in [32]. Subscripts "p" and "n" denote upper and lower quantities, respectively. At its AC terminals, the MMC gets interfaced with a three-phase voltage source through a series connection of an inductor and resistor (eventually). Thus, the same model can be used for real-time simulations of an MMC connected to an AC grid, AC machine or any other converter through the inductive interface (e.g. low-frequency transformer).

blocked and active states is obtained, providing one with the MMC model depicted in **Fig. 4**. As explained in [32], voltage sources v_1 and v_2 from **Fig. 3** represent a combination of SM switching signals and instantaneous values of SM capacitor voltages.

As suggested in the previous section, some HIL simulators have a limited number of digital/analog inputs/outputs. On these terms, simulation model needs to be split among different HIL units. In this work, RT Box 1 [11] is used and, due to the insufficiency in the number of digital inputs (which equals 32), voltages v_1 and v_2 are calculated in a separate HIL unit for every individual branch. Such a choice becomes clear based on the fact that the simulator used in this work hosts the model of the converter comprising 48 FB SMs in total. As the MMC contains six branches, it is straightforward to calculate that every branch receives $(48/6) \times 4 = 32$ switching signals. Therefore, the box running the model depicted in **Fig. 4** will be referred to as the Application RT Box, whereas calculations of relevant branch voltage components take place in six Branch RT Boxes, as presented in **Fig. 5**. The upcoming sections will provide more information on the HIL simulator used for verification of results presented herewith.

At this point, it must be emphasized that boxes presented in **Fig. 5** do not have to operate with identical time-steps, meaning that they are to a certain extent independent from

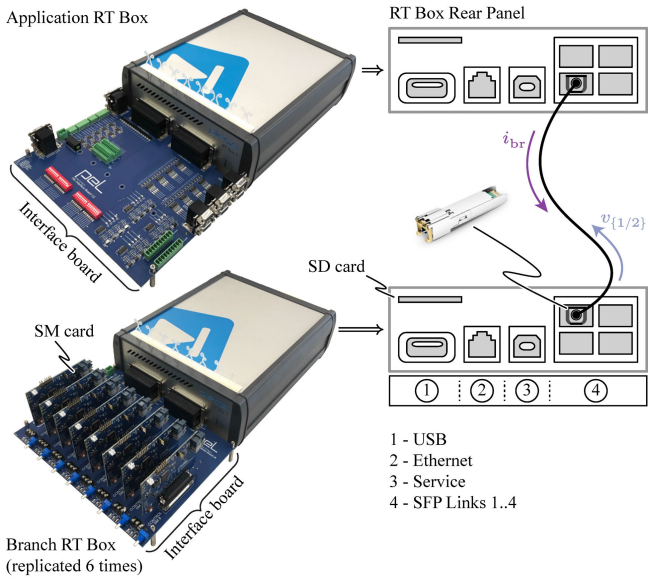


FIGURE 5. Two essential parts of the HIL simulator used to verify the results derived throughout the following sections. Branch RT Boxes provide the Application RT Box with voltage components labeled with v_1 and v_2 in the adopted branch model. On the other hand, information on a relevant branch current is sent back to the Branch RT Box, which is needed according to [32].

each other. The number of SMs, labeled with N_{SM}, simulated within a Branch RT Box determines its step size, whereas the model run in the Application RT Box remains the same irrespective of N_{SM}. In other words, in the Application RT Box, simulation step size does not depend on the number of SMs simulated on the other boxes, but rather on the structure of the MMC model itself.

Running the model depicted in **Fig. 4** on the Application RT Box requires the simulation step size $T_{\mathrm{step}} > 75\mu$s. It is noteworthy that this value was determined empirically as no means of guessing it analytically exist in case CPU-based simulators, such as the RT Box, are used. Notwithstanding, such a high value was considered unacceptable from the simulation fidelity standpoint. Consequently, further splitting of the circuit provided in **Fig. 4** must be investigated, as thoroughly explained in the next section.

III. SPLITTING THE MMC REAL-TIME MODEL

A. MOTIVATION FOR FURTHER SPLITTING

In case an arbitrary circuit is to be simulated, the solver running on the HIL simulator employed in this work creates state-space matrices prior to commencing any real-time calculations. Thereafter, depending on the state the simulated circuit is found in, different state-space matrices are used. However, the solver needs to recognize changes in the circuit configuration in order to update the state matrix being in use. In case switching devices with forced commutations (e.g. IGBT) are considered, whenever the switching signal is issued to any device, the solver gets an information about the necessary state-space matrix change. In circuits with natural commutation, alike the one in **Fig. 4**, the state-space matrix change occurs only when current through any switch crosses zero. To achieve high simulation fidelity, the solver must recognize these moments such that the state matrix can be updated. In offline simulations, where the use of variable step size is allowed, this identification does not represent a challenge since the solver is allowed to go back and forth around the critical interval and determine the exact time instant at which the state-matrix should be changed. In real-time simulations, the step size is fixed and the solver does not have time for multiple inspections of the circuit matrix change. In other words, the solver is not allowed to go backwards in time.

As the circuit size increases so does the number of state matrices, whose dimension depends on the number of reactive elements in the circuit. Moreover, if the circuit consists of diodes only, high computational resource is required to determine time instants at which previously mentioned state-space matrices should be updated [33]. In **Fig. 4**, the number of diodes employed to model the MMC equals twelve. This indicates that the number of state-space matrices the solver must take into account equals $N_{\mathrm{mat}} = 2^{12}$, slowing down the real-time simulation process. Nevertheless, an improvement can be found in a suitable model splitting. In case the circuit from **Fig. 4** is split in, for example, two independent parts, the number of possible states (combinations) decreases to $N_{\mathrm{mat}} = 2 \times 2^6$. Consequently, the simulation step size can be significantly reduced compared to the value indicated above.

To provide a better illustration of the circuit splitting benefits, **Fig. 6** illustrates this principle on an exemplary circuit found in an arbitrarily chosen state. Even though **Fig. 6a** presents only one state generated by a random combination of switches being on and off, the number of possibly created circuits equals 2^8. Splitting of the circuit from **Fig. 6a** can be performed as in **Fig. 6b**, where separation of state variables is obtained through the introduction of artificial system inputs (i.e. v_{s} and i_{s}), allowing the newly formed circuits, labeled with System 1 and System 2, to be described by a new set of state-space matrices. Since both systems depicted in **Fig. 6b** comprise four switching elements (from the circuit configuration viewpoint, IGBT/diode pair is considered a single element), the total number of circuits created through different switching combinations equals 2×2^4, which is an 8-fold decrease compared to the case where no splitting was performed. As the simulator must handle a significantly lower number of state-space matrices, the simulation step size reduction becomes self-explanatory.

In contrast to the exemplary case discussed above, the MMC does not comprise a concentrated DC link. This might seem as an inevitable obstacle in the circuit splitting procedure. However, addition of the so-called virtual components into the model from **Fig. 4** allows for such a shortcoming to be addressed, as demonstrated in the following section.

B. VIRTUAL CAPACITOR CONCEPT AND SPLITTING METHODOLOGY

The whole HIL concept implies the processing of virtual power and extending the system with additional

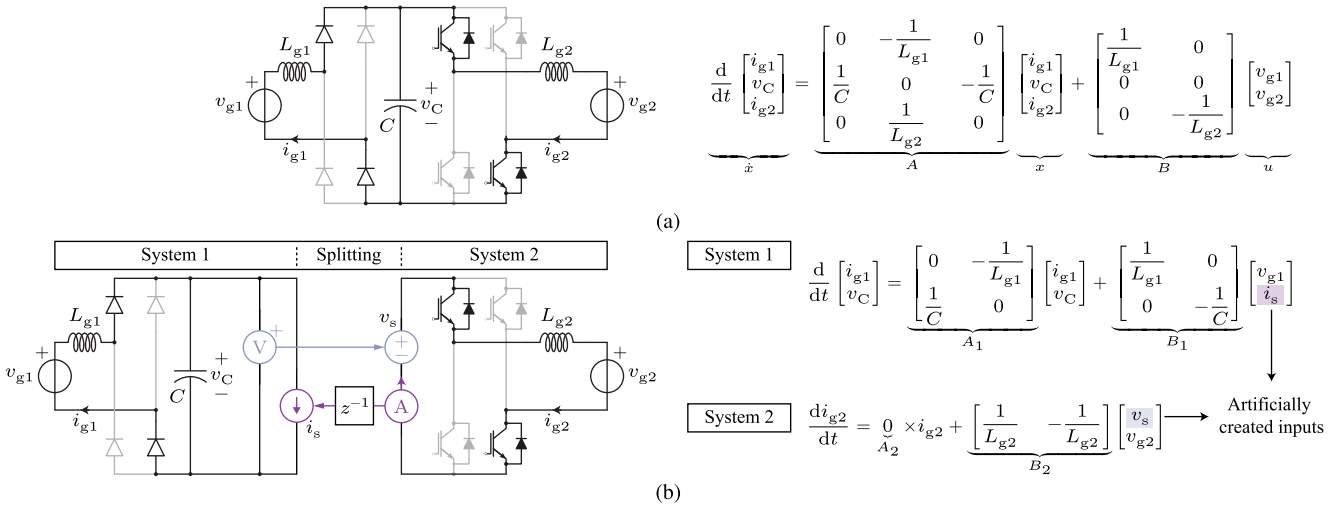


FIGURE 6. An exemplary circuit used to highlight the benefits of circuit splitting upon the reduction in the number of circuits possibly created through a different combination of switches being on and off.

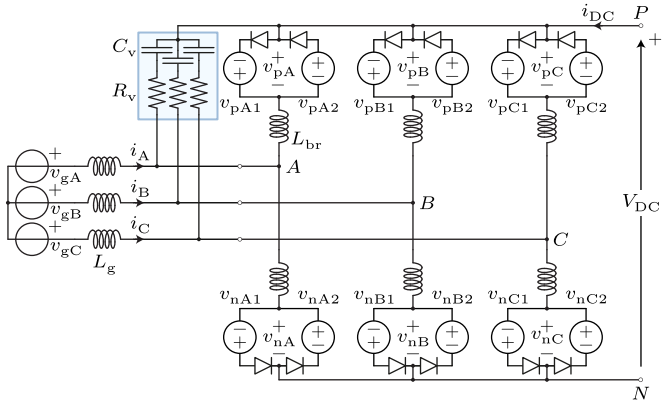


FIGURE 7. Extension of the original MMC by the so-called virtual network highlighted in blue. In this way, further model splitting is enabled.

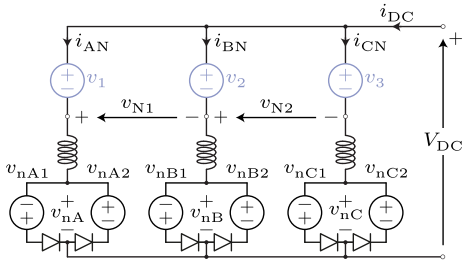


FIGURE 8. Separating the set of lower branches from the original MMC model.

component(s) is not prohibited as long as Kirchhoff voltage and current equations in a newly formed circuit correspond to the ones in the parent model. **Fig. 7** depicts the extension of the MMC model provided in **Fig. 4** by a set of three capacitors and three resistors denoted by C_v and R_v, respectively. As these elements do not exist in reality, while they are used only for real-time simulation purposes, they will be referred to as the Virtual Capacitors (VCs) and Virtual Resistors (VRs). VCs provide the means for circuit splitting, while the role of resistors VRs will be explained shortly.

Let one commence the analysis by observing the circuit from **Fig. 4**, while splitting the set of lower branches from the rest of the system can be set as a goal. Here, the following expression can be established

$$V_\mathrm{DC} = \frac{1}{3}(v_\mathrm{PA} + v_\mathrm{PB} + v_\mathrm{PC}) + \frac{1}{3}(v_\mathrm{NA} + v_\mathrm{NB} + v_\mathrm{NC}), \quad (1)$$

while the AC current of any phase leg $x \in \{A, B, C\}$ can be expressed as

$$i_x = i_{x\mathrm{N}} - i_{\mathrm{P}x}. \quad (2)$$

Addition of virtual elements into the circuit from **Fig. 4** does not violate (1), however, relation (2) holds only if virtual elements do not conduct any current. This condition cannot be fulfilled unless the impedance of virtual elements is infinitely large. Yet, one should always keep in mind the primary purpose of an HIL simulator - to test and verify converter control schemes. Normally, controllers ignore (filter out) high frequency components in converter currents, therefore, as long as parameters of the virtual network are set such that its fundamental frequency current (e.g. 50Hz) is negligible, the circuit from **Fig. 7** satisfies (2), at least in the frequency range being of interest for the tested controller.

Assuming that parameters of the virtual network are properly chosen allows one to separate the set of lower branches from the rest of the model given in **Fig. 7** as depicted in **Fig. 8**. However, the choice of voltage components v_1, v_2 and v_3 must be clarified. Basically, these three voltages must ensure the satisfaction of two criteria:

1) Voltages v_N1 and v_N2 from **Fig. 8** must correspond to line voltages v_AB and v_BC from **Fig. 7**,
2) What is seen from the DC terminal must be equivalent to the original circuit, meaning that (1) must be satisfied.

These two requirements ensure the preservation of Kirchhoff voltage laws, while the Kirchhoff current law regarding the DC link current is inherently preserved given that $i_{\mathrm{DC}} = i_{\mathrm{nA}} + i_{\mathrm{nB}} + i_{\mathrm{nC}}$. If

$$\begin{bmatrix} v_1 & v_2 & v_3 \end{bmatrix}^T = \begin{bmatrix} v_{\mathrm{PA}} & v_{\mathrm{PB}} & v_{\mathrm{PC}} \end{bmatrix}^T, \tag{3}$$

based on **Figs. 7** and **8**, one can derive the following expression for every phase leg $x \in \{A, B, C\}$

$$L_{\mathrm{br}} \frac{\mathrm{d}}{\mathrm{d}t} \underbrace{\frac{i_{\mathrm{P}x} + i_{x\mathrm{N}}}{2}}_{i_{cx}} = \frac{V_{\mathrm{DC}}}{2} - \frac{v_{\mathrm{p}x} + v_{\mathrm{n}x}}{2}. \tag{4}$$

In (4), the average of branch currents belonging to the leg labeled with x was denoted by i_{cx} and henceforward this component will be referred to as the leg common-mode current. What is more, expression (4) can also be derived from **Fig. 4**. Consequently, the circuit from **Fig. 8** truly represents the equivalent of an MMC seen from its DC terminals.

Once the set of lower branches is modeled, it can be separated from the upper branches set. As every branch represents a series connection of a voltage source and an inductor, lower branches can be replaced by controlled current sources, which are fed with the lower branch current measurements, as presented in **Fig. 9**. As currents of controlled sources i_{nA}, i_{nB} and i_{nC} do not sum up to zero, the star point at which these sources meet must be connected to the point labeled with P'. In this way, each one of the upper branches becomes parallel connected to the current source being fed with current of its lower counterpart. In other words, seen from the AC terminals, branches operate in parallel.

To prove that the demonstrated circuit splitting does not change the dynamics of the MMC AC currents, two important remarks must be made beforehand. Firstly, for a properly tuned virtual network, current component at the fundamental frequency can be neglected. Hence, the presence of the virtual network can be discarded from the following analysis. Secondly, the simulation step size is assumed to be small enough such that one step size delay can be approximated as $e^{-sT_{\mathrm{step}}} \approx 1$ in the relevant frequency range. On these terms, parallel connection of an upper branch and the current source representing its lower counterpart can be replaced with Thevenin's equivalent, as depicted in **Fig. 10**.

For an arbitrary phase leg $x \in \{A, B, C\}$, voltage of the source labeled with $v_{\mathrm{eq},x}$ can be calculated as

$$v_{\mathrm{eq},x} = v_{\mathrm{p}x} + L_{\mathrm{br}} \frac{\mathrm{d}}{\mathrm{d}t} \underbrace{i_{x\mathrm{N}}(t - T_{\mathrm{step}})}_{\approx i_{x\mathrm{N}}(t)}, \tag{5}$$

which, in combination with (2) and (4), yields

$$v_{\mathrm{eq},x} = \underbrace{-\frac{v_{\mathrm{n}x} - v_{\mathrm{p}x}}{2}}_{v_{\mathrm{s}x}} + \frac{L_{\mathrm{br}}}{2} \frac{\mathrm{d}i_x}{\mathrm{d}t} + \frac{V_{\mathrm{DC}}}{2}. \tag{6}$$

The above expression allows one to form the circuit from **Fig. 10b**. Thereafter, dynamics of the MMC AC currents can be described with (7) to (9), where $L_\Sigma = L_{\mathrm{g}} + L_{\mathrm{br}}/2$,

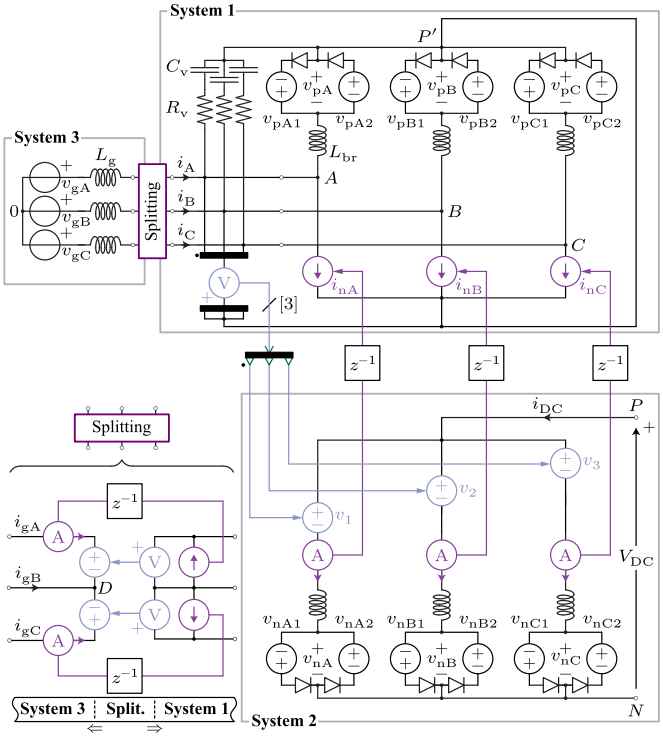


FIGURE 9. Model of the MMC relying on the use of three independent circuits. In order to respect the first Kirchhoff law in nodes *A*, *B* and *C*, the set of lower branches was replaced with the controlled current sources.

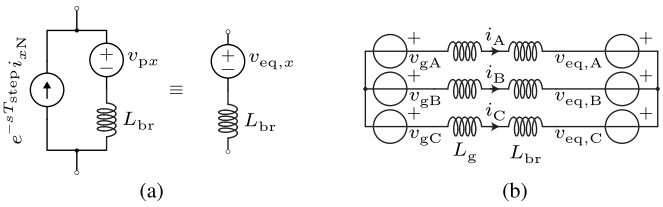


FIGURE 10. (a) Thevenin's equivalent of an upper branch being connected in parallel with the current source driven by its lower counterpart current; (b) Equivalent circuit of the analyzed MMC model seen from its AC terminals.

which is identical to the expression that can be derived from the parent circuit provided in **Fig. 4**. Since the dynamics of terminal and common-mode currents is unaffected by the proposed splitting method, so is the dynamics of the branch currents. Therefore, the model presented in **Fig. 9** replaces its counterpart from **Fig. 4**, while reducing the number of state-space matrices real-time solver needs to handle from 2^{12} to 2×2^6.

$$L_\Sigma \frac{\mathrm{d}i_{\mathrm{A}}}{\mathrm{d}t} = -\frac{2v_{\mathrm{sA}} - v_{\mathrm{sB}} - v_{\mathrm{sC}}}{3} + \frac{2v_{\mathrm{gA}} - v_{\mathrm{gB}} - v_{\mathrm{gC}}}{3} \tag{7}$$

$$L_\Sigma \frac{\mathrm{d}i_{\mathrm{B}}}{\mathrm{d}t} = -\frac{2v_{\mathrm{sB}} - v_{\mathrm{sA}} - v_{\mathrm{sC}}}{3} + \frac{2v_{\mathrm{gB}} - v_{\mathrm{gA}} - v_{\mathrm{gC}}}{3} \tag{8}$$

$$L_\Sigma \frac{\mathrm{d}i_{\mathrm{C}}}{\mathrm{d}t} = -\frac{2v_{\mathrm{sC}} - v_{\mathrm{sA}} - v_{\mathrm{sB}}}{3} + \frac{2v_{\mathrm{gC}} - v_{\mathrm{gA}} - v_{\mathrm{gB}}}{3} \tag{9}$$

Lastly, the part of **Fig. 9** labeled with "Splitting" depicts additional convenience provided by the presence of VCs. Namely, as currents flowing through the AC sources v_{gA}, v_{gB}

TABLE 1. Rated parameters of the simulated converter operating in the rectifier mode.

Rated power (S^*)	Output voltage (V_{DC})	Grid voltage (v_g)	Number of SMs per branch (N_{SM})	SM capacitance (C_{SM})	Branch inductance (L_{br})	Branch resistance (R_{br})	PWM carrier frequency (f_c)	Fundamental frequency (f_o)	Charging resistors (R_{ch})	Grid inductance (L_g)	Load resistance (R_L)	Load inductance (L_L)
0.25MVar	5kV	3.3kV	8	2.25mF	2.5mH	60mΩ	1kHz	50Hz	210Ω	13.86mH	100Ω	20mH

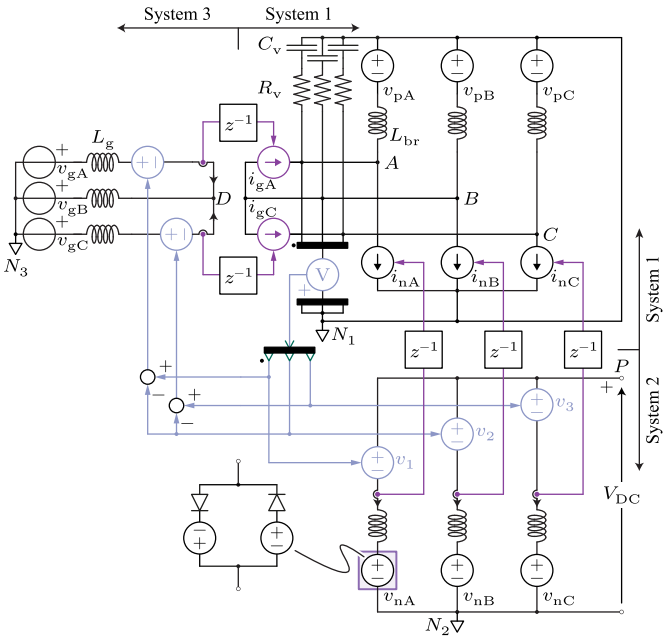


FIGURE 11. Simplification of Fig. 9 adopted with purpose of tuning the virtual network. Annotations of systems separated by delay blocks remain the same.

and v_{gC} sum up to zero, this part of the model can be separated from the circuit containing the upper branches. In summary, MMC model from **Fig. 4** was split in three parts:

- System 1 ⇒ Upper branches including VCs and VRs
- System 2 ⇒ Lower branches
- System 3 ⇒ AC grid (or AC machine, another converter coupled with the MMC through a transformer, etc.),

which allows real-time simulation step size to be reduced, approximately ten times, to $T_{step} = 7\mu s$.

IV. VIRTUAL CAPACITOR DETERMINATION

Upon the addition of VCs, state matrix A can be calculated for every valid circuit formed within the set of 2^7 possibilities derived from **Fig. 9**. Thereafter, resonant frequencies of an analyzed system can be obtained from eigenvalues of its state matrix A. As VC is actually an element possibly triggering resonance(s) in the system, it can be determined such that the model discretization step size T_{step} is at least ten times shorter than the shortest of all the system resonance periods $T_n = 2\pi/\omega_n$. However, determining the value of VC in this way is not straightforward and numerous iterations, requiring a multitude of circuits to be solved, are needed before even determining its order of magnitude. Thus, another method for VC determination is presented hereafter.

During the MMC operation, an equivalent capacitance, which depends on the number of inserted SMs [34], is actually seen between terminals of an observed branch. As the number of inserted SMs in a branch changes in time, one can realize that equivalent branch capacitance, and consequently, resonant frequencies in the system also change. Nonetheless, the SM capacitance is normally selected to limit low frequency oscillations of SM voltage [35], [36]. From the real-time simulation viewpoint, this means that, during several simulation discretization steps, the voltage across an SM cluster can be considered constant. Since the discretization step is normally too small for the instantaneous branch voltage oscillations to become visible, especially if fundamental components are considered, the above statement is justified allowing the branch to be modeled with an inductor and a constant voltage source. To put it differently, diodes used to model the branch are discarded in the forthcoming analysis, meaning that only the circuit depicted in **Fig. 11** needs to be considered in the virtual network tuning process.

Even though state-space matrices describing three systems in **Sec. III-A** are generated independently, cross-coupling among the system variables still exists. For example, current sources i_{nA}, i_{nB} and i_{nC} in System 1 originate from the branch current measurements in System 2. As a consequence, three systems used to model the MMC in real-time cannot be observed separately when tuning of VCs is to be performed, as will be seen shortly. For the moment, one can assume that currents i_{nA}, i_{nB}, i_{nC}, i_{gA} and i_{gC} from **Fig. 11** remain constant during several simulation steps. From the physical viewpoint, such an assumption is reasonable since branch inductors L_{br} are normally chosen to protect the MMC in case of a fault [37], while providing the means for control of internal low frequency components (i.e. circulating currents). Therefore, System 1 from **Fig. 11** is to be analyzed as if its dynamics was completely independent on Systems 2 and 3. On these terms, nodal analysis of System 1, conducted in the s-domain with N_1 being adopted as the reference node, reveals that its poles can be identified by solving the equation

$$3\,C_v L_{br} s\left(s^2 + \frac{R_v}{L_{br}}s + \frac{1}{C_v L_{br}}\right) = 0. \tag{10}$$

According to (10), every pole determining the stability of System 1, under the assumptions adopted above, resides in the Left Half-Plane (LHP), meaning that R_v can be set as zero. Additionally, natural frequency of the system can be calculated as $\omega_n = 1/\sqrt{L_{br}C_v}$. Following the sizing rule set as

$$T_{step} \leq 0.1\frac{2\pi}{\omega_n}, \tag{11}$$

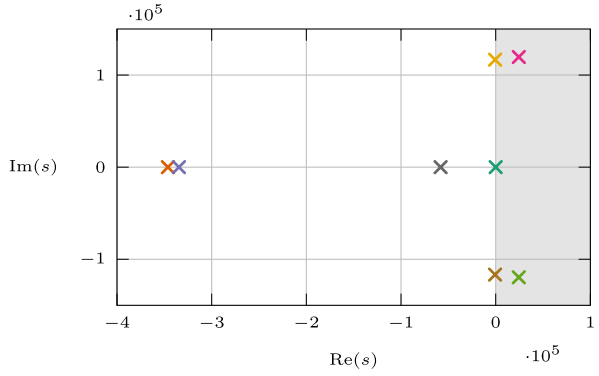


FIGURE 12. Position of poles in the network comprising the upper branches, current sources fed with the lower branch current measurements, VCs and VRs. In the presented case, VC was set as $C_v = 50$ nF, while, according to the discussion made around (10), the value of VR was chosen as $R_v = 0$.

one can set the VC as $C_{v,min} \approx 2.5\, T_{step}^2/L_{br}$. Verification of results derived in this work was performed on the exemplary converter with parameters provided in **Tab. 1**. With the Application RT Box running with the step size of $T_{step} = 7\mu$s, and based on the previously conducted analysis, the VC is tuned as $C_{v,min} \approx 50$nF. However, to validate the choice of VC and VR, one must actually solve the circuit from **Fig. 11**.

In case Tustin discretization in performed, the relationship between variables s and z is $s = (2z-2)/(T_{step}z + T_{step})$. As Systems 1, 2 and 3 are separated by delay blocks, points N_1, N_2 and N_3 can be adopted as their reference nodes, respectively. Furthermore, potentials of nodes A, B, C, D and P are of interest. Owing to cumbrousness of expressions describing the above mentioned potentials, while the circuit from **Fig. 11** can be solved by means of any tool supporting symbolic calculations (e.g. Matlab), these are omitted for space reasons. Instead, **Fig. 12** presents positions of poles for node A in case parameters from **Tab. 1** are used. As can be seen, two poles reside in the Right Half-Plane (RHP), making the system, tuned according to the above discussion, numerically unstable. One might attempt to stabilize (numerically) the system through a substantial increase of C_v. Yet, such an attempt contradicts the desire to keep the impedance of virtual elements as high as possible in the low frequency range. Another degree of freedom with regards to positioning of poles presented in **Fig. 12** lies in the tuning of VRs. However, the analyzed system is of eight order and optimizing it by hand seems to be out of reach. Please notice that the addition of VRs does not increase the computational complexity of the model as it does not introduce new state variables into the system.

This work proposes a simple algorithm able to provide a pair $\{C_v, R_v\}$ guaranteeing numeric stability of the analyzed MMC model. As can be seen in **Fig. 13**, the process of virtual elements tuning begins by defining a set of variables, some of which were already introduced in the beginning of this paper. It was assumed that an *RL* load was connected across the MMC terminals, while $C_{v,init}$ and $C_{v,end}$ denote the initial

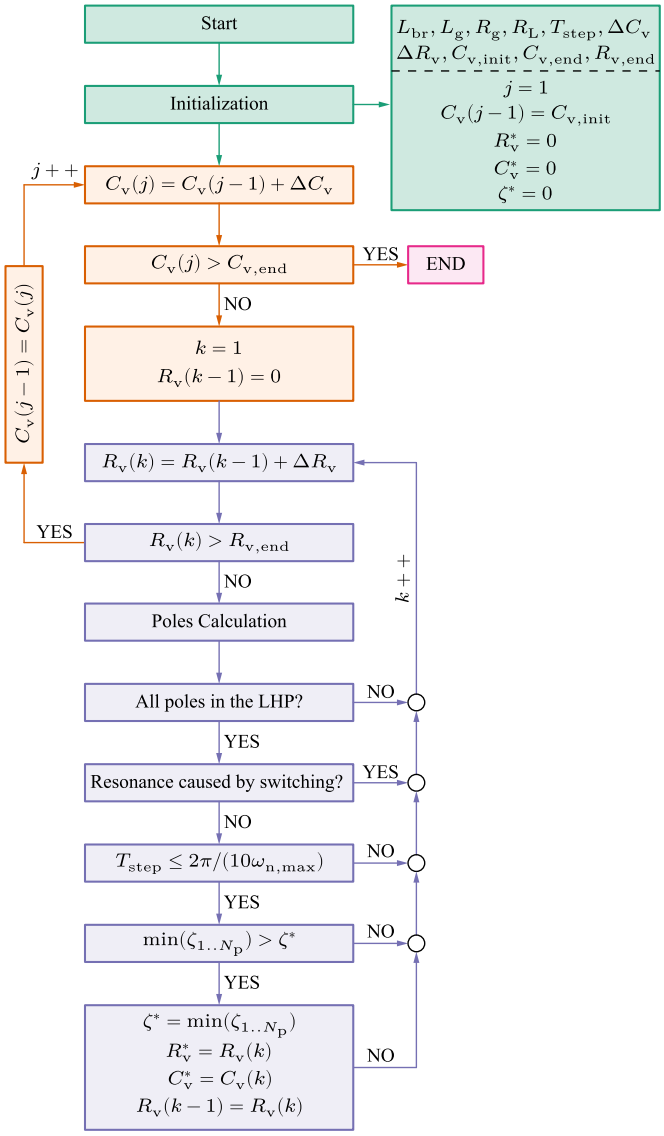


FIGURE 13. Algorithm used to determine the values of VCs and VRs.

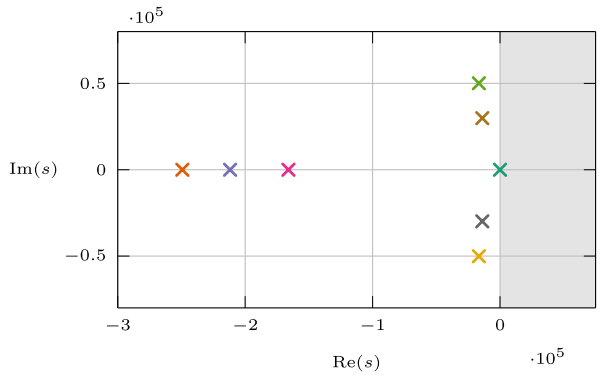
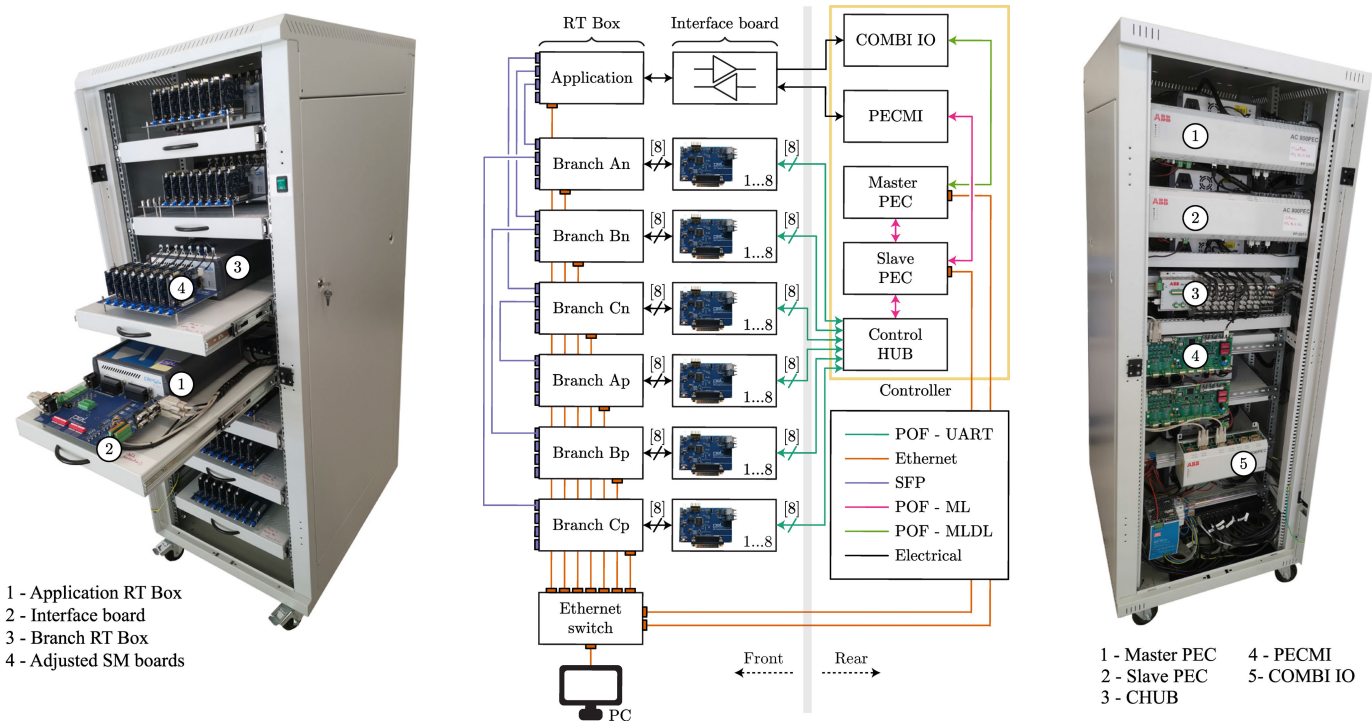


FIGURE 14. Setting the VC and VR according to (12) and (13), moves the poles presented in Fig. 12 to the positions indicated above. As can be seen, RHP remains free of any poles, meaning that the circuit presented in Fig. 11 becomes stable and suitable for real-time simulation.

and final value of capacitance being taken into account by the algorithm. Further, ΔC_v and ΔR_v denote VC and VR steps, respectively, while the final value of VR considered by the algorithm was denoted by $R_{v,end}$.



(a) Front view (b) Wiring diagram (c) Rear view

FIGURE 15. **HIL system used for model verification purpose.**

Even though previously adopted value of $C_{\mathrm{v,min}}$ does not guarantee numeric stability of the system, when combined with a suitable value of VR, it might bring the system poles into the LHP. Therefore, it is reasonable to adopt $C_{\mathrm{v,init}} = C_{\mathrm{v,min}}$. The maximum value of VC can be calculated according to a current allowed to flow through the virtual network. With parameters from **Tab. 1** and with the upper limit of VC current being equal to $\alpha = 0.5\%$ of the converter rated current, one can estimate $C_{\mathrm{v,end}}$ as $C_{\mathrm{v,end}} \approx \alpha S^*/(200\pi f_{\mathrm{o}} v_{\mathrm{g}}^2) = 365.37\mathrm{nF}$. Initial value of the VR is adopted as $R_{\mathrm{v,init}} = 0$, while its final value can be estimated by observing (10). According to (10), a pair of conjugate complex poles characterizing System 1 (assuming absolute decoupling from the other two systems) can be damped by means of VRs. Since $R_{\mathrm{v}}/L_{\mathrm{br}} = 2\zeta\omega_{\mathrm{n}}$, where ζ denotes damping factor, it is easy to calculate that $R_{\mathrm{v}} = 2\zeta\sqrt{L_{\mathrm{br}}/C_{\mathrm{v}}}$, leading to $R_{\mathrm{v,end}} = 2\sqrt{L_{\mathrm{br}}/C_{\mathrm{v,min}}}$.

Starting the algorithm implies that analytic expressions for potentials of nodes labeled with A, B, C, D and P in **Fig. 11** are already known. Once the value $C_{\mathrm{v}}(j)$ is obtained, the algorithm enters the loop where system poles are determined by substituting the value $C_{\mathrm{v}}(j)$ and $R_{\mathrm{v}}(k)$ into the analytic expressions obtained prior to commencing the calculations. All the poles obtained by the presented combination of virtual elements must reside in the LHP, otherwise, the algorithm selects a new value of VR. If, however, all the poles are stable, it must be ensured that switching of SMs will not give rise to any resonances in the circuit. If such a requirement is met, the pole characterized by the highest natural frequency, denoted by $\omega_{\mathrm{n,max}}$ is identified. Thereafter, comparison between the simulation step and period associated with $\omega_{\mathrm{n,max}}$ is made in accordance with criteria (11). Subsequently, the algorithm identifies damping factors for the conjugate-complex poles identified in the previous steps. If a minimal damping factor $\min(\zeta_{1..N_{\mathrm{p}}})$, where N_{p} denotes the number of conjugate-complex poles in the observed algorithm step, surpasses the value denoted by ζ^*, values $C_{\mathrm{v}}(j)$ and $R_{\mathrm{v}}(k)$ are memorized. In such a way, at the end of the algorithm, a pair $\{C_{\mathrm{v}}, R_{\mathrm{v}}\}$ guaranteeing the highest possible damping of resonant poles, while satisfying the criteria (11), is selected. With the following selection of algorithm steps

$$\Delta C_{\mathrm{v}} = \frac{C_{\mathrm{v,end}} - C_{\mathrm{v,init}}}{50} \tag{12}$$

$$\Delta R_{\mathrm{v}} = \frac{R_{\mathrm{v,end}}}{50}, \tag{13}$$

VCs and VRs were set as

$$C_{\mathrm{v}} = 359\mathrm{nF} \tag{14}$$

$$R_{\mathrm{v}} = 45.2\Omega, \tag{15}$$

which at the fundamental frequency provides the impedance of $Z_{\mathrm{v}} \approx 8.9\mathrm{k}\Omega$. For the energy transfer at nominal power and nominal voltage level, current flowing through the virtual network corresponds to around 0.4% of the nominal AC current, which is in alignment with the requirement set initially. Lastly, **Fig. 14** provides the position of node A poles, for the adopted values of VC and VR. As can be seen, all the poles

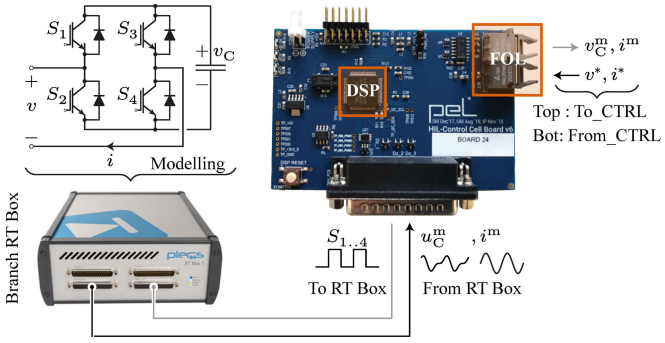


FIGURE 16. SM cards emulating the behavior of the real FB SM explained in [38]. Four switching signals are sent to the Branch RT Box, while SM DC link voltage and current are retrieved from it.

reside in the LHP, making the simulated network numerically stable, as presented in the next section.

V. MODEL VERIFICATION

A. SETUP DESCRIPTION

As presented in **Fig. 15a**, the setup used for HIL verification purpose comprises seven RT Boxes. 48 SM cards, presented in **Fig. 16**, hosting the Digital Signal Processor (DSP) and logical circuitry of the real MMC SM, described in [38], were interfaced with six Branch RT Boxes, each containing the model of an MMC branch. From the employed controller, SM cards receive three references - for terminal voltage (v), terminal current (i) and SM capacitor voltage (v_C). Subsequently, based on measurements delivered to an SM card by the RT Box it is associated with, the DSP generates switching pulses ($S_{1..4}$) being passed to the HIL unit. It must be emphasized, therefore, that voltage balancing among SMs, belonging to the same branch, is handled on the SM level and VCs discussed above have no influence on this control layer.

Seventh RT Box (fourth from the top in **Fig. 15a**), corresponds to the Application RT Box already presented in **Fig. 5**. In **Fig. 15c**, two ABB PEC800 controllers can be recognized and they are connected in the Master/Slave structure. The main reason for such a choice lies in the fact that several of these HIL systems can be connected to operate in various configurations (e.g. [39]). Slave controller is assigned the task of controlling the MMC, while Master controller is to handle the general (application) state machine and references. Other parts of the system visible in **Fig. 15c** are in charge of voltage/current measurements (PECMI), distribution of SM optical signals (CHUB) and manipulation of relays, switches and other user defined arbitrary signals (COMBIO). Real MMC prototype uses the identical control structure, making all of the presented results realistic. **Fig. 15b** provides wiring diagram of the system. Communication between the PC and other system parts is established through an Ethernet switch. As can be seen, SM cards communicate with the control system through the Plastic Optic Fiber (POF) pair, whereas conventional UART protocol is used for this purpose. Communication among different controller parts happens through POF links, however, different, ABB proprietary, protocol named MultiLink (ML), is relied on. Connection between two RT Boxes can be established through the use of SFP ports. However, one RT Box contains four SFP links, leading to the conclusion that six Branch RT Boxes cannot be directly connected to the Application RT Box. Therefore, daisy chain presented in **Fig. 15b** had to be created.

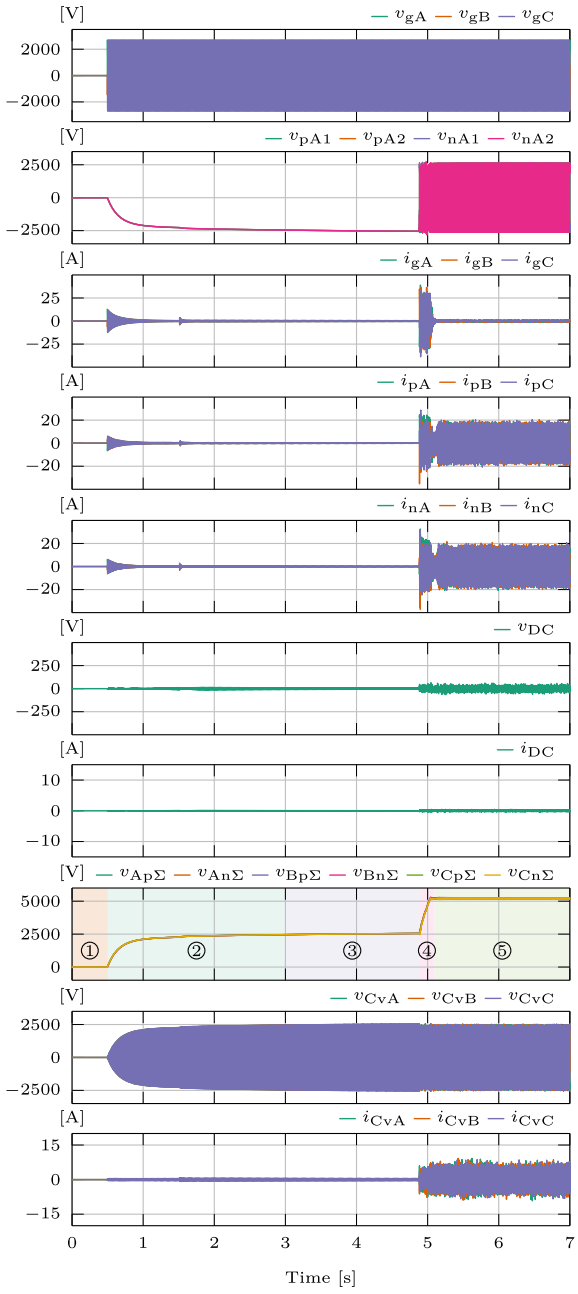


FIGURE 17. Converter charging process presented through several stages.

B. RESULTS

To validate the proposed model, the system with parameters given in **Tab. 1** was simulated on the previously described setup. Distribution of the MMC model over seven RT Boxes was performed, however, computational burden

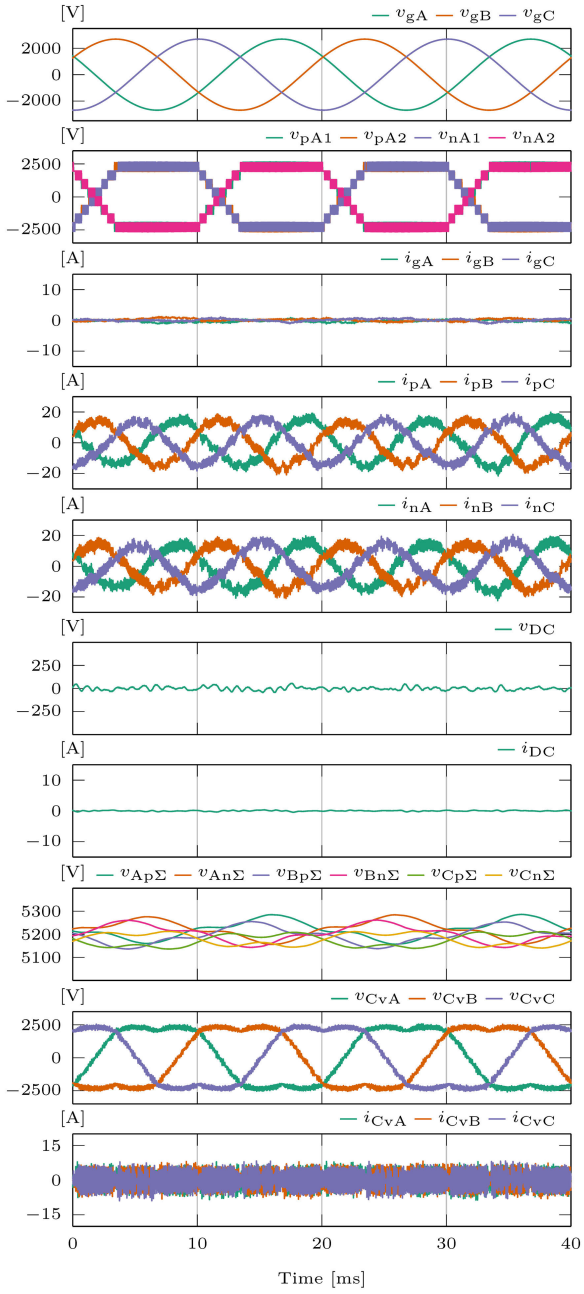


FIGURE 18. Converter operation at no load ($P_{DC} = 0$).

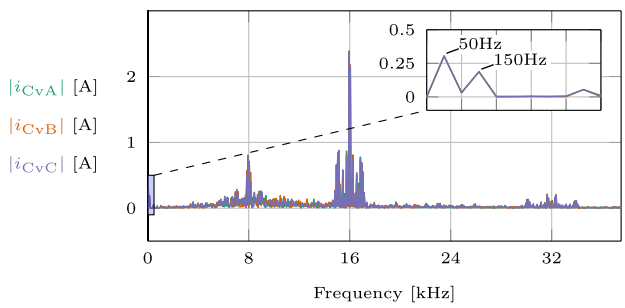


FIGURE 19. Spectral content of VC currents in case converter operates with no load on the DC side.

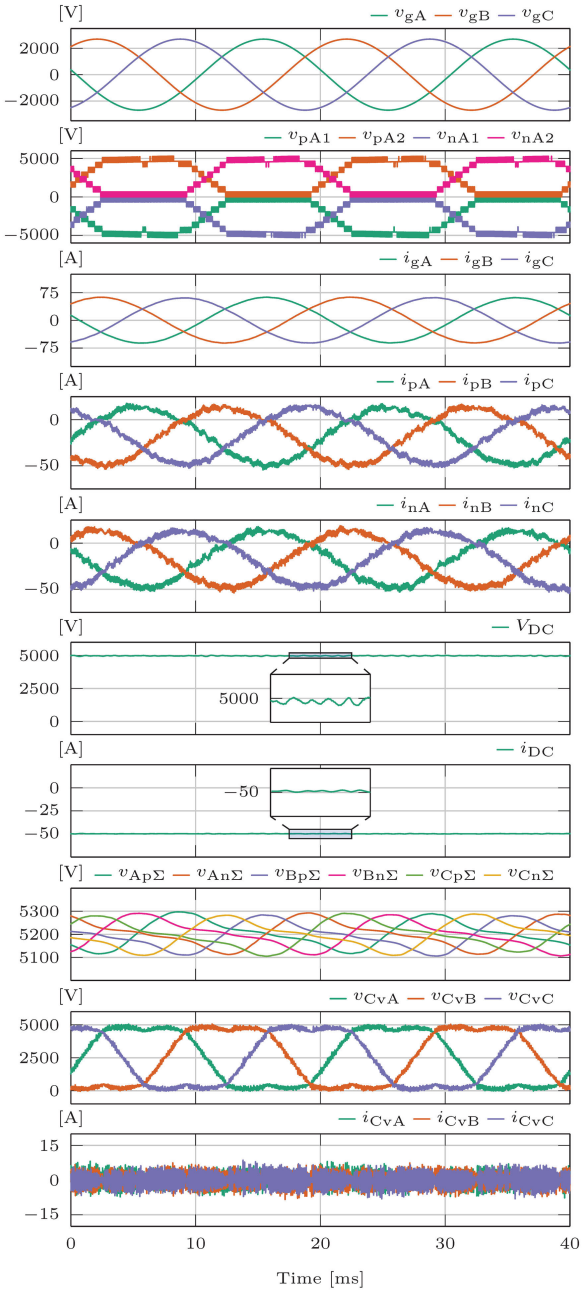


FIGURE 20. Converter operation at full load ($P_{DC} = 250$kW).

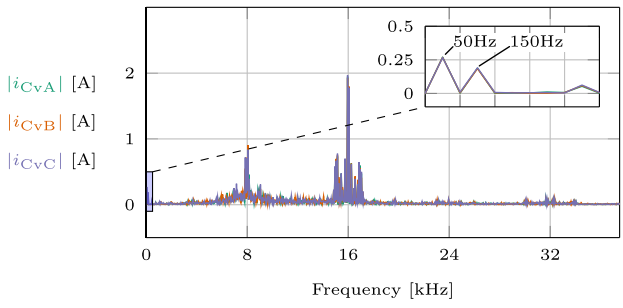


FIGURE 21. Spectral content of VC currents in case the converter operates with full load.

imposed on Branch and Application RT Boxes is not the same. Simulation step sizes were selected differently as $T_{\text{step}}^{\text{app.}} = 7\mu$s and $T_{\text{step}}^{\text{br.}} = 3.5\mu$s, while verification of the model is conducted based on different operating regimes described below.

1) MMC CHARGING

Fig. 17 reveals several stages in the converter charging process. One can see that all quantities are equal to zero as long as no voltage is present on the AC grid side. Such a situation describes the converter being disconnected from the grid and it was labeled with ①. Upon connecting the MMC to the grid, voltages v_{gA}, v_{gB} and v_{gC} become different than zero and this time instant implies the beginning of the passive charging process, labeled with ②.

Once the passive charging commences, grid currents i_{gA}, i_{gB} and i_{gC} start to flow towards the MMC. Since SM capacitors are not charged, a set of charging resistors, which is irrelevant for the scope of this paper, limits the inrush current from the grid, as can be observed from **Fig. 17**. During passive charging, every branch behaves as a single-phase diode rectifier. Consequently, branches get charged to the level matching the amplitude of the grid phase voltage. At this point, the converter is able to control its AC currents, therefore, further voltage boost can be performed through the so-called active charging process. Between passive and active charging processes there is a certain period of time, being referred to as timeout, and this period was labeled with ③.

Once the active charging process, labeled with ④, commences, branches start to switch, which can be observed from the plot presenting instantaneous values of voltage components v_{pA1}, v_{pA2}, v_{nA1} and v_{nA2}. As relevant voltage components in legs *B* and *C* are shifted by one third of the fundamental period, they are not presented in order to compress the discussed figure as much as possible. During active charging, AC grid currents are controlled such that the converter internal energy (total branch voltages) increases to the setpoint value. Once the converter gets charged, the active charging is considered over and the converter enters the operating state, which is labeled with ⑤. At this point, the converter is capable of creating an arbitrary DC voltage falling in the range of ±5kV. In the example discussed so far, $V_{DC}^{*} = 0$ for the simplicity reasons.

The last two plots present voltages and currents of the virtual network. During passive charging, envelope of voltage across the VCs corresponds to the total branch voltage components $v_{pA\Sigma}$, $v_{pB\Sigma}$ and $v_{pC\Sigma}$. Nevertheless, negligible currents flow through the virtual network during this process. When branches start to switch, currents flowing through the virtual network remain negligible, while being comprised only of higher order harmonics, as will be shown in the upcoming paragraphs. Therefore, converter terminals remain undisturbed, which is the main criteria allowing the model from **Fig. 4** to be extended by the set of VCs and VRs.

2) NO LOAD OPERATION

To prove that demonstrated modeling approach can be used in case the converter branches receive switching signals, no load operation is presented in **Fig. 18**. To control the grid currents, branches receive voltage references being realized through the PWM principles. As the number of SMs per

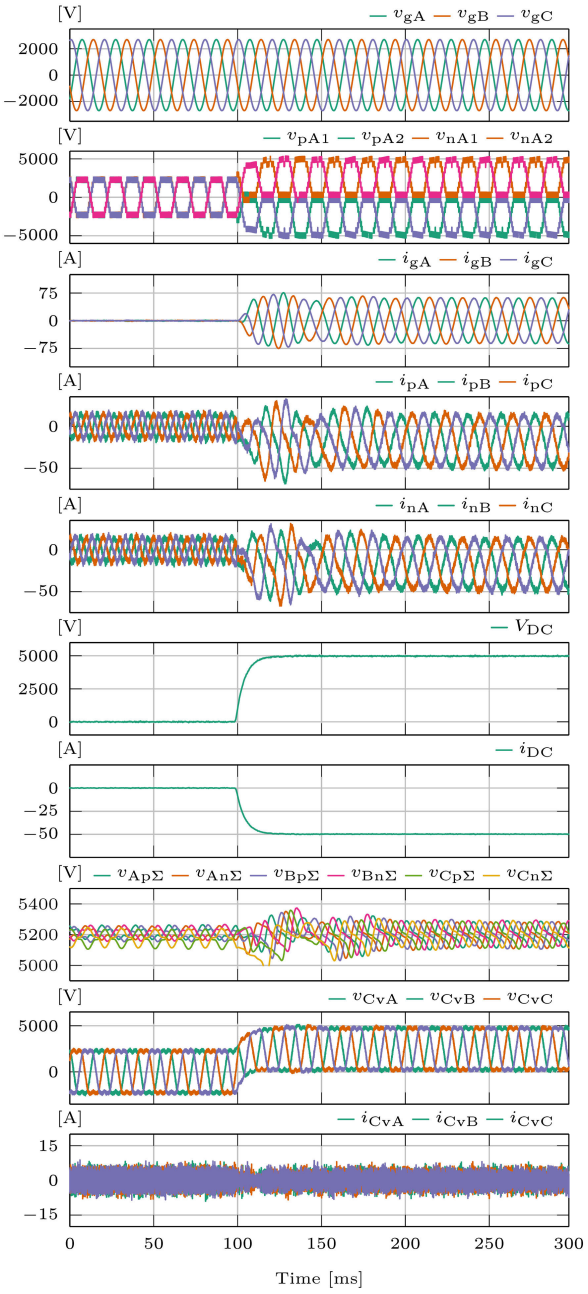


FIGURE 22. Operating waveforms in case DC voltage reference is changed from 0 to 5kV.

branch equals $N_{SM} = 8$, while approximately half of the available branch voltage range is used, every branch creates up to $N_{SM} + 1 = 9$ voltage levels, which is straightforward to confirm from **Fig. 18**.

As no power is processed to the DC side, the converter total energy balancing requires almost no current to be drawn from the AC side. However, balancing of the SM voltages, in case Phase Shifted Carrier (PSC) modulation is used, requires the presence of currents circulating inside of the converter. In this work, circulating currents at double the fundamental frequency and with amplitude equal to 20A were used, however, such a topic falls of this paper's scope. Lastly,

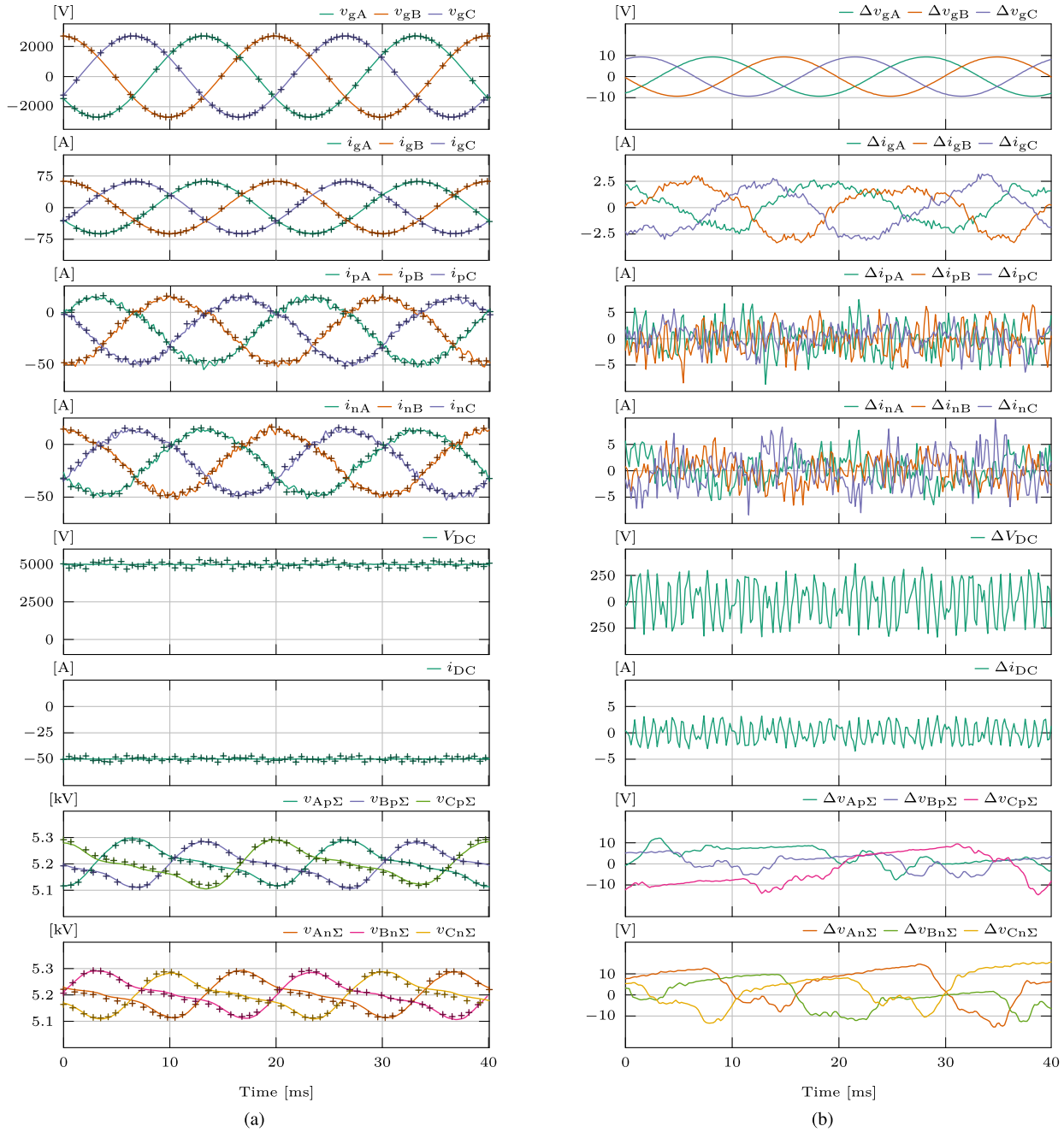


FIGURE 23. (a) Comparison of results obtained on the developed HIL platform (solid lines) and offline simulations (+ signs) at full power; (b) Difference (error) between waveforms obtained in HIL and offline simulations.

DC voltage and current average values equal zero, whereas a certain amount of ripple, being caused by the switching, cannot be avoided.

Second last plot from **Fig. 18** shows voltages measured across the VCs. As expected, voltages v_{VcA}, v_{VcB} and v_{VcC} follow the shape of the upper branch voltage references. Moreover, the presence of third harmonic, injected with the aim of extending the converter AC voltage capacity, can be noticed. To provide a better insight into the VC currents, **Fig. 21** provides their spectral content. Owing to the switching nature of the branches, most of the spectral energy is concentrated around the multiples of the frequency equal to $N_{SM}f_{sw}$. Even though the theoretical value of the branch apparent switching frequency equals $f_{app} = 2N_{SM}f_{sw} = 16$kHz, voltages of SM belonging to the same branch are never identical, therefore, the harmonic components at 8kHz cannot be completely canceled. Yet, fundamental frequency component in the VC currents equals $i_{cV}(f_o) \approx 0.25$A, which is around 0.4% of the nominal AC current. Thus, AC terminal currents are not affected by the presence of VCs, making the design procedure explained in **Sec. IV** verified.

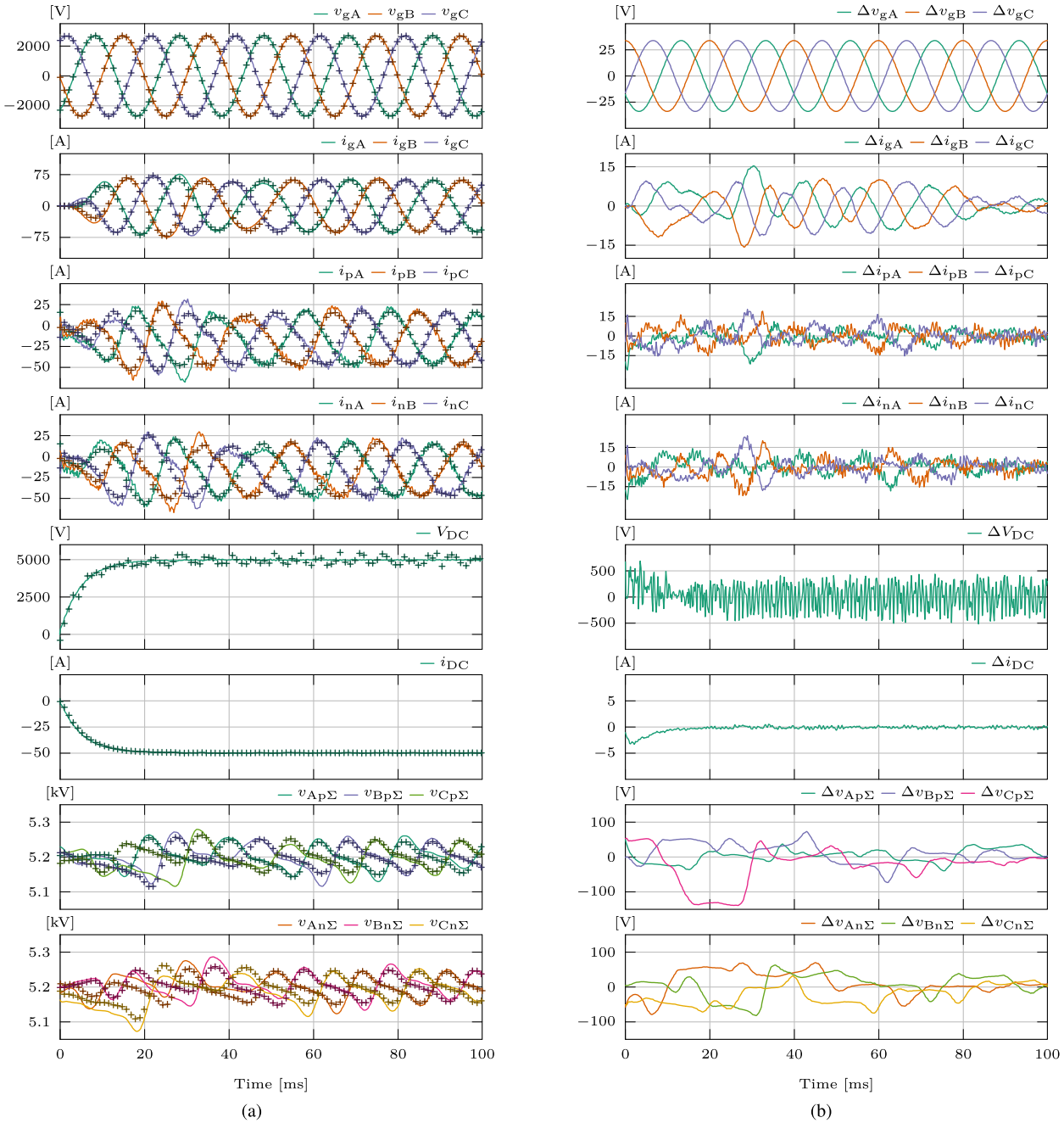


FIGURE 24. (a) Comparison of results obtained on the developed HIL platform (solid lines) and offline simulations (+ signs) in case DC voltage reference is changed from 0 to 5kV; (b) Difference (error) between waveforms obtained in HIL and offline simulations.

3) OPERATION AT FULL LOAD

Fig. 20 presents the converter operating waveforms in case energy is transferred from AC to DC side at nominal power. As the grid currents increase in amplitude so do the branch currents, which, in conjunction with branch voltages, causes branch powers, and inherently voltages, to oscillate. Comparison of instantaneous branch voltages provided in **Figs. 18** and **20** reveals the method used to generate the desired DC voltage reference. In case DC voltage labeled with V_{DC}^{*} is to be realized, both upper and lower branches contribute with $V_{DC}^{*}/2$. Similarly to the case from **Fig. 18**, DC voltage and current contain the switching ripple, however, with mean values being different than zero. Tracking of the DC voltage, labeled with V_{DC}, with a negligible error was achieved, while negative value of the DC current originates from the adopted reference direction.

Similarly to **Fig. 21**, the spectral content of VC currents was presented in **Fig. 21** indicating that, irrespective of the operating regime, VC currents fall significantly below the converter nominal currents. It must be emphasized that controllers react only to low-frequency components of currents/voltages, given that these are the only ones taking part in

the energy transfer. To put it differently, in this case, converter voltage and current ripples are filtered out with the aim of controlling only the fundamental and DC components. As a results, the presence of virtual network does not alter the basic functionality of the employed MMC model, while allowing for significant reduce in the simulation step size.

4) VOLTAGE REFERENCE CHANGE

Lastly, **Fig. 22** presents the converter operating waveforms in case DC voltage reference is changed from 0 to 5kV. In order to avoid fast discharge of the SM capacitors, a first-order filter, with the time constant $\tau = 10$ms, was applied to the DC voltage reference. What can be seen is that, apart from the voltage and current waveforms matching their theoretical shapes, current flowing through the VCs retains its most important property - negligible amplitude in the spectral part including low frequencies.

5) ERROR ANALYSIS

Before assembling the described HIL simulator, an offline simulation model (developed in Matlab Simulink and operating with fixed time-step of 12.5 μs) including detailed models of the employed controller (ABB PEC800) and the real SM (cf. [38]), was developed. It is noteworthy that the employed offline model does not use VCs, but rather the circuit depicted in **Fig. 4**.

Figs. 23a and **23b** and provide the comparison between waveforms obtained in real-time HIL simulations (solid lines) and offline simulations (+ signs in colors of signals they are associated with) in case full load operation is considered. Similarly, **Figs. 24a** and **24b** provide the same comparison in case the MMC voltage reference is changed from 0 to 5kV. As can be seen, an excellent matching between the two is achieved in both cases, which validates the statement that virtual capacitors do not alter the functionality of the model they are employed in. To put it differently, the introduction of virtual elements does not have any impact on control loops deployed outside the RT-Box (in the real controller).

VI. CONCLUSION

This paper proposed and elaborated in detail the application of virtual capacitance concept on the MMC real-time model. It targets small-scale real-time simulators, relying on the state-space modeling and requiring large simulation step sizes in case topologies with large number of switching elements are considered. Extending the MMC real-time model by the set of virtual capacitors allows for the model splitting, which leads significant reduction in the number of state-space matrices describing the system, which is a main contribution of this paper. Consequently, more than tenfold reduction in the simulation step size was observed in the example analyzed throughout this work. Virtual capacitors conduct high frequency components, however, these are normally ignored (filtered) by the controller tested against a real-time simulator. Therefore, one can claim that proposed extension of the MMC model does not alter its basic functionality, at least from the standpoint of low frequency components, which are the only ones being of importance. An extensive set of real-time simulations, performed on the hardware-in-the-loop setup comprising seven RT Boxes, interfaced with an industrial ABB PEC800 controller, validated all of the statements made above.

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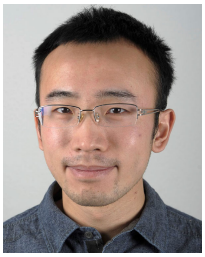

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