

Nanopillars Enabling III-V Integration on Si (100) and (111)

Présentée le 29 octobre 2021

Faculté des sciences et techniques de l'ingénieur
Laboratoire des matériaux semiconducteurs
Programme doctoral en science et génie des matériaux

pour l'obtention du grade de Docteur ès Sciences

par

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If by anything I have here written I may assist any student in
understanding Faraday's modes of thought and expression,
I shall regard it as the accomplishment of one of my principal aims –
to communicate to others the same delight
which I have found myself in reading Faraday's *Researches*.
— James Clerk Maxwell

To my family,
to my friends,
and to my students. . .

Acknowledgements

What an adventure ! As these incredible four years (and a half) are coming to an end, I realize how much I owe and how much I learned from people that surrounded me at the lab, at EPFL, at home, in Lausanne or in the rest of the world. I will try to thank everyone, something that I doubt I can do. But I will try anyway. Life is about trying :

First and foremost I would like to thank my supervisor **Anna Fontcuberta i Morral**. Anna is a person of heart that will never fully be able to understand how much of an impact she had during my studies. From being my teacher already in second year Bachelor, to coming with our class to Japan during the student trip. From co-supervising my master thesis to supervising my PhD. Anna transmitted me the love for semiconductor science, taught me to believe in myself and was always here when I needed it. And if she thinks going the extra mile for students is "just doing her job", then she is doing an **amazing** job, and I really hope I can be half as good as her in my career. Thank you, Anna. For everything.

I would like to thank **Kirsten Moselund**, **Erik Bakkers**, **Michele Ceriotti** and **Dragan Damjanovic** for agreeing to be on my PhD defense committee. I feel very humbled to have you judging my work, and I very much look forward to the discussion.

I would like to thank our collaborators **Renato Minamisawa** and the team at EULITHA, **Harun Solak**, **Christian Dais** and **Li Wang** for providing samples and knowledge on the Si (111) pillars project. This part of my work would have not been possible without your support. Thank you to **Jordi Arbiol** and **Sara Martí-Sánchez** from ICN2 for the fruitful collaboration and their electron microscopy expertise on the first nanoplates paper.

I would like to thank my colleagues, the "LMSC squad", as nothing would have been possible without them. First I would like to thank **Gözde Tütüncuoğlu** for being my semester project supervisor and bearing with me as I was discovering the

Acknowledgements

world of optoelectronics. This project showed me that nanostructures can be fascinating ! Thank you **Luca Francaviglia** and your little braid (Why do I remember this so vividly ?) for showing me the CL at that time, and thank you for all the great time we shared in and out of the lab. I would like to thank **Jean-Baptiste Leran** without who our MBE would have never survived all the obstacles of life (and of the PH building !). You showed me that nothing is fixed by just looking at it. I value our time representing the french culture in the lab and sharing our passion for cheese. Speaking about MBE, I would like to thank all of the III-V team with who the collaborations (and laughs) were so enriching : Thank you **Wonjong Kim** for introducing me to the Korean "way of life", including agarijous, pajeons and even inviting me to your wedding ! Flying to Korea and sharing this moment with you and **Sol Lee** was an honour. I cannot believe you guys agreed to let me speak in the world's most broken Korean, in front of everyone. This is true friendship. Thank you **Martin Friedl** for being the multi-talented person that you are, showing me that technical challenges are actually what makes life so enjoyable. And also for bearing with my hobbies monologues ! I truly cherish all those hours we spent as Snorlax and MBreezy, and I value your friendship. Thank you **Mahdi Zamani** for showing me that it is truly possible to go until the end of an idea and turning it into something great (liquid ordering was not trendy when you first talked about it). Thank you **Lea Ghisalberti** for teaching me the importance of listening to others. Thank you **Akshay Balgarkashi** for all the time we spent as flatmates, for all the laughs and positivity, for changing Beatrix's opinion about the Indian culture. Thank you **Didem Dede** for being **Didem Dede**. I don't know how to say it differently : you are a unique, cheerful, explosive person and I am truly grateful to count you as my friend. Thank you **Nicholas Paul Morgan** for all the times shared at PolyDoc, for widening my perspective about life, for sharing all these memes. For someone that wanted to have "zero responsibility", I can tell you that you have a part of it in this work and in my life. Thank you **Valerio Piazza** for nuancing my views on my research, for being so optimistic and interested in what I do. It's hard to explain how much someone else telling you "this is interesting" while looking at your work means. Thank you **Michele Zendrini**, even if you joined not so long ago, I can feel you are a great addition to the lab ! But life for me at LMSC was not only at the MBE room, and I would like to thank all of the other lab members : Thank you **Nicolas Tappy** for the immense support you gave me in CL, but also for being a great friend. You showed me the passion for instrumentation, for long discussions about life, for coffee. You are the definition of the french saying: "avoir le coeur sur la main". Thank you **Santhanu Panikar Ramanandan** for being such an intense human being, for making me believe in the million q-bits dream. Thank you **Rajrupa Paul** for being

Raj, I think that says it all. Thank you **Simon Escobar Steinvall** for showing me how electron microscopy can be fascinating. Thank you **Andrea Giunto** for showing me that confidence and success can go hand-to-hand with kindness and humour. Yes, you learnt to endorse being "the worst" but I truly believe that most of the times, you are the best. Thank you **Elias Stutz** for showing me that not everything is conveyed through words, and that sharing joy can transcend the human voice. Thank you **Anna Kúkol'ová** for all the dinners, apero's or rants we shared about anything. Our time together is like my experience with Tatratea, in a way : the sharing times were breve, but fruitful, and I wish there was more. Thank you **Claire Blaga** for being such a colourful person, and bringing your optimism to the lab. Thank you **Dmitry Mikulik** for your faith in nanowire solar cells, and for showing me that great PhD thesis come in all shapes or form. Thank you **Pablo Romero Gomez** for all the collaborations and great discussions about science, politics or Córdoba. Thank you to **Alok Rudra** and **Benjamin Dwir** for the great work we did with the MOVPE, for allowing me to design and characterize growths outside of our MBE world !

Many many thanks to the **CMi staff**. EPFL is where it is due to you, to your hard work, to your advices, to your trainings and your fixes. I want to thank particularly **Joffrey Pernollet**, **Cyrille Hibert** and **Remy Juttin** for the process advices, for the technical support and for the nice conversations we had between two book-ings/trainings. Joffrey, I don't understand how you are so nice. It is a super-power. Please stay the same. Cyrille, I admire your morals, your perfectionism and your kindness. Remy, you were the first person to train me in the clean room when I was in Master and I knew I was off for a great start. Thank you **Zdenek Benes** for teaching me electron-beam lithography, for showing me that it is indeed possible to love and hate an equipment at the same time. Thank you **Niccolo Piacentini** for sharing with me your passion for DUV lithography, for helping me so much while I was trying to figure out how to make my process work. I truly owe you this great discovery in my life. Thank you **Gatera Kumuntu** and **Patrick Madliger** for all the support regarding logitics and equipment. Patrick, your "bad cop" role might sometimes bring you trouble sometimes, but I truly believe we need someone endorsing this role and that you do an incredible job. Please stay the same. An last but not least, thank you **Didier Bouvet**. It is hard to explain, but I am sure my PhD would have been very different without you. Many thanks as well to the whole **CiMe** staff for teaching me electron microscopy and always maintaining the microscopes to a perfect state. I would also like to thank **EDOC** and more particularly **EDMX** for always helping with administrative matters (more particularly **Chrystelle Demierre** and **Anne Kolly**).

Acknowledgements

People outside of the lab, even if not directly in touch with my research, played an immense role in helping me succeed.

First I would like to thank my family : My sister **Sandra Güniat** with who I shared most of my life and that is so important to me. She was always here, in the good and the hard times, and I truly value our relationship that we managed to keep after leaving home. My mother **Laure Enouf** for being one of the most amazing women I know, for raising me with all her love and embracing me in all my annoyingness. My father **Serge Güniat** for being such an inspiration, for teaching me to embrace who I am and love what I love. You all always encouraged me in all my passions, my interests, and now I hope you are proud of what I can accomplish with what you taught me. My grandmother **Geneviève Enouf** that unfortunately will never be able to read those lines. You passed away right before I could graduate, and I would have loved you to see me succeed. We shared amazing moments that you remembered until the very end, and you will forever live in the hearts of the people that loved you. My uncle and aunt **Agnès Enouf** and **Philippe Sibourd**, my cousins **Roxane, Vanessa and Cyrielle** and her partners **Antoine, Damien and Fabien**.

Now I would like to thank my friends outside of LMSC. First my best friend **Jose Hoyos** for being such an amazing person. The connection we have is so important to me that I consider you as my brother. You showed me that life is not only about thinking, but also to act. You taught me so much about myself and made me grow as a person. Thank you, Jose. Thank you also to **Alvaro Charlet** for the amazing moments we always share, for sharing me your love for design and 19th/20th century artists. Thank you to the Cat's home, my second family, and more specifically the **Mokhtari Family**, Beatrix, Soraya and Elias. When I arrived in Switzerland my real family was far away, and you adopted me into your home. I will never be thankful enough for all the laughs, the support and the emotions we shared in the Uttins house. Thank you to, of course, to all the cats **Filou, Khatoussa, Khalousha, Charlie, Princesse, Dasha** that provided me with so much joy. Thank you **Lucas Chays** for showing me that silliness is the purest form of humour and that raging over Age of Empire is OK, **Laurent Michaud** for bearing with my poor athletic abilities and sharing with me great moments on the bike and around a beer, **Leo Garin** for being such a great friend with so many talents and resources, showing me that life is so much more than work, **Guillaume Bonneau** for all the great times discussing about life, neuroscience, youtube videos, and ultimate chicken horse, **Armin Sigmund**

our antartic explorer, **Felix Martel** for all the crazy gaming nights, **Clémence Thébaud** for being such an interesting and complete person, **Tomáš Krásnie** for making me discover Horcize, and all the other Cat's home people. I would like to thank also the whole Lausanne korean group that included me in many events, evenings and fun times : **Mintae Chung** for being an amazing friend, **Dong Cheon Kim** for showing me that sometimes, "almost entering to a disco" is enough for a fun night, **Hyungoo Ji** and your incredible home-made maggkeoli, **Semin Kwak** and **Jeonghyeon Kim** and **Sol Lee** for sharing so much with me. Thank you to **Philippe Schwaller** for being such a talented, funny and trustful person. You showed me that everything can be mastered if given the time, effort and interest.

I would like to thank **Sho Watanabe**, for the great friendship that we share and for being who you are. You taught me that fun can come in many shapes or form, and that sometimes it is alright to let your crazy side shine ! I would also like to thank all the LMGN people, **Korbinian Baumgärtl**, **Ping Che**, **Andrea Mucchiello**, **Maria Carmen Giordano** and **Mohammad Hamdi**.

I would also like to thank all my students, hoping they learnt as much from me that I learnt from them : **Morgan Binggeli**, my first student that is now pursuing a PhD, **Oscar García** for all the fun and the great science and for inviting me to your thesis defense, **Mégane Boscardin** for her tenacity at measuring contact angles, **David Vindice** for the great help on pillars, **Alexandra Byba** for being a great student on a project that was tough, **Luca Schaufelberger** for being so passionate and so creative, **Shreyas Joglekar** for wanting to deeply understand things, **Titouan Charvin** for persevering despite the very trying times that we experienced, **Raphaël Lemerle** for your great work on TEM imaging that is now getting submitted, **Antonia Hager** for your creativity in problem solving and your tenacity. Thank you to all the student I had during my teaching-assistant sessions : I am very thankful for you asking great questions, and me mainly trying to come up with a good-enough answer. Now, it might be weird for some, but I wish to thank my university, **EPFL**. Before starting my studies I would have never imagined how much of a positive impact an establishment can have. EPFL gave me everything in my scientific career : the knowledge, the tools, the experience, the laugh during events, the stress during exams, the joy at the end of the ride. I hope I can now represent my school in my career and make it grow as much as it made me grow. Thank you, EPFL.

And of course I would like to thank **Fanny Borza**, for being one of the most amaz-

Acknowledgements

ing women I know, for being such an incredible partner in life, such a creative, bright human being. The love you give me every day is certainly the second reason I managed to succeed, the first one being how you made me believe in myself. I am so grateful to be able to share my life, my doubts, my laughs and my tears with you. I love you. I would also like to thank her family that always supported me and with who we share amazing moments : Her sisters **Chloé** and **Inès**, her father **Alain**, her mother **Danielle**, **Philippe Weber**, **Christian**, her uncles and aunts, and all the family friends (thinking about the Crooks, the Tyburn's, The Gradewohl's, the Muller's and others).

That was a long list, nevertheless I am sure I missed people. If yes, I am sorry. What is for sure is that I thank you all deeply, and that I cannot wait to see what the next chapter of my life has in stock.

Lausanne, September 28, 2021

L. G.

List of Publications

First-Authored Publications

- Güniat, L., Martí-Sánchez, S., Garcia, O., Boscardin, M., Vindice, D., Tappy, N., Friedl, M., Kim, W., Zamani, M., Francaviglia, L., Balgarkashi, A., Leran, J. B., Arbiol, J., & Fontcuberta I Morral, A. (2019). III-V Integration on Si(100): Vertical Nanospades. ACS Nano, 13(5), 5833–5840.
- Güniat, L., Tappy, N., Balgarkashi, A., Charvin, T., Lemerle, R., Morgan, N., Dede, D., Kim, W., Leran, J.B. Fontcuberta i Morral, A., (2021). Light emitting InGaAs Heterostructures on Si (100) integrated GaAs Nanospades. *Manuscript to be submitted*
- Güniat, L., Ghisalberti, L., Wang, L., Dais, C., Morgan, N., Dede, D., Kim, W., Leran, J.B., Balgarkashi, A., Minamisawa, R., Solak, H., Carter, C. and Fontcuberta i Morral, A. (2021) GaAs Nanowires on Si Nanopillars : Towards Large Scale, Phase-engineered Arrays. *Manuscript to be submitted*
- Güniat, L., Caroff, P., & Fontcuberta Morral, A. I. (2019). Vapor Phase Growth of Semiconductor Nanowires: Key Developments and Open Questions. Chemical Reviews.
- Kim, W., Güniat, L., Fontcuberta I Morral, A., & Piazza, V. (2021). Doping challenges and pathways to industrial scalability of III-V nanowire arrays. Applied Physics Reviews, 8(1).

Co-Authored Publications

- Friedl, M., Cervený, K., Weigele, P., Tütüncüoğlu, G., Martí-Sánchez, S., Huang, C., Patlatiuk, T., Potts, H., Sun, Z., Hill, M. O., Güniat, L., Kim, W., Zamani, M., Dubrovskii, V. G., Arbiol, J., Lauhon, L. J., Zumbühl, D. M., & Fontcuberta Morral, A. I. (2018). Template-Assisted Scalable Nanowire Networks. Nano Letters, 18(4), 2666–2671.

List of Publication

- Zamani, M., Tütüncüoğlu, G., Martí-Sánchez, S., Francaviglia, L., Güniat, L., Ghisalberti, L., Potts, H., Friedl, M., Markov, E., Kim, W., Leran, J.-B., Dubrovskii, V. G., Arbiol, J., & Fontcuberta i Morral, A. (2018). Optimizing The Yield Of A-polar Gaas Nanowires To Achieve Defect-free Zinc Blende Structure And Enhanced Optical Functionality. *Nanoscale*, 10(36), 17080–17091.
- Kim, W., Dubrovskii, V. G., Vukajlovic-Plestina, J., Tütüncüoğlu, G., Francaviglia, L., Güniat, L., Potts, H., Friedl, M., Leran, J. B., & Fontcuberta I Morral, A. (2018). Bistability of Contact Angle and Its Role in Achieving Quantum-Thin Self-Assisted GaAs nanowires. *Nano Letters*, 18(1), 49–57.
- Francaviglia, L., Giunto, A., Kim, W., Romero-Gomez, P., Vukajlovic-Plestina, J., Friedl, M., Potts, H., Güniat, L., Tütüncüoğlu, G., & Fontcuberta I Morral, A. (2018). Anisotropic-Strain-Induced Band Gap Engineering in Nanowire-Based Quantum Dots. *Nano Letters*, 18(4), 2393–2401.
- Dubrovskii, V. G., Kim, W., Piazza, V., Güniat, L., & Fontcuberta I Morral, A. (2021). Simultaneous Selective Area Growth of Wurtzite and Zincblende Self-Catalyzed GaAs Nanowires on Silicon. *Nano Letters*, 21(7), 3139–3145.
- Vukajlovic-Plestina, J., Kim, W., Ghisalberti, L., Varnavides, G., Tütüncüoğlu, G., Potts, H., Friedl, M., Güniat, L., Carter, W. C., Dubrovskii, V. G., & Fontcuberta i Morral, A. (2019). Fundamental Aspects To Localize Self-catalyzed III-V Nanowires On Silicon. *Nature Communications*, 10(1), 869.
- Balgarkashi, A., Ramanandan, S. P., Tappy, N., Nahra, M., Kim, W., Güniat, L., Friedl, M., Morgan, N., Dede, D., Leran, J. B., Couteau, C., & Fontcuberta I Morral, A. (2020). Facet-driven formation of axial and radial In(Ga)As clusters in GaAs nanowires. *Journal of Optics (United Kingdom)*, 22(8).

Abstract

The majority of current semiconductor technologies are built on Si (100), such as the CMOS technology, or conventional solar cell devices. III-V semiconductors offer great perspectives given their high carrier mobility and direct band gap. However their integration on Si remains a challenge: defects due to the lattice mismatch and cost, among others. We explore the growth of nanostructures using molecular beam epitaxy as a potential solution. Nanostructures possess a very low footprint, limiting defects at the interface and throughout the active material. If grown using the VLS mechanism, the catalyst droplet configuration permit to engineer the crystal phase in wurtzite or zinc-blende, opening perspectives for III-V phase-engineering. In this work we studied the use of Si nanopillars as a patterning method in order to grow vertical nanostructures on Si (100) that we coined nanospades. Nanospades exhibit a bi-crystal structure and a high crystalline purity, making them great candidates for optoelectronics on Si (100). Therefore we grew InGaAs heterostructures on Si (100) using vertical nanospades as templates and demonstrated optically-active structures that emit in the infrared. We unveiled an emission spatial splitting in the emission spectra throughout the nanospade. We correlated this feature with the unique crystalline structure of the nanospade and show the potential for manufacturing dual wavelength light-emitting diodes.

We also explored the use of Si nanopillars on Si (111) for growing large-area GaAs nanowire arrays. We first identified the key parameters and fundamental aspects of nanowires growth on Si pillars by electron-beam lithography where we reached vertical yields of 55%. We showed that the droplet configuration, i.e contact angle and triple phase line, are central for a successful growth, and that the pillar geometry permits to engineer the droplet contact angle. We compared our experiments with simulations performed in Surface Evolvertm and observed a strong correlation. We then manufactured SiO_2/Si pillars using phase-shift lithography and grew large-area GaAs nanowire arrays. We reached a maximum local vertical yield of 67% and a global chip-scale yield of 40%. We also unveiled the potential for phase engineering using the pillar geometry.

Résumé

La grande majorité des microtechnologies modernes reposent sur l'usage de substrats de Si, comme la technologie CMOS ou encore les cellules solaire conventionnelles. Les semiconducteurs III-V possèdent un grand potentiel grâce à leur haute mobilité de charges ainsi qu'à leur bande interdite au gap direct. Seulement, leur intégration sur Si reste un défi, entre autres à cause de l'apparition de défauts dus à la différence de paramètre de maille, ou bien du coût. Nous explorons la croissance de nanostructures par épitaxie à jet moléculaire afin de pallier à ces problèmes. Les nanostructures possèdent un facteur de surface très bas, ce qui limite les défauts à l'interface ainsi que le long de la structure cristalline. Si celles-ci sont crûes en utilisant la méthode VLS, la configuration de la goutte catalyseur permet de sélectivement choisir la phase cristalline entre wurtzite et zincblende. Lors de cette thèse, nous avons étudié l'utilisation de piliers en Si afin de fabriquer des réseaux de nanostructures verticales sur Si (100). Nous avons appelé les structures résultantes nanospades. Les nanospades possèdent une structure bi-cristalline d'une très haute pureté, ce qui en fait des candidates idéales pour la pratique de l'optoélectronique sur Si (100). Nous avons donc fait pousser des hétérostructure InGaAs sur Si (100) en utilisant des nanospades comme supports. Nous avons démontré l'obtention de structures émettant dans l'infra-rouge et possédant une bi-émission séparant le spectre le long du nanospade. Nous avons lié ce comportement à la cristallographie unique du nanospade et avons démontré son potentiel pour la fabrication de diodes électroluminescentes à double longueurs d'ondes.

Nous avons également exploré l'utilisation de piliers en Si sur Si (111) afin de faire pousser des réseaux de nanofils de GaAs sur une très large surface. Nous avons en premier identifié les paramètres clés de ce système ainsi que ses aspects fondamentaux en fabriquant des piliers par lithographie à faisceaux d'électrons. Nous avons atteint un taux de nanofils verticaux de 55%. Nous avons démontrés que la configuration de la goutte catalyseur, autrement dit son angle de contact et ligne triple, est d'une importance majeure pour obtenir une bonne croissance. Nous avons également démontré que la géométrie du pilier de Si permet de maîtriser l'angle de contact à notre guise. Nous avons comparé nos résultats à des simulations

Résumé

faites sur le logiciel Surface Evolvertm et avons observé une bonne corrélation. Nous avons ensuite fabriqué des piliers en SiO_2/Si par lithographie de masque à décalage de phase et avons fait pousser des réseaux de nanofils sur de très grandes surfaces. Nous avons atteint un taux de 67% localement ainsi que 40% à l'échelle du substrat. Nous avons également démontré le potentiel de sélection de phase par l'utilisation de piliers en Si.

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1 Motivation and Context

”Über Halbleiter soll man nicht arbeiten, das ist eine Schweinerei; wer weiss, ob es überhaupt Halbleiter gibt”.

Or poorly translated, *”one shouldn’t work on semiconductors, that is a filthy mess; who knows whether any semiconductors exist”.*

Although they seem harsh, those words belong very well to the era they were written at. They are from a letter sent by the Physics Nobel prize winner, theoretical physicist and quantum physics pioneer Wolfgang Ernst Pauli, to Rudolf Peierls in New-York city in 1931. They illustrate the historical reputation of semiconductor materials, hence of semiconductor physics : a non-reproducible, non-explainable, non-desirable *”filthy mess”*. Pauli does not save his words, *excluding* even the existence of what is now the pillar of modern electronics.

The goal of bringing this up is not to criticize Pauli for what he wrote. The interest of such citation is in the understanding of its contemporary veracity. When and why was the scientific community so reluctant to study “materials with midway non-reproducible resistivities” ?

Examining the historical journey of our field shines light on what makes semiconductor physics so interestingly different. By grazing on challenges faced in the 19th and 20th century, we are able to apprehend the ones we are facing today, and hopefully tackle them along with the ones of tomorrow. In the next section, we will shortly describe the rise and fall of obsolete concepts, to continue with current interrogations in semiconductor technologies and to finish, our way of answering them.

1.1 Semiconductors and their Semiaccurate Story

In 1731, studies reported by Stephen Gray in a letter to the UK Royal Society secretary show a qualitative characterization of many materials' conductivities. He started by observing the attraction of light metallic particles on a statically-charged surface. He wondered then how far can this effect be extended. Stephen ended up making a "communication line" of over 250m in which he could transmit an "electric effluvium". This is considered one of the pioneering work of solid electric conduction.

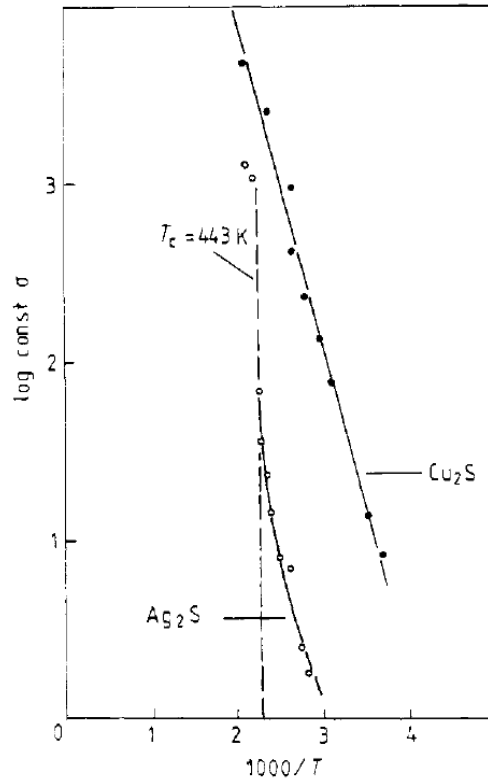
With the growing number of similar experiments, scientists saw in electricity an opportunity to create a safe source of light, but also to send signals over very long distances. *Tensions* between european nations during the 19th century were undoubtfully a motivation for the development of fast and reliable communication methods. This period led many countries to perfectionnate their knowledge of electrical conductivity and the behavior of elemental, binary, ternary compounds under heat or reduced temperatures.

Semiconductors were discovered in this context, between the end of the 18th and the beginning of the 19th century. As their name suggests it, they were revealed by their conductivity of "semi-metallic" nature. The first mention is attributed to Alessandro Volta in a paper read to the Royal Society in 1782. After the invention of his pile, Alessandro had in his possession a powerful and stable source of electricity. He studied the time needed for a pile drainage when discharged through different materials. Metals were doing so instantly, insulators not at all, and semiconductors slowly. This led the way to a more quantitative study performed by Johann Wilhelm Hittorf[20, 104] in 1851 where he describes the change in electrical conductivity of Ag_2S and Cu_2S with temperature. The puzzling fact about these compounds is that they exhibit a *positive change in electrical conductivity* with increasing temperature. Figure 1.1 shows a plot of the measurements done by Hittorf. Cu_2S displays a linear relation of $\log(\sigma)$ with $1/T$, which have been explained much later by the relation :

$$\sigma \propto \exp \frac{-E_g}{2kT}$$

where σ is the material's conductivity in $\Omega.m$, E_g is the band gap energy in eV, k is the Boltzmann constant and T the temperature in Kelvin. This equation characterizes intrinsic semiconductors at relatively high temperatures (more than 400K).

1.1. Semiconductors and their Semiaccurate Story



Chapter 1. Motivation and Context

Wilson for the use of Bloch's functions for derivating the band theory in solids and establishing the notions of "intrinsic" and "extrinsic" semiconductors. They set foundations for a new emerging field later called *solid state physics*. While theoretical knowledge of quantum and solid state physics was revolutionizing how we see matter, two major characteristics of semiconductor systems played an immense role in the materials' industrial interest : rectification and amplification.

Simply defined, rectification is the act of converting an alternative current (AC) to a direct current (DC), and amplification is the act of *amplifying* any signal. Rectification is essential to the world of telecommunication, more precisely telegraphy, as a electro-magnetic (EM) waves received by an antenna produces an AC signal, but needs to be converted into DC in order to be heard with any kind of audio device. The first used rectifiers were solid-state (Germanium or Galena "cat whisker" point contact crystal diode) but were completely supplanted by vacuum tubes at the beginning of the 20th century until the 1940s. Vacuum tubes, working on the thermionic principle, were much more reliable to manufacture and to use, but most importantly they were capable of amplification, what point contact crystal diodes could not do. But it is with the development of radar that nation's interest in solid-state rectifiers amplifiers raised from the ashes. In fact, state-of-the-art vacuum tubes like triodes and pentodes were making very poor detectors in the 3000-4000 MHz range, and in order to perform had to be pushed beyond their operation limit, reducing their lifetime to about 4 hours. the fundamental problem was the transit time of electrons traveling from the cathode to the anode and the relatively high capacitance between the latter, creating a slow response rate.

During all these years, however, semiconductor science did not disappear. The community was now aware of the extreme sensitivity of doping, and that when prepared correctly, Solid-state diodes showed record-breaking fast responses due to the absence of transit time of charges and the relatively low capacitance. The forgotten crystalline semiconductor system now seemed to be the answer for humanity's new urging needs. Manufacturing techniques evolved and technologies permitted the refinement and isolation of certain elements. Industrial production of such devices became feasibly nigh. Vacuum tubes were progressively left behind and the semiconductor era was coming fast. Labs and fabs focused their effort on the purification of Ge and Si, along with controlling re-introduced dopants. It was a strange dance between pureness and controlled chaos that lead to the birth, in 1947 at Bell Laboratories, of the first solid-state transistor.

The rise and fall of vacuum tubes, mid-tier performers but reliable to manufacture, permits to reflect on solid-state semiconductors very central challenges : As magnificent and desirable as they can be, 0.01% of an uninvited element will completely change the device's performance. Sample preparation does not let room for approximations : a meticulous control over the elements natures, compositions and concentrations is crucial for creating a device that works as intended. But if one understands and applies the correct experimental techniques, it is possible to create a plethora of powerful, energy-efficient, inexpensive objects.

As will be discussed further, state-of-the-art III-V nanostructures and their integration onto Silicon bears remarkable similarities with 19th century Galena point-crystal diodes. Sample preparation, manufacturing techniques, but also doping, are still open questions.

1.2 III-Vs on Si : The Challenge

Nowadays, Si can very well be considered as "the king of all semiconductors" in terms of production volume. Si wafer-based Photovoltaic panels constitutes 95% of all the solar panel production in 2019 [66]. The current major platform for integrated circuits such as sensors, non-volatile random access memory (NVRAM), microprocessors and batteries is the complementary metal-oxide-semiconductor (CMOS) platform, also Si-based. This abundance in use, among other reasons (such as the high Si oxide quality), can be explained by its earth abundance, as more than 90% of the earth's crust is composed by silicate minerals, which puts Si at the second place for most abundant element on our planet (right after the one we breathe, oxygen).

The increasing need for performance in applications such as self-driving cars, next-generation computers, hyper-efficient solar panels or quantum computing set Si to the verge of its fundamental capacities. More and more devices will need to include parts manufactured out of scarce, but fitter materials. Promising candidates for many applications are III-V materials. They are binary, ternary or quaternary compounds of elements from the third and from the fifth period of the periodic table, such as GaAs, GaP, GaN, InAs, InSb, AlAs, $\text{Al}_{1-x}\text{Ga}_x\text{As}$. They exhibit astonishing electronic properties and great potential for outperforming Si in many domains such as infrared and/or terahertz detection [178], high-mobility transistors[37, 31], topological superconductors [169, 152, 157] and high-yield

Chapter 1. Motivation and Context

photovoltaics [210, 139, 235]. They have the potential for improving the lives of billions of people, as the 2014 Nobel prize to Isamu Akasaki, Hiroshi Amano and Shuji Nakamura for the invention of the GaN-based blue LED shows it[1].

Nonetheless, most of III-V materials are composed of scarce elements. Indium for example makes up for less than 0.00003% of the earth's crust. As an estimate, it represents the volume of lake Ontario on the totality of the earth's crust volume. The annual worldwide volume production is around 1300 Tonnes[153], and demand grows fast. Therefore, it is vital to use III-V element's minimum required amount and integrate it on Si as a platform. This poses significant challenges, which arise from the fact that trying to associate two materials of very different natures is not straightforward : their atomic spacings, their preferred structure arrangements, their electronic properties will often be incompatible, leading to defects, cracks, dislocations or recombination centers that will deteriorate greatly the device performance.

This "association", or junction, of two different semiconductor materials is named a heterostructure. Fabricating a III-V on Si heterostructure is not an easy task, as defects will easily form. It is usually accepted that the ideal method would be growing the III-V crystal layer on top of the Si wafer. Crystal growth is the field of producing chemical reactions in a controlled atmosphere for arranging atoms in a desired way. This can be done in a vacuum chamber, where controlled fluxes of vapors elements are sent to the Si surface and chemically react to form the desired binary, ternary or quaternary compound. Temperatures, pressure, vapor fluxes and time can be tuned in order to optimize the growth quality. It is however virtually impossible to obtain a perfectly grown crystal layer, and researchers are always actively looking for ways to improve the crystal quality and reduce costs. The goal is usually to avoid defects in the region of interest, i.e the active region. Strategies consist in accumulating all the defects in a sacrificial layer at the start of the growth (buffer layer growth [204]), some consist in playing on the defects' crystalline orientation (lateral overgrowth[80]). Though the main strategy of interest here is the one theorized and reported in 1986 by Luryi and Suhir[155]:

"Our theory predicts that Ge films of arbitrary thickness can be epitaxially grown without dislocations on a Si substrate, provided the latter surface is patterned with pads of half-length of 100\AA , separated by "trenches" [...]. This is probably beyond the reach of any lithography."

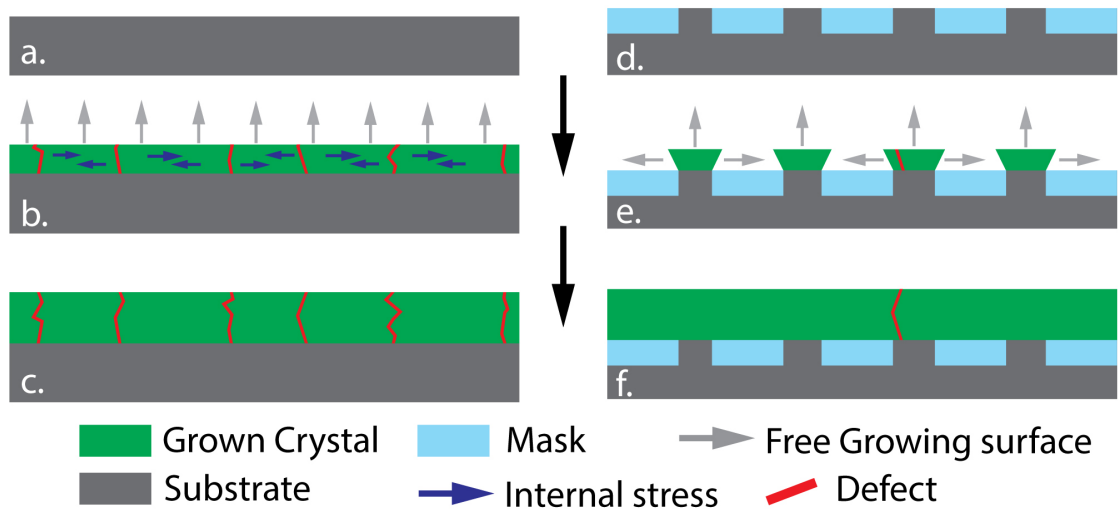


Figure 1.2: Side-by-side comparison of a thin film growth (a. b. and c.) and selective area growth (d. e. and f.). Defects can be largely avoided by the use of a patterned surface as seen in f.

The idea is to reduce the probability of forming a defect by reducing the "nucleating area", or the contact point area between the wafer and the growing crystal. As illustrated in figure 1.2 b., defects would arise from built-up internal stress during growth. This stress comes from the natural difference in crystal size between the two materials : If the top material has a larger crystal, the layer will mostly feel compressive stress. Same goes for a material with a smaller crystal and tensile stress.

Reducing the "nucleating area" serves as a stress reliever as seen in figure 1.2. In fact, considering the thin film can glide on a mask where growth cannot happen, the grown crystals can freely relax along x,y and z. One can choose to continue the growth and making the crystals coalesce forming a uniform layer as shown in subfigure e. The coalescence of individual nuclei can still produce some defects. Stopping it beforehand permits to keep arrays of small, pure crystals as shown in subfigure f. This method is named selective area growth. This can lead to better-performing devices, as defects such as dislocations are heavily detrimental. Luryi and Suhir hypothesized that if the heterostructure contact point was small enough, the formation of defects could even be completely avoided. As the target III-V elements in a circuit are usually small, this would permit to solve many issues : Instead of growing a full crystal layer and carving the desired shapes from it (top-down approach), one could only grow III-Vs where it is needed and not having to carve, touch or damage this precious material (bottom-up approach).

Unfortunately, because of the technological limitations from the 1980s till the early 2000s, large scale patterning of a surface such as seen on figure 1.2 d. at the effective scale was impossible.[146]. However, in the past 25 years, the race for electronic miniaturization stimulated a 40 times improvement in resolution. This paved the way for growing nano-sized objects in a controlled manner, with astonishing electronic and optical properties.

1.3 III-V Nanostructures, and the Promise of Integration

Nanostructures such as nanowires (NWs)[91], nanomembranes (NMs)[223, 70] and nanospades (NSPDs)[92] originate from the idea of reducing the amount of defects and material utilization by growth miniaturization. They are *small* crystals with regular, perfect shapes that expresses their purity. They permit to avoid defects by reducing the contact area between Si substrate and the III-V active area. Nanostructures in general can be fabricated either by etching a thin film or by crystal growth. The first approach is called top-down, and the second one bottom-up. The one we will focus on now is the bottom-up approach, that greatly reduce surface states and still lets room for pattern design. It was shown that bottom-up nanostructures exhibit unique properties that are not possible using bulk materials such as photon and/or phonon confinement [126, 67, 40].

A large part of nanostructures' interest is beyond defect reduction or performance improvement. Studies showed that materials in a nanowire form can adopt crystalline structures that are not stable as bulk. We can cite Wurtzite GaAs NWs[86, 63, 26], but also hexagonal Si [154] and hexagonal Ge[99]. It shows the potential for nanostructures to revolutionize the properties and performance of a given material.

Nanostructure properties have been studied for far longer than the 80s. In fact, one of the first NW report (named whiskers at that time) is from Sears in 1955[200] where condensing vapor materials such as Cu or CdS on a cold surface in vacuum was demonstrated. This work paved the way for the study of Wagner and Ellis in 1964 [232] that truly was the infancy of vapor-phase growth of semiconductor NWs, and as seen in figure 1.3, made room for a plethora of studies experimenting with very different materials : from III-V,II-V or II-VI semiconductors to metals or even oxides.

1.4. Why Scaling-Up is Crucial, and Difficult

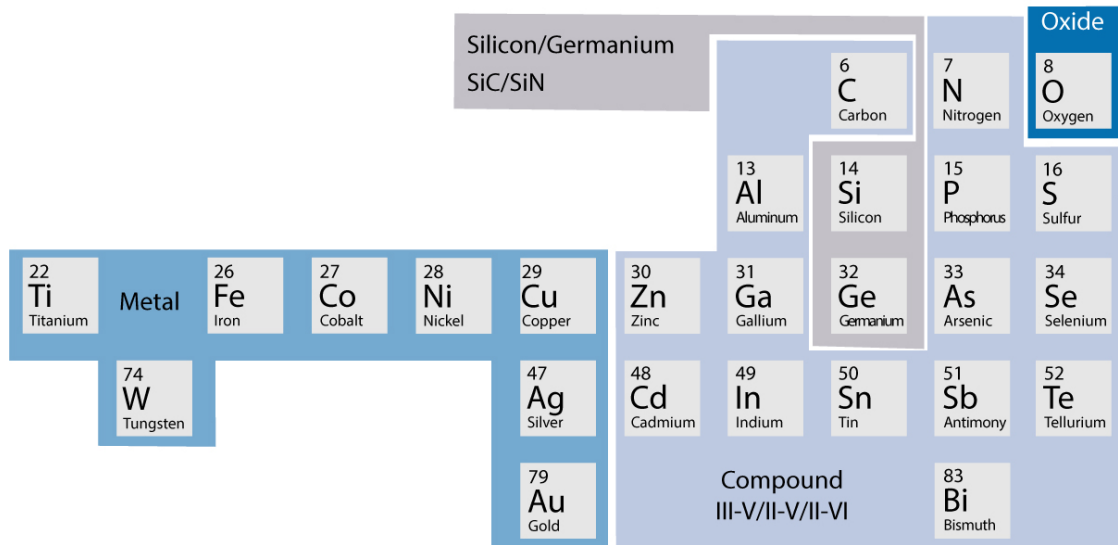


Figure 1.3: An overview of the plethora of materials that can be used for synthesizing NWs by vapor-phase growth.

At first grown randomly on Si and III-V substrates, the development of clean-room technologies such as electron beam lithography or deep ultraviolet (DUV) stepper lithography now permit to localize and control with *great* precision the formation of these structures. The community is currently capable of producing precise and pure arrays of III-V NWs on Si [183, 196] that open great perspectives in domains such as optoelectronics or photovoltaics.

However, until now, the semiconductor industry has had troubles integrating vapor-phase nanostructures into functional devices or concrete large scale projects. They are currently more seen as a curiosity than a real industrial opportunity. This is because the nanostructure community currently faces challenges that are hindering its expansion. In the following chapter we will introduce those challenges, and how we are planning to tackle them.

1.4 Why Scaling-Up is Crucial, and Difficult

III-V NWs usually grow vertically along the $\langle 111 \rangle$ crystalline orientation, which is not the $\langle 100 \rangle$ direction industry standards for Si wafers. This means that NWs will spontaneously grow in a misoriented manner on (100). Using these arrays in electronic or optoelectronic devices becomes extremely challenging. Now, even considering that we can use (111) Si wafers for devices, the time needed

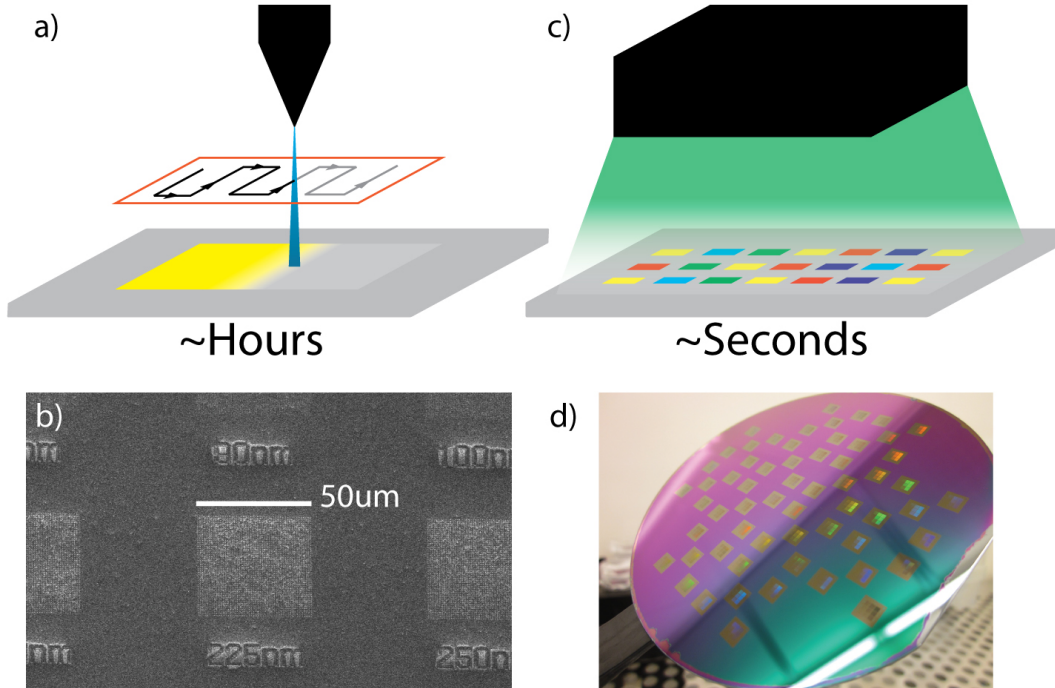


Figure 1.4: a. A schematic representation of EBL showing the direct writing of a micron-scaled array. b. SEM image of a nanopillar array fabricated using EBL. c. A schematic representation of DUV stepper lithography showing a simultaneous exposure of multiple mm-scaled array. d. Photography of macroscopic nanopillars arrays on a 100mm Si wafer fabricated using an ASML PAS 5500/350C DUV stepper lithography.

for fabricating cm-scale arrays is still orders of magnitude too high to be economically viable. This is because the main method used for patterning wafers is electron beam lithography (EBL), which exposure time increases dramatically with exposed area, even taking several days for a single wafer[5]. Techniques such as nano-imprint lithography[115, 170] can rapidly fabricate large-scale arrays using a patterned stamp and an imprinted polymer layer. However this is only proven on the short term, and its stability and robustness for industrial applications still needs to be assessed. Lastly, we also show that doping remains hardly understood in bottom-up nanosystems[127] given the difficulty of accessing such small concentrations in such small objects. What are the roles of the different dopant incorporation pathways, or how large is the impact of surface states and/or dopant accumulations remain largely open questions. Fortunately, with the improvement of characterization techniques such as cathodoluminescence (CL) [28], atom probe tomography (APT)[95], Raman spectroscopy [58] or photolumi-

1.4. Why Scaling-Up is Crucial, and Difficult

nescence [8] it becomes more and more possible to access single NW doping profiles.

In this section we have identified three key elements that make the field of bottom-up nanostructuring so challenging : The Si wafer crystalline orientation, the patterning method and the doping. These are problematic in almost every application as they involve practicality, scalability and control. In this thesis, we will be interested in trying to solve these key elements in given systems and open perspectives for bottom-up nanostructures in industrial applications such as solar cells, quantum computing and photonics. We will focus on the case of III-Vs on Si and propose ideas for pushing the field forward from the technological perspective.

2 Scientific Foundations

In this chapter we will go through the scientific background that is needed to properly assess this thesis work. We will start with glimpses of theoretical concepts that will introduce experimental notions used in our scientific articles.

2.1 Crystals

Crystals are commonly known to exist in minerals (quartz, salt), jewellery (diamond, sapphire, ruby) or science fiction (infinity stones, kyber crystal, sakuradite). In the collective thinking they refer to rare, symmetric and pure materials with unique properties.

Reality is not as far. A crystal can be simply defined as an ordered arrangement of atoms. Thanks to this order, Crystalline materials usually exhibit better and/or unique electrical, optical or mechanical properties compared to their semi-crystalline or non-crystalline (amorphous) counterparts. Many organic, metallic and semiconductor elements exist in crystalline phases and can occur naturally or are intentionally fabricated. We will delve into what defines a crystal, its defects and see relevant examples for this work.

2.1.1 Periodicities and Sizes

A crystal is a periodic repetition of a base pattern. Therefore, defining a particular crystal requires :

- A lattice : This is defined by non-coplanar vectors (two for 2D materials

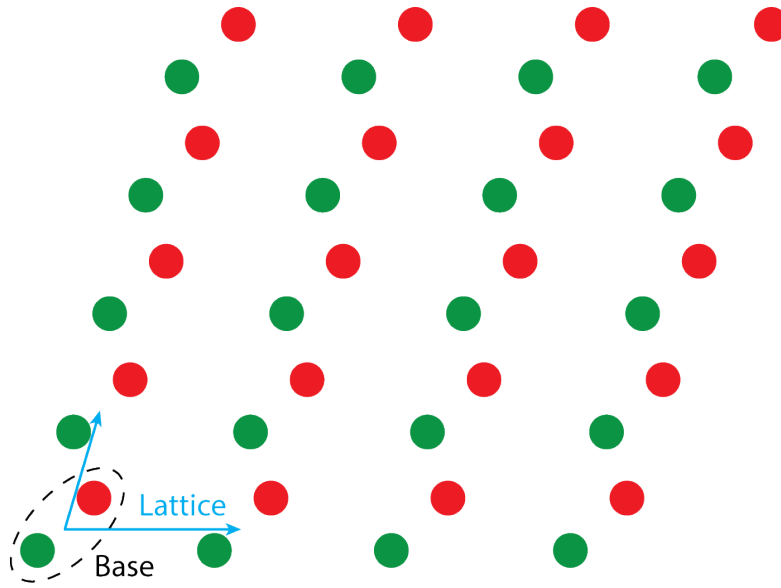


Figure 2.1: Simplified representation of a 2D lattice with a bi-atomic base pattern. The (semi)-infinite repetition of these two atoms forms the 2D crystal. Adapted from [89]

and three for 3D materials) that together form the fundamental translation vectors. The infinite linear combinations of these vectors form the lattice called Bravais lattice. The set of all points R is then defined as :

$$R = n_1v_1 + n_2v_2 + n_3v_3$$

where n_1, n_2, n_3 are any integer and v_1, v_2, v_3 the fundamental translation vectors. There are multiple ways of defining the translation vectors for one lattice. A set of translation vectors forms a repeatable volume in space called the unit cell.

- A base pattern: Every point of the Bravais lattice can correspond to one **or more** atoms. As examples, many metals have simple base patterns with one atom (Austenite, Aluminum) but the earth-abundant semiconductor Zn_3P_2 has a base pattern of 40 atoms [209].

All the possible Bravais lattices are classified with respect of their degree of symmetry, from the cubic to the triclinic system. III-V semiconductors and Si are usually adopting simple and highly symmetrical crystal phases from the cubic or hexagonal system. Their base pattern is also usually simple, formed by either one or two atoms. In the sub-chapter "Crystal Structure Cheat Sheet", the major structures of interest for this work will be introduced.

By their ordered nature, crystals will tend to exhibit anisotropic behaviors, from mechanical to growing properties. All directions and planes are not equivalent as they can possess different atomic densities and inter-atomic distances. Visualizing it can be done by the following analogy : imagine cutting a "pièce montée de nougatine" as seen in figure 2.2 with a very sharp knife. Depending on the cutting angle, one might end-up with more or less dense slices. It is even possible to argue that the densest slice would be a horizontal cut, permitting to eat an entire nougatine layer. This is in fact completely correct : These nougatines are stacked in what is named an hexagonal closed-packed (hcp) structure. The pièce montée layers are the densest possible arrangement of spheres : This concept can be applied to atoms as well, as will be seen in the section "Crystal Structure Cheat Sheet".

For understanding nanostructures growth directions or Si wafer processing, it is crucial to identify the different crystalline planes. The next section will introduce an indexing method permitting a clear identification of every direction or plane in a given lattice.



Figure 2.2: Photography of a pièce montée, certainly prepared for a wedding. source : Gelin Traiteur on Facebook.

2.1.2 Miller Index : Planes and Directions

Starting from a unit cell of a given crystal defined by the three translational vectors v_1, v_2, v_3 . This set forms a coordinate system where any vector can be represented as $\sum a_i v_i$. Directions will then be indexed by the integer coordinates a_i of the smallest vector parallel to this direction. As an example, in a cubic system the

Chapter 2. Scientific Foundations

direction crossing the cube from one vertex to the opposite one will be indexed $[111]$.

Indexing a plane is done by first assessing the coordinate of intersections with the axes formed by v_i . Then the reciprocal values of these coordinates are expanded to the smallest set of integers. As an example, in a cubic system, the plane that intersects the axes in $(2,3,1)$ which reciprocal values forms the set $(\frac{1}{2}, \frac{1}{3}, 1)$ will be indexed by the set of values $(3,2,6)$.

For both directions and planes, these indexes are called Miller indices and are denominated by the letters h, k and l . Figure 2.3 shows the most important crystal planes of a cubic system and their Miller indices.

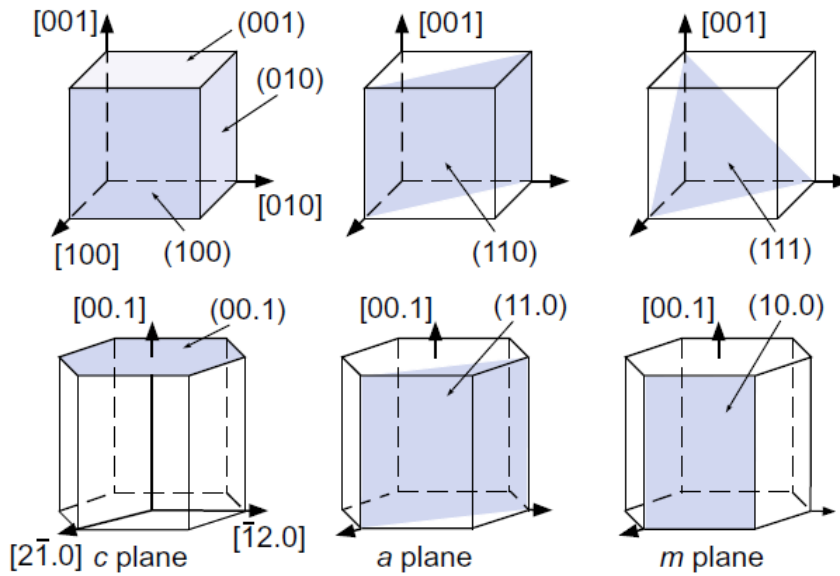


Figure 2.3: Schematic of the most important crystal planes in a cubic lattice. Adapted from [185].

The possibilities for associating atoms in Bravais lattices is virtually endless, and it is needless to say providing an exhaustive list goes beyond the scope of this work. In the following subsection we will cover the most important crystals for III-V and Si nanostructures.

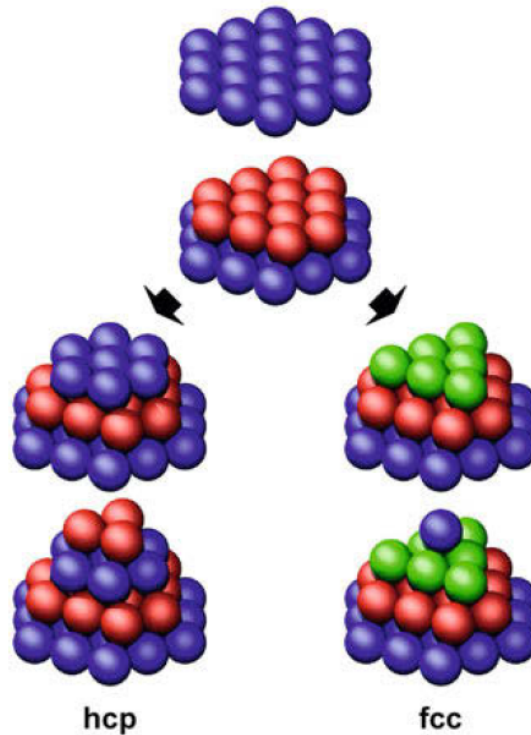


Figure 2.4: Visual representation of the hcp and fcc lattices as closed-packed structures. Adapted from [89].

2.1.3 Crystal Structures Cheat Sheet

Momentarily coming back to the "pièce montée de nougatine" seen in figure 2.2. The nougatine layers are stacked in a hcp manner. There are two ways of stacking nougatine/atoms in the densest manner. They both use layers of spheres aligned in an hexagonal manner as seen in figure 2.4. The first one, hcp, consists in consecutive bi-layers (ABABAB...) that corresponds to the (0001) planes of an hexagonal Bravais lattice, and the second one, fcc, consists in consecutive tri-layers (ABCABCABC...) that corresponds to the (111) planes of a face-centered cubic lattice. They both possess a fill-factor of 74% and are sometimes referred as gliding planes. In fact, every layer being the densest possible, if the crystal would be mechanically deformed, it would require a minimum amount of energy for a layer to "glide" on top of another. The serie of layers (ABC or AB) can then be altered and introduce non-periodic layers called stacking faults. As an example in the hcp ABABCBABA... layer C has glided and locally introduces a defect.

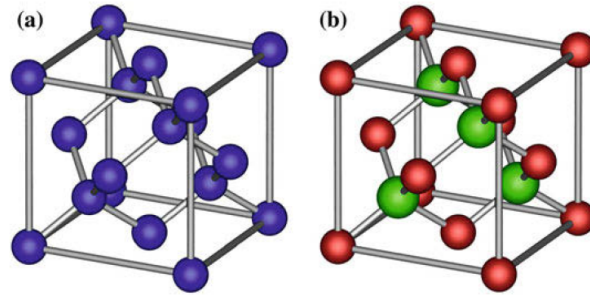


Figure 2.5: Visual representation of the diamond structure in a) and the zincblende structure in b). For obtaining the zincblende structure, one simply needs to change one of the base atoms of a) by an atom of a different element. Adapted from [89].

Diamond Structure

Si occurs naturally in what is called the diamond structure. It is a face-centered cubic Bravais lattice with a bi-atomic base pattern at (000) and $(1/4, 1/4, 1/4)a$. Each atom has a tetrahedral coordination. It is possible to recognize the ABC-type stacking in the $[111]$ direction of the crystal, as seen in subfigure 2.5 a). In subfigure 2.5 b) it is possible to observe the zincblende structure.

Zincblende

Zincblende (ZB) structure is a face-centered cubic Bravais lattice with a bi-atomic base pattern at (000) and $(1/4, 1/4, 1/4)a$. The only difference with the diamond structure is that the base pattern is formed by atoms of different elements. It is the most-occurring crystal structure of GaAs, InAs, AlGaAs, InP or GaP. This crystal is a polar crystal, meaning not all directions of a same family are equivalent : They differ in sequence of the bi-atoms. For example, direction GaAs $\langle 111 \rangle$ will therefore correspond to dense planes of Ga, then As... whereas $\langle -1-1-1 \rangle$ will correspond to As, then Ga... repeatedly. The first is called B-polar direction and the latter A-polar.

Wurtzite

Wurtzite (WZ) structure is an hcp lattice with a bi-atomic base pattern. The base pattern is formed by atoms of different elements. The $[0001]$ distance between layers differs from the "ideal" hcp value and is about $(1.6)a$. It is possible to recognize the AB-type stacking in the $[0001]$ direction of the crystal, as seen in subfigure 2.6 b). Like ZB, WZ is a polar structure.

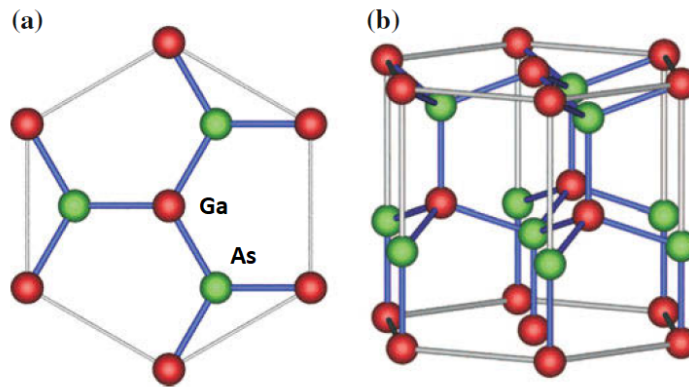


Figure 2.6: Visual representation of the wurtzite structure. Adapted from [89].

2.1.4 Defects in crystals

The symmetry of a crystal can quickly be altered and/or broken by a defect. The latest can be a simple local defect called a point defect, a one-dimensional mismatched atom line called a dislocation or it can be a two-dimensional gliding plane as seen in section 2.1.3. We will present here the defects of interest concerning the study of Si and III-V semiconductors.

Dislocation

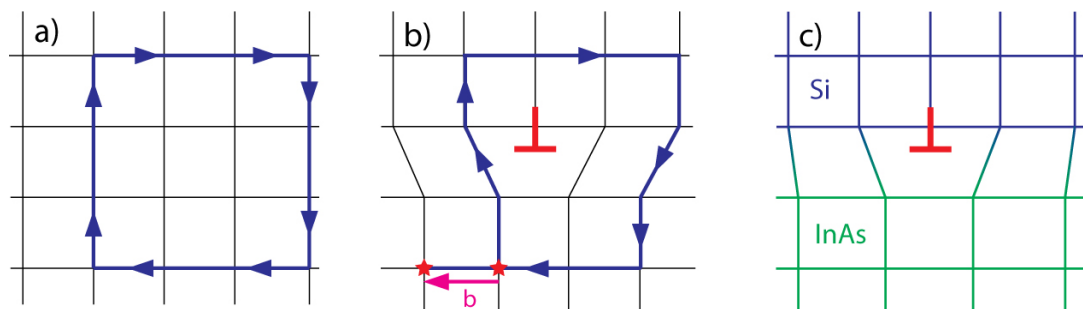


Figure 2.7: Visual representation of an edge dislocation. a) shows a closed loop in a regular lattice, and b) shows the same loop around an edge dislocation. The difference between the beginning and the end of the former loop (represented by stars) is the Burger's vector b . c) shows a misfit dislocation at an interface between InAs and Si.

A dislocation is a line defect along which the crystal is shifted by a certain amount. This shift is usually quantified by comparing a closed loop in the crystal and around the dislocation : The difference vector between those two loops is called a Burger's vector. Dislocation that has their Burger's vector being a translation vector of

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the lattice are named full dislocations. The ones that has their Burger's vector not being a translation vector of the lattice are named partial dislocations. The one represented in subfigure 2.7 b) is a full dislocation called edge dislocation. It corresponds to an insertion of a semi-infinite plane of atoms represented by the red edge symbol.

By adding a semi-infinite plane of atoms, edge dislocations can be very convenient to accommodate for differences in atom spacings. In fact, considering a large lattice crystal such as InAs connecting with a crystal such as Si, dislocations will appear as Si dangling half-planes. This is visible in subfigure 2.7 c) where the top part is the lower lattice constant, in this case Si, and the bottom part is the higher lattice constant, in this case InAs. These dislocations are named misfit dislocations and will spontaneously form at a heterointerface if the lattice constant of both materials is different enough.

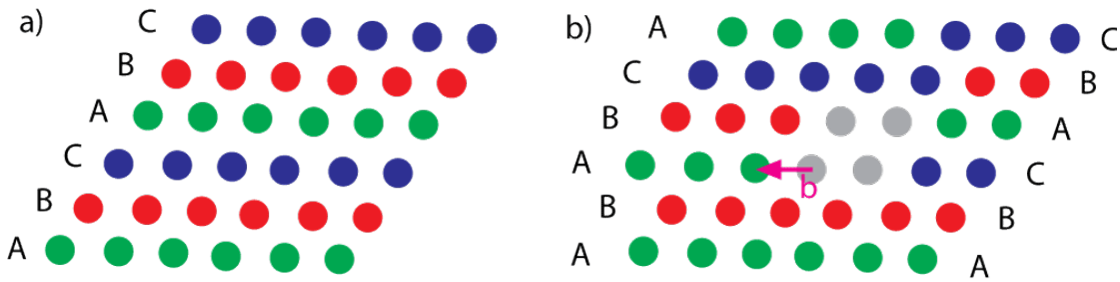


Figure 2.8: Visual representation of a Schockley partial dislocation. The ABC... stacking turns into a ABA... stacking at the left of the dislocation. Burger's vector $b = (a_0/6) \langle 112 \rangle$ is visible.

Partial dislocations are of particular interest in III-Vs, and more precisely the Schockley partial with a burger's vector $b = (a_0/6) \langle 112 \rangle$ and the Franck partial with $b = (a_0/3) \langle 111 \rangle$. It is energetically favorable for a full dislocation to dissociate into two partial ones, therefore it is frequent to observe the formation of Schockley partial dislocations in GaAs or InAs nanostructures. They correspond to a shift in position of a 6th of a lattice parameter for an atom of the dense (111) plane, as seen in figure 2.8. This can locally change the sequence ABCABC... to ABAB... and if the (111) plane is of finite size (hundreds of nanometers), the schokley dislocations will propagate and form a stacking fault.

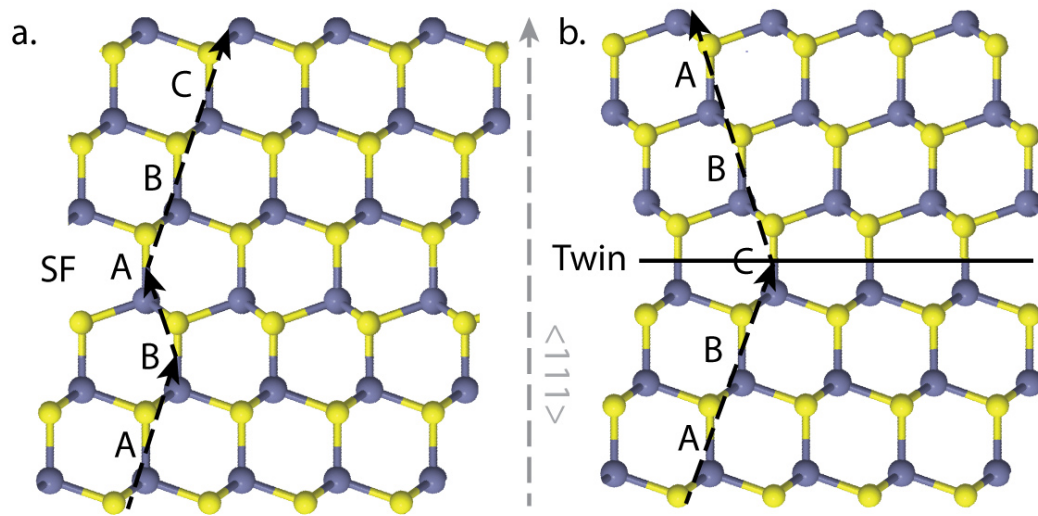


Figure 2.9: Visualization of a stacking fault (a.) and a twin boundary (b.) in a zincblende crystal.

Stacking Faults and Twinning

Stacking faults are the insertion of a faulty layer in the ABC... stacking of a zincblende crystal, leading to a local order of ABCABABCA... They arise from Shockley partial dislocations that propagate along the (111) plane and reach the end surface of the crystal. They are very common in nanowires given their short cross-section and how energetically favourable it is for the dislocation to relax its internal stress on a free surface. A visual of it can be seen on figure 2.9 a.

Twinning is, like stacking faults, a 2-dimensional defect with the dominating plane of the (111) type, but differs in its crystal alteration. Twinning is a mirror or a rotation symmetry plane in a crystal. In III-Vs such as GaAs and InAs it will be a (111) rotation plane transforming a ABCABC... sequence into a CBACBA... sequence. This twin is called an orthotwin and corresponds to a 60° rotation around the orthogonal direction of the twin plane. A visual of it can be seen on figure 2.9 b.

Polytypism

In systems such as GaAs or InAs, the energy difference between zincblende and wurtzite is small, and this difference decreases further in quasi-one dimensional structures like nanowires (cite glas). It is therefore common to encounter wires exhibiting both phases and mixed zones that, in the short range, exhibit neither of the two pure phases [185]. This effect is named polytypism and exhibits non-trivial

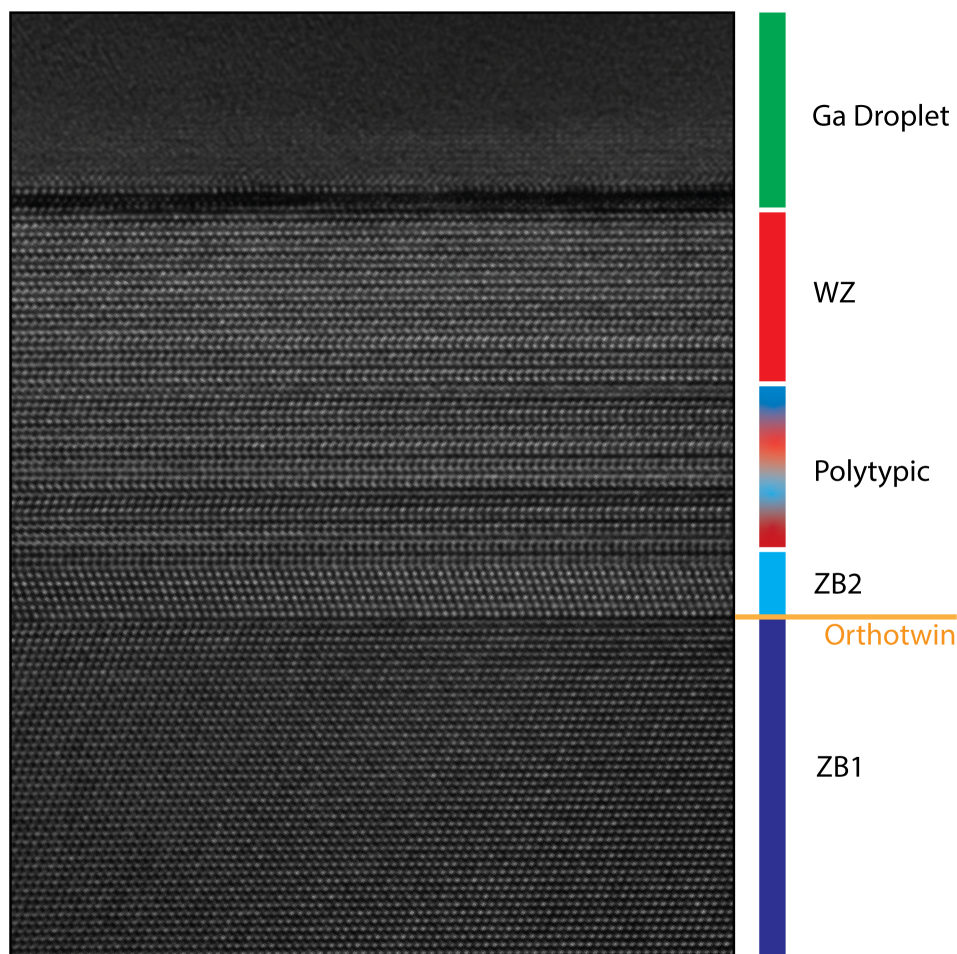


Figure 2.10: High resolution transmission electron microscopy image showing defects that can be found in GaAs nanowires : an orthotwin in the blue ZB zone and a polytypic region before a WZ zone.

sequences of the A,B and C layers. In figure 2.10 it is possible to see a polytypic region in a GaAs nanowire : from the ABCABC... stacking of the zincblende region to the ABAB... stacking of the wurtzite one lies a mixed region that is characteristic of polytypic behavior.

Anti-phase Domains

The last defect we will cover in this section is one of the most historically relevant in III-V integration on Si : Anti-phase domains.

Anti-phase domains are regions in a polar crystal where atoms are located on regular sites but in opposite orders with respect to the rest of the crystal. Therefore, the material exhibits a momentary change in polarity through an anti-phase domain. The consequence of such a domain is a bonding between atoms of the same element at its boundary : for example an As-As or Ga-Ga bonding in ZB GaAs. These boundaries are named anti-phase boundaries and are largely detrimental for any device performance.

Anti-phase domains are very common at heterointerfaces between a non-polar substrate, usually Si, and a polar grown crystal, for example III-Vs. As not all sites in GaAs are equivalent, a monoatomic step on the Si substrate will create a shift in the epitaxially-grown GaAs layer, creating anti-phase boundaries as illustrated in figure 2.11. This has been historically preventing high-quality growths of III-Vs uniform thin films on Si.

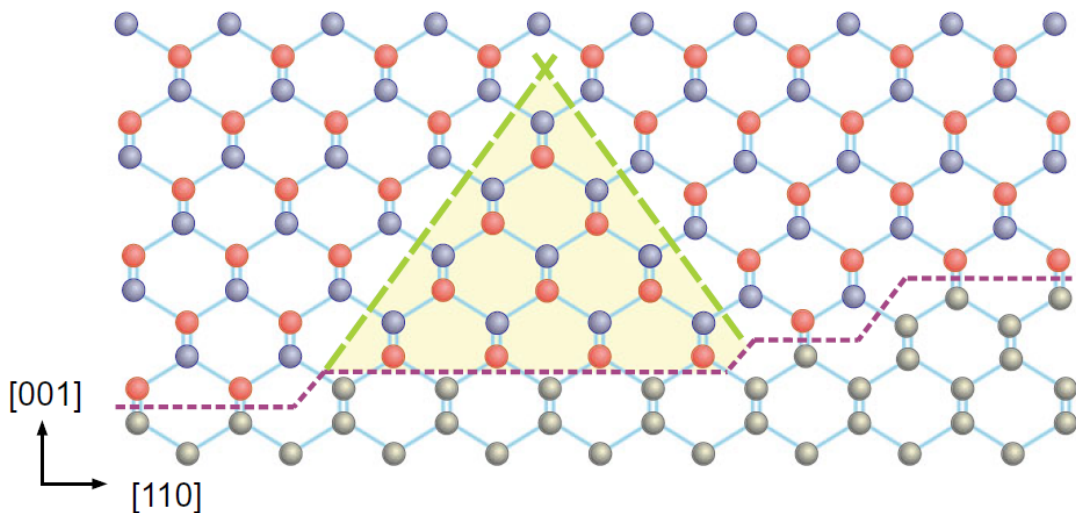


Figure 2.11: Visualization of an anti-phase domain at the boundary between a non-polar and a polar ZB material. The green dashed line shows the anti-phase boundary, being a blue-blue atomic junction.

Crystallography permits to understand materials' internal structures, their mechanical properties and the defects one needs to avoid for having a high-performance device. Nevertheless, it is crucial to understand what are the performances one is targeting, and more specifically what makes semiconductor materials so unique in an application perspective. In the next chapter we will cover their main properties and specificities.

2.2 III-V Semiconductors and Si

Semiconductors' general characteristic is that they lie between the highly-conducting metallic materials and the insulators. To gain a deeper understanding of their electrical and optical behaviours, we need to delve into their electronic structure. The next section will cover the general assessment for energy band calculations and their practical meanings, and I strongly encourage neophytes to the field to refer to more detailed and thorough calculations as seen in [89, 128].

2.2.1 Energy bands : Mind the Gap

Atoms in a crystal can be seen as an electrical potential for electrons that travel in this crystal. A Bravais lattice being periodic, as seen in section 2.1, it is safe to assume that the potential of a crystal will be periodic. It is represented by :

$$U(r) = U(r + R) \quad (2.1)$$

U being the potential, r being the position and R being the lattice periodicity of the crystal. The wave-function Ψ of an electron in a periodic potential satisfies the following Schrödinger equation :

$$H\Psi(r) = \left[-\frac{\hbar^2}{2m}\Delta^2 + U(r) \right] \Psi(r) = E\Psi(r) \quad (2.2)$$

U being the same as (2.1), $-\frac{\hbar^2}{2m}\Delta^2$ being the free electron kinetic energy and E the eigenfunctions of Ψ that corresponds to the energy dispersion of the electron. This equation represents, in a way, all the possible wave-functions and energies that an electron can adopt in a crystal of periodic potential U. We are therefore looking for solutions to this equation.

Bloch's theorem stipulates that the solution to this equation has the following form :

$$\Psi_{nk}(r) = A \exp(ikr) u_{nk}(r) \quad (2.3)$$

A being a normalization constant, n being a quantum number, k being the wave vector and $u_{nk}(r)$ the Bloch function periodic with the lattice. n and k are the indexing numbers of the wave-function $\Psi_{nk}(r)$. This expression remains hard to solve and requires approximations in order to extract energy dispersions for different materials. The simpler approximation is the free electron approximation, setting the periodic potential U to zero (i.e ignoring the effect of the lattice). This gives the following energy dispersion :

$$E(k) = \frac{\hbar^2}{2m} k^2 \quad (2.4)$$

This dispersion is unsurprisingly continuous given that it represents the allowed energies of an electron in free space. In order to assess the effect of a lattice on the energy dispersion, it is necessary to introduce a non-zero function for U. One of the simpler approximation that can be done in 1D is the Kronig-Penney model that models the potential U as a square periodic function of finite height U_0 . Solving this equation leads to the following solution :

$$\cos(ka) = \beta \frac{\sin(Ka)}{Ka} + \cos(Ka) \quad (2.5)$$

Where k is the wave-vector, a the potential well width, β the named "coupling strength" that represents the strength of the lattice potential barrier, and $E(K) = \frac{\hbar^2}{2m} K^2$ the energies for the electron to adopt in this one-dimensional crystal. Therefore, by choosing any energy E_i and computing the right-hand term, applying \arccos to the expression gives the corresponding solutions for the electron wave-vector k. However, choosing values of E where the right-hand term is greater than 1 or smaller than -1 yields **no solution** for k. This means that certain energies corresponds to no electron state in this crystal.

Figure 2.12 shows the free electron energy dispersion (equation 2.4) in red dashed

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line and the computed solutions of equation (2.5) with a coupling strength of 20 in blue filled line. The free electron relation shows a continuous dispersion with all energies yielding at least one solution for k . The Kronig-Penney model however shows energies yielding no solutions, as highlighted by the red band. This band is usually named **band gap**, and physically represents forbidden energies in the crystal that electrons can not adopt. In the case of a semiconductor, this band contains the Fermi level of the crystal, i.e the thermodynamic work to add one electron to the crystal. Therefore, the band gap separates the band highlighted in green, called **valence band** representing states of electrons bound to the crystal, and the band highlighted in blue called **conduction band** representing higher-energy electrons that can move in the crystal. The smaller jump from one band to another can be centered around 0 in k -space like subfigure 2.12 a. We then speak about a direct band gap. However this is only the case for certain semiconductors like GaAs, InAs, GaN or GeSn with Sn concentrations exceeding 15%[81]. Sometimes the transition from one band to another, i.e the dip of the conduction parabola and the tip of the valence parabola, will not be aligned in k -space and electrons will require an additional change in momentum in order to access the conduction band. We then speak about an indirect band gap. Materials such as Si, Ge and GaP possess an indirect band gap. The Kronig-Penney model however remains a rather simplified method for demonstrating the band gap existence, and much more accurate methods are used such as the empirical-pseudopotential method[27].

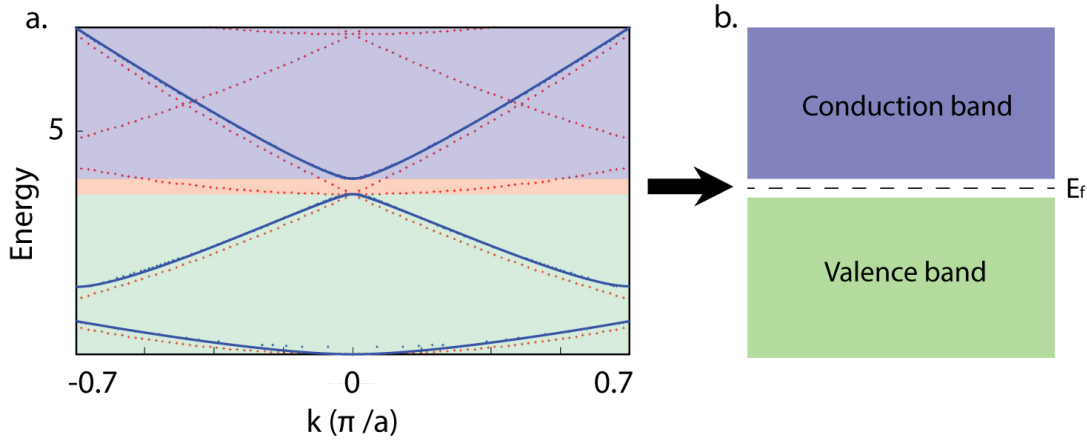


Figure 2.12: In a. : computing of the solutions for the free electron energy dispersion (red dashed line) and the Kronig-Penney model energy dispersion (blue line). In b. : schematic of the resulting band diagram for a semiconductor with the Fermi level E_f highlighted in the band gap.

In order to access the conduction band, electrons in the semiconductor must over-

come the energy barrier that constitutes the band gap. This can be done by thermal (energy coming from heat), optical (absorption of a photon) or electronic (interaction with a high-energy electron) excitation. Once in the conduction band, the electron (negatively-charged) leaves behind, in the valence band, a vacancy named hole. This hole is considered positively-charged. At low temperatures, the Coulomb interaction between the electron and the hole becomes significant and binds both "particles" together. This electron-hole pair is called an exciton. At higher temperatures, the excitonic effect is negligible and electrons populating the conduction band are considered "free electrons". These are able to move in the lattice and carry an electrical charge. A material becomes conductive when enough "free" electrons are generated in the lattice.

Conductivity depends on the quantity of free electrons in the conduction band, but also on how efficiently can electrons travel in the crystal. The following section will define how to quantify and characterize conductivity in a semiconductor.

2.2.2 Conductivity and Mobility

In the previous section we discussed about optical and electronic excitations in order to populate the conduction band. These methods, being a momentary excitation, usually lead to an unstable situation where the electron will rapidly release this excess of energy and recombine back in the valence band. The case of thermal activation is however different. If the temperature of the material is stable and high enough, even with fast recombination rates, electrons will keep being activated and populate the conduction band at equilibrium.

In the case of an intrinsic semiconductor, the amount of electron in the conduction band can be defined by the following expression :

$$n_e = \int_{E_c}^{\infty} D_e(E) f_e(E) dE \quad (2.6)$$

Where E_c is the conduction band's lowest energy level, $D_e(E)$ the density of state (DOS) of every energy level E in the conduction band and $f_e(E)$ the Fermi-Dirac distribution defined as :

$$f_e(E) = \frac{1}{\exp(\frac{E-E_F}{kT}) + 1} \quad (2.7)$$

Where E_F is the Fermi energy level, k is the Boltzmann constant and T the temperature of the system.

It is therefore possible to apprehend that the higher the temperature of the system is and the higher the amount of electrons accessing the conduction band is. Therefore the conductivity of an intrinsic semiconductor will increase with temperature, as seen in the very first figure presented in this thesis (1.1). Nevertheless, this is not the full story, as temperature usually brings agitation in a system and electrical scattering. The full behavior of conductivity can then be defined by the product of the carrier concentration n_e , the carried charge q and the semiconductors carrier mobility μ representing the system's scattering :

$$\sigma = qn\mu \quad (2.8)$$

Equation (2.8) shows that intrinsic semiconductor's conductivity is impacted by several factors and can have complex behaviors with temperature : for example increasing until a certain point by carrier concentration increase (n_e), but then decreasing by increased thermal scattering (μ).

Improving σ by increasing T appears as a double-edged sword. Scientist were fast to discover that playing with the term $(E - E_F)$ in equation (2.7), i.e the location of the Fermi level, can improve the conductivity more efficiently. This can be done by doping the semiconductor and is presented in the next subsection.

2.2.3 Doping

Doping is the action of voluntarily introducing foreign elements at a very low concentration for altering the electrical properties of a material. Doping elements are only constituting around 1/100th to 1/1000000th of the atoms in a semiconductor, but they tremendously impact the Fermi level, carrier concentration and band

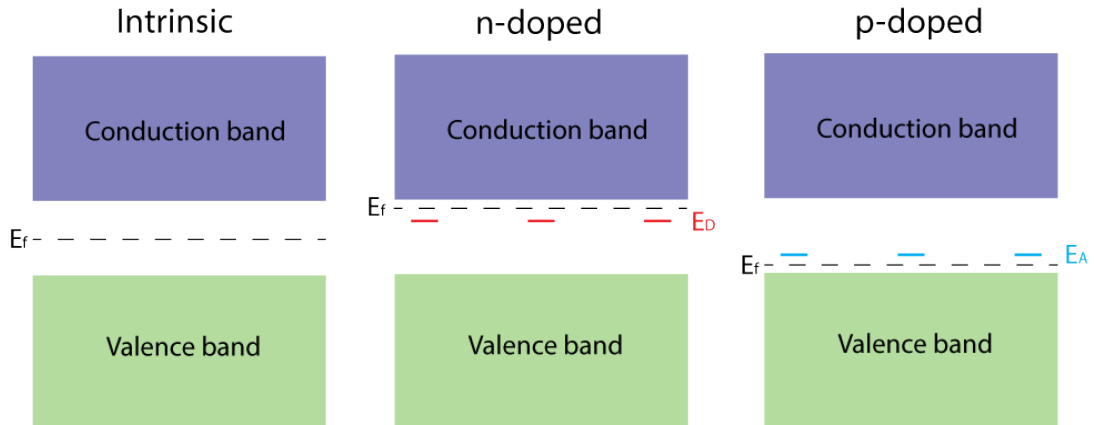


Figure 2.13: Schematic of an intrinsic, a n-doped and p-doped semiconductor. The Fermi energy E_f is consequently shifted closer or further from the conduction band depending on the donor energy level E_D or the acceptor energy level E_A .

structure. In fact, they can introduce energy levels within the band gap that, if close to the conduction band, can create free electrons easily (donors), or if close to the valence band, can capture electrons easily and create a hole (acceptors). Semiconductors doped with donors are named n-doped and semiconductors doped with acceptors are named p-doped.

The Fermi level will then move closer (n-doped) or further (p-doped) from the conduction band depending on which impurities are introduced. A semiconductor will then see a drastic increase of charge carrier concentration : negative electrons for n-doped and positive holes for p-doped. From there, the carriers in higher concentration will be called majority carriers and the other one minority carriers.

A concrete example is the p-doping of Si by Boron introduction in a simplistic view : to satisfy the tetrahedral bonds of the Si diamond lattice, B needs an extra electron and will take it from a neighbouring Si atom. This will create an electron vacancy in the lattice i.e a hole. The n-doping of Si by Phosphorous works in the same fashion : to satisfy the tetrahedral bonds, P needs to give away one electron and will give it to the neighbouring Si atoms, creating a negative supplementary charge called free electron.

In III-V semiconductors, certain impurities are named amphoteric : depending on which group element they replace they will either act as a donor or an acceptor.

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This is the case for Si in GaAs : If Si replaces As it will act as an acceptor, and if it replaces Ga it will act as a donor. One can influence the Si behavior in GaAs by playing with the crystal growth temperature or the Si incorporation method[27].

We now understand the separate behaviour of an intrinsic, a n-doped and a p-doped semiconductor. We saw that n-doped crystals possess a majority of free electrons and that p-doped crystal possess a majority of holes. Now, what makes semiconductor technology so exciting relies in this next (and last) sub-section : The act of combining semiconductors with different doping concentrations and nature, i.e junctions.

2.2.4 Junctions

The art of combining can very much be related with the art of creating. When put together, different semiconductors permit to exhibit unique and exciting properties such as photoabsorption, photogeneration, diodic effect, seebeck effect among others. In this subsection we will briefly present junctions between semiconductors of different dopings or/and different natures.

Homojunction

Homojunctions are a junction of two semiconducting crystals from the same materials, but with different dopings. More specifically, the junction between a n-doped and a p-doped semiconductor is named a pn homojunction. When put together, the excess electron on one side and excess hole in the other side will tend to diffuse and try to equilibrate their concentrations in each side. However this diffusion of charges will, locally at the interface, create a depletion of electron in the n-doped side and a depletion of holes in the p-doped side. This region is usually called the depletion region.

Because of the charge diffusion, there will be the appearance of a resisting electric field from the n-doped to the p-doped side. These two opposite forces, i.e diffusion force and electric force, reaches a steady state that naturally fixes a certain depletion width. The electric field is the key interest of a pn junction because it fundamentally acts in opposite manners for electrons and holes. For example it permits to, upon exciton generation, to overcome Coulomb interaction and separate the charge carriers. They can then be used separately, like in a photovoltaic panel.

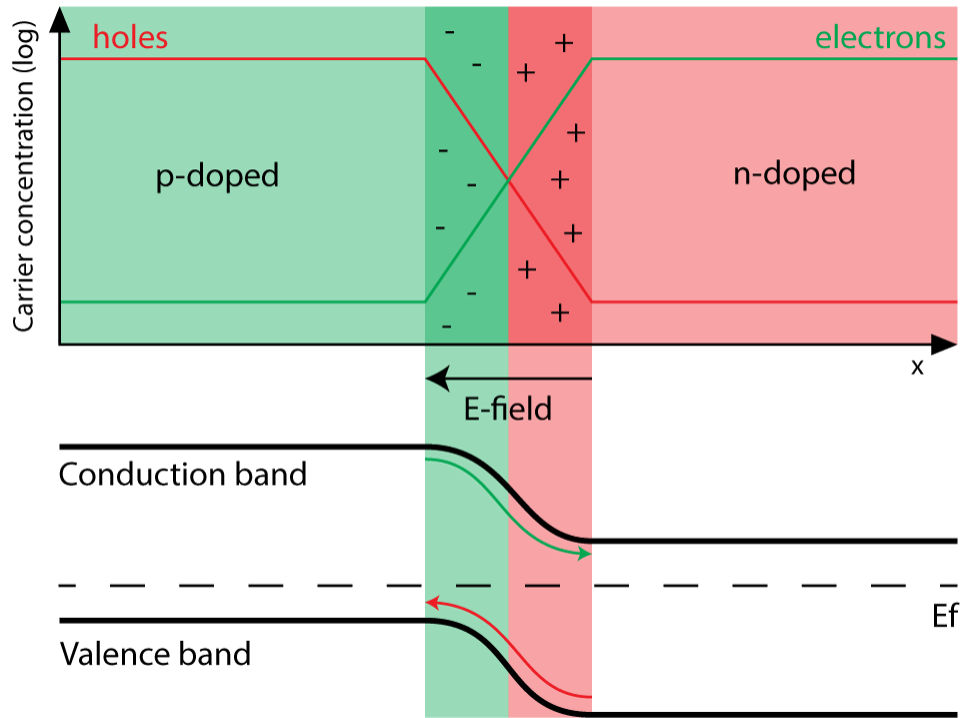


Figure 2.14: Schematic of a pn junction.

The pn junction can also be represented in a band diagram as band bending. This is due to the Fermi level equilibrating across the whole junction. Figure 2.14 shows a schematic representation of a pn junction, from electron and hole concentration in each side of the depletion region to the resulting band diagram. The curved red and green arrows represents accordingly the drift path of the holes and the electrons upon carrier generation.

Heterojunction

A heterojunction is a junction between two semiconductors having different band structures. By this definition we can link the concept of heterostructure and heterojunction : although they mostly are analogous, we need to make the distinction in the case of different crystal structures of the same elements having different band structures. This is the case for ZB and WZ GaAs, that is a heterojunction but not a heterostructure.

Due to differences in band gaps and electron affinities (work function of a semiconductor), a heterojunction can exhibit different band alignments as shown in figure

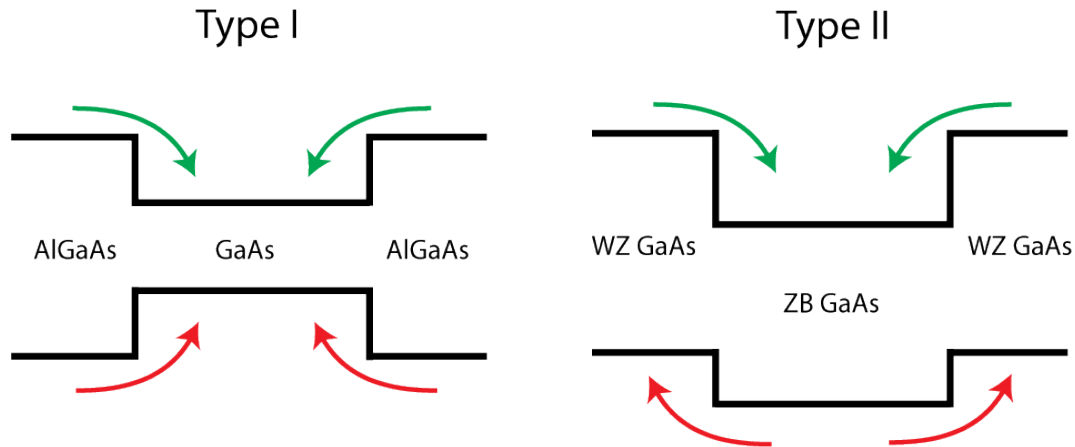


Figure 2.15: Schematics of type I and type II band alignment in a heterojunction. Green arrow represents electron diffusion and red represents hole diffusion.

2.15. Type I is usually seen for GaAs/AlGaAs or GaAs/InAs and type II for Si and Ge, or ZB and WZ GaAs. It is possible to observe that the type I band alignment looks similar to a periodic potential in a crystal as described in section 2.2.1. In fact, when done in nano-dimensions, type I heterojunctions can exhibit similar properties than an atom in a crystal. In the "well" created by the difference in band gaps, we can observe quantum confinement. This can be used as a building block for a plethora of quantum structures such as multiple quantum wells, superlattices, quantum dots and quantum wires. These structure will be further discussed in the "Nanostructures" section.

Materials with such unique and interesting properties must have interesting and unique fabrication methods. In the next section, we will explore the field of epitaxy, and more specifically the field of semiconductor epitaxial growth by molecular beam epitaxy.

2.3 Vapor Phase Epitaxy

As mentioned in chapter 1, semiconductor materials and more specifically III-Vs are scarce and it is crucial, for an industrial perspective, to master their integration on Si. We saw that there are two main strategies for doing so : Top-down and bottom-up. In this section we will solely focus on bottom-up and discuss the driving forces and challenges for the growth of III-V crystals onto Si.

2.3.1 What Makes a Crystal Grow (Fundamentals of Epitaxial Growth)

Crystal growth, even if present in our everyday life, stays a fascinating transformation of matter. In a reality where it is far more easy to destroy a card castle than building one, how does nature find the driving force for arranging millions of atoms by itself, and how does the process take place ? Answering those two questions requires the use of both thermodynamics and kinetics.

Thermodynamics

Thermodynamics is the macroscopic study of matter and energy transfers. It permits to describe atoms' collective behaviours when a steady state is reached, i.e after enough time that properties such as temperature or pressure can be attributed to the whole system. It is a study that leaves time to matter.

If one does not interact with a system, i.e not providing nor taking any energy, it will eventually reach a steady-state where global statistics remains unchanged in time. We call this state equilibrium. The internal energy of a system under equilibrium can be described as :

$$U(S, V, \{n_i\}) = TS - PV + \sum_{i=1}^{N_c} \mu_i n_i \quad (2.9)$$

Where U is the total internal energy of a system, T is the temperature, S is the entropy, P is the pressure, V is the volume, μ_i is the chemical potential of component i , N_c the total number of components and n the total number of moles in the system. The variables S, V, U and n_i are referred as extensive parameters, meaning their value depends on the system size. The variables T, P and μ_i are referred as intensive parameters, meaning their value does not depend on the system size.

Growing a crystal implies that humans will act on the system and provide a driving force for its change of state. This means making the desired phase more thermodynamically stable than the original phase. For doing so, the grower can choose between acting on the extensive parameters or the intensive ones. Practically, it is easier to change the temperature and/or pressure of a system :

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temperature can be adjusted by heating/cooling down and pressure can be adjusted by putting the system under vacuum. As we can see in equation (2.9), U takes mainly extensive parameters as variables, therefore we need to introduce a new state function G named Gibbs free energy, defined as :

$$G(T, P, \{n_i\}) = U - TS + PV \quad (2.10)$$

That takes intensive parameters T and P as variables. Gibbs free energy can also be written as :

$$G = \sum_{i=1}^{N_c} \mu_i n_i \quad (2.11)$$

Where it is visible that G depends directly from the chemical potentials of every component. If the system contains several phases, G total is a sum of all the phases' Gibbs free energies.

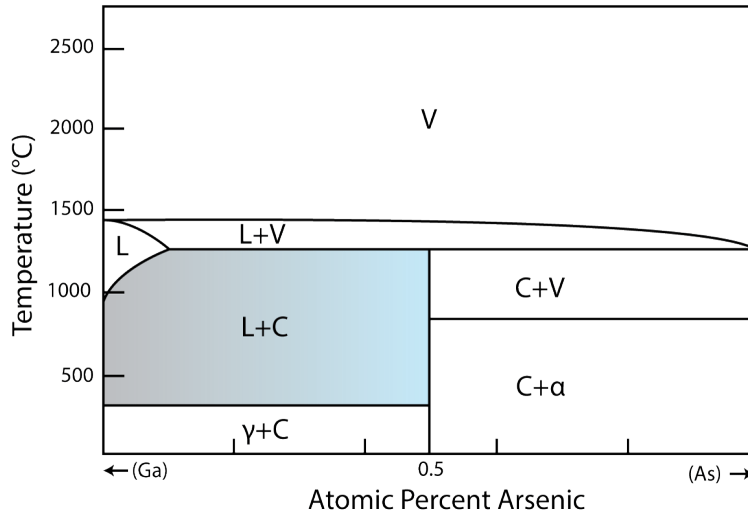


Figure 2.16: GaAs phase diagram at 10^{-1} Torr. Adapted from [220].

The goal of a system will then be to minimize its Gibbs free energy, and the goal of the grower is to make this minimization happen through a phase change, usually

from vapor to solid. The driving force for crystallization will be provided by controlling pressure and temperature such that the chemical potential of the target phase is lower than the initial phase.

The study of Gibbs free energies as a function of temperature, pressure and composition permits to build diagrams showing the stable phases at a certain temperature, pressure and composition. These diagrams are named phase diagrams and are crucial for many fields of material science, including metallurgy and ceramics. Image 2.16 shows the Ga-As binary phase diagram at low pressure, and highlighted a temperature/pressure zone that shows both liquid Ga and solid GaAs at equilibrium. This zone is intimately linked with self-catalyzed GaAs nanowire growth : in fact, as long as the system is in Ga-rich condition (less than 50% As) and in the right process window, A liquid Ga catalyst droplet and a solid GaAs nanowire can be at equilibrium. Further details about GaAs self-catalyzed VLS growth can be found in section 2.4.1.

Crystal are, by nature, anisotropic. As seen in section 2.1 atomic planes possess different surface energies and reaching equilibrium for a nuclei/3D crystal means finding the combination of planes in space reaching an energy minimum. This combination is named equilibrium crystal shape (ECS). This process can be expressed by the use of Gibbs free energy :

$$G_s = \sum_i \gamma_i A_i \quad (2.12)$$

Where G_s is the surface Gibbs free energy, γ_i is the surface energy density and A_i the area of facet i . The ECS is the shape that minimizes G_s . Consequently, low-energy facets will tend to have higher surface area and high-energy facets suppressed to a geometrical minimum. This expression can be combined with Wulff's hypothesis : at thermodynamic equilibrium, the surface energy density of a facet depends on its distance to the crystal center [245, 214]. This permits to compute the ECS by a Wulff construction.

In 2D at a given volume, the Wulff construction is a (r, ϕ) polar representation where $r = \gamma_i$, and ϕ is the orientation angle of the given plane i . The center of

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the polar representation is called the Wulff point and is located within the bulk of the crystal. Once γ_i is resolved, the ECS is given by the inner tangent lines of the polar plot. This construction places high surface energy density orientations farther from the crystal, decreasing their relative surface area. Respectively it places low surface energy density orientation closer from the crystal, increasing their relative surface area. This can be seen in figure 2.17 a. where an example of a Wulff construction can be seen. Extended to 3D, this permits to compute the ECS of a crystallite like the GaAs ECS seen on figure 2.17 b. Because surface energy density also depends on the environment, this ECS corresponds to an As-rich environment and zero temperature.

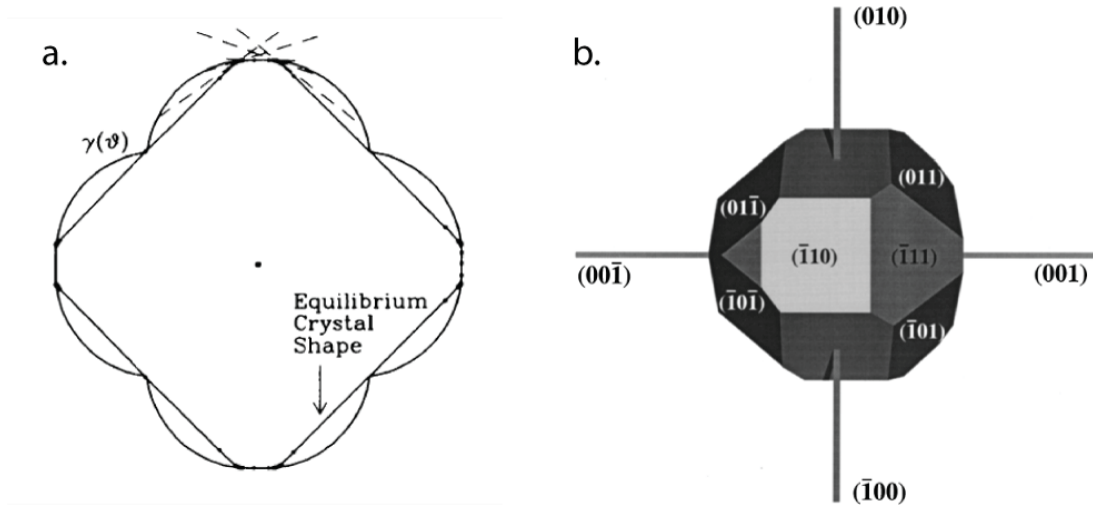


Figure 2.17: a. Wulff construction of a 2D crystal at a fixed volume. Taken from [220] b. ECS of 3D GaAs under As-rich atmosphere, computed by Wulff construction. Taken from [167]

Crystallization will happen through attachment of particles, i.e atoms or molecules, to a surface. However for a correct attachment, there is a minimum size of nuclei called critical size that is needed on the surface. This effect can be explained by the following expression :

$$\Delta G_N = \Delta G_S + \Delta G_V \quad (2.13)$$

ΔG_N being the total Gibbs free energy of the crystal nucleation, ΔG_S being the contribution of the nuclei surface and ΔG_V being the contribution of the nuclei

2.3. Vapor Phase Epitaxy

volume. ΔG_V is usually favorable to the nuclei expansion, but ΔG_S is usually positive. In fact, surfaces are usually energetically expensive to create, and for an small-enough volume ΔG_S will remain the main contribution. The critical size represents the size from which ΔG_V becomes the main contribution and nucleation becomes thermodynamically favourable.

Now focusing on 2D-layers, When critical size is reached, the growth of the new crystal phase can adopt different modes that are presented in figure 2.18. The dominant mode is adopted following Young's equation :

$$\gamma_{as} = \gamma_{ns} + \gamma_{an} \cos(\Theta) \quad (2.14)$$

Where γ_{as} is the interface energy between the ambient and the substrate, γ_{ns} between the news phase and the substrate, γ_{an} between the ambient and the new phase, and Θ the contact angle between both phases. A Frank-Van de Merve mode, i.e layer-by-layer mode, is adopted if the contact angle is close to zero, i.e γ_{as} exceeds $\gamma_{ns} + \gamma_{an}$. The Volmer-Weber mode, i.e island growth, is adopted if the contact angle is close to 180deg, i.e γ_{ns} exceeds $\gamma_{as} + \gamma_{an}$. The Stranski-Krastanow mode, i.e mixed growth, is adopted when at first $\gamma_{as} > \gamma_{ns} + \gamma_{an}$, but after a few monolayers γ_{ns} increases and the relation $\gamma_{ns} > \gamma_{as} + \gamma_{an}$. This is often encountered by strain accumulation in the grown layer, for example in a heterostructure.

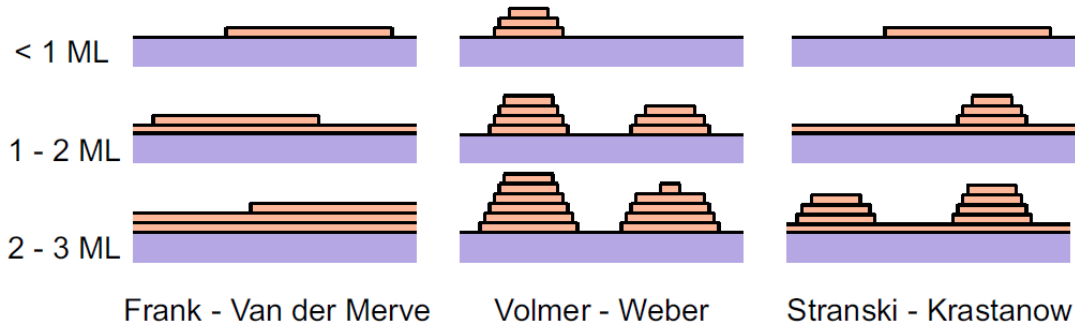


Figure 2.18: Representation of the different growth regimes. Left the layer-by-layer mode, usually desired for thin films. Center the island mode, and right the "mixed" mode. Adapted from [185].

It is observed that the system always wants to minimize surface energy. Nevertheless, questions remain open, such as how do atoms overcome the nucleation barrier

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and reach critical size, and how do atoms attach to the surface. These questions can be answered by studying the kinetics of thin film growth.

Kinetics

In vapor-phase epitaxy, growths usually happen far from equilibrium in short time scales, which make thermodynamics impractical. Processes are affected by energy barriers and by how well atoms can diffuse. The study of kinetics permits to understand at an atomic level the several incorporation mechanisms that precursors can adopt.

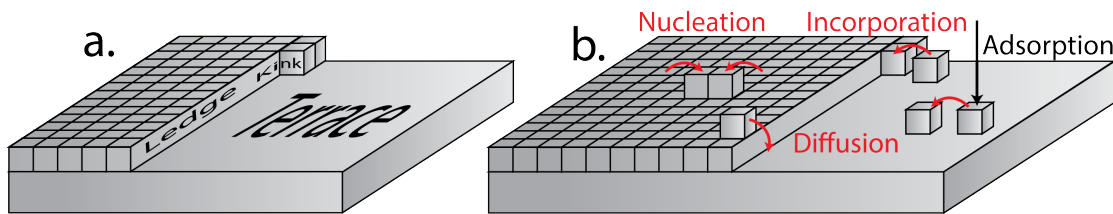


Figure 2.19: Representation of the TLK sites and the atomistic rates processes.

A simple and robust kinetic model is the Kossel crystal which assumes atoms as cubes and only nearest-neighbour interactions. In this model, a forming layer at the surface of the crystal will look like subfigure 2.19 a. It is possible to identify different positions on the surface identified by the number of neighbouring atoms. An embedded atom in the uppermost layer will have four neighbours, leaving only one "dangling" bond. An atom at the edge of this layer, named ledge, has two dangling bond. The atom at the forming row of the uppermost layer, named kink, is of particular importance because it has three neighbours and three dangling bonds. The work required to detach an atom from this kink position is just half the work required to detach one from the bulk, which makes it the position at which crystal growth proceeds. Removing or adding an atom at this site does not impact the total amount of dangling bonds, therefore does not change surface energy.

These three positions in a Kossel crystal and the study of their role in crystal growth is called the TLK (terrace ledge kink) model. In the TLK model the energy of an atom's position is determined by the number of neighbouring atoms. Processes are represented by a number of transient atomic steps that an atom can experience, as seen in subfigure 2.19 b. Atoms arriving at the surface are adsorbed. Depending on temperature and surface energies, they can either rapidly exhibit desorption or diffuse at the surface. Diffusion can lead to nucleation of an

island (island growth mode) or be incorporated to the kink and contribute to the uppermost layer growth.

Using these processes accurately is key for a successful crystal growth. In fact, the principle of selective area growth is the difference of desorption rate between different materials, for example between the mask and the growth area. Nonetheless, such techniques can lie far from equilibrium conditions and the resulting structures can greatly diverge from the predicted ECS using thermodynamics. Kinetic effects such as inclination-dependent exposure to fluxes, adatom diffusion, relative plane growth rates and simultaneous growth modes result in a kinetic crystal shape (KCS). KCS stands as the equivalent of ECS for kinetic considerations only. In reality, a crystal will express more one or the other depending on the growth parameters.

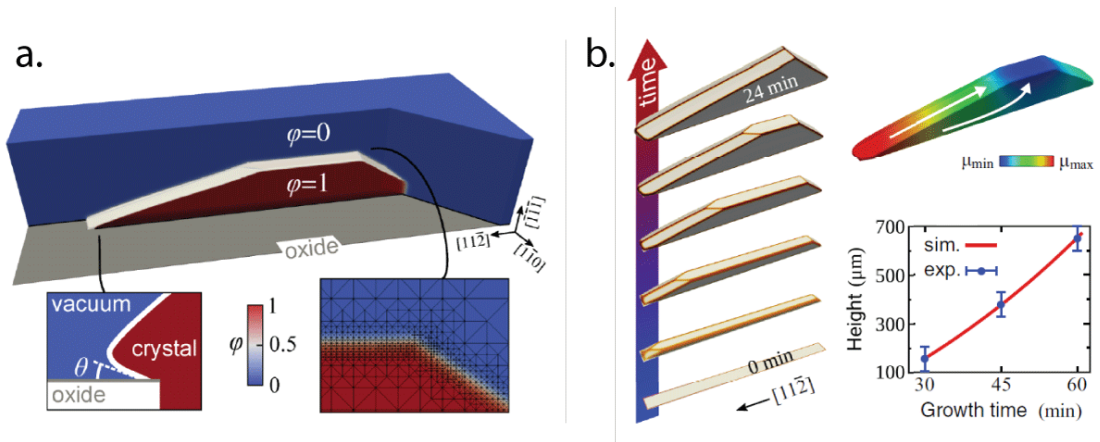


Figure 2.20: a. Representation of the phase-field simulation setup for GaAs nanomembrane growth. b. PF simulation results for vertical nanomembranes : Time evolution, representation of the flow of material and graph comparing nanomembranes heights from experiments and simulation. Taken from [3].

One of the key parameter influencing crystal shape is the precursors deposition rate : Low rates correspond to slower crystal growth and tend to favour thermodynamic effects, whereas high rates tend to favour fast-growing crystal orientations i.e kinetic effects. Catalyst-free selective-area nanowire growth is a direct product of kinetic effects : In fact, $(111)\text{B}$ planes has a high growth rate and grows faster than (110) side walls, leading to crystals elongated in the $\langle 111 \rangle \text{B}$ direction[112]. There are computation methods used to predict KCS. One is the continuum model, developed by J.Cahn and J.Taylor [22] and numerically implemented using the phase-field (PF) approach [148, 189]. Albani et al. [3] uses the PF approach for

describing the crystal shape of GaAs nanoscale membranes grown by selective-area vapor phase epitaxy. In figure 2.20 a. we can see the simulation setup for a vertical nanomembrane (NM): The function φ is named phase field function and defines the facets of the NM as continuous/diffuse interfaces. Outside the crystal φ is equal to zero, and inside equal to 1. As φ is continuous everywhere the surface is defined at the line where φ is equal to 0.5. The time evolution of the phase-field function can then take into account several kinetic factors, depending on the growth parameters. Subfigure 2.20 b. shows simulation results with a time evolution of a GaAs NM growth. The graph visible in the bottom right is a comparison between experimental measures done by SEM and the computed values. It is clear that the PF approach permits to efficiently model the kinetic growth of nanostructures.

Using kinetics efficiently however requires a precise control of the systems temperature and pressures. In the next section we will present the molecular beam epitaxy system used in this work.

2.3.2 Molecular Beam Epitaxy : a Fruitful Void

A molecular beam epitaxy (MBE) system is a vapor-phase epitaxy system that uses ultra-high vacuum and ballistic fluxes of atoms to grow highly pure crystals in a very controlled manner. It comes-up as the most elaborate, most thoughtful and most expensive way of growing semiconductors. Its elegant concept and versatility has made it the reference method for very demanding applications such as quantum computing, space design or high-speed electronics. Although MBE's are complex systems and require very skilled operators and frequent maintenance, they are certainly a thing of beauty and I feel very privileged to have had the chance of working with one during my PhD. In the next sections we will present the main features of an MBE and then introduce our own system.

MBE principles

An MBE operates at ultra-high vacuum (UHV), i.e exhibiting a base pressure of 10^{-10} Torr. For obtaining such pressure, the chamber is first primarily pumped by a mechanical/turbo-pump until 10^{-7} Torr. Afterwards we use the conjunction of two cold-trap pumping methods : two cryo-panels that are nitrogen-cooled, and two cryo-pumps that are helium-cooled. Cryo-pumps reach a steady-state temperature of 14K by adiabatic dilatation of He. He is then passed-through a compressor

2.3. Vapor Phase Epitaxy

that pressurizes the line back, forming a closed-loop. In figure 2.21 it is possible to see a cryo-panel, usually located inside the chamber around the side-walls, and a cryo-pump, usually connected to the chamber.

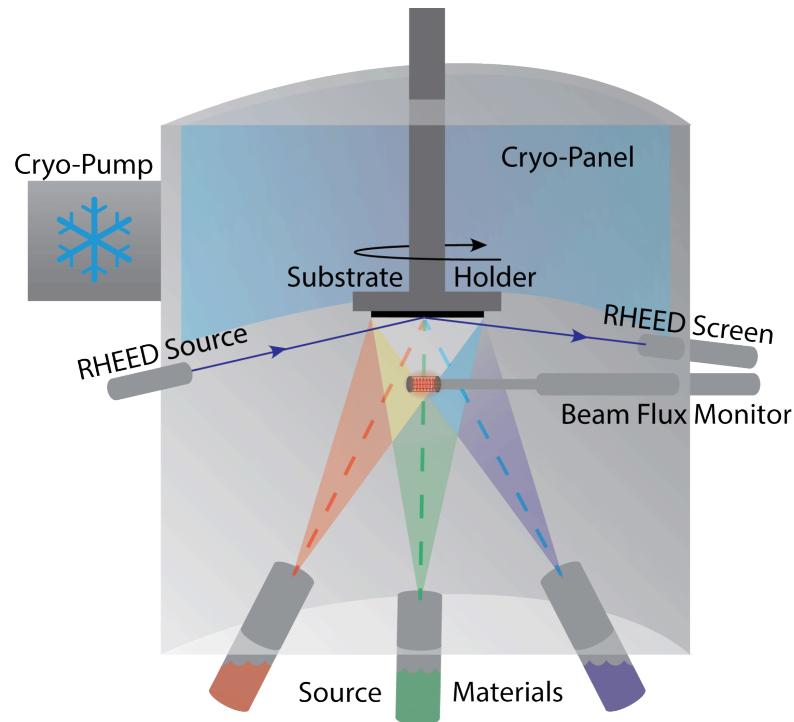


Figure 2.21: Schematic representation of an MBE chamber.

The substrate is positioned on a holder and rotates at 7rpm to ensure an even flux distribution. Heating happens through radiative heat from the backside of the holder and permits to reach up to 900degC. Usual growth temperatures range between 400degC and 650degC.

Source materials are contained by crucibles placed in cells. We can separate the type of cells into three :

- Effusion cells for group III (Ga,In,Al): The material is melted and heated-up until its vapor pressure exceeds the one of the chamber, causing atoms to be vaporized and ejected from the melt. In vacuum the atoms follow a ballistic trajectory until reaching the substrate. The flux is tailored through a change of the melt temperature.
- Cracker valved cells for group V (As,Sb): The material is heated-up until

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its vapor pressure exceeds the one of the chamber, although the material remains solid. Before reaching the chamber, atoms pass through a hot cracker zone (600-900degC) that permits to "crack" the vapor molecules. For As a cracker at 600degC gives As_4 molecules and at 900degC As_2 . The flux is tailored through a needle valve.

- Sublimation cells for doping elements (Si,C): The material is heated-up at 1000degC until sublimation by running a current through them. The flux is doping-level, meaning orders of magnitude lower than the other cells. It is tailored through a change of the current.

Points of references to quantitatively assess the precursor fluxes are obtained through the use of two techniques :

- Beam flux monitor (BFM) : An ion gauge that can be directly placed on top of the substrate. Permits to correlate changes in partial pressure with a change in current between the thermionic emitting filament and the faraday cage. Although fast and easy to implement, BFM measurements only gives relative values and needs a reference calibration. This is obtained through the second technique.
- Reflective high-energy electron diffraction (RHEED) : An electron beam is sent towards the growing crystal surface at a very low incident angle. If tailored properly, the electrons will be in Bragg condition and diffract with the crystal structure. Diffraction intensity is maximized when the growing layer is uniform and minimized when it is partially-formed. By gathering the diffraction pattern on a phosphorous screen and monitoring the pattern's intensity, one can observe oscillations caused by atomic monolayers growth. Extracting the period of these oscillations gives an incredibly precise value of the growth rate. Although long and tedious to implement, RHEED had to be done regularly to confirm BFM flux values.

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Our MBE is a custom-made DCA P600 dual chamber cluster. The different modules can be seen on figure 2.22 and are detailed as follows :

- D1 : First deposition chamber and the one used for this work. Possesses two cryo-pumps Brooks CTI-Cryogenicstm 8 and 10, two cryo-panels, a residual

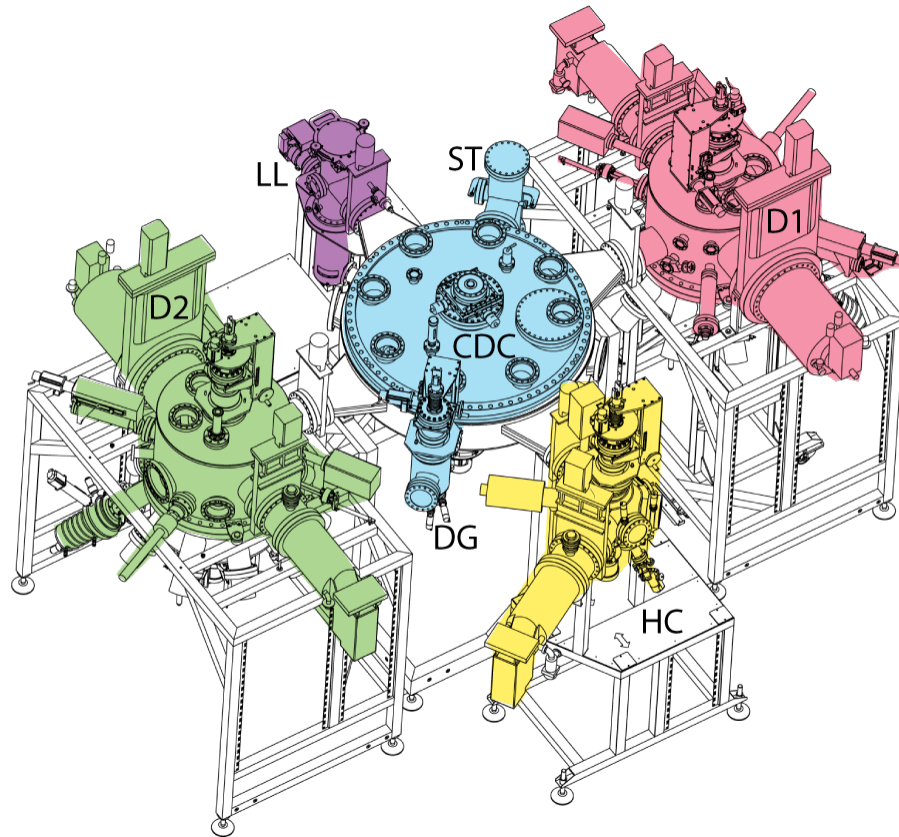


Figure 2.22: Technical drawing of our EPFL MBE cluster.

gas analyser (RGA), a RHEED system and a Pyrometer. Available cells are Ga, In, Al, As, Sb (from Veecotm), C, Si.

- D2 : Second deposition chamber, currently not in use.
- CDC : The central chamber possesses a robot manipulator. Permits to automatically transfer samples from one module to another. Although very appealing on paper, this manipulator causes many transfer issues and loss of holders that fell into D1. Its maintenance have been hectic. CDC also possesses a degassing module (DG) where samples were heated-up to 800degC for four hours before being transferred to D1. CDC also has a storage (ST) module for storing up to eight samples under ultra-high vacuum. Its base pressure is $1,5.10^{-10}$ Torr.
- LL : The load-lock of the cluster. Up to 8 samples can be loaded into it at once. Possesses a turbo-pump. Equipped with halogen lamps that heat-up the samples and cassette up to 120degC, permitting a faster de-hydration

and to reach 5.10^{-8} Torr in about 4 hours.

- HC : Hydrogen cleaning chamber, currently being restored. Have not been used in this work.

All of the modules are separated by VATtm gate valves to avoid cross-contamination.

Now that we detailed the fundamentals of crystal structures, semiconductor properties and vapor-phase epitaxy, we will delve into the characteristics and properties of semiconductor nanostructures, more specifically their growth mechanisms.

2.4 Nanostructures : Why and How

This section was taken from our review article work : Vapor Phase Growth of Semiconductor Nanowires: Key Developments and Open Questions[91].

Nanowires are filamentary crystals with a tailored aspect ratio ranging between few and hundred nanometers. Their particular shape and dimensions render them particularly attractive for a large variety of applications and open new perspectives in many others. Reviews and manuals on the synthesis, applications and properties of nanowires are abundant[51, 173, 60, 211, 42, 100, 191, 106, 149, 134, 195, 47, 7, 216, 241, 246, 12, 10, 140, 116, 142, 49, 144, 111, 77, 145, 247, 194] . An up-to-date overview on the properties and applications can be found in [91].

Among several interesting properties, nanowires offer two key advantages in the form of their excellent material quality and the stunning design freedom associated with their morphology. These characteristics open new possibilities both in the advance of engineering and fundamental science. Historically, the bottom-up growth vapor phase is celebrated for providing the highest degree of materials perfection. Opposed to this, the top down approach can potentially lead to defected surfaces and poor control on the resulting facets, with some exceptions [174, 206]. Several breakthroughs have conferred nanowires the reputation for outstanding functional properties and design/engineering of materials at the nanoscale level.

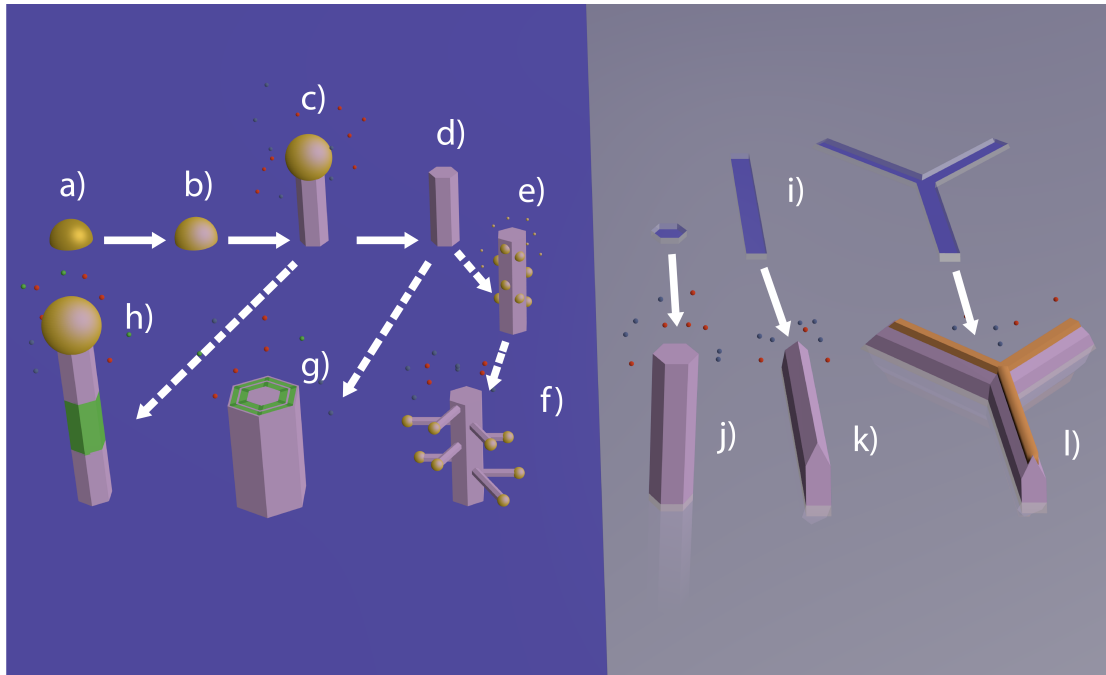


Figure 2.23: An overview of possible nanostructures/heterostructures using VLS and/or VS growth. a) shows the primary catalyst droplet, followed by the formation of a eutectic in b). c) depicts the formation of the stem wire that can be used to produce h) axial heterostructure, or d) by removing the droplet catalyst to produce e) f) branched "tree like" structure or g) radial heterostructure. i) from openings in an oxide mask, one can also produce j) nanowires, k) nanomembranes or l) networks by selective area epitaxy (SAE) growth.

2.4.1 Nanostructures growth methods

VLS and VSS

Historically, the first significant milestone for vapor phase growth of nanowires is the work from Wagner and Ellis on the vapor-liquid-solid mechanism, VLS [232]. For the first time, it was realized that a liquid metal droplet (impurity) can mediate the crystallization of silicon at a lower temperature. Crystallization of Si at low temperatures was achieved by alloying gold with silicon, for which the eutectic temperature is as low as 360°C [47, 212]. Silicon tetrachloride, SiCl_4 , was provided as the vapor phase as a silicon growth precursor. SiCl_4 would decompose at the gold surface at temperature below its pyrolysis. Alternative to SiCl_4 , silane (SiH_4) or pure Si can also be used for VLS growth of silicon nanowires [240, 123, 96]. Silicon would then form an alloy with the gold till it would melt. Upon supersaturation, silicon would precipitate underneath the droplet [119]. The liquid droplet would define both the location of the growth and the lateral size of the nanowire. This

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process is schematically drawn in Figure 2.23 a-c.

VLS has had a major impact in the area of crystal growth, as the main principle can be applied to a broad variety of material systems [82, 84, 251]. Still today, it is probably the most commonly used method for the synthesis of nanowires. The liquid component of VLS plays a central role in the process: not only it provides a nucleation point for the solid nanowire, but it fosters the gathering and in some cases the decomposition of precursors. It is because of the latter that it is often called ‘catalyst’, or ‘physical catalyst’ when it does not lead to a reduction of the activation energy for precursor decomposition. Pioneers like C.M. Lieber, P.D. Yang and L. Samuelson demonstrated that high quality nanowire structures could be obtained by VLS [53, 109, 244, 197]. Their ideas gave birth to a whole new area of research, whose momentum is still increasing today.

What is particularly novel and attractive with the nanowire geometry is that heterostructure formation can occur in three dimensions[103, 39, 9, 156, 124]. Examples of this are depicted in Figure 2.23 h-f. In addition, epitaxy is no longer limited by the condition of lattice-match [85]. In this particular morphology, the strain can relax in a more effective manner, providing the setting for novel heterostructures. Strain relaxation is much more effective for axial than for radial structures [55, 85]. One should also note that in the eventual case that dislocations will form in nanowire heterostructures, they are often of the misfit kind[43]. In addition, they do not significantly affect the functionality of the materials/devices [219, 17]. Finally, one should highlight other design opportunities provided by selective area growth on a patterned substrate, as shown in Figure 2.23 j-l. Here, restricting epitaxy in nanoscale regions of a substrate allows for additional nanowire geometries, junctions and heterostructure formation.

A slight variation of the VLS method consists of the VSS method, standing for vapor-solid-solid[180, 132] . The mechanism mostly identical to VLS, the only difference being that the metal droplet stays solid during the whole process. This results into a bit slower nanowire growth. The main advantage of VSS is the possibility of obtaining sharper heterostructures, potentially down to the monolayer accuracy. Growth precursors tend to be much less soluble in the solid than in the liquid metal. Consequently, the switch of precursors does not result in a significant reservoir effect[132, 180].

This last point brings us to the choice of catalyst for nanowire growth. Au is the most employed method in VLS as it does not oxidize and supports well the decomposition and gathering of many growth precursors. Still, the use of gold is incompatible with CMOS technology. Gold introduced deep traps in silicon and it thus damages the electronic properties at very low concentrations [141, 215] .

Self-Catalyzed VLS

The unsuitability of Au in Si technology has led to the question of what makes a metal a good catalyst for VLS or VSS growth [199, 49]. The following criteria should be taken into account for the choice of the catalyst: i) solubility of the precursor in the metal, ii) solubility of the catalyst in the material to be grown and iii) surface tension of the catalyst. First, indeed the precursor should be to some extent soluble in the metal so that the catalyst can gather it. The thermodynamic phase diagram of the two will determine the temperature range at which VLS and/or VSS can take place. The thermodynamic phase diagram also provides information on the solubility of the growth precursor. CALPHAD has been used to determine the phase diagrams for new systems in which such diagram did not exist [79]. The solubility of the metal in the grown material is also key. A non-zero solubility value leads to incorporation of the metal during growth. Consequently, the size of the catalyst is progressively reduced till it disappears and the grown material is contaminated. Incorporation of the catalyst in the nanowire can lead to damage on the functional properties or doping, depending on the type of levels introduced. As an example, In or Ga have been used for the growth of Si and Ge nanowires. The catalyst was consumed during growth, leading to p-type structures [252, 257, 188] . Subsequent radial growth led to the formation of a pn junction and a nanowire-based solar cell device [30].

Finally, it has been argued that surface tension of the liquid metal is also a fundamental property to consider for successful nanowire growth. It has been suggested that low values should not allow for VLS growth due to the lack of stability[198]. This criterion results from the adaptation of the Young equation describing wetting on planar surfaces. Liquids with low surface tension tend to form flatter droplets, which are not favorable to VLS. One should note here Young's equation should not be applied for the wetting of liquids on non-planar structures such as nanowire tips. Stability of a droplet on a tip cannot be modeled by this equation. In this

configuration, a wide range of wetting angles are possible by just modifying the droplet volume [114, 253] , in principle in contradiction with the wetting on planar surfaces (Ghisalberti *et al.* 2019 Nanotechnology, accepted). Experimentally, low surface tension metals were indeed extensively used for nanowire growth [256, 252, 33] . Surface tension also plays a role in the Gibbs-Thomson effect as it determines the diameter below which precursors are not able to incorporate in the liquid metal, thereby stopping nanowire growth [88, 147].

Alternatively, one can just use an element composing the grown material for VLS. This method is also called self-assisted growth. This kind of growth was already predicted in the seminal work by Wagner and Ellis: ‘an excess of one of the component materials can act as a liquid-forming impurity’[232] , the impurity here taking the role of ‘catalyst’[83]. As an example, Ga or In can be used to assist the growth of GaP, GaAs and InAs respectively [33, 113, 186, 59]. A difference here with traditional VLS and VSS is that the catalyst needs to be continuously refilled, otherwise the axial elongation of the nanowire stops. Also here, the thermodynamic phase diagram acts as a guide to determine the growth parameter space. To illustrate this, one can look at the thermodynamic phase diagram of GaAs [220]. The growth of GaAs and related compounds relies on the thermodynamic equilibrium between the stoichiometric GaAs and the vapor phases Ga and $As_{2/4}$. Thanks to this, the impinging Ga and $As_{2/4}$ fluxes must not contain the exact stoichiometry of the GaAs compound. In thin film growth, an excess $As_{2/4}$ is preferred as this is desorbed; while in self-catalyzed growth the excess Ga stays liquid at the tip of the nanowire [220]. Liquid-phase epitaxy predates the self-catalyzed growth and one has now recognized that mechanism as part of a macroscopic parent. Alternatively, self-catalyzed growth is the nanoscale version of liquid-phase epitaxy.

Among the advantages of self-assisted growth are the high purity, the possibility of varying the catalyst size/volume. In itself, the free-variation of the catalyst volume allows a relatively straight forward path to modify the contact angle and the nanowire diameter. The value of the contact angle has a direct impact on the crystal phase [2] and the regulation of the diameter [33, 56, 126]. The straightforward modification of the catalyst volume also provides obvious means to switch from axial to radial growth and vice versa. Axial elongation can be ceased by complete consumption of the droplet. Further epitaxy results into radial structures [101] . On the other hand, axial growth can be resumed by simply redepositing the catalyst at the nanowire tip [187]. Nonetheless, self-catalyzed method comes with challenges such as the need of a well-balanced precursor’s flux which affects the

steady-state growth but also the crystal phase control.

VS

An alternative path to avoid gold as a catalyst is to simply avoid any metal or intermediate phase. This is often referred as vapor-solid, VS. VS relies on the imbalance in crystal growth velocities, depending on their crystallographic orientation [21, 3]. There are two main approaches to obtain nanowires by VS: in a self-assembled manner and by selective-area-growth, or selective-area-epitaxy (SAG or SAE) on localized areas of a patterned substrate. Direct self-assembly usually relies on a lattice-mismatched substrate where growth does not proceed on a layer-by-layer fashion. It rather starts by islands that then evolve into nanowires [16, 35, 131]. In some studies, it has been claimed that growth starts with a liquid droplet [50, 190, 18]. Typical examples of self-assembled VS-grown nanowires are GaN on sapphire or silicon and InAs on silicon [23, 45, 24, 72, 50]. Both in MBE and MOCVD, VS growth tends to result in a higher number of stacking faults, compared to VLS.

VS can be initiated with a higher yield by the use of a mask. As an example, where a dielectric mask is, we keep an unfavorable nucleation site and remain free of III-V growth under appropriate conditions. Adatoms are able to diffuse through this mask but cannot easily nucleate a droplet or crystallite, they rather desorb. Small openings or pinholes in the mask act as nucleation points for growth. These can be random due to the partial discontinuity of the oxide layer (aka pinholes) or provoked in a deterministic manner by nano-lithography approaches [131, 218, 102, 75, 76, 193]. SAE can be used to achieve freestanding structures but also structures and networks that are solidary with the substrate. Defect-free nanoscale membranes have been achieved by SAE both by metal-organic chemical vapor deposition and molecular beam epitaxy [29, 222]. These membranes can be used as 1D buffer structures for more complex and scalable networks [69]. They can host 1D structures on top, which at the same time can be branched and contacted electronically [69, 138]. Among the advantages of the SAE approach are the deterministic localization of the structures, scalability of the process and a larger freedom in shape engineering to suit a large pool of potential applications while retaining lots of the nanowire features. It opens real perspectives towards mass production of connected nanostructures [175].

Doping

The mastery of the composition in nanowires also apply to doping schemes. The ability to engineer the electrical conductivity through impurity doping is an essential property of semiconductors and thus a necessary step for the implementation of semiconductor nanowire devices. This was recognized early on. Already in the late 90s Hiruma et al provided evidence of doping of GaAs nanowires.[97] Interestingly, the nanowire configuration allows for three-dimensional doping profiles, such as radial p-n junctions [97, 33, 122] . In addition, structures of lower dimensionality such as quantum wires and quantum dots can be added on the nanowire facets to increase the functionality [9, 225, 194, 73, 229]. Finally, the detached nature of nanowires allows for a further extension of the free-standing structures in three dimensions. Nucleation of a second generation of nanowires on the facets results in the formation of branched and/or hierarchical structures, which can be used in applications where a large surface-to-volume ratio is required [48], and electronic devices[213]. This design freedom provided by the nanowire morphology and growth mechanism inspired many materials systems and applications. The easy positioning of the structures via the catalyst on any substrate also opened up new possibilities and the idea of integration with other technologies [11, 160]. Among the achievements allowed by this new design possibility: single electron transistors, Majorana physics, biosensors, quantum dot single photon emitters, light emitting diodes, solar cells etc. . . [136, 258, 54, 14, 71, 122, 250, 129, 169, 46, 213, 184] .

Nevertheless, accessing nanowires and nanostructures properties is not an easy task given their very small footprint. In the next section we will introduce the characterization methods used in this work in order to assess crystal quality and optoelectronic properties.

2.5 Characterization Methods

2.5.1 Electron Microscopy

This section mainly refers to the books by David B. Williams and C.Barry Carter : Transmission Electron Microscopy, A Textbook for Materials Science[243] and to Transmission Electron Microscopy, Electron Techniques by James M. Howe, Brent Fultz and Shu Miao[108]. For a deeper understanding of the mechanisms and theory behind electron microscopy, the reader is invited to refer to these exhaustive

works.

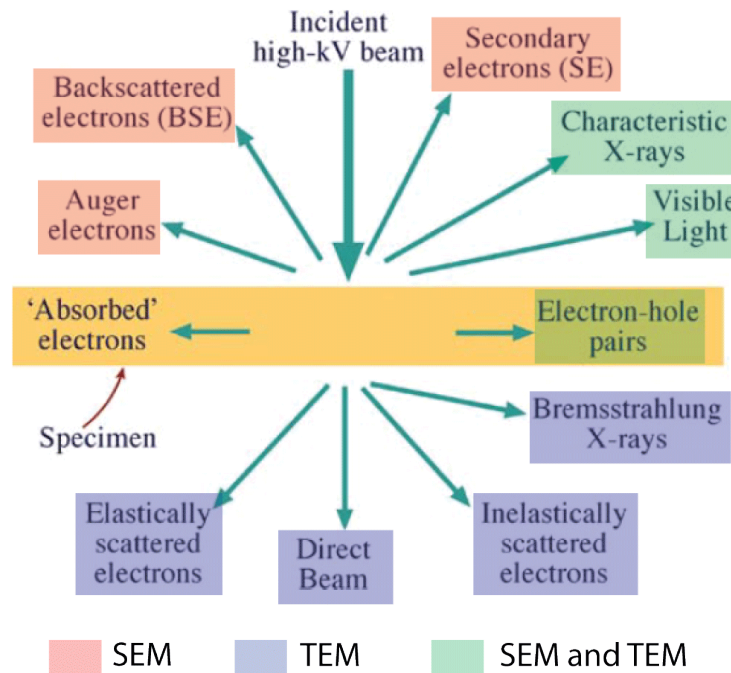


Figure 2.24: An overview of all the possible interactions and resulting signals of electrons with matter. Taken from [243] and adapted.

In order to assess nanostructures structural quality, conventional microscopes do not suffice : In fact, nanowire's feature sizes range from 1 to 300nm, which is below the typical wavelength of light (400-800nm). Electron microscopy uses electrons as primary imaging source and permits to push the resolution past light's diffraction limit. Moreover, electrons interact with matter in a very rich manner and a plethora of resulting signals can be acquired and treated in a meaningful way, as seen in figure 2.24. The two electron microscopy techniques used in this work are presented and linked with the signals of interest presented in the latter figure.

SEM

Scanning electron microscopy (SEM) consists in scanning a conductive sample with a "low-kV" focused electron beam (between 1 and 5kV) and gathering the resulting secondary electrons (SE) and/or backscattered electrons (BSE) for surface imaging. SEM permits to obtain nanostructures images quickly without the need of long sample preparation. The used models are Zeisstm LEO and Zeisstm Merlin both using GEMINItm II columns, which permit to reach a 5nm resolution. In figure 2.25 we can observe nanowires imaged by SEM under a tilting angle of 20 degrees.

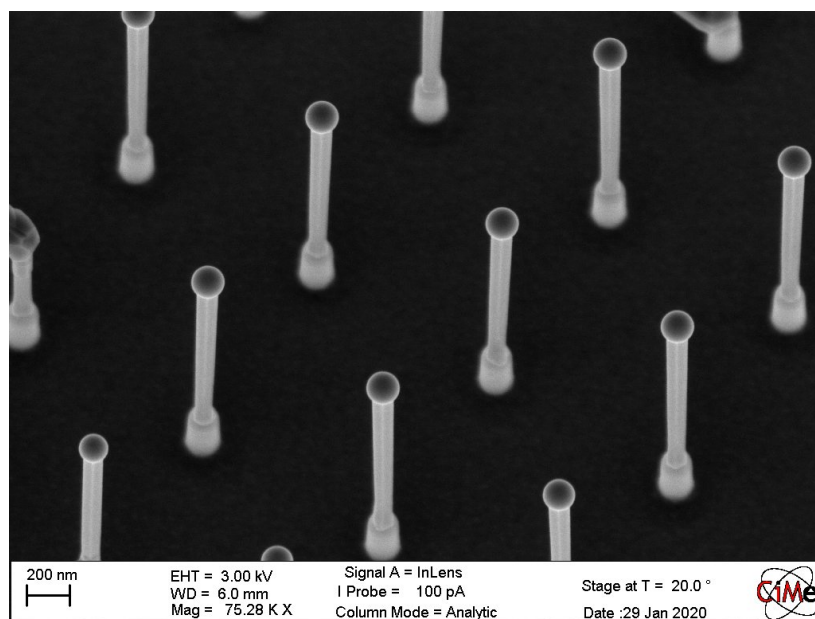


Figure 2.25: SEM Merlin image of GaAs nanowires on top of Si(111) nanopillars. The image caption shows the typical beam energy, tilting angle, and working distance used for SEM imaging.

The conditions visible at the bottom represents the usual imaging conditions used during this work.

In an SEM chamber it is also possible to perform energy-dispersive X-ray spectroscopy (EDX) that permits elemental mapping of the sample surface : In fact, by gathering characteristic X-rays which energy is correlated with the electronic configuration of an atom, it is possible to qualitatively assess elements and phases at the surface of a sample. This is used for a quick and easy mapping and/or contamination identification (usually metals like Cu,Fe,Au coming both common acid baths in clean room)‘.

Nevertheless the main disadvantage of SEMs is its resolution limitation for certain needs such as atomic resolution or crystal defect characterization. For such matter, transmission electron microscopy (TEM) is used.

TEM

TEM consists in sending a much-higher energy beam of electrons, between 30kV to 100kV, and gathering the transmitted signal. In figure 2.24 they belong to the signals highlighted in blue. To do so, the sample needs to be much thinner,

between 100nm and 10 μ m, which requires more preparation than SEM (through ultramicrotomy, focused ion beam (FIB), ion milling or polishing). TEM is also a more sophisticated and hard-to-maintain machine, although it permits to reach higher resolution, down to individual atoms. TEMs can be operated in different modes that are detailed below :

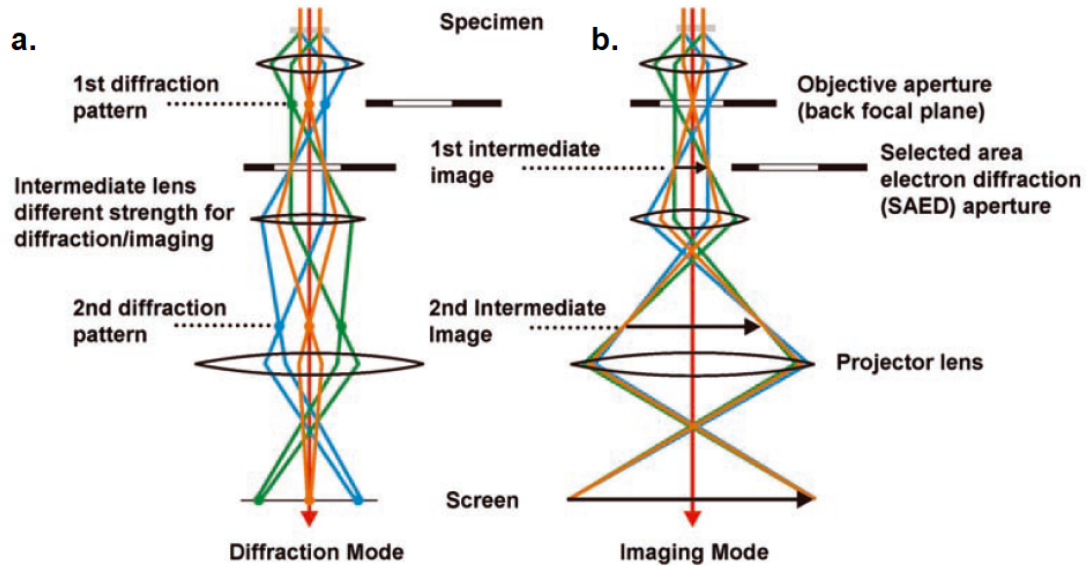


Figure 2.26: Visual schematics of TEM imaging and diffraction mode. Green and blue rays represents the diffracted rays, and orange and red the transmitted rays. Taken from [158].

- **Bright-field/Dark-field imaging** : In imaging mode the intermediate lens will focus the image of the sample onto the CCD, meaning diffracted **and** transmitted rays from a same point are focused on screen. Then, the objective aperture is used : either one can choose to filter-out the diffracted rays. In figure 2.26 b. this corresponds to filtering out the green and blue rays. This mode is named bright-field and will show transmitting regions as highlights and diffracting regions as lowlights. This was primarily used for oxidation characterization of Si nanopillars. Or one can choose to let only one diffracted family of rays through. In figure 2.26 b. this corresponds to filter-out the red, orange and either the green or blue rays. This mode is named dark-field and will uniquely show regions that are diffracting the chosen family of rays as highlights. This was rarely used, except for twinning relations assessment in nanostructures.
- **Diffraction** : The intermediate lens will focus the diffraction pattern on screen, meaning every family of diffracted rays is focused on one point on

the CCD. In figure 2.26 a. this corresponds to focus the green rays together, the orange and red rays together and the blue rays together on screen. This mode is used for understanding the crystalline quality, orientation and phase of nanostructures by identifying the diffraction pattern of a certain crystal. It is also used to align the sample to zone-axis, i.e in Bragg condition for a maximized number of planes in the sample.

- High resolution TEM (HRTEM) : This is an imaging mode where the objective aperture is either very large or not used at all, letting transmitted and diffracted rays through. These consequently interfere with each other, giving the resulting image a contrast depending on the relative phases of the rays. When a sample is thin enough ($<100\text{nm}$) this will permit to observe "pseudo-atomic" resolution, i.e a phase contrast that is the product of individual atomic columns.
- Scanning TEM (STEM) : This mode holds the fundamental difference of using a converging beam on the sample where all the previous modes possess a "parallel illumination". The converged beam scans the sample and permits, by gathering highly-diffracting electrons, to obtain atomic resolution of a crystal. This mode is named high-angle annular dark field (HAADF) and is used to resolve III-V's polarity by identifying individually group III and group V atoms. STEM permits also to perform EDX at nanometer resolution (STEM-EDX) which resolves quantum wells or core-shell structures.

The majority of the samples used in TEM for this work were prepared by dry-transfer, which is rather easier to implement than FIB. Samples with grown nanostructures were observed under an optical microscope and a sharp single-use blade was used to scrap the surface. An eyelash glued to a wooden stick was then used to brush the blade and transfer the nanostructures to a TEM copper grid.

Electron microscopy is a great tool for structural characterization. Nevertheless the optoelectronic properties of semiconductors are as important. To assess those, two techniques were mainly used that are presented in the next section :

2.5.2 Luminescence

Referring to section 2.2.1, luminescence from semiconductors implies the generation of excitons and their radiative recombination. How are excitons generated is

the main difference between the next two techniques.

*This section mainly refers to the books by Sydney Perkowitz, *Optical Characterization of Semiconductors, Volume 14*[179], and by Yacobi, B. G. and Holt, D. B., *Cathodoluminescence Microscopy of Inorganic Solids*[249]. For a deeper understanding of the mechanisms and theory behind luminescence, the reader is invited to refer to these exhaustive works.*

Photoluminescence

Photoluminescence (PL) consists in using a spectrometer to measure the luminescence of a material upon excitation by a light source. The measurements can be done at room temperature (RT), in which case the band gap is usually detected. Measurements can also be done at low-temperature (LT) in which case it is possible to detect excitons, but also light emitted from quantum emitters such as quantum wells and quantum dots. PL also permits to detect radiative recombination from defects such as twins or vacancies, or from impurities such as C. Being a technique that uses light, PL is bound by the diffraction limit, setting the spatial resolution above the micron scale. The excitation depth is limited by the refractive index of the sample at laser's wavelength.

In this work, micro-PL has been carried using an in-house built setup using a 532 nm sapphire optically pumped semiconductor laser.

Cathodoluminescence

Cathodoluminescence (CL) is analogue to PL except in the excitation method. In fact, CL uses an electron beam in order to generate carriers. Therefore one can utilize the electron's much shorter equivalent wavelength to obtain very localized excitation. Its depth is limited by the acceleration voltage of the electron beam, therefore permitting a highly surface-sensitive emission. CL appears as a very adequate tool for observing nanostructures, as it permits to spatially localize emissions of different regions in a single structure, which is extremely challenging with PL. One should keep in mind that excitation volume and emission volume are not equivalent, given the significance of carrier's diffusion length at that scale, mostly at LT.

In this work, CL has been carried using an Attolight Rosa 4634 SEM-CL microscope.

Main Matter

Part I

3 III-V Integration on Si (100) : Vertical Nanospades

The results of our experiments about integrating III-V materials on Si (100) are presented in this chapter. This initial work shows the discovery of a novel nanostructure that we named nanospades and its unique crystalline structure.

Güniat, L., Martí-Sánchez, S., Garcia, O., Boscardin, M., Vindice, D., Tappy, N., Friedl, M., Kim, W., Zamani, M., Francaviglia, L., Balgarkashi, A., Leran, J. B., Arbiol, J., and Fontcuberta I Morral, A. (2019). III-V Integration on Si(100): Vertical Nanospades. *ACS Nano*, 13(5), 5833–5840.

The content of this paper has been reformatted to match that of this thesis with references combined with those at the end of this thesis. The content and figures have been reproduced here without modification with the permission of the American Chemical Society.

3.1 Introduction

My contribution to this work consisted of :

- Substrate preparation, including designing the masking method that permitted selective deposition of Ga droplets on top of Si pillars.
- Planning the growth and experiments.
- Performing the growth and statistical analysis (SEM).
- Taking active part in interpreting the results.
- Writing the manuscript.

When I first started my PhD, the idea was to find a way to engineer the VLS droplet's contact angle in a reproducible way. Anna came-up with the idea of having nano-pillars and finding a way to constraint the droplet at the top. The main challenge then was to find a way to selectively cover the whole substrate with a mask, and just uncovering the top of the Si pillars. Retrospectively, it seems evident that we had to do it the way we did it.

3.2 Abstract

III-V integration on Si(100) is a challenge: controlled vertical VLS (Vapor Liquid Solid) nanowire (NW) growth on this platform has not been reported so far. Here we demonstrate an atypical GaAs vertical nanostructure on Si(100), coined nanospade, obtained by a non-conventional droplet catalyst pinning. The Ga droplet is positioned at the tip of an ultra-thin Si pillar with a radial oxide envelope. The pinning at the Si/oxide interface allows the engineering of the contact angle beyond the Young-Dupré equation, and the growth of vertical nanospades. Nanospades exhibit a virtually defect-free bi-crystalline nature. Our growth model explains how a pentagonal twinning event at the initial stages of growth provokes the formation of the nanospade. The optical properties of the nanospades are consistent with the high crystal purity, making these structures viable for the use in integration of optoelectronics on the Si(100) platform.

3.3 Introduction

Because of their exclusive and intriguing properties, semiconductor NWs draw an increasing interest among researchers for their potential applications in a diverse range of fields, from p-n junction and high performance transistors [37, 31] to light-emitting diodes [135], solar cells [210, 139, 235], quantum computing [169, 152, 157], terahertz detection [178] and even biology [163, 78]. To complete their path towards the electronic and optoelectronic applications, their up-scalability and its compatibility with modern semiconductor processing needs to be tackled. There is currently a joint effort in the NW community to bring the technology closer to compatibility with CMOS technology. A first step was replacing Au as the liquid catalyst in the VLS mechanism[233], by other compounds, avoiding deep level traps in Si[33, 64, 105]. Highly uniform arrays have been successfully obtained by self-catalyzed VLS method[196, 126, 183, 171], allowing Au-free opportunities for solar cells. Yet, those very promising results were exclusively obtained on Si wafers oriented in the [111] crystallographic direction, which

is not the industry standard.

This work aims at implementing vertical, III-V based self-catalyzed VLS grown nanostructures on Si (100). Due to their preferential [111]B growth direction[86], NWs spontaneously grows at an angle of 35° with the (100) surface, which would strongly compromise their functionality[196]. Several groups reported [100] oriented III-V growths on III-V substrates using Au as a catalyst. This constitutes a limited number of systems, indicating the still open potential [19, 237, 166, 236]. So far, controlled, defect-free [100] oriented growth has not been demonstrated neither on the Si platform, nor in a Au-free manner.

Here, we propose an original way of engineering the contact angle from the initial stages of growth by patterning Si (100) substrates into oxidized nanoscale pillars. This is one of the key elements that we propose to obtain Au-free vertically [100]-oriented flat nanostructures on the (100) Si platform, with a yield of currently 10% (number of structures over the total number of nucleation sites). These flat NW structures, called nanospades, exhibit high quality crystalline structure with extremely few defects, rendering them suitable for photonic and energy harvesting applications.

3.4 Results/Discussion

Several studies suggest that the configuration of the droplet catalyst determines the crystal phase [86, 126], growth direction [237], polarity [253, 255] and the uniformity [162]. Here, we engineer the liquid catalyst droplet in terms of size and contact angle, before the VLS growth initiation itself to enable growth in the [100] direction. For doing so, a positive height-difference Si surface is crafted in the shape of a nanoscale pillar. Ga is then constrained at the tip using a SiO₂ mask. By varying the Ga predeposition time we make the droplet swell. This allows us to obtain contact angles that are higher than those expected for Ga on Si at equilibrium, the latter reported not stable for a reproducible NW growth [162].

The Si nanopillar arrays are produced using a process similar to Varricchio *et al*[228]. First, a dotted pattern is defined on a 4" Si wafer using electron beam lithography. Then the pillars are defined by RIE (reactive ion etching) using a

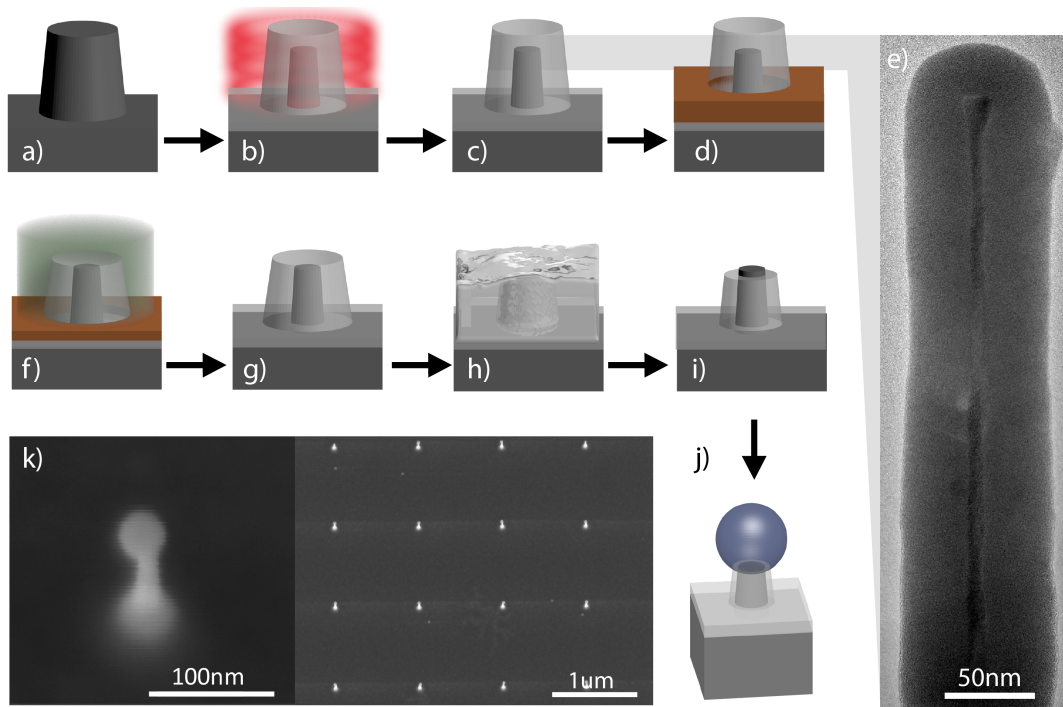


Figure 3.1: Scheme for the fabrication of the SiO_2 mask around a) Si nanopillars. b) A thermal oxidation is done at 900°C c) for nominal planar thicknesses ranging from 10 to 100nm, as seen in the TEM micrograph e). d) a spin-coating of a polymeric protective layer, and f) a reactive ion etching offer a directional etching of the dielectric mask. g) 5nm is kept at the top of the pillar to keep the Si surface intact. A final hydrofluoric acid bath h) permits to uncover the Si nanopillar's top. The sample is then introduced in the MBE chamber, and the growth is initiated with a liquid catalyst droplet predeposition j). k) SEM pictures of a Ga predeposition of 10 mins on Si at 640°C . The first picture depicts one pillar among the array shown in the second picture.

mixture of SF_6 and C_4F_8 , followed by a buffered hydrofluoric acid bath for resist stripping. The bare Si nanopillars heights vary between 150nm and $1\mu\text{m}$, and their diameters from 300 nm to 30 nm. In this study we keep the pitch distance at $1\mu\text{m}$. The pillars are subsequently oxidized at 900°C , the oxide providing the role of selective growth mask, as depicted in figure 3.1. The tips of the pillars are uncovered by a second RIE using a mixture of SF_6 and CHF_3 . Finally, a diluted HF bath is used for an isotropic etching, ensuring the uncovering of the silicon pillar tip - see Fig. 3.1- .

Given the geometry of the Si pillar, its oxidation should reach a self-terminating regime, resulting in a sub-10nm diameter[234]. This is due to the build-in of internal stresses upon oxidation, limiting the reaction rate at the interface. The

strain tends to be compressive due to the incorporation of oxygen in the Si lattice[120, 151, 36]. The thermal mismatch between both species is also expected to produce further internal stresses (tensile) during the cooling down [203]. Walavalkar *et al.* [234] showed by finite element simulations that the overall build-in stress in the Si is likely to be tensile at room temperature. The nature of the strain in our pillars is not central to this work and it will be further clarified in follow-up studies.

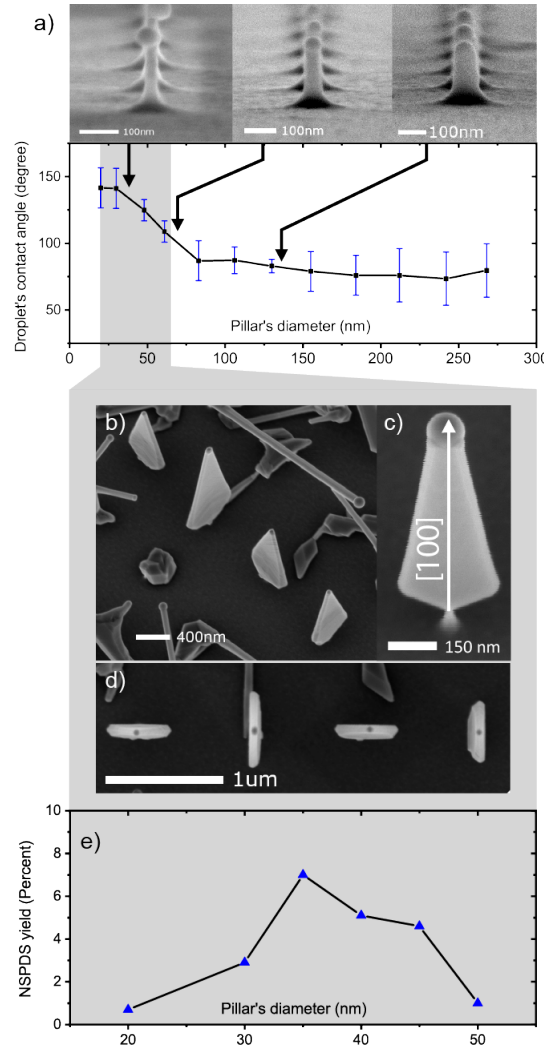


Figure 3.2: a) Table showing the relation between Si pillars' diameter and the Ga droplets' contact angle, along with SEM images representing certain diameters. b), c), and d) are SEM pictures of GaAs nanopads on Si pillars, and their growth range in the table. e) shows the relation between the yield of NSPDs and pillars' diameter for a 20nm (nominal) oxide mask.

Chapter 3. III-V Integration on Si (100) : Vertical Nanospades

Figure 3.1 e) shows a representative BF TEM (Bright-field Transmission Electron Microscopy) micro-graph of an oxidized Si nanopillar. The nominal diameter of this pillar is 75 nm and the oxidation time is set for a nominal thickness of 100nm, at a temperature of 1000°C. The contrast between SiO₂ and Si is the result of dynamical scattering at the interface and in the bulk Si, which is enhanced by the aforementioned stress[234]. The oxide is thicker at the sidewalls than at the top due to the increased surface exposed to oxygen during the thermal process, but also to the radial tensile strain in the bulk oxide, easing the early supply of oxidants radially[120]. The core Si pillar is 5 nm, indicating that the extent of the self-limiting oxide thickness can be reached in our system. The present work will focus on samples having a 15nm Si core.

Several studies show that a deterministic contact angle engineering should serve in crystal phase engineering [86, 114], and growth direction [237]. Therefore we focused on the mastering of the wetting angle of the Ga droplets on top of the pillars. In order to vary the contact angle, we increased the total volume of the droplet by changing the Ga predeposition time. The resulting contact angles have been measured by cross-sectional SEM (scanning electron microscopy). Pillars from 35 nm to 270 nm in diameter have been fabricated, oxidized, and loaded in the MBE (Molecular Beam Epitaxy) chamber where a Ga equivalent flux of 0.15×10^{-6} Torr is kept for 10 min under an ultra high vacuum. The manipulator temperature is set at 740°C, which corresponds to a substrate temperature of 650°C. Figure 3.2 a) shows SEM images, representative of the configurations obtained. We depict also the values of the contact angle as a function of the pillar diameter. We observe angles between 140° and 75°, from smaller to larger diameter pillars. There is a range between 40 nm and 100 nm where the contact angle varies almost linearly. For smaller pillars, the droplets fall down the side, which is expected to be detrimental for further MBE growths. For higher diameter pillars, the contact angle reaches the equilibrium value of liquid Ga on Si [161]. This variation of contact angle should translate to higher pillar diameters for longer deposition times, which shows the versatility and potential of this platform. It would be possible to tune the diameter and contact angle that one needs by correctly adapting the process parameters and growth conditions.

Figure 3.2 b) to d) highlights structures obtained in the range of contact angles marked in gray. They are oriented along the [100] direction. They exhibit a spade-like shape, substantiating their name. They can reach a high aspect ratio in two orthogonal directions. SEM pictures show the presence of a Ga droplet at the top,

which confirms that they grow by the self-catalyzed VLS mechanism. However, their shape evolution throughout the growth appears to be a mixed contribution between VLS [183] and VS (Vapor-Solid)[222], the former for the vertical elongation and the later for the horizontal elongation. The NSPDs presented here have been grown using a Ga predeposition step of 10min as mentioned in Figure 3.2 a), a Ga equivalent flux of 0.14×10^{-6} Torr and a V/III ratio of 12. Figure 3.2 e) indicates the yield as a function of the pillar diameter. We can reach a maximum yield close to 10% for 35 nm diameter pillars. The other pillars contain [111]B-oriented GaAs NWs and parasitic growth. The yield drastically decreases for pillars larger than 50 nm, plummeting to a value of 1%. The low yield in smaller pillars can be explained by the Ga droplet falling down the side, and in larger pillars by the energy of formation of the initial seed, as explained further below.

NSPDs have been transferred flat on a TEM grid and observed using an C_s -corrected TEM. Figure 3.3 shows a HAADF-STEM general overview of the studied nanopillar in a), details obtained on the tip in b) and c), and color map showing structure at the base in d). Polarities have been resolved by an intensity analysis, as heavier atoms (As) appear brighter. The overall structure exhibits an original crystalline structure. The base is composed of several symmetrical twins and polarities, while the body consists of a bi-crystal. Fig. 3.3 d) shows the presence of a [100] oriented domain (light blue) that is A-polar, Ga terminated, which is believed to be in epitaxial relation with the Si. This [100]A oriented domain creates a truncated octahedron with (111)A facets where twin boundaries form upon further growth, showing a multiple order twinning mechanism[226]. A similar mechanism has been observed in [111]-B oriented nanowire growth. It consists of the formation successive twinning events in the three dimensions of space, resulting in well-defined modifications in the nanowire orientation with the substrate. Interestingly, after the first monolayer, one side exhibits a change of polarity (dark blue) with respect to the other side (red). To the best of our knowledge, this is one of the first reports of a polarity change during nanostructure growth. Due to its high energetic cost, this polarity change should be very unlikely to happen[41]. Its function is the conservation of the overall polarity in both sides of the truncated octahedral seed. This structure reminds of the InAs V-shaped membranes obtained by Conesa-Boj *et al.*[34], where an [100]-oriented truncated octahedron is the seed of two [111]B-oriented "wings".

In the case of NSPDs, the top of the seed exhibits the formation of two extra twins forming an angle of 70.53° with the vertical direction, giving rise to a pentagonal grain boundary structure. It is important to note that a regular pentagon would

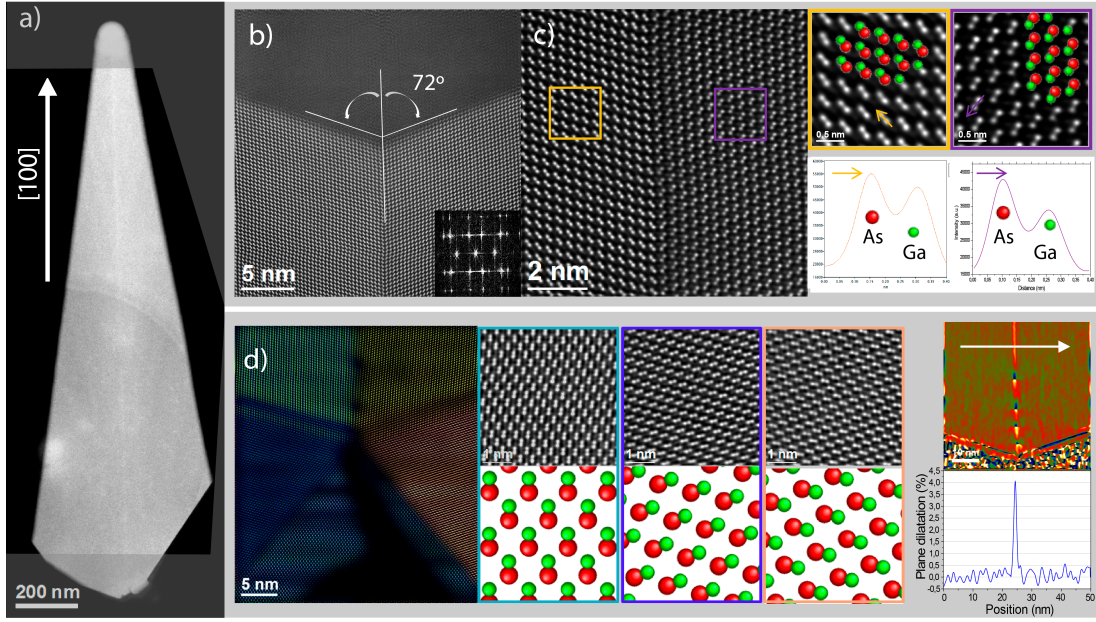


Figure 3.3: HAADF STEM study of the GaAs NSPD shown in a). b) is the growth front, c) shows the central vertical twin with the polarity of each side. d) shows a color structural map of the penta-twin at the base of the NSPD and the resolved polarities of each grain. A GPA study at the base shows the plane dilatation on the vertical twin (the strain is around 4%), along with dislocations on this boundary. Far away from the base, after a partial relaxation, the remanent strain in the boundary along the [100] direction is shown to be 2.5%.

have angles of exactly 72° , while the $\{111\}$ twinning happens at 70.53° . There is a 7.32° mismatch that is relaxed by the creation of dislocations in the first few nanometers of the vertical twin boundary. This fact is clearly visible in figure 3.3 d) where a GPA (Geometrical phase analysis) study shows 4 misfit dislocations aligned on this domain boundary, and a plane dilatation of 4% is measured in the upper region. Figure 3.3 c) demonstrates that the structure succeeds in compensating for this mismatch forming a virtually defect-free bi-crystal.

Twinning with five-fold symmetry has been observed in a variety of systems such as copper bulk [110] and NWs [125], diamond [172], Au [107, 181], but also GaAs in a study by Däweritz *et al.* [38] where RHEED (Reflexion High Energy Electron Diffraction) examinations of defects on GaAs(001) reveal a structure analog to the nanospade pentagonal seed. L.D. Marks [159] presents modified Wulff constructions for twinned nanoparticles, including five-fold symmetry twins. He divides the twinned particles into different segments bounded by the twin planes. Each segment possesses planes with given surface energies γ_x . For each twin bound-

aries, the energy is divided into two fractions: $\alpha\gamma$ and $(1 - \alpha)\gamma$ respectively for the segments sharing this twin, where α is defined as the partition coefficient. The lowest energy crystal shape is then determined by Wulff construction for each of the defined segments, with the twin boundaries included as pseudo-surface facets. The volume partition and geometric constraints are also taken into considerations. If values of α_x can be found where the segments still assemble to a complete particle, a local energy minimum may be found. The symmetrical case of $\alpha = \frac{1}{2}$ and equal volumes for each segment is always a solution, and proven to be a true minimum. In the case of a five-fold symmetry twinned particle, a second solution arises by placing two asymmetric twin relationships, pushing the meeting point of the five segments well away of the particle center. This case resonates with the NSPDs, where the pentagonal twin is located very close to the (100) substrate surface, *i.e* at the base of the structure. Despite the fact that our system is mainly kinetically-driven, it is worth noting that such asymmetry can be caused by a difference in the twinning energies due to the polarity inversion.

Interestingly, figure 3.3 b) shows the growth front formed by two {111} planes that seem to grow simultaneously. This is known as the twin plane re-entrant (TPRE) mechanism, observed recently in the growth of GaAs NWs [133], but also in other material systems such as ZnSe[239], InSb [44] and Si or Ge [168, 74], but also in the bulk. Bulk TPRE configuration permits a fast expansion of platelets creating re-entrant edges, which at the same time serve as active nucleation sites. As elucidated by R.S Wagner[231], the TPRE mechanism in bulk needs at least two twinning events to be stable. Otherwise, a single twin would rapidly outgrow itself. The platelet growth rate would then be limited by the nucleation at the ridge, which is significantly smaller. Nonetheless, Gamalski *et al.*[74] showed that the nanoscale geometry allows steady-state growth based on a single twin boundary. Here, the growth rate of the structure is completely determined by the nucleation rate at the twin rather than at the triple-phase line. This avoids any of the sides of the twin to outgrow the other. Thus, the structure remains symmetrical despite having one B-polar and one A-polar orientation, which are known to have different nucleation and growth rates[192, 254, 87, 253].

One should note that contact angle engineering resulted into a maximized yield of 8%, which is relatively low. We believe this is related to the growth mechanism, combining both a polarity inversion and a five-fold symmetry twinning. Nonetheless, we think that the yield could be further controlled. In particular, we believe the engineering of the pillar surface by nano-faceting could enable the

TPRE mechanism without the need of the pentagonal twin structure. In addition, introduction of impurities or change in the growth regime may as well increase the probability of five-fold symmetry twinning and TPRE.[90, 61]

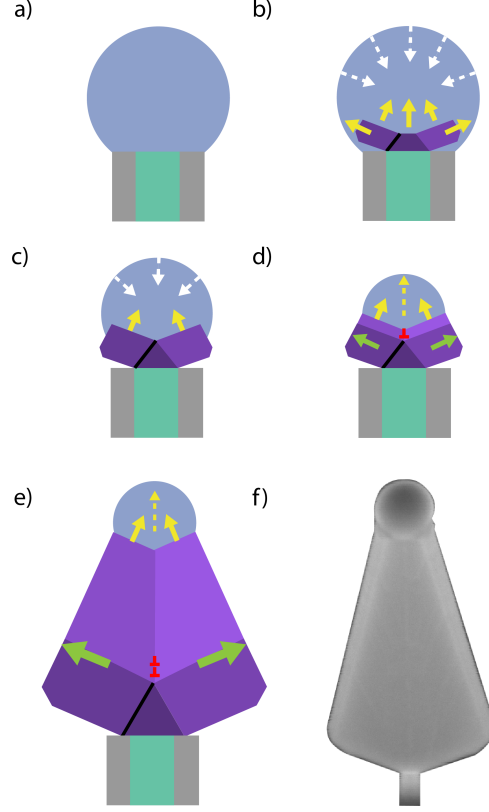


Figure 3.4: Schematic growth model depicting in a) the Ga droplet pinning, b) followed by the start of the growth with three VLS growth fronts : a [100]-oriented and two [111]-oriented. The droplet shrinks progressively, leading to a transient mode c) that is followed by d) the penta-twin formation. The growth is further continued by the VLS/TPRE on top and the VS on the sides. The polarity inversion is highlighted by the dark line, the VLS growth by yellow arrows and the VS growth by green arrows. Dislocations formed by the built-in strain are represented by inverted "T"-shapes. f) depicts a tilted SEM view of a generic nanospade.

We now proceed with the proposal of a growth model for the NSPDs, combining our observations with other groups' results on the formation of penta-twins [217] and the *in-situ* TEM observation of NW growth [98, 192, 74]. Figure 3.4 depicts the model we propose. The process starts with the pinning of the Ga droplet at the Si/oxide interface at the pillar tip. After a brief incubation time, the nucleation of GaAs layers starts. Initially, a [100] Ga-oriented pyramid forms (truncated octahedron), with the two opposite (111)A and (111)B facets. Overall, this results

in 5 liquid/solid growth fronts, leading to a decrease in the size of the droplet due to Ga consumption. The [111]-oriented lateral fronts outgrow the (100) plane, reaching the triple phase boundary, ceasing to be expanded by the VLS mechanism. After the termination of the [100]-oriented domain, a double-twinning event occurs, modifying the orientation of the growth front. As a consequence, the bi-crystals constituting GaAs NSPD's main core is formed and grows perpendicularly to the substrate. The growth will proceed by the TPPE/VLS mechanism at the top, pushing the structure up. Additional VS growth expands the structure laterally, in two [110] directions (as it is the case for typical NW growth).

The presence of twins and dislocations in semiconductor architectures could potentially reduce their viability for further applications. In order to assess the impact of the crystalline structure on the optoelectronic properties, we characterized them by luminescence. In particular, we were interested in obtaining signal of the defects at the NSPD base. For this, we increased the volume of the NSPDs by vapor-solid growth akin to ref [165]. The thick NSPDs are then transferred flat onto an Au-coated Si substrate. Figure 3.5 shows in a) the micro-photoluminescence (μ PL) spectra at 300K and 8K, and in b) the cathodoluminescence (CL) spectra line scan.

In the RT (room temperature) μ PL spectra, an emission at 867 nm which corresponds to the band gap of GaAs can be seen, along with a secondary much weaker peak slightly above noise level between 900 nm and 930 nm. This secondary feature becomes almost invisible at 8K where the overall signal -corresponding to the free-exciton recombination emission in bulk GaAs at 1.51 eV, and to an impurity-related band between 1.48 eV and 1.5 eV[117, 130, 137] - is much higher. We attribute this weaker peak to defects at the base of the nanostructure. These defects exhibit energy levels with a limited density of states, as it is usually the case for localized defects. As expected, emission from such states saturate with increasing excitation power, especially at low temperature where recombination lifetimes are longer. By looking at the CL spectra in b), the same feature is observed. The line scan along the NSPD unveils its origin at the base, close to the semi-octahedron seed, the polarity inversion and dislocations. It is concluded that those radiative transitions occur at the mentioned defects, and are not observed in the rest of the structure. The CL spectra also show a decrease of the 819nm exciton emission in upper half of the structure. This is explained by the increase of the surface to volume ratio, quenching the emission by non-radiative recombinations at the GaAs surface. Further CL characterizations using AlGaAs shells and GaAs quantum wells are envisioned, along with a study on self-assembled quantum dots [103, 65] for assessing the impact of the NSPD structure on their formation.

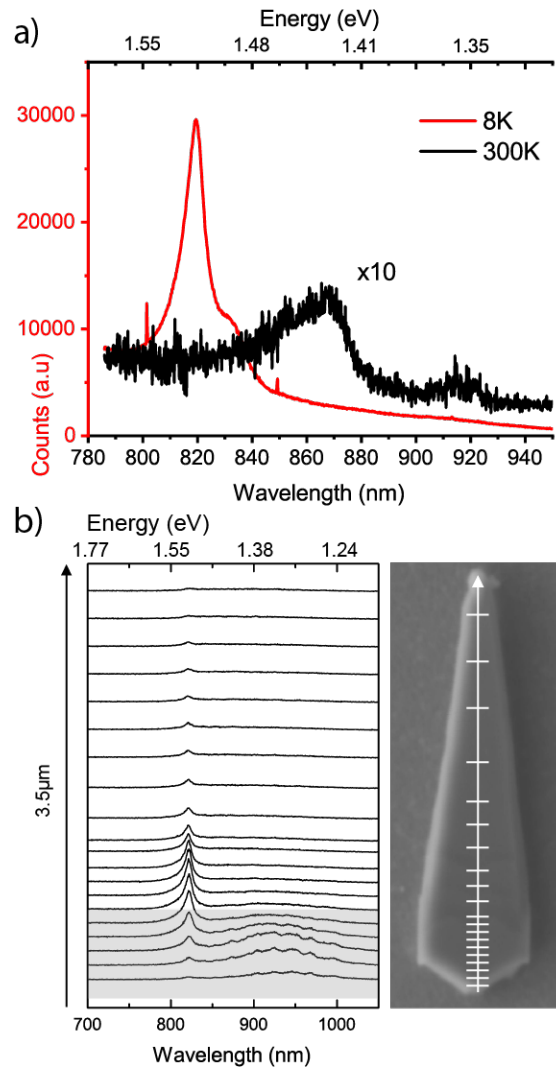


Figure 3.5: a) Photoluminescence and b) 10°K Cathodoluminescence characterization of two different NSPDs. The vertical lines in the SEM picture shows where the CL spectras have been acquired. Both studies show the presence of low-energy peaks linked spatially with the penta-twin and polarity inversion region.

3.5 Conclusion

To conclude, we have successfully designed and built an innovative Si platform for self-catalyzed VLS growth, consisting of etched nanopillars covered by a thermal oxide. The presence of a self-limiting oxidation effect permits a Si exposure in the chamber that is under 10nm, enabling non-equilibrium growth conditions. The appearance of [100]-vertically oriented nanostructures, called nanospades, is a proof of the viability of this approach. A yield of NSPDs up to 10% has been obtained. This is expected to increase with further growth optimization. Overall, the NSPDs are mainly a bi-crystal nucleated by penta-twins at the base. The optical properties are clearly consistent with high quality GaAs. The penta-twin exhibits weak luminescence below the GaAs bandgap, spatially localized at the base of the nanostructure. The NSPDs are promising structures for room temperature lasing, energy harvesting and photonic applications. [165, 177, 118, 207].

Methods/Experimental

A 2min 600W O₂ plasma power in a TEPLATM GigaBatch is done on a 100mm Si wafer for surface activation before exposing it by E-Beam lithography with a VistecTM EBPG5000ES, and using Dow Corningtm HSQ 006 (Hydrogen silsesquioxane) as a resist. The dose used is 2740 μ C/cm² for all the pillar's diameters. The wafer is then developed using a commercial solution of Microposit^R MF^R CD26 for 2 minutes, and rinsed sequentially with water, acetone and propan-2-ol. A 2min 600W O₂ plasma power in a TEPLATM GigaBatch is done for further cross-linking the HSQ. The wafer is then introduced in an AlcatelTM AMS200 DSE reactive ion etcher, where a customized recipe using SF₆ and C₄F₈ is used for creating the pillars. A buffered hydrofluoric acid (7:1) bath is then used for 2 minutes to remove any trace of resist. A thermal oxidation is then done at 900°C for a variable amount of time depending on the wanted oxide thickness. After the oxide growth, a 20nm Styrene Methyl Acrylate based resist (ZEP) film is spin coated and heated for 2min at 180°C for polymerization. The sample is inserted in an OxfordTM Plasmalab system 80 PLUS using a mixture of SF₆ and CHF₃ at 100W plasma power for 40 seconds to uncover the pillars. 10min of O₂ plasma permits to remove the resist, and a last cleaning involving a 5min acetone bath, a 2min propan-2-ol bath and a 35sec HF bath at 1% concentration makes the sample ready for growth.

The growths are conducted in a DCATM MBE chamber under a Ga BEP (beam equivalent pressure) of 0.14×10^{-6} Torr and an As BEP of 1.7×10^{-6} Torr for 45 minutes. The samples were characterized by SEM using a ZeissTM Merlin and by HAADF STEM using a probe corrected FEI Titan 60-300 equipped with a high brightness field emission gun (XFEG) and a CETCOR corrector from CEOS. The μ PL measurements were done using a in-house built setup using a 532nm SapphireTM optically-pumped semiconductor laser, and the CL using an AttolightTM Rosa 4634 SEM-CL microscope at 5keV.

3.6 Acknowledgements

LG thanks all the MBE team for the very nice coordination and collaboration. Special thanks to AFiM for fully supporting this work. We thank also the SNF and QSIT for funding the project (projects 200021_169908 et IZLRZ2_163861). SMS acknowledges funding from "Programa Internacional de Becas "la Caixa"-Severo Ochoa". JA and SMS acknowledge funding from Generalitat de Catalunya 2017 SGR 327 and the Spanish MINECO project ENE2017-85087-C3. ICN2 is supported by the Severo Ochoa program from Spanish MINECO (Grant No. SEV-2017-0706) and is funded by the CERCA Programme / Generalitat de Catalunya. Part of the present work has been performed in the framework of Universitat Autònoma de Barcelona Materials Science PhD program. The HAADF-STEM microscopy was conducted in the Laboratorio de Microscopias Avanzadas at Instituto de Nanociencia de Aragon-Universidad de Zaragoza. Authors acknowledge the LMA-INA for offering access to their instruments and expertise.

4 Light-Emitting InGaAs Heterostructures on Si (100)-Integrated GaAs Nanospades

The results about growing heterostructures on GaAs nanospades and characterizing their luminescence are presented in this chapter. This part of the thesis is the linear follow-up to the previous chapter and intends on functionalizing the nanospade structure.

Güniat, L., Tappy, N., Balgarkashi, A., Charvin, T., Lemerle, R., Morgan, N., Dede, D., Kim, W., Piazza, v., Leran, J.B. Fontcuberta i Morral, A., (2021). Light emitting InGaAs Heterostructures on Si (100) integrated GaAs Nanospades.

The content of this paper has been reformatted to match that of this thesis with references combined with those at the end of this thesis. Although this paper has not been submitted for publication, it has been brought as close as possible to the final version using the currently-available data.

4.1 Introduction

My contribution to this work consisted of :

- Substrate preparation
- Planning the growth and experiments.
- Performing the growth and statistical analysis (SEM).
- Taking active part in interpreting the results.
- Writing the manuscript.

4.2 Abstract

III-V materials outperform Si in optoelectronics due to high carrier mobility, electron mean free path, spin-orbit coupling, and g-factor, as well as the possibility to engineer their bandgap through alloying. Nevertheless complementing Si technology with III-Vs by integration on Si(100) remains a challenge. Vertical nanospades (NSPDs), i.e III-V nanostructures that grow on Si(100), provide a viable solution. Here, we showcase the potential of these structures in optoelectronics by demonstrating InGaAs heterostructures on GaAs NSPDs that emit in the infrared. We observe distinct localization of different wavelengths in different regions of the NSPD. We correlate this characteristic to the bipolar nature of the structure thus opening new perspectives for dual wavelength light emitting diode structures. This work paves the path for integrating optically active III-V structures on the Si(100) platform.

4.3 Introduction

As researchers look for materials and systems to meet today's advancing technological needs, one of the key challenges remains the integration of emerging materials with established platforms. The semiconductor field does not deviate from this rule; III-V systems show outstanding performance in applications such as solar cells[210, 139, 235], transistors[37, 31], and infrared or terahertz detectors. [178]. However, their monolithic integration on Si wafers is still challenging, limiting their up-scalability. In fact, one needs to overcome inherent difficulties to heteroepitaxy such as polarity and lattice mismatch[221]. One way to tackle these issues is to grow III-V nanowires (NWs) on Si [115, 170, 126]. Nano-sized objects show an increased capacity for strain relaxation, and they also possess a very small footprint that protects them from anti-phase boundaries[91]. NWs have shown to be great templates for the growth of quantum heterostructures[143, 101, 103] and open perspectives in fields such as quantum computing[169, 152, 157] and optoelectronics[208, 164]. Despite their promise, vertical III-V NWs have proven very challenging to obtain on Si (100), since a (111)B growth direction is energetically preferred[6]. Recently, we have demonstrated the integration of vertical nanostructures on Si (100) by the growth of vertical nanospades (NSPDs) [92], which permits to combine the advantages of the NW architecture and the CMOS-compatible Si (100) platform.

NSPDs are very pure crystalline GaAs vertical nanostructures on Si (100) nanopillars. This study shows their capacity to serve as templates for growing quantum heterostructures such as GaAs/InAs/GaAs directly on Si (100). We show how to

grow heterostructures on NSPDs, and what differentiates them from conventional NW heterostructures. We show the optoelectronic behavior of a GaAs/InGaAs/-GaAs core-shell NSPD system and link it with morphological aspects, such as shell thickness, the NSPDs' stem crystal polarity and In concentration. Finally we comment on the future of III-V implementation on Si(100).

NSPDs are elongated nanostructures obtained using the self-catalyzed vapor-liquid-solid (VLS) mechanism in a molecular beam epitaxy (MBE) system. Compared with GaAs self-catalyzed VLS NWs that usually grow in the [111]B direction, NSPDs are bi-crystals growing in the [100] direction with mirrored (111) growth planes. The two (111) planes have a twinning relationship in the [110] direction perpendicular to the growth axis and therefore exhibit different polarities at the growth front[92]. As a consequence, NSPDs are [100]-oriented structures born from the joint growth of a (111)A and a (111)B plane. Despite the difference in growth kinetics between (111)A and (111)B planes, NSPDs remain morphologically symmetrical due to the growth being completely limited by the nucleation at the twin boundary.

4.4 Results/Discussion

The twin plane crosses the entire NSPD and divides it into two symmetrical (111) domains that are visible in bright-field transmission electron micrographs (BF TEM) (see supplementary information). The crystal rotation through that twin is 60 degrees in the direction orthogonal to the twin plane (ortho-twin[121]) and do not form a polarity inversion. In Figure 4.1a. it is possible to see a scanning electron micrograph (SEM) of an as-grown NSPD on a Si (100) substrate. The Ga droplet catalyst is visible on top of the nanostructure. NSPDs exhibit a hexagonal cross-section with two (110) vertical side-walls, front and back on this Figure, and four higher-index converging side-walls, left and right on the same Figure. For a more detailed analysis of the growth mechanisms and initiation of NSPDs, please refer to our previous study on NSPDs that can be found in ref.[92].

We use GaAs NSPDs on Si (100) nanopillars as a core for the growth of III-V heterostructures. We observed early in our experiments that shell growth in the MBE[187] resulted in the transformation of the former tilted side-walls observed in Figure 4.1a. into vertical side-walls on a substantial portion of the nanostructure,

Chapter 4. Light-Emitting InGaAs Heterostructures on Si(100)-Integrated GaAs Nanospades

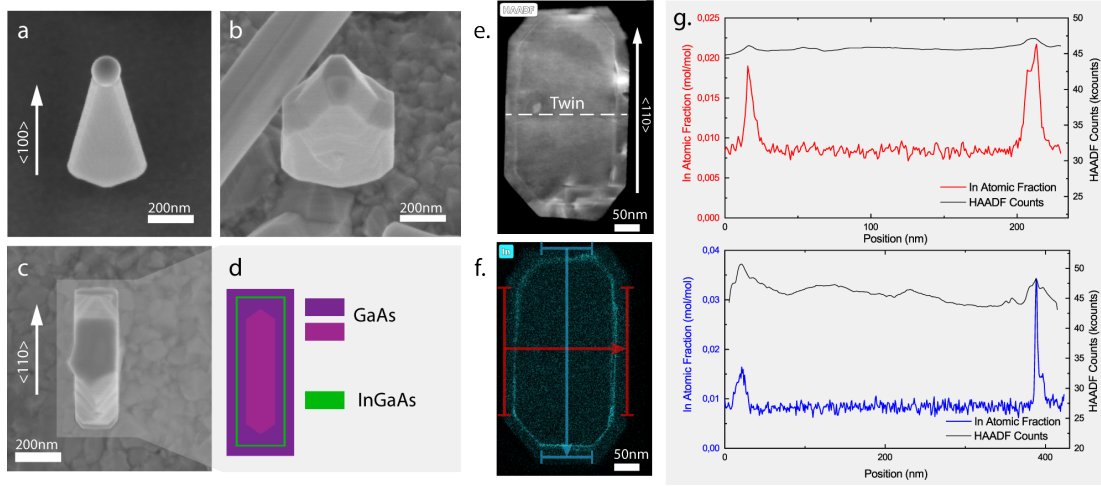


Figure 4.1: SEM micrographs of a. as-grown GaAs NSPD on Si(100) (20° tilted view), b. capped NSPD (20° tilted view), c. top-view of a capped NSPD showing the rectangular base cross-section, d. schematic of the inner layers of the studied NSPDs, e. Scanning transmission electron microscopy (STEM) high-angle annular dark-field (HAADF) image of a NSPD cut by ultra-microtomy, f. STEM energy-dispersive x-ray (EDX) map showing the In-rich shell, g. Average line scans of the In concentration in f. Red corresponds to the left-right scan and blue to the top-down scan. On the right axis the HAADF intensity counts are shown.

as seen in Figure 4.1b. The cross-section shape changes from hexagonal to rectangular, as seen in Figure 4.1c. (NSPD SEM top-view). We attribute the obtained shape to a change in growth temperature and As partial pressure that, together, kinetically favours vertical fronts, i.e switches the kinetic crystal shape (KCS) of the system[4]. The crystalline orientation of these facets is discussed further in this study.

Growing a first GaAs shell for long enough, i.e generating the change of KCS, before growing an InGaAs/GaAs shell opens perspectives for growing rectangular InGaAs quantum wells. In such wells, it is predicted that quantum states at the corners will be energetically distinct from quantum states in the facets.[202, 227, 157]. This can confine electrons at the corners, meaning a NSPD could host up to four quantum wires that are robust to many kinds of perturbations. With this in mind, we show the target cross-section of the grown structure in Figure 4.1d. A GaAs NSPD core (light purple) is grown at higher temperature (610°C) and lower As partial pressure (1.5×10^{-6} Torr) for a V/III ratio of 12 until reaching a length of 1.5µm. The As_4 partial pressure is then raised up to 1×10^{-5} Torr, Ga shutter closed for 30 minutes in order to stop the VLS growth process and consume the Ga

droplet. The temperature is also dropped significantly for entering the VS growth regime. Then a first GaAs shell (dark purple) is grown, forming the rectangular vertical facets. Pure InAs is sent for a relatively short time with a decreased As_4 flux of 5×10^{-6} Torr and a V/III ratio of 55 (light green), before re-initiating a GaAs capping shell growth (dark purple). We varied the shell growth temperature from 430°C to 390°C. We expect a substantial inter-diffusion of elements, leading to an InGaAs nanostructure with an In-rich region where InAs was deposited, and Ga-rich regions for the core NSPD and the two capping GaAs-grown shells[13]. For high shell growth temperatures (430°C and 420°C) we expect InGaAs clustering or accumulation at defects such as stacking faults or dislocations. This can be explained by InAs strain relaxation and a high In diffusion length, leading to the nucleation of 3D structures[13]. For samples with a lower shell growth temperature (400°C and 390°C) we show that a more uniform GaAs/InGaAs/GaAs heterostructure is obtained.

Cross-sections of NSPDs grown as a GaAs core and GaAs/InGaAs/GaAs shells grown at 400°C were prepared using ultramicrotomy[242]. In order to confirm the heterostructure, high-angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) was performed, given that such technique permits to obtain images with an atomistic contrast (Z contrast). Figure 4.1e. shows a HAADF STEM image of the NSPD's cross-section. The contrast allows us to identify the presence of a thin well in the structure. Figure 4.1f. shows the corresponding STEM energy-dispersive X-ray (EDX) map for In. We observe the presence of an In-rich thin shell in the structure that corresponds to an InGaAs well. The thin layer is uniform and conformal to the NSPD core, as expected from a low-temperature shell growth. Although in the STEM EDX measurement we observe an octagonal shell and not a rectangular shell like the ideal structure cross-section of Figure 4.1d, we believe this cross-section comes from an upper-part of the NSPD where the (112)-oriented side-walls are not completely kinetically supplanted by the newly-vertical side-walls, similar to the work by Fonseka et al. on <100>-oriented InP nanowires[62].

Figure 4.1g. shows the line scans for In composition averaged over each vertical sidewall. The red curve corresponding to a left-right scan and the blue curve to a top-down scan on image f. It confirms the presence of In in highly localized and narrow regions corresponding to the position of the target quantum well. The left-right scan (red curve) shows two peaks of relatively equal heights at $2 \pm 0.3\%$ In composition. Their full-width half-maximum (FWHM) values are 3nm and 4.5nm.

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The top-down scan (blue) shows two peaks of relatively different heights at 1.5% and 3.5%. Their FWHM values are respectively 5.7nm and 1.7nm by Gaussian fitting. Although these values can show a difference in InGaAs well width for a given In quantity, or a difference in In concentration, this difference in height and FWHM can also be caused by a STEM misalignment or drifting. In fact, measuring the area under the peaks, the respective difference between left and right peaks are similar for red and blue curves : left red is equal to 0.075, right red to 0.14, left blue to 0.09 and right blue to 0.16. Unveiling composition differences between each side of a NSPD needs further studies such as atom-probe tomography (APT)[68]. Nevertheless, we explore this asymmetry further by studying the optoelectronic behaviour of such NSPDs.

NSPDs were transferred flat on a TEM grid and loaded in an Attolight Rosa cathodoluminescence (CL) setup. CL permits to excite a sample using an electron source and to simultaneously gather photons emitted from the excited area and surrounding region. The resolution is limited by the interaction volume of the electrons within the structure as well as the diffusion length of the excited electron-hole pairs[32, 108]. CL raw data consists of one acquired spectra for each pixel of a two-dimensional map, called a hyperspectral (HS) map. This map can be correlated with a secondary electron (SE) image of the probed surface.

Samples grown at a higher shell temperature (430°C and 420°C) were exhibiting localized emissions throughout the NSPD, as we previously observed in nanowire based heterostructures[13], due to In clustering and inter-diffusion. CL analysis of such samples can be found in the supplementary information. Here we will mainly discuss the obtained CL results of samples with shells grown at 390°C.

Figure 4.2 shows a CL overview of measurements performed at 10K on a NSPD with the shell grown at 390°C. Figure 4.2a. shows, as a dotted curve, the average intensity spectrum, which corresponds to the sum of the CL intensity for every emission energy over the entire acquired map divided by the total number of acquired spectra within that map. Figure 4.2b. shows the SE image of the studied NSPD. Figure 4.2c. shows the CL-panchromatic map (CL-PAN) which corresponds to the sum of the CL intensity for every acquired spectra over all the emission energies divided by the total number of acquired spectra within that scanned region.

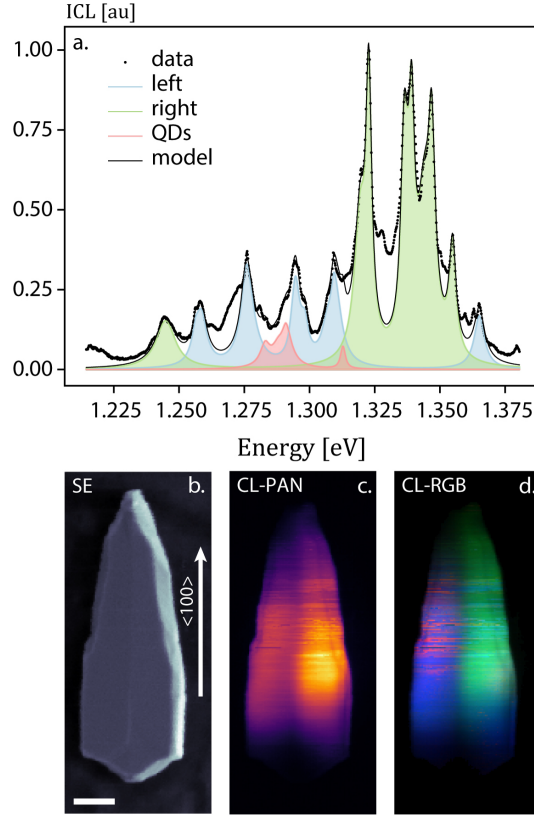


Figure 4.2: CL measurements obtained on a NSPD with 390°C shell growth temperature. *a.* Average spectra showing the raw data, the fitted average model and the three emission groups as green, blue and red. *b.* SE image of the measured NSPD. *c.* Panchromatic map of the signal. *d.* HS map of the three emission groups. Scale bar is 200nm.

Figure 4.2a. depicts the measured emission spectrum. NSPD's luminescence appears rich between 1.225eV and 1.375eV. The spectral range is consistent with $In_xGa_{1-x}As$ emitting features such as In-rich regions, quantum structures like quantum dots and quantum wells. 1.225eV would correspond to the band-edge emission of $In_{0.2}Ga_{0.8}As$ and 1.375eV to $In_{0.09}Ga_{0.91}As$. The high number of emission peaks could indicate that In composition varies within the structure. We modelled the raw data by fitting 19 Lorentzian peaks for each acquired spectra, i.e each point of the HS map. The model's corresponding average intensity spectrum is indicated as the black line. The agreement between the model and the experimental data confirms that the emission fingerprint of the NSPD arises from the combination of a finite number of narrow emission lines.

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The SE image in Figure 4.2b. shows that this NSPD exhibits vertical side-walls from both sides like seen in Figure 4.1b. The top-half of the NSPD shows rough converging side-walls. We believe the top-half GaAs shell grew conformally to the NSPD core. The key elements that permit extended vertical side-walls still need to be systematically assessed.

Figure 4.2c. indicates that the entire structure emits with some intensity variation. The base emits at a lower intensity which is consistent with our previous work[92] showing that the crystalline structure of the NSPD has a higher defect concentration in this zone, including a five-fold twinning region, dislocations and a polarity inversion. The end of the structure also shows a low emission, often linked with the consumption of the Ga droplet forming a defected region[13]. The NSPD's geometrical axis shows a decrease in intensity that is linked with the central twin. We believe the mentioned defects act as non-radiative recombination centres and decrease the local luminescence.

When tracking the emitting areas as a function of the emission energy, we see that peaks can be classified in three distinct groups corresponding to different emitting features and locations within the NSPD. The three groups are indicated in Figure 4.2a. as blue, green and red. Blue is composed by seven peaks between 1.250eV and 1.315eV and one peak at 1.365eV. Green is composed by seven peaks between 1.315eV and 1.355eV and one peak at 1.2435eV. Red is composed by three peaks between 1.27eV and 1.29eV and one at 1.312eV. Figure 4.2d. shows the average intensity spectra for the three groups. The red group emits at the top-half of the NSPD in a localized and non-uniform way. Its emitting behaviour could be attributed to multiple InGaAs clusters forming at the surface of the rough, conformal GaAs shell[94].

We observe that, despite some signal intermixing, the blue and green groups emit uniformly along the NSPD and are respectively dominant at the left and right. These two emission groups are attributed to features present through the whole structure, namely the GaAs/InGaAs/GaAs heterostructure seen in Figure 4.1f. This asymmetry in CL emission is correlated with the NSPD crystalline structure: specifically the central twin. The emission energy significantly changing from one side to the other denotes a change in morphological and/or compositional properties of the InGaAs section. We believe this unique optoelectronic "dual emission" is characteristic of the NSPD geometry and can be explained by its internal crys-

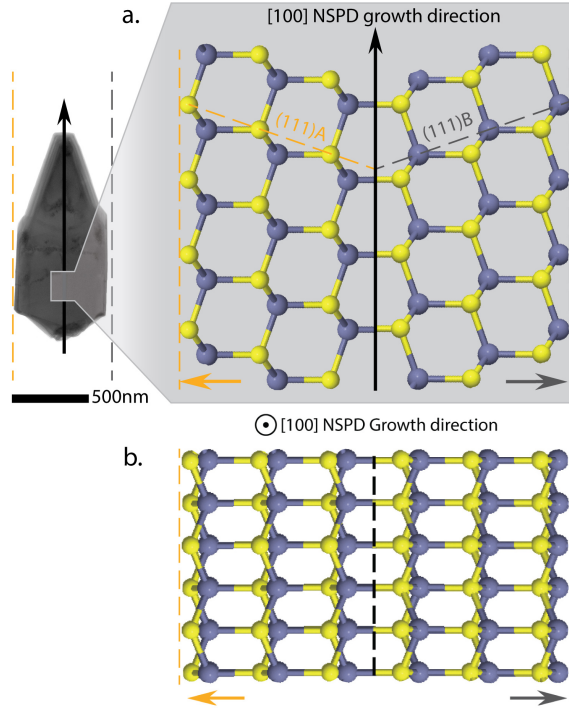


Figure 4.3: *Atomistic model of the NSPD crystal structure. a. BF TEM image of a NSPD with the crystal side view. b. Crystal top view. The central twin is represented by a dotted line.*

talline orientation. Eventually, one could use this energy shift to design a dual wavelength light emitting diode structure, LED. By exciting selectively on each side, one could selectively emit the required wavelength.

We move now to the correlation between the differentiated light emission with the atomic structure of each side of the NSPD. To illustrate this, we show in Figure 4.3 an atomistic model of the internal structure of the NSPD far from the base. We can see that the $\langle 100 \rangle$ growth direction of the NSPD is only referring to the substrate orientation and not the internal orientation of the crystal domains. In fact, the NSPD VLS growth front is composed by a (111)A and a (111)B plane, visible respectively in orange and grey in the Figure. Figure 4.3a. also shows that, due to the $\langle 110 \rangle$ orientation of the central twin, the left and right vertical side-walls of the NSPD are (111) planes of different polarities, highlighted by the orange and grey arrows on the Figure. The left side corresponding to the (111)A VLS growth front also exhibits a (111)A vertical side-wall. Similarly, the right side corresponding to the (111)B VLS growth front exhibits a (111)B vertical side-wall.

Figure 4.3b. shows a top view of the NSPD with the central twin plane shown as a dotted line. We can observe the left (111)A vertical side-wall and the right (111)B vertical side-wall. Top and bottom vertical side-walls on this image correspond to the (110) vertical planes and do not exhibit a particular polarity. We link the optoelectronic properties of GaAs/InGaAs/GaAs NSPDs with their crystal structure, i.e the difference in polarity between the opposite vertical side-walls. The literature shows that the kinetics of III-V VS growth is polarity-dependant[260, 259, 93], including, more specifically the growth of InAs heterostructures on GaAs nanowires[93]. Guo et al. explain the polarity-driven effect by a difference in lattice strain relaxation between the A-polar and the B-polar facet during In incorporation. As every group III-element needs to form three bonds on the (111)A surface and only one on (111)B, the InAs higher lattice constant leads to a preferential In incorporation at the B-polar surface. We believe the mechanism for this left/right asymmetry in the CL measurements observed in NSPDs with shells grown at 400°C and 390°C can be explained by the polarity-driven effect. The (111)B vertical side-wall appears preferential for In incorporation, hence showing a higher In composition. Higher In composition leads to a red-shifted emission, thus the blue group emission of Figure 4.2 corresponds to the (111)B vertical side-wall. This opens perspectives for single free-standing III-V heterostructures on Si exhibiting two distinct square quantum wells with distinct optical responses.

4.5 Conclusion

In this study we show the potential for growing InGaAs/GaAs quantum heterostructures in VLS-grown GaAs NSPDs. We manage to obtain a continuous InGaAs thin shell by decreasing the shell temperature, avoiding In clustering and inter-diffusion. We studied the optoelectronic properties of such heterostructures and linked them with the unique crystalline structure of NSPDs. We unveiled the potential presence of a dual emission due to a difference in polarity between each side of the NSPD. If engineered, this opens perspectives for dual-LED nanostructures on Si where each side of the central twin could be excited separately at will. Nevertheless, as the CL spectra appear richer than a simple, single-well exciton emission or band edge transition, more advanced optoelectronic and compositional characterization is needed. Power-dependent photoluminescence or STEM CL combined with APT or aberration-corrected HAADF STEM could provide valuable insights to this complex system[41].

Methods/Experimental

For EBL pillars: A 2min 600W O₂ plasma treatment in a TEPLA™ GigaBatch system is done on a 100mm Si wafer for surface activation before exposing it by E-Beam lithography with a Vistec™ EBPG5000ES, using Dow Corning™ HSQ 006 (Hydrogen silsesquioxane) as a resist. The dose used is 2740 μ C/cm² for all pillar diameters. The wafer is then developed using a commercial solution of Microposit^R MF^R CD26 for 2 minutes, and rinsed sequentially with water, acetone and propan-2-ol. A 2min 600W O₂ plasma treatment in a TEPLA™ GigaBatch is done for further cross-linking the HSQ.

The wafer is then introduced in an Alcatel™ AMS200 DSE reactive ion etcher, where a customized recipe using SF₆ and C₄F₈ is used to etch back the substrate in the un-patterned regions, creating the pillars. A buffered hydrofluoric acid (7:1) bath is then used for 2 minutes to remove any trace of resist. A thermal oxidation is then done at 900°C for a variable amount of time depending on the wanted oxide thickness. After the oxide growth, a 20nm Styrene Methyl Acrylate based resist (ZEP) film is spin coated and heated for 2min at 180°C for polymerization. The sample is inserted in an Oxford™ Plasmalab 80 PLUS system using a mixture of SF₆ and CHF₃ at 100W plasma power for 40 seconds to uncover the pillars. 10min of O₂ plasma permits to remove the resist, and a last cleaning involving a 5min acetone bath, a 2min propan-2-ol bath and a 35sec HF bath at 1% concentration makes the sample ready for growth.

The growths are conducted in a DCA™ MBE chamber. All the reported MBE growth temperatures are estimations of the substrate temperature. From measurements done with an infrared camera on known standard GaAs samples, we estimate a difference of 130°C between the set PID and the real temperature.

Ultramicrotomy: structures were peeled-out from the substrate using an epoxy resin. The thin cross-sections were prepared using a Leica EM UC7 Ultramicrotome system at room temperature. A Diatome ultra 35° diamond knife was used to obtain smooth cross-sections. The thickness of each cross-section was 90nm.

The samples were characterized by SEM using a Zeiss™ Merlin and by BF TEM/HAADF STEM using a FEI™ Talos. The CL measurements were done

using an Attolighttm Rosa 4634 SEM-CL microscope.

4.6 Acknowledgements

LG thanks all the MBE team, but also the CMi staff at EPFL without whom this study could not be possible. LG thank SE for the fruitful discussion about STEM EDX. LG and AB thank Colette Valloton for the help on ultramicrotomy. We thank the Swiss National Science Foundation (SNF) and QSIT for funding the project (projects 200021_ 169908 et IZLRZ2_ 163861).

5 GaAs Nanowires on Si Nanopillars : Towards Large Scale, Phase-engineered Arrays.

The results of our experiments about growing large-scale arrays on Si(111) using nanopillars are presented in this chapter.

Güniat, L., Ghisalberti, L., Wang, L., Dais, C., Morgan, N., Dede, D., Kim, W., Leran, J.B., Balgarkashi, A., Minamisawa, R., Solak, H., Carter, C. and Fontcuberta i Morral, A. (2021) GaAs Nanowires on Si Nanopillars : Towards Large Scale, Phase-engineered Arrays.

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5.1 Introduction

My contribution to this work consisted of :

- Substrate preparation.
- Planning the growth and experiments.
- Performing the growth and statistical analysis (SEM, TEM).
- Taking active part in interpreting the results.
- Writing the manuscript.

This part translates from Si (100) to Si (111) and has a complementary objective. We found technical challenges to increase the nanospade's vertical yield above

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20% on Si (100) and we believed we needed better quality pillars, i.e a clear flat Si/SiO_2 interface at the top and keeping the side-wall oxide untouched. We decided to "step back" and focus on bringing the developed Si pillar geometry to the Si (111) platform, experimenting with nanowires, which is a much more studied nanostructure. The idea is also to take advantage of the contact angle engineering and the possibility to produce Si pillars by photolithography in order to produce large-scale, phase engineered arrays. This work demonstrates the possibility of large-scale GaAs nanowires arrays using SiO_2/Si pillars and demonstrates the phase-engineering potential of the pillar geometry.

5.2 Abstract

Large-scale patterning for vapor-liquid-solid growth of III-V nanowires is a challenge given the required feature size for patterning (45 to 60nm holes). In fact, arrays are traditionally manufactured using electron-beam lithography, for which processing times increase greatly when expanding the exposure area. In order to bring nanowire arrays one step closer to the wafer-scale we take a different approach and replace patterned holes with Si pillars that are between 150nm to 200nm in size. We fabricate them using photolithography methods such as phase-shift lithography or deep ultraviolet (DUV) stepper lithography. We use Si oxidation to reach the desired feature sizes and stabilize the Ga catalyst droplet in order to successfully grow nanowire arrays. In this study we first identify the key parameters and fundamental aspects of nanowire growth on Si pillars by electron-beam lithography, where we reach vertical yields of 55%. We show that the droplet configuration, i.e contact angle and triple phase line, are central for a successful growth, and that the pillar geometry permits to engineer the droplet contact angle. We compare our experiments with simulations performed in surface evolvertm and observe a strong correlation. We then manufacture SiO_2/Si pillars using phase-shift lithography and grow large-area GaAs nanowire arrays. We reach a maximum local vertical yield of 67% and a global chip-scale yield of 40%. We believe that, through a greater control over certain key processing steps, such as reactive ion etching, one can push this yield to 90+% and open perspectives for deterministic nanowire phase-engineering at the wafer-scale.

5.3 Introduction

The increasing need for performance in applications including self-driving cars, next-generation computers, hyper-efficient solar panels and quantum computers

had pushed Si to the verge of its fundamental capacities. Promising candidates for many applications are III-V materials, as they exhibit valuable electronic/optoelectronic properties, which outperform Si in these domains. Yet the lattice mismatch, polarity mismatch and surface defects are prohibiting the integration of III-V thin films on Si. One way that researchers have tried to address these challenges is through nucleation and growth at the nanoscale, for example via nanowires (NWs). These filamentary structures also permit crystal phase engineering by controlling the formation of either wurtzite (WZ) or zincblende (ZB) phases. They can be obtained in perfect arrays, making them promising for infrared and/or terahertz detection [178], high-mobility transistors[37, 31], topological superconductors [169, 152, 157] or high-yield photovoltaics [210, 139, 235].

Semiconductor NWs can be grown using a plethora of techniques, from top-down[174] to bottom-up vapor-phase methods[91]. In this work we will solely focus on GaAs NWs grown by the vapor-liquid-solid method (VLS) in a molecular beam epitaxy (MBE) system[64]. Operating at ultra-high vacuum, MBE allows for very precise control over precursor fluxes, making it an ideal tool for fundamental studies of vapor-phase nanostructure growth on Si. MBE appears as the ideal tool for fundamental studies about vapor-phase nanostructure growths on Si[230]. We use self-catalyzed VLS, meaning the droplet catalyst is composed of Ga (and As at low concentration)[15, 57, 183]. This differs from conventional VLS that uses Au or other metals as the liquid catalyst[25]. Self-catalyzed VLS avoids metal contamination in the grown material[91].

Vertical NW arrays are a promising platform, but their fabrication comes with a twist: the most common processing methods rely on electron-beam lithography (EBL), a slow technique with processing times that increase dramatically with the exposed area, even taking several days for a single wafer[5]. The community is actively looking for alternatives, and methods like nano-imprint lithography[115, 170] have been proposed, permitting the rapid fabrication of large-scale arrays using a patterned stamp and an imprinted polymer layer. Here, we propose a different approach based on the use of advanced photolithography for substrate patterning, the same technology used to pattern Si wafers for current CMOS technology.

We trade the common use of nano-patterned holes[196] for the use of SiO_2/Si pillars that, by oxidation and dimension engineering, permit to potentially obtain

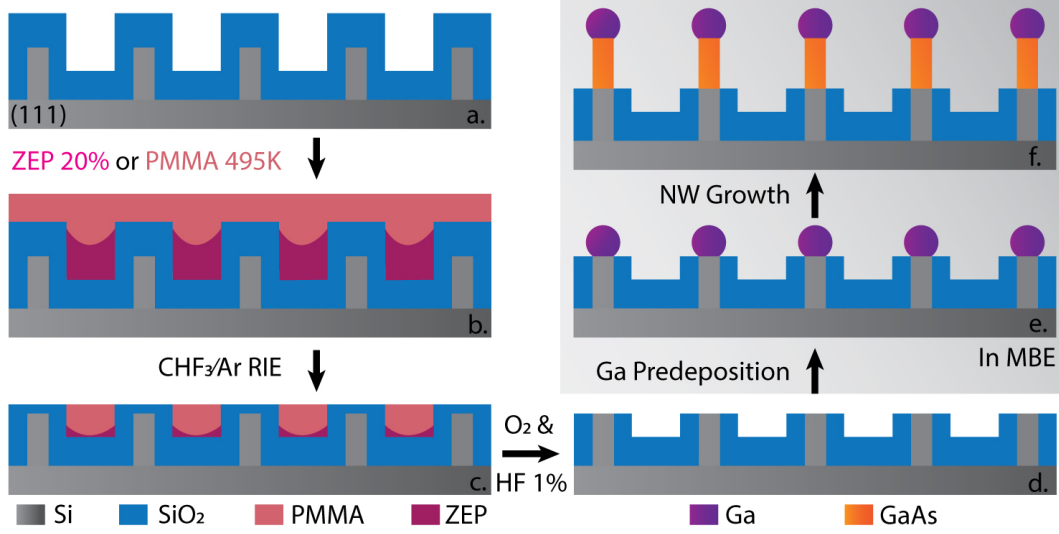


Figure 5.1: *Schematic detailing the fabrication steps of SiO₂/Si(111) pillars for self-catalyzed VLS GaAs NW growth. a. to b. the resist spin-coating process, b. to c. the RIE step and c. to d. the last wet etching before MBE loading. e. shows the very critical Ga predeposition step followed by f. showing NW growth.*

high-yield vertical nanostructure arrays. We showed previously how VLS contact-angle engineering on Si pillars enables vertical $\langle 100 \rangle$ -oriented GaAs growth on Si [92]. In this study we first demonstrate the growth of $\langle 111 \rangle$ -oriented, EBL-patterned SiO₂/Si pillars and discuss the key growth parameters.. We then transfer the concept to displacement Talbot phase-shift lithography (PSL) and grow large-scale NW arrays with a higher local yield of 67% (defined as the number of vertical structure over the total number of nucleation sites). DUV-stepper lithography (DUVSL) will also be discussed as a reliable way for patterning Si (111) wafers for III-V NW growth. Finally, we also examine the possibility of phase engineering by showing both WZ and ZB NWs grown on Si pillars.

5.4 Electron-beam Lithography

In this section, Si substrate preparation is analogous to our previous work[92]: Si pillars[228] of various diameters, ranging from 65nm to 250nm in diameter, are patterned by EBL using the negative resist hydrogen silsesquioxane (HSQ). We etch the pillars by a top-down method using a reactive-ion etcher (RIE) with a fluorine chemistry plasma. After an oxygen plasma and a hydrofluoric acid (HF) cleaning, a dry oxidation is performed at 900°C for a nominal planar thickness of 50nm. Figure 5.1 summarizes the next steps for oxide etching and NW growth: after the oxidation, a polymer layer is spin-coated onto the sample. This

layer is either poly methyl methacrylate (PMMA) 495K or styrene methyl acrylate (ZEP). It is worth noting that Figure 5.1 b. shows both options schematically superimposed; both polymers are never used simultaneously. The meniscus effect represented for ZEP 20% can be experimentally observed and is visible for the reader in the supplementary information. A RIE step is used to partially remove the top oxide, though 5 to 10nm are left on top to avoid damage to the Si by the RIE plasma. A following HF 1% etching allow to uncover the Si core completely.

The sample is then loaded in the MBE for vapor-phase growth. Figure 5.1 e. represents the Ga predeposition step that forms the liquid catalyst droplet necessary for VLS. A constant Ga flux is sent to the substrate and Ga selectively aggregates at the Si pillar core, forming a droplet. The predeposition time, i.e the time during which Ga flux is on, as well as the substrate temperature[182], determine the droplet volume. This step is crucial as the volume of the droplet is one of the determining parameters for the contact angle, defined as β , discussed later in this section.

Figure 5.2 a. is a scanning electron microscopy (SEM) image at a 20° tilt angle of the NWs grown on 135nm nominal diameter Si pillars with a 50nm nominal oxidation. Figure 5.2 b. shows the yield as a function of the pillar nominal diameter for the growth shown in a. named growth 1. It is worth noting that the nominal diameter differs from the real pillar diameter due to EBL dose/development (real size 20% smaller for sizes <100nm diameter and 10% smaller for larger pillars until 300nm diameter) and oxygen incorporation during oxidation (the SiO_2 volume is 2.25 times that of Si[201]). For growth 1, the set manipulator temperature was 610°C. Predeposition time was set at 15min with a Ga beam equivalent pressure (BEP) of 2.1×10^{-7} Torr. We subsequently open As for a V/III ratio of 11 for 30min. Fluxes are then stopped and the substrate is cooled down to 100°C.

Figure 5.2 a. gives us information about the growth mechanisms and growth selectivity; a Ga droplet is visible on top of each GaAs NW, confirming the VLS growth mechanism, and no parasitic growth is visible on the oxide mask, confirming the expected selectivity for NW arrays. Each vertical nanowire starts from a SiO_2/Si pillar, which indicates a good selectivity. NWs possess a slight inverse tapering due to a Ga droplet volume increase during growth[182].

Figure 5.2 b. informs us about the evolution of the vertical yield with respect to

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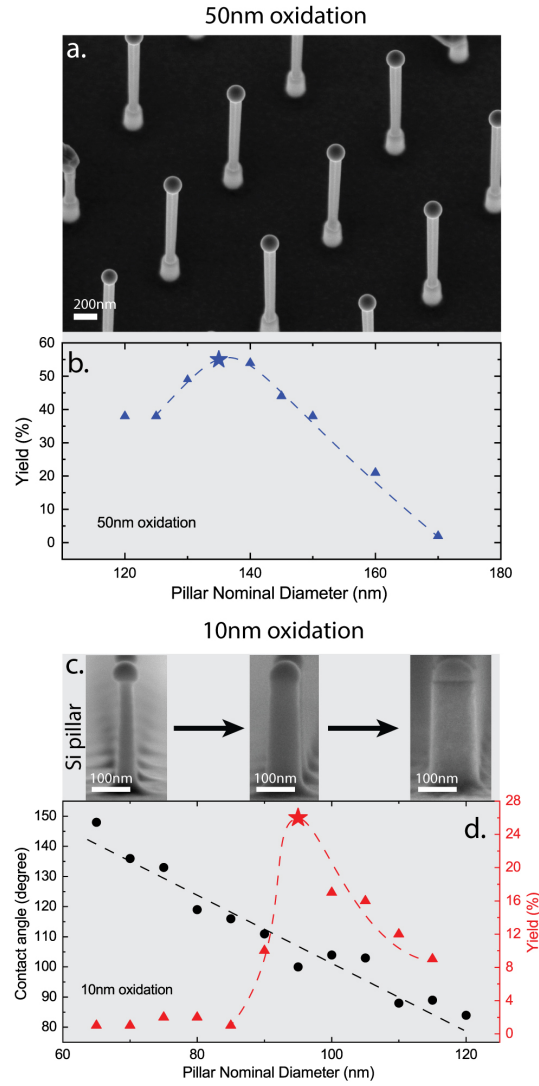


Figure 5.2: Aspects and statistics of a NW growth done on EBL-exposed SiO₂/Si pillars. *a.* SEM image (20° tilt) showing vertical GaAs NWs grown on SiO₂/Si (111) pillars. *b.* Vertical yield in function of pillar nominal diameter. *c.* SEM images showing Ga droplets on top of SiO₂/Si pillars of different nominal diameters. *d.* Contact angle and yield in function of pillar nominal diameter for pillars as shown in *c.* The optimum contact angle is identified as the one showing the best vertical yield.

pillar diameter. The curve shows a global maximum value at $55 \pm 3\%$ for a nominal diameter of 135nm. This value then decreases steadily. We can link this behaviour with the study by Matteini et al.[162] showing that vertical growth is initiated at an optimal β ; as the entire substrate is exposed to the same Ga flux for the same amount of time, we assume the resulting droplet on top of every pillar has the same volume. After a certain volume threshold we also assume that the droplet is pinned at the SiO_2/Si pillar sidewall. Therefore we expect very large β for smaller diameters and lower β for higher diameters. In this context, the vertical yield is maximized when the diameter of the SiO_2/Si pillar permits the optimal β for vertical NW growth at the SiO_2/Si interface.

This assumption is verified by the experiments shown in Figure 5.2 c. and d. The measurements presented correspond to pillars oxidized for a nominal thickness of 10nm. Figure 5.2 c. shows SEM images of SiO_2/Si pillar cross-sections for the same predeposition time as growth 1. The SiO_2/Si pillars' nominal diameters are 65nm, 100nm and 135nm. Figure 5.2 d. shows both β (in black) and NW vertical yield (in red) as a function of the pillar nominal diameter for a second growth with the same conditions used in growth 1. The variation of β shows a linear decrease when increasing the pillar diameter. The maximum vertical yield is obtained for $\beta = 100^\circ$. This value can be compared with the one of Matteini et al. where the optimum β value is 94° . The difference between both values can be explained by the Ga droplet constraint; Matteini et al. experimented on flat SiO_2 surfaces, whereas we use SiO_2/Si pillar. The measurement method also exhibits an error of $\pm 5^\circ$.

So far, we have shown that self-catalyzed VLS growth of GaAs NWs on SiO_2/Si pillars is possible at a good yield. We drew attention to the importance of reaching $\beta = 100^\circ$ for maximizing vertical NWs. As we linked the droplet volume to a given predeposition time, we can expect a variation of the maximum vertical yield in SiO_2/Si pillar diameter by changing the predeposition time. In Figure 5.3 we show the comparative results of three different growths having predeposition times of 10min, 15min and 20min. The rest of the parameters are identical to growth 1. Figure 5.3 a. shows schematics that illustrate the shift in Ga droplet volume for a given β . We observe a shift of the maximum yield to higher SiO_2/Si pillar nominal diameters by increasing the predeposition time, which corroborates the previous assumption. The SiO_2/Si pillar geometry therefore permits to choose a desired NW diameter by tuning the predeposition time, which can be attractive for applications that couple optical/acoustic/microwave modes with NWs for higher

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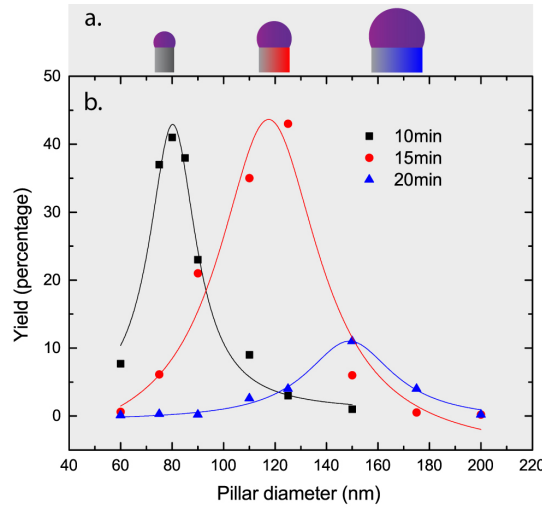


Figure 5.3: *a. Schematics showing the increase in droplet volume with SiO₂/Si pillar diameter at a fixed contact angle. b. Vertical yield in function of SiO₂/Si pillar nominal diameter for Ga predeposition times of 10min, 15min and 20min.*

efficiencies, such as photodetectors[52] or solar cells [139]. Nevertheless we observe a decrease in the maximum yield for a predeposition time of 20min. We explain this by the fact that all three growths share identical conditions (apart from the predeposition time) for the sake of the experiment, and a larger droplet is expected to require a higher As flux for an optimum NW growth.

Coming back to Figure 5.2 b. and d. focusing on the yield curves for 50nm and 10nm oxidation: Comparing the yield curves for 50nm and 10nm oxidation in Figure 2 b. and d., respectively, we observe that, for identical growth conditions, the global maximum stands at different SiO₂/Si pillar diameters. Its value also varies from 55% to 26%. We thus deduce that there is an influence of the oxide thickness on the maximum yield and optimum SiO₂/Si diameter. We develop this hypothesis in Figure 5.4 by showing a comparative study of three different growths identical to growth 1, but on substrates oxidized for nominal thicknesses of 10nm, 30nm and 50nm. The Ga predeposition time and flux being fixed, we assume the Ga droplet volume is identical throughout the growths. We see that we have an increase in optimum SiO₂/Si pillar diameter by increasing the oxide thickness. We link this with the fact that thicker nominal oxidations result in a reduction of the Si core[201]. The Ga droplet volume being constant, $\beta = 100^\circ$ is reached at fixed Si core diameter, i.e larger SiO₂/Si nominal diameter for a higher nominal oxide thickness. This is illustrated in Figure 5.4 a. where the Si core diameter at $\beta = 100^\circ$ for the three different oxidations is schematically illustrated.

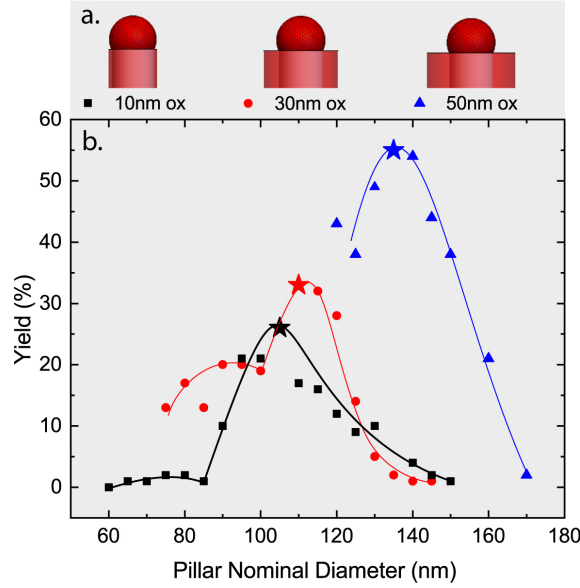


Figure 5.4: a. schematics showing the change in SiO_2/Si pillar nominal diameter for a fixed Si core diameter and Ga dropelt volume. b. Vertical yield in function of the SiO_2/Si pillar nominal diameter for nominal oxidations of 10nm, 30nm and 50nm.

We now focus on the increase of maximum yield with oxidation; Figure 5.4 b. shows that increasing the oxide thickness around the Si core permits a higher yield. We explain this by studying the location of the triple phase line (TPL), i.e the line that simultaneously separates liquid Ga, solid Si and vapor phases[86]. We assume that the ideal droplet configuration for the vertical NW growth is $\beta = 100^\circ$ with the TPL at the SiO_2/Si interface, i.e the inner interface. During predeposition the droplet volume and β increase simultaneously on top of the Si core. After reaching the equilibrium β value for Si, i.e 51° , the droplet pins at the SiO_2/Si interface and swells until reaching the equilibrium β value for SiO_2 , i.e 116° . Further swelling, firstly, moves the TPL away from the Si core by keeping $\beta = 116^\circ$. Secondly, the droplet pins to the pillar side and continues swelling, increasing β to out-of-equilibrium values, as seen in Figure 5.2 d. We believe a thicker oxide permits to stabilize the TPL close to the Si core with β relatively close to 100° .

In order to visualize such droplet evolution, we performed simulations using the software Surface Evolvertm, which permits one to study the shape of liquid surfaces under the effect of different energies and constraints. We computed the equilibrium shape of the liquid and verified the development of the surface energy of the system

Chapter 5. GaAs Nanowires on Si Nanopillars : Towards Large Scale, Phase-engineered Arrays.

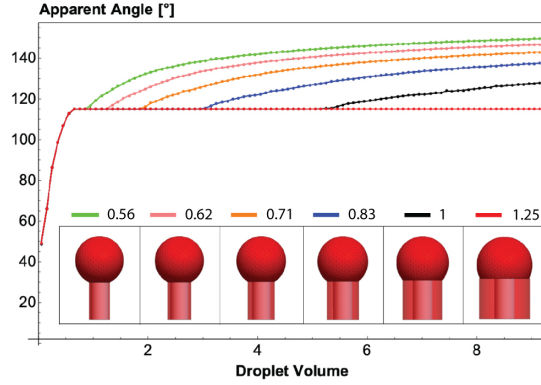


Figure 5.5: Results of simulations done on *surface evolvertm*. The graph shows the droplet apparent angle, i.e contact angle, for d_{SiO_2}/d_{Si} ratios of 0.56, 0.62, 0.71, 0.83, 1 and 1.25.

as a function of the droplet volume. In Figure 5.5 we show six different curves of the apparent droplet angle as a function of the droplet volume for different d_{SiO_2}/d_{Si} ratios, keeping d_{Si} constant, d_{SiO_2} being the oxide thickness and d_{Si} the Si thickness on a pillar diameter. We observe three main evolution regimes: the initial steep increase for very small diameters corresponding to the swelling with the TPL at the SiO_2/Si interface. All d_{SiO_2}/d_{Si} ratios share the same curve in this regime, as d_{Si} defines the critical volume for the onset of the first pinning. The second regime is a plateau at the equilibrium $\beta = 116^\circ$ value for SiO_2 . The length of this plateau depends on d_{SiO_2}/d_{Si} : the thicker the oxide, the longer the plateau. We attribute this evolution to the free increase of the droplet volume with the TPL on the SiO_2 . Therefore this regime covers a larger range of volumes for a higher d_{SiO_2}/d_{Si} ratio. The third regime corresponds to the second pinning at the pillar side wall where β increases again. The simulations are in agreement with experiments, showing that thicker oxides exhibits a contact angle relatively close to 100° for a larger droplet volume window.

This study on EBL pillars permits us to understand the underlying mechanisms and critical parameters for maximizing the NW vertical yield; SiO_2/Si pillars can be larger than 130nm if oxidized properly and the predeposition time chosen accordingly to reach an initial $\beta = 100^\circ$. These criteria open perspectives of large-scale implementation. In fact, pillars larger than 150nm can be produced using industrial lithography techniques like PSL or DUVSL. The next section aims at growing large-scale GaAs NW arrays on $SiO_2/Si(111)$ pillars based on photolithographically defined patterns.

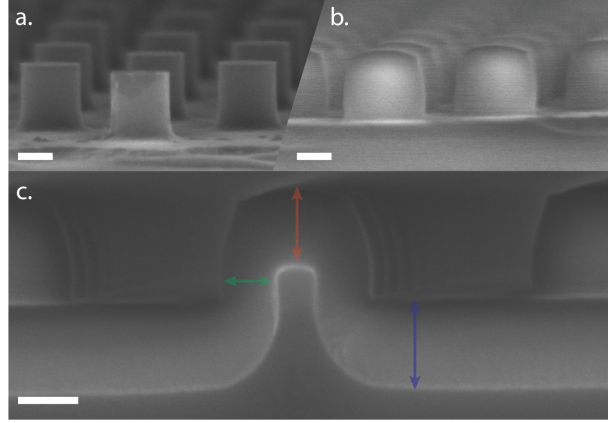


Figure 5.6: SEM images showing a. PSL-exposed Si pillars after RIE, b. after 70nm nominal dry oxidation and c. a cross-section of a SiO_2/Si pillar after 160nm dry oxidation. Scale bar is 100nm.

5.5 Photolithography

The next NW growths were performed on PSL pillars, though we present analogous arrays using DUVSL in the supplementary information. PSL exposure was performed by EULITHAtm using their in-house Phabletm system, which is a displacement Tablot lithography system [205, 238] permitting periodic arrays of 130nm features. The PSL technology allows for exposures lasting few seconds and can be expanded beyond 4 inches wafers. Subsequent RIE steps for anti-reflective coating and Si etching permitted to manufacture arrays shown in Figure 5.6 a. Figure 5.6 b. shows the same array after dry oxidation, nominal planar thickness 70nm at 1050°C. The increase in volume due to oxygen incorporation is visible, as pillars exhibit a 50nm increase in diameter after oxidation. Figure 5.6 c. shows a cleaved SEM cross section of the pillars used for growth, with a nominal dry oxidation thickness of 160nm at 1050°C. This SEM image depicts the influence of geometry on oxidation; the top, side and planar thickness exhibit different values. This is explained by the oxygen incorporation rate and strain build-up inside the SiO_2 for the pillar geometry [120, 150, 36]. On Figure 5.6 c. three coloured arrows indicate the local planar (blue, 125nm), side wall (green, 80nm) and top (red, 150nm) oxide thickness.

The array covers the entire 4-inch Si wafer. The potential for very large-scale NW arrays is clear and presented in Figure 5.7. Figure 5.7 a. shows a 2cm x 2cm chip used for the MBE growth fully covered by a 40% yield array. Local yield variations of $\pm 10\%$ happen between the center and the border due to edge effect

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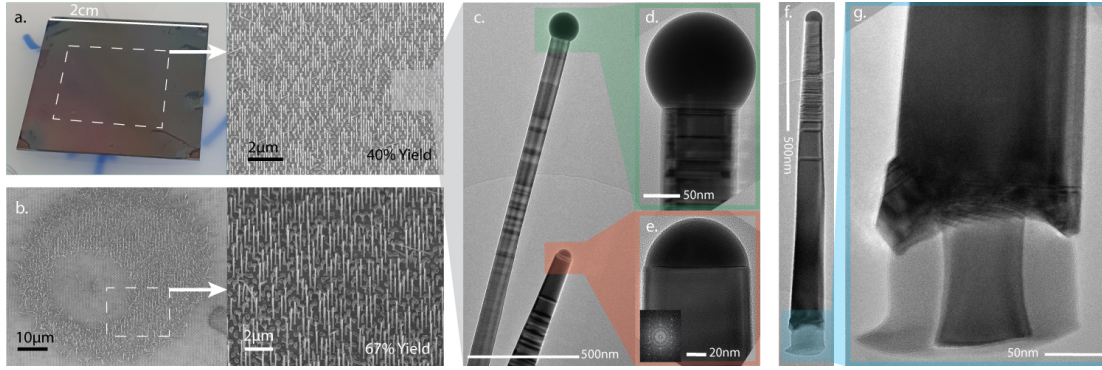


Figure 5.7: Self-catalyzed VLS growth of GaAs NWs on SiO_2/Si (111) PSL pillars. *a.* Large-scale array showing a 40% vertical yield. *b.* Local vertical yield of 67% from a spin-coating comet. *c., d.* and *e.* TEM bright-field images of ZB and WZ nanowires coming from the same SiO_2/Si large-scale array. The WZ FFT is visible. *f.* and *g.* WZ GaAs NW and the SiO_2/Si pillar where it grew from. The pillar's Si core and SiO_2 shell are visible.

during spin-coating[224]. In fact, the spin-coating and the RIE steps depicted in Figure 5.1 between a. and c. are critical for a proper pillar uncovering and droplet configuration. Figure 5.7 b. illustrates this by showing an SEM image of a spin-coating comet, i.e an irregularity in the spin-coated thickness due to an impurity, that locally exhibits a 67% yield whereas the rest of the chip did not give any growth. We believe this unveils the last key parameter in order to obtain 90+% yield arrays : the top SiO_2/Si interface. If we over-etch, the droplet becomes unstable and does not grow into a NW. If we under-etch, Si is still covered by SiO_2 which prevents growth completely. If the spin-coated polymer does not protect the SiO_2 side-walls properly, RIE alters the shape of the pillar and impairs droplet stability. We believe that spin-coating a layer thicker than the pillar's height, planarizing it and controlling precisely the RIE are the key elements to obtain yields comparable to hole-based arrays.

We now focus on the transmission electron microscopy (TEM) measurements presented in Figure 5.7. Figure 5.7 c. to g. show the presence of ZB and WZ NWs simultaneously from the same growth. Whereas this was observed in the past from self-assembled growths [57], it was mainly through stochastic events and did not open perspectives for precise phase engineering. Many studies point out the correlation between droplet contact angle and NW crystal phase[176, 86, 126]. Thanks to contact angle engineering from SiO_2/Si pillar diameter and predeposition time tuning, the pillar geometry potentially permits to obtain either WZ NWs, ZB NWs or both at patterned locations in a deterministic way.

Figure 5.7 d. shows a ZB GaAs NW with its characteristic Ga droplet configuration, i.e $>130^\circ$ contact angle[176]. We can also observe the presence of stacking faults that are frequently observed in $\langle 111 \rangle$ B NWs[254]. Figure 5.7 e. Shows a WZ GaAs NW with the image's fast-Fourier transform (FFT) confirming its phase[57]. Figure 5.7 f. and g. show the interface between a WZ NW and the SiO_2/Si pillar from which it grew. The NW starts from the pillar sidewalls, which we believe is the reason for its WZ phase. In fact, as the Ga droplet un-pins from the SiO_2/Si inner interface and pins to the outer SiO_2 side-wall, for a given volume, the contact angle decreases drastically. This decreased contact angle appears nearly ideal for WZ NW growth, triggering pure WZ NWs. We even observed a short growth on 10nm dry oxide SiO_2/Si pillars where all the vertical NWs appear to be WZ, based on the morphology of the NW and the droplet configuration. This can be seen in the supplementary information.

5.6 Conclusion

This in-depth study of the mechanisms and key elements that constitute vertical self-catalyzed VLS NW growth on SiO_2/Si pillars reveals once again the central importance of the Ga droplet contact angle for reaching high vertical yield, but also for phase-selection. The SiO_2/Si pillar geometry, by allowing a precise and deterministic contact angle engineering, opens perspectives for reliable large-area patterning and freedom in design. Although moderately-high yields were demonstrated here, by the help of simulations we believe we have laid the foundation for very high vertical yield on SiO_2/Si pillars. Moreover, we successfully transferred this NW growth method to use light-based lithography fabrication techniques, more particularly phase-shift lithography. This brings NW arrays one step closer to large-scale implementation for devices.

Methods/Experimental

For EBL pillars : A 2min 600W O_2 plasma in a TEPLATM GigaBatch is done on a 100mm Si wafer for surface activation before spin coating with Dow Corning HSQ 006 and EBL exposure with a Vistectm EBPG5000ES system. The dose used is $2740\mu C/cm^2$ for all the pillar's diameters. The wafer is then developed using a commercial solution of Microposit^R MF^R CD26 for 2 minutes, and rinsed sequentially with water, acetone and propan-2-ol. A 2min 600W O_2 plasma in a

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TEPLA™ GigaBatch is done for further cross-linking the HSQ.

For PSL pillars : After exposure at EULITHAtm using the PHABLEtm system, samples were shipped to EPFL for further processing. Sample is introduced in an SPTS APS plasma etcher where a plasma of CHF_3/O_2 of 20sec is done for anti-reflective coating etching.

The wafer, EBL or PSL, is then introduced in an Alcatel™ AMS200 DSE reactive ion etcher, where a customized recipe using SF_6 and C_4F_8 is used for creating the pillars. A buffered hydrofluoric acid (7:1) bath is then used for 2 minutes to remove any trace of resist. A thermal oxidation is then done at 1050°C for a variable amount of time depending on the desired oxide thickness. The nominal oxide thickness mentioned throughout this study corresponds to the planar thickness obtained for a nominal oxidation time. After the oxide growth, a 50nm Styrene Methyl Acrylate based resist (ZEP) film is spin coated and heated for 2min at 180°C for polymerization. Alternatively, a 170nm thick poly methyl methacrylate (PMMA) can be used. The sample is inserted in an Oxford™ Plasmalab system 80 PLUS using a mixture of SF_6 and CHF_3 at 100W plasma power for 40 seconds to uncover the pillars. 10min of O_2 plasma permits to remove the resist, and a last cleaning involving a 5min acetone bath, a 2min propan-2-ol bath and a 35sec HF bath at 1% concentration makes the sample ready for growth.

The growths are conducted in a DCA™ MBE chamber under a Ga BEP (beam equivalent pressure) of 0.21×10^{-6} Torr and an As BEP of 2.2×10^{-6} Torr for 45 minutes. The samples were characterized by SEM using a Zeiss™ Merlin. NWs were transferred flat onto TEM copper grids and observed using an FEI Talostm microscope for BF and HR images. The reported MBE growth temperatures are estimations of the substrate temperature. With measurements done with an infrared camera on known standard GaAs samples, we estimate a difference of 130°C between the set PID and the real temperature.

Acknowledgements

LG thanks all the MBE team, but also the CMi staff at EPFL without who nothing of this study could be possible. LG thanks EULITHA for the precious help in exposing the (111) Si wafers. We thank the SNF and QSIT for funding the project

5.6. Conclusion

(projects 200021_ 169908 et IZLRZ2_ 163861).

6 Conclusion and Outlook

In this work we studied the integration of vapor-phase III-V nanostructures on Si wafers. For doing so, we designed and implemented a novel patterning method that enabled us to pin the VLS catalyst droplet on top of a top-down Si nanopillar. We were able to engineer the droplet contact-angle, a characteristic that is intimately linked with nanostructure's growth quality and crystalline properties. We started to explore the possibilities of growing vertical nanostructures on Si (100) wafers.

We manufactured nanopillar arrays with diameters ranging from 35nm to 300nm on Si (100) wafers. The surface of the substrate was coated with an oxide layer except for the very top of the pillars. This permitted us to selectively grow VLS nanostructures on Si (100) pillars. By tuning the contact angle and diameter of the droplet, we managed to grow vertical nanostructures on Si (100) that we named nanospades. Nanospades exhibited a unique symmetrical shape and bi-crystal structure. They grow by the VLS mechanism however possess a strong VS side-wall contribution. The optical properties of the nanospades are consistent with their high crystal purity, making these structures viable for the use in integration of optoelectronics on the Si(100) platform.

Therefore, the next step of our project consisted in manufacturing optically-active components from vertical nanospades. We focused on InGaAs quantum wells given the unavailability of the Al cell at this moment of the project. We unveiled the possibility of obtaining square cross-sections by tuning the growth parameters which open perspectives for generating quantum wires at the nanostructure's corners. We successfully grew InGaAs heterostructures on vertical nanospades that emit in the infrared. We also unveiled an emission spatial splitting in the

Chapter 6. Conclusion and Outlook

emission spectra throughout the nanospade. We correlated this characteristic with the unique crystalline structure of the nanospade and show the potential for manufacturing dual wavelength light-emitting diode structures if engineered. Nevertheless we did not manage to improve the nanospade yield further than 20% which we linked with their nucleation mechanism.

And so we decided to implement the Si nanopillar substrate preparation to Si (111) wafers. Our goal was to use the contact angle engineering possibilities to selectively grow wurtzite or zincblende nanowires. Moreover, the Si pillar geometry allows us to shrink-down the size of the patterned Si pillar by oxidation, which enabled us to pattern large areas using photolithography techniques such as phase-shift lithography and DUV stepper lithography. We first identified the key parameters for obtaining a high VLS GaAs nanowire yield on Si (111) pillars using electron beam lithography. We demonstrated the possibility of tuning the nanowire diameter by changing the droplet catalyst's volume and the impact of the oxidation on the vertical yield. We then manufactured Si pillars using photolithography techniques and grew large-scale GaAs nanowire arrays.

Phase-engineered, wafer-scale, vertical nanowire arrays : what a grail for the nanowire community ! These perfect rows of nanowires, standing straight and improving solar cells performance. It was what motivated us, and I think our study proves that the Si pillar geometry has what it takes to make this dream come true : the droplet pinning, the contact angle and size engineering, and the up scalability.

There are still many aspects that need to be improved : I would start by the clean room process flow, where a few key elements are critical for improving the yield further.

- The pillar oxidation : As seen in chapter 3, the oxidation temperature is critical for a good control over the pillar's oxide thickness. Therefore, accessing an oven that is very stable in temperature and very pure is of uttermost importance.
- The pillar uncovering : The Si/SiO_2 interface needs to be flat and well-defined. Several polymer spin-coating approaches were explored for RIE uncovering (step f. in figure 3.1 , and step b. in figure 5.1), and I believe that planarization and/or reflow for obtaining a perfectly flat (roughness rms in the nm range) layer before RIE is crucial.

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- The pillar height : Oxidation, but also MBE growth might vary depending on the pillar height. This aspect was not thoroughly studied in this thesis and holds potential for playing with precursor's diffusion and nanowire shape.

After addressing these technical points, I believe the Si pillar platform will be ready for large-scale integration of III-Vs on Si. The connection between PSL/DUV stepper and vapor-phase growth opens the doors of device fabrication and product design. The possibility of producing low-cost pillar arrays also opens perspectives in nanoimprint lithography, where stamps can be inexpensively produced and re-used, dropping even more the production price. This workflow also permits to experiment with horizontal nanowire growth : as an example, [110]-oriented Pd-catalyzed InAs nanowires have been demonstrated on GaAs[248]. It is possible to extend this concept and deposit Pd droplets on horizontal etched, oxidized and uncovered Si (100) "membranes" exposed by DUV stepper lithography. This could open perspectives for high-mobility InAs transistors directly on Si (100).

We can also imagine transferring the knowledge acquired in MBE growth to the use of an MOVPE chamber for a next step towards the semiconductor industry. The growth of other materials such as InAs, GaN or InP also holds great perspectives.

To summarize, this work was mainly about pillars. From design to fabrication. From small-scale to large-scale. From oxidation to growth. This project aimed at demonstrating the potential of a novel patterning approach in the field of nanostructures. Even if we explored many aspects of the pillar geometry, I feel like we barely scratched the surface. I would have never thought possible to spend four years and a half on these little Si cylinders and have so much fun doing it. It truly shows that science has no bottom and that there is so much we still ignore.

A Paper Supplementaries

A.1 Light emitting InGaAs Heterostructures on Si (100) integrated GaAs Nanospades

A.1.1 TEM Study of GaAs/InGaAs/GaAs NSPDs

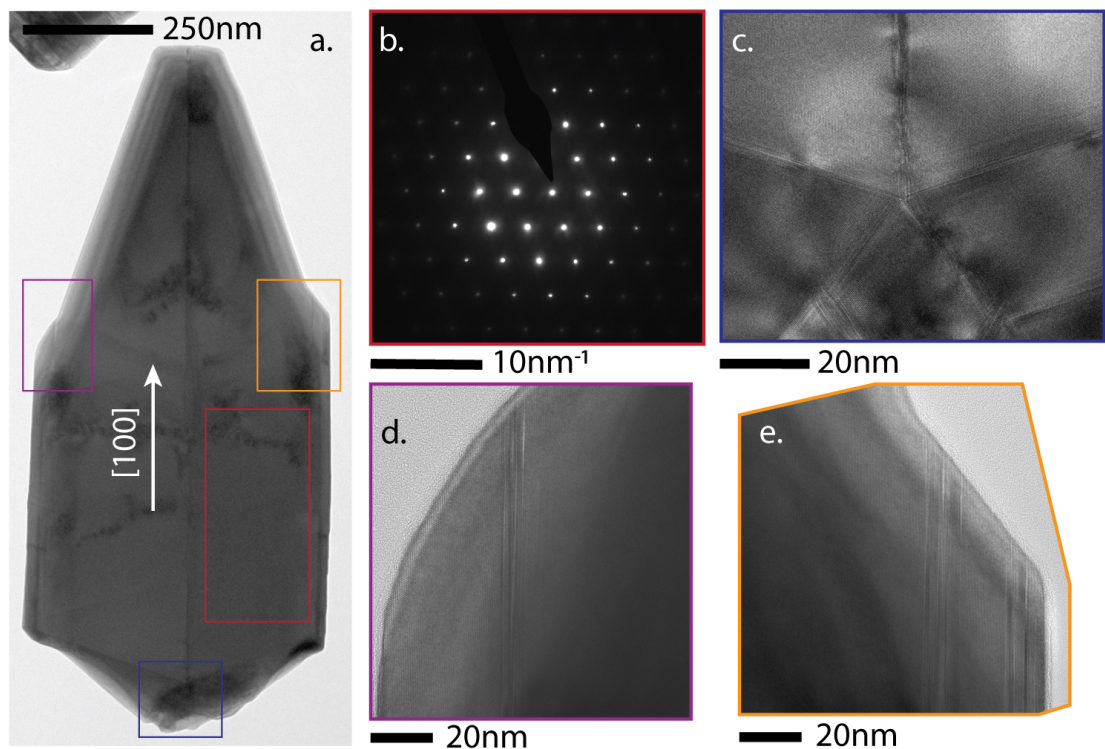


Figure A.1

Figure A.1 shows the high-resolution transmission electron microscopy (HRTEM)

Appendix A. Paper Supplementaries

study of a nanospade (NSPD) grown at the following conditions : A GaAs stem NSPD is grown at higher temperature (610degC) and lower As partial pressure (1.5e-6 Torr) for a V/III ratio of 11 until reaching a length of 1.5µm. The As partial pressure is then raised up to 1.5×10^{-6} Torr, Ga shutter closed for 30 minutes in order to stop the VLS growth process. Temperature is dropped to 390°C in order to enter a VS growth regime. Then a first GaAs shell is grown, forming the rectangular vertical facets (that can be seen on figure A.1a.). Pure InAs is sent for a relatively short time with a decreased As partial pressure of 1.5×10^{-6} Torr and a V/III ratio of 11, before re-initiating a GaAs capping shell growth.

Figure A.1a. shows bright-field TEM (BFTEM) image of the full NSPD. The central twin is visible crossing the structure at the center. We also observe the vertical section of the side-walls on both sides. Figure A.1b. shows the diffraction pattern of the right side (red square in a.) confirming the high crystalline quality of the NSPD. Figure A.1c. shows the penta-twin located at the base of the NSPD (dark blue square in a.) where the central NSPD twin can be seen at the top. Figure A.1d. and e. shows respectively the left and right end of the vertical sections of the sidewalls (purple and dark yellow squares). We can see vertical stacking faults coming from the VS growth step (shell growth). As stacking faults are commonly $\langle 111 \rangle$ -oriented in GaAs and InGaAs it shows the (111) orientation of the sidewalls' vertical sections. Figure 4.3 of the main manuscript represents with an atomic model the (111) orientation of these sidewalls.

A.1.2 RT CL of NSPDs with shells grown at 430°C

Figure A.2 shows the room-temperature cathodoluminescence (CL) results on NSPDs with shells grown at 430°C. We can see the scanning electron microscope (SEM) image, taken in the CL setup, of the NSPD. Figure A.2 a. shows the average spectra over the whole structure, showing a rich signal between 850nm and 1010nm. Figure A.2 b. shows the panchromatic emissions for different wavelength ranges. We observe localization of emission throughout the structure, which is consistent with In diffusion and accumulation at defects.

A.1.3 RT CL of NSPDs with shells grown at 420°C

Figure A.3 shows the cathodoluminescence (CL) results on NSPDs with shells grown at 420°C. Like the results presented for the NSPD with shell grown at 430°C, we can see the scanning electron microscope (SEM) of the structure. Figure

A.1. Light emitting InGaAs Heterostructures on Si (100) integrated GaAs Nanospades

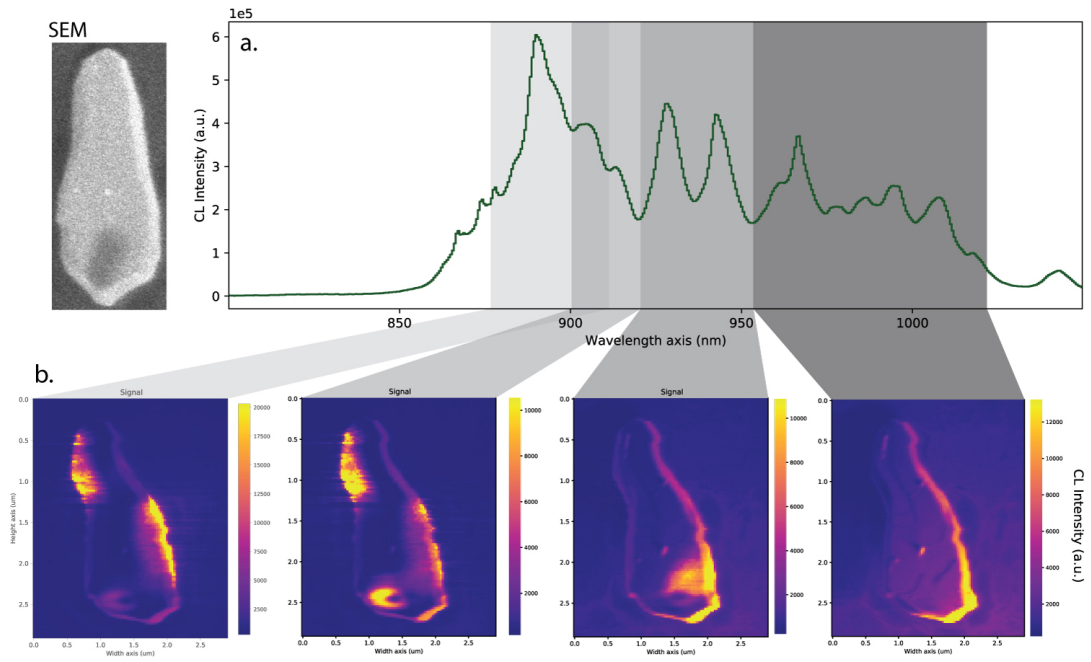


Figure A.2

A.3 a. shows the average spectra over the whole structure, showing a rich signal between 850nm and 1010nm. Figure A.3 b. shows the panchromatic emissions for different wavelength ranges.

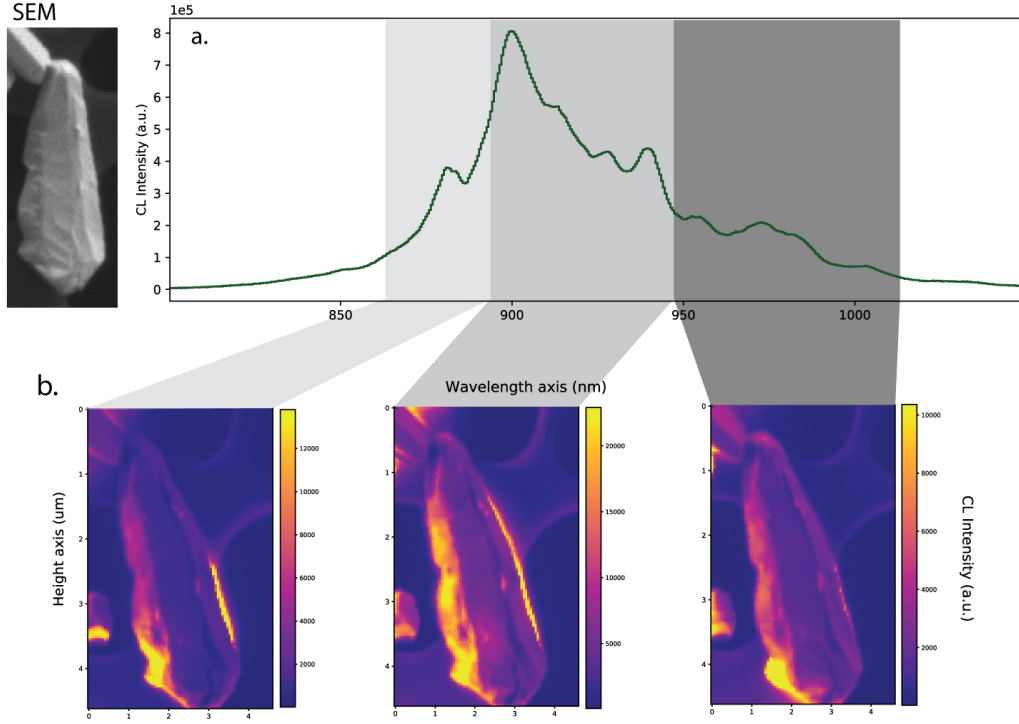


Figure A.3

A.2 GaAs Nanowires on Si Nanopillars : Towards Large Scale, Phase-engineered Arrays.

A.2.1 Atomic Force Microscopy of Spin-coated Pillars

Figure A.4 Shows phase-shift lithography (PSL) SiO_2/Si pillars before (a.) and after (b.) spin-coating of ZEP 20% dilution in Anisole at 2500rpm. This step appears to be important for the correct opening of the SiO_2/Si pillars : In fact, the observed meniscus prevents the exposure of the sidewalls to the reactive ion etching (RIE) plasma, permitting to obtain a flat and directional etching. Nevertheless this was observed to be true only for relatively short etchings (<5min). For long etchings, i.e long enough to etch the ZEP on the side-walls, we found that spin-coating a thick layer of poly methyl methacrylate (thicker than the SiO_2/Si pillars height) and etching down with two RIEs : a first O_2 plasma for the top PMMA and a second CHF_3/Ar plasma for the oxide etching, yields better results.

Knowing the pillars height from subfigure a. and measuring the step height in subfigure b. we can extrapolate the spin-coated ZEP thickness. For those spin-coating parameters the value is close to 30nm.

A.2. GaAs Nanowires on Si Nanopillars : Towards Large Scale, Phase-engineered Arrays.

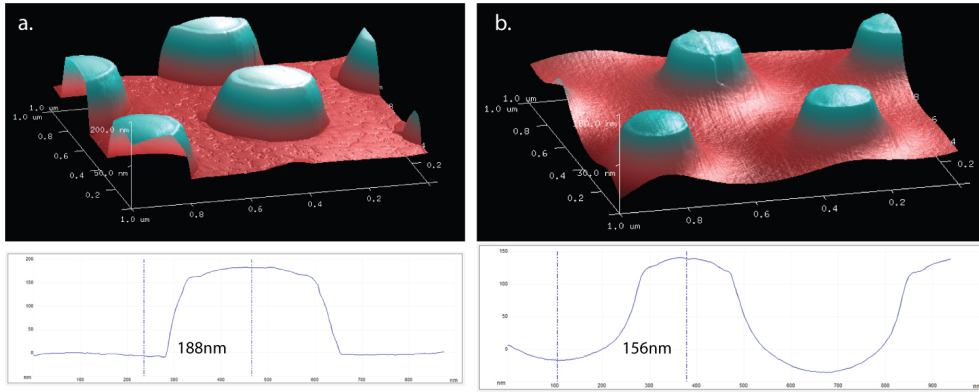


Figure A.4: AFM data of *a. bare SiO₂/Si pillars and b. after ZEP spin-coating.*

A.2.2 DUV Stepper Lithography of SiO₂/Si Pillars

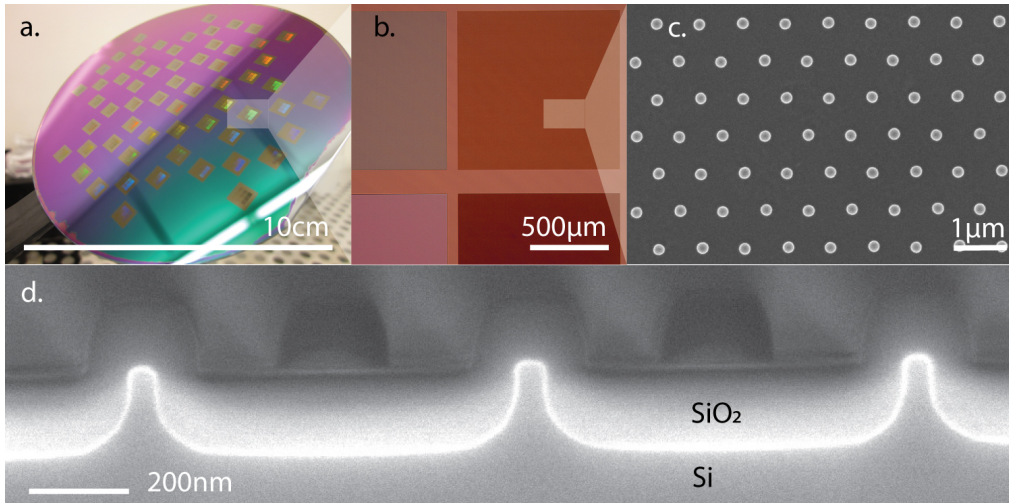


Figure A.5: Overview of the SiO₂/Si pillars fabricated by DUV stepper lithography. *a. Photograph of the wafer, b. optical microscope image of an array, c. Top view SEM image of a pillar array and d. cross-section of the oxidised SiO₂/Si pillars.*

Figure A.5 shows an overview of the SiO₂/Si pillars fabrication using deep-ultraviolet stepper lithography (DUVSL). They are exposed using an ASMLtm PAS 5500/350C system and developed using a Süss Microtechtm ACS200 gen3 system. The resin used is M108Y to a thickness of 140nm with a buffered anti-reflective coating (BARC) of 40nm. The dose used is 14.5μC/cm² at a z = -0.2μm focus. Sample is then introduced in an SPTS APS plasma etcher where a plasma of CHF₃/O₂ of 34sec is done for BARC etching. The wafer is then introduced in an AlcatelTM AMS200 DSE RIE, where a customized recipe using SF₆ and C₄F₈ is used for creating the pillars. An oxygen plasma is performed in a Teplatm GigaBatch system for stripping the resist/BARC. A buffered hydrofluoric acid (7:1)

Appendix A. Paper Supplementaries

bath is then used for 2 minutes to remove any trace of resist/BARC. A thermal oxidation is then done at 900°C for a variable amount of time depending on the wanted oxide thickness.

Subfigure a. shows the full 100mm wafer after exposure. Each square represents several mm-scale arrays of different diameters and pitches. Subfigure b. is a microscope image showing four different arrays which periodicity changes, altering their colours. Subfigure c. is an SEM image of 190nm Si pillars after RIE. Subfigure d. shows an SEM cross-section of a cleaved SiO_2/Si pillar array. As seen the arrays are highly uniform and suitable for VLS growth of GaAs NWs. Moreover the freedom in design open perspectives for fabricating non-periodic arrays, contrarily to phase-shift lithography (PSL) techniques presented in our main study.

A.2. GaAs Nanowires on Si Nanopillars : Towards Large Scale, Phase-engineered Arrays.

A.2.3 Wurtzite Nanowire Array from SiO_2/Si Pillars

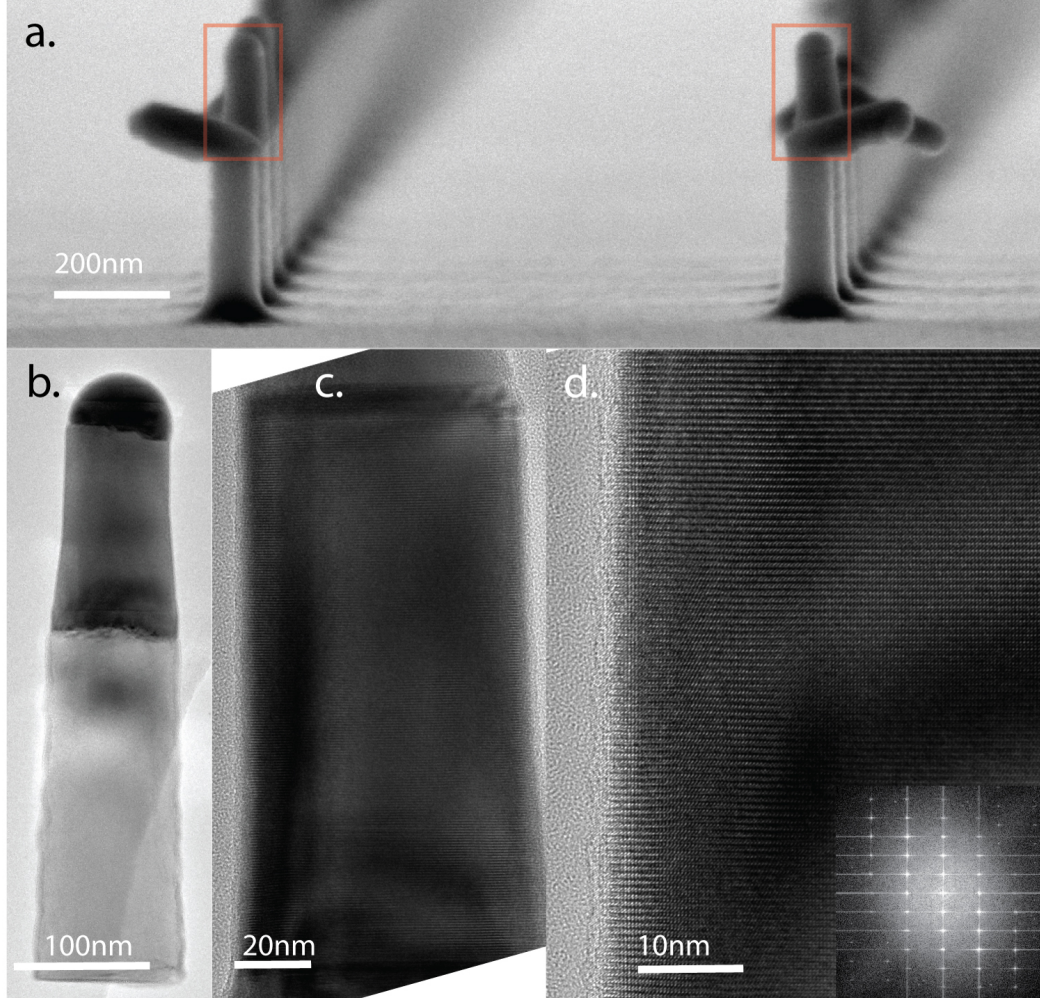


Figure A.6: SEM and TEM images showing self-catalyzed VLS GaAs NW growth on SiO_2/Si 10nm oxidised. a. SEM crosssection image shows the 105nm nominal diameter array with tilted and vertical NWs. b. TEM BF image of a GaAs NW along with the SiO_2/Si pillar it grew from. c. and d. HRTEM images of a vertical NW on a SiO_2/Si pillar showing pure defect-free WZ structure. The FFT confirms the WZ phase.

Figure A.6 shows an overview of MBE growth on 10nm nominally-oxidized SiO_2/Si EBL pillars. The NWs shown here are from 105nm nominal diameter pillars array. The growth parameters are analog to growth 1 presented in our main study. Subfigure a. Shows a cross-section view of the 105nm nominal diameter array after GaAs VLS NW growth. We can see that we have tilted and vertical nanowires. The contact angle appears to be close to the wurtzite (WZ) stable one during growth. Subfigure b. shows a TEM micrograph of a transferred GaAs NW with its base

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SiO₂/Si pillar. The oxide is hard to see given its very low thickness. subfigure c. and d. show HRTEM images of a vertical NW on Si pillar, showing a defect-free WZ crystal structure. Subfigure d. also shows the image FFT confirming the WN crystal structure.

From SEM characterization, all the vertical NWs were exhibiting morphological characteristics analogue to the ones observed by TEM. This leads us to think that all vertical NW from this growth are WZ, confirming the phase-engineering potential of the *SiO₂/Si* pillar patterning method.

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Education

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- 2014–2016 **Master in Material Science and Engineering**, *Ecole Polytechnique Fédérale de Lausanne. Courses aimed on Semiconductors, Thin films, Epitaxy, Photovoltaic Devices..*
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Technical skills

Epitaxy	Clean Room Processes	Metrology	Simulation
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