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Hybrid Modular Multilevel Converter Design and Control for Variable Speed Pumped Hydro Storage Plants

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ABSTRACT Hybrid modular multilevel converter control and design for pumped hydro storage plants is presented, addressing application-specific shortcoming of conventional back-to-back half-bridge modular multilevel converter: high common-mode-voltage machine stress. Common-mode-voltage-free operation in the entire or partial frequency range is enabled by variable DC link voltage control, through introduction of minimal full-bridge submodule share in hybrid active front-end converter stage. The developed generalized converter design approach for arbitrary DC link voltage range operation and additional internal energy balancing control layers enable down-to-zero DC voltage control. The results are verified through high-fidelity switched-model simulations of 6 kV converter, with 10/6 ratio of full-bridge to half-bridge submodules in active front-end. The analyzed hybrid active front-end stage benefits from lower converter losses for equal machine operation flexibility compared to full-bridge design, while trade-off between grid-side power factor range and full-bridge submodule share is offered within the design stage. Compared to the state-of-the-art, zero-to-rated DC link voltage operation is possible at lower full-bridge submodule share (62 % against 75 %), at the penalty of reduced grid-side power factor. Alternatively, operation at higher full-bridge submodule share (62 % against 50 % existing solution) enables grid-side reactive power support over wide speed range, without branch current overload.

INDEX TERMS Hydroelectric power generation, modular multilevel converter, retrofit.

I. INTRODUCTION

Fossil- and nuclear-fuel dominated power systems of today are seeing persistent increase in share of photo-voltaic and wind generation capacities [1], driving them slowly but imminently to a Renewable Energy Sources (RES)-dominated scenario of the future. Historically, Pumped Hydro Storage Plants (PHSPs) were built as peak-shaving units, operated by absorbing excessive energy from base generating units at periods of low demand, typically during the nighttime, and storing it in the form of potential energy in the upper reservoir. During periods of high demand, typically during the daytime, a PHSP would be operated in turbine mode, providing back the energy to the grid, while base generating units could keep optimal output power levels. In the upcoming frame of high non-dispatchable RES share, however, energy storage units of higher dynamics are required to counter-weight the stochastic nature of such sources, otherwise RES balancing issue will certainly arise [2]–[4].

Compared to fixed speed units, power-converters-enabled variable speed PHSPs offer higher dynamics, higher overall efficiency [5], [6], and additional ancillary services, e.g. power-frequency regulation in both pumping and generating modes. Voltage (6 kV to 21 kV) and power ratings (80 MVA to 400 MVA) of machines found in typical large PHSPs, along with power electronics converter topologies- and components-imposed limitations, have so far favored Doubly-Fed Induction Machine (DFIM) to Converter-Fed Synchronous Machine (CFSM) solution. Requiring a rotor-side converter rated at a fraction of machine power, unlike full-size stator-side converter in CFSM, DFIM established as the dominant variable speed PHSP technology

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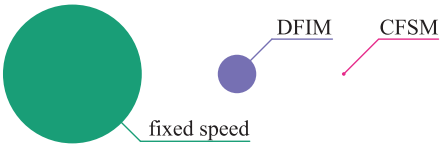

FIGURE 1. Share of variable speed DFIM (≈10 GW) and CFSM (0.1 GW) units larger than 100 MW, compared to fixed speed PHSP capacity (≈160 GW) [8], [9].

to date, with only one large CFSM-based variable speed unit in operation (Fig. 1) [7]–[9].

Retrofit of existing fixed speed PHSPs to variable speed CFSM-based operation, considering that readily deployed fixed speed units are to date the most established grid-scale energy storage, represents an extraordinary potential (Fig. 1). CFSM plant offers higher dynamics through faster pump/turbine switch-over without de-watering, relying on rated torque at all operating speeds. Further, grid-side dynamics during transients is decoupled from the hydraulic system and only limited by the fast current control loops. Superior low-voltage ride-through behavior compared to DFIM units is well-known, while no change to the machine and hydraulic circuit is necessary. Increased efficiency through operation at the optimal speed regarding hydraulic system [5], as well as higher revenue from ancillary service market participation add further value [10], [11].

Unlike monolithic converter topologies with limited scalability and thus additional voltage-matching transformers and paralleling strategies requirements [7], Modular Multilevel Converter (MMC) is a good retrofit candidate considering PHSP machine ratings, owing to inherent redundancy and straight-forward scalability to power/voltage range of interest [9], [10]. MMC was first developed for and deployed in high-voltage DC inter-ties, where typically low-loss Half-Bridge (HB) Submodules (SMs) are utilized as converter building blocks [12], [13]. In PHSP AC-AC application of interest, either a matrix-like Direct-MMC [14], or a back-to-back (Indirect-)MMC can be considered [10]. While Direct-MMC is superior for new installations with differing machine- and grid-side frequencies, Indirect-MMC is more suitable for similar frequency values [14], [15]. As retrofit ideally presumes keeping the original machine, Indirect-MMC is the preferred topology (Fig. 2).

Low frequency operation of the machine-side MMC is coupled with excessively high capacitor voltage ripple in its SMs. One possible solution to the problem relies on Common Mode (CM)-voltage injection [16], [17]. While such Variable Speed Drives (VSDs) are in use [18], the additional CM voltage-imposed stress, ranging up to rated winding voltage, may prove prohibitively high when retrofitting PHSPs machines originally designed for sine-wave grid supply [19], [20]. Reduction of average SM voltage at lower-than-rated frequency, thus allowing for higher capacitor voltage ripple, has been proposed in [21], enabling CM-voltage-free operation down to 30 % of rated frequency.

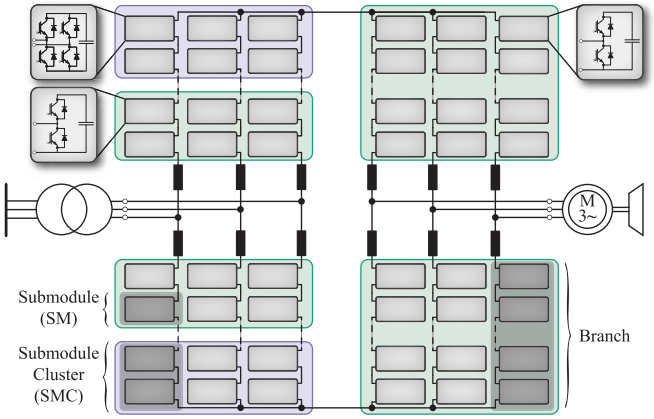

FIGURE 2. Back-to-back MMC solution to retrofit of existing PHSP to variable speed operation, without machine modifications. Machine-side is realized as a standard HB MMC, while active front-end stage is an H-MMC based on a mix of FB and HB SMs. Internal and higher-level control of both stages are presented, while H-MMC stage design is also derived.

CM-voltage-free operation can be performed by varying the DC link voltage with output machine frequency, in the range $(0, V_{DC,n}]$, $V_{DC,n}$ denoting rated DC voltage value [22], [23]. However, HB-based MMC Active Front-End (AFE) operation is limited to a narrow band around $V_{DC,n}$, owing to fixed grid-side AC voltage amplitude.

Reduced DC link voltage operation of MMC has been well studied in high-voltage DC applications, where boosted AC-side modulation index, which to good extent may be equalized with reduced DC voltage operation, is considered. Likewise, DC fault handling and DC link voltage reduction under certain operating conditions attract significant researchers' interest. Design of an H-MMC enabling both reduction of DC link voltage down to zero and DC fault handling capability, comprising 2/3 of FB SMs per branch, has been presented in [24], along with a control approach relying on a capacitor sorting algorithm. Starting from operation at rated DC voltage and unity modulation index, the converter can be operated at unity power factor down to $0.5V_{DC,n}$, while further voltage reduction requires a linear decrease of power factor down to zero. A thorough high-voltage-DC-optimized design approach has been carried out in [25]. The proposed method also relies on capacitor sorting algorithm, and offers reduction of DC link voltage down to $0.5V_{DC,n}$ at theoretical FB/HB SM ratio of 1/4. However, further reduction down to zero, discussed for unity power factor, requires approximately 80% of installed SMs being FB. While also offering negative DC voltage operation, this feature is not of interest in MMC VSD applications. Variable DC link voltage operation of H-MMC fed from a line-commutated converter is assessed in [26], for DC link power flow control. SM energy balancing is performed through modified sorting algorithm, where FB SM voltage measurements are added a calculated offset to alter insertion preference and ensure energy balance. Operation down to $0.4V_{DC,n}$ at unity power factor is achieved, with 50 % FB SM share, and without additional circulating current

injection. Further control actions to achieve down-to-zero DC link voltage range have not been addressed. Starting from H-MMC with FB/HB ratio of 2/3, branches SMs charged to a total of $1.5V_{DC,n}$ each, and operating at boosted AC modulation index, an energy balancing method based on additional fundamental frequency reactive circulating current injection is introduced in [27] and [28]. Capacitor voltage balancing at boosted modulation index has been assessed in [29] utilizing a coupling of additional second-order SM-level voltage component and second-order circulating current for energy transfer. Influence of modulation index, power factor and FB/HB ratio on converter operation have been addressed. H-MMC balancing at reduced DC link voltage operation has been performed utilizing additional second-order circulating current injection in [30]. Additional current component ensures bipolar branch current in all operating areas and, in turn, proper balancing of HB even at reduced DC link voltage and high power factor values. Asymmetric H-MMC for variable DC link voltage operation has been presented in [31] for high-voltage DC power flow control. However, no details on capacitor voltage balancing at unequal upper- and lower-branch inserted DC voltage component were provided. H-MMC operation at boosted AC modulation index has as well been studied for medium-voltage DC applications. In such domain, due to lower SM-count and inadequacy of nearest-level modulation typically found in high-voltage DC [32], a form of Phase-Shifted Carrier (PSC) modulation with reference modification has been proposed in [33], along with an additional capacitor sorting algorithm.

Operation at variable DC link voltage has also been studied specifically with VSD application in mind. An extreme case utilizing a FB MMC as AFE is presented in [22] and [23], enabling $[-V_{DC,n}, V_{DC,n}]$ operating range while doubling AFE stage losses. In [34], constant DC voltage is chopped by a DC link switch, to achieve desired average V_{DC}, while in [35] further SM capacitance reduction through decreased SM average voltage operation has been studied. As converter operation relies on the newly introduced switch, high reliability based on MMC redundancy is compromised. H-MMC AFE with all-FB upper branches and all-HB lower branches is presented in [36], demonstrating DC link voltage reduction down to practically zero. Non-equal insertion voltage references of FB- and HB-based branches call for non-equal AC current component share among the branches, where at certain operating frequencies, sum of AC current component in branches is a couple of times higher than the grid (output) current. At unity power factor there is little current overload in certain operating points, due to grid current being proportional to machine frequency. However, provision of reactive energy at lower-than-rated machine frequency, e.g. at 80% as a possible lower range for PHSP operation, would drive some of the converter SMs into a more prominent over-current state.

Variable DC link voltage operation of H-MMC, comprising a mix of HB and FB SMs within each branch, has also been addressed in [37], with VSD application in mind. DC voltage reduction and consequently CM-voltage-free operation have been achieved down to 50 % of rated DC voltage and machine speed, respectively. Below this speed, CM voltage injection, albeit of lower amplitude than with rated DC voltage, has still been used. The method enables arbitrary grid-side power factor over the entire operating range, at reduced FB SM share compared to all-FB-based converter. However, SMs have to be sized for higher current rating compared to conventional MMC.

The reviewed references readily offer variable DC link voltage operation at reduced FB SM share. In methods that require no additional balancing current capacity, the penalty comes in the form of higher FB SM share. Methods utilizing the theoretical minimum of 50 % of FB SMs require non-negligible additional balancing current capacity. Between the two lies the opportunity for improvement, which is where this paper aims to provide contribution.

This paper explores the design and control of H-MMC-based AFE operated at a variable DC link voltage level, to achieve CM voltage-free machine-friendly variable speed PHSP operation crucial for the retrofit applications. AFE stage comprises branches with a mix of HB and FB SMs, grouped into Submodule Clusters (SMCs) (see Fig. 2).

The main contributions of the paper are: 1) a control method for H-MMC AFE that enables variable DC link voltage operation down to zero volts, at equal upper- and lower branches loading, using a standard PSC modulation method, without sorting algorithms; 2) a design approach for selection of the required FB/HB SM ratio for an arbitrary DC voltage reduction range, along with resulting attainable operating area; 3) a CM voltage-free, machine-friendly control of the proposed back-to-back MMC. In whole, the paper offers a retrofit solution that can exploit the existing fixed speed PHSPs capacity through increased flexibility and efficiency at variable speed operation.

The rest of the paper is organized as follows. Section II identifies the machine-side stage operating requirements at CM-free variable DC voltage operation. In addition, H-MMC AFE internal energy dynamics is analyzed, considering variable DC voltage operation. Section III introduces operating principles of the proposed H-MMC, followed by design for the desired DC voltage reduction range. Internal H-MMC control approach, comprising conventional MMC control, augmented by additional H-MMC-specific control layers, is presented in Section IV. Section V introduces the applied system-level control. Results of characteristic test scenarios, obtained through high fidelity simulations, are provided and discussed in Section VII. Obtained performance, as well as limitations, of the method are discussed and compared against relevant published work in Section VIII. The final Section outlines the conclusions.

II. VARIABLE DC LINK VOLTAGE OPERATION

CM voltage-free low frequency operation of a machine-side MMC is enabled through variable DC link voltage operation [23], [34]. In the VSD application, only positive DC

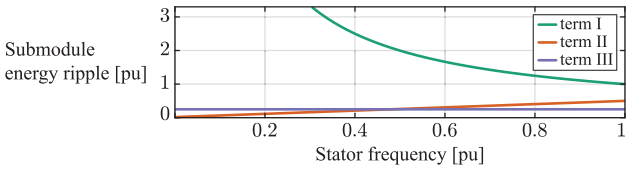

FIGURE 3. Frequency dependence of the SM energy ripple components (3). The first term is dominant in low frequency region.

voltage values are of interest, defined henceforth by the factor $k_{\mathrm{DC}} \in (0, 1]$ such that $V_{\mathrm{DC}} = k_{\mathrm{DC}} V_{\mathrm{DC,n}}$, as briefly analyzed hereafter.

A. LOW-FREQUENCY ENERGY DYNAMICS

Inserted upper- and lower-branch voltages and branch current are described by (1) and (2), respectively, assuming an ideally balanced converter, while neglecting phase index.

$$v_{\{\mathrm{p,n}\}} = \frac{k_{\mathrm{DC}} V_{\mathrm{DC,n}}}{2} \mp \frac{m_s V_{\mathrm{DC,n}}}{2} \cos(\omega_s t + \theta_s) \tag{1}$$

$$i_{\{\mathrm{p,n}\}} = \frac{I_{\mathrm{DC}}}{3} \pm \frac{\hat{i}_s}{2} \cos(\omega_s t + \varphi_s) \tag{2}$$

The following notation is adopted: m_s – modulation index, ω_s – AC-side angular frequency, θ_s – AC-side voltage angle, $\hat{i}_s$ – AC-terminal current amplitude, φ_s – AC-side voltage-to-current displacement angle, I_{DC} – DC-terminal current amplitude.

Starting from (1)-(2), SM energy ripple components are obtained. Positive (upper) branch is observed.

$$\tilde{w}_{\mathrm{SM}} = \frac{1}{N_{\mathrm{SM}}} \int v_{\mathrm{p}} i_{\mathrm{p}} \, \mathrm{d}t = \frac{k_{\mathrm{DC}} V_{\mathrm{DC,n}} \hat{i}_s}{4 N_{\mathrm{SM}}} \left\{ \underbrace{\frac{1}{\omega_s} \sin(\omega_s t - \varphi)}_{\text{(I) decreases with } \omega_s} \right.$$
$$\left. \underbrace{- \frac{m_s^2}{2\omega_s} \cos(\varphi) \sin(\omega_s t)}_{\text{(II) increases with } \omega_s} \underbrace{- \frac{m_s}{4\omega_s} \sin(2\omega_s t - \varphi)}_{\text{(III) constant}} \right\} \tag{3}$$

At the rated DC link voltage ($k_{\mathrm{DC}} = 1$), assuming constant-torque variable speed operation of the machine, $\hat{i}_s \approx$ const, while $m_{\mathrm{s}} \propto \omega_{\mathrm{s}}$. Consequently, energy oscillations increase with frequency decrease, as visualized in Fig. 3 where all three components of (3) are drawn. This calls for either very high SM capacitance or additional control action based on CM voltage injection [16]. On the other hand, varying the DC link voltage with machine-side frequency, $k_{\mathrm{DC}} V_{\mathrm{DC,n}} / \omega_s =$ const, ensures constant SM capacitor energy ripple without CM voltage injection, usually prohibited in retrofit applications.

B. AFE INSERTION VOLTAGE REQUIREMENTS

Controlled operation of PHSP down to zero speed with no CM voltage injection requires DC voltage reduction range of $k_{\mathrm{DC}} \in (0, V_{\mathrm{DC,n}}]$. Under normal operating conditions, grid AC voltage amplitude is found in a grid-code-defined narrow band around rated value. Following (1) for $m_{\mathrm{s}} = 1$, provision of lower-than-rated DC link voltage ($k_{\mathrm{DC}} < 1$) by the AFE imposes negative branch insertion voltage references, which cannot be achieved by an HB-based converter. This calls for consideration of H-MMC as AFE solution.

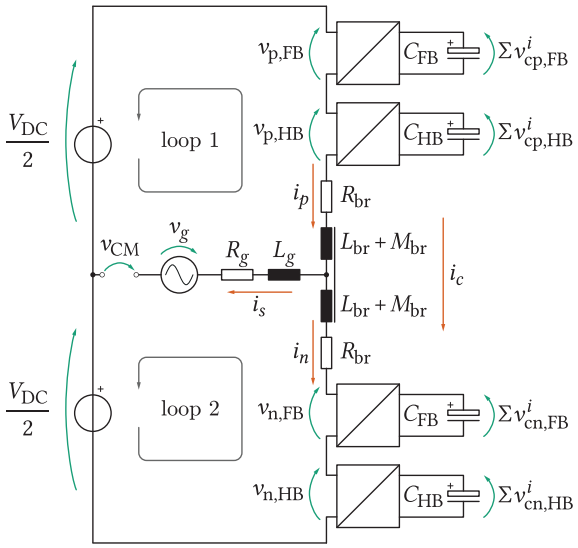

FIGURE 4. Equivalent circuit of one phase of a hybrid MMC, where all the SMs are presented as two units, being equivalent to the clusters of the installed FB and HB SMs. The following notation is applied: C_{FB}, C_{HB} – equivalent capacitance of all SMs within FB and HB, respectively; $\Sigma v^i_{\mathrm{c\{p,n\},FB}}$, $\Sigma v^i_{\mathrm{c\{p,n\},HB}}$ – total available capacitor voltage of the corresponding clusters, $v_{\mathrm{\{p,n\},FB}}$, $v_{\mathrm{\{p,n\},HB}}$ – total inserted voltage of the corresponding SM clusters.

III. H-MMC OPERATING PRINCIPLES AND DESIGN

Starting from an all-HB MMC designed for fixed DC link voltage operation, comprising N_{SM} SMs per branch, charged to $V_{\mathrm{SM}} = V_{\mathrm{DC,n}} / N_{\mathrm{SM}}$, a portion of the SMs can be replaced by FB units, to achieve sufficient negative voltage insertion capability required by the variable DC link voltage operation (1), as presented in Fig. 2. This section presents proposed operating principles in terms of insertion voltage reference share between FB and HB SMCs, as well as minimal FB count, that yield inherently balanced converter at an arbitrary DC link voltage value, without the need to employ any sorting algorithm.

A. EQUIVALENT CIRCUIT

H-MMC equivalent circuit is depicted in Fig. 4. All the SMs of a branch are represented by two equivalent clusters, corresponding to N_{FB} and N_{HB} individual SMs. As the analysis of the two branches within a phase of Fig. 4 is equivalent, upper branch is observed. The problem is discussed for a certain operating point, defined by the following.

- **DC-side** voltage reference, determined through k_{DC}.
- **AC-side** (grid) voltage reference $\hat{v}_{\mathrm{s}}$, corresponding modulation index – m_{s}, power factor – $\cos(\varphi_{\mathrm{s}})$ and output voltage displacement angle – θ_{s}, as well as current amplitude – $\hat{i}_{\mathrm{s}}$.

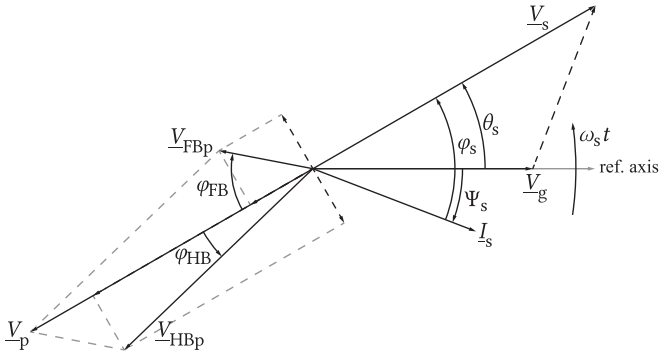

FIGURE 5. Phasors of grid- and converter-side relevant voltage and current values, with corresponding angles defined. Upper-branch inserted SMC AC voltage phasors, as well as resulting branch-level AC voltage phasor, are presented. Please note that angle sign is defined by an arrow with respect to mathematically positive direction, e.g. φ_{FB} is negative, while φ_{HB} is positive in the given example.

Following the convention defined in Fig. 5, grid-side voltage phasor is aligned to the reference axis. Converter AC-side terminal voltage v_s is displaced with respect to the reference axis by the angle θ_s. Assuming purely inductive equivalent AC-side impedance, grid current is in quadrature with $\underline{V}_s - \underline{V}_g$. Grid current to converter AC-side voltage displacement angle is defined as $\varphi_s = \theta_s - \Psi_s$.

In general, insertion voltage references of HB (4) and FB (5) SMCs can have arbitrary AC voltage amplitudes ($\hat{v}_{HBAC}$, $\hat{v}_{FBAC}$), AC voltage displacement angles (φ_{HB}, φ_{FB}) and DC voltage amplitudes (V_{HBDC}, V_{FBDC}), as long as the MMC operating constraints are satisfied, as discussed later in Section III-B. Following the notation of Fig. 5, SMC AC displacement angles are referenced with respect to total branch AC insertion voltage amplitude, in this example v_p, defined by the phasor magnitude $\underline{V}_p$ and displacement angle $\theta_s + \pi$ with respect to the reference axis.

Please note that equations (4) and (5) for the upper branch are written in general form and are always valid if the convention of Fig. 5 is respected. In the given example, angle φ_{FB} is negative with respect to Fig. 5 convention, and its amplitude will thus appear with a minus sign in (5).

$$v_{HB} = V_{HBDC} - \hat{v}_{HBAC}\cos(\omega t + \theta_s + \varphi_{HB}) \quad (4)$$

$$v_{FB} = V_{FBDC} - \hat{v}_{FBAC}\cos(\omega t + \theta_s + \varphi_{FB}) \quad (5)$$

B. OPERATING CONSTRAINTS

SMC insertion voltage waveforms can be arbitrarily chosen as long as the following conditions are met.

1) TERMINAL VOLTAGE CONSTRAINTS

DC- and AC-side, i.e. sum- and differential voltages must sum up to the DC voltage reference and grid current controller reference, respectively (see (1)), as in (6)-(7). Following (1), the relation between the DC terminal (6), AC terminal (7) and SMC voltages (4)-(5) can be derived.

$$\text{DC: } k_{DC}V_{DC,n}/2 = V_{FBDC} + V_{HBDC} \quad (6)$$

$$\begin{aligned}\text{AC: } & m_s V_{DC,n}\cos(\omega_s + \theta_s)/2 \\ &= \hat{v}_{FBAC}\cos(\omega t + \theta_s + \varphi_{FB}) \\ &\quad + \hat{v}_{HBAC}\cos(\omega t + \theta_s + \varphi_{HB}) \\ &= \underbrace{\left[\hat{v}_{FBAC}\cos(\varphi_{FB}) + \hat{v}_{HBAC}\cos(\varphi_{HB})\right]}_{=m_s V_{DC,n}/2}\cos(\omega_s t + \theta_s) \\ &\quad - \underbrace{\left[\hat{v}_{FBAC}\sin(\varphi_{FB}) + \hat{v}_{HBAC}\sin(\varphi_{HB})\right]}_{=0}\sin(\omega_s t + \theta_s)\end{aligned} \quad (7)$$

2) TERMINAL AND SMC ENERGY CONSTRAINTS

Energy exchange in an MMC must be matched between AC and DC terminals, otherwise SM capacitors may be discharged or overcharged. In case of H-MMC, this is true at both branch-terminal-level (8) and SMC-level (9)-(10). Zero-average values of (8)-(10) must be maintained.

$$\bar{p}_{DC} + \bar{p}_{AC} = \frac{k_{DC}V_{DC,n}i_{DC}}{6} - \frac{m_s V_{DC,n}\hat{i}_s}{8}\cos(\varphi_s) \quad (8)$$

$$\bar{p}_{FB,SMC} = \frac{V_{FBDC}i_{DC}}{3} - \frac{\hat{v}_{FBAC}\hat{i}_s}{4}\cos(\varphi_s + \varphi_{FB}) \quad (9)$$

$$\bar{p}_{HB,SMC} = \frac{V_{HBDC}i_{DC}}{3} - \frac{\hat{v}_{HBAC}\hat{i}_s}{4}\cos(\varphi_s + \varphi_{HB}) \quad (10)$$

Among (8)-(10), only two equations are independent, as $\bar{p}_{FB,SMC} + \bar{p}_{HB,SMC} = \bar{p}_{AC} + \bar{p}_{DC}$. Thus, (8) and either (9) or (10) can be considered as the system of two equations fully defining terminal and SMC energy constraints of a H-MMC. As (8) is a terminal constraint unrelated to intra-branch control, i.e. contains only converter-level operating point variables, it will not contribute the system of internal H-MMC variables. Relationship between the AC and DC current components is derived from (8).

$$i_{DC} = \frac{3m_s\hat{i}_s}{4k_{DC}}\cos(\varphi_s) = \frac{3\hat{v}_s\hat{i}_s}{2k_{DC}V_{DC,n}}\cos(\varphi_s) \quad (11)$$

3) SM VOLTAGE CONSTRAINTS

At the SM- and SMC-level, limitations to the design space are introduced, imposed by the electrical ratings of SMs and number of SMs per SMC. HB insertion voltage reference must always be non-negative (12), while maximal available insertion voltage of FB (14) and HB (13) SMCs are determined by their corresponding number.

$$V_{HBDC} + \hat{v}_{HBAC} \geq 0 \quad (12)$$

$$V_{HBDC} + \hat{v}_{HBAC} \leq (1 - N_{FB}/N_{SM})\,V_{DC,n} \quad (13)$$

$$|V_{FBDC} + \hat{v}_{FBAC}| \leq (N_{FB}/N_{SM})\,V_{DC,n} \quad (14)$$

C. SMC INSERTION VOLTAGE DETERMINATION

In the H-MMC, we can differentiate three sets of variables.

1) **System-level:** AC-side voltage amplitude (through m_s), grid current – i_s and power factor – $\cos(\varphi_s)$.
2) **Converter-level:** DC-side rated voltage and reduction factor – $V_{DC,n}$, k_{DC}; total number of SMs, share of FB and HB units – N_{SM}, N_{FB}, N_{HB}.

3) **Branch-level SMC:** AC voltage amplitudes – $\hat{v}_{\mathrm{FBAC}}$, $\hat{v}_{\mathrm{HBAC}}$; AC voltage displacement angles – φ_{FB}, φ_{HB}; DC voltage amplitudes – V_{FBDC}, V_{HBDC}.

System-level variables can be set to their rated values, while converter-level variables, with the exception of k_{DC}, are defined by the converter design. This leads to the branch-level variables. The six intra-branch variables are defined by a total of four equations (6), (15)-(16), (17), obtained as follows.

- DC insertion branch voltage constraint (6).
- AC insertion branch voltage constraints, starting from (7).

$$\hat{v}_{\mathrm{FBAC}}\cos(\varphi_{\mathrm{FB}}) + \hat{v}_{\mathrm{HBAC}}\cos(\varphi_{\mathrm{HB}}) = \hat{v}_{\mathrm{s}} \tag{15}$$

$$\hat{v}_{\mathrm{FBAC}}\sin(\varphi_{\mathrm{FB}}) + \hat{v}_{\mathrm{HBAC}}\sin(\varphi_{\mathrm{HB}}) = 0 \tag{16}$$

- SMC energy balance constraint, from either (10) or (9), utilizing DC- to AC-terminal current relationship $i_{\mathrm{DC}} = f(\hat{i}_{\mathrm{s}})$ (11). In this case, equation (10) is chosen.

$$\frac{\hat{v}_{\mathrm{HBAC}}}{V_{\mathrm{HBDC}}} \cdot \frac{k_{\mathrm{DC}}}{m_{\mathrm{s}}}\cos(\varphi_{\mathrm{s}} + \varphi_{\mathrm{HB}}) = \cos(\varphi_{\mathrm{s}}) \tag{17}$$

Since there are four equations and six variables, two among them are to be chosen freely. The selection is made to set V_{HBDC} (18) and $\hat{v}_{\mathrm{HBAC}}$ (19) voltage amplitudes in a way to maximally utilize insertion voltage potential of installed HB SMs, respecting (electrical) SM voltage constraints (12)-(13). This leads to the design with the minimal number of lossier and more expensive FB SMs, in favor of more efficient and cheaper HB units. As certain control voltage reserve must be accounted for, AC voltage component of HB SMC should not exceed (19), where k_{res} determines AC voltage control reserve. Factor k_{res} is defined as a fraction of maximal available AC voltage, and is taken as 5 % in this work, i.e. $k_{\mathrm{res}} = 0.05$.

$$V_{\mathrm{HBDC}} = \frac{N_{\mathrm{HB}}}{N_{\mathrm{SM}}} \cdot \frac{V_{\mathrm{DC,n}}}{2} \tag{18}$$

$$\hat{v}_{\mathrm{HBAC}} = (1 - k_{\mathrm{res}})V_{\mathrm{HBDC}} \tag{19}$$

FB SMC DC insertion voltage component is defined from (6).

$$V_{\mathrm{FBDC}} = \frac{V_{\mathrm{DC,n}}}{2}\left(k_{\mathrm{DC}} - \frac{N_{\mathrm{HB}}}{N_{\mathrm{SM}}}\right) \tag{20}$$

Furthermore, observing (17), m_{s} is constant for a grid-connected application, while k_{DC} can be in the range of $k_{\mathrm{DC}} \in [0, 1]$. Likewise, the ratio of AC to DC insertion voltage components of HB SMC can be in the range of $\hat{v}_{\mathrm{HBAC}}/V_{\mathrm{HBDC}} \in [0, 1]$, following (12). Thus, for minimal alteration of φ_{HB}, and consequently minimal additional SMC AC voltage amplitude required to synthesize required branch-level voltage (refer to $\underline{V}_{\mathrm{p}}$ of Fig. 5), the maximal value of $\hat{v}_{\mathrm{HBAC}}/V_{\mathrm{HBDC}} = 1 - k_{\mathrm{res}} = 1$ should be selected (17), (19), which proves the validity of choices (18)-(19). For the purpose of control voltage reserve, this ratio should be kept below unity, as aforementioned.

Finally, four equations with four variables are left, and the system can be solved. HB displacement angle is calculated from (17) and (19).

$$\varphi_{\mathrm{HB}} = \arccos\left(\frac{m_{\mathrm{s}}\cos(\varphi_{\mathrm{s}})}{k_{\mathrm{DC}}(1 - k_{\mathrm{res}})}\right) - \varphi_{\mathrm{s}} \tag{21}$$

Amplitude of FB SMC AC insertion voltage is obtained from (15)-(16), following phasor representation of AC voltages given in Fig. 5. Knowing that $\hat{v}_{\mathrm{p}} = \hat{v}_{\mathrm{n}} = \hat{v}_{\mathrm{s}}$, d- and q-axis components of $\underline{V}_{\mathrm{FB\{p,n\}}}$ can be determined.

$$\hat{v}_{\mathrm{FBAC}}\cos(\varphi_{\mathrm{FB}}) = \hat{v}_{\mathrm{s}} - \hat{v}_{\mathrm{HBAC}}\cos(\varphi_{\mathrm{HB}}) \tag{22}$$

$$\hat{v}_{\mathrm{FBAC}}\sin(\varphi_{\mathrm{FB}}) = -\hat{v}_{\mathrm{HBAC}}\sin(\varphi_{\mathrm{HB}}) \tag{23}$$

Further, FB SMC AC insertion voltage amplitude and displacement angle are derived.

$$\hat{v}_{\mathrm{FBAC}} = \sqrt{\hat{v}_{\mathrm{s}}^2 - 2\hat{v}_{\mathrm{s}}\hat{v}_{\mathrm{HBAC}}\cos(\varphi_{\mathrm{HB}}) + \hat{v}_{\mathrm{HBAC}}^2} \tag{24}$$

$$\varphi_{\mathrm{FB}} = \arctan\frac{-\hat{v}_{\mathrm{HBAC}}\sin(\varphi_{\mathrm{HB}})}{\hat{v}_{\mathrm{s}} - \hat{v}_{\mathrm{HBAC}}\cos(\varphi_{\mathrm{HB}})} \tag{25}$$

D. POWER FACTOR LIMITATION

Assuming constant-voltage-amplitude grid-connected operation of the converter, the modulation index is constant. Power factor limitation is derived from (17) and (19), keeping in mind that HB SMC AC voltage displacement angle is calculated to satisfy SMC energy equilibrium (17). Without affecting the generality, we can observe positive value of cosine functions. In this case, maximal value of $\cos(\varphi_{\mathrm{s}}+\varphi_{\mathrm{HB}})$ equals one, and defines the limiting factor of attainable AFE power factor.

$$\cos(\varphi_{\mathrm{s}}) = \underbrace{(k_{\mathrm{DC}}(1 - k_{\mathrm{res}})/m_{\mathrm{s}})}_{\leq 1 \text{ for } m_s=1}\underbrace{\cos(\varphi_{\mathrm{s}} + \varphi_{\mathrm{HB}})}_{\max=1} \tag{26}$$

Power factor limitation is derived.

$$\cos(\varphi_{\mathrm{s}}) \leq k_{\mathrm{DC}}(1 - k_{\mathrm{res}})/m_{\mathrm{s}} \tag{27}$$

Thus, at unity modulation index, power factor is limited by DC voltage reduction factor and AC voltage control reserve.

E. DESIGN FOR ARBITRARY DC VOLTAGE RANGE

Previously formulated relations can be used to aid the design of H-MMC. For a desired DC voltage reduction and known input power factor, one could determine optimal ratio of FB and HB SMs. However, to explore all the combinations, an illustrative example is presented hereafter, related to converter parameters of Table 1 with 16 SMs per branch.

A minimal number of FB SMs should be determined, so as not to violate the available SM insertion voltage limitation (14), for a given total number of SMs and desired DC voltage operating range, i.e. k_{DC} range. Determination process is iterative, as follows, and demonstrated on medium voltage MMC with parameters given in Table 1, where $m_{\mathrm{s,n}} = 0.95$ and $k_{\mathrm{res}} = 0.05$.

- Starting from an all-HB MMC, one HB SM per branch is replaced by a FB SM.
- DC voltage reference is swept over the desired operating range, i.e. $k_{\mathrm{DC}} \in [k_{\mathrm{DC,min}}, 1]$.

- Power factor is swept from maximal value (27) to zero.
- For each operating point defined by N_{FB}, k_{DC} and $\cos(\varphi_s)$, SMC-level variables are calculated according to (6) and (18)-(25).
- Voltage insertion capability of the selected number of FB and HB SMs is compared against calculated insertion voltage references. If assumed SM configuration cannot synthesize required references, one more HB SM is replaced by a FB unit and the entire process is repeated.
- The solution with the highest share of HB SMs, not violating insertion voltage capability (14), is adopted.

Following the generalized derivation of Sec. III-B to Sec. III-D, the presented iterative design approach will always produce optimal design in terms of the lowest share of FB SMs for the required DC link voltage range and AC-side power factor range.

F. DESIGN SELECTION FOR PHSP APPLICATION

For CM-free PHSP operation, value of $k_{DC,min} = 0$ is required. Attainable operating range, in terms of DC voltage reduction and power factor range, is presented in Fig. 6, for the converter ratings given in Table 1. For each N_{HB}/N_{FB} ratio, the grey area in graphs shows the achieved increment in converter operating range compared to the configuration with one FB SM less, which is marked by black area. In an all-HB MMC case, operation at arbitrary power factor in a narrow band around rated DC voltage is possible. Introduction of FB SMs in place of HB units gradually increases operating range towards lower DC voltage values. Surpassing $N_{FB} = 10$, there is no further yield in increased FB share.

Following this analysis, minimal FB share that enables DC link operating range down to zero for the exemplary MMC ratings, is $N_{FB} = 10$. This hardware configuration is henceforth used in test scenarios. Naturally, if one only has a need for partial DC voltage reduction, lower FB count and thus cheaper and more efficient configuration can be chosen. The optimization criteria of the presented method is to obtain the lowest FB SM share, starting from a converter of arbitrary ratings and SM count. This has been demonstrated for arbitrary DC link voltage range and AC-side power factor.

TABLE 1. Medium voltage MMC parameters used for the design example.

Parameter	Symbol	Value
Line voltage	U_n	6 kV
Apparent power	S_n	0.5 MVA
Grid frequency	f_n	50 Hz
Number of SMs per branch	N_{SM}	16
SM voltage	V_{SM}	650 V
SM capacitance (tolerance ±10%)	C_{SM}	2.25 mF
Branch inductance	L_{br}	2.5 mH
Branch inductance coupling coeff.	k_{br}	0.3
Branch resistance	R_{br}	50 mΩ
Switching frequency	f_{sw}	1 kHz

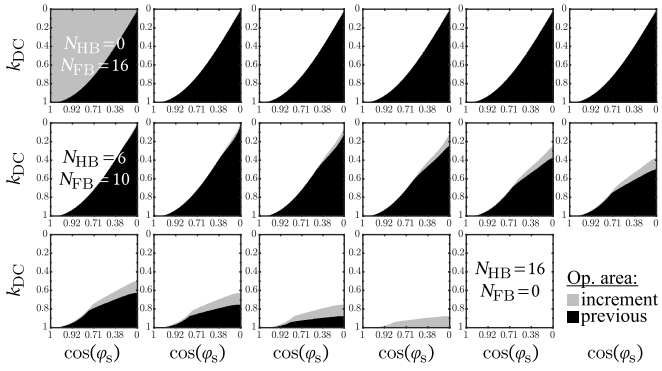

FIGURE 6. Attainable operating region for varying share of FB SMs, starting from Table 1 converter parameters for $m_s = 0.95$ and $1 - k_{res} = 0.95$. For each N_{HB}/N_{FB} ratio, the grey area in graphs shows the achieved increment in converter operating range compared to the configuration with one FB SM less, which is marked by the black area. It can be noticed that an increase in FB count above $N_{FB} = 10$ doesn't provide further operating range extension for the presented method. FB-only solution achieves full DC voltage range at arbitrary power factor, whereas HB-only setup operates at arbitrary power factor in a narrow band around rated DC voltage.

IV. INTERNAL H-MMC CONTROL

Zero-average energy exchange is ensured both at the branch level through AC and DC terminal constraints, as well as at the SMC level, through novel insertion voltage and displacement angles strategy. At SM level, PSC modulation establishes energy balance. However, as in a conventional MMC with uniform SMs, limited corrective energy balancing actions are required. Four principal balancing actions are inherited from the conventional MMC, while an additional SMC balancing layer is added, as presented in Fig. 7.

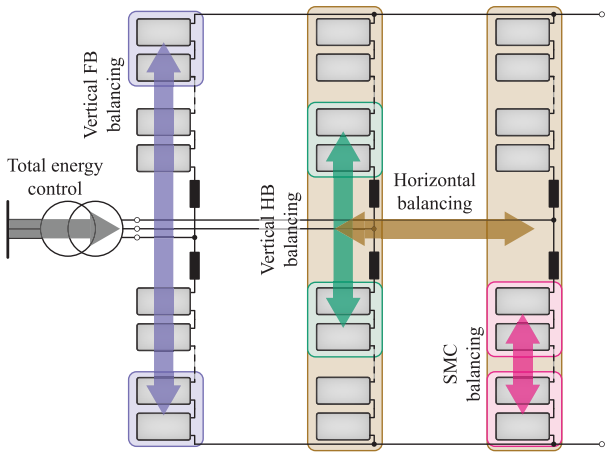

FIGURE 7. Energy control and balancing loops of H-MMC operating as AFE are presented. While total energy control and inter-phase horizontal energy balancing are performed equally as in a conventional MMC, inter-branch vertical energy balancing is altered. Due to displacement angles in inserted AC voltages of SMCs (21), (25), independent balancing control loops are established for HB and FB SMCs. An additional intra-branch balancing layer has been added to compensate for imbalance between same-branch SMCs.

A. CONVENTIONAL ENERGY BALANCING LOOPS

Three out of four conventional energy balancing actions are implemented identically to a MMC with uniform SMs.

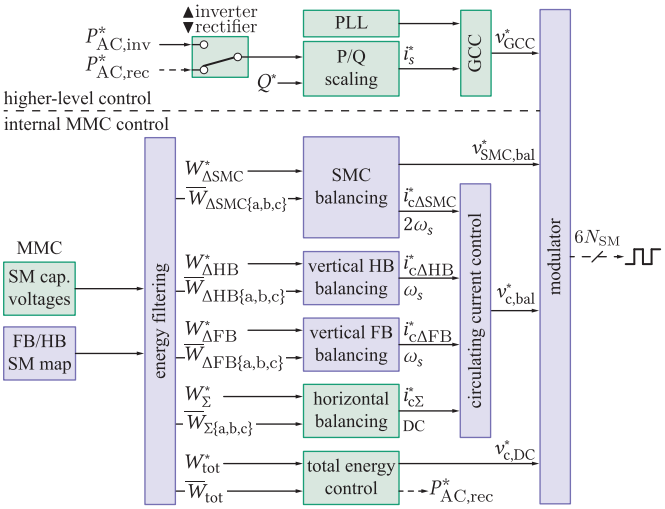

FIGURE 8. H-MMC control outline is presented. Starting from conventional MMC control (green), vertical balancing is performed independently for FB and HB SMCs, while SMC balancing layer is added to the internal control. A FB/HB SM map is required for proper SMC energy measurement and control. Upper-level control is unaffected, comprising grid-code-compliant scaling of active (P) and reactive (Q) power references, followed by grid current controller (GCC), synchronized to the grid through phase-locked loop (PLL).

Total energy is controlled in the same manner as for a conventional MMC [38], [39]. In the case of AFE, this loop is supplied from the grid side ($P^*_{\mathrm{AC,rec}}$ in Fig. 8).

Horizontal energy balancing is performed in the same manner as with a conventional MMC [39], [40]. DC circulating current $i_{\mathrm{c}\Sigma}$ is fed to the circulating current controller (Fig. 8), and balancing action is performed in conjunction with inserted DC voltage component (6).

Local SM energy balancing is performed as in [41], through correction of SM insertion voltage reference.

B. VERTICAL ENERGY BALANCING

Vertical energy balancing approach equally relies on [39], [40], where inserted AC voltage component (7) is used in conjunction with a balancing current component for the control action. However, AC insertion voltage components of HB and FB SMCs differ (19), (24), thus a unique circulating current reference cannot be generated for both SMCs due to differing AC voltage displacement angles, φ_{HB} and φ_{FB}. Thus, two vertical energy controller are generating two independent circulating current references, $i^*_{\mathrm{c}\Delta\mathrm{HB}}$ and $i^*_{\mathrm{c}\Delta\mathrm{FB}}$ (Fig. 8) for control of the appropriate SMCs, with respect to their AC insertion voltages. Differential energy references are naturally set to zero, while feedback values $\overline{W}_{\Delta\mathrm{HB}\{\mathrm{a,b,c}\}}$ and $\overline{W}_{\Delta\mathrm{FB}\{\mathrm{a,b,c}\}}$ are obtained from filtered-out SM capacitor voltage measurements.

C. INTER-SMC ENERGY BALANCING

In the presented control method, SMC balancing is inherently guaranteed under the steady-state conditions, as demonstrated in Section III. However, as in horizontal and vertical balancing actions, a small corrective balancing capacity is required to re-balance SMCs after transient events.

1) BALANCING MECHANISM

Inter-SMC energy exchange is achieved utilizing additional circulating current and voltage components, which will not interact with terminal voltages and currents. Thus, an AC circulating current at $2\omega_s$ (28), along with an additional SMC voltage at $2\omega_s$ (29), is introduced to produce this corrective action, where $x \in \{a, b, c\}$ and $\theta_{\mathrm{x}} \in \{0, -2\pi/3, 2\pi/3\}$. Zero-sum DC terminal circulating current condition must be satisfied (30), determining balancing current per-phase amplitudes $\hat{i}_{\mathrm{c}\Delta\mathrm{SMCx}}$ and displacement angles Ψ_{x}.

$$i_{\mathrm{c}\Delta\mathrm{SMCx}} = \hat{i}_{\mathrm{c}\Delta\mathrm{SMCx}} \cos(2\omega_s t + \Psi_{\mathrm{x}}) \tag{28}$$

$$v^*_{\mathrm{SMC,bal\{HB,FB\}x}} = \pm\hat{v}_{\mathrm{SMC,bal}} \cos(2\omega_s t + \theta_{\mathrm{x}}) \tag{29}$$

$$\sum i_{\mathrm{c}\Delta\mathrm{SMCx}} = 0 \tag{30}$$

Energy flow between SMCs of the same branch by means of (28) and phase-opposing voltages (29) is thus compensating the energy imbalances.

SMC differential energy reference is defined by FB to HB ratio, i.e. the difference in rated energy levels of the corresponding SMCs (31).

$$W^*_{\Delta\mathrm{SMC}} = C_{\mathrm{SM}} V^{*2}_{\mathrm{SM}} (N_{\mathrm{HB}} - N_{\mathrm{FB}})/2 \tag{31}$$

SMC energy balancing relies on a dedicated energy controller, outputting per-phase balancing current components (28), further modified to guarantee zero-sum amplitude at DC converter terminals (30). As the same mapping principle is used in conventional inter-branch vertical MMC balancing, the same control structure can be used [40].

D. MODULATION

In high-SM-count MMC applications, e.g. high-voltage DC inter-ties, the use of nearest-level modulation is common due to high output voltage resolution [32], [33]. Medium-voltage applications, however, comprise far fewer SMs. Inheriting modulation of high-voltage DC installations would result in poor output voltage waveform quality, further followed by significant current harmonic distortion [32].

A method to adapt modulation approach to medium-voltage installations, by combining nearest-level and pulse-width modulation, is presented in [32]. Another approach can naturally be the use of PSC modulation, introduced for multilevel converters in [42]. In such a case, N_{SM}-times higher apparent switching frequency at the converter branch terminals, with respect to SM switching frequency, ensures high-quality output voltage waveform, i.e. low total harmonic distortion.

In conventional MMC with either all-HB or all-FB layout, PSC modulation can be implemented as in [42]. So far presented PSC-based medium-voltage H-MMC solutions with reduced DC voltage (boosted AC modulation index) operation capability, with a mix of HB and FB SMs within

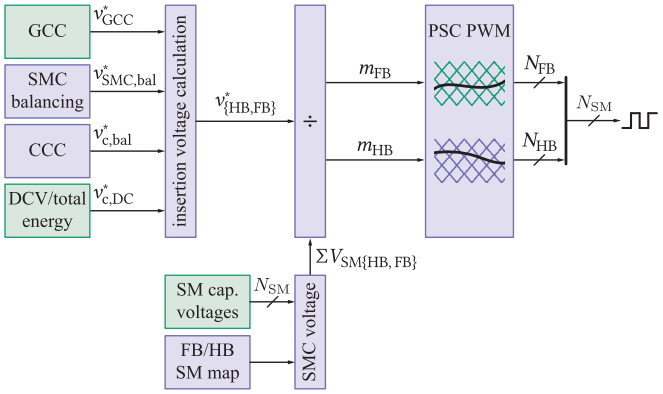

FIGURE 9. Modulation scheme of H-MMC is presented, with conventional MMC control blocks in green and newly-introduced blocks in violet. SM mapping stores information on FB/HB SM position in the branches and is used to correctly sum available insertion voltages of FB/HB SM clusters. In contrast to a conventional MMC, SM cluster balancing voltage components $v^*_{\mathrm{SMC,bal}}$, and circulating current controller additional SM cluster balancing currents are added. Insertion voltage references $v^*_{\mathrm{\{HB,FB\}}}$ are obtained by the voltage sharing algorithm presented in Sec. III-C. FB/HB clusters' insertion indices are then obtained, based on available insertion voltages $\Sigma V_{\mathrm{SM\{HB,FB\}}}$. Two sets of phase-shifted carriers are used to generate SM gating signals.

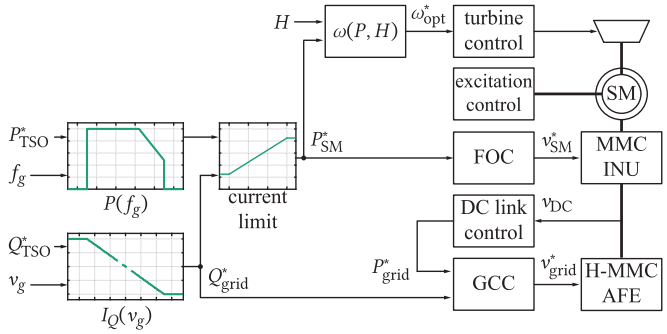

FIGURE 10. Overview of the complete higher-level control system structure of the proposed converter. Active and reactive power references are fed to the machine- and grid-side conversion stages, respectively. Field-oriented control operates the machine at unity power factor and constant excitation current, while shaft speed is controlled for optimal hydraulic efficiency by the turbine controller. DC link voltage is controlled by the grid-side stage.

branches, require capacitor sorting algorithms and modifications to modulation reference for proper operation [33].

In the method we propose, HB and FB SMCs within each converter phase leg act as two independent voltage sources (Fig. 4), with a separate layer controlling energy balancing between the two. Thus, classical PSC modulation with two sets of carriers for FB and HB SMCs has been implemented, requiring no capacitor sorting algorithm.

Following developed control structure (Fig. 8), the modulator is presented in more details in Fig. 9. Starting from voltage references of the grid current control, SMC balancing and balancing current control, circulating current control and total energy control, insertion voltages of HB and FB SMCs are generated. Individual SM capacitor voltages are measured, filtered, and summed-up based on SM map, to obtain HB and FB SMC available insertion voltages for closed-loop control. Two sets of PSCs are used to generate gating signals for SMs of corresponding SMCs.

V. SYSTEM-LEVEL CONTROL

Higher-level control system of H-MMC is developed in compliance with the control schemes utilized in the existing variable speed PHSPs [43] (Fig. 10).

Transmission system operator's active and reactive power references are, if necessary, scaled by grid-code frequency- and voltage-support functions $P(f_g)$ and $I_Q(v_g)$ [44].

A. GRID-SIDE HIGHER-LEVEL CONTROL

AFE stage has a dual role. Firstly, exchange of reactive energy with the grid is performed according to the schedule, regardless of the synchronous machine operating state. Reactive power reference Q^*_{grid} is fed to the grid current controller.

Secondly, total energy of the AFE is controlled through the active power reference P^*_{grid} (Fig. 8). This value is equal in amplitude to the machine-side active power reference, P^*_{SM}, augmented by converter losses.

B. MACHINE-SIDE HIGHER-LEVEL CONTROL

Machine-side MMC stage exchanges active energy with the hydraulic system at reference P^*_{SM} – pumping or generating, at arbitrary power factor, as it is decoupled from the grid.

P^*_{SM} and water head H are fed to an algorithm that outputs optimal machine speed for the highest hydraulic system efficiency. Turbine controller operates guide vanes following ω^*_{opt}. Based on P^*_{SM} and instantaneous machine speed, field-oriented (vector) control is performed. Dynamics of response to the P^*_{SM} change is thus determined by fast machine current control.

Wound rotor excitation controller is operated in the constant flux mode up to the rated speed.

VI. CONVERTER MODEL

Verification of the derived H-MMC control loops and limits of operation have been performed utilizing high-fidelity switched-model, i.e. each switching element of each SM is modeled. Further, the proposed modulation scheme is implemented as described in Sec. IV-D. Measurement, calculation and actuation time delays are taken into account in the model. FB and HB SM models are presented in Fig. 11. Auxiliary control system consumption is taken into account through the resistor $R_{\mathrm{SM}} = 21\,\mathrm{k\Omega}$, based on measured consumption in a SM of similar ratings [45]. The capacitance manufacturing tolerance has been taken into account through randomization of $C^{(\mathrm{i})}_{\mathrm{SM}}$ in the range of $\pm 10\%$ around the rated value (Table 1) at each simulation run.

Utilization of the switched model ensures verification of the H-MMC operation over the entire DC voltage range, including the region of very low DC link voltage amplitude, when HB SMs are bypassed, as discussed later in Sec. VII.

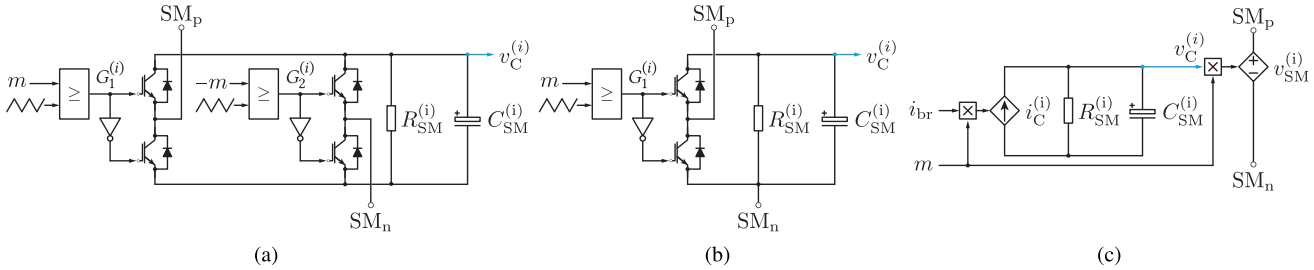

FIGURE 11. Implemented SM models: switched FB (a), switched HB (b), averaged (c). SM auxiliary losses are modeled by the resistor R_{SM}.

For the application-level analysis, i.e. operation of the entire PHSP, averaged SM model is used, once H-MMC control and limits of operation are already verified.

VII. TEST SCENARIOS AND RESULTS

A total of three test scenarios have been performed – AFE stage supplying a passive DC load, AFE operation under alteration of power factor beyond attainable operating area, and finally synchronous machine start-up sequence of the H-MMC-based converter.

The presented results are obtained from high-fidelity switched model simulations utilizing *PLECS* software package. Exceptionally, system-level test scenario (Sec. VII-C) has been simulated utilizing an averaged model, since the converter operation and limits have been demonstrated in details in test scenarios of Sec. VII-A and Sec. VII-B.

A. H-MMC AFE SUPPLYING PASSIVE LOAD

In the first scenario, presented in Fig. 12, H-MMC AFE operation is observed over the entire DC link voltage operating range, at 90 % of the rated DC link current. DC voltage reference is increased from zero to rated value in steps of $0.1\,V_{DC,n}$, while load is varied to maintain constant DC current amplitude. This resembles a VSD operation, where DC current is a reflection of the machine-side AC current, which is approximately constant in the PHSP application of interest. On the grid side, reactive power reference is determined from the maximal power factor expression (see (27)), reaching unity at rated DC voltage. Active and reactive power references are correctly tracked. Sum- and differential average capacitor voltages are correctly controller within the predefined limits. Zoomed-in areas at $t = 2\,\text{s}$ and $t = 8\,\text{s}$ reveal sinusoidal waveforms of both grid current and voltage before and after DC voltage change transients.

Inter-SMC balancing action, specific to the presented H-MMC control approach, is presented in more details in Fig. 13. Topmost plot presents variation of power factor $\cos(\varphi_s)$ as a function of DC voltage reference (27), taking the maximal value attainable for the given operating point. Dedicated balancing current (28) is limited in amplitude, and presented in the next subplot. Further, differential energy reference (31) and measured per-phase values are seen. The last subplot presents the controller error, which converges to zero after each transient. In this work, inter-SMC balancing

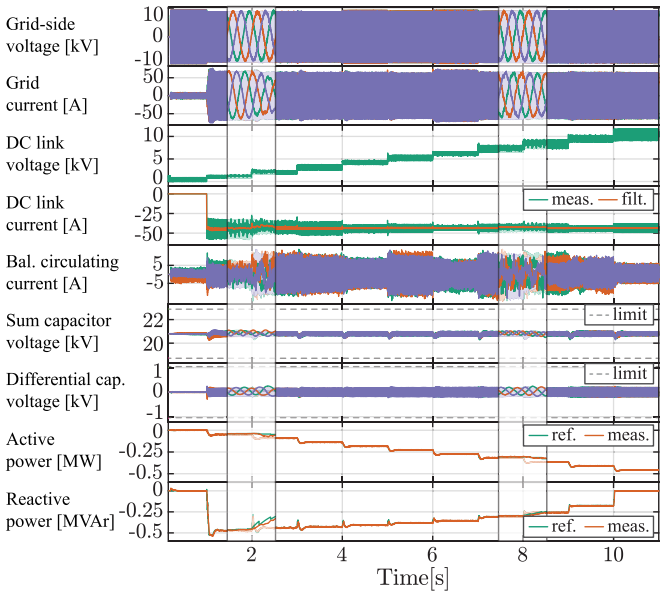

FIGURE 12. H-MMC test sequence presenting variable DC voltage operation in the entire range from zero to the rated value. Power factor is set at the limit of the safe operating range (27). Zoomed-in areas at $t = 2$ s and $t = 8$ s confirm that AC voltage and current are virtually unaffected by the k_{DC} transients.

current limit is set to 5 A, i.e. approximately 10 % of branch current amplitude.

At the rated DC voltage value, when there is no negative insertion voltage requirement, the converter can operate as a conventional MMC with equal insertion voltage references for both FB and HB SMs (1). In case of very low DC link voltages, in this design $k_{DC} < 0.2$, voltage insertion capability of FB SMs is sufficient for both DC and AC voltage component amplitudes (see (1)), thus converter can operate as conventional FB MMC. In both cases, SMC balancing action is not required and is thus disabled through zero current and voltage limit (28), (29).

As branch-level sum- and differential capacitor voltages (Fig. 12) only reflect horizontal, vertical and total balancing actions, Fig. 14 presents individual capacitor voltage values of one phase-leg, grouped to FB and HB SMCs of upper and lower branch. Following the test scenario in the topmost graph of Fig. 13, three operating segments can be identified.

In the range (0, 2)s, while $k_{DC} < 0.2$, only FB SMs are switched, while HB SMs are bypassed. This operating region

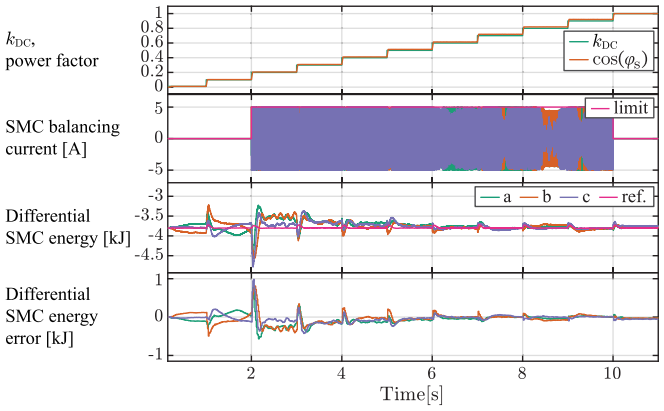

FIGURE 13. SMC energy balancing action is presented in more details for variable DC voltage operation scenario, at highest attainable power factor. Differential energy between SMCs of each phase converges to the reference value. Balancing action is unnecessary at very low DC voltage value, when converter operates using only FB SMs, as well as at the rated DC voltage, when conventional MMC operation is possible.

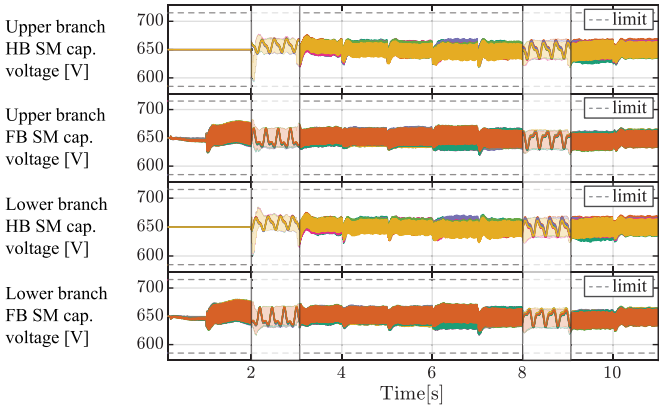

FIGURE 14. Capacitor voltages of individual SMs of one converter phase-leg, grouped in the SMCs. Zoomed-in areas at $t = 2.5$ s ($k_{DC} = 0.2$) and $t = 8.5$ s ($k_{DC} = 0.8$) reveal capacitor voltage waveforms in more details, when both HB and FB SMs are utilized.

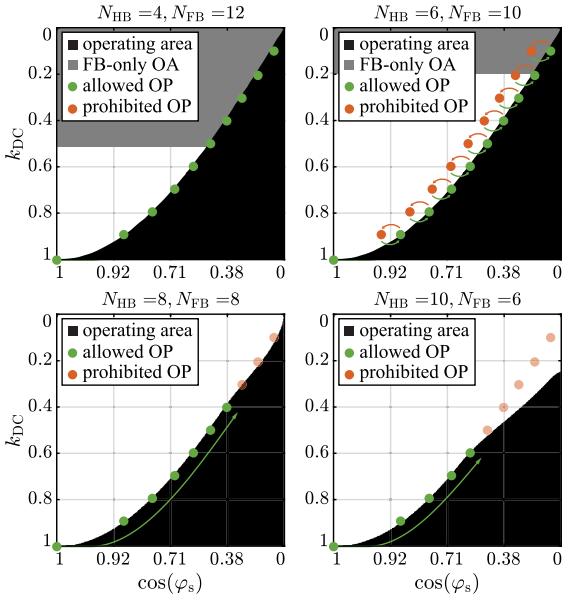

FIGURE 15. Limit of the H-MMC operating area in terms of DC voltage and power factor range is presented for different hardware configurations. For the selected configuration of $N_{FB} = 10$, operation in both allowed and prohibited operating area is presented, by deliberately increasing power factor 10% above the limit at each operating point, for a short time interval. Below $k_{DC} = 0.2$, available FB insertion voltage is sufficient for AC and DC side insertion voltage requirements (see (1)), thus converter can operate as conventional FB unit at any power factor.

coincides with FB-only operating area in Fig. 15, for the selected hardware configuration ($N_{FB} = 10$). Zero-current flows through the HB SM capacitors, thus constant voltage and no ripple are observed. Auxiliary SM power supply is fed internally from the SM capacitor, and its power consumption is typically very low compared to the rated SM power. Using the SM presented in [45] as an example similar to simulated converter parameters (Table 1), total internal power consumption of 20 W leads to the discharge time constant in the order of a minute during bypass.

Further, in the range of [2, 10)s, the converter is operated as presented in Sec. IV. Both HB and FB SMs contribute to the output voltage, however different references are fed to the SMCs, as derived in the previous sections. It can be seen that inter-SMC balancing action ensures average SMC voltages are equal to the reference values, while local SM balancing compensates for capacitance tolerance taken into account in the model (Table 1).

Lastly, in the range of [10, 11)s, DC link voltage reference is at rated value. As there is no need for negative branch voltage insertion, all SMs operate with equal insertion voltage references, as in a conventional MMC.

B. H-MMC LIMIT OF OPERATION

Limit of H-MMC operation for the presented control approach is presented for multiple hardware configurations in Fig. 15. For the chosen hardware configuration ($N_{FB} = 10$), operation in the entire DC voltage range is tested with $0.1V_{DC,n}$ increments, at the border of attainable operating area, marked by green dots.

In this test scenario, for each of the DC voltage operating points, power factor is set for a short time to 10 % above the limit (27), to the operating point marked by a red dot. Under such conditions, SMCs cannot be balanced through any choice of inserted voltages or displacement angles, inter-SMC differential energies diverge and cannot be re-balanced through a limited corrective inter-SMC balancing action. After return to safe operating area, SMC energy controller gradually reestablishes balance.

Results are depicted in Fig. 16. For each DC voltage reference, a short alteration of power factor to restricted area is visible in reactive power subplot, while terminal voltage and current waveforms remain unaffected by the short power factor alterations.

At the SMC level (Fig. 17), however, after expected transient on k_{DC} change, a sharp deviation of SMC differential energies is visible at each prohibited power factor alteration.

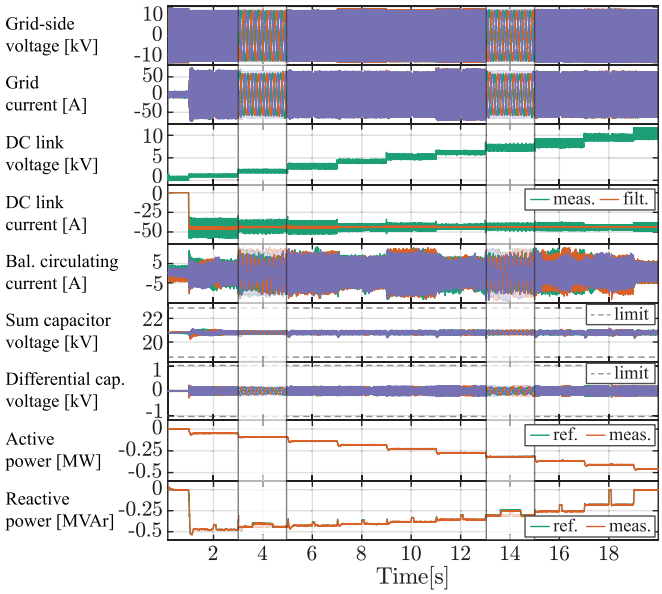

FIGURE 16. Operating sequence of H-MMC at constant DC current load, over the entire DC voltage operating range. For each applied k_{DC}, operation at 10% higher-than-allowed power factor is tested by applying power factor step-changes at $t \in \{4\text{ s}, 6\text{ s}, \ldots, 18\text{ s}\}$ instants. Consequently, short-term alterations in reactive power amplitude are seen. While AC terminal current and voltage waveforms are unaffected, as seen in the zoomed-in areas, converter cannot operate permanently in these points. At over-the-limit power factor (see (27)), differential SMC energy cannot be balanced anymore, leading to capacitor voltage divergence between FB and HB SMs and ultimately converter failure.

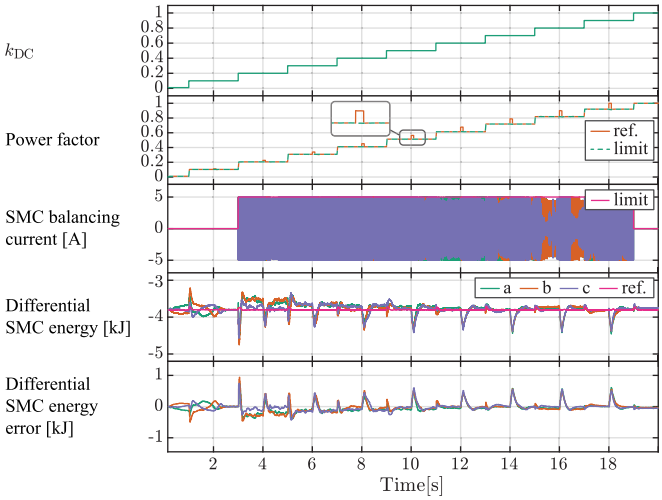

FIGURE 17. SMC balancing action for the second test scenario. Differential energy divergence is seen successfully controlled after each k_{DC} step. However, power factor alteration above the limit causes sharp SMC energy deviation, at $t \in \{4\text{ s}, 6\text{ s}, \ldots, 18\text{ s}\}$ instants. Operation in prohibited area would thus quickly drive the converter out of operation by overcharging FB- and fully discharging HB SMs, or vice versa. One can notice power factor deviation at $k_{DC} = 0.1$ has no impact, as this is the area of FB-only operation capability (see Fig. 15).

At such a rate of change, prolonged operation in the prohibited area leads to very high SMC energy deviations, ultimately leading to overcharge of FB and full discharge of HB SMs, or vice versa, and failure of the converter in either case.

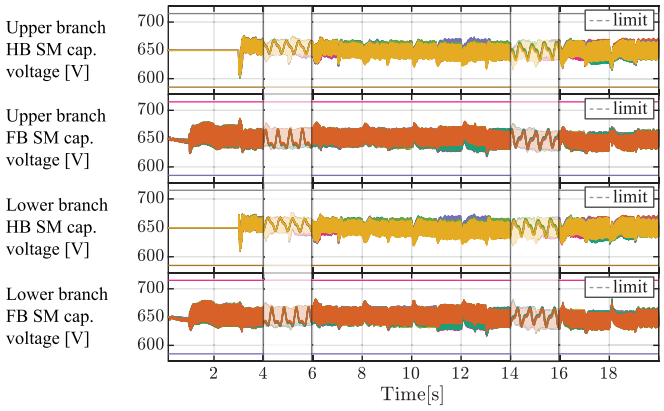

FIGURE 18. Instantaneous voltage of individual capacitors belonging to one phase-leg is presented. Effects of the short-term alterations of power factor beyond the limit, at $t \in \{4\text{ s}, 6\text{ s}, \ldots, 18\text{ s}\}$ instants, are compensated by the SMC controller, as shown in Fig. 17. This figure demonstrates that the SM voltages remain mutually balanced under all scenarios.

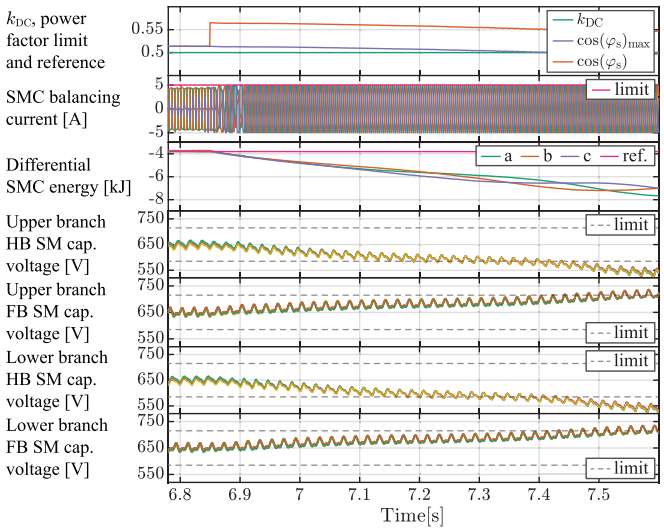

FIGURE 19. A more severe case of the second test scenario is presented, for $k_{DC} = 0.5$. In this case, power factor $\cos(\varphi_S)$ is augmented 10% above the maximally allowed value $\cos(\varphi_S)_{max}$ for the operating point, violating (27) and resulting in continuous deviation of SMC energies beyond balancing action corrective capacity. Average capacitor voltages of HB and FB SMs cannot be controlled, ultimately resulting in converter operation failure.

Individual capacitor voltages of one phase-leg are presented in Fig. 18. Short duration of deviations to prohibited operating area and consequent SMC balancing action have ensured average capacitor voltages remain within the predefined limits.

Figure 19 illustrates H-MMC operation limit in more details, for a single operating point, arbitrarily chosen as $k_{DC} = 0.5$. Power factor $\cos(\varphi_s)$ increase above the maximally permitted value $\cos(\varphi_s)_{max}$ violates constraint (27), meaning the converter is not inherently balanced anymore. This results in an immediate deviation in SMC differential energies, which is of permanent character, as we have not returned to safe operating area (see Fig. 15). Inter-SMC balancing corrective action cannot handle such a permanent

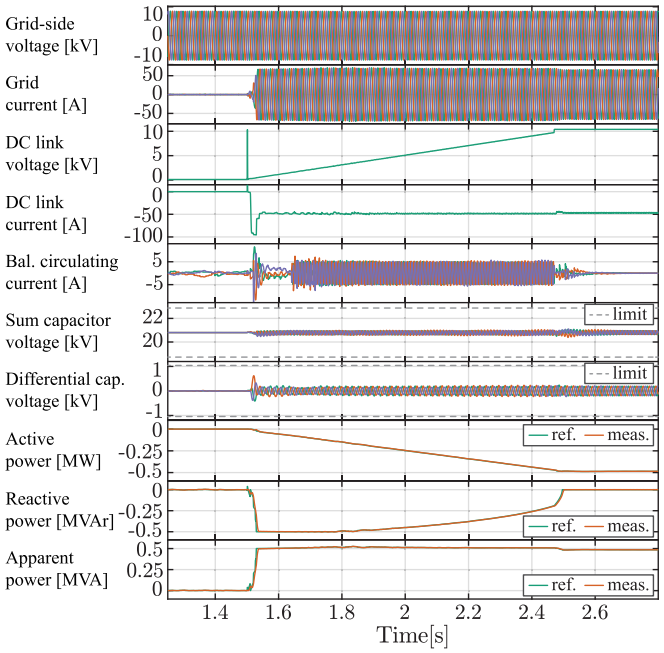

FIGURE 20. Grid-side operating sequence of H-MMC in a PHSP application is presented, for machine start-up sequence. DC voltage reference is changed in proportion to the machine stator frequency, while under such conditions DC current is constant due to the constant machine torque.

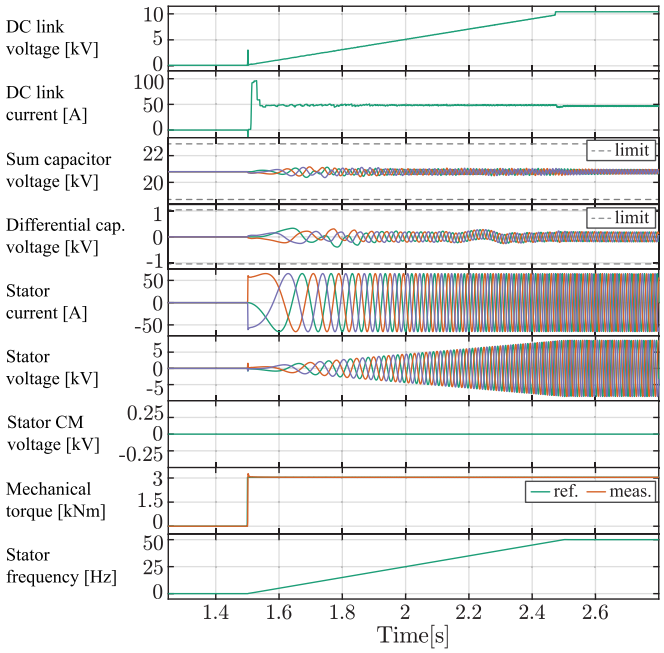

FIGURE 21. Machine-side MMC operating sequence during machine start-up at rated torque. DC voltage is changed in proportion with the output (stator) frequency, thus approximately constant voltage ripple is ensured throughout the entire frequency range, without additional control action involving CM voltage injection.

imbalance, thus average capacitor voltages of HB and FB SMCs quickly deviate out of normal operation limits. Gradual discharge of HB SMs and overcharge of FB SMs follows, ultimately leading to converter control failure.

C. MACHINE START-UP SEQUENCE

As converter limits of operation have been presented and verified, the last test scenario presents H-MMC in its intended application – variable speed PHSP. Synchronous machine start-up sequence, according to the PHSP control presented in Section V is tested under the rated torque, from standstill to the rated speed. Operation sequences of the grid- and machine-side stages are provided in Fig. 20 and Fig. 21, respectively.

DC link voltage reference is kept in proportion to machine stator frequency, ensuring constant amplitude of the dominant SM capacitor energy ripple, as derived in Section II. Both machine torque and DC current are kept at constant, rated, values. Sum- and differential capacitor voltage ripples are kept well within the limits, at approximately constant amplitudes over the entire speed range.

Machine is operated at unity power factor, while grid-side reactive power reference follows H-MMC demand during the reduced DC voltage operation. Both active and reactive power references are tracked correctly. It can be noted that reactive power demand of the presented control method does not require higher-than-rated apparent converter power. In other words, there is no overload in terms of grid current. Deviations around rated apparent power in Fig. 20 are within ±4%.

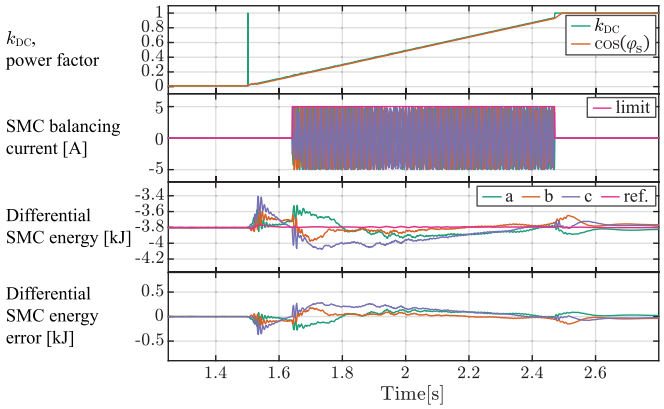

FIGURE 22. SMC balancing action for machine start-up test sequence is presented. Differential SMC energy deviation is even lower due to linear rise in k_{DC}, unlike step changes seen in the previous test scenarios. Controller error converges to zero.

The capacitor voltage ripple in the machine-side MMC remains well withing the limit of ±10% regardless of the machine operating frequency. This confirms theoretical considerations presented in Section II, and demonstrates the ability of the proposed converter configuration to enable CM voltage-free variable speed operation of the PHSP, along with other ancillary services.

SMC balancing action is presented in Fig. 22. Compared to step-change in k_{DC} of the previous scenarios, here the energy deviation is even lower, thus capacitor voltage deviations between FB and HB SMCs are even smaller. Individual capacitor voltage levels are well within ±10% limit, seen in Fig. 23.

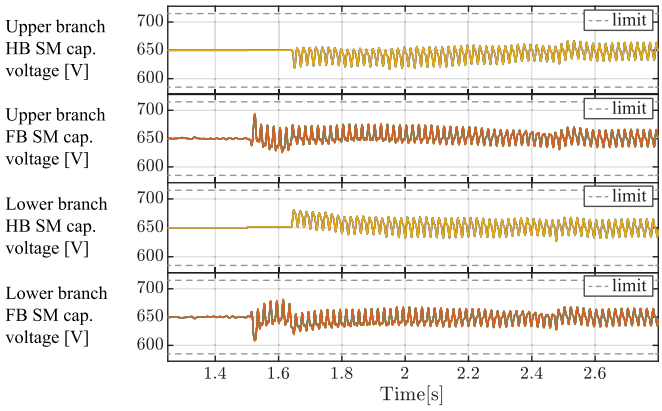

FIGURE 23. H-MMC capacitor voltage ripple of individual SMs during rated-torque machine start-up sequence. As in previous test scenarios, values are kept well within the ±10% limit.

VIII. DISCUSSION

The developed H-MMC control method relies on HB and FB SMC insertion voltage determination that yields inherent energy balance among the SMCs within each branch, while inheriting conventional MMC energy balancing loops. An additional inter-SMC energy balancing path ensures transient stability. Certain current capacity is required for such a control action, which was limited to 10 % of rated branch current in test scenarios. Trade-offs of the method can be evaluated through comparison to relevant published methods. Lower FB/HB share for zero-to-rated DC voltage operating range is achieved compared to [25], at the price of higher power factor reduction towards the grid. Higher FB/HB share (62 % against 50 %) is required compared to [36]. Unlike [36], grid can be supported by reactive power under reduced DC link voltage without branch current overload, as grid current component is equally shared between the branches. Compared to PHSP-oriented method [37], where 56 % FB share enables down to 50 % DC link voltage reduction at unity power factor, the method proposed here achieves down-to-zero DC voltage reduction with only slightly higher FB share (62 %), but with obligatory grid-side power factor reduction. At slightly lower FB share (50 %), method of [26] enables the advantage unity power factor operation down to 40 % of rated DC link voltage. However, method for further reduction is not offered. With respect to some relevant high-voltage-DC-oriented methods [27], [29], it is not possible to form a fair comparison, as they assume operation under boosted AC modulation index, which is not of interest in the observed PHSP application. The two methods, [27] and [29], utilize additional first- and second-order circulating current components, respectively, as the primary means of energy balancing among the FB and HB SMs, while the second-order circulating current is only used as a corrective measure in the newly proposed solution. The method published in [30] imposes lower FB SM share (50 %) for the same down-to-zero DC link voltage range, at higher power factor compared to the method presented here. The method, in turn, requires additional second-order circulating current injection for proper balancing. The amplitude of additional circulating current is the highest for high power factor operation at low DC link voltages.

IX. CONCLUSION

A CM voltage-free machine-friendly back-to-back MMC is presented, operating at variable DC link voltage thanks to H-MMC AFE stage. The proposed topology addresses an immense potential laying in conversion of existing fixed speed PHSPs to highly flexible and more profitable variable speed units, while requiring no additional work on the machine, mechanical and hydraulic systems.

A novel H-MMC design and control method has been presented and demonstrated on a 6 kV MMC with 16 SMs per branch. Attainable operating region in terms of DC voltage reduction and maximal power factor in each of the operating points have been presented for each possible share of FB and HB SMs. Further analysis was performed with $N_{\mathrm{FB}} = 10$, $N_{\mathrm{HB}} = 6$ hardware configuration, as it can achieve zero to rated DC voltage operating range, with minimal FB count. The developed generalized iterative design approach is based around optimization criteria of minimal FB SM share, and is valid for arbitrary converter ratings and SM count.

Building on conventional MMC control, additional inter-SMC balancing layer has been added and discussed in details.

Newly introduced control layers have been verified through a set of high-fidelity simulations of representative test scenarios. Firstly, normal operation of AFE stage has been presented. Further, theoretical limits of operating area were verified. Finally, start-up sequence of a 6 kV, 0.5 MVA synchronous machine has been presented, under rated torque operation. CM voltage-free machine supply is demonstrated over the entire operating range, ensuring full compatibility of the proposed solution with the existing fixed-speed PHSP units considered for retrofit.

The developed method offers reduced DC link voltage operation in an arbitrary range, with minimal share of FB SMs, and low additional balancing current requirement. H-MMC-based back-to-back drive does suffer from higher losses compared to the standard HB-based MMC, but offers common-mode-voltage-free machine operation in return. Compared to the other relevant methods, reduced FB SM count and very low additional balancing current requirement come at the price of reduced grid-side power factor range. A trade-off between FB/HB share and power factor range can be chosen within the provided design stage.

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