*IEEE Transactions on Power Electronics*, pp. 1–1, 2021

# Condition Health Monitoring of Modular Multilevel Converter Submodule Capacitors

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2021.3118602, IEEE Transactions on Power Electronics



# Condition Health Monitoring of Modular Multilevel Converter Submodule Capacitors

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***Abstract*—With a large deployment of power electronic converters in various critical applications, condition health monitoring is increasingly becoming important. In modular multilevel converter, submodule capacitors represents one of the critical components, having a strong impact on the overall converter cost and performance. This paper proposes a simple method for the submodule capacitance monitoring, deployed directly on the low-cost submodule controller and operating without disturbing or impacting the normal converter operation. Offline and real-time simulations, as well as experimental results, demonstrate the effectiveness of the proposed method in identifying changes in the submodule capacitance, which is of high importance for reliable converter operation.**

***Index Terms*—modular multilevel converter, submodule, condition health monitoring, capacitors.**

## I. Introduction

SINCE the concept was first introduced in 2001 [1], the Modular Multilevel Converter (MMC) technology has been widely investigated and proposed as a feasible alternative in different medium and high-voltage high-power applications. In contrast with other multilevel solutions, MMCs present notable advantages such as modularity, voltage-scalability, high efficiency, voltage-waveform quality, fault-tolerance, and absence of bulky dc-link capacitors [2]. Despite its extraordinary features, MMC reliability could be of concern since it is composed of hundreds of Submodules (SMs) which in turn are made up of several sensitive and expensive components such as power semiconductors devices and power capacitors [3], [4] among other electronic components subject to failure [5], [6]. Moreover, MMC technology has been adopted in highly critical applications such as High-Voltage Direct Current (HVDC) power transmission [2], electric railways interties [7] for massive public transportation, or pumped hydro storage power plants [8] as a machine-grid interface. Commonly, MMC reliability is addressed at the production level through considering proper electric circuit design, use of verified and tested components, and strict quality control procedures performed before and after the converter is placed in the field [9], [10] and, at the operational level, through fault-detection [11] and fault-tolerant methods [12] at the SM and MMC level respectively. Once a fault is detected, the damaged SM is isolated to reduce consecutive failure and extra damage to the converter. Depending on the fault-tolerant strategy, the converter may operate with reduced voltage capacity and power quality [13], [14] or at full capacity if redundant SMs are available [15], [16]. SM redundancy is visibly more favorable for the operation; nevertheless, it represents a higher investment cost and increases converter volume. [17]. Moreover, any fault situation may trigger unscheduled corrective maintenance, representing a high extra cost, especially in difficult access facilities [3]. Thus, it becomes evident that notwithstanding a failure in the MMC SMs might be managed up to some extent; the converter reliability can be improved further if a Condition Health Monitoring (CHM) technique of some sort is performed. Selected critical components can be continuously monitored to estimate their health condition and trigger preventive maintenance alarms before severe deterioration or major failure occurs [18].

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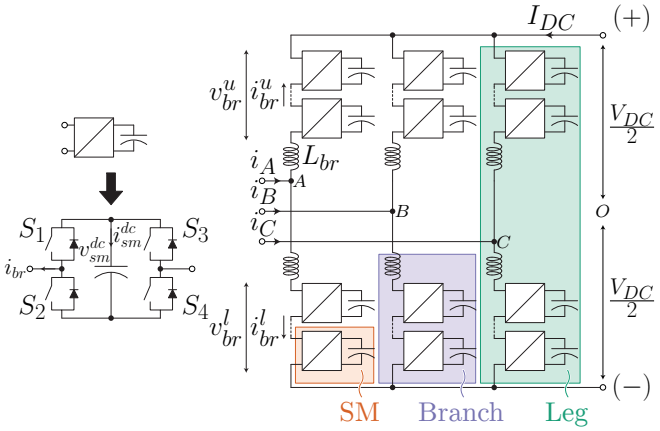


Fig. 1. A typical configuration of the MMC for the AC-DC conversion. FB SMs are considered in the paper, without loss of generality of the proposed method.

Several publication have addressed CHM of power semiconductor devices, specially IGBTs deterioration [19], [20], [21], [22] as they are considered as a sensitive component in power electronics applications [3], [23]. Nevertheless, the power capacitors are other components that fail frequently compared to other power electronics devices [3]. This takes special importance in MMCs, where SM's dc-link power capacitors are put under different stressors such as high current and voltage ripple and high temperature, among others degradation factors

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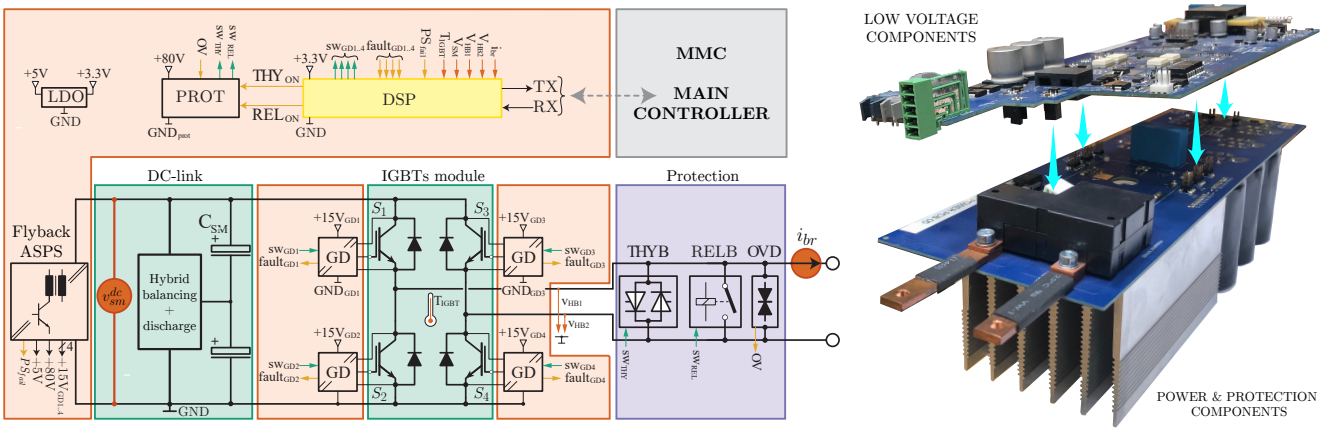


Fig. 2. Left side: considered SM scheme. The red label highlights the low-voltage components, the green label highlights the power components, and the blue label highlights the protection components. Right side: the existing SM prototype. The top-PCB contains the low-voltage components while the bottom-PCB the power and protection components.

related to environmental conditions such as humidity, mechanical vibrations, and high ambient temperature [10]. Typically in power electronics applications, three types of capacitors technologies are used in dc-links: Aluminum Electrolytic Capacitor (Al-cap), Metallized Polypropylene Film Capacitor (MPPF-cap) and Multi-layer Ceramic Capacitor (MLC-cap), and it is widely accepted that failure criteria for these technologies are [10]

- Al-cap: 20 % reduction in capacitance and/or Equivalent Series Resistance (ESR) increase two and a half times,
- MPPF-cap: 5 % reduction in capacitance and,
- MLC-cap: 10 % reduction in capacitance.

Thus, from capacitor CHM point of view, the main challenge is to estimate, with reasonable accuracy, the change over time of the capacitance or the ESR or both. Several works have addressed capacitance and ESR estimation in different power electronics applications [24], [25], [26], [27], [28], however research in CHM technique applied to MMCs is recent and limited. In fact, the authors of [29] presented the first work where CHM technique was used in a MMC. As in [30], [29] utilized a branch current injection in order to produce a second-harmonic SM capacitor current and voltage perturbation that is isolated using a band-pass filter and processed with the Recursive Least Squares (RLS) method to estimate the capacitance. Nonetheless, extra control effort and processor burden are needed to produce the perturbation and filter it, besides the drawback that added circulating branch current produces additional power losses and voltage stress in the SMs. Similarly, [31], [32] and [30] utilize the second-harmonic impedance to estimate the SM capacitance, but it is extracted from the inherent second-harmonic voltage/current ripple that circulates in the SM capacitors. On the other hand, the concept of Reference Submodule (RSM) where an SM within a branch is selected as a reference device to be compared respect others was first introduced in [33]. The authors claim that if the RSM is operated with the same switching signals of the SM monitored, then any difference in the capacitor ripple voltage is due to the difference between their capacitor impedances. Based on the same RSM idea, the authors of [34] proposed to estimate the capacitance using the capacitor voltage difference between the RSM and the monitored SM during its start-up passive charging process. The RSM-based methods main drawbacks are that the dc-link capacitance of the first used RSM has to be estimated in advance using another CHM technique, and at least one SM per branch (the one used as a RSM) does not contribute to the converter operation. This is a severe shortcoming of the method proposed in [34] where two SMs per branch are bypassed during the estimation process. The work presented in [35] takes advantage of the SM bypass capability and a bleeding resistor to passively discharge its dc-link. Similarly to [34], at least six SMs are off during the discharge process since symmetrical SMs operation among branches is sought to reduce converter performance deterioration. In contrast, the method presented in [36] applies the adaptive algorithm Fast-affine Projection to estimate both the ESR and C during the ON-state of the SM; thus, the sorting algorithm is modified to find and place the monitored SM in the most extended ON-state period possible. Researchers in [37] estimate the capacitance based on Nearest Level Modulation (NLM) algorithm. The method relies on the relationship between the SM capacitor voltage and the NLM within an entire fundamental period. Then, the RLS method is used to reduce the uncertainties related to measurements. All previously mentioned methods can be classified as online since their application allow the converter to operate continuously. Instead, the work presented in [38] is considered an offline method since the converter

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is not operating while the CHM technique is performed. The main idea is to estimate the SM capacitance during the MMC's start-up, particularly during the passive charging of the SMs from the dc-side of the converter. One significant disadvantage is that several MMC applications require continuous operation and shut down only is permitted during major failure and scheduled maintenances.

This article presents an alternative and simple approach for the MMC SMs dc-link capacitor CHM based on the Recursive Weight Least Squares (RWLS) technique to estimate and track its capacitance value and changes within time. The use of such a technique assures relatively high accuracy when sensors, acquisition systems, power switching events, and others sources of noise and error are present. In contrast with the previous works based on the Least Squares (LS) methods and the capacitance monitoring, the proposed method does not require any current injection nor any band-pass filter, representing a significant reduction in complexity and processing burden. Also, the proposed scheme does not need to modify the MMC or the SM's existing control strategy, no SMs are bypassed, and no extra hardware is required as the branch current and the SM dc-link voltage measurements are commonly available. The proposed method's performance is validated through offline and real-time simulations and experimental studies.

This article is organized as follows. Section II introduces the MMC SM where the presented scheme is deployed. Section III proposes the CHM method. Section IV presents simulation studies and experimental verification of the proposed method, respectively. Finally, the conclusions are presented in Section V.

## II. Preliminary considerations

The proposed capacitor CHM method is developed considering the MMC topology depicted in Fig. 1 and the already existing SM design presented in Fig. 2, which has already been detailed in previous publications of the authors [39], [6], [40]. The method is deployed in each SM so that each dc-link capacitance is estimated locally using the available dc-link voltage and terminal current measurements to reconstruct the SM dc-link current. Thus relevant considerations of these elements are presented hereafter.

### A. SM overview

Fig. 2 shows the considered MMC SM structure and laboratory prototype. Three main parts can be recognized

- the power components, composed of a FB Insulated Gate Bipolar Transistor (IGBT)-based converter whose dc-link includes an Al-cap bank, a hybrid balancing circuit to keep series connected capacitor voltages balanced within the bank, a flyback-based Auxiliary Submodule Power Supply (ASPS), already presented in [41], a dc-link voltage sensor and a terminal current sensor,
- the low-voltage low-power components, supplied from the ASPS, namely a Digital Signal Processor (DSP)-based local controller, communication components, IGBT gate drivers, and protection circuitry,
- the protection components, namely, a fast and non-permanent bypass thyristor and a permanent bypass relay.

TABLE I
SM characteristics.

| Parameter | Symbol | Value |
|---|---|---|
| Rated power | $S$ | 20 kV A |
| Rated ac rms voltage | $v_{sm}$ | 460 V |
| Rated ac rms current | $i_{br}$ | 45 A |
| Switching frequency | $f_{sw}$ | 1 kHz |
| Rated dc-link voltage | $v_{sm}^{dc}$ | 650 V |
| DSP sampling frequency | $f_s$ | 40 kHz |
| dc-link nominal capacitance | $C_{nom}$ | 2.25 mF |
| dc-link nominal ESR | $ESR_{nom}$ | 66.6 mΩ |
| dc-link nominal ESL | $ESL_{nom}$ | 66.6 nH |
| ASPS + hybrid balancing circuit power | $P_s$ | 16 W |

While the MMC SM can find itself in several operating states, only regular operation (SM on and switching) is considered relevant here, since the DSP, where the method is deployed, has available in every sampling period $T_s$ the dc-link voltage measurement $v_{sm}^{dc}$, the terminals current measurement $i_{br}$ and the four gate-driver signals (which are updated by the Pulse-width Modulation (PWM) module each switching period $T_{sw}$, with $T_s \ll T_{sw}$). The DSP performs other measurements, protection and communication tasks beyond the scope of the proposed method.

### B. SM dc-link current nature

The SM dc-link current is a direct consequence of the MMC control strategy keeping its terminals voltages (or currents) as the desired reference while, simultaneously, its internal energy stored in the SM dc-link capacitors is kept constant within a fundamental period, and equally balanced between SMs within a branch, between branches belonging to the same leg and between the legs. Assuming a symmetrical number of SMs operating per branch, balanced currents and voltages in the converter ac terminals, circulating currents close to zero and steady-state operation, then the branch voltage $v_{br}$ and current $i_{br}$ can be written as (please, note that in order to simplify the mathematical notation, all the expressions that follow are referred to the leg A, upper branch and $i$th SM)

$$v_{br}(t) = \frac{V_{DC}}{2} - v_x \cos \omega t \tag{1}$$

$$i_{br}(t) = \frac{i_x \sin(\omega t + \varphi)}{2} + \frac{I_{DC}}{3} \tag{2}$$

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where $V_{DC}$ and $I_{DC}$ are the converter dc terminals voltage and current, respectively; $v_x$ and $i_x$ with $x \in \{A, B, C\}$ are the converter ac terminal voltage magnitudes with respect to the reference node $O$ and the ac terminal line current magnitudes with phase-shift angle $\varphi$, respectively; and $\omega$ is the grid angular frequency. On the other hand, assuming that power exchange between the SM's terminals and its dc-link is lossless, it can be derived that

$$i_{sm}^{dc}(t) = m(t) i_{br}(t) \tag{3}$$

where $m(t)$ is the branch voltage $u_{br}$ normalized by $V_{DC}$ and it can be understood as the SM modulation index. Then, using (1) and (2) in (3) yields:

$$\begin{aligned} i_{sm}^{dc}(t) = & \underbrace{\frac{I_{DC}}{6} - \frac{i_x v_x \cos\varphi}{4V_{DC}}}_{\text{dc component}} \\ & + \underbrace{\frac{i_x \cos(\omega t + \varphi)}{4} - \frac{I_{DC} v_x \cos\omega t}{3V_{DC}}}_{\text{fundamental component}} \\ & - \underbrace{\frac{i_x v_x \cos(2\omega t + \varphi)}{4V_{DC}}}_{\text{second-order component}} \end{aligned} \tag{4}$$

Equation (4), in addition to showing the oscillating nature of $i_{sm}^{dc}$, also reveals that its frequency component's amplitudes depend of the converter operating point. Assuming power balance between the converter's ac and dc terminals, i.e., the dc component in (4) is zero, yielding that (4) can be rewritten as a function of the converter active and reactive power

$$V_{DC} I_{DC} = P_{DC} = \frac{3}{2} v_x i_x \cos\varphi = S_{3\phi} \cos\varphi = P_{3\phi} \tag{5}$$

$$\begin{aligned} i_{sm}^{dc}(P_{3\phi}, Q_{3\phi}) = & \\ & \frac{\sqrt{Q_{3\phi}^2 + P_{3\phi}^2}}{6} \left( \frac{\cos(\omega t + \arctan(Q_{3\phi}/P_{3\phi}))}{v_x} \right. \\ & \left. - \frac{\cos(2\omega t + \arctan(Q_{3\phi}/P_{3\phi}))}{V_{DC}} \right) \\ & - \frac{P_{3\phi} v_x \cos\omega t}{3V_{DC}^2} \end{aligned} \tag{6}$$

where $S_{3\phi}$, $P_{3\phi}$ and $Q_{3\phi}$ are the converter apparent, active and reactive power, respectively. As a illustration, Fig. 3 shows the dependency of the $i_{sm}^{dc}$ max. amplitude respect to the converter active and reactive power, where it is considered a lossless 250 kV A MMC operating as a rectifier, with line-voltage 3.3 kV, $\omega = 2\pi 50$ rad s$^{-1}$ and 5 kV in the dc side. It becomes evident that the lower the load, the lower the SM dc-link current amplitude. This analysis is relevant to consider since a significant current component allows to extract more information about the SM capacitance, suggesting that the MMC operating point might be considered in the decision process related to activation of the calculations of the method.

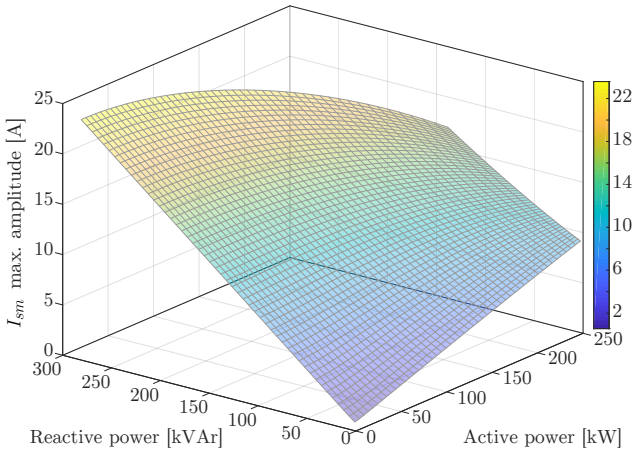


Fig. 3. The SM dc-link maximum amplitude current with respect to the MMC active and reactive power.

### C. SM dc-link current reconstruction

It is important to highlight that, as it was explained in the beginning of this section, the proposed method requires $i_{sm}^{dc}$ as a input signal, however the considered SM does not possess a sensor to measure it, and the expression (4) does not take into account its switching nature. To overcome this restriction, $i_{sm}^{dc}$ can be reconstructed from $i_{br}$ (measured) and the SM switch states

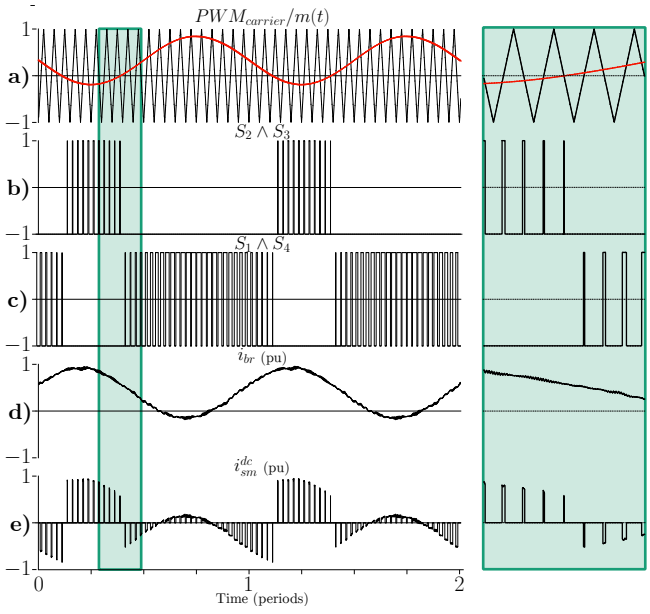


Fig. 4. SM main waveforms during two fundamental periods. From top to bottom: a) SM PWM triangular carrier at $f_{sw}$ and the corresponding output voltage reference signal (red) coming from the MMC main controller, b) the term $S_2 \wedge S_3$ from (7), c) the term $S_1 \wedge S_4$ from (7), d) the SM ac terminal current $i_{br}$ sampled at $f_s \gg f_{sw}$, and e) SM dc-link current reconstructed $i_{sm}^{dc}$.

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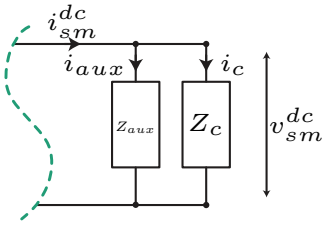


Fig. 5. The SM dc-link impedance scheme.

presented in Table II (available in the DSP registers), yielding

$$i_{sm}^{dc}(t) = i_{br}(t)(S_2 \wedge S_3) \vee -i_{br}(t)(S_1 \wedge S_4) \tag{7}$$

where $S_1$, $S_2$, $S_3$, $S_4 \in \{0,1\}$ represent the power switch states open (0) or closed (1). An illustration of the signals involved in the reconstruction of $i_{sm}^{dc}$ is presented in Fig. 4.

### D. SM dc-link impedance

The capacitance estimation problem based on the impedance measurement, as it is done in this work, faces not only the issue related to its parameters changing due to the aging process but also the effect of the surrounding components connected to the SM dc-link and the frequency response of the current flowing through it, as analyzed in this section.

Fig. 5 shows the considered SM's dc-link impedance scheme, where $Z_c$ represents the power capacitors impedance and $Z_{aux}$ represents the impedance of the auxiliary components connected to the SM dc-link such as the ASPS and the hybrid balancing circuit. It is widely accepted that $Z_c$ can be modeled as

$$Z_c(s) = \frac{1}{sC} + ESR + sESL \tag{8}$$

where $s$ is the Laplace operator, $C$ is the ideal capacitance, $ESR$ is the equivalent series resistance that represents all ohmic losses, and Equivalent Series Inductance (ESL) is the equivalent series inductance due to capacitor's leads connection path. On the other hand, when the SM is in operation, $Z_{aux}$ can be modeled as a constant power load $P_{aux}$ since the ASPS keeps its output voltage regulated while its input voltage varies widely, thus

TABLE II
SM SWITCH STATES, WHERE UNIPOLAR PWM IS ASSUMED.

| $S1$ | $S2$ | $S3$ | $S4$ | $i_{sm}^{dc}$ | cap. status |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $\lvert i_{br}\rvert$ | passive charg. |
| 1 | 0 | 0 | 1 | $-i_{br}$ | active disch. |
| 0 | 1 | 1 | 0 | $+i_{br}$ | active charg. |
| 0 | 1 | 0 | 1 | 0 | bypass (passive disch.) |
| 1 | 1 | 0 | 0 | 0 | bypass (passive disch.) |
| 0 | 0 | 1 | 1 | | FORBIDDEN |
| 1 | 1 | 1 | 1 | | |

$$Z_{aux} = \frac{P_{aux}}{i_{aux}^2} \tag{9}$$

where $i_{aux}$ is the primary-side power supply current consumption. In consequence, the SM dc-link impedance $Z_{SM}$ can be written as

$$Z_{SM}(s) = \frac{(C \cdot ESL \cdot P_{aux})s^2 + (C \cdot P_{aux} \cdot ESR)s + P_{aux}}{(C \cdot ESL \cdot i_{aux}^2)s^2 + C(ESR \cdot i_{aux}^2 + P_{aux})s + i_{aux}^2} \tag{10}$$

Fig. 6 shows the bode diagram of the considered $Z_{SM}$. The continuous black line is the impedance magnitude (top plot) and phase-shift (bottom plot) curve using $P_{aux} = P_s$, $C = C_{nom}$, $ESR = ESR_{nom}$, and $ESL = ESL_{nom}$ values (see Table I). Color-dashed lines illustrate how the nominal curve changes when those parameters are modified. As expected, $Z_{aux}$ behaves as a linear high-impedance in the zero-frequency range. In the low-frequency range (few Hz to few hundred Hz), $Z_{SM}$ is dominated by the ideal capacitor impedance. In the medium-frequency range (few kHz to few MHz), $Z_{SM}$ is influenced by the ESR. Finally, in the high-frequency range (above a few tens of MHz) ESL dominates $Z_{SM}$. This diagram shows that the extractable information is limited to the SM dc-link current frequency components that excite the SM dc-link impedance. The expression (4) exposed the oscillating nature of $i_{sm}^{dc}$ at fundamental $\omega = 2\pi f_0$ and $2f_0$ while the previous section, together with the unipolar modulation scheme adopted, reveal the pulsating component in the SM dc-link current at the switching frequency $f_{sw}$ and the $2f_{sw} \pm f_0$ sideband components around the $2f_{sw}$ apparent switching frequency component (vertical green lines in the frequency axis). Consequently, the primary information extractable is likely the $C$ value due to the $f_0$ and $2f_0$ current components close to the ideal-capacitive zone. On the other hand, the ESR estimation is theoretically possible to carry out, however difficult to implement since it is needed both high measurements sampling frequency and high precision measurement, especially

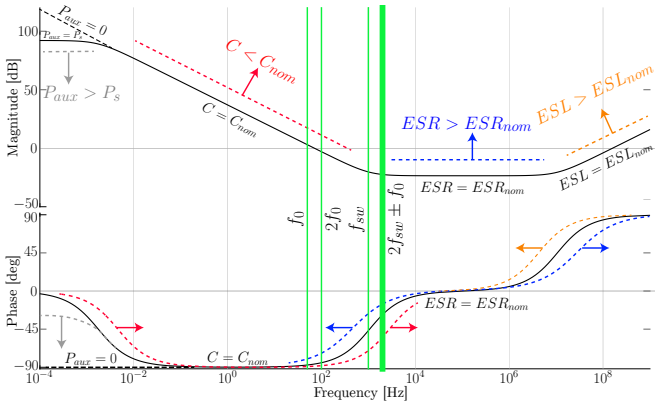


Fig. 6. The SM dc-link impedance transfer function in the frequency domain.

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the $2f_{sw} \pm f_0$ SM dc-link voltage component due to it is highly attenuated. Even more, with the considered $P_s$ and $ESL_{nom}$ it is deduced that $Z_{aux}$ and ESL do not play an essential role in the capacitance estimation. It is important to mention that when the SM dc-link capacitor bank ages or some of its components fail, the $C$ value will be reduced, increasing the impedance magnitude and moving the phase-shift curve to the right, improving the $C$ estimation even though, at the same time, the ESR will increase its participation in the impedance composition since $ESR \ll 1/sC$. In consequence, $Z_{SM}$ for the estimation can be re-written as

$$\frac{v_{sm}^{dc}(s)}{i_{sm}^{dc}(s)} = Z_{SM}(s) = \frac{1}{sC} \tag{11}$$

## III. Proposed SM capacitor CHM method

In the previous section, all the considerations and operating principles related with the converter and the SM were presented as they are needed to analyze and describe the proposed scheme. The MMC SM dc-link capacitor CHM method relies on extraction of capacitance value from the low-frequency SM dc-link impedance, taking advantage of the existing sensed variables of the SM and the oscillating nature of the SM dc-link current. Fig. 7 shows the scheme of the proposed method. In each sampling period the DSP discretize the sensed $v_{sm}^{dc}$ and $i_{br}$ and retrieves the switching signals $S_1(k)$ and $S_3(k)$ (or equivalent $S_2(k)$ and $S_4(k)$) calculated comparing the reference $m(k)$ and $-m(k)$ with the PWM carrier, respectively. Using the discrete quantities $i_{br}(k)$, $S_1(k)$ and $S_3(k)$ in (7), the dc-link current $i_{sm}^{dc}(k)$ is reconstructed. Then, both $i_{sm}^{dc}(k)$ and $v_{sm}^{dc}(k)$ together with the same signals from the previous iteration $(k-1)$ are used to estimate a new parameter $\hat{C}(k)$, using the RWLS technique. This procedure is repeated $M$ iterations or until the difference between two consecutive found parameters is less than a defined limit, as it is expressed in (12)

$$StopCond = k \leq M \vee |\hat{C}(k) - \hat{C}(k-1)| \leq \varepsilon \tag{12}$$

when the stop condition is met, the parameter estimated is sent to the MMC main controller.

Generally, the RWLS is a mathematical tool used in the parameters estimation problem of a gray-box models that can handle the measurement uncertainties introduced by sensors and the digitalization process. Given a system that can be modeled as a linear function of a set of unknown parameters in general, the main principle of any Least Squares method is to determine the unknown parameters by minimizing the sum of the squared error between the real system output (measured) and linear system model output (calculated) while they are stimulated with the same input. In particular, the RWLS solves the minimization problem recursively, advantageous in an industrial application where computing capacities might be limited. Please, see the Appendix for more details about the mathematical development of the RWLS algorithm. For the case of the presented method, the RWLS is applied as follows:

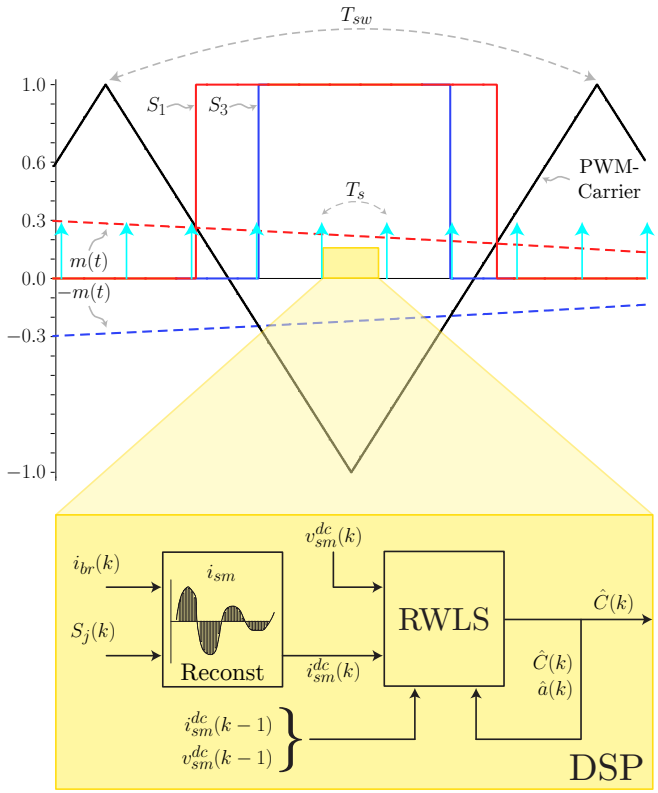


Fig. 7. Proposed method scheme respect the main time-events in the SM. The top picture shows the $S_1$ and $S_3$ DSP PWM output signals as a consequence of the comparison of $m(t)$ ($S_1$) and $-m(t)$ ($S_3$) respect the PWM triangular-waveform carrier signal. The straight arrows represent the DSP sampling instant, where $i_{br}$ and $v_{sm}^{dc}$ are acquired. During this period ($T_s$) one iteration of the RWLS is performed resulting in preliminary $\hat{C}(k)$ estimation. This procedure is repeated until the stop condition (12) is met.

Using the Bilinear transform the transfer function proposed in (11) is discretize, yielding

$$G(z^{-1}) = \frac{v_{sm}^{dc}}{i_{sm}^{dc}} = \frac{\frac{T_s}{2C}(z^{-1}+1)}{1-z^{-1}} \tag{13}$$

which resembles (16) in the Appendix. Then, the data vector $\psi^T(k)$ and the parameter vector $\hat{\theta}^T(k)$ are written as

$$\psi^T(k) = \begin{bmatrix} v_{sm}^{dc}(k-1) & \frac{T_s}{2C_{nom}}\left(i_{sm}^{dc}(k) + i_{sm}^{dc}(k-1)\right) \end{bmatrix} \tag{14}$$

$$\hat{\theta}^T(k) = \begin{bmatrix} a(k) & \frac{1}{\hat{C}(k)} \end{bmatrix} \tag{15}$$

Please note that the estimate $\hat{C}(k)$ from the above equation, represents the normalized values respect to $C_{nom}$ and $a(k)$ reflects the past value of $v_{sm}^{dc}$. Finally, one has

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to calculate iteratively (19), (20) and (21) as it is explained in the Appendix.

## IV. Method Validation

In order to validate the proposed CHM method, three different steps were followed: a) an offline simulation considering MMC model from Fig. 1, b) MMC RT-HIL simulation where the method is deployed in the actual SM's control and communication environment (hardware and software) while the power components are simulated in real-time, and c) MMC test setup where the method is deployed in the SMs prototype. It is important to note that all the measurements used in the offline and MMC RT-HIL simulations were degraded with additive white Gaussian noise $\sim \mathcal{N}(\mu = 0, \sigma = 0.5)$. Both MMC RT-HIL and MMC test setup aiming to make the SMs and its controller to operate at similar conditions as they would be exposed to during a regular MMC operation. To do so, an MMC reduced branch circuit is considered and presented in the central part of Fig. 11. Four SMs and an inductor are connected in series to form the reduced MMC branch (MMC-branch). The MMC-branch is connected to an external voltage source, made of four series-connected SMs forming the so-called source-branch (S-branch). Each SM of the S-branch has available dc-link terminals, and they are connected to four isolated dc sources. The S-branch operates as a voltage-source; thus the MMC-branch operates modifying its terminal voltage (1) to induce the desired current through the SM terminals (2).

### A. CHM practical considerations

Independently of the validation strategy, the proposed method is implemented considering the next steps and details:

1. parameter vector initial condition. It is chosen as the result of the previous estimation process. When previous result does not exist then the parameter vector initial condition is chosen as $\hat{\theta}^T(0) = [1 \quad 1]$. In other words, the RWLS assumes $C_{nom}$ as initial guess of the first iteration and previous $v_{sm}^{dc}$.
2. covariance matrix initial condition. Choosing a big covariance value for each unknown parameter can be interpreted as the RWLS assumes that the parameters initial condition are not close to the real values, increasing the parameters' searching range and the convergence speed. However, big covariance values might cause numeric instability as the calculated variables might overflow or underflow in a limited data type size implementation. Thus, the initial covariance was chosen $P_w(0) = 1e^-4 I_{2x2}$.
3. solve the capacitance estimation problem:
   - 3.1. reconstruct $i_{sm}^{dc}$ using $i_{br}$ and the switching signals $S_1$ and $S_3$ in (7). $S_1$ and $S_3$ are retrieve from the DSP's PWM module,
   - 3.2. using $i_{sm}^{dc}$ and $v_{sm}^{dc}$ together with (14) and (15) it is applied the RWLS technique presented in the appendix, following the next order of the equations: (19) $\rightarrow$ (20) $\rightarrow$ (21).
   - 3.3. check the stop condition considering $M = 40e^3$ (approximately 5 s at $f_s$) and $\varepsilon = 1e-3$,
4. retrieves the estimated capacitance physical values using $\hat{C}(mF) = C_{nom}\hat{C}(k)$.
5. report found parameter value to the MMC main controller.

TABLE III
MMC Characteristics

| Parameter | Symbol | Value |
|---|---|---|
| Rated power | $S$ | 250 kVA |
| Grid voltage | $V_g$ | 3.3 kV |
| Fundamental frequency | $f_0$ | 50 Hz |
| Branch inductance | $L_{br}$ | 2.5 mH |
| Max. output voltage | $V_{DC}$ | 5 kV |
| Number of SMs per branch | $N$ | 8 |
| Number of branches | $Nbr$ | 6 |

### B. Offline simulation studies

Parameters of the simulated MMC and SMs are presented in Table III and Table I, respectively. The modeled MMC utilizes 48 SMs, an standard d-q frame GCC and outer layer controller for the dc terminals. The total energy control and the internal energy balancing control are based on [42]. Then, the simulation is carried out considering the next scenario

- the SM dc-link capacitance CHM is performed while the MMC operates as a rectifier fully loaded on its dc side. Each SM dc-link actual capacitance is initialized randomly in the range of $C_{nom} \pm 20\%$, simulating the manufacturing tolerance. On the other hand, ESR is set nominal. Between $t$ =5 s and $t$ =5.5 s the CHM method is stopped, each dc-link capacitance is reduced to 80% of its initial condition, and ESR

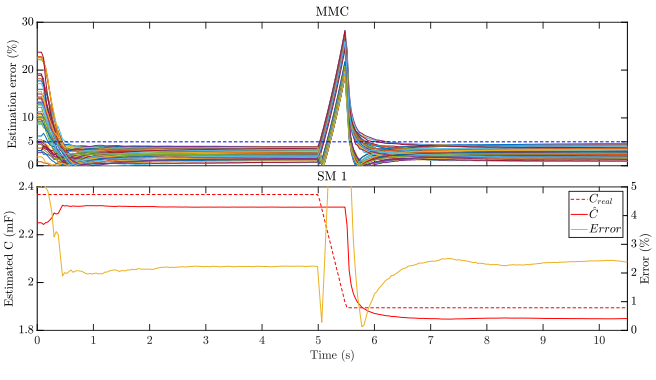


Fig. 8. Offline simulation results. Top plot: estimation error for each SM dc-link capacitance. In the first part of the simulation ($t$ <5 s) the real capacitance for each SM is set randomly and ESR is set nominal. In the second part ($t$ >5.5 s) the real capacitance is set to 80% of its initial value and ESR is set 2.5 times its nominal value. Bottom plot: the estimated parameter for the $SM_1$ (leg A, upper branch). The continuous red line is the estimated capacitance $\hat{C}_1$ while the dashed red line is the real value.

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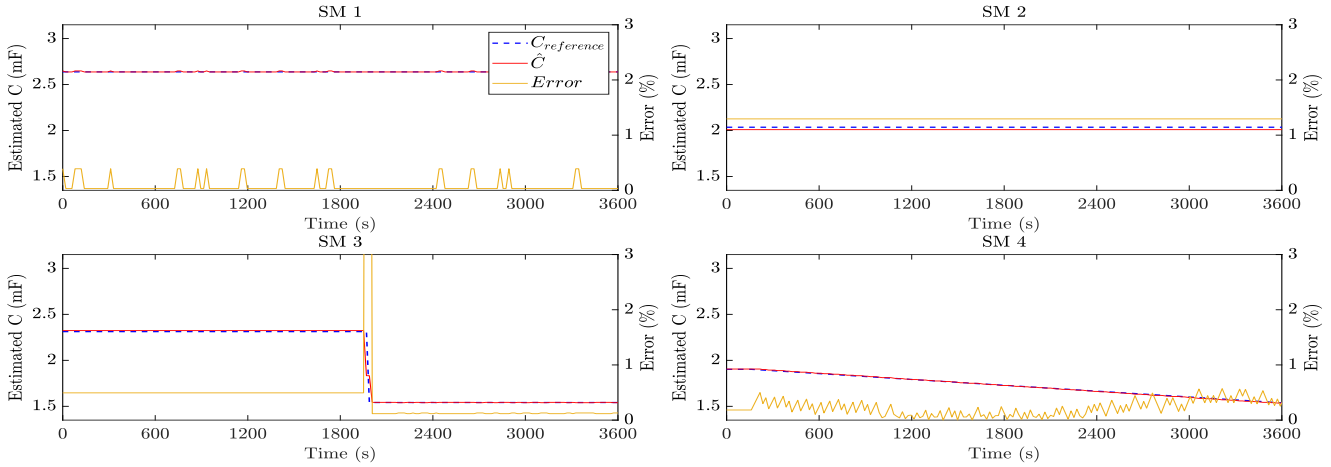


Fig. 9. Parameter estimation results for the MMC RT-HIL simulator. The dashed red lines is the reference capacitance value. The continuous red lines is the estimated capacitance, respectively. The continuous yellow line is the estimated percentage error. Each SM is set with different reference capacitance and ESR to demonstrate the proposed method capacitance track capability.

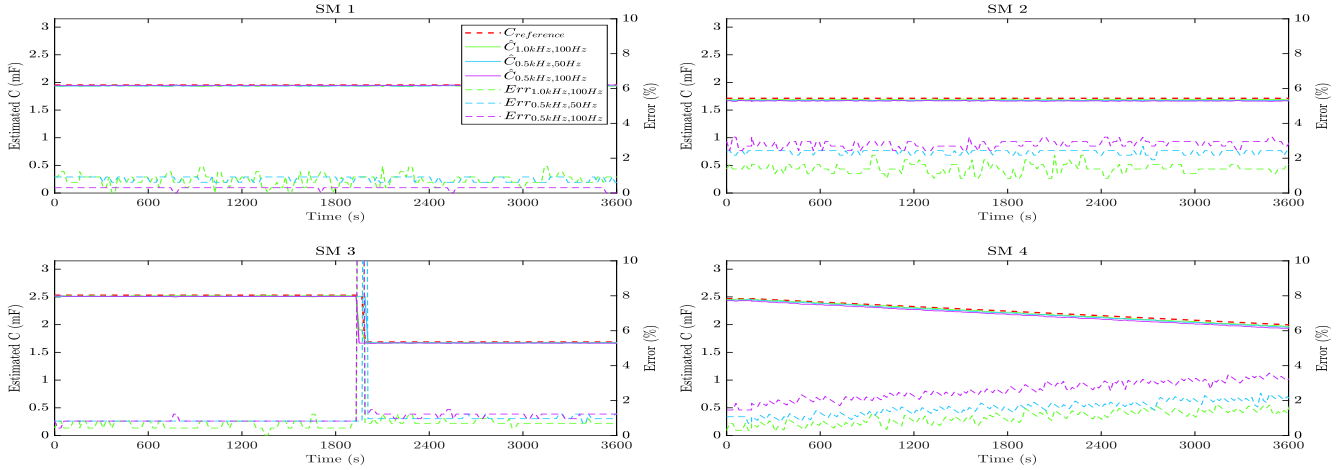


Fig. 10. Parameter estimation results for the MMC RT-HIL simulator under different MMC switching and ac terminals frequencies. The dashed red line is the reference capacitance value. The colored continuous and dashed lines are the estimated capacitance, and its error respect the reference value, respectively, for three different cases of switching frequency and converter ac terminals frequency.

is increased 2.5 times. In $t = 5.5\,\mathrm{s}$ the method is started again using the last estimated parameters as starting point.

The top part of Fig. 8 shows the parameter estimation results for each SM expressed as the error with respect to their real value while the bottom part presents the result for the SM1 expressed in physical units. The error is calculated using $error(\%) = 100\left|\hat{C} - C_{real}\right| / C_{real}$. At the beginning of the simulation the error is high due to the initial conditions and the simulation start transient. After 100 ms it starts to converge and after 2 s it settles down. At $t$ =5 s the method is stopped and initialized at $t$ =5.5 s finding a big error as the real capacitance was reduced 20%. The maximum error found is 4.6%.

### C. MMC RT-HIL simulation

Following successful verification of the model in offline simulations, complete algorithm is deployed on the DSP of the actual MMC SM. In order to extensively verify its performances under various test cases that are not easy to achieve in the experimental setup, RT-HIL system is developed. The MMC RT-HIL simulator, depicted in the top part of Fig. 11, comprises eight SM control boards, each one with a replica of the prototype SM local controller, a PLECS real-time simulator RT-Box 1, and an interface board to adapt the signals between them. Consequently, the RT-Box simulates the MMC-branch SMs power components, the S-branch SMs power components, the inductor between them and the S-branch dc sources. In order to show the method capability to estimate the SM dc-link capacitance under different capacitor ageing states, each SM capacitor impedance was set with different values and time dependency. Also, each capacitance initial condition was set randomly in the range $C_{nom} \pm 20\%$ and ESR initial condition was set $ESR_{nom}$, thus

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- SM1: Both parameters are kept constant along with the simulation as it would be the case with capacitor parameters at the beginning of its lifespan,
- SM2: The capacitance and ESR are set at 80% and 250% of its initial condition respectively, as it would be the case with capacitor parameters at the end of its lifespan,
- SM3: capacitor bank is reduced one third at $t$ =2000 s as emulating artificially loss of capacitance in order to verify performance of the method, representing a 33.3% capacitance reduction and 50.1% ESR increase,
- SM4: capacitance and ESR are linearly changed to 80% and 250% from their initial condition respectively, emulating ageing.

It is important to highlight that ohmic losses in the capacitors foils, tabs, terminals, and electrolytes, mainly responsible for their temperature rise, are included in the ESR term, and its effect in the proposed method is taken into account as ESR is considered in the simulation conditions.

The MMC RT-Hardware-in-the-loop (HIL) simulator was set at the equivalent MMC rated values (cf. Table III), and the experiment was performed during 60 min. Every 5 s a new capacitance estimation was available to be sent to the MMC main controller. Fig. 9 presents the parameter estimation results for the aforementioned conditions while Fig. 10 presents the parameter estimation results for the equivalent MMC operating at different switching and ac terminals frequencies.

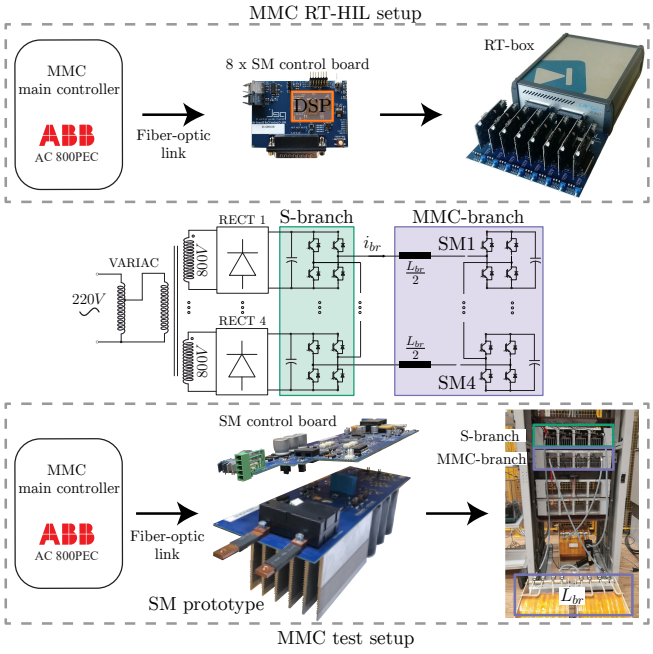


Fig. 11. Central picture shows the scheme of the MMC reduced branch. The top part presents the elements of the MMC RT-HIL setup. The DSP in each SM control board receives and sends the same signals as it would be operating in the SM prototype. Four DSP are loaded with the proposed CHM method as they are emulating the MMC-branch SMs controller. The RT-box simulates in the real-time the power components such as the IGBTs, dc-link capacitors, branch inductance and S-branch dc sources. The bottom part presents the components of the MMC test setup, where four SMs prototype, loaded with the proposed CHM method, form the MMC-branch and other four SMs prototype form the S-branch.

TABLE IV
MMC TEST SETUP CONDITIONS

| Parameter | Symbol | Rated value | Tested value |
|---|---|---|---|
| AC voltage p | $v_{sm}$ | 650 V | 600 V |
| AC current p-p | $i_{br}$ | 45 A | 45 A |
| Phase-shift | $\varphi$ | - | - |
| Modulation index | $m$ | - | 0.7 |
| Switching frequency | $f_{sw}$ | 1 kHz | 1 kHz |
| DC-link voltage | $v_{sm}^{dc}$ | 650 V | 600 V |
| DSP sampling frequency | $f_s$ | 40 kHz | 40 kHz |
| DC-link capacitance | $C$ | 2.25 mF | - |
| DC-link ESR | $ESR$ | 66.6 mΩ | - |
| ASPS + hybrid balancing circuit power | $P_s$ | 16 W | 16 W |

Results show that the CHM method performs satisfactorily for the different capacitors states, even when applied to a capacitance step-change. It is observed that variations in the switching and terminals frequencies have a moderate impact on the performance of the estimation, being the worst case when switching frequency is reduced to half, and terminals frequency is double. In addition, it can be deduced that the switching frequency reduction has less impact than ac terminals frequency increase. This outcome can be explained by observing Fig. 5. As the fundamental frequency increases the ESR component of the impedance increases while the capacitive part decreases, and the impedance magnitude is reduced. On the other hand, a reduction in the switching frequency increases the ESR component; however, the impedance magnitude is still highly attenuated. Finally, presented results prove that the proposed method does not interfere with other routines running in the SM local controller, and it is numerically stable within time, frequency, and impedance variations, as no divergence nor undefined values were found.

### D. MMC test setup

The MMC test setup, depicted in the bottom part of Fig. 11, comprises four series-connected SMs prototype in series with a 2.5 mH inductor to form the MMC-branch. The S-branch is made of four SMs series connected. The S-branch dc sources are made of an isolating transformer with one primary and four secondary windings supplying four full-wave diode rectifiers. The primary side of the transformer is supplied by a single-phase autotransformer (VARIAC). The MMC main controller is based on the industrial controller ABB PEC 800 and a custom-made serial protocol and a fiber-optical link to exchange information with either the SMs prototype or SM control boards.

Four experiments were conducted with the SMs operating accordingly to Table IV. In the first two

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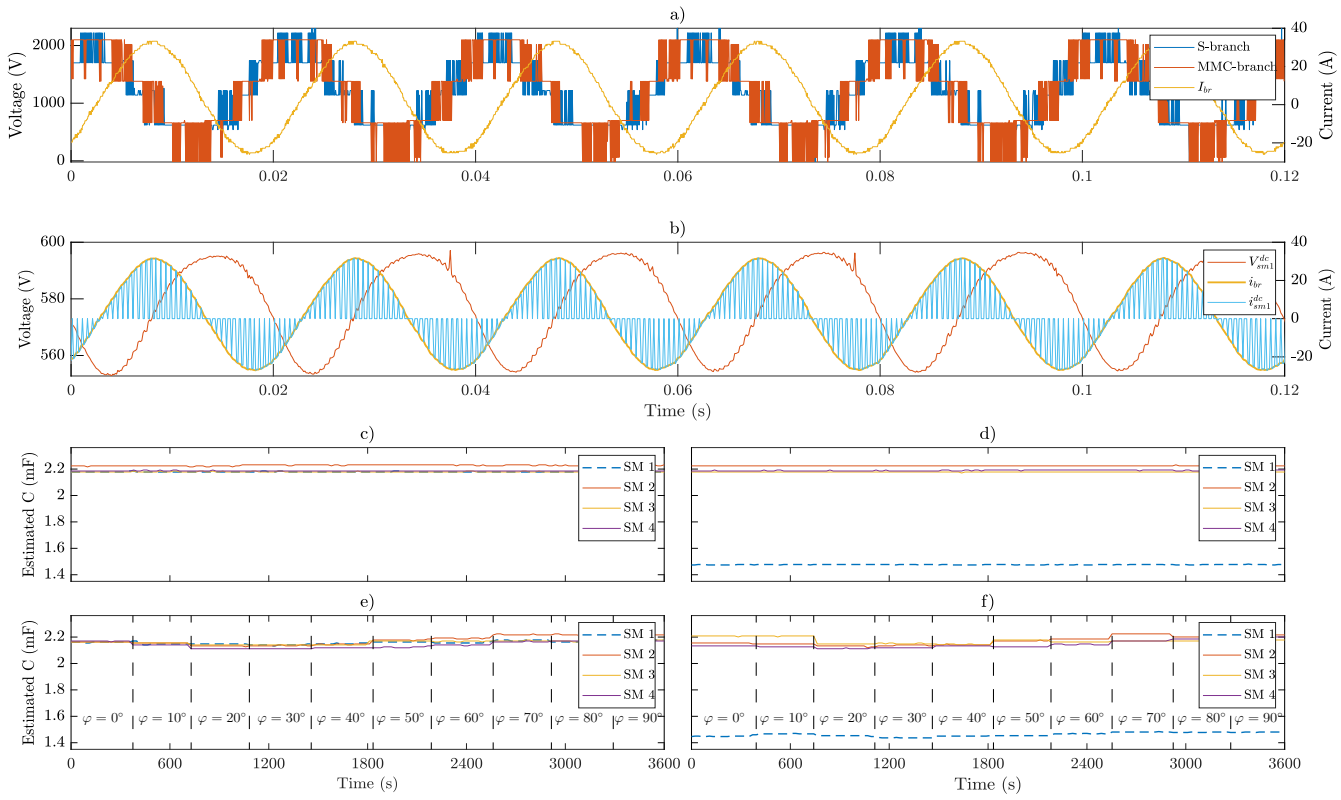


Fig. 12. MMC test setup results. Tests were carried out during 60 min, branch current set at 65 A peak-to-peak, $m(t) = 0.7$ and $v^{dc}_{sm} = 600$ V. Plot a) shows S-branch, MMC-branch and branch current waveforms recorded from scope with the SMs capacitor bank fully populated. Plot b) shows the measured $v^{dc}_{sm}$ and reconstructed $i^{dc}_{sm}$ retrieved from SM1 DSP, with the capacitor bank fully populated. Plot c) presents SMs dc-link capacitance estimation results for capacitor bank fully populated and $\varphi = 90$ř. Plot d) presents SMs dc-link capacitance estimation results for capacitor bank reduced one-third and with $\varphi = 90$ř. Plot e) presents SMs dc-link capacitance estimation results for capacitor bank fully populated and $\varphi$ varying from 0ř to 90ř. Plot f) presents SMs dc-link capacitance estimation results for capacitor bank reduced one-third and with $\varphi$ varying from 0ř to 90ř.

experiments all the SMs were with the full dc-link capacitor bank, however one experiment was carried out with $\varphi = 90$ř and the other with $\varphi$ varying from 0ř to 90ř. In the last two experiments, one-third of the capacitors were removed from the SM1 dc-link. In addition, to reduce the effect of the temperature in the measurements, the experiment was kept running during the hour before the data was taken. Fig. 12 shows the parameter estimation results for the MMC test setup. Plot a) presents the S-branch and MMC-branch voltage, and the branch current waveforms. Plot b) presents $v^{dc}_{sm}$ measurement and reconstructed $i^{dc}_{sm}$ retrieved from SM1. Plots c) and e) show the results considering all the SMs capacitor bank fully populated, while plot d) and f) show the results considering that one-third of the SM1 capacitor bank was removed. Plots e) and d) shows the results with $\varphi = 90$ř while plots d) and f) the results with $\varphi$ varying from 0ř to 90ř. Consistent with the results found in the MMC RT-HIL simulator, the proposed CHM detected a 32.3% capacitance drop which matches with the one-third capacitors removed (plot d). On the other hand, when the power factor is changed, it can be seen that the capacitance estimation reduces its accuracy specially when $\varphi < 60$ř as it was suggested in Section II however, the error respect the cases where $\varphi = 90$ř is less than 5 %.

## V. Conclusion

Despite the extraordinary features of MMC topology, reliability could be of concern since several sensitive and expensive components are present in the SMs. CHM technique of some sort might improved converter reliability further performing state condition monitoring over selected critical components before severe deterioration or major failure occurs. This paper presented anMMC SM dc-link capacitor CHM method, addressing its mathematical development, application scope and practical considerations. In addition, offline simulations, and MMC RT-HIL and MMC experiments were carried out in order to validate the proposed scheme under different SM dc-link impedance conditions and power factors. Results showed that using available SM measurements and the RWLS simple technique it is possible to extract the SM dc-link capacitance with maximum error below 5%, even under extreme capacitance change condition and different converter power factors.

## APPENDIX
## RWLS METHOD

Considering the following discrete-time transfer function that represents a system

$$G(z^{-1}) = \frac{y(z)}{u(z)} = \frac{b_1 z^{-1} + ... + b_m z^{-m}}{1 + a_1 z^{-1} + ... + a_m z^{-m}} \tag{16}$$

it is defined the data vector $\psi^T(k)$ as

$$\psi^T(k) = (-y(k-1)... - y(k-m)|u(k-1)...u(k-m)) \tag{17}$$

and, the parameter vector $\theta^T(k)$

$$\hat{\theta}^T(k) = (\hat{a}_1...\hat{a}_m|\hat{b}_1...\hat{b}_m) \tag{18}$$

then, it is calculated the updating factor $\gamma(k)$

$$\gamma(k) = \frac{1}{\psi^T(k)P_W(k-1)\psi(k) + \frac{1}{w}} P_W(k-1)\psi(k) \tag{19}$$

where $P_W(k-1)$ is the previous measurement covariance matrix and it reflects how reliable are the measurements. $W$ is the weight factor that reflects how reliable the parameters are estimated, and it is chosen constant for this application. Then, the new parameter estimated $\hat{\theta}(k)$ is given by

$$\hat{\theta}(k) = \hat{\theta}(k-1) + \gamma(k)(y(k) - \psi^T(k)\hat{\theta}(k-1)) \tag{20}$$

finally, the covariance matrix $P_W(k)$ for the next iteration is calculated as follow

$$P_W(k) = (I - \gamma(k)\psi^T(k))P_W(k-1) \tag{21}$$

It is important to note that RWLS method performs optimum if the following conditions are met

- the input signal $u(k)$ is perfectly measurable (no noise, no error) and linearly independent,
- the input signal is such that it can excite the system to obtain sufficient information about itself.
- the perturbation is a zero-mean, constant variance, uncorrelated random variable.

## ACKNOWLEDGMENT

This work has received funding in part by Swiss Governmental Scholarship for foreign students and in part from the Swiss Innovation Agency - Innosuisse, as the innovation project 38041.1 IP-ENG.

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