Impact of Embedded Liquid Cooling on the Electrical Characteristics of GaN-on-Si Power Transistors

Luca Nela, Remco Van Erp, Nirmana Perera, Armin Jafari, Catherine Erine, and Elison Matioli

***Abstract*- Wide-Band-Gap semiconductors have enabled considerable miniaturization of power devices, which requires, however, new thermal management solutions to handle the resulting high heat fluxes. Recently, embedded liquid cooling in GaN-on-Si devices was demonstrated as a promising solution by flowing a coolant through microchannels etched in the silicon substrate. However, its impact on power devices' electrical characteristics, especially at high voltage, is yet to be investigated, which is crucial to assess the viability of the technology. Besides, previous demonstrations were limited to relatively low-power devices, while embedded liquid cooling for high-current and high-voltage (650 V) commercial GaN transistors would show the full potential of the technology. Here, we integrate embedded liquid cooling on 650 V, 50 mΩ GaN-on-Si commercial power devices. We demonstrate no negative impact on the device dc or switching performance due to the embedded liquid cooling, which proves the robustness and validity of the technology. Besides, liquid-cooled devices show more than 4× higher current capability and much-improved $R_{ON} \times E_{oss}$ figure-of-merit in a large output current range compared to forced-convection air-cooling, highlighting their potential for high-current applications. Finally, deionized water and a dielectric fluid (3M Novec 7200) are compared as coolants, revealing a trade-off between thermal performance and reliability during high-voltage operation.**

***Index terms*- GaN, HEMTs, Power Devices, Losses Characterization, Liquid Cooling, Microchannels**

I. Introduction

The miniaturization of power devices enabled by wide-band-gap (WBG) semiconductors [1], [2] has resulted in unprecedented heat fluxes [3], which are challenging to handle with conventional thermal management techniques, such as forced-convection air-cooling [4]. Excessive self-heating of the device results in a reduced component lifetime, degraded performance, and limited power density. In addition, the reduced device current capability due to self-heating requires paralleling several transistors for high-current applications, which increases the overall system cost and complexity. Embedded liquid cooling, where a coolant flows through microchannels that are etched directly inside the device substrate, is an effective and well-established technique to cope with high heat fluxes. Such an approach presents important advantages compared to conventional liquid cooling as it enables to eliminate the thermal resistance contributions linked to the device package and thermal interface material, while also significantly increasing the convective heat transfer to the coolant [5], [6]. While this technology was first proposed for silicon logic circuits [7]–[11] and has been studied also for GaN-based RF applications [3], its adoption by power devices is usually limited by their vertical architecture, which prevents the micro-structuring of the substrate. For this reason, the integration of embedded liquid cooling in power devices is a rather unexplored field and its impact on the electrical performance of power transistors, especially at high voltages, is unknown. Yet, GaN-on-Si devices present a lateral device structure on a silicon substrate that is well-suited for deep etching, making it ideal for the integration of this technology.

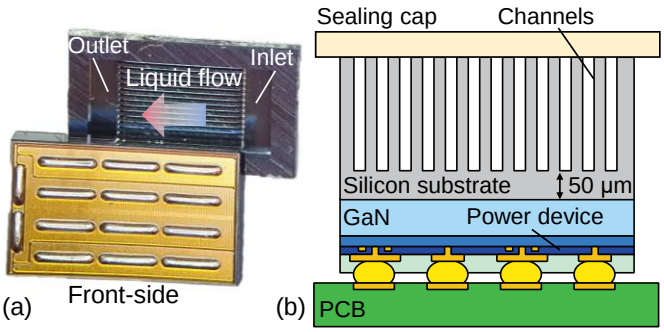


Fig. 1. (a) Top view of the front- and back-side of the 650 V, 50 mΩ commercial GaN power device investigated in this study. On the backside, the micro-channels etched in the Si substrate for the embedded liquid cooling are visible. The device dimensions are 4 mm × 2.4 mm (b) Cross-sectional schematics of the liquid-cooled DUTs mounted on the testing PCB.

Recently, GaN-on-Si devices with embedded microchannels in the silicon substrate were proposed, demonstrating excellent thermal performance [12], [13]. However, despite the promising potential, a thorough characterization of the impact of embedded liquid cooling on the device's electrical performance, especially at a few hundreds of volts, is still lacking, which is crucial to validate the technology for power applications. In particular, it has been shown that the removal of the Si substrate may cause increased switching losses [14], [15], potentially outweighing the benefits from the improved device cooling. Besides, while previous demonstrations were limited to devices operating at relatively low currents and voltages, and fabricated in university facilities [16], embedded liquid cooling of high-current and high-voltage (650 V) commercial GaN devices would show the full potential of the technology for high-power-density applications. In addition, the reduced device-to-device variation of commercial devices enables better determining the possible impact of embedded liquid cooling on the device's electrical performance. Finally, it is still unclear which type of coolant is the best candidate for

Authors are with the Power and Wide-Band-Gap Electronics Research Laboratory, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland (e-mail: luca.nela@epfl.ch, elison.matioli@epfl.ch). This work was supported in part by the Swiss National Science Foundation through Assistant Professor (AP) Energy under Grant PYAPP2_166901, in part by the Swiss Office of Energy under Grant SI501887-01 (MEPCO), and in part by the ECSEL Joint Undertaking (JU) under Grant 826392. The JU receives support from the European Union's Horizon 2020 research and innovation program and Austria, Belgium, Germany, Italy, Norway, Slovakia, Spain, Sweden, Switzerland.

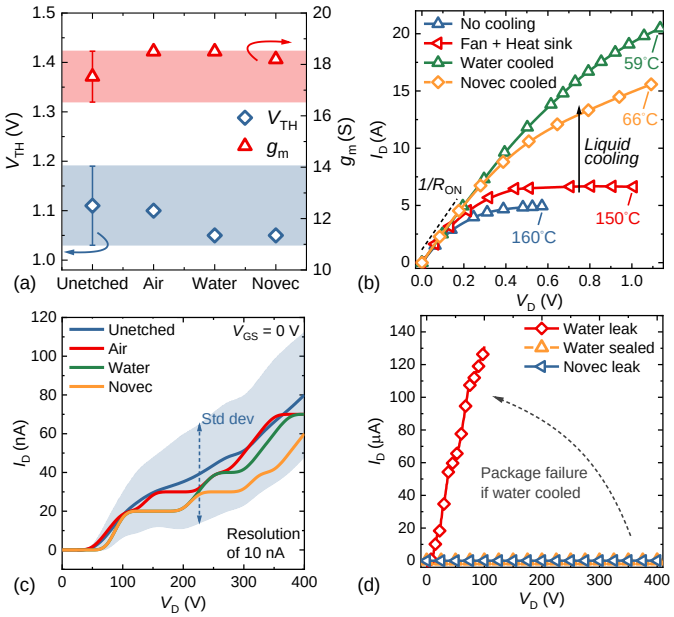


Fig. 2 (a) V_{TH} (at 1 mA) and peak g_m extracted from the device pulsed transfer curve. (b) DC output curve for the DUTs. The liquid coolant flow rate was set to 280 µl/s. (c) Off-state leakage up to 400 V. The resolution of the current measurement is 10 nA. (d) Off-state leakage in case of package failure with DI water and Novec 7200 as coolants flowing in the device.

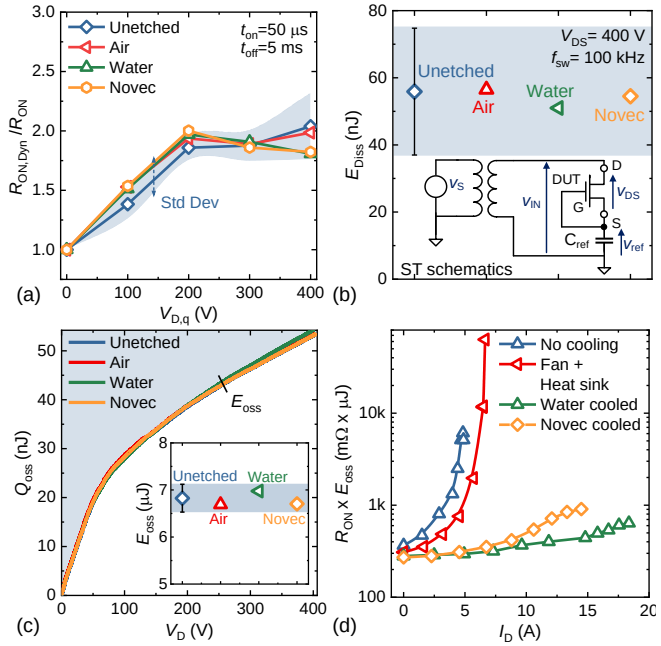


Fig. 3. (a) Dynamic on-resistance as a function of $V_{D,q}$ for unetched DUTs and devices with embedded liquid cooling. (b) E_{Diss} at 100 kHz and v_{DS} of 400 V for the DUTs. The bottom inset shows the ST measurement setup. (c) Q_{oss} as a function of v_{DS} and corresponding E_{oss} extracted from the curve integration. (d) $R_{ON} \times E_{oss}$ figure-of-merit as a function of the device drain current.

embedded liquid cooling of power devices and whether this influences the device's operation.

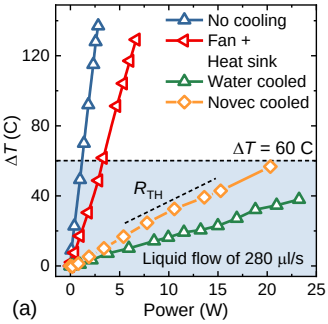
In this work, we investigate the integration of liquid cooling on 650 V, 50 mΩ GaN-on-Si commercial power devices. We perform a thorough characterization of the device dc and switching characteristics and demonstrate no degradation as a consequence of the channel etching in the Si substrate or the liquid flow. Besides, we show that much higher current capabilities and an improved $R_{ON} \times E_{oss}$ figure-of-merit in a large output current range can be achieved by the proposed approach, compared to forced-convection air-cooling. Finally, we present that, while deionized (DI) water provides better thermal performance as a coolant, the dielectric fluid 3M Novec 7200 results in improved package reliability during high-voltage operation.

II. Device Structure and Experimental Setup

The device under test (DUT) is a 650 V, 50 mΩ GaN-on-Si commercial power transistor with a 4 mm × 2.4 mm wafer-level chip-scale package (WLCSP), exposed-backside Si substrate, and solder bumps. No internal connection is present between the source and the substrate, which is floating. However, a similar characterization to the one here presented was performed on a commercial 100 V GaN-on-Si power device with substrate internally grounded, which showed the same behaviour as the one here reported.

Micro-channels were defined on the DUT's backside by optical lithography followed by deep reactive ion etching (DRIE) of the Si substrate (Fig. 1 (a)). This process relies on a simple wafer-scale post-processing, which enables the substrate microstructuring of several chips in a full wafer at the same time, and thus can be very cost-effective. The channel width and spacing were both set to 50 µm while their depth was 330 µm, leaving about 50 µm of Si between the channels and the GaN buffer layers. While the remaining Si layer does not impact significantly the overall thermal resistance (R_{TH}) [16], it preserves the chip's mechanical stability and provides a common potential to the device substrate. Reference transistors with the same design but completely removed Si substrate showed early failure during switching operation, likely due to an uneven potential distribution in the GaN buffer layer as a result of the missing connection to the substrate, and thus were not characterized in this work. Two larger (0.5 mm × 1.7 mm) openings at the device edges provided the inlet and outlet for the coolant (Fig. 1 (a)). Further analyses on the microchannels geometry optimization, in particular of the optimal width and its impact on the thermal resistance and pressure drop [17]–[19], and on the long-term stability under different flow conditions [20] can be found in the literature, and are not the main focus of this work.

Following the micro-channel etching, the devices were soldered to a PCB for testing (Fig. 1 (b)). The device temperature was monitored through a thermistor placed close to the DUT, which was first calibrated to the device surface temperature using an infrared camera. Devices with no microchannels in the Si substrate (*Unetched*) were used as a reference to compare the electrical performance. For the thermal characterization, reference devices with no heatsink under natural convection (*No cooling*) and with a heat sink and fan with a nominal R_{TH} of 5 K/W (*Fan + heat sink*,) were considered. The performance of DI water (*Water cooled*) and the dielectric fluid Novec 7200 (*Novec cooled*) were compared at the same flow rate of 280 µl/s, which resulted in a pressure drop of 500 mbar. While the flow rate has no direct impact on the DUT electrical performance and thus it was not varied in this work, it affects the device thermal resistance as higher flow rates result in a decrease of R_{TH} [5]. Statistical analyses were performed on at least 8 devices of each kind.



(a) (b)

	R_{TH} (K/W)	P_{Max} (W)*	Heat flux (W/cm²)*
No cooling	47.8	1.2	13
Fan + Heat sink	19.5	3	32
Water cooling	1.6	37.5	390
Novec cooling	2.95	21	220

*For ΔT_{Max} of 60 °C

Fig. 4. (a) DUTs temperature increase (ΔT) as a function of the dissipated power over the device for different cooling techniques. (b) R_{TH}, and maximum power and heat flux that can be extracted for a temperature rise of 60 °C.

III. Results and Discussion

Figure 2 (a) shows the threshold voltage (V_{TH}), extracted at 1 mA, and the peak transconductance (g_m) for unetched DUTs (*unetched*), DUTs with etched microchannels with no fluid flowing (*Air*), with DI water cooling (*water*), and with Novec 7200 cooling (*Novec*). No appreciable variation between the different conditions was observed, suggesting that the device gate control is unaffected by the embedded liquid cooling. However, the DUTs output characteristic highly benefited from the more efficient cooling. While the on-resistance (R_{ON}) at room temperature (RT) was identical for all DUTs in Fig. 2 (b), which proves no significant strain variation in the structure affecting the carrier density, the achievable drain current (I_D) for uncooled transistors was strongly limited by the device self-heating (Fig. 2 (b), blue curve). The use of a heat sink and fan alleviated the self-heating degradation but still resulted in an early saturation of the maximum I_D. On the contrary, DUTs with embedded liquid cooling showed a much-reduced R_{ON} increase due to self-heating with no I_D saturation in the measured range. This enabled to achieve a drain current more than 4 times larger than with conventional cooling techniques (Fig. 2 (b)) and offers a promising solution to reduce conduction losses in power devices and the need for device parallelization in high-current applications.

The off-state leakage current of the DUTs was measured up to the rated device voltage and showed no noticeable variation between unetched and liquid-cooled devices (Fig. 2 (c)). However, a significant difference between devices cooled with DI water and Novec 7200 was observed in case of a coolant leak from the liquid cooling package (Fig. 2 (d)). A water leak was particularly detrimental for the DUT voltage blocking capabilities due to the liquid ionization, which led to high leakage current and device failure. On the contrary, a Novec 7200 leak did not impact at all the device off-state leakage (Fig. 2 (d)) because of the coolant large dielectric strength, which results in no additional leakage and improved reliability in case of a package failure.

Previous works have shown an additional dynamic R_{ON} ($R_{ON,Dyn}$) degradation following the Si substrate removal due to the newly created GaN buffer-to-air interface on the device backside [14], [15]. Fig. 3 (a) presents the typical $R_{ON,Dyn}$ degradation measured by pulsed IV for unetched devices, which reached about 2 times the dc value for a stress voltage $V_{DS,q}$ of 200 V, and then saturated. However, no relevant variation was observed as a consequence of the micro-channels etching or the coolant flow. Indeed, the remaining Si layer between the GaN and the microchannels prevents the formation of additional trapping sites at the bottom GaN buffer interface and any variation in $R_{ON,Dyn}$.

To determine the impact of embedded liquid cooling on the device soft- and hard-switching losses a Sawyer Tower (ST) measurement (inset in Fig. 3 (b)) was performed [21]. Fig. 3 (b) shows the energy dissipated at each soft-switching cycle (E_{Diss}) which presented a rather small value [21]–[23] for all DUTs, regardless of the presence of the microchannels or the embedded liquid cooling. This shows that soft-switching losses are not affected by embedded liquid cooling and indicates that traps in the GaN buffer are the main responsible for determining E_{Diss} in these devices [24], [25], which were not impacted by introducing microchannels in the substrate.

By integrating the Q_{oss} versus v_{DS} curve obtained from the ST measurement (Fig. 3 (c)), one can extract the energy stored (E_{oss}) in the device output capacitance, which is dissipated at each hard-switching cycle and represents an important term in hard-switching losses [26]. Since the microchannel etching and the liquid flow do not impact the Q_{oss} nor its dependence on v_{DS}, a constant E_{oss} value is measured for all the DUTs (inset in Fig. 3 (c)). On the other hand, the important device figure-of-merit $R_{ON} \times E_{oss}$, which summarizes the contribution of conduction and hard-switching losses, is greatly improved with the embedded liquid cooling. Thanks to the reduced device self-heating, a low $R_{ON} \times E_{oss}$ value can be maintained for much larger output currents (Fig. 3 (d)), which ensures efficient operation for high-current applications and reduces the need for device oversizing. Besides, no coupling between the electrical signal and the coolant was observed up to a frequency of ~ 6 GHz, which was determined by measuring the transmission parameter (S_{21}) of a waveguide realized on a similar structure with embedded liquid cooling. This shows that no significant electrical coupling to the coolant is present in the whole frequency domain relevant to power electronics.

The improvement in $R_{ON} \times E_{oss}$ is due to the ability of embedded liquid cooling to manage much larger heat fluxes with a reduced device temperature rise, as is shown by the 12-fold reduction in the device thermal resistance compared to the fan + heat sink cooling (Fig. 4). It can also be noted that Novec 7200 results in an R_{TH} which is almost double the one of DI water at the same flow rate. Such a difference can be explained by the larger specific heat capacity of water (4.2 kJ/kgK) compared to Novec 7200 (1.2 kJ/kgK), which directly affects the coolant temperature rise. Nevertheless, Novec 7200 leads to improved reliability in case of package failure during high-voltage operation (Fig. 2 (d)), which poses a trade-off between thermal performance and reliability.

IV. Conclusion

In this work, we have demonstrated 650 V, 50 mΩ GaN-on-Si commercial power devices with embedded liquid cooling in the device substrate. The presented devices show no degradation of the device dc or switching performance as a consequence of the embedded liquid cooling, while they result in higher current capability and much-reduced $R_{ON} \times E_{oss}$ figure-of-merit in a large output current range compared to forced-convection air-cooling.

REFERENCES

[1] K. J. Chen *et al.*, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, 2017.

[2] H. Amano *et al.*, "The 2018 GaN power electronics roadmap," *J. Phys. D. Appl. Phys.*, vol. 51, p. 163001, 2018.

[3] A. Bar-cohenl, J. Maurer, A. Sivananthan, and A. Hamilton, "Near-Junction Microfluidic Thermal Management of RF Power Amplifiers," *IEEE Int. Conf. Microwaves, Commun. Antennas Electron. Syst.*, 2015.

[4] B. Agostini, M. Fabbri, J. E. Park, L. Wojtan, J. R. Thome, and B. Michel, "State of the art of high heat flux cooling technologies," *Heat Transf. Eng.*, vol. 28, no. 4, pp. 258–281, 2007.

[5] S. G. Kandlikar, S. Garimella, D. Li, S. Colin, and M. R. King, *Heat Transfer and Fluid Flow in Minichannels and Microchannels*. 2014.

[6] L. Zhang, K. E. Goodson, and T. W. Kenny, *Silicon Microchannel Heat Sinks*. Springer, 2004.

[7] D. B. Tuckerman and R. F. W. Pease, "High-Performance Heat Sinking for VLSI," *IEEE Electron Device Lett.*, vol. EDL-2, no. 5, pp. 126–129, 1981.

[8] D. B. Tuckerman, "Heat-Transfer Microstructures for Integrated Circuits," 1984.

[9] W. Escher, B. Michel, and D. Poulikakos, "A novel high performance, ultra thin heat sink for electronics," *Int. J. Heat Fluid Flow*, vol. 31, no. 4, pp. 586–598, Aug. 2010.

[10] D. H. Altman, A. Gupta, and M. Tyhach, "Development of a diamond microfluidics-based intra-chip cooling technology for GaN," in *International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, InterPACK*, 2015.

[11] K. P. Drummond *et al.*, "A hierarchical manifold microchannel heat sink array for high-heat-flux two-phase cooling of electronics," *Int. J. Heat Mass Transf.*, vol. 117, pp. 319–330, Feb. 2018.

[12] R. van Erp, R. Soleimanzadeh, L. Nela, G. Kampitsis, and E. Matioli, "Co-designing electronics with microfluidics for more sustainable cooling," *Nature*, vol. 585, no. 7824, pp. 211–216, 2020.

[13] R. van Erp, G. Kampitsis, L. Nela, R. Soleimanzadeh, N. Perera, and E. Matioli, "Bringing the Heat Sink Closer to the Heat: Evaluating Die-Embedded Microchannel Cooling of GaN-on-Si Power Devices," in *2020 26th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2020, pp. 17–23.

[14] R. Reiner *et al.*, "Si-Substrate Removal for AlGaN/GaN Devices on PCB Carriers," *Proc. Int. Symp. Power Semicond. Devices ICs*, pp. 286–289, 2020.

[15] R. Reiner *et al.*, "Characteristics of Hetero-Integrated GaN-HEMTs on CMOS Technology by Micro-Transfer-Printing," *Proc. Int. Symp. Power Semicond. Devices ICs*, 2021.

[16] R. Van Erp, G. Kampitsis, L. Nela, R. S. Ardebili, and E. Matioli, "Embedded Microchannel Cooling for High Power-Density GaN-on-Si Power Integrated Circuits," *Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst. ITHERM*, pp. 53–59, 2020.

[17] J. H. Ryu, D. H. Choi, and S. J. Kim, "Numerical optimization of the thermal performance of a microchannel heat sink," *Int. J. Heat Mass Transf.*, vol. 45, no. 13, pp. 2823–2827, Jun. 2002.

[18] S. J. Kim, "Methods for thermal optimization of microchannel heat sinks," *Heat Transf. Eng.*, vol. 25, no. 1, pp. 37–49, 2004.

[19] V. K. Samalam, "Convective heat transfer in microchannels," *J. Electron. Mater.*, vol. 18, no. 5, pp. 611–617, Sep. 1989.

[20] D. Squiller, I. Movius, M. Ohadi, and P. McCluskey, "Degradation mechanisms of embedded cooling systems for high heat flux power electronics: Particle erosion of silicon and silicon carbide," in *Proceedings of the 16th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITherm 2017*, 2017, pp. 1298–1305.

[21] N. Perera *et al.*, "Analysis of Large-Signal Output Capacitance of Transistors using Sawyer–Tower Circuit," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6777, no. c, pp. 1–1, 2020.

[22] L. Nela, N. Perera, C. Erine, and E. Matioli, "Performance of GaN Power Devices for Cryogenic Applications down to 4.2 K," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, 2020.

[23] A. Jafari *et al.*, "Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12595–12600, 2020.

[24] M. Guacci *et al.*, "On the Origin of the Coss-Losses in Soft-Switching GaN-on-Si Power HEMTs," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 2, pp. 679–694, 2019.

[25] J. Zhuang, G. Zulauf, J. Roig, J. D. Plummer, and J. Rivas-Davila, "An investigation into the causes of coss losses in gan-on-si hemts," *2019 IEEE 20th Work. Control Model. Power Electron. COMPEL 2019*, 2019.

[26] R. Hou, J. Lu, and D. Chen, "Parasitic capacitance Eqoss loss mechanism, calculation, and measurement in hard-switching for GaN HEMTs," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2018-March, pp. 919–924, 2018.