LiNiO Gate Dielectric with Tri-Gate Structure for High Performance E-mode GaN transistors

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Abstract– In this work, a Tri-Gate AlGaN/GaN metal-oxide-semiconductor high electron mobility transistor (MOSHEMT) with lithium nickel oxide (LiNiO) gate dielectric is demonstrated for enhancement-mode (e-mode) operation. The high-quality of pulse-laser-deposited (PLD) LiNiO resulted in e-mode devices without the need for special epitaxial layers, barrier recess, or regrowth. The LiNiO Tri-Gate devices presented a positive Vth, low Ron, large maximum on-current (Ion, max), and high breakdown voltage (Vbr) simultaneously. LiNiO also yielded excellent negative bias temperature instability (NBTI) performance, small hysteresis, and small frequency dispersion.

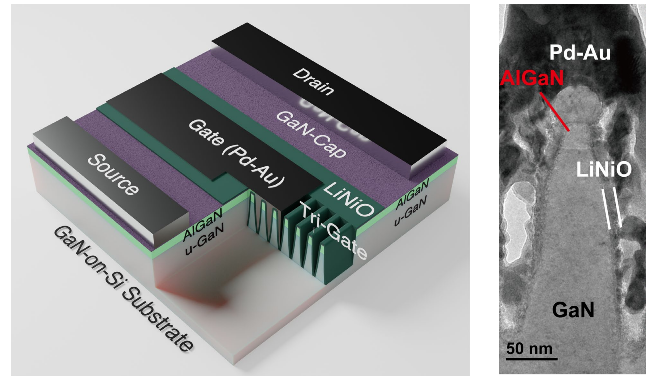
Index Terms – **GaN, HEMT, Enhancement-mode, NiO, LiNiO, tri-gate, Normally-off.**

I. Introduction

P-GaN gates are currently the technology mostly adopted commercially for e-mode GaN-on-Si high electron mobility transistors (HEMTs) due to its high reliability and stability[1]. However, to successfully reach high performance, this technology requires a thin-barrier epitaxy, selective etching p-GaN layer or re-growth of the barrier layer to meet the requirements of low R_{on} and positive V_{th}. An alternative approach is to use p-type oxides as a flexible, and activation free replacement for p-GaN, which offers simple deposition and patterning methods. In this work, a Tri-Gate AlGaN/GaN metal-oxide-semiconductor high electron mobility transistor (MOSHEMT) with lithium nickel oxide (LiNiO) gate dielectric is demonstrated for enhancement-mode (e-mode) operation. The high-quality of pulse-laser-deposited (PLD) LiNiO resulted in e-mode devices without the need for special epitaxial layers, barrier recess, or regrowth. The LiNiO Tri-Gate devices presented a positive V_{th}, low R_{on}, large maximum on-current ($I_{on,\ max}$), and high breakdown voltage (V_{br}) simultaneously. LiNiO also yielded excellent negative bias temperature instability (NBTI) performance, small hysteresis, and small frequency dispersion.

II. Device Structure and Fabrication

The device schematic is illustrated in Fig. 1 (a). The cross-section TEM image of fin region is shown in Fig. 1 (b). To understand the band offset between LiNiO and AlGaN XPS analysis and UV-Vis (Fig. 1 (c)) were performed. In this work, different Li contents were investigated, revealing that the higher Li-content LiNiO films presented larger valence band offset



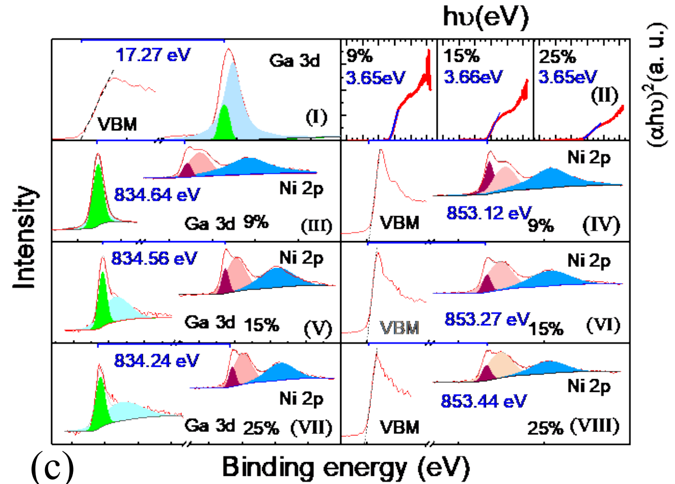


Figure 1. (a) Schematic of the device and cross-sectional view of tri-gate MOSHEMT structure with LiNiO gate dielectric. (b) cross-sectional transmission electron microscope (TEM) image of the LiNiO film on AlGaN/GaN tri-gate structure. (c) X-ray photoelectron spectroscopy (XPS): (I) valence band and Ga 3d core level spectra for AlGaN/GaN. (III)(V)(VII) core level spectra of Ga 3d and Ni 2p from ~3nm thick 9%, 15%, 25% Li doped NiO on AlGaN/GaN. (IV)(VI)(VIII) Ni 2p core level spectra and valence band for ~60nm thick 9%, 15%, 25% Li doped NiO on AlGaN/GaN. (II) absorption ($(\alpha h\nu)^2$) versus hν optical transmission spectra plot from ultraviolet-visible spectroscopy (UV-Vis) for different Li doping concentration LiNiO film on fused silica, band gap values are extracted from these absorption spectra.

(ΔE_V) (Fig. 2 (a)), which is not ideal for e-mode operation. This was confirmed from gated-hall measurements on HEMT structures covered by LiNiO films and Pd gate, which showed a reduction in sheet resistance as the Li-content increased (Fig. 2 (b)), based on this, 9% Li-content film was used in the device fabrication. By depositing LiNiO layers over Tri-Gate

This work was supported in part by the ECSEL JointUndertaking (JU) under grant agreement No 826392.The JU receives support from the European Union's Horizon 2020 research and innovation programme and Austria, Belgium, Germany, Italy, Norway, Slovakia, Spain, Sweden, Switzerland.

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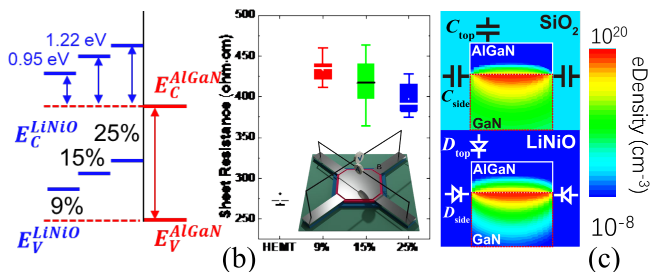

Figure 2. (a) Band alignment between LiNiO and AlGaN determined from XPS and UV-Vis measurements, for Li content of 9%, 15% and 25%. (b) Measured sheet resistance on hall structures patterned on an AlGaN/GaN HEMT structure (black), and three HEMT structures covered with LiNiO with Li concentrations of 9% (red), 15% (green) and 25% (blue) and Pd/Au gate. Inset: schematic of gated hall structure. (c) Simulated electron density distribution in gate width direction of a single fin for top: LiNiO and bottom: SiO_2. 25 nm thick $Al_{0.25}Ga_{0.75}N$, 30 nm-wide 200 nm-tall fins, and 40 nm thick oxide were used for both structure, V_G = 0 V, 5.5 eV Schottky gate and ohmic gate were used for SiO_2 and LiNiO respectively.

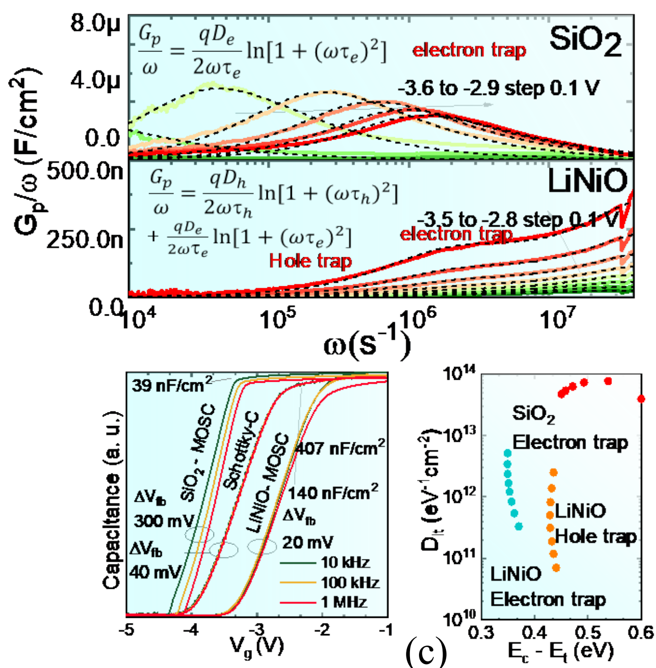

Figure 3. (a) Measured curves and fitting curves of G_p/ω vs ω at different bias voltage for SiO_2 /AlGaN/GaN (top) and LiNiO/AlGaN (bottom). A double trap equation was used for LiNiO MOSC and both are better fitted by continues trap level equation. (b) Multi-frequency (10k Hz, 100kHz, and 1MHz) capacitance versus gate voltage (C-V) characteristics of SiO_2 MOSHEMT capacitor, LiNiO MOSHEMT capacitor, and Ni gate Schottky HEMT capacitor. First capacitor plateau value of three measurements are scaled to similar level for easier V_{fb} shift comparison. LiNiO device shows nearly no dispersion at the rising edge of flatband voltage, while SiO_2 device presents a much larger dispersion among different frequency. (c) Trap state density as a function of energy level for both device, corresponding parameters (ν_{th}, σ_n, σ_p, N_c, N_v) were used for hole and electron trap states in Shockley-Read-Hall statistics.

structures, the channel could be depleted from three sides of the Tri-Gate structures (Fig. 2 (c)).

III. Results and Discussion

The interface properties of LiNiO/AlGaN were studied. As shown in Fig. 3 (b), compared with SiO_2 metal-oxide-semiconductor capacitor (MOSC) and Ni gate Schottky diode,

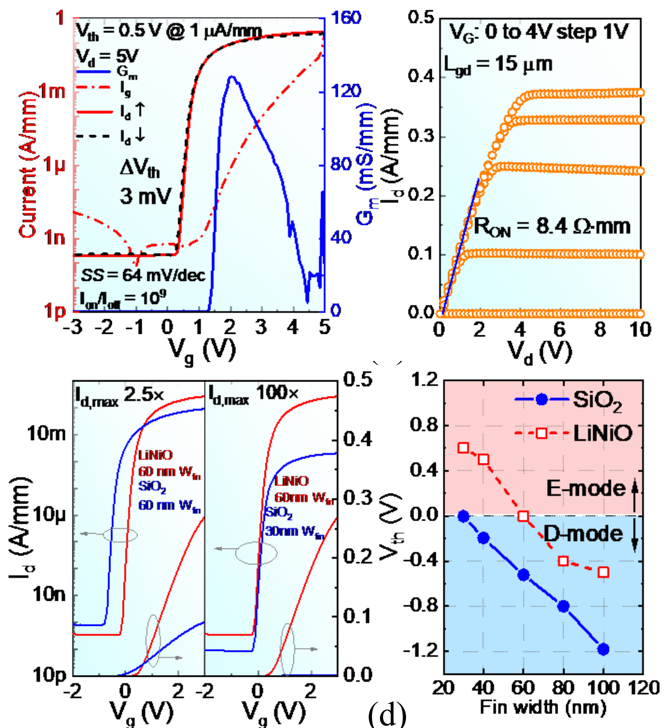

Figure 4. (a) Transfer characteristics of 40nm fin width Tri-Gate MOSHEMT with 9% Li-content LiNiO gate dielectric, measured at V_d = 5 V, a 0.5 V (defined at 1μA/mm) V_{th} was achieved. To characterize hysteresis of device, a 10 mV step and long integration time was used in Keysight B1505A to have a good voltage resolution and hash stress condition. (b) Output characteristic of LiNiO Tri-Gate MOSHEMT.A R_{on} of 8.4 Ω·mm is from the linear fitting of I_d at Vg = 4 V, V_d = 1 V. (c) Transfer characteristic comparison between SiO_2 and 9% LiNiO device under same fin width (left) or same V_{th} (right). Under same fin width, V_{th} shift toward positive, and on-current also increase due to hole injection mode operation. (d) V_{th} (defined at 1 μA/mm) as a function of fin width and gate dielectric. The requirement of fin width to achieve e-mode operation greatly increase from 30 nm to 60 nm due to the junction depletion from the three side of fins.

LiNiO resulted in a small frequency dispersion in the C-V curves, which is similar to the Schottky diode and much smaller than that of SiO_2 dielectric (deposited by thermal ALD at 300°C). To quantitatively study the interface trap states of LiNiO, a model comprised of parallel-connected C_p and G_P in series with a $C_{barrier\ +\ oxide}$ was deployed with frequency dependent impedance measurement. In LiNiO MOSC, two peaks were observed (Fig. 3 (a)), the slower one is likely due to the hole traps at the LiNiO/AlGaN interface, and the faster one is related to trap states the AlGaN/GaN interface, which is also shown in the Schottky diode. The low density and fast emission time of trap states guarantee a high stability operation (Fig. 3(c)), Apart from the electron trap state (also presents in Ni/AlGaN/GaN Schottky capacitor), an additional trap state is shown, which results from the hole trap states at LiNiO/AlGaN interface.

By integrating of LiNiO with Tri-Gates, a V_{th} of 0.5 V (defined at 1μA/mm) was achieved with 40 nm fin width, with a subthreshold swing (*SS*) of 64 mV/dec, on/off ratio of 10^9, peak transconductance (G_m) of 130 mS/mm and small V_{th} hysteresis of 3mV (Fig. 4 (a)). $I_{on,\ max}$ of 380 mA/mm, and R_{on} of 8.4 Ω·mm were also observed (Fig. 4 (b)). Compared with Tri-Gate structures with SiO_2, devices using LiNiO showed a 0.7 V positive shift in V_{th} and greatly improved the on-current for the same fin width (Fig. 4 (c) and (d)).

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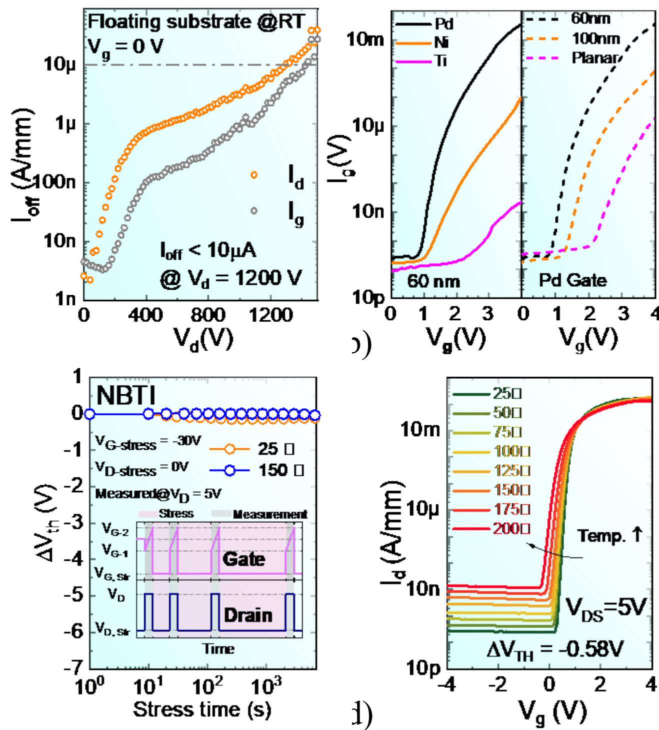

Figure 5. (a) Three terminal breakdown characteristics of devices at $V_g = 0$ V (floating substrate). Due to the usage of ohmic gate off-state leakage is higher than normal MOSHEMTs, however, the device still can hold a voltage over 1500 V without hard breakdown (15μm L_{gd}). Engineering on gate leakage could further increase the soft breakdown voltage. (b) Gate leakage characteristic of devices with different gate metal (left) on 60nm fin, and with different fin width (right) with Pd gate. (c) Threshold voltage shifts of LiNiO gate dielectric Tri-Gate MOSHEMT during the gate bias stress of V_g = - 30 V at 25 °C and 150 °C (inset: waveform of NBTI test) (d) temperature-dependent transfer

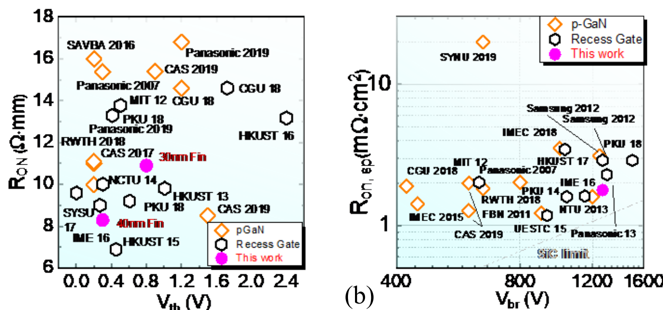

Figure 6. Benchmarking of (a) R_{on} versus V_{th} (defined at 1 μA/mm) compared with e-mode GaN-on-Si HEMTs with p-GaN gate and gate recess technology, (b) $R_{on,sp}$ versus V_{br} by defining V_{br} at $I_{off} \leq 10$ μA/mm, for recess gate, floating substrate result are shown for a fair comparison. $R_{on,sp}$ was calculated considering a 1.5 μm of transfer length for each ohmic contact, which was taken into account for $R_{on,sp}$ calculation. The V_{br} results in the literature were re-calculated by $I_{off} \leq 10$ μA/mm. Table. 1, comparison of reported e-mode Tri-Gate AlGaN/GaN HEMTs.

Thanks to the improved electric field uniformity by the Tri-Gate structure, the devices could hold off-state voltages of 1270 V at I_{off} < 10 μA/mm (under floating substrate) (Fig. 5 (a)). The forward gate current was compared for different gate metals and fin widths showing that LiNiO can works as a low leakage gate dielectric (Pd gate was used in this work to mimic hole injection operation mode [2]) (Fig. 5 (b)). By replace the ohmic gate of Pd to Schottky gate Ti the positive gate leakage greatly reduced, it proves the LiNiO is a good gate dielectric with low leakage. Positive gate leakage on different fin widths with ohmic gate was also studied, gate leakage is smaller under larger fin width device, step coverage difference of LiNiO film among different fin width devices and different flat-band voltage of side wall junction among different fin width devices could be the two reasons for this phenomenon. To evaluate the time-dependent V_{th} stability, NBTI test were done at V_g = -30 V, varying the temperature from 25 °C to 150 °C. Small ΔV_{th} of -50mV (25°C), and -100mV (150°C) respectively were observed under NBTI (Fig. 5 (c)). High temperature transfer characteristic revealed great high temperature V_{th} stability over other solutions using gate dielectrics to achieve e-mode operation[3].

Table 1. Comparison of reported high performance e-mode tri-gate AlGaN/GaN HEMTs

References	This work	[4]	[5]	[6]	[3]
Technologies	LiNiO	NiO_x	Pt Gate	Neg. Charge	e-trap
V_{TH} [a] (V)	0.5	0.45	0.6	0	2.61
SS (mV/dec.)	64	63	110	64	64
BV[b] (V)	1200	650	1100	150	900
R_{on}(Ω·mm)	8.4	9.42	7.4	4.5	12
I_{max}(A/mm)	0.385	0.185	0.58	0.67	0.9
W_{Fin} (nm)	40	60	20	130	100

[a]Extracted at I_D = 1μA/mm.
[b]Under floating substrate except third work, BV was taken at I_D = 10 μA/mm.
[c]Interpolating from fin width versus V_{TH}, the maximum fin width of e-mode operation (at 1μA/mm).

Fig. 6 (a) benchmarks the R_{on} versus V_{th} among reported p-GaN devices and gate recess MOSHEMTs, a small R_{on} was achieved along with positive V_{th}. The high-power figure-of-merit of the proposed device benchmarks very well against recess gate and p-GaN gate devices in the literature (Fig. 6(b)). Table 1 summarizes the device performance in this work and compares with other e-mode Tri-Gate devices. The device in this work presented a positive V_{th}, achieved at a low R_{sheet} (275 Ω/sq.) substrate. A good R_{ON} and V_{BR} were shown at the same time. Tri-Gates require small fin widths to achieve e-mode operation, but by combining with LiNiO, this requirement was significantly reduced, which led to a much smaller Ron for the same V_{th}.

Conclusion

These results show the enormous potential of LiNiO gate dielectric for high-performance and high-reliability e-mode GaN MOSHEMTs.

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