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Gate energy efficiency and negative capacitance in ferroelectric 2D/2D TFET from cryogenic to high temperatures

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We report the fabrication process and performance characterization of a fully integrated ferroelectric gate stack in a $WSe_2/SnSe_2$ Tunnel FETs (TFETs). The energy behavior of the gate stack during charging and discharging, together with the energy loss of a switching cycle and gate energy efficiency factor are experimentally extracted over a broad range of temperatures, from cryogenic temperature (77 K) up to 100 °C. The obtained results confirm that the linear polarizability is maintained over all the investigated range of temperature, being inversely proportional to the temperature T of the ferroelectric stack. We show that a lower-hysteresis behavior is a sine-qua-non condition for an improved energy efficiency, suggesting the high interest in a true NC operation regime. A pulsed measurement technique shows the possibility to achieve a hysteresis-free negative capacitance (NC) effect on ferroelectric 2D/2D TFETs. This enables sub-15 mV dec^{-1} point subthreshold slope, 20 mV dec^{-1} average swing over two decades of current, I_{ON} of the order of 100 nA μm^{-2} and $I_{ON}/I_{OFF} > 10^4$ at $V_d = 1$ V. Moreover, an average swing smaller than 10 mV dec^{-1} over 1.5 decades of current is also obtained in a NC TFET with a hysteresis of 1 V. An analog current efficiency factor, up to 50 and 100 V^{-1} , is achieved in hysteresis-free NC-TFETs. The reported results highlight that operating a ferroelectric gate stack steep slope switch in the NC may allow combined switching energy efficiency and low energy loss, in the hysteresis-free regime.

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INTRODUCTION

The scaling of complementary metal-oxide-semiconductor (CMOS) is facing several fundamental and technical challenges due to the inability to remove the heat generated in the switching process¹. This results in jeopardizing the performance of aggressively scaled CMOS technology nodes^{2,3}. The origin of this issue can be traced back to the inability to scale the power supply, which is limited by the physic of thermionic injection of carriers. Thus, the subthreshold slope (SS) can not be any lower than 60 mV per decade at room temperature (Boltzmann limit). This impedes a fundamental limit to lowering the dynamic power consumption of a transistor. One of the possible solutions to overcome the Boltzmann limit is to rely on other mechanisms of carrier injection to break through the barrier^{4–6}. Tunneling field effect transistors (TFETs) have been proposed to overcome this thermionic limit of SS by exploiting the Band-to-Band tunneling (BTBT) of carriers as the charge transportation mechanism⁴. The use of conventional three-dimensional semiconductors (like silicon, germanium and III–V materials) as TFETs have shown sub-60 mV per decade subthreshold swing at room temperature^{4,7}. However, the presence of band-tail states and trap assisted tunneling paths in such devices would drastically deteriorate the turn-on slope^{8,9}.

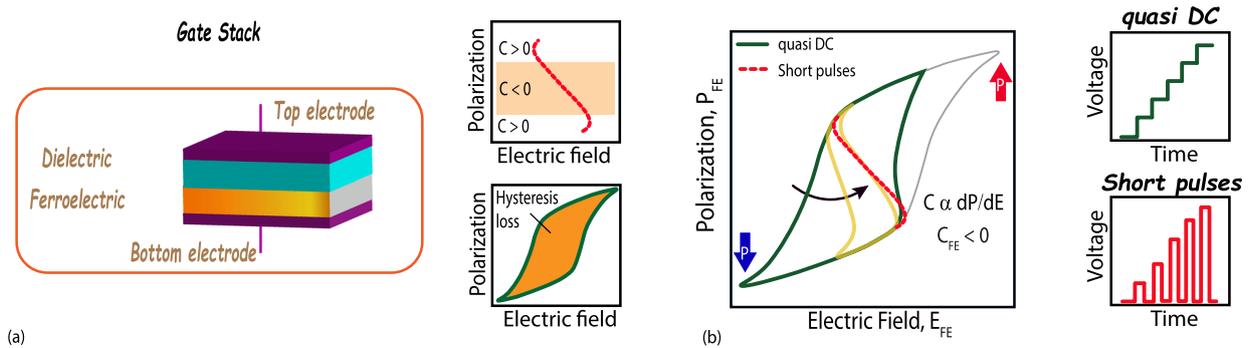
Recently, two-dimensional (2D) materials come to the forefront with their excellent electronic properties and the possibility of assembling atomically sharp van der Waals heterojunctions¹⁰, making them promising candidates for replacement of conventional TFETs and silicon. Although there have been several reports of tunneling in 2D-based heterojunctions with negative differential resistance (NDR) observed at room temperature or cryogenic^{11–15}, this type of devices suffer from poor SS. Among the reported configuration of 2D/2D TFETs^{11,13–19}, $WSe_2/SnSe_2$ heterostructure has recently attracted a great deal of attention due to its near broken band alignment which enables BTBT. The band alignment of the $WSe_2/SnSe_2$ heterostructure has been

derived by density functional theory (DFT) calculations that shows a type III, broken gap with an expected energy overlap of 26 meV²⁰. Moreover, the peculiar electronic properties of the two members of transition metal dichalcogenide (TMD) constituting this configuration make this system more favorable. Tunability of WSe_2 for both electron and hole transport^{21,22} with relatively high mobility²³, presents this material as one of the outstanding candidates for the realization of a single material 2D CMOS technology. On the other hand, the electrostatic control on the degenerately n-doped $SnSe_2$ is extremely low²⁴. Several demonstrations of NDR in $WSe_2/SnSe_2$ heterojunction devices have been recently reported, but there are only two reports on n-type and p-type TFETs with minimum SS of 50 and 35 mV per decade over one decade of drain current^{17,20}.

Another way of achieving subthermionic SS is to benefit from the differential voltage amplification of an active gate, such as exploring the negative capacitance (NC) of ferroelectric materials²⁵. The negative capacitance originates from the dynamics of the stored energy in the phase transition of ferroelectric materials²⁶. This provides an internal voltage amplification in an MOS device and hence, the channel surface potential can be changed faster than the gate voltage in an NC field-effect transistor (NC-FET)^{27,28}. The practical implementation of the NC is difficult due to its instability. However, it is possible to partially or fully stabilize the ferroelectric capacitor in the NC state by placing it in series with a dielectric capacitor of proper value²⁹. Until now, such NC effect has been exploited for conventional FETs^{26,30–34}, TFETs^{34,35}, and 2D-FETs^{36–38} but never for a 2D/2D TFET. Additionally, the ferroelectric is externally connected to the gate of the conventional TFETs in the previous reported NC TFETs³⁴. Accordingly, it would be highly desirable to explore the performance of an integrated NC 2D/2D TFET.

In this context, we have designed and experimentally characterized the NC 2D/2D TFET by incorporating the CMOS

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Effect of temperature on ferroelectric and NC effect

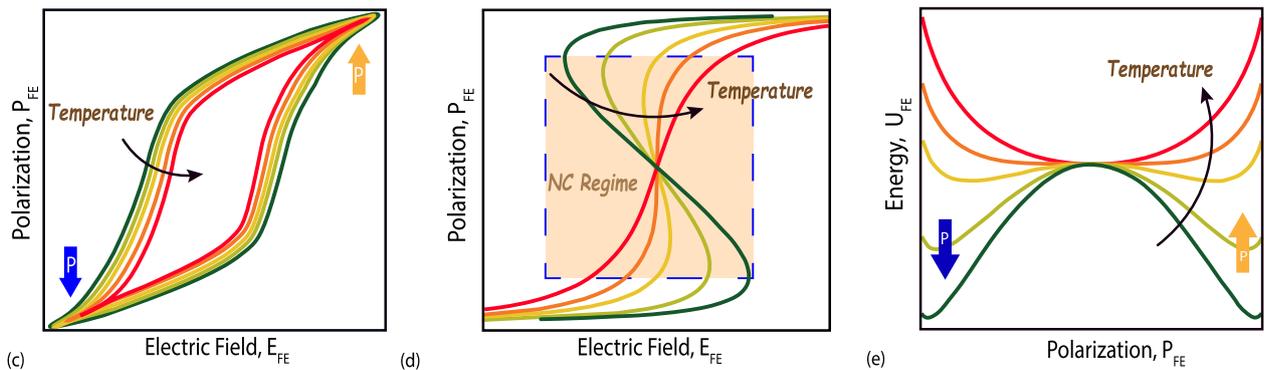


Fig. 1 Rationale and principle. **a** Schematic of the gate structure (left). The hysteretic behavior leads to an energy loss (right bottom) while the stable NC region without hysteresis improves the energy behavior of the gate stack (right top). **b** Qualitative comparison between quasi-DC and pulsed measurement techniques. **c** Temperature-dependent $P - E$ loops. **d, e** The evolution trend of the NC effect and the potential energy U with increasing temperature.

compatible poly-crystalline Si:HfO₂ as the NC booster into the gate stack of a 2D/2D tunneling transistor. The bottom gated WSe₂/SnSe₂ p-type TFET is fabricated based on the dry transfer technique and both the WSe₂ FeFET and WSe₂/SnSe₂ FeTFET are characterized in DC mode. Gate energy efficiency factor is defined and studied at different temperatures to highlight the importance of exploiting the NC region of ferroelectrics. Additionally, this work reports a detailed study on energy charging/discharging behavior of the gate stack across a wide range of temperatures, from temperatures close to operational ones in modern microprocessors (100 °C) down to 77 K. The proposed device exhibits an improved SS down to 6.5 mV per decade with a hysteresis of 1 V in a partially matched design, using a pulsed measurement technique. In another device structure with a fully matched design of capacitances, an average SS of 20 mV per decade over two decades of drain current and minimum point SS less than 15 mV per decade are achieved with negligible hysteresis. An enhanced current efficiency factor, g_m/I_d , up to 100 V⁻¹ is also obtained. The NC effect in 2D/2D TFETs is studied by evaluating the device performance at high temperatures, up to 100 °C, in both DC and pulsed measurement techniques. The proposed device offers performance beyond the state of the art 2D/2D systems^{11,13–20}.

A negative capacitance transistor has this property that the gate stack contributes to the differential voltage amplification and enhances the surface potential at a given gate voltage from weak to strong inversion, acting both as a subthreshold and overdrive booster³⁹. In order to have a maximum enhancement due to the NC effect, the negative value of the ferroelectric's NC (C_{FE}) should be relatively close to the intrinsic gate capacitance (C_{int})^{40,41}.

Additionally, to achieve an exploitable stable regime for negative capacitance transistor in the non-hysteretic operation mode, the total capacitance of the structure should remain positive in the whole range of operation⁴². Note that a negative value of the total capacitance leads to instability and hysteretic behavior. It is well known that a hysteretic $I_d - V_g$ leads to dissipated energy (E_h), which is not favorable for energy-efficient switches (Fig. 1a).

In general, the electrostatic energy of a capacitor is given by

$$\delta E = VdQ = V \frac{dQ}{dt} dt = VIdt, \quad (1)$$

where V is the applied voltage and Q is the electric charge. Similarly, the consumed energy during the charging and discharging of the gate capacitor at each point can be written as

$$\delta E_{(i)} = V_{g(i)} I_{g(i)} dt, \quad (2)$$

where $V_{g(i)}$ is the applied voltage and $I_{g(i)}$ is the current passing through the gate stack at the bias $V_{g(i)}$. Therefore, the energy dissipated in the gate stack due to hysteresis can be calculated as

$$\delta E_{h(i)} = |\delta E_{ch(i)}| - |\delta E_{dis(i)}| = |V_{g(i)} I_{gch(i)} dt| - |V_{g(i)} I_{gdis(i)} dt|, \quad (3)$$

$$E_h = \sum_i^N \delta E_{h(i)}. \quad (4)$$

Thus, the efficiency of the gate stack can be defined as

$$\eta = 1 - \frac{E_h}{E_{ch} + E_{dis}}, \quad (5)$$

where E_{ch} and E_{dis} are the total energy supplied during charging and discharging, respectively. As can be seen from Eq. (5), a

hysteresis-free NC transistor has an efficiency factor of $\eta = 1$ since $E_n = 0$. In another word, gate energy efficiency factor is defined to evaluate the gate control ability for the realization of steep slope switches with negligible hysteresis loss.

Figure 1b qualitatively compares the impact of the pulsed and quasi-DC measurement techniques on the NC effect of ferroelectric materials. The advantage of the pulsed technique is that it applies short pulses for both biasing and measurement, which allows us to investigate the device performance before the gate leakage jeopardizes the NC effect^{43,44}.

The differential voltage amplification of an NC booster, integrated into the gate stack of a TFET, is highly beneficial for energy band bending and enhancing the BTBT probability. This can be understood by considering the SS equation of a TFET. According to the transport mechanism by Sze and Ng⁴⁵, the SS can be obtained by taking a derivative of the interband tunneling current, $I_d = aV_{\text{eff}} \xi e^{-b/\xi}$:

$$SS = \left[\frac{\partial(\log I_d)}{\partial V_g} \right]^{-1} = \text{Ln}10 \left[\frac{1}{V_{\text{eff}}} \frac{\partial V_{\text{eff}}}{\partial V_g} + \frac{\xi + b}{\xi^2} \frac{\partial \xi}{\partial V_g} \right]^{-1}, \quad (6)$$

where V_{eff} is the tunnel-junction bias, a and b are the factor related to the properties of the materials constituting the heterojunction and the cross-section area (A), and ξ is the electric field. Accordingly, the NC effect of the incorporated ferroelectric in the gate stack of 2D/2D TFETs can modulate the channel and tunneling probability faster, providing a steeper switching. Furthermore, the derivation of ξ on V_g can be boosted significantly employing NC. Supplementary Fig. 1 shows a qualitative comparison between the input transfer characteristics of a MOSFET, TFET, and NC TFET.

It is well known that the performance of a ferroelectric transistor strongly depends on the temperature⁴⁶ as ferroelectric's properties are a function of temperature^{47,48}. Figure 1c qualitatively shows the polarization hysteresis loops at different temperatures, from which the evolution of the coercive field and remnant polarization can be identified depending on the temperature. It is worth-mentioning that, depending on the field regions where the measurements are performed in, temperature scaling of the polarization hysteresis differs significantly in terms of the shape, area, remnant polarization, and coercive field⁴⁹. The effects of temperature, time and electric field on polarization switching dynamics have been successfully predicted by Vopsaroiu et al. based on the classical Landau–Devonshire free energy functions in their non-equilibrium statistical model⁵⁰. For all independent switching regions (defined as elementary polar sites by the authors), the nucleation process is considered to be activated when the region of reversed polarization reaches a critical volume V^* . The reversal time of the material is determined by the switching rate of the critical volume V^* . The increased thermal energy facilitates the transition over the energy barrier, and therefore the reversal time is much faster. For our measurements with fixed frequency or electric field ramping rate, this effect is represented by a reduction of the coercive field with increasing temperature. This can be also expressed analytically based on Vopsaroiu's model⁵⁰, in which the coercive field and the temperature are related by the following equation:

$$E_C \cong \frac{W_B}{P_s} - \frac{K_B T}{V^* P_s} \text{Ln} \left(\frac{v_0 \tau}{\text{Ln}(2)} \right), \quad (7)$$

where W_B is the energy barrier per unit volume, P_s is the spontaneous polarization, v_0 is the soft mode attempt frequency, V^* is the critical nucleation activation volume, and τ is the time scale of the measurement.

Furthermore, the influence of temperature on the negative-susceptibility region of the $P-E$ curve, which is called the "S" shape behavior, is qualitatively illustrated (Fig. 1d). The NC region narrows down by increasing the temperature and almost

disappears at higher temperatures. This behavior can be explained if we carefully look at the dielectric susceptibility according to the Curie–Weiss law

$$\chi_e = \frac{C}{T - T_C}, \quad (8)$$

where the constant of proportionality C is the Curie constant and T_C is the Curie temperature of the material where the phase transition occurs. The interest of this study is in the state of the system below T_C , where the material exhibits negative susceptibility. Moreover, the relative permittivity for a ferroelectric can be approximated by $\epsilon_r = 1 + \chi_e \approx \chi_e$. This indicates that ferroelectric materials intrinsically exhibit negative permittivity and thus negative capacitance. Accordingly, the NC effect in ferroelectric gate stack transistors is inversely proportional to the temperature T .

The thermodynamic free energy density (U) described within Landau–Ginzburg–Devonshire (LGD) theory⁵¹ can be expressed as a polynomial expansion up to the fourth order

$$U(T) = \frac{\alpha(T)}{2} P^2 - \frac{\beta}{4} P^4 - PE, \quad (9)$$

where α and β are Landau coefficients. It should be noted that the coefficient α represents the reciprocal of the dielectric susceptibility. Given the temperature dependency of χ_e , α is considered linearly dependent on temperature while β is temperature independent. Therefore, the energy landscape of the ferroelectric is dependent on temperature⁵² which is shown qualitatively in Fig. 1e.

According to the device configuration, there are multiple temperature dependencies in the transfer characteristic: ferroelectric properties, TAT, Shockley-Read-Hall (SRH), and BTBT. When the temperature decreases, the effect of SRH and TAT components is relatively minimized while the BTBT term of the current has a little dependence on the temperature. Therefore, the BTBT could prevail as the main carrier transport mechanism and hence, a relative improvement in the SS is expected in low temperatures. The enhancement of SS can be also attributed to a more effective NC at low temperatures. It is worth-noting that other factors such as 2D/2D heterojunction area, trap density, and defect variability can also cause significant variability at room temperature. Although these variability effects can be relatively removed at our low temperature study, deep cryogenic measurement is required to completely suppress the impact of the noted parameters.

Based on Eqs. (2–5), the gate energy efficiency of a ferroelectric transistor mainly depends on hysteresis (ΔV) and gate current (I_g) during charging and discharging. As mentioned earlier in this section, the hysteresis of ferroelectric materials decreases by increasing the temperature. Therefore, it is expected that the gate energy efficiency increases at elevated temperatures. However, the other factor that plays an important role in device efficiency, the gate current, increases with the temperature which may lead to a higher energy loss. Therefore, these two effects provide two opposite trends for the gate energy efficiency versus temperature and the resulting behavior is complex and was never reported to date. The experiments reported in next sections will reveal the overall gate energy efficiency dependence on temperature from cryogenic to high temperature, in ferroelectric gate stacks using Si:HfO₂ applied to a Tunneling FET device.

RESULTS AND DISCUSSION

Fully integrated NC 2D/2D TFET

The process flow designed for the fabrication of our proposed NC WSe₂/SnSe₂ TFET devices is summarized in Fig. 2a. First, a LOR/AZ1512 bilayer was patterned by conventional photolithography to define the bottom gate contact. Then, 50 nm of TiN was

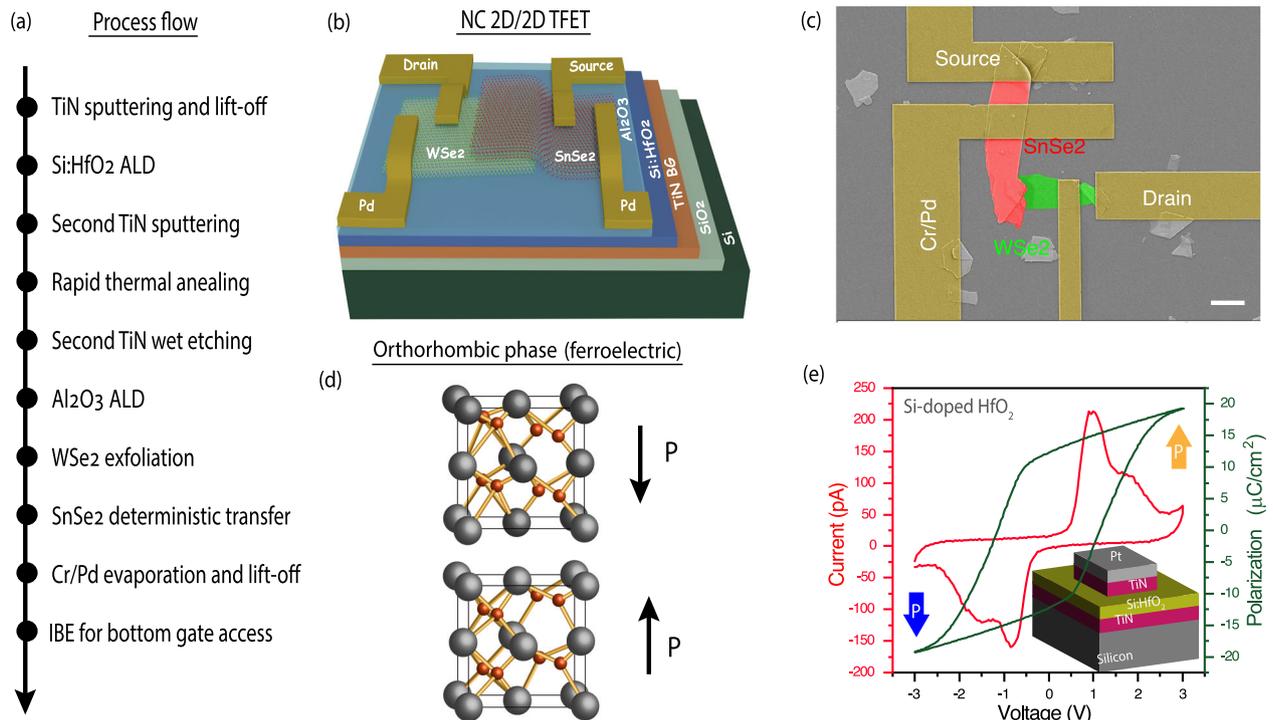


Fig. 2 Fully integrated NC 2D/2D tunnel FET. **a** Summary of the process flow followed for the realization of the NC WSe₂/SnSe₂ TFET. **b** Schematic diagram of the NC 2D/2D vdW vertical TFET in which 16 nm of Si:HfO₂ is integrated into the gate stack (4-nm-thick Al₂O₃) of a back gated WSe₂/SnSe₂ heterojunction TFET. **c** SEM image of the fabricated device, showing WSe₂ and SnSe₂ flakes for the junction, the Pd contacts, and the overlapped tunneling region (scale bar 2 μm). **d** The crystal structure of Si:HfO₂ in its two stable polarization states, which occurs due to the ionic movement. **e** The *P*–*V* and *I*–*V* curves of a 16-nm-thick Si:HfO₂ ferroelectric capacitor, exhibiting a sharp and coherent switching.

sputtered and lifted-off. Atomic layer deposition (ALD) of 16-nm-thick Si:HfO₂ followed by the sputtering of top TiN layer were performed to complete the metal-ferroelectric-metal (MFM) stack. To activate the ferroelectricity of Si:HfO₂, rapid thermal annealing (RTA) in nitrogen ambient was done at 600 °C for 2 min. The bottom gate structure was completed by wet etching the second TiN layer and depositing 4 nm Al₂O₃. 2D flakes of WSe₂ were mechanically exfoliated directly onto the gate stack. Afterward, SnSe₂ flakes were exfoliated onto a PDMS stamp stuck on a glass slide. The glass slide was used to deterministically transfer SnSe₂ flakes on previously selected WSe₂ flakes^{22,53}. The electrodes of source and drain were established by a standard E-beam lithography on a MMA/PMMA bilayer resist, followed by the evaporation of Cr/Pd (5 nm/50 nm) and lift-off process. Finally, the stack was locally etched by ion beam etching (IBE) to provide electrical access to the TiN contact.

A three dimensional schematic view of the final configuration is shown in Fig. 2b which consists of 16 nm polycrystalline Si:HfO₂ and 4 nm amorphous Al₂O₃ layers as the gate dielectric of a WSe₂/SnSe₂ heterojunction TFET. A false-color scanning electron microscopy (SEM) image of a representative NC WSe₂/SnSe₂ TFET is illustrated in Fig. 2c. The different flakes, the heterojunction region, and the metallic contacts are visible in this image. The present devices are fabricated on 8-nm-thick WSe₂ flakes and relatively thick SnSe₂ flakes (larger than 50-nm-thick), as confirmed by the atomic force microscopy (AFM) profile shown in Supplementary Fig. 2. Figure 2d is the crystal structure of two stable polarization states of Si:HfO₂. The MFM capacitor used in this work is characterized by measuring both the *I*–*V* and polarization hysteresis loops to ensure ferroelectric behavior (Fig. 2e). A sharp and coherent domain switching is observed and

further validated by piezoelectric force microscopy (PFM) (Supplementary Fig. 2).

DC Characterization

The electrical properties of individual WSe₂ and SnSe₂ flakes have been characterized at room temperature to confirm the electrical polarity of these two kinds of semiconductor. The DC characteristics of both SnSe₂ and WSe₂ FeFETs are fully demonstrated in the Supplementary Figs. 3 and 4. The electrical characteristics of the WSe₂/SnSe₂ heterostructure FeTFET fabricated on the same flake of WSe₂ FeFET are also shown in Supplementary Fig. 5. The input transfer curve of the fabricated device exhibits the p-type tunneling transistor behavior at RT. Comparing the DC characteristics of the proposed WSe₂/SnSe₂ heterostructure FeTFET and WSe₂ FeFET confirm that the main charge injection mechanism in our 2D/2D device is BTBT of carriers²⁰. A reference 2D/2D TFET with a 10-nm thick HfO₂ gate has been fabricated to evaluate the impact of ferroelectric in the gate stack of a 2D/2D system. The device is fully characterized and the results are reported in the Supplementary section.

Energy charging and discharging at cryogenic temperatures

The energy charging and discharging behavior of the fabricated ferroelectric gate stack has been investigated by decreasing the temperature down to 77 K (liquid nitrogen). Figure 3a shows the double sweep transfer characteristics, *I*_d – *V*_{gr}, at different temperatures for a drain voltage *V*_d of 1 V (2D/2D FeTFET#1). The extracted hysteresis values at different temperatures are shown in the inset of Fig. 3a. The hysteresis is effectively reduced when the temperature decreases down to 77 K. The smaller hysteresis for lower temperature is possibly related to the larger coercive field of

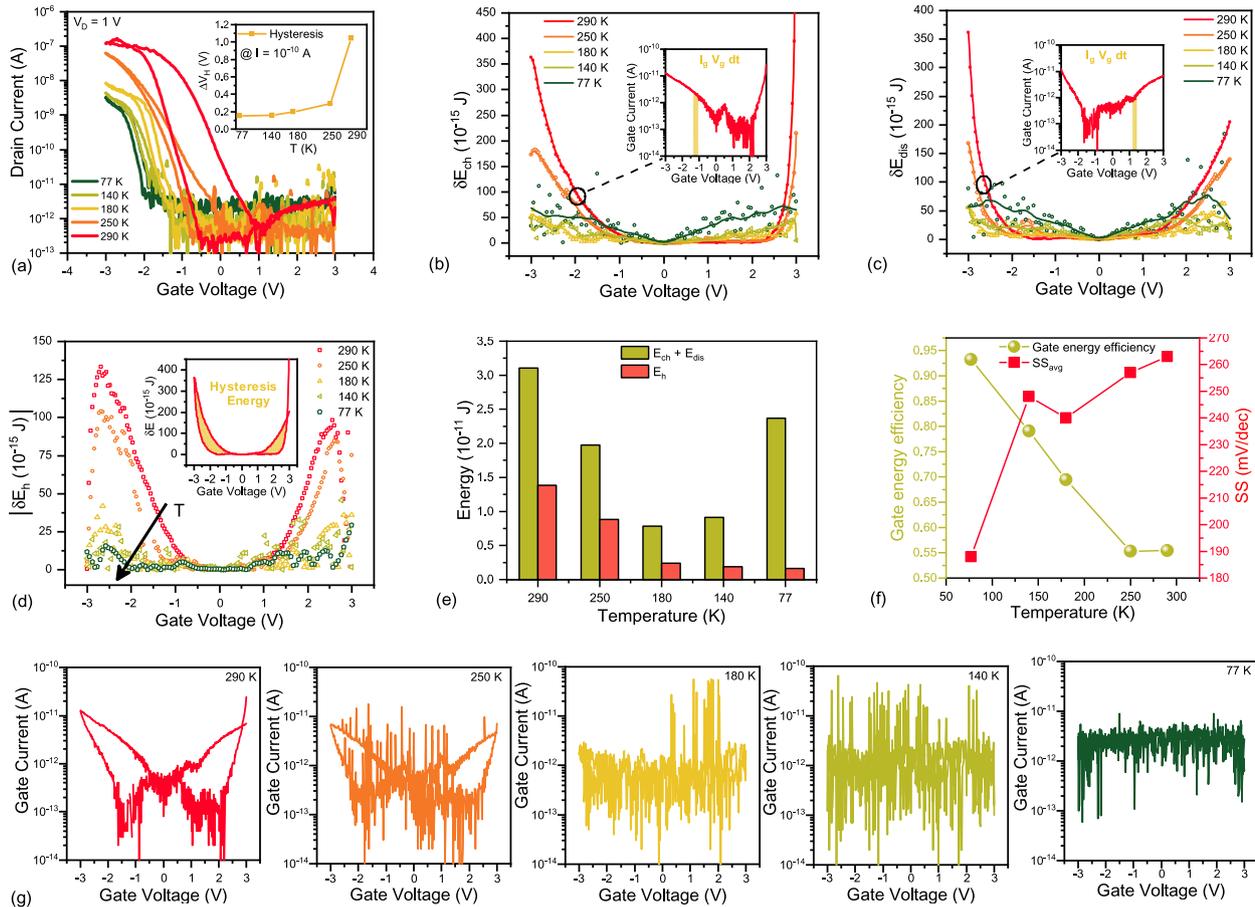


Fig. 3 Electrical and energy behavior characteristics of the 2D/2D FeTFET at low temperatures. **a** Performance of the device at low temperatures, down to 77 K, while the V_d is set to 1 V. The extracted point and average subthreshold swings show a little dependence on the temperature (Inset figure). **b, c** Charging and discharging energy behavior of the gate stack and **d** corresponding energy loss at low temperatures ($V_d = 1$ V). **e** Evolution of the hysteresis energy and total supplied energy with decreasing temperature. **f** Extracted average subthreshold swing and gate energy efficiency factor at different temperatures. **g** Gate current vs gate voltage at different temperatures.

the ferroelectric, and to the beneficially effect of low temperatures to thermally de-activate traps at the interface between WSe_2 and the back gate and the $WSe_2/SnSe_2$ interface. The direct comparison between the transfer characteristics, SS as a function of the drain current and output characteristics of the device for both the 77 and 290 K temperatures are shown in Supplementary Fig. 7. Additionally, the output characteristic of the device is studied to further validate the BTBT transportation mechanism in our device. A negative differential resistance effect, NDR, is observed at 77 K, which fully confirms the band-to-band tunneling of carriers in a $WSe_2/SnSe_2$ heterostructure tunnel FET device (Supplementary Fig. 8). The device performance at 77 K is reported in Supplementary Fig. 8, showing the resulting improvement at cryogenic temperatures as well as the robustness of our proposed device at low temperatures.

The energy charging and discharging behavior of the gate stack in forward and reverse sweeps of the gate voltage at the investigated temperatures are studied. The energy plots are obtained according to Eq. (2) and based on the forward and reverse current of the gate shown in Fig. 3g. The extracted energy during charging (δE_{ch}) and discharging (δE_{dis}) as a function of the gate voltage are demonstrated in Fig. 3b, c, while the hysteresis energy (δE_h) is highlighted in Fig. 3d. Figure 3e illustrates the total energy during charging/discharging and the dissipated energy due to hysteresis (E_h) for all the temperatures. Lower hysteresis energy is observed with the decrease of the temperature. This can

be explained by considering the fact that due to the larger coercive field and multi-domain structure of $Si:HfO_2$, only a small fraction of the polarization gets switched for the investigated range of voltages at low temperatures, providing a relatively smaller hysteresis. On the other hand, at cryogenic temperatures, the slope of the S-shape characteristics offers better conditions for a larger stable range of NC, which would result in non-hysteretic $I_d - V_g$ characteristics. Therefore, overall a much lower energy loss is expected at cryogenic temperatures, as confirmed by our experimental results. Additionally, the total charging and discharging energies during forward and reverse sweeps is decreasing with temperature and it starts to increase above 180 K. We believe that the increase of the charging/discharging energy below 180 K is due to the fact that the gate current reduces below the detection limit of our measurement setup, and cannot be distinguished by the noise. Therefore, a measurement system with higher precision would confirm that the charge/discharge energy decreases monotonically by reducing the temperature. The gate energy efficiency factor and average value of SS with respect to the studied temperatures are shown in Fig. 3f. The continuous yet still limited improvement of SS with temperature indicates that the trap-assisted tunneling (TAT) may remain a significant contribution to the charge transport, and lower temperatures are needed to fully remove it to significantly improve the slope^{54,55}. Such an assumption is also consistent that even an improved NC effect at a lower temperature will have little effect

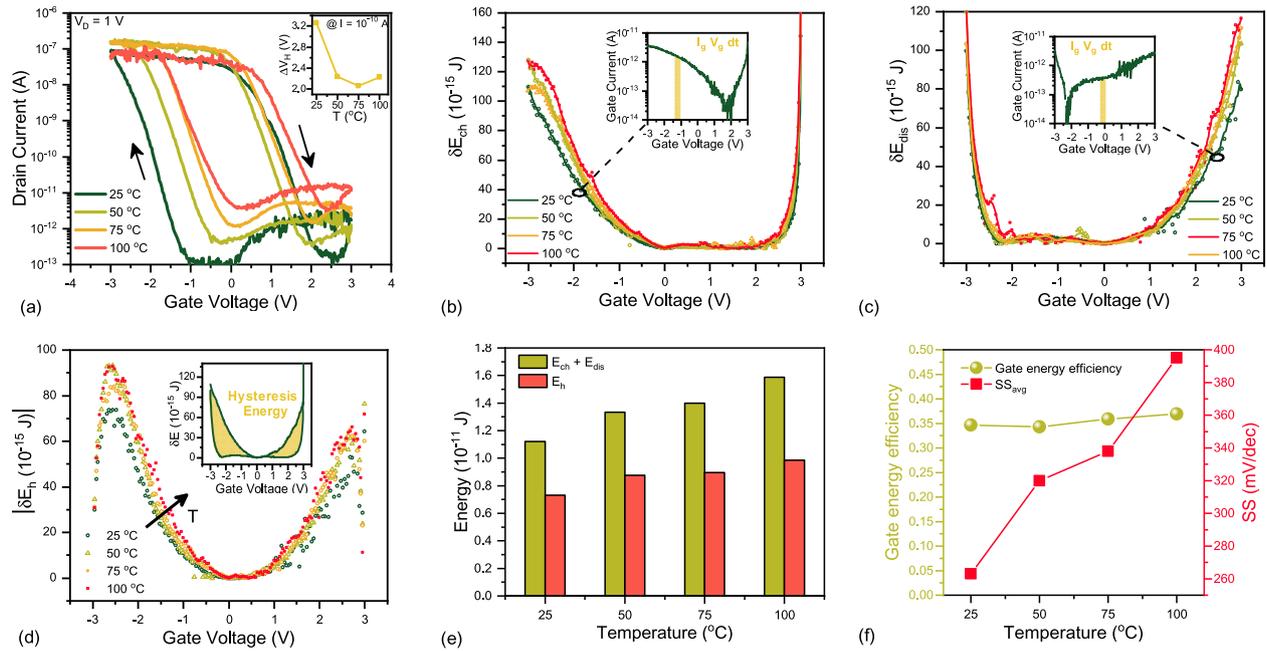


Fig. 4 Electrical and energy behavior characteristics of the 2D/2D FeTFET at high temperatures. **a** Input transfer characteristics of the 2D/2D FeTFET at $V_d = 1$ V for different temperatures. **b, c** Energy behavior of the FeTFET gate stack in forward and reverse sweeps of V_g . **d** Energy loss of the gate capacitors during a dual sweep of the device. **e** The total energy consumed during charging/discharging and the energy dissipated due to hysteresis at elevated temperatures. **f** The gate energy efficiency factor and SS with respect to the investigated temperatures.

on a TAT current contribution. In our device, the experimental average and best point swings are near 188 and 69 mV per decade at 77 K, respectively, while these values reach 263 and 153 mV per decade at 290 K. A higher η is observed at lower temperatures due to the reduction of the hysteresis and hence, the lower dissipated energy. The 2D/2D FeTFET has an efficiency factor of 93% and 55% at 77 K and 290 K, respectively.

Energy charging and discharging at high temperatures

In order to further elaborate on the gate energy behavior, another series of experiments have been conducted on the 2D/2D FeTFET#1 at high temperatures up to 100 °C. Figure 4a shows the transfer characteristics, $I_d - V_g$, from room temperature up to 100 °C, with the corresponding hysteresis values reported in the inset figure. The higher I_{off} corresponds to the temperature dependence of the SRH leakage current, and is responsible for the apparent deterioration of the point and average subthreshold slopes. A relatively smaller hysteresis is observed at elevated temperatures. This can be explained by the increase of the leakage current and temperature dependency of the thermal coefficient and the coercive field of the ferroelectric material. These results demonstrate that the ferroelectricity is well preserved in the Si: HfO₂ stack at elevated temperatures close to the working temperature of modern processors.

To have a more comprehensive understanding of the ferroelectric gate stack behavior as a function of temperature, the charging and discharging energies of the gate capacitor are calculated based on gate leakage current when performing forward and reverse gate voltage sweeps, as shown in Supplementary Fig. 9. We observe a clear butterfly shape in the gate leakage current characteristics for all the investigated temperatures, which is related to the switching behavior of the ferroelectric in the gate stack. The energy of the gate capacitor during charging (δE_{ch}), discharging (δE_{dis}) and the absolute value

of their difference (δE_h) are shown in Fig. 4b–d. For each temperature, the energy plots are calculated according to Eqs. (2) and (3). The total energy during the charging/discharging and the energy of hysteresis at different temperatures are presented in Fig. 4e. It is evidenced that both the hysteresis energy and charging/discharging energy are increased by the temperature increase. This is due to the fact that the impact of the increase of the leakage current is dominant compared to the hysteresis. Gate energy efficiency factor and average subthreshold swing are illustrated in Fig. 4f, at temperatures close to the operational one in microprocessors. In a tunnel FET where the main conduction is based on BTBT, one would expect a little dependence of the subthreshold swing on the temperature. However, in the low current range, the SS of the ferroelectric gate Tunnel FET is relatively deteriorated, as shown in Fig. 4f, essentially due to the influence of the SRH leakage increase at elevated temperatures and also, possibly due to the temperature dependence negative slope of the S-shape polarization characteristics. On the other hand, the gate energy efficiency factor remains almost constant, which suggest that in the range of studied temperature (up to 100 °C), far from the critical T_c of the investigated gate stack, the proposed ferroelectric Tunnel FET transistor will not have significant gate energy efficiency deterioration. This is due to the fact that the gate current and hysteresis, two important factors in gate efficiency, provide opposite trends at elevated temperatures, as explained earlier. Additionally, it should be noted that the relatively small difference in the gate energy efficiency value at 300 K in Figs. 4f and 3f is attributed to the fact that the data in Fig. 4f has been extracted after the cooling of the sample down to 77 K. Therefore, the interface traps between flake and the linear dielectric, the SnSe₂/WSe₂ interface and the source and drain contacts on the flakes are going to be relatively modified. Given the gate energy efficiency factor formula, any changes in the hysteresis can affect the gate energy efficiency value. Moreover, the measurement under vacuum could be another contributing

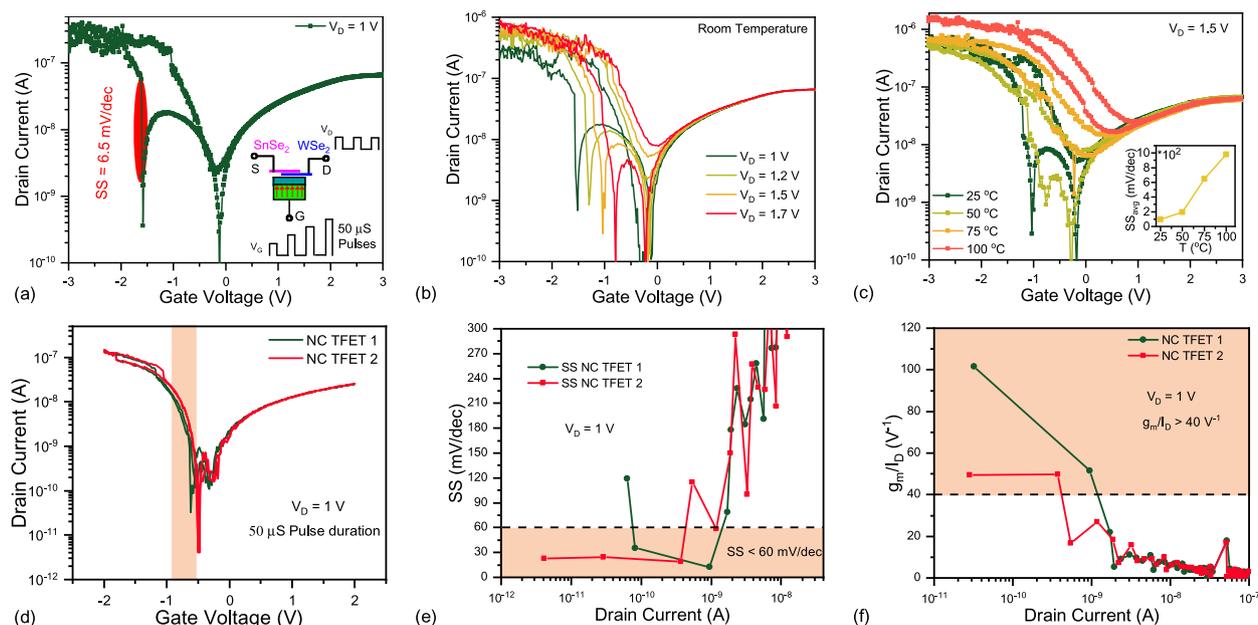


Fig. 5 Pulsed measurements of the hysteric and hysteresis-free NC 2D/2D TFETs. **a** $I_d - V_g$ curve of the NC-TFET, showing a steep SS of 6.5 mV per decade over almost two decades of current. The employed pulsed measurement technique is schematically demonstrated in the inset figure. **b** Transfer characteristic of the NC-TFET at multiple drain voltages, showing a clear degradation of SS by increasing V_d . **c** $I_d - V_g$ plots of the same device in different temperatures ($V_d = 1.5$ V). The SS of the device increases at elevated temperatures. **d** Transfer characteristic of two different non-hysteric NC-TFETs, and **e** the corresponding subthreshold swings. A sub-thermionic SS, down to 15 mV per decade over two decades of current, is reported at room temperature. **f** Transconductance efficiency of both devices, showing a peak of 50 V^{-1} and 100 V^{-1} . The peak transconductance efficiency exceeds the fundamental 40 V^{-1} limit of MOSFET devices.

factor to this relatively small difference. In general, these results show that considerable energy is lost in each cycle when the ferroelectric operates in the hysteric mode. Therefore, a significant improvement in efficiency can be achieved if the ferroelectric performs a true hysteresis-free NC effect.

Pulsed measurement

Pulsed measurement technique have been proposed as a valuable tool for the exploration and demonstration of NC in ferroelectric materials, due to its ability to reduce charge injection assisted switching and ferroelectric's leakage current^{44,56}. Therefore, to demonstrate that in our fabricated devices can reach the NC regime, we have carried out our experiments on the pulsed mode characterization of NC 2D/2D TFET. To experimentally investigate this structure in which the NC effect is combined with a 2D/2D TFET, short pulses were applied to the gate electrode. The device configuration and measurement setup can be found in the Supplementary. Additionally, the impact of the pulse duration/frequency is fully investigated and discussed in the Supplementary. Based on the obtained results, a pulse duration on the order of $90 \mu\text{s}$ is used to extract the transfer characteristics. The reported current in the $I_d - V_g$ plots is an average of readings taken in a predefined measurement window of each pulse. This window is after the rising and before the falling of the applied pulses on the gate.

Hysteric NC 2D/2D TFET

In this section, the electrical performance of a hysteric NC 2D/2D TFET, where the NC of ferroelectric is partially stabilized, is reported. It should be noted that the device used for this experiment is the same as previous section, 2D/2D FeFET#1. Figure 5a illustrates the $I_d - V_g$ plot of the NC-TFET, where the gate voltage is swept from 3 V to -3 V and back to 3 V while the drain

voltage is set at 1 V . The inset shows the schematic of the pulsed measurement technique. The DC characteristics of this device were previously demonstrated in Fig. 4a. An improvement in the subthreshold swing is explicitly observed due to the differential voltage amplification. A measured point SS of 6.5 mV per decade and an average SS of 15 mV per decade over almost two decades of the drain current is achieved at RT. A relatively large hysteresis of 1 V is observed due to the fact that the NC of Si:HfO_2 is stabilized only in a limited range of the gate voltage^{42,57}. The transfer characteristic of the NC 2D/2D TFET is also measured at different drain voltages varied from 1 to 1.7 V , while the pulse duration is constant (Fig. 5b). It is evidenced that the steepness of the subthreshold swing can be affected by the variation of the drain voltage as the operation point of an NC transistor depends also on the drain bias⁴⁰. The impact of the temperature on the performance of our proposed structure is also investigated by measuring and analyzing the $I_d - V_g$ curves at multiple temperatures with a constant voltage of 1.5 V (Fig. 5c). Inset of this figure exhibits how the extracted average of SS is deteriorated when the temperature increases, showing the impact of temperature on the value of ferroelectric NC. Supplementary Fig. 14 reports the $I_d - V_g$ plots at different temperatures when V_d is set at 1.7 V . Although, the ferroelectric capacitor in this structure implies an NC effect, a large hysteresis together with a sharp transition is not appealing for transistor applications. The hysteresis of the NC 2D/2D TFET can be alleviated by modifying the value of the ferroelectric NC, and the effective gate capacitance of TFET to ensure a fully matched design of capacitances in the whole range of operation.

Hysteresis-free NC 2D/2D TFET

Here, other NC 2D/2D TFETs with the same configuration and the NC matching condition close to the ideal are presented. A negligible hysteresis of less than 10 mV is obtained for two TFETs designed on the same chip (Fig. 5d). SEM images and DC

characteristics of the fabricated devices for this experiment, NC TFET#1 and NC TFET#2, are depicted in Supplementary Figs. 15 and 16, respectively. The gate voltage was swept from 2 to -2 V and back to the initial point with the same pulse condition and drain voltage of the previous experiment. It is expected that any changes in the pulse frequency can affect both the SS and hysteresis of the transfer characteristic, as experimentally demonstrated in the Supplementary information. Figure 5e shows the subthreshold swing as a function of the output current for both of the investigated NC TFETs, exhibiting a steep *off-to-on* transition. The minimum point subthreshold slope of 15 mV per decade and an average of 30 mV per decade over 1 order of drain current is reported for the NC TFET#1 at RT. In NC TFET#2, the SS falls below the Boltzman limit for over two decades of current, with an average subthreshold swing of 20 mV per decade at RT. These results confirm that a hysteresis-free NC-TFET, suitable for logic applications, can be realized by properly satisfying the NC matching condition⁵⁷. Although, the gate stack is similar for all the reported devices, the capacitance per unit area is different and defined by the overlap between the drain and source electrode, and the geometry of the flakes. Therefore, different gate capacitances and NC effects are expected. The larger SS and smaller hysteresis in these cases compared to the previous experiment are probably due to the negative capacitance value in the investigated range of the gate voltage. This means that a trade-off is required between the hysteretic behavior and the performance-boosting that is caused by the NC of the ferroelectric⁵⁸. In these devices, the total capacitance of the structure remains positive in a wider range of the V_g which leads to a non-hysteretic transfer characteristic. Further characterization of these NC 2D/2D TFETs revealed an abrupt and dramatic switching behavior of the current efficiency factor, g_m/I_d , as an analog figure of merit of transistors⁵⁹. The extracted values are reported in Fig. 5f which demonstrates peaks of 100 and 50 V^{-1} over one decade of drain current for NC TFET#1 and #2, respectively. These values exceed the 40 V^{-1} analog efficiency limit of MOSFET, highlighting the effect of integrating a ferroelectric layer into the gate stack of a 2D/2D TFET. Supplementary table 1 summarizes the performance of the NC 2D/2D TFET. The lowest point SS, sub-60 mV per decade SS_{avg} over two decades of the drain current, negligible hysteresis, with reasonable ON/OFF current ratio and the possibility of integrating the NC and heterojunction TFET are achieved. A well-designed negative capacitor integrated to the gate stack of a 2D/2D TFET significantly improved the SS and hysteresis. Therefore, an NC 2D/2D platform is a potential configuration for energy-efficient applications.

DISCUSSION

We have reported a comprehensive experimental study of a NC Si: HfO₂ ferroelectric gate stack WSe₂/SnSe₂ TFET focused on the influence of the temperature gate charging and discharging and static characteristics. A gate energy efficiency factor has been defined and used to evaluate the energy efficiency of the gate stack. The energy behavior in ferroelectric gate stack is studied using DC measurement techniques in a wide range of temperatures, from cryogenic temperature, 77 K, to 100 °C, to highlight the importance of exploiting the non-hysteretic NC regime. A pulsed measurement technique has been employed to enable the visualization of NC effect on the device characteristics. In a partially matched NC capacitor, a hysteretic NC effect leads to an SS of 6.5 mV per decade with an average value of 15 mV per decade. In another configuration, near hysteresis-free NC 2D/2D TFETs with point sub-thermionic swing below 15 mV per decade, average swings of 15–20 mV per decade over almost two decades of current and ON/OFF current ratio exceeding 10^4 are demonstrated. An enhanced current efficiency factor up to 100 V^{-1} is reported, presenting a well-designed NC as an analog booster for 2D/2D

TFETs. We explored NC 2D/2D TFET performances from cryogenic temperature up to 100 °C, showing device reproducibility and robustness. The experimentally reported results contribute to the performance engineering of 2D/2D systems for the realization of high performance steep-slope devices. This study provides an insight into the potential of a negative capacitance booster to address the most limiting performances of 2D/2D TFETs. Additionally, the energy behavior of the ferroelectric gate stack under NC condition fulfillment can be effectively applied as a universal method to design more energy efficient switches.

METHODS

Si:HfO₂ deposition

Sixteen nanometer of silicon-doped HfO₂ were deposited by atomic layer deposition (ALD) in a BENEQ TFS200 ALD tool. The starting substrate was a p-doped Si/(100 nm) SiO₂ wafer covered by 50 nm TiN as the bottom electrode. The precursors were tetrakis(ethylmethylamino)hafnium (TEMA-Hf) for Hf and SiH₂(N(C₂H₅)₂)₂ (SAM24) for SiO₂. Water and ozone were used as the oxygen source and the deposition temperature was 300 °C. The Si:HfO₂ film was achieved by alternating ALD cycles of TEMA-Hf and SAM24. The cycle ratio of 16:1:16 (HfO₂:SiO₂:HfO₂) corresponds to a silicon concentration of 3.4% and a thickness of ~13–16 nm was used in this experiment. Top TiN of 10 nm was then deposited by sputtering of TiN target in an Alliance-Concept DP650 physical vapor deposition tool at room temperature. Rapid thermal annealing (RTA) in nitrogen ambient was performed for 2 min at 600 °C to activate the ferroelectricity and complete the metal-ferroelectric-metal (MFM) structure.

TiN wet etching

Top TiN electrode was etched away after the RTA step using the wet etch process. The sample was placed in a solution consists of 10 ml NH₄OH, 20 ml H₂O₂, and 500 ml H₂O solution at 50 °C for 3 min.

Characterization

The measurement of electrical properties in DC mode was acquired with a conventional semiconductor parameter analyzer and electrical probes. In all the reported electrical measurements the WSe₂ is biased as the drain of the device. For pulsed measurements, the pulses were applied to the gate by a Keithley 4200A-SCS with 4225-PMU and simultaneously, the output current is measured. Rise and fall time of the voltage pulses were fixed to 15 μs each. The duration was set to 90 μs for each pulse.

Metrology

SEM analysis of the devices was carried out on a Zeiss Merlin SEM. AFM in contact mode and the off-resonance PFM were performed by using Cypher AFM (Asylum Research) for accurate thickness estimation and switching behavior of Si:HfO₂, respectively. Measurement of polarization versus electric field were performed using an AixACCT TF 2000 tester with an FE module.

DATA AVAILABILITY

The raw data used in this study are available upon reasonable request to the corresponding author.

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AUTHOR CONTRIBUTIONS

S.K. and A.M.I. conceived the main idea of this experimental study on negative capacitance 2D/2D TFET, designed, and developed the process flow. S.K. performed all the fabrication processes, the electrical measurements and data analysis. C.G., A.S.

and M.C. performed AFM and PFM measurements. S.K., C.G. and A.S. carried out the MFM characterization and optimization. S.K. and T.R. prepared the low temperature setup. S.K., A.S. and L.C. prepared the figures and schematics. S.K., A.S. and A.M.I. wrote the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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