A Low-noise CMOS SPAD Pixel with 12.1 ps SPTR and 3 ns Dead Time

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***Abstract*—Single-photon avalanche diodes (SPADs) have become the sensor of choice in many applications whenever high sensitivity, low noise, and sharp timing performance are required, simultaneously. Recently, SPADs designed in CMOS technology, have yielded moderately good performance in these parameters, but never equaling their counterparts fabricated in highly customized, non-standard technologies. The arguments in favor of CMOS-compatible SPADs were miniaturization, cost and scalability. In this paper, we present the first CMOS SPAD with performance comparable or better than that of the best custom SPADs, to date. The SPAD-based design, fully integrated in 180 nm CMOS technology, achieves a peak photon detection probability (PDP) of 55% at 480 nm with a very broad spectrum spanning from near ultraviolet (NUV) to near infrared (NIR) and a normalized dark count rate (DCR) of 0.2 cps/μm^2, both at 6 V of excess bias. Thanks to a dedicated CMOS pixel circuit front-end, an afterpulsing probability of about 0.1% at a dead time of $\sim$3 ns were achieved. We designed three SPADs with a diameter of 25, 50, and 100 μm to study the impact of size on the timing jitter and to create a scaling law for SPADs. For these SPADs, a single-photon time resolution (SPTR) of 12.1 ps, 16 ps, and 27 ps (FWHM) was achieved at 6 V of excess bias, respectively. The SPADs operate in a wide range of temperatures, from -65°C to 40°C, reaching a normalized DCR of 1.6 mcps/μm^2 at 6 V of excess bias for the 25 μm at -65°C. The proposed SPADs are ideal for a wide range of applications, including (quantum) LiDAR, super-resolution microscopy, quantum random number generators, quantum key distribution, fluorescence lifetime imaging, time-resolved Raman spectroscopy, to name a few. All these applications can take advantage of the vastly improved performance of our detectors, while enjoying the opportunities of megapixel resolutions promised by the economy of scale that is offered by CMOS technologies.**

***Index Terms*—Active reset, cascode, jitter, low noise, low power, photon detection probability (PDP), pixel, quantum key distribution (QKD), single-photon avalanche diode (SPAD), timing.**

I. Introduction

SILICON-BASED Single-photon avalanche diodes (SPADs) attracted increasing interest in the last decades thanks to their interesting performance [1], [2]. These devices showed relatively low noise, high photon detection probability (PDP), and very good timing performance [3]–[5]. Initially, SPADs were fabricated in custom epitaxial technology [6]. The use of a custom technology guarantees freedom in design optimization, in order to obtain the best performance in terms of sensitivity and noise [7], [8]. Recently, important efforts have been devoted to implement SPADs in commercial CMOS platforms [9]–[25]. Although CMOS SPADs are generally less performing in terms of PDP and noise, the benefit of integrating them side-by-side with electronic circuits is quite obvious. Indeed, this approach leads to reduced parasitics and more sophisticated ancillary circuits, larger application spectrum through more extensive functionality, and cost reduction thanks to mass production. Moreover, the circuits used for the SPAD front-end interface have been substantially improved over time, allowing the implementation of much more complex systems that fit a wider spectrum of applications [26]–[30]. In this context, very large array sizes, up to 1Mpixel have been achieved [31], [32].

In this work, we present three SPAD pixel detectors, based on high-performance SPAD pixels implemented in 180 nm CMOS technology. This device is specifically designed to achieve high performance in terms of count rate, sensitivity, timing precision, noise, and power consumption. The latter is very important if the same architecture is implemented in large arrays. The paper is organized as follows. After a description of the SPAD structure and corresponding TCAD simulations, along with the electronic front-end in Section II, the device characterization is presented, covering noise performance (Section III), sensitivity (Section IV), and timing (Section V). The setup for each of the parameters is added to the results. Section VI presents a discussion of the results followed by perspectives opened up by this work. Section VII closes the paper.

II. SPAD Design

We designed three devices in separate dies. Each device comprises four independent SPADs with a dedicated pixel circuit, placed at a distance of 250 μm. Fig. 1 shows the micrograph of the three implementations, whereas the inset on the *top-right* of each micrograph, shows three different SPAD diameters (25 μm, 50 μm and 100 μm, respectively). To achieve the maximum of controllability and observability of the system, each chip has a large padring. Several pads were added in this prototyping phase to ensure the possibility of fine tuning the several control voltages of the pixel circuit,

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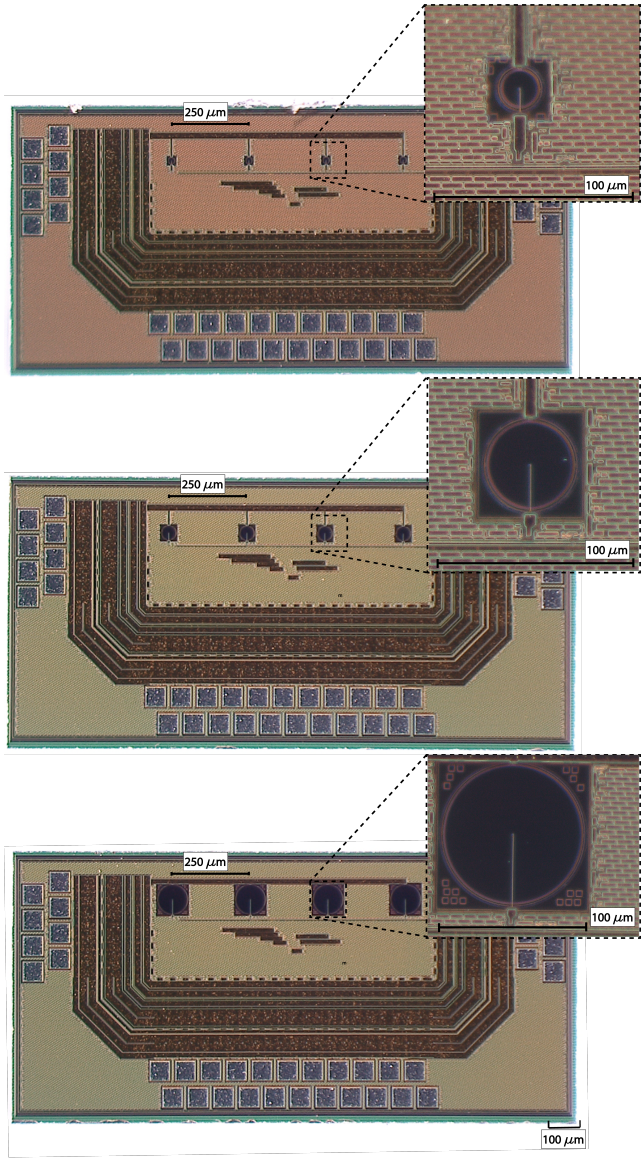

Fig. 1. Micrograph of the implemented *chip 1* (*top*), *chip 2* (*middle*), and *chip 3* (*bottom*) with a zoom-in on the SPAD pixel (*top-right* of each image). These devices embed four SPADs of 25 μm, 50 μm, and 100 μm for chip 1, 2, and 3 respectively. Each SPAD has a dedicated pixel and a pixel pitch of 250 μm.

together with the high voltage to bias the SPAD, digital VDD, ground, and ESD supplies. The SPADs, implemented in 180 nm CMOS technology, rely on a p-i-n structure, similar to [21]. Fig. 2 shows the cross-section of the SPAD (*top*) and a TCAD simulation of the electric field in 2D, as well as a quantitative plot of the field along the vertical axis. The SPAD is a substrate-isolated type, where a p-well (PW) layer forms the anode of the SPAD and a buried n-well (BNW) layer creates the cathode contact. The latter is connected to the high voltage through a deep-n-well (DNW). An epi layer between anode and cathode allows a fairly large high-field region (Fig. 2, *bottom*), thus achieving a large sensitivity spectrum. The simulation results correspond to the SPAD operation at an excess bias voltage of 6 V.

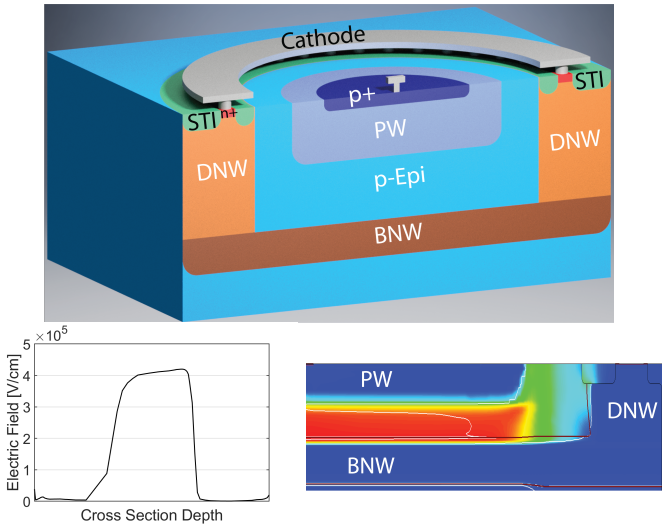

Fig. 2. SPAD cross-section (*top*) and TCAD simulation of the electric field (*bottom*). A quantification of the electric field along the vertical axis is also shown (*left-side*).

The SPAD breakdown voltage was measured to be about 22 V at room temperature. The corresponding I-V curve is shown in Fig. 3 under both dark and illuminated conditions.

The SPAD front-end circuit, shown in Fig. 4, was inspired by [33], whereas cascode transistor M_1 is used as a resistive divider, along with M_2 to enable high excess bias (up to 11 V) [34] in combination with thin-oxide MOS transistors in the remainder of the front-end.

The gate of M_1 is fixed at V_{CAS}, supplied externally. When an avalanche is triggered in the SPAD, the voltage at the source of M_1 rises, thus decreasing the transistor overdrive. When the voltage reaches $V_{CAS} - V_{th}$, M_1 turns off boosting the impedance seen at the SPAD's anode. Thanks to the *body effect* acting on these transistors, the overdrive of M_1 is dynamically reduced, thus making it turn off faster.

Both passive and active recharge strategies are available in the

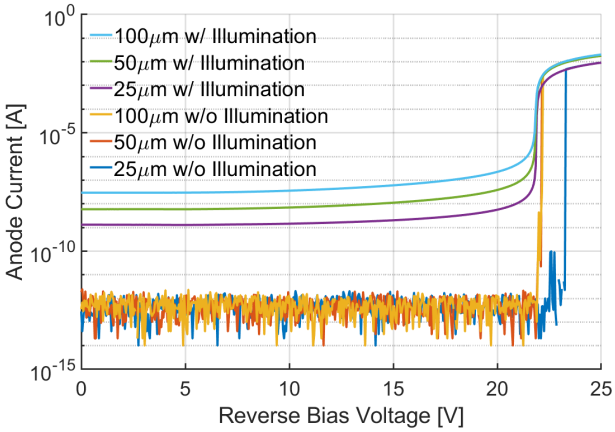

Fig. 3. IV curve measured on isolated SPAD samples with the same cross section and size. The measurements were performed both with and without illumination. The breakdown voltage is about 22 V. As it possible to see in the measurements without illumination the breakdown results overestimated. This is an indication of the low noise of the device.

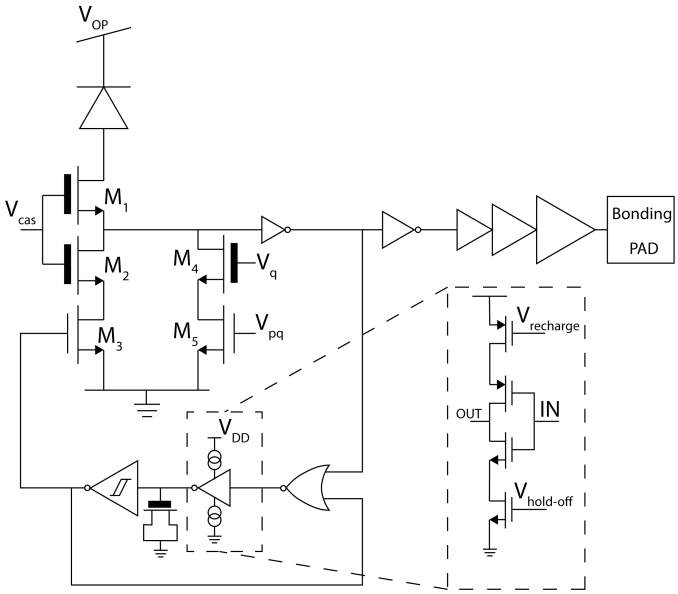

Fig. 4. Simplified schematic of the SPAD pixel. A cascode structure is used to allow high excess bias voltage (up to 11 V). An active reset feedback guarantees the fine control of the SPAD deadtime. A buffering chain is implemented to output the signal on an analog pad.

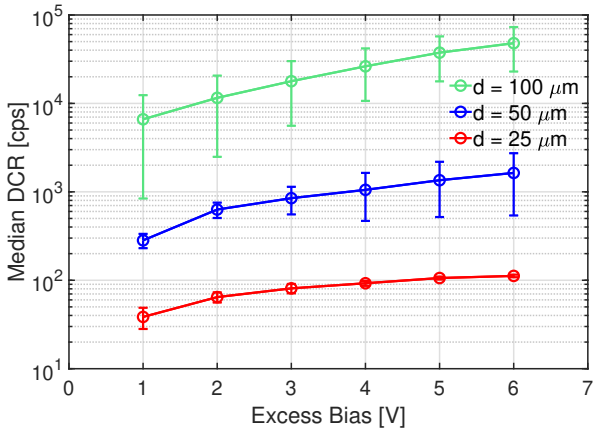

Fig. 5. DCR median value measured at several excess bias voltages for the different SPAD sizes. The results are obtained measuring 15 devices for each size.

pixel and can be used independently. M_5, controlled by V_{pq}, is used to disable the passive quenching/recharge branch, represented by M_4. Active recharge is formed by M_2 and M_3, the latter being turned on by the feedback loop represented by the OR gate, Schmitt trigger, and tunable delay element. The loop acts as a programmable-length monostable. The delay element is implemented using a current starved inverter (CSI) with a series voltage controlled transistor for both pMOS and nMOS branches (Fig. 4 *right*). Controlling this delay, and thus the hold-off time is important to control afterpulsing, especially in relatively large SPADs. This mechanism determines both the pulse width at the output and, in large part, the dead time. To guarantee the stability of the monostable and to get sharp edges at the output, an inverting Schmitt trigger was added, while, to improve the linearity of the CSI controls, a current mirror was included [35]. The slew rate of the output was maximized, unlike in [34], using a custom buffering chain to the bonding pad. This solution ensured an output slew rate of approximately 1 V/ns.

III. Noise Performance

A. Dark Count Rate

Dark count rate (DCR) was measured at different excess bias voltages for all three SPAD structures (Fig. 5). The measurement was performed at room temperature using an oscilloscope (Teledyne LeCroy WaveMaster 813 Zi-B). To a first approximation, DCR is linear in the area of the active region. However, a super-linear behavior is generally observed in the normalized median DCR due to the increased probability of traps in larger SPADs, thus causing trap-assisted dark counts. The results are shown in Fig. 5, where the median DCR is 0.2 cps/μm^2 at 6 V excess bias and room temperature for the 25 μm diameter SPAD. The DCR of the devices was also measured as a function of temperature in the -65°C to 40°C range using a climate chamber operated in a closed loop. Fig. 6 shows DCR in cps as a function of temperature for a range of excess bias voltages for the smaller (25 μm) and the larger (100 μm) SPADs. The figure also shows the breakdown voltage behavior over temperature for the same devices. These values were used to apply a precise excess bias. By decreasing the temperature, DCR decreases by about three orders of magnitude, reaching a value of 1.6 mcps/μm^2 at 6 V_{ex} for a diameter of 25 μm, operating at -65°C. The normalized DCR on the active area reaches a value of 4 mcps/μm^2 at 8 V_{ex} at -65°C.

B. Afterpulsing

Afterpulsing probability is another very important parameter, especially when one wants to minimize dead time through active recharge, so as to increase the maximum count rate in SPADs. This effect is due to some carriers, generated during the avalanche process, that may be captured by deep-level traps [36]–[38]. These carriers are then released after a statistical delay that depends on the lifetime of the traps [37], [38]. If a free carrier is released in a region where the electric field is sufficiently high it can ignite another avalanche. In general, the probability that this event occurs is more frequent with short dead times. Afterpulsing characterization for silicon SPADs is performed by histogramming the pulse inter-arrival time. This can be measured in the dark or under dim and uniform illumination. It can also be indirectly obtained by estimating the lifetime and density of traps using the time-correlated carriers counting (TCCC) technique [38], [39], which is typically more useful for III-V SPADs where the afterpulsing probability is significantly higher. In the presented work, the afterpulsing probability was obtained through inter-arrival histogramming under controlled dim illumination. Fig. 7 shows the measured inter-arrival time between pulses generated by the 25-μm SPAD at 6 V_{ex}. The SPAD dead time was set at about 11 ns using the integrated active recharge circuit described earlier.

In Fig. 8 it is possible to see the measured afterpulsing

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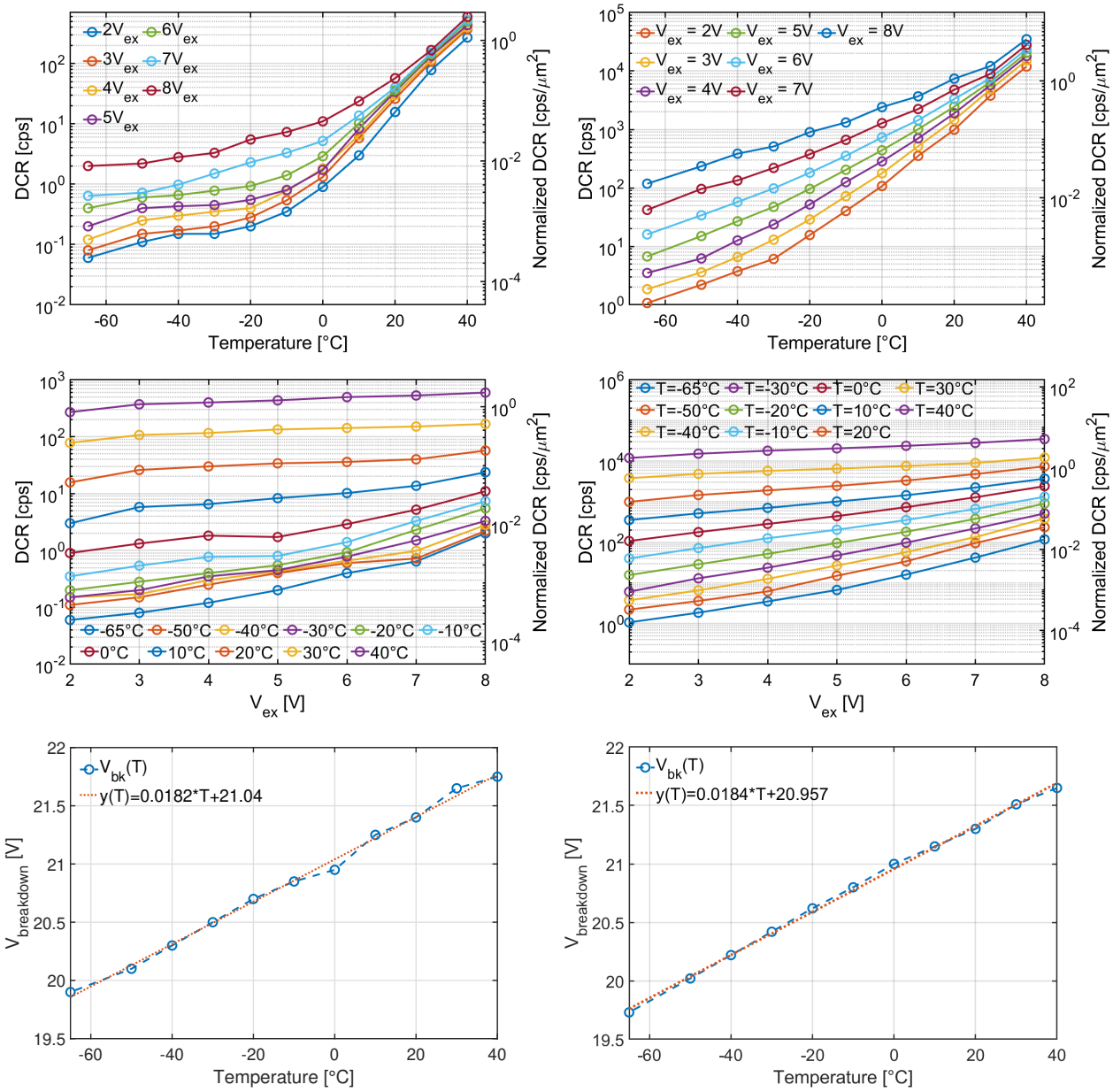

Fig. 6. *Top*: DCR measured at different temperatures; *Middle*: DCR shown as a function of the excess bias voltage; *Bottom*: Breakdown voltage as a function of temperature. The results refer to a SPAD diameter of 25 μm (*left side*) and 100 μm (*right side*), respectively.

probability on the same SPAD, as a function of the pulse width. The afterpulsing probability remains as low as 0.1% for a pulse width of about 5 ns. With the current architecture, the minimum achievable SPAD dead time is 3 ns.

IV. Sensitivity Performance

A. PDP Setup

The most common method of measuring the PDP is to create an area with uniform photon flux of a particular wavelength and compare the responsivity of the SPAD under test to a calibrated reference device (usually a photodiode). The setup used to measure PDP is based on the continuous light technique [40], schematically shown in Fig. 9. The setup comprises a wide-spectrum Xenon lamp that generates wide spectrum light, a monochromator, an integrating sphere, a calibrated reference photodiode (PD) with a precision source and measurement unit (SMU) to measure the photocurrent generated by the PD, and a universal counter connected to the device under test (DUT). The integrating sphere and the DUT are enclosed in a light tight box to eliminate any source of background noise that would affect the measurement. A custom software was developed to automate the scan at a very fine wavelength resolution. The DUT has been placed at distance L from the output window of the integrating sphere, so as to ensure lower light level and high uniformity [41]. The reason to have a lower light level is that the SPAD (sensible to single photons) can be saturated if exposed to high light level, thus causing pile-up, which distorts the SPAD's sensitivity curve,

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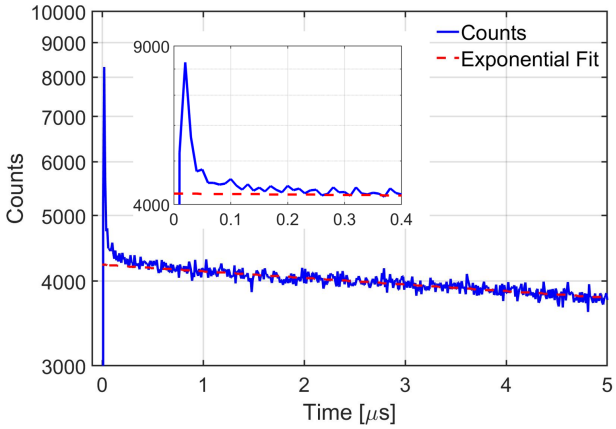

Fig. 7. Inter arrival time distribution measured with the pulse width of 11 ns on the SPAD of 25 μm size. The measurement is taken at a temperature of 25°C.

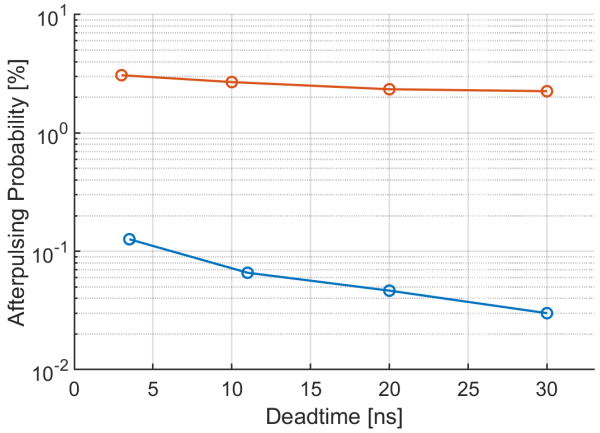

Fig. 8. Afterpulsing probability as a function of the pulse width on the 25 μm diameter and 100 μm diameter SPADs at 6 V excess bias. All the measurements are taken at a temperature of 25°C.

causing an underestimation of PDP. Moreover, a stronger light impinging on the reference photodiode can improve its SNR. A 45 s integration time was used for each step. For each value of excess bias, the DCR is measured before starting the acquisition under the light. This value is then used to compute the PDP as shown in [40]:

$$PDP(\lambda) = \eta \frac{S - DCR}{A_{SPAD} F_{PD}(\lambda)} = \eta \frac{F_{SPAD}(\lambda)}{F_{PD}(\lambda)} \quad (1)$$

Where η is a light ratio computed during the calibration phase measuring the light power at the integrating sphere output port and at the location of the DUT with a calibrated reference photodiode; S is the number of pulses at the SPAD output when exposed to light; A_{SPAD} is the active area of the SPAD; $F_{PD}(\lambda)$ is the photon flux detected by the reference photodiode.

B. PDP Results

The PDP is plotted in Fig. 10 as a function of wavelength (*top*) and excess bias voltage (*bottom*). All the measurements

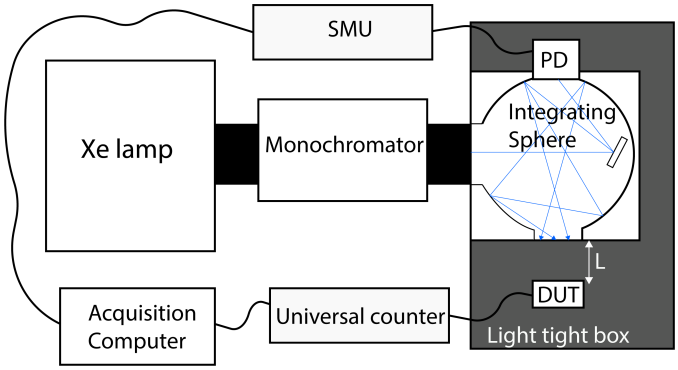

Fig. 9. PDP setup used for device characterization. A Xenon lamp generates a wide spectrum photon flux. Narrow band of wavelengths are selected with the monochromator and the integrating sphere diffuses the photons equally to the DUT and the reference PD, while the PD (Hamamatsu S2281) and the DUT are placed at a calibrated distance *L*. The setup is enclosed in a light tight box and an universal counter (Keysight 53230A) is used to evaluate the SPAD output.

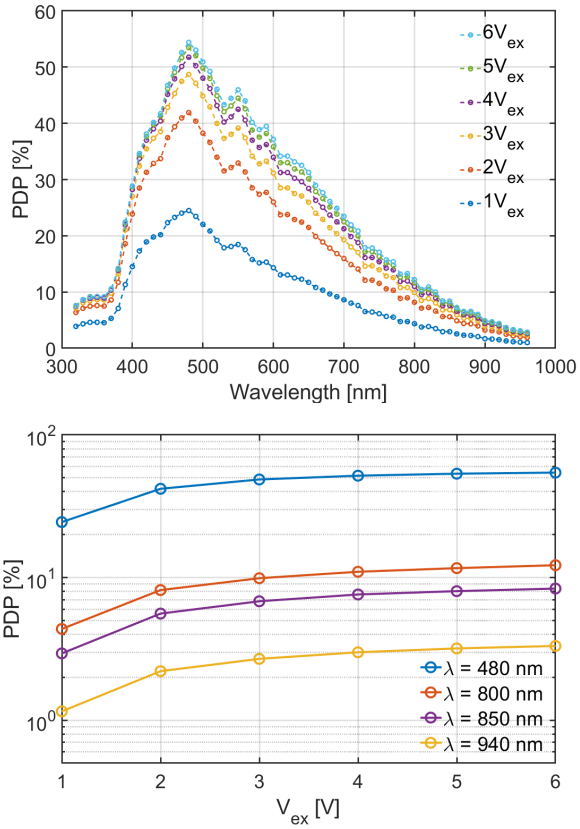

Fig. 10. *Top*: PDP measurements for several excess bias voltages (from 1 V to 6 V excess bias). The measurement is performed with a wavelength step of 10 nm in a wavelength range between 320 nm and 960 nm. *Bottom*: saturation effect of PDP over bias voltage for four selected wavelengths.

were performed at room temperature. The wavelength scan was performed with a step of 10 nm. The sensitivity peak is 55% at 480 nm at 6 V_{ex}. These results are consistent with [21], [34] for similar SPAD cross-sections. The relatively large sensitivity spectrum is also in line with the structure used (Fig. 2). Note the typical PDP saturation above 5 V_{ex}. At and above this voltage, the PDP becomes increasingly

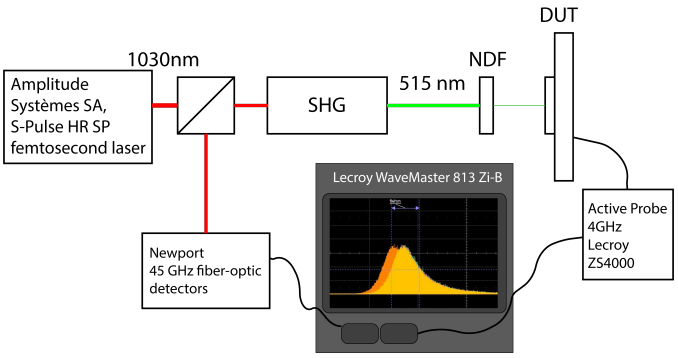

Fig. 11. Optical setup used for the single-photon timing resolution measurement. A femtosecond laser generates a 150 fs pulse at 1030 nm, which is then upconverted to 515 nm after SHG. A fast PD is used as a reference to the oscilloscope, while the upconverted beam (515 nm) is filtered by neutral density filters (NDFs). The output of the DUT is sampled through a 4 GHz, 0.6 pF active probe by a 40 GS/s, 13 GHz oscilloscope to generate a histogram using time-correlated single-photon counting (TCSPC) acquisition.

insensitive to variations of breakdown voltage, which makes this SPAD amenable to integration in large arrays, where the breakdown voltage could vary significantly across the chip, thereby causing unwanted PDP variability.

V. Timing Jitter

A. Jitter Setup

The setup used to evaluate timing jitter in the DUT shown in Fig. 11 is based on [42]. The setup comprises a femtosecond laser (Amplitude Systèmes SA, S-Pulse HR SP), capable of generating 150 fs pulses at a wavelength of 1030 nm and 515 nm after second-harmonic generation (SHG). A fast photodiode (Newport InGaAs Photodetector, 45 GHz bandwidth) is used as a timing reference, while the upconverted beam is attenuated by a bank of neutral density filters (NDFs), so as to achieve single-photon detection regime. The DUT has a high-impedance output and thus an active probe is used to capture the output. An oscilloscope (LeCroy WaveMaster 813 Zi-B) is used to capture both the waveform from the DUT and the reference PD.

B. Jitter Results

Timing jitter measurements for the 3 device sizes are shown in Fig. 12. The plot shows the histograms of the response of the SPADs when biased at an excess bias voltage of 6 V and at room temperature. The oscilloscope trigger threshold was set at 400 mV for the SPAD pulse and 300 mV for the PD. The laser repetition rate is 100 MHz and the light was reduced in order to detect less than a laser pulse every 100. The jitter value (FWHM) of the response distribution was measured at 12.1 ps for a diameter of 25 μm, 16 ps for 50 μm, and 27.2 ps for 100 μm. To capture the diffusion tails, the full width at tenth of maximum (FWTM) was extracted as well; it results in 55.7 ps for a diameter of 25 μm, 66.8 ps for 50 μm, and 91.7 ps for 100 μm. The exponential time constant for the diffusion tails was also extracted from the plot to be 31.5 ps, 40.7 ps and 36 ps for the 25 μm, 50 μm and 100 μm SPAD, respectively. The plots in Fig. 13 show the response of a 100

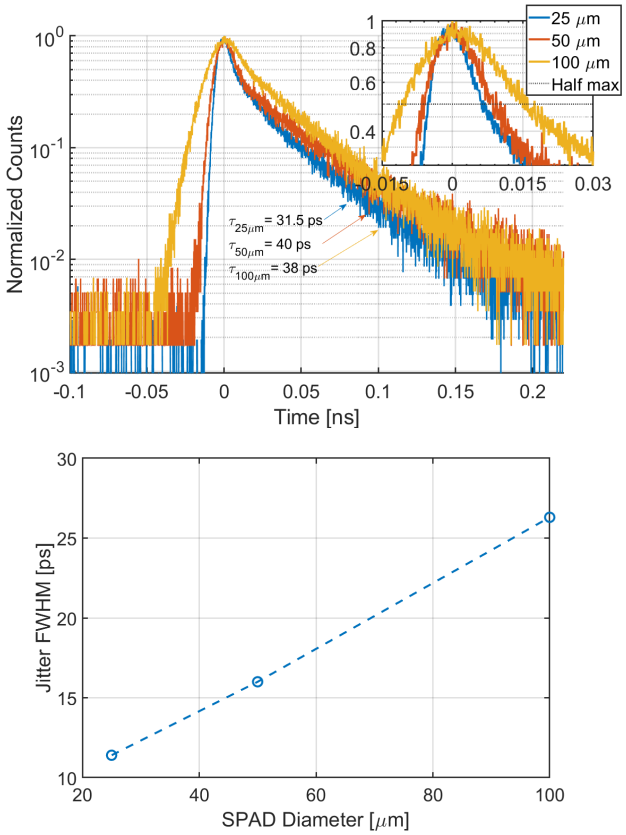

Fig. 12. Jitter measurements performed with a 515 nm femtosecond pulsed laser. Histogram results (*top*) and extracted jitter value as a function of the area (*bottom*) are visible in the graphs. The jitter results to be around 12.1 ps, 16 ps and 27.2 ps FWHM for the 25 μm, 50 μm, 100 μm diameter SPADs, respectively. The measurement is performed at V_{ex} = 6V excess bias for the three samples.

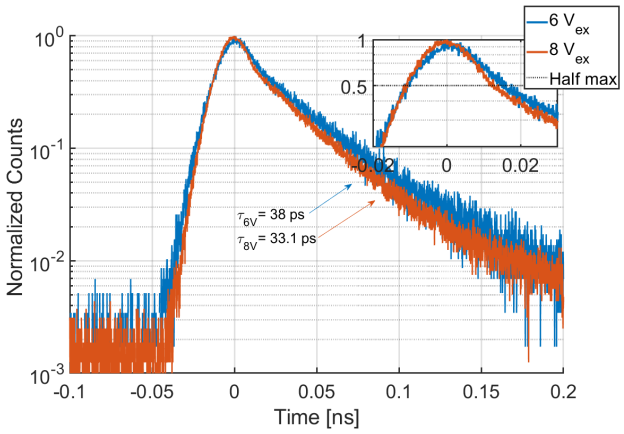

Fig. 13. Jitter measurements comparison at two excess bias voltages (6 V and 8 V) performed on the 100 μm diameter SPAD. The jitter results to be 27.2 ps and 23.5 ps FWHM, respectively.

μm SPAD with two excess bias voltages of 6 and 8 V, with an improvement of the jitter from 27.2 to 23.5 ps FWHM. Also in this case the exponential time constant of the diffusion tail was extracted and it is 38 ps for 6 V excess bias and 33.1 ps for 8 V excess bias. It is important to note that these results were obtained without the need for low threshold comparators, thus a simplified circuit can be used in each pixel, thereby ensuring

scalability to large arrays of pixels.

VI. Discussion

Table I and Fig. 14 summarize the performance of several state-of-the-art devices found in the literature in comparison to the SPADs presented in this work. Many of the SPADs listed here were developed in standard technologies. SPADs implemented in older technology nodes (between 0.35 μm and 0.16 μm) exhibit the best sensitivity performance [16]–[19], [21], [24]. Instead, in more recent nodes, where higher doping and shallower standard layers are used, peak PDP does not usually exceed 32% and noise is higher [10]–[13], [15], [20], [22]. In [43] it is shown how very high PDPs can be achieved in the red in a 180 nm CMOS node using custom layers. However, this SPAD is not isolated, and thus the integration of front-end circuits is not straightforward. In addition, the achieved timing jitter is high because of its large drift region. The PDP performance of the devices presented in this work is among the best ever reported in the literature for substrate isolated SPADs. The peak value of $\sim$54% at 480 nm with 5 V excess bias is quite close to that reported in [24], device (C), for the same bias. The noise performance reported in this work is also among the best shown in the literature (Fig. 14 *right*).

To the best of our knowledge, the timing jitter achieved in this work is superior to any other CMOS SPAD-based device reported in literature, except for [5], which reports a peak PDP of 8% and a DCR of 2800 cps/μm^2, while our device achieves a peak PDP of 55% and worst-case DCR of 0.23 cps/μm^2 (Fig. 14 *left*). Moreover, in our solution, we have shown the performance of the SPAD with a low-power digital front-end and without the need for any circuit that could affect power consumption, such as a low threshold comparators. Thus, we believe that the proposed SPAD is an example of a new generation of devices with similar or better performance than custom SPADs but allowing scalable architectures with little to no power budget restrictions. Finally, we believe that the reduction of the front-end circuit threshold could improve timing performance and power consumption even further.

VII. Conclusions

We report on the design and characterization of a new SPAD fabricated in 180 nm CMOS technology, exhibiting a performance comparable or better than that of the most advanced custom SPADs, to date. The devices have a peak PDP of 55% at 480 nm and DCR is as low as 0.2 cps/μm^2 at room temperature, both at 6 V excess bias. The DCR is as low as 1.6 mcps/μm^2 at -65°C, while the SPAD operated normally at 40°C. The pixel circuit used allows the fine tuning of the SPAD dead time to control the maximum achievable count rate up to 300 Mcps, while afterpulsing remains in the order of 0.1%.

Three SPAD families were designed with 25, 50, and 100 μm. The SPTR reached 12.1 ps (FWHM) in the smallest SPAD and did not exceed 27 ps in the largest, all at 6 V of excess bias and room temperature. Low static power consumption is compatible with large arrays of SPADs, which makes this technology amenable to scalable Mpixel sensor architectures, suitable for a variety of applications demanding high sensitivity, low noise, and sharp timing performance.

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TABLE I
SUMMARY OF SPAD PERFORMANCE

Comparative Table									
	Technology (nm)	Diameter μm	V_{EX}/V_{BD} (V)	Peak PDP (%) @λ (nm)	PDP (%) @850 nm	DCR/unit area ($cps/\mu m^2$)	AP (%)	Jitter (ps)	FoM$_T$ [44]
Ghioni [7]	Custom Thin	50-200	5-10/30-35	52-68 @550	12-15	0.4-1.6[a]	2[b]	35[c]	1.88E+11
Gulinatti [8]	Custom RE	50	20/45-55	58 @650	28	0.3[d]	N/A	93[c]	N/A
Villa [16]	350	10-500	2-6/25	37-53 @450	2-4.5	0.05[a]	1[e]	90[f]	6.52E+11
Leitner [17]	180	10	1-3.3/21	35-47 @450	N/A[g]	0.3-1.8[a]	N/A	N/A	N/A
Veerappan [18]	180	12	2-10/23.5	24-48 @480	3-8	0.16-176[a]	0.03-0.3[h]	112-88[i]	1.37E+9
Veerappan [19]	180	12	1-4/14	23-47 @480	4-7	0.28-16[d]	0.2[j]	161-141[i]	2.78E+9
Veerappan [21]	180	12	1-12/25	18-47 @520	2-8	0.2-6[d]	7.2[k]	139-101[i]	5.88E+9
Xu [22]	150	10	2-5/19	24-32 @450	2-3.5	0.1-1	1-13[l]	42[m]	1.33E+11
Lee [20]	140(SOI)	12	0.5-3/11	12-25 @500	2.5-7	0.9-260	1.7[n]	65[o]	1.17E+9
Richardson [13]	130	8	0.6-1.4/14	18-28 @500	3-5	0.24-0.6[a]	0.02[p]	200[q]	9.04E+9
Richardson [12]	130	8	0.2-1.2/12-18	18-33 @450	2-5	0.4-0.8	0.02[r]	237-184[s]	4.01E+10
Niclass [10]	130	10	1-3.5/10	31-41 @450	3	120-1300[d]	N/A	144[i]	N/A
Niclass [43]	180	25	5/20.5	64.8 @610[ii]	24	0.6	0.49[dd]	190	1.83E+11
Gersbach [11]	130	4.3	1-2/9	18-30 @480	3.5-5	1.5-11.5	<1[t]	125[i]	3.89E+9
Charbon [15]	65	8	0.05-0.4/9	2-5.5 @420	0.2-0.4	340-15.6k[a]	<1[u]	235[i]	3.71E+5
Sanzaro(A) [24]	160(BCD)	10-80	3-9/36	31-58 @450	2.5-6.5	0.12-0.2[v]	0.43-1.59[w]	39-28[c]	9.12E+11
Sanzaro(B) [24]	160(BCD)	10-80	3-9/25	2-47 @450	2.5-6.5	0.1-0.18[v]	0.02-0.14[w]	36-28[c]	7.9E+11
Sanzaro(C) [24]	160(BCD)	10-80	3-9/26	55-71 @490	6-9	0.13-0.19[v]	0.41-1.26[w]	41-28[c]	1.15E+12
Pellegrini [25]	40	18.36	1/15.5	45 @460[+]	5	N/A[†]	0.1	170[*]	N/A
Nolet [5]	65	20	1.75/9.9	8 @470	N/A	2.8k	<10	7.8[♯]	N/A
Webster [14]	90	6.4	14.9/2.4	44 @700	22	8.1k	0.375	84	N/A
This Work	**180**	**25-100**	**1-11/22**	**25-55@480**[2]	**3-8.4**[x]	**0.06-0.23**[y]	**~0.12-3**[z]	**12.1**[1]	**2.78E+13**

[a] At 20°C. [b] 200μm-diameter, at 25°C, 80 ns dead time,V$_{EX}$=5V. [c] 820 nm wavelength. [d] At 25°C. [dd] 24 ns dead time. [e] 30 μm-diameter, at 25°C, 40 ns dead time,V$_{EX}$=5 V, integrated AQC. [f] A time resolution of 28-37 ps FWHM and a diffusion tail of 160-340 ps were demonstrated in Ref. [45] using the substrate bias as a trade-off parameter between jitter and diffusion tail. [g] PDE=10-13% at 800 nm. [h] 300 ns dead time, V$_{EX}$=2-10 V. [i] 637 nm wavelength. [ii] Substrate not isolated SPAD. [j] 300 ns dead time, V$_{EX}$=4V. [k] 300 ns dead time, V$_{EX}$=11 V. [l] 50 ns dead time, V$_{EX}$=1.5-5 V. [m] 831 nm wavelength. [n] 200 ns dead time, V$_{EX}$=2V. [o] 405 nm wavelength. [p] 200 ns dead time,V$_{EX}$=2V. [q] 815 nm wavelength. [r] 50 ns dead time. [s] 470 nmwavelength. [t] 180 ns dead time. [u] 5μs dead time. [v] At 300 K. [w] 30μm-diameter, at 300 K, 50 ns dead time. [x] Measured between 1V and 6V excess bias at 25°C. [y] 25μm-diameter at 20°C measured at 1 V and 6 V excess bias. [z] For a dead time of 3 ns on the 25 μm-diameter and 100 μm-diameter SPADs at 25°C and 6 V excess bias. [*] 1 V excess bias, room temperature and 850nm laser. [+] Using microlenses. [†] About 100 cps at room temperature at 1V excess bias. [♯] 410 nm laser. [1] 25μm-diameter at 20°C with an excess bias of 6V. [2] value taken at 1 V and 6 V excess bias.

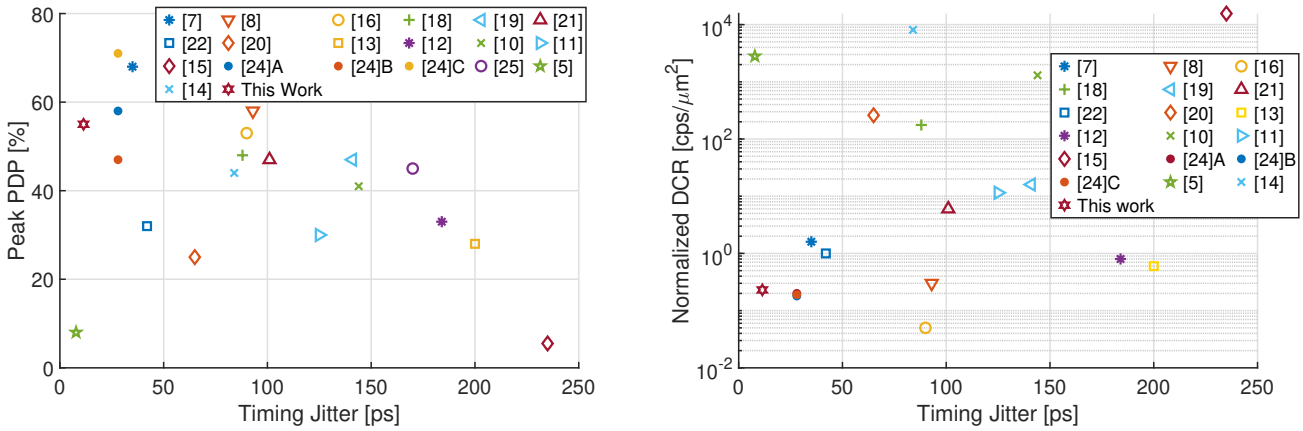

Fig. 14. *Left*: visualization of state-of-the-art performance in terms of PDP and timing jitter. The best solutions are located toward the top-left corner of the graph. *Right*: Performance comparison in terms of normalized DCR and timing jitter. The best performance is found at the bottom-left corner of the graph.

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