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High-Performance Enhancement-Mode AlGaN/GaN Multi-Channel Power Transistors

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***Abstract*—AlGaN/GaN devices have shown outstanding potential for power conversion applications. However, despite the recent progress, their performance is still far from what the material can offer in terms of on-resistance and breakdown voltage. To address this challenge, here we demonstrate a multi-channel tri-gate High-Electron-Mobility Transistor (HEMT) based on an AlGaN/GaN multiple channel heterostructure and a nanostructured gate region. The multi-channel heterostructure leads to a significantly reduced sheet resistance while the nanostructured gate provides excellent control over all the embedded channels and enables to effectively manage the large off-state electric fields. This approach results in e-mode devices with a threshold voltage (V_{TH}) of 0.85 V at 1 µA/mm, very low specific on-resistance of 0.46 mOhm·cm², and a large breakdown voltage of 1300 V. In addition, we demonstrate multi-channel devices with excellent V_{TH} stability and reduced current collapse thanks to a novel conformal passivation technique, which shows the potential of the multi-channel tri-gate technology for future power conversion applications.**

Keywords—GaN HEMTs, AlGaN/GaN, Multi-Channel, Tri-Gate, Surface Passivation, Current Collapse

I. INTRODUCTION

AlGaN/GaN devices have shown great potential for efficient power conversion applications thanks to the excellent GaN material properties. However, despite the recent progress, their performance is still far from the theoretical limits of the material [1]. An effective way to enhance device performance consists of increasing its carrier concentration (N_s), which directly results in a smaller on-resistance (R_{ON}). Yet, increasing N_s leads to major challenges for the heterostructure and device design. On the one hand, a larger N_s severely impacts the carrier mobility (µ), limiting the reduction of the heterostructure sheet resistance (R_{sh}). On the other hand, a large carrier concentration results in a difficult control of the channel, which hinders enhancement-mode (e-mode) operation and degrades the device voltage blocking performance.

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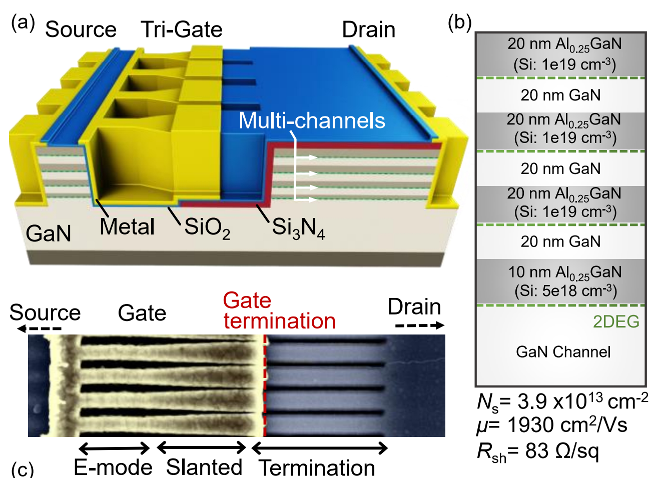

Fig.1. (a) Three dimensional schematics of the multi-channel tri-gate MOSHEMT. (b) Schematics of the multi-channel heterostructure. A 1 nm-thick AlN spacer (not shown) is present between the AlGaN barrier and the GaN channel. (c) Top SEM view of the nanostructured gate region.

A promising approach to address this trade-off is with the use of multi-channel heterostructures [2]–[7], in which several barrier/channel layers are stacked to achieve multiple 2DEGs, which allow to increase the N_s and thus the heterostructure conductivity. While these structures have been proposed for RF applications [8]–[10], their use for power devices depends on very different requirements, which need to be separately addressed. In particular, enhancement-mode (e-mode) operation, large blocking voltage capabilities with reduced leakage current, and good stability during switching operation are fundamental features for power devices, which require careful solutions on a multi-channel platform.

In this work, we address these challenges by demonstrating a high-performance e-mode multi-channel tri-gate High-Electron-Mobility Transistor (HEMT) based on a multiple channel heterostructure and a nanostructured gate region (Fig. 1). The multi-channel heterostructure allows distributing a large N_s in multiple channels, thus maintaining a very high µ and leading to a much-reduced R_{sh}. The nanostructured gate [2], [4] provides excellent control over all the embedded channels and enables to effectively manage the large off-state electric field, leading to e-mode devices with very low on-resistance combined with excellent breakdown voltage. In addition, we demonstrate multi-channel devices with excellent threshold voltage (V_{TH}) stability and reduced current collapse thanks to a conformal surface passivation technique, showing the potential of this technology for future power conversion applications.

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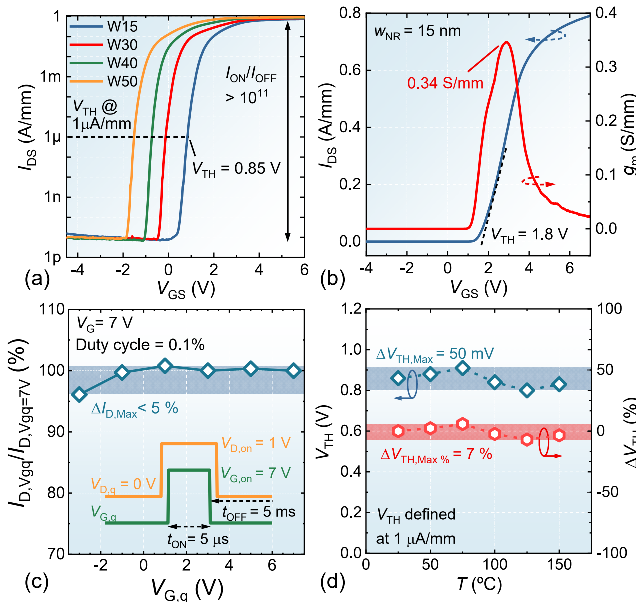

Fig. 2. (a) Transfer curve in logarithmic scale for devices having different nanoribbon width. (b) Linear transfer curve and transcondcutance for a multi-channel device with w_{NR} of 15 nm. (c) Gate lag measurement (d) V_{TH} temperature stability for an e-mode multi-channel device.

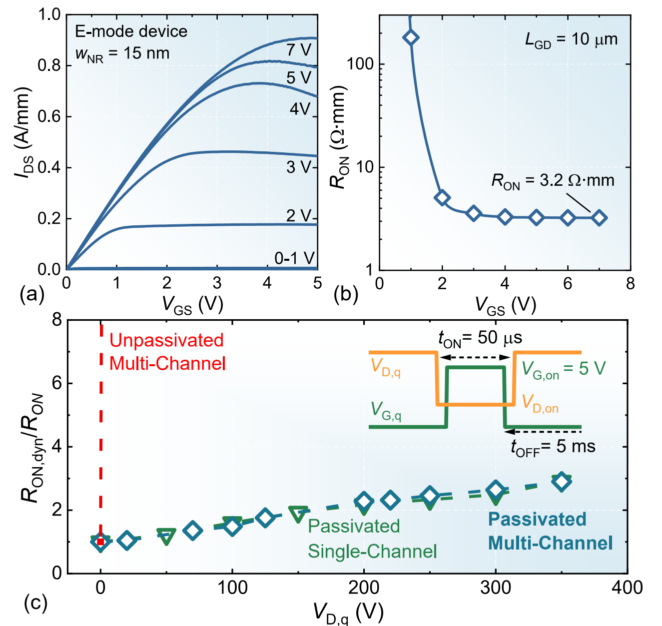

Fig.3. (a) Output curve for a normally-off multi-channel device having w_{NR} of 15 nm and L_{GD} of 10 µm (b) On-resistance vs gate voltage extracted from (a). (c) Dynamic on-resistance as a function of the quiescent drain voltage for unpassivated multi-channel devices and passivated multi- and single- channel devices. The top right inset shows the pulse schematics used to perform the measurement.

II. Device Structure

The multi-channel AlGaN/GaN heterostructure herein proposed is comprised of 4 parallel 2DEG channels (Fig. 1 (b)). The top 3 channels included 20 nm AlGaN barrier (Si-doped with a concentration of 10^{19} cm^{-3}), 1 nm AlN spacer, and a 20 nm unintentionally-doped (UID) GaN channel layer, while the last channel featured a 10 nm AlGaN barrier (Si-doped with a concentration of 5×10^{18} cm^{-3}) and 1 nm AlN spacer. The electron mobility and concentration, extracted by Hall measurement are 1930 $cm^2 \cdot V^{-1}s^{-1}$ and 3.9×10^{13} cm^{-2} respectively, which results in a sheet resistance of 83 Ω/sq.

The multi-channel device fabrication started with electron-beam lithography to define the mesa and the nanoribbon in the gate region (Fig. 1 (a-c)), followed by Cl_2-based inductively coupled plasma etching (ICP). The etch depth was set to 250 nm. The design of the nanoribbons in the gate region is shown in Fig. 1 (c). Each nanoribbon comprises, from the source to the drain, a 500 nm-long straight portion whose width was tuned to adjust the device threshold voltage (V_{TH}) and achieve e-mode operation, a 700 nm-long slanted portion which acts as a field plate and reduces the high-off state electric field, and a 1 µm-long termination region where the gate electrode is terminated. Reference devices without the slanted portion and with the gate electrode termination on the planar region were fabricated for comparison.

Following the dry etching, a 5-cycle O_2 plasma/HCl treatment was performed to reduce the etching damages on the nanoribbon sidewalls. A passivation stack comprising 2 nm of ALD SiO_2 and 100 nm of LPCVD Si_3N_4 was deposited [6]. The ALD deposition took place at 300 °C while the LPVCD deposition occurred at 770 °C with a flow of 30 sccm of SiH2Cl2 and 180 sccm of NH3 at a chamber pressure of 100 mT. The 2 nm-thick SiO_2 served as an interlayer and protected the GaN surface from desorption during the LPCVD deposition [11], [12]. The passivation stack was removed in the gate and contact regions with low power RIE etching to enable the formation of tri-gate and tri-ohmic structures. A Ti/Al/Ti/Ni/Au metal stack was evaporated and annealed at 780 °C for 30 s to form the ohmic contacts, followed by the deposition of 25 nm-thick ALD SiO_2 layer, which served as the gate oxide. Lastly, a Pt/Au (40 nm / 100 nm) gate metal stack was deposited. The device dimensions are L_{GS} = 1 µm, L_G = 1.5 µm and L_{GD} = 10 µm. Reference single-channel devices were fabricated in the same batch and underwent the same fabrication steps.

III. Device Characterization

Figure 2 (a) reports the transfer curve of multi-channel devices with different nanoribbon widths (w_{NR}) (see Fig. 1 (c)), which shows that precise control of the device threshold voltage V_{TH} can be achieved by simply designing the nanoribbon geometry. Besides, the reduction of w_{NR}, in combination with large work-function gate metals [13], enables to reach enhancement-mode operation with V_{TH} of 0.85 V at 1 µA/mm for w_{NR} of 15 nm, despite the large carrier density (3.9×10^{13} cm^{-2}) of the multi-channel heterostructure. The transfer curve of multi-channel devices with w_{NR} of 15 nm show V_{TH} of 1.8 V from linear extrapolation and a large transconductance (g_m) peak of 0.34 S/mm thanks to the large N_s. The threshold voltage stability of the presented multi-channel devices was tested both during switching operation and at high temperatures. In particular, a gate lag measurement was performed to characterize the V_{TH} variation during pulsed conditions. To this end, the device was stressed for a time t_{off} = 5 ms at a quiescent gate voltage $V_{G,q}$ with a drain bias $V_{D,q}$ of 0 V and then briefly switched-on to $V_{G,on}$ of 7 V and $V_{D,on}$ of 1 V for a time t_{on} = 5 µs during which the drain current I_D was measured (Fig. 2 (c)). A shift of V_{TH} due to the gate stress would result in a variation of I_D. Figure 2 (c) shows a negligible drain current variation of less than 5 % in the whole $V_{G,q}$ range between -2 V to 7 V for the multi-channel tri-gate devices, which demonstrates their excellent

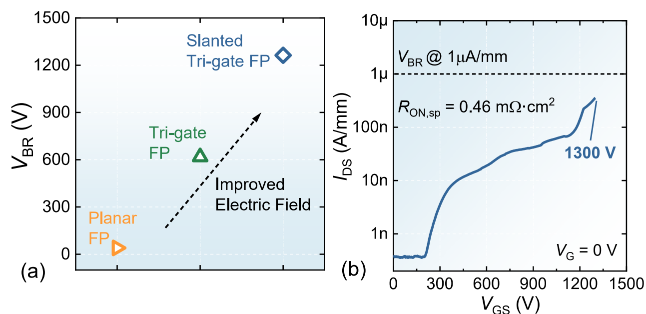

Fig.4. (a) Breakdown voltage for multi-channel devices having planar field plate termination, tri-gate field plate and slanted tri-gate field plate. (b) Off-state leakage current as a function of the drain-to-source voltage (V_{DS}), showing breakdown voltage of 1300 V.

V_{TH} stability during switching operation. The threshold voltage stability was also tested at high temperatures by mounting the device on a heated stage and measuring its transfer curve. A negligible V_{TH} variation below 50 mV is measured in a temperature range up to 150 °C (Fig. 2 (d)), which shows good V_{TH} stability also at elevated temperatures. The output curve for a multi-channel normally-off device with w_{NR} is reported in Fig. 3 (a) which presents a large saturation current of 900 mA/mm and a very low on-resistance (R_{ON}) of 3.2 Ω·mm, with full device turn-on for gate voltages above 4 V (Fig. 3 (b)). Such low R_{ON} for a device with L_{GD} of 10 µm is possible thanks to the much-reduced sheet resistance of the multi-channel platform compared to conventional single-channel heterostructures. It is of great importance that a low R_{ON} is maintained also during switching operation. To reduce current collapse, a conformal SiO_2/Si_3N_4 passivation layer was deposited around the nanoribbons terminations (Fig. 1 (a-c)) and in the planar drift region. The dynamic on-resistance $R_{ON,dyn}$ was measured with a double-pulse test (DPT) setup. First, the device was stressed in the off-state for a time t_{off} = 5 ms with a large drain quiescent voltage $V_{D,q}$ and then it was switched on with a V_G of 5 V for a short time t_{on} = 50 µs during which its on-resistance was measured (Fig. 3 (c)). While unpassivated multi-channel devices show a large increase of their $R_{ON,dyn}$, even at low $V_{D,q}$, such degradation was strongly reduced for passivated multi-channel devices, which presented good dynamic on-resistance up to large $V_{D,q}$ of 350 V. Notably, the $R_{ON,dyn}$ behavior and values of multi-channel tri-gate devices is similar to the ones of reference single-channel devices with conventional gate electrode termination on the planar drift region, which suggests that further reduction $R_{ON,dyn}$ could be achieved by improving the passivation layers quality.

To manage the large off-state field in such highly conducting and three-dimensional heterostructures, novel field plate structures are required. In particular, conventional gate field plates with the gate electrode termination on the planar part of the drift region are not effective due to their inability to deplete all of the embedded channels and result in early device breakdown at about 40 V (Fig. 4(a)). A more suitable solution for multi-channel structures is achieved by a tri-gate field plate. In this case, the nanoribbon width is enlarged from ~ 15 nm (which is required to achieve e-mode operation) to ~ 100 nm in the termination region (Fig. 1 (c)). The gate electrode is conformally deposited around the nanoribbon with its edge being placed in the termination region, which results in a tri-gate field plate, whose threshold voltage can be set by tuning the nanoribbon width. Thanks to this approach, the breakdown voltage of multi-channel devices can be considerably increased to above 600 V. In addition, by designing a slanted transition between the nanoribbon e-mode and termination region (Fig. 1 (c)), it is possible to realize a slanted tri-gate field plate [14], [15], which further improves the off-state electric field and resulted in V_{BR} of 1300 V. In particular, figure 4 (b) shows the off-state leakage for a multi-channel device with slanted tri-gate field plate which presents low current values well below 1 µA/mm and large hard-breakdown at 1300 V. Combined with a much reduced specific on-resistance ($R_{ON,sp}$) of 0.46 mΩ·cm^2, this results in a large high-power figure-of-merit of 3.8 GW/cm^2, which shows the promising potential of this technology for power conversion applications.

IV. Conclusions

In this work, we demonstrated multi-channel tri-gate HEMT based on a multiple channel heterostructure and a nanostructured gate region. Thanks to this approach, e-mode devices showing very low specific on-resistance combined with large breakdown voltage were achieved. Besides, we demonstrated multi-channel devices showing excellent V_{TH} stability and reduced current collapse. We believe that these results show the promising potential of the multi-channel tri-gate technology for future power conversion applications.

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