PCIM Europe Digital Days 2021

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Abstract

In this paper, the real-time simulation model of the modular multilevel converter was split into several independent parts through the use of the virtual capacitor concept. As a result, the number of state-space matrices the real-time solver needs to take into account reduces, which leads to the simulation step size decrease. The proposed concept was verified on a large-scale hardware-in-the-loop system comprising seven RT Boxes, where the model of the physical system is deployed, and ABB PEC800 industrial controller, where control algorithms of the real power hardware are executed.

1 Introduction

Nowadays, Hardware-In-The-Loop (HIL) real-time simulations can be described as an irreplaceable tool in the testing of complex control systems. The idea implies the connection, ensured using an appropriate interface, of a tested controller and an HIL simulator, where the model of a physical system is deployed. Simulator inputs are read within a fixed time step and used subsequently to provide an output being as close as possible to the response obtained in the real physical system. In this way, the controller being tested cannot differentiate between the HIL simulator and real power hardware. Consequently, an environment allowing for fast and risk-free testing of various control schemes is ensured, which is of high importance especially if large and expensive systems are considered.

Modeling of any power electronics system stands in a tight connection with an employed model of the switch, which can be found in one of two possible states - on or off. While various switch models (e.g. [1], [2]), adopted in the real-time simulation domain, can be considered, this work relies on the use of ideal switches. Therefore, in an electric network containing n switches, the number of distinct topologies (states) created through different combinations of devices being on/off equals 2^n. Furthermore, depending on the employed calculation approach, every valid configuration detected within the set of possible 2^n states can be associated with an appropriate state-space [3] or admittance matrix [4].

Due to frequent changes in the circuit states, guaranteeing high fidelity of the real-time simulation requires step sizes to fall within the boundaries of several microseconds or even hundreds of nanoseconds. To avoid time-consuming calculations of relevant system matrices (e.g. in the state-space), these are normally pre-computed and stored in the simulator memory. On these terms, a set of pre-computed matrices, used in the upcoming simulation step, must be selected and loaded from memory, which is an inevitable time expense. However, the higher the number of switches, and simultaneously the matrices, the longer the time needed for the simulator to select the matrix being applied in the upcoming switching period. Thus, one can conclude that simulation speed and the ability to address as many switching devices as possible represent two contradictory requirements.

Modular Multilevel Converter (MMC) [5], depicted in **Fig.** 1, comprises a series connection of submodules (SMs), which are normally found in Half-Bridge (HB) or Full-Bridge (FB) configuration, while other choices have been listed in [6]. By stacking the SMs in series, theoretically unlimited voltage scalability is provided, while current capacity

ISBN 978-3-8007-5515-8

increase can be achieved in several ways, as explained in [7], [8]. In spite of the advantages mentioned above, a series connection of SMs comprises a high number of switching devices, making the MMC implementation challenging for any real-time simulator. Such a technological hurdle can be circumvented through an appropriate compression of the simulated circuit, meaning that sophisticated modeling approaches, putting the emphasis on minimization of the number of modeled switches, need to be considered. In summary, employing a suitable modeling technique allows real-time simulations, being out of reach otherwise, to be feasible. Even though different real-time MMC models have been proposed so far, this work relies on the approach demonstrated in [9]. In this way, the versatile model of a branch allowing for emulation of all states it can be found in can be derived, providing one with the MMC model depicted in **Fig.** 2.

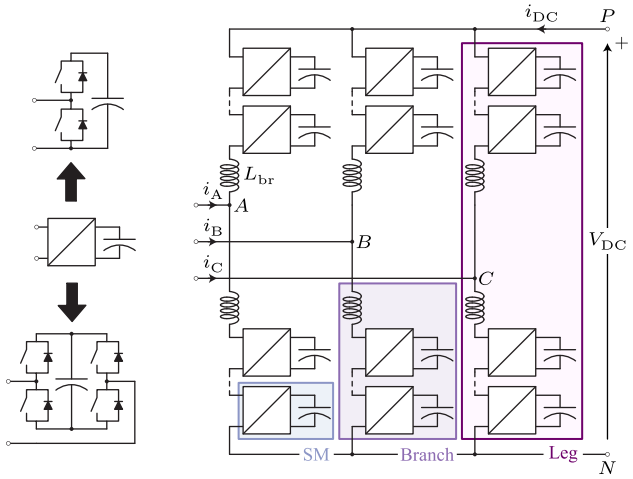

Fig. 1: MMC along with the adopted nomenclature.

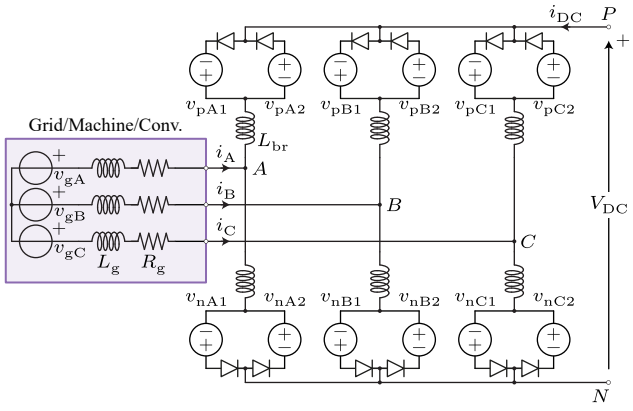

Fig. 2: MMC real-time model considered in this work.

Hereafter, subscripts ”p” and ”n” denote upper and lower quantities, respectively. According to [9], in an observed branch, voltage sources $v_{\mathrm{br},1}$ and $v_{\mathrm{br},2}$ represent a combination of SM switching signals and instantaneous values of SM capacitor voltages. As can be seen from **Fig.** 2, at its AC terminals, the MMC gets interfaced with a three-phase voltage source through a series connection of an inductor and resistor. Thus, the same model can be used for real-time simulations of an MMC connected to an AC grid, AC machine, or any other converter through an inductive interface.

Nevertheless, even if an appropriate modeling scheme is adopted, the employed simulator might not necessarily guarantee satisfactory performance. For example, the number of switching combinations can be quite high resulting in unacceptably large code used by the simulator. Furthermore, in some cases, computational effort can be too large requiring a reduction of the execution times.

The above-mentioned challenges can be addressed by splitting the model of a circuit running on the HIL simulator. Namely, an artificial delay is included in the interaction among parts of the circuit created through the splitting procedure. Consequently, separated parts of the circuit are treated independently, which reduces the number of state matrices describing the converter [10]. Moreover, different parts of the model are run on different hardware nodes, resulting in the step size reduction, which is thoroughly explained in the next section. Generally, whenever a circuit splitting is required, performing so at a point containing capacitor or inductor can be considered a good practice, as explained in [10]. Nevertheless, the MMC model provided in **Fig.** 2 does not contain a concentrated DC link, where the circuit splitting can be performed, making the model separation rather non-trivial. To eliminate this shortcoming, this paper proposes, presents and exploits the concept of the virtual capacitor. In this work, seven RT Box 1 [10] units were employed to run the real-time model of a $3.3\mathrm{kVac}/5\mathrm{kVdc},\ 250\mathrm{kW}$ MMC comprising 48 FB SMs in total. With respect to the model from **Fig.** 2, being chosen as a starting point, significant simulation step size reduction was achieved while preserving all physical properties of the original model.

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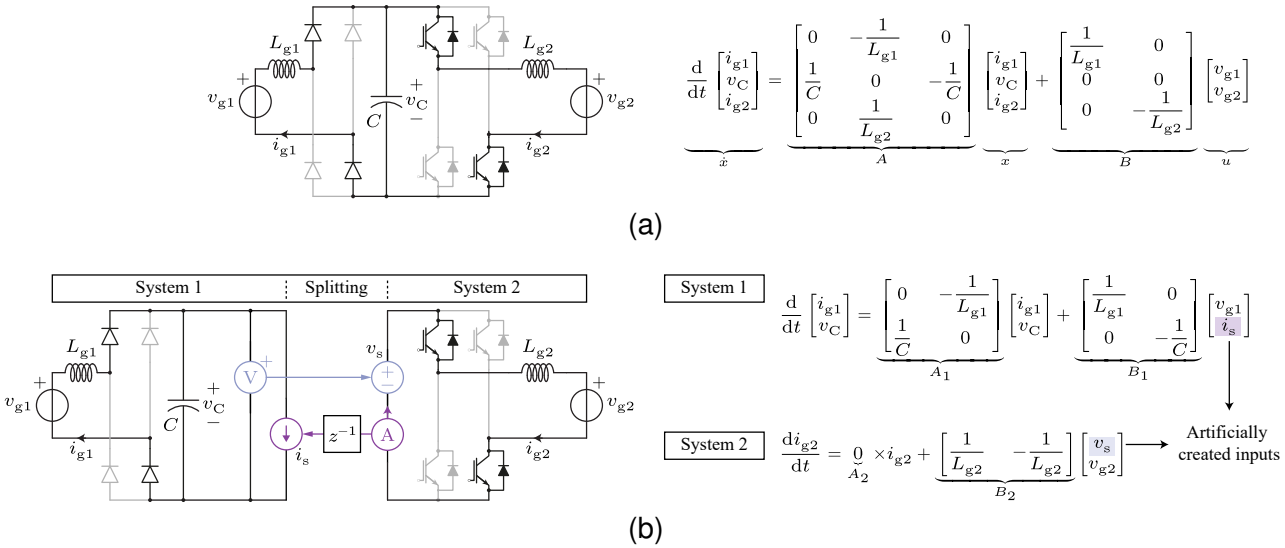

Fig. 3: An exemplary circuit used to highlight the benefits of circuit splitting upon the reduction in the number of circuits possibly created through a different combination of switches being on and off.

2 Motivation for circuit splitting

As can be seen from **Fig.** 2, the whole MMC consisting of an arbitrary number of switches can be modeled with twelve controlled voltage sources and twelve diodes, which might be perceived as a success at first glance. Nonetheless, the model from **Fig.** 2 might be improved further and before extending on this topic, its flaws should be revealed.

Namely, in case an arbitrary circuit is to be simulated, the solver running on HIL simulator employed in this work creates state-space matrices prior to commencing any real-time calculations. Thereafter, depending on the state the simulated circuit is found in, different state-space matrices are used. To update the state matrix being in use, the solver needs to recognize changes in the circuit configuration. In circuits with natural commutation, like the one in **Fig.** 2, the state-space matrix change should take place only when current through any switch crosses zero and high-fidelity simulation implies precise detection of these time instants. Unfortunately, if the circuit consists of diodes only, a high computational resource is required to achieve such a goal [11].

For the model from **Fig.** 2, the number of state-space matrices the solver must take into account equals $N_{\mathrm{mat}} = 2^{12}$. Running such a model in real-time on RT Box 1 requires the simulation step size $T_{\mathrm{step}} > 75\mu\mathrm{s}$, which is considered unacceptable from the simulation fidelity standpoint. However, if the analyzed circuit is split in, for example, two independent parts containing six diodes, the number of possible states decreases to $N_{\mathrm{mat}} = 2 \times 2^6$. Consequently, the simulation step size can be significantly reduced compared to the value indicated previously.

To provide a better illustration of the circuit splitting benefits, **Fig.** 3 illustrates this principle on an exemplary circuit found in an arbitrarily chosen state. Even though **Fig.** 3a presents only one state generated by a random combination of switches being on and off, the number of possibly created circuits equals 2^8. Splitting of the circuit from **Fig.** 3a can be performed as in **Fig.** 3b, where separation of state variables is obtained through the introduction of artificial system inputs (i.e. v_{s} and i_{s}), allowing the newly formed circuits to be described by a new set of state-space matrices $\{A_1, B_1\}$ and $\{A_2, B_2\}$, respectively. Since both systems depicted in **Fig.** 3b comprise four switching elements (from the circuit configuration viewpoint, IGBT/diode pair is considered a single element), the total number of circuits created through different switching combinations equals 2×2^4, which is an 8-fold decrease compared to the case where no splitting was performed. As the simulator must handle a significantly lower number of state-space matrices, the simulation step size reduction becomes self-explanatory.

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3 Virtual Capacitor Concept

The whole HIL concept implies the processing of virtual power and extending the system with additional component(s) is not prohibited as long as it does not corrupt the correctness of the model. For example, if an element is connected between an arbitrary DC port of the MMC and any of its AC terminals, the current flowing through the element depends on its impedance. Moreover, if an added element represents a very high impedance for low frequency (e.g. $50\ \mathrm{Hz}$) currents, which are typical for the MMC, almost no current flows through it, which is nearly identical to reality. Luckily, a capacitor, which is anyhow needed for the circuit splitting purposes, satisfies this criterion, however, its value must be properly selected.

Fig. 4 depicts the extension of the MMC model provided in **Fig.** 2 by a set of three capacitors and three resistors denoted by C_v and R_v, respectively. As these elements do not exist in reality, while they are used only for simulation purposes, they will be referred to as the Virtual Capacitors (VCs) and Virtual Resistors (VRs). Although virtual, capacitors C_v provide the means for circuit splitting, while resistors R_v ensure numeric stability, which is the topic falling out of this paper's scope, of the model from **Fig.** 4

Let one commence the analysis by observing the set of lower branches, where circuit conditions dictate the commutation process of diodes used for the branch modeling purpose. Therefore, to separate the set of lower branches from the rest of the circuit, voltages seen between terminals labeled with A, B and C must remain unchanged. Another important remark concerns the DC side voltage balance. Based on **Fig.** 4, the expression

$$V_\mathrm{DC} = \frac{1}{3}(v_\mathrm{PA}+v_\mathrm{PB}+v_\mathrm{PC})+\frac{1}{3}(v_\mathrm{NA}+v_\mathrm{NB}+v_\mathrm{NC}) \quad (1)$$

can be derived and this is the first condition that the circuit created in the splitting procedure must fulfill. Also, the Kirchhoff Voltage Loop (KVL) equations formed around the lower branches set must correspond to the original circuit, which can be accomplished in case the structure from **Fig.** 5 is used. However, the choice of voltage components v_1, v_2 and v_3 must be clarified. These voltages must ensure the satisfaction of two criteria:

1. KVL equations (loops labeled with 1 and 2 in **Fig.** 5) must correspond to the ones observed in the original circuit from **Fig.** 2,
2. What is seen from the DC terminal must be equivalent to the original circuit from **Fig.** 2.

Both requirements set above are met in case

$$\begin{bmatrix} v_1 & v_2 & v_3 \end{bmatrix}^T = \begin{bmatrix} v_\mathrm{PA} & v_\mathrm{PB} & v_\mathrm{PC} \end{bmatrix}^T. \quad (2)$$

Once the set of lower branches is modeled, it can be separated from the upper branches set. As every branch represents a series connection of a voltage source and an inductor, lower branches can be replaced by controlled current sources, which are fed with the lower branch current measurements, as presented in **Fig.** 6. To be consistent with the principle illustrated in **Fig.** 3 currents flowing through the controlled voltage sources v_1, v_2 and v_3 get passed to the controlled current sources being in parallel to the set of VCs.

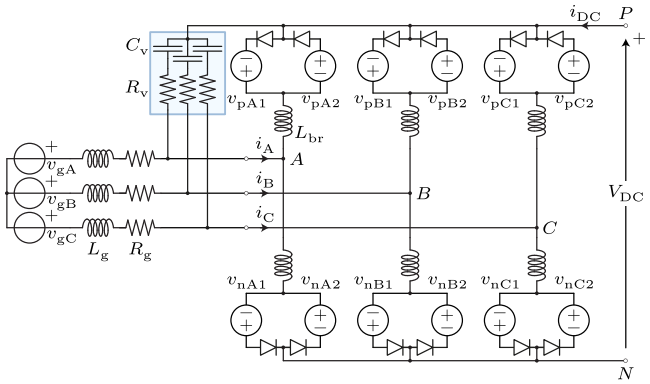


Fig. 4: Extension of the original MMC by virtual elements highlighted in blue.

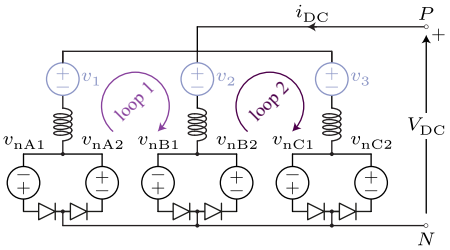


Fig. 5: Separating the set of lower branches from the original MMC model.

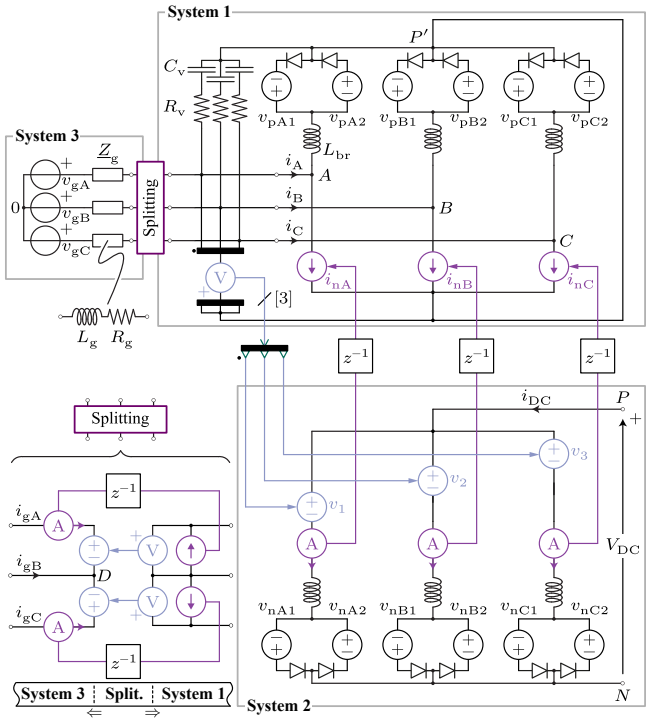


Fig. 6: Model of the MMC obtained through the splitting procedure discussed throughout the paper.

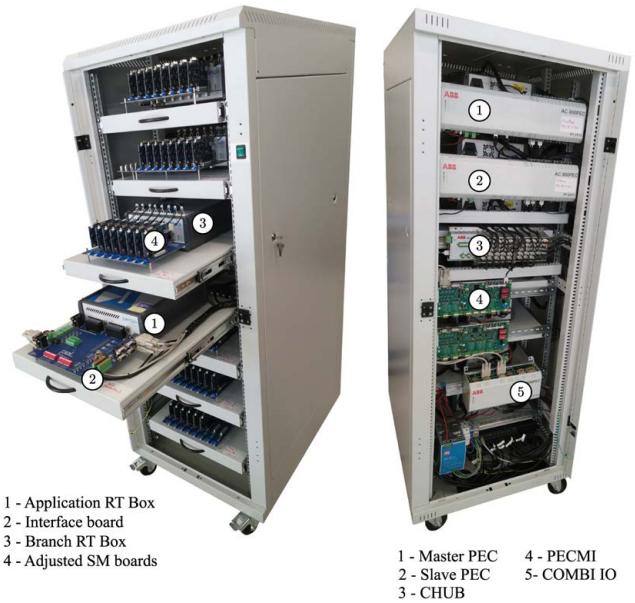
As currents of controlled sources i_{nA}, i_{nB} and i_{nC} do not sum up to zero, the star point at which these sources meet must be connected to the point labeled with P'. In this way, each one of the upper branches becomes parallel connected to the current source being fed with the current of its lower counterpart. In other words, seen from the AC terminals, branches operate in parallel, which can also be seen from the basic MMC equations (e.g. [12]). Lastly, by establishing equations, according to Kirchhoff current and voltage laws, for circuits depicted in **Figs.** 4 and 6, one can realize that the behavior of both terminal and internal MMC currents remains unchanged, which was exactly the goal set prior to commencing the circuit splitting procedure. Lastly, the part of **Fig.** 6 labeled with "Splitting" depicts additional convenience provided by the presence of VCs. Namely, as currents flowing through the AC sources v_{gA}, v_{gB} and v_{gC} sum up to zero, this part of the model can be separated from the circuit containing the upper branches. In summary, the MMC model from **Fig.** 2 was split into three parts, allowing for the model depicted in **Fig.** 6 to run with the step size of $T_{\mathrm{step}} = 7\mu\mathrm{s}$.

4 Model Verification

4.1 Setup description

As presented in **Fig.** 7a, the setup used for HIL verification purposes comprises seven RT Boxes. 48 SM cards, hosting the digital signal processor and logical circuitry of the real MMC SM, described in [13], were interfaced with six Branch RT Boxes performing calculations of relevant branch voltage components ($v_{\mathrm{br},1}$ and $v_{\mathrm{br},2}$) based on the SM switching signals and instantaneous values of SM DC voltages. The seventh RT Box (fourth from the top in **Fig.** 7a), referred to as the Application RT Box, hosts the model given in **Fig.** 6.

In **Fig.** 7b, two ABB PEC800 controllers can be recognized and they are connected in the Master/Slave structure. The main reason for such a choice lies in the fact that several of these HIL systems can be connected to operate in various configurations. For example, the control performance of multiple series-connected MMCs, as mentioned in [14], can be tested, while other options (e.g. back-to-back connection of two MMCs) are not excluded either. Slave controller is assigned the task of controlling the MMC, while Master controller is to handle general (application) state machine and references. Other



(a) Front view (b) Rear view

Fig. 7: HIL system used for model verification purposes.

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parts of the system visible in **Fig.** 7b are in charge of voltage/current measurements (PECMI), distribution of SM optical signals (CHUB) and manipulation of relays, switches and other user-defined arbitrary signals (COMBIO). The real MMC prototype uses the identical control structure, making all of the presented results realistic.

4.2 Results

To validate the model described throughout the previous paragraphs, the system with parameters given in **Tab.** 1 was simulated on the previously described setup. Verification of the model is conducted based on different operating regimes described hereafter.

4.2.1 No load operation

To prove that the demonstrated modeling approach can be used in case the converter branches receive switching signals, no load operation is presented in **Fig.** 8. To control the grid currents, branches receive voltage references being realized through the PWM principles. As the number of SMs per branch equals $N_{\mathrm{SM}} = 8$, while only half of the available branch voltage range ($\{-v_{\mathrm{br}\Sigma}/2 \ldots v_{\mathrm{br}\Sigma}/2\}$) is used, every branch creates up to $N_{\mathrm{SM}} + 1 = 9$ voltage levels, which is straightforward to confirm from **Fig.** 8. As no power is processed to the DC side, the converter total energy balancing requires almost no current to be drawn from the AC side.

Tab. 1: Rated parameters of the simulated converter

Parameter	Label	Value
Rated power	S^*	0.25 MVar
Output voltage	V_{DC}	5 kV
Grid voltage	v_{g}	3.3 kV
No. of SMs per branch	N_{SM}	8
SM capacitance	C_{SM}	2.25 mF
Branch inductance	L_{br}	2.5 mH
Branch resistance	R_{br}	60 mΩ
PWM carrier freq.	f_{c}	1 kHz
Fundamental freq.	f_{o}	50 Hz
Grid inductance	L_{g}	13.86 mΩ
Virtual capacitance	C_{v}	360 nF
Virtual resistance	R_{v}	45 Ω
Simulation step size	T_{step}	7 μs

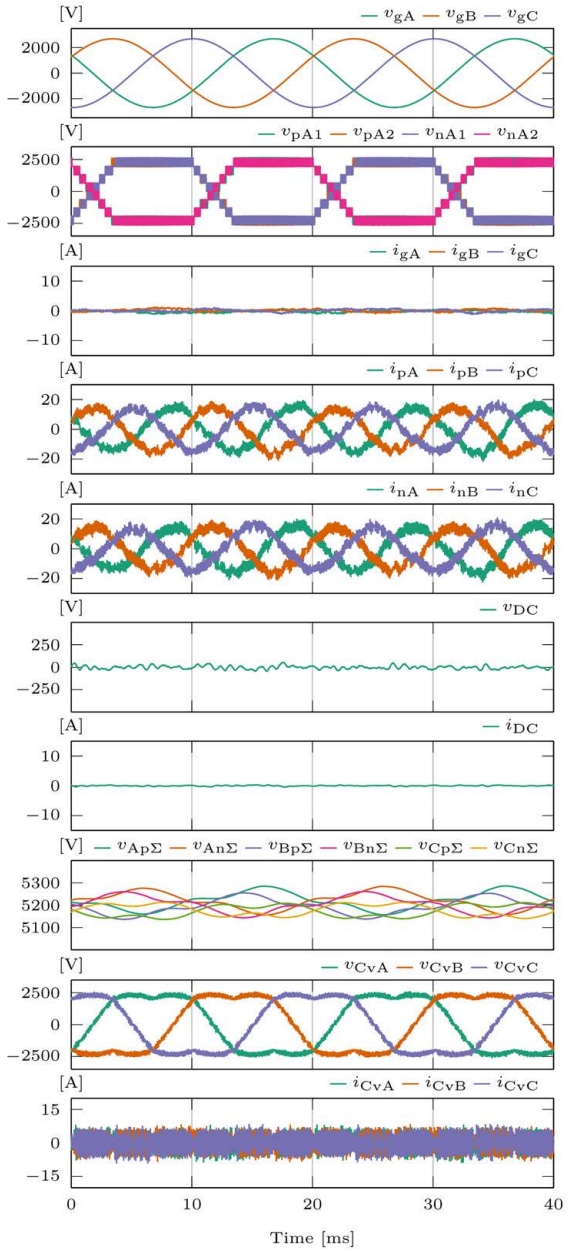

Fig. 8: Converter operation at no load ($P_{\mathrm{DC}} = 0$).

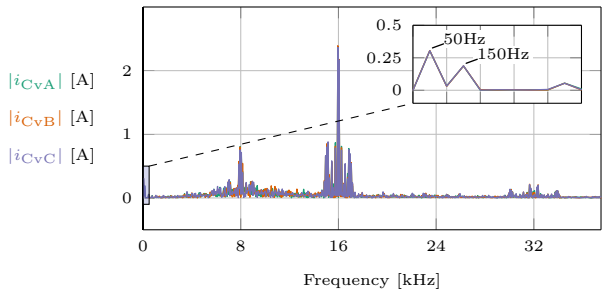

Fig. 9: Spectral content of VC currents in case converter operates with no load on the DC side.

The second last plot from **Fig.** 8 shows voltages measured across the VCs. As expected, voltages v_{CvA}, v_{CvB} and v_{CvC} follow the shape of the upper branch voltage references. To provide a better insight into the VC currents, **Fig.** 11 provides their spectral content. Owing to the switching nature of the branches, most of the spectral energy is concentrated around the multiples of the frequency equal to $N_{\mathrm{SM}} f_{\mathrm{sw}}$. Yet, the fundamental frequency component in the VC currents equals $i_{\mathrm{Cv}}(f_{\mathrm{o}}) \approx 0.25\mathrm{A}$, which is around 0.4% of the nominal AC current. Hence, this current component can be considered negligible.

4.2.2 Operation at full load

Fig. 10 presents the converter operating waveforms in case energy is transferred from AC to DC side (rectifier mode) at nominal power. As the grid currents increase in amplitude so do the branch currents, which, in conjunction with branch voltages, causes branch powers, and inherently voltages, to oscillate. Similarly to the case considering operation at no load, DC voltage and current contain the switching ripple, however, with mean values being different than zero.

Similarly to **Fig.** 11, the spectral content of VC currents was presented in **Fig.** 11 indicating that, irrespective of the operating regime, VC currents fall significantly bellow the converter nominal currents. It is noteworthy that controllers react only to low-frequency components of currents/voltages, given that these are the only ones taking part in the energy transfer. To put it differently, in this case, converter voltage and current ripples are filtered out with the aim of controlling only the fundamental and DC components. As a result, the presence of the virtual network does not alter the basic functionality of the employed MMC model, while allowing for a significant reduction in the simulation step size.

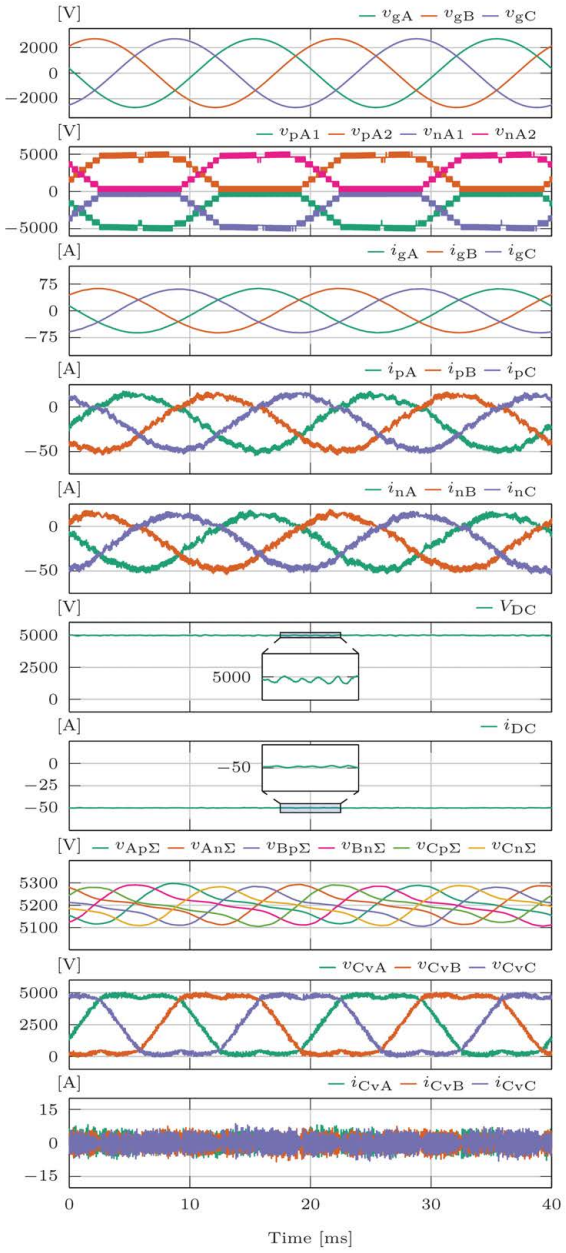

Fig. 10: Converter operation at full load ($P_{\mathrm{DC}} = 250\mathrm{kW}$).

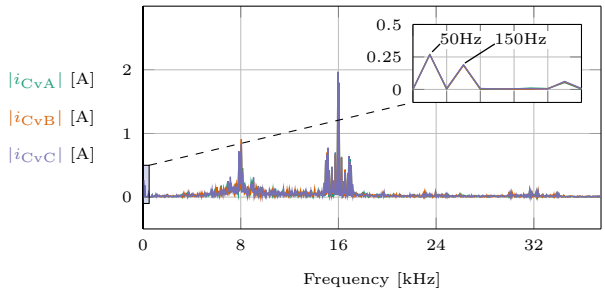

Fig. 11: Spectral content of VC currents in case the converter operates with full load.

5 Conclusion

This paper proposed and elaborated in detail the application of the virtual capacitance concept on the MMC real-time model. It targets small-scale real-time simulators, relying on the state-space modeling and requiring large simulation step sizes in case topologies with a large number of switching elements are considered. Extending

ISBN 978-3-8007-5515-8

the MMC real-time model by the set of virtual capacitors allows for the model splitting, which leads to a significant reduction in the number of state-space matrices describing the system. Consequently, more than a tenfold reduction in the simulation step size was observed in the example analyzed throughout this work. The name virtual originates from the fact that currents flowing through the set of introduced capacitors fall significantly bellow the converter nominal currents. What is more, virtual capacitors conduct high-frequency components, however, these are normally ignored (filtered) by the controller tested against a real-time simulator. Therefore, one can claim that the proposed extension of the MMC model does not alter its basic functionality.

Acknowledgment

This work has received funding in part from the European Union's Horizon 2020 research and innovation programme under Grant Agreement No 881772 (FUNDRES project) and in part from the Swiss Innovation Agency - Innosuisse, as the innovation project 38041.1 IP-ENG.

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