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Co-designing electronics with microfluidics for more sustainable cooling

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Thermal management is one of the main challenges for the future of electronics [1]–[5]. With the ever increasing rate of data generation and communication, as well as the constant push to reduce volume and costs of industrial converter systems, the power density of electronics rises [6]. Consequently, cooling has an increasingly large environmental impact [7], [8], and new technologies are needed to efficiently handle the heat in a sustainable and cost-effective way [9]. Embedding liquid cooling directly inside the chip is a promising approach for a more efficient thermal management [5], [10], [11]. However, even in state-of-the-art approaches, the electronics and cooling are treated separately, leaving the full energy-saving potential of embedded cooling untapped. Here we demonstrate that co-designing microfluidics and electronics into the same semiconductor substrate, to produce a monolithically-integrated manifold microchannel (mMMC) cooling structure, provides efficiency beyond the state-of-the-art. Our results show that heat fluxes exceeding 1.7 kW/cm^2 can be cooled down using only 0.57 W/cm^2 of pumping power. We observed an unprecedented coefficient of performance (>10^4) for single-phase water-cooling of heat fluxes exceeding 1 kW/cm^2, corresponding to a 50-fold increase compared to straight microchannels, as well as a remarkably high average Nusselt number of 16. The proposed cooling technology enables further miniaturization of electronics, potentially extending Moore's law and greatly reducing energy consumption worldwide. Furthermore, by removing the need for large external heat sinks, we demonstrate how this approach enables ultra-compact

power converters integrated on a single chip, supporting the electrification trend of our society.

Data centers, in the US alone, consume 24 TWh of electricity and 100 billion liters of water to satisfy their cooling demands [8], corresponding to the residential needs of a city of the size of Philadelphia [12]–[14]. Their environmental impact is expected to increase dramatically [9], accounting for 31% of the Ireland's electricity demand by 2027 [15]. This development is accompanied by the constant push to reduce the size of semiconductor devices, which results in higher heat-fluxes that become increasingly challenging to cool down. A similar trend is observed in power electronics, as the electrification of our society demands more powerful, efficient and smaller energy conversion systems. Wide-band-gap semiconductors, such as gallium nitride (GaN), are promising candidates for this purpose [16]. These materials enable much-smaller dies than traditional semiconductors as well as the monolithic integration of power devices, supporting the miniaturization of complete power converters into a single chip [17]. However, to unlock its full potential, new strategies for sustainable cooling of high heat-flux applications are required.

Significant research efforts focus on improving the thermal path between the hot-spot and the coolant [12]. However, their heat extraction capability is fundamentally limited by the thermal resistance between the semiconductor die and packaging. Furthermore, relying on large heat sinks hinders the power density and integration, since devices cannot be densely packed. Bringing the coolant in direct contact with the device is an actively-investigated strategy to break this limit. For example, impinging coolant on a bare die [18], or etching micrometer-sized channels directly inside the device to turn the substrate into a heat-sink. The latter demonstrated state-of-the-art cooling performance by exploiting the much-improved heat transfer at the microscale [19]–[21]. The high pressure drop and large temperature gradients associated with these straight, parallel microchannels (SPMCs) were overcome by splitting the flow into multiple parallel sections, and distributing the coolant over these channels using manifolds [22]. Early investigations [23]–[26] and systematical numerical studies [27]–[30] of

manifold microchannel (MMC) heat sinks showed a significant reduction in pumping power requirements and thermal resistance compared to SPMCs. Excellent heat extraction has been demonstrated with copper microchannels [31], compact micro-fabricated multi-layer silicon structures [32]–[35], and by using additive manufacturing [36] [37]. However, in all these approaches, the heat sink and electronic structure and fabrication process are considered separately, either by integrating a simple resistive heater functioning as heat source, or by bonding the MMC structure to a commercial device [38]. This leaves the large potential of MMCs untapped. Improving the thermal coupling between the heat source and cooling was investigated for hot-spot mitigation [39]–[41], but remained unexplored for a complete device structure. Furthermore, despite the long history of MMC heat-sinks research, the increasing complexity and associated reliability concerns due to the multiple bonded layers required for coolant delivery have prevented its adoption in commercial devices.

In this work, we address these concerns by demonstrating a new paradigm for cooling and device design, in which a MMC heat-sink is designed and fabricated in conjunction with the electronics. This led to a novel *monolithically-integrated* manifold microchannel (mMMC) heat-sinks in a single-crystalline silicon substrate without the need for cumbersome bonding steps. Here the device design and heat-sink fabrication are combined within the same process, with buried cooling channels embedded right below the active area of the chip. Coolant impinging directly underneath the heat sources provides local and efficient heat extraction (Fig. 1a). Within this same substrate, manifold channels spread the liquid over the die (Fig. 1c) to obtain high temperature-uniformity and low pressure-drop, leading to a very low pumping-power consumption and vastly improved cooling performance. Since the electronics and microfluidics are fully coupled and aligned (Fig. 1b), this approach is denominated as *Microfluidic-electronic co-design*. We demonstrated this microfluidic-electronic co-design on GaN-on-Si, a low-cost platform promising for realizing high-power converters on a chip, comprising a few micrometer-thick GaN epilayer on a low-cost silicon substrate. The passive silicon substrate typically lacks functionality, but by turning it into an active cooling layer, it has the potential to extract extreme

heat fluxes, without the added cost of high-thermal conductivity substrates. Our results show that considering cooling as an integral part of device design can result in orders-of-magnitude improvement in cooling performance. The embedded-cooling approach is used to demonstrate a super-compact GaN-on-silicon integrated AC-DC converter, containing four power devices on the same microfluidic-cooled chip, yielding a power density of 25 kW/dm^3. A simple multi-layered printed circuit board (PCB) was designed to direct the coolant flow into the semiconductor device.

Co-design concept and fabrication

Our proposed co-design approach, where each heat source is coupled to an individual buried cooling-channel serving as a local heat sink, is particularly interesting for lateral GaN power electronic applications. Typical source-drain spacing for high electron mobility transistors in >1kV applications matches the optimum dimensions for microchannel cooling of ~20 μm, [19], [42]–[44]. Therefore, we investigated a GaN-on-Si device structure in which liquid impinges directly onto the epilayer below each contact, ensuring minimum thermal resistance between the hot-spot and coolant. In this structure (Fig. 1a), the GaN epilayer provides the power electronics (Fig 1b), and the silicon functions as microchannel cooling and fluid-distribution network in a 3D arrangement (Fig 1c). Figure 1d illustrates the corresponding fabrication method. A staggered pattern of slits was formed in the Si by anisotropic deep-etch through narrow incisions in the AlGaN/GaN epilayer to achieve the desired microchannel depth. This pattern provided better structural integrity of the epilayer during fabrication compared to continuous slits. During the subsequent isotropic gas-etch, the channels widened and coalesced in the silicon substrate, while monitored through the transparent GaN epilayer using an in-situ optical etch-rate tracking. This two-step etching process provides independent control over channel width and depth, making it suitable to a wide range of contact pitches. The incisions were finally hermetically-sealed during the device metallization step. The methods section, as well as Extended data Fig. 1, explain the fabrication procedure in details. Figure 1e shows a scanning electron microscope (SEM) image of the device after the

metallization step with sealed channels. Because of the narrow incisions in the epilayer, the contacts do not require significant oversizing. The microchannels are in direct contact with the active area of the chip, thus providing excellent thermal coupling between the hot-spot and the cooling channel (Fig. 1f). Through micron-sized openings in the AlGaN/GaN layer, 125 μm-deep and *2*0 μm-wide channels were realized in the silicon substrate (Fig. 1g,h).

A series of devices was fabricated with SPMCs with equal width and spacing of 100 μm, 50 μm and 25 μm, and a channel depth of 250 μm in GaN-on-Si power devices, functioning as reference heat sinks (Fig. 2a) for evaluating the performance of the co-designed electronic-microfluidic mMMC devices. mMMC chips with 2, 4 and 10 inlet and outlet manifold channels and identical 20 × 125 μm microchannels were fabricated, referred to as 2x, 4x and 10x-manifold (Fig. 2b). Figure 2c shows a picture of the mMMC device with 10x-manifold, including a schematic (Fig 2d) to illustrate the flow path with coolant impinging directly onto the bottom of the GaN epilayer.

Thermo-hydraulic evaluation

A thermo-hydraulic analysis, using de-ionized water as a coolant, was performed on the 6 cooling structures (Fig. 2a,b) to assess the cooling performance by measuring the thermal resistances, pressure drop and the resulting cooling coefficient-of-performance (COP), which indicates the energy efficiency of the heat sink. Fig. 3a shows the total thermal resistance (R_{tot}) between the surface temperature-rise and the inlet temperature for the evaluated structures. By reducing the SPMC channel dimensions from 100 μm to 25 μm at identical flow rates, R_{tot} reduces, which can be attributed to the increased surface area for heat transfer. However, the 4x- and 10x-mMMC heat sinks show an additional significant reduction in R_{tot} compared to the 25 μm SPMC, approaching the limit of single-phase water-cooling (defined by its heat capacity). R_{tot} was separated in three terms: the contribution due to the heating of the water based on its heat capacity (R_{cal}), the contribution due to convective heat-transfer in the microchannels (R_{conv}), and the contribution due to conduction (R_{cond}). The full data reduction procedure to obtain these values is explained in the Methods section, as well as in Extended

Data Fig. 3. A breakdown of R_{tot} is shown in Fig. 3b, revealing a strong relation between R_{conv} and microchannel size, where smaller channels reduce $R_{conv.}$ A significant further decrease in R_{conv} was achieved with the 10x-manifold, resulting in an 85% and 76% reduction compared to 50 μm and 100 μm SPMC, respectively. In combination with a very low R_{cond} for the co-designed manifolds, at a flow rate of 1.0 ml/s, a thermal resistance of 0.43 K/W was achieved. The 10x-manifold design thus allows heat fluxes up to 1723 W/cm^2 for a maximum temperature rise of 60 K, which is more than twice that of a 25μm-wide SPMC.

Narrow channels, however, require a higher pressure to achieve equal flow rate (Fig. 3c). For a flow rate of 0.5 ml/s, microchannel widths of 100 μm, 50 μm and 25 μm require pressures of 160 mbar, 260 mbar and 810 mbar, respectively. The manifold structure significantly lowers the pressure drop by reducing the length of the flow path through the microchannel. When splitting the flow in smaller sections with the 10x-manifold, the pressure drop reduced significantly to 210 mbar. This highlights the benefit of the MMC structure: a lower thermal resistance than SPMCs can be obtained at a reduced pumping power consumption. However, although the manifold structure can reduce the pressure drop, the additional contractions and turns of the fluid can hinder this reduction. For example, 20 µm-wide microchannels in a 4x-manifold require a significantly higher pressure of 1300 mbar compared to 25 μm-wide SPMC (Fig. 2d), which in part can also be attributed to the higher fluid velocity as the mMMC channels (125 μm) are not as deep as the SPMC (250 μm). These finding demonstrate the need for a carefully optimized geometry of the microchannel and manifold.

Fig. 3d shows a clear trend for SPMCs of increased effective base-area averaged heat-transfer coefficient (h_{eff}) for smaller microchannels. This is due to the combined effect of the increased surface area and local heat-transfer coefficient in fully-developed laminar-flow regime. The co-designed mMMC structures with 4x-manifold channels and 20 µm-wide microchannels matches this trend with h_{eff} = 3.1 × 10^5 W/m^2-K, but a large deviation from this pattern is observed when the effective length through which the coolant flows in the microchannel is reduced. For the 10x-manifold, h_{eff} more than doubles to 7.3 × 10^5 W/m^{2}K, a rise that can be

accounted to the much-increased Nusselt number due to the developing flow in the MMC structure [27], [45]. This effect becomes more pronounced by considering the wall-area averaged heat-transfer coefficient (h_{wall}) (Fig. 3e), which eliminates the contribution of the increased surface area from the heat-transfer coefficient, as well as accounts for the limited fin efficiency of the channels. Over a 3-fold increase in h_{wall} is observed between 25 μm-straight microchannels and the 10-channel mMMC heat-sinks, up to 2.4×10^6 W/m^2-K. This value corresponds to a remarkably high Nusselt number of 16, generally only achieved in larger-scale systems, or in more complex two-phase cooling systems, highlighting the superior thermal performance of this structure.

The combination of improved heat transfer and reduced pressure drop leads to significantly lower pumping power requirements. The cooling COP is defined as the ratio of extracted power to the pumping power required to provide such level of cooling, while maintaining a maximum surface temperature rise of 60K. Higher heat fluxes require higher flow rates, reducing the COP due to the larger pumping power required. Figure 3f benchmarks the evaluated devices, along with other technologies found in the literature. For SPMC, channel widths of 100 µm, 50 µm and 25 µm show a consecutively higher COP for higher heat fluxes, with a COP in the range between 10^2 and 10^4 and heat fluxes between 350 W/cm^2 and 800 W/cm^2. The 10x-manifold device vastly outperforms these SPMCs. At an identical COP of 5.0×10^3, the 10x-manifold can sustain heat fluxes up to 1.7 kW/cm^2 at 1.0 ml/s, compared to 400 W/cm^2, 450 W/cm^2 and 550 W/cm^2 for 100 µm, 50 µm and 25 µm SPMCs, respectively. Furthermore, at a heat flux of 780 W/cm^2, the 10x-manifold provides a 50-fold increase in COP with respect to 25 µm SPMCs. Compared to MMC heat sinks presented in the literature, the proposed mMMC device outperforms the current state-of-the-art, and demonstrates a significant potential for energy-efficient cooling by having a thermal-centered approach in the device design.

Power IC with embedded cooling

The lateral nature of AlGaN/GaN electronics enables the monolithic integration of multiple power devices onto a single substrate. This opens a new horizon for power electronics, where

an entire converter can be integrated on a small chip, opening a large potential for energy, cost and space savings. However, the resulting high heat-fluxes limit the maximum output power of the chip. To demonstrate the potential of embedded cooling in a semiconductor device, we monolithically-integrated a full-bridge rectifier on a single GaN-on-Si die. Rectification was provided using four high-performance tri-anode Schottky barrier diodes (SBDs) with a breakdown voltage of 1.2 kV and high-frequency capability up to 5 MHz [46]. 50 µm-wide cooling channels were integrated on the silicon substrate (Fig. 4a). To fully benefit from the compactness of high-performance microchannel cooling, a novel 3-layer PCB with embedded coolant delivery channels was developed, used to guide the coolant to the device (Fig. 4b). The full fabrication of this monolithically-integrated power device and the PCB is described in the Methods, as well as shown in extended data Fig. 8. The device was finally fluidically connected to the PCB using laser-cut liquid- and solvent-resistant double-sided adhesive, providing a leak-tight connection. This method is low-cost and easy-to-prototype, but translates well to conventional solder bonding. Figures 4c,d show the converter implemented, with a very compact form factor, rectifying an AC signal with peak voltage/current of 150 V/1.2 A (Fig. 4e). Integrated liquid cooling led to a small temperature rise of 0.34 K per Watt of output power. For a maximum temperature rise of 60 K, this single die can thus produce an output power of 176 W at a flow rate of only 0.8 ml/s. Furthermore, the reduced operating temperature led to an increased conversion efficiency (Fig. 4f) by eliminating self-heating degradation from the electrical performance. The AC-DC converter was experimentally evaluated up to 120 W of output power, while the temperature rise stayed below 50 K (Fig. 4g). Considering the small converter volume (4.8 cm^3), this corresponds to an ultra-high power-density of 25 kW/dm^3. Moreover, since all cooling occurs within its footprint, multiple devices can be densely packed on the same PCB to increase the output power. This is a clear benefit over conventional heat sinks relying on heat spreading to large areas. These results show that the proposed high-performance cooling approach can enable the realization of high-power (kW-range) converters of the size of USB-sticks in a foreseeable future.

Discussion and outlook

In this work, a new approach of co-designing microfluidics and electronics for energy-efficient cooling was presented, and demonstrated on GaN-on-Si power devices by turning the passive silicon substrate from a low-cost carrier into a high-performance heat sink. COP values above 10^4 for heat fluxes surpassing 1 kW/cm^2 could be obtained by focusing on cooling in an early stage of the device design. As a practical implication, the average added-energy expenditure of 34% for cooling in data centers could potentially drop below 0.01% by adopting this design approach. The entire mMMC cooling structure can be monolithically integrated in the substrate, requiring only conventional fabrication procedures, thus making this economically viable. To materialize this concept, new solutions in packaging and interconnects are required. The presented PCB-based fluid delivery provides an example of a strategy to use these co-designed chips, based on components familiar to the electronics designer. This consequently means that, in order to provide maximum energy savings, cooling should be an integral step in the entire electronic design chain, from the device to the PCB design, and not merely an afterthought. If these practicalities can be addressed, the co-design of microfluidic and electronics has the possibility to become a new paradigm in energy-efficient thermally-aware design of electronics. This may aid in solving critical challenges in electronics applications, as well as enabling future integrated power converters on a chip to support the electrification of our society in a sustainable manner.

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Author contributions:

R.v.E. and E.M. conceived the project. R.v.E., R.S. and L.N. developed and optimized device fabrication processes. R.v.E. and L.N. fabricated the devices. R.v.E. designed and developed the experimental setup to study cooling performance. G.K. designed the circuits for evaluating the fabricated devices. R.v.E. and G.K. designed and performed the experiments. R.v.E. analysed the data. E.M. supervised the project. R.v.E. and E.M. wrote the manuscript with input from all authors.

Competing interests: The authors declare no competing interests.

Figures

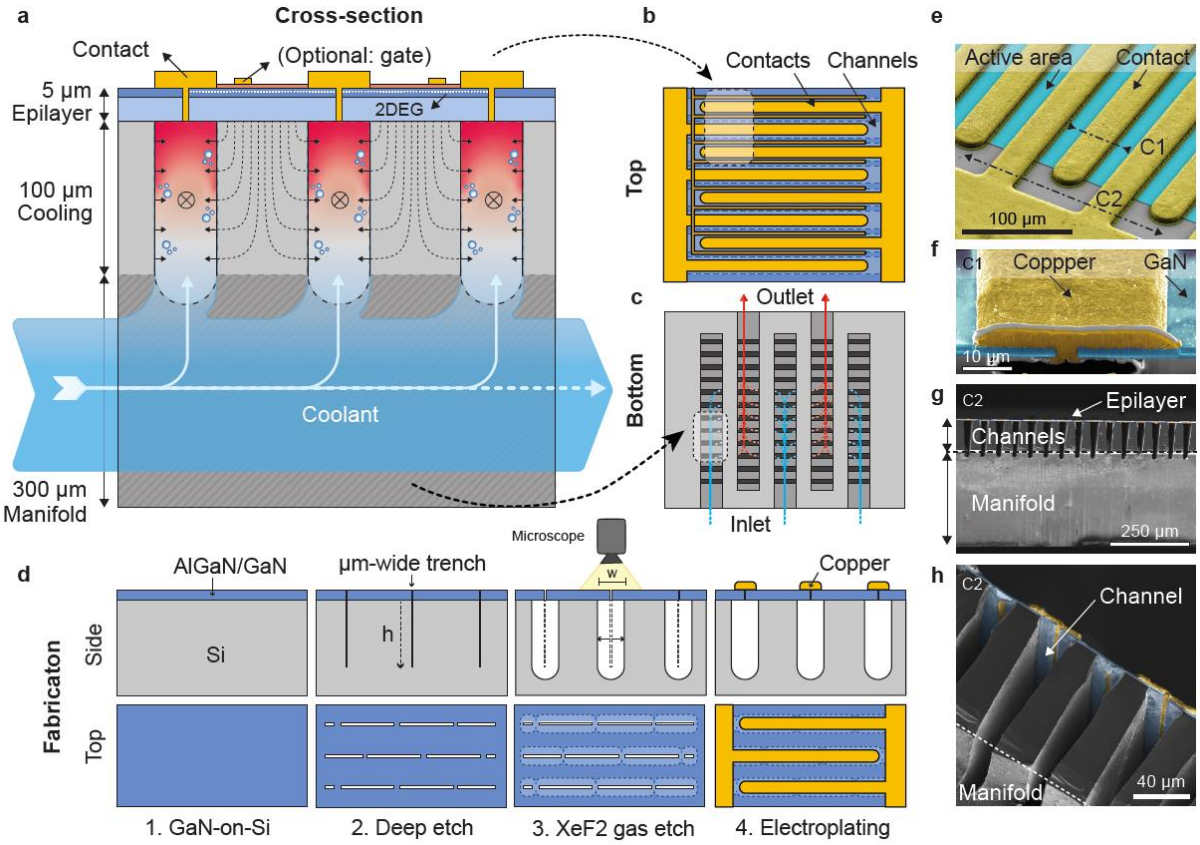

Fig. 1 | Co-designed microfluidically-cooled electric device. a, Schematic of the device structure, where the AlGaN/GaN epilayer provides the electronic functions, and the silicon functions as cooling and fluid distribution manifold. Metal contacts seal the buried microchannels embedded underneath. Coolant coming from the manifolds flows in the out-of-plane orientation inside the microchannels to remove the heat away from the device. **b,** Top-view of the co-designed device structure: each contact is aligned and sealing the buried channel in a scaled-up multi-finger structure. **c**, Bottom-view, showing the manifold structure that distributes the flow over the microchannels. **d**, Summary of the proposed cooling method: A staggered pattern of narrow high aspect-ratio slits is first etched through the AlGaN/GaN epilayer into the silicon. Next, an isotropic gas etch widens the channels in silicon, coalescing under the epilayer. The openings in the epilayer are then sealed using electroplating. **e,** Scanning electron microscopy (SEM) image of the AlGaN/GaN surface after sealing the microchannels. Contact pads hermetically seal the incisions in the AlGaN/GaN epilayer. **f,** Cross sectional SEM image along C1, showing the incision in the epilayer sealed with electroplated copper. **g,** Cross-sectional SEM image along C2, showing an array of buried microchannels, as well as a sidewall of the perpendicular manifold channel. **h,** Close-up of the cross section image along C2, showing the exposed microchannel below the electroplated-copper sealing-layer.

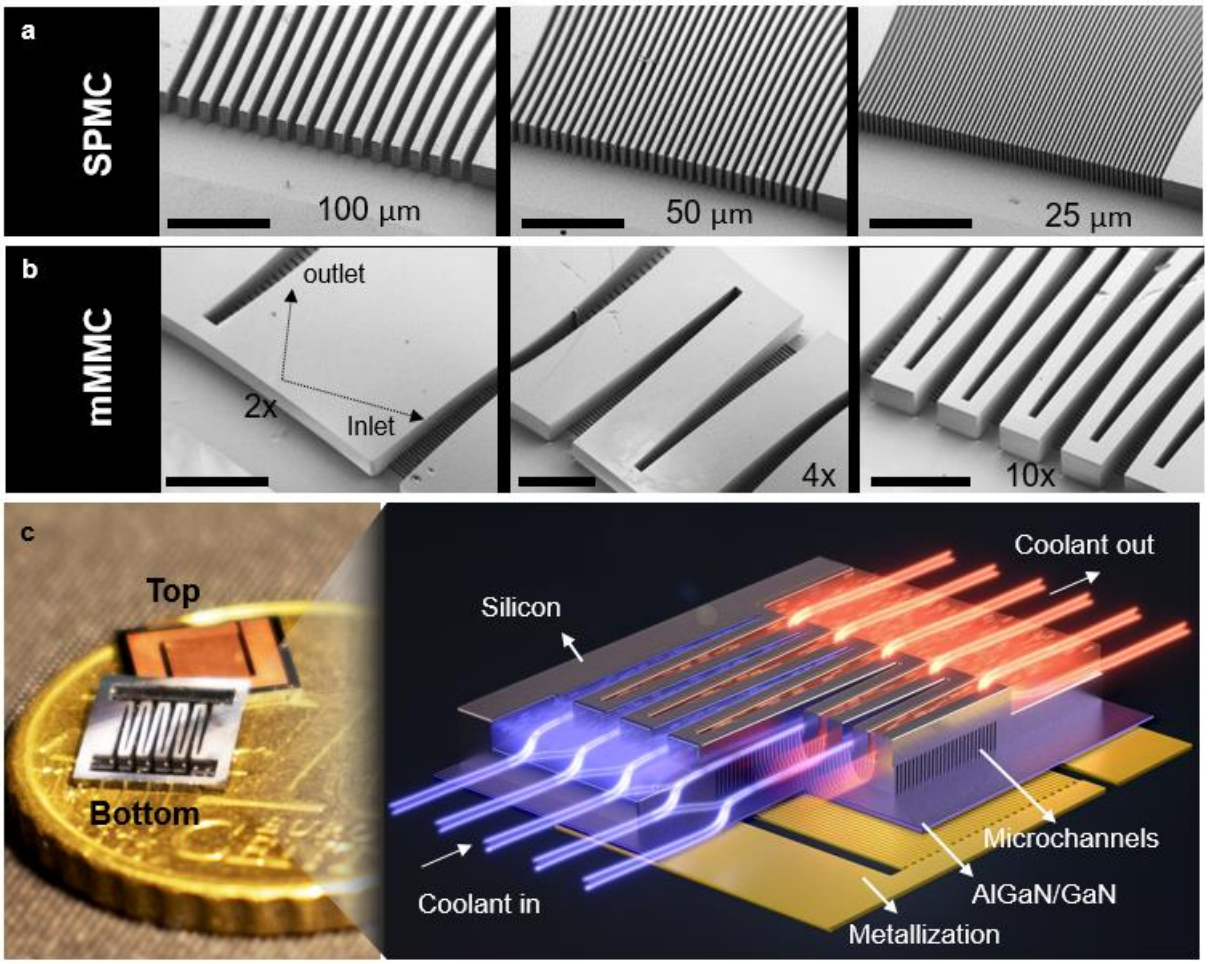

Fig. 2 | Microchannel cooling configurations. a, SEM images of the backside of the silicon substrate with SPMCs. Microchannel widths are 100 µm, 50 µm and 25 µm and the scale bars represent 1 mm. **b,** SEM images of backside of the silicon substrate with mMMCs, with 2x, 4x and 10x-manifold sections. Scale bars represent 850 µm. **c,** Picture of the co-designed devices, from the top and bottom sides, with 10x-manifold mMMC cooling. Top-side shows the electronic structure and the bottom shows the manifold etched in the silicon substrate. **d,** Illustration of the fluid flow through the mMMC structure. Blue lines indicate the cold coolant flow entering the chip, and red lines indicate the hot coolant leaving the chip.

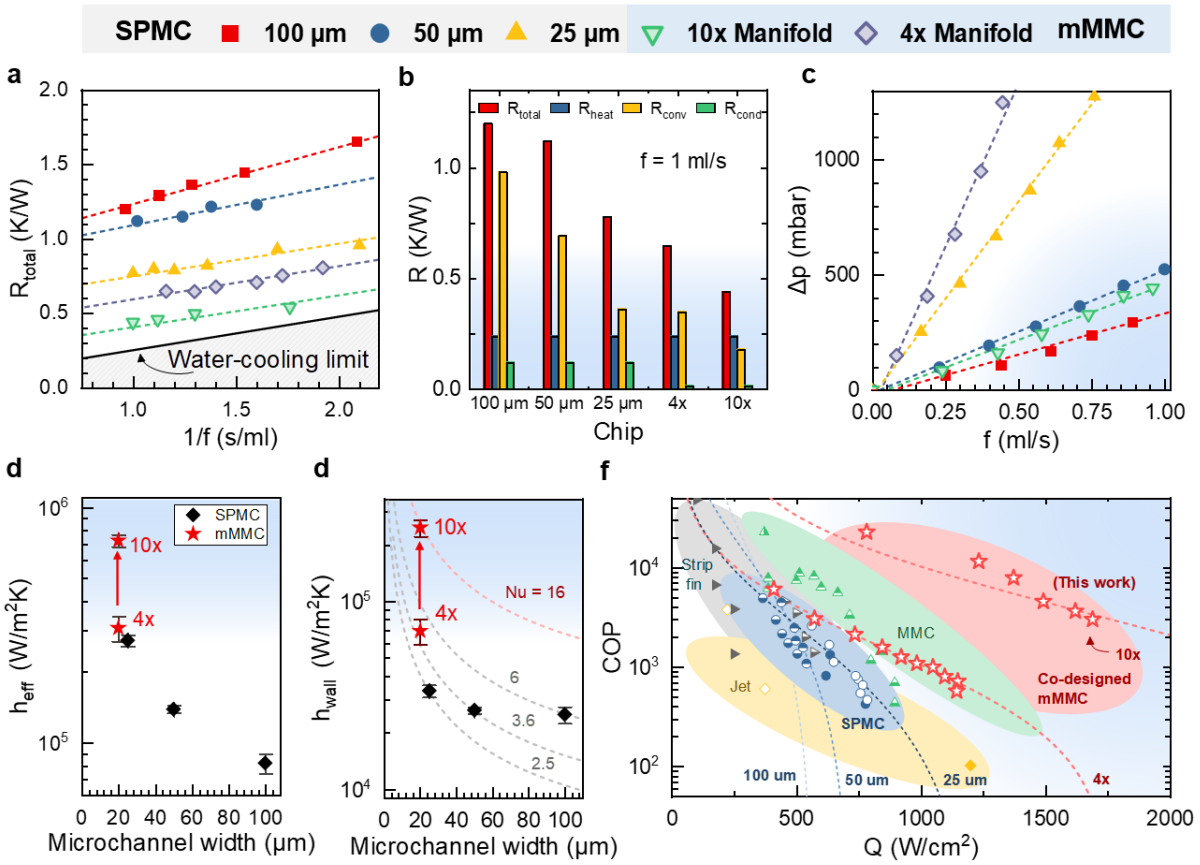

Fig. 3. | Thermo-hydraulic evaluation of the cooling strategies. a, Total thermal resistance between the surface temperature and the inlet temperature of the coolant. The black line indicates the lower limit of thermal resistance for single-phase water cooling, determined by its heat capacity. **b,** Breakdown of the contributions of R_{total}, into R_{heat}, R_{conv} and R_{cond}, for all evaluated devices. **c,** Pressure drop versus flow rate for the considered microchannel structures. The 4x- and 10x-manifold had 20 µm-wide channels. **d,** Effective (base-area averaged) heat-transfer coefficient for straight (SPMC) and manifold (mMMC) structures. **e,** Wall-averaged heat-transfer coefficient for straight and manifold microchannels. A 4.4-time increase in Nusselt number was observed between the 4x- and 10x-manifold. **f,** Benchmark of the experimentally-demonstrated coefficient of performance (COP) versus the maximum heat flux for a temperature rise of 60 K. SPMC (blue) MMC (Green), Impinging jet (Yellow), strip-fin (grey) and mMMC (red) and are shown. More extensive benchmarking with simulation/analytical results, full references and further classification is provided in Extended Data Fig. 6. And Extended Data Table 2. A significant improvement in COP for a given heat flux is achieved with our proposed mMMC structures (red). Dashed lines are models for COP vs heat flux, under the assumption of a constant heat transfer coefficient and a linear pressure-flowrate relation, fitted through the experimental data.

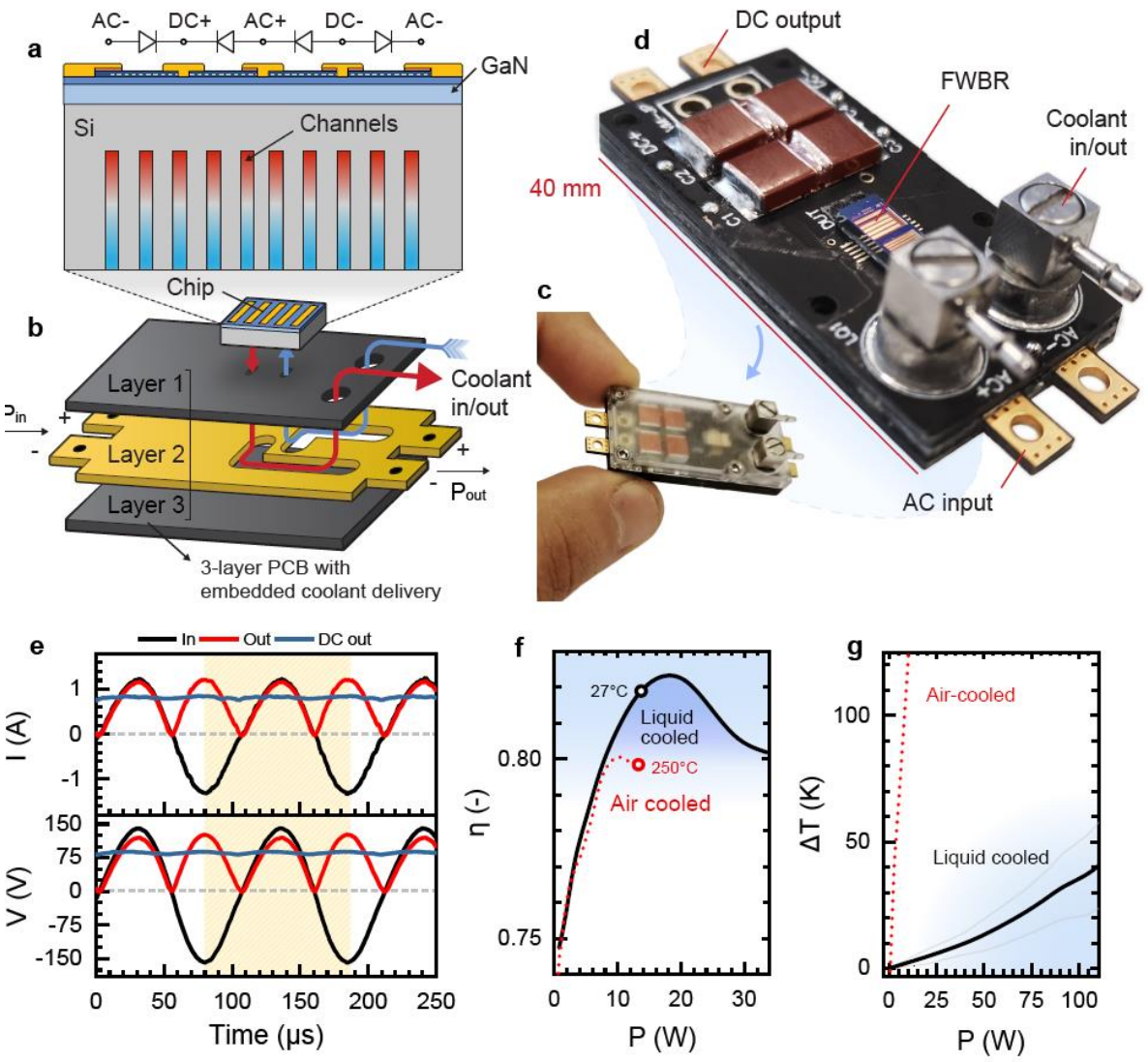

Fig. 4. | AC-DC Converter with embedded liquid cooled GaN power IC. a, Schematic illustration of the super-compact liquid-cooled power IC based on four GaN power SBDs integrated in a single chip in a full-bridge configuration. **b,** A PCB-embedded coolant delivery was developed to feed the coolant to the device. The PCB consists of 3 layers, where the middle layer contains a fluid distribution channel. **c,** Picture of the full 120 W AC-DC converter with coolant delivery to the liquid-cooled power IC. **d,** Converter without encapsulation, revealing the monolithically-integrated Full-Wave Bridge-Rectifier (FWBR) IC. **e,** Converter 150 V AC input (black) and output before (red) and after (blue) filtering using output capacitors. **f,** Efficiency versus output power for the air-cooled and liquid-cooled AC-DC converter. At identical output power, the liquid cooled converter exhibits significantly higher efficiency due to elimination of self-heating degradation. **g,** Temperature rise versus output power, showing a significantly higher temperature at equal output power for the air-cooled device compared to the embedded liquid cooling, which causes a large self-heating degradation.

METHODS

Device fabrication process. The fabrication process of the co-designed microfluidic-electronic device is shown in Extended Data Fig 1. Fabrication started with an AlGaN/GaN-on-silicon wafer with, from top to bottom: 2.9 nm GaN cap-layer, 20 nm AlGaN barrier, 420 nm GaN channel, 4.2 µm buffer layer, on a 400 µm-thick silicon. First, a mesa was etched to define the active area of the chip, followed by a 1 µm-thick plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 as an etching mask to obtain sharp sidewalls after GaN etching. Photoresist was lithographically patterned on top of the SiO2 layer, to define and open a staggered pattern of slits in the SiO_2 mask using inductively coupled plasma (ICP) etching using C_4F_8 chemistry. The staggered pattern, with 30 µm-long slits spaced 2 µm apart, prevented the epilayer from turning into a fragile cantilever after performing an undercut in the silicon substrate. Instead, the 2 µm spacing between each slit kept the epilayer together, resulting in good mechanical integrity of the epilayer during the fabrication process. The photoresist was stripped using an O_2 plasma and the exposed GaN slits were consecutively etched using Cl_2+Ar chemistry until the silicon substrate was reached, which was confirmed using end-point detection. The chips were then dipped into 40% KOH at 60ºC for 5 minutes to remove any remaining AlN-based material from the buffer [47], [48]. The Bosch process was used to etch the silicon slits for approximately 115 µm deep, resulting in high aspect ratio slits. The microchannels in silicon were widened using an isotropic XeF_2 gas etch, which provided selectivity over GaN [49]. XeF_2 gas etching was performed in a pulsed manner: The sample was exposed to XeF_2 at a controlled pressure (1.33 mbar) for 30 seconds, followed by evacuation of the etching chamber. This process was repeated for 45 cycles until the desired channel width was obtained. In-situ optical etching tracking through the transparent GaN membrane was performed using a camera directly mounted on the etching chamber, as shown in Extended Data Fig. 1. This method enabled to accurately obtain the desired channel width, and to ensure that all slits were coalesced into continuous channels underneath the epilayer. This way, 20-µm wide microchannels were etched through the narrow openings in the epilayer. Next, the SiO_2 hard mask was stripped using 50% HF for 10 minutes, and the surface was

further cleaned from all organic residues using piranha treatment. A Ti/Al/Ti/Ni/Au Ohmic contact stack was deposited using e-beam evaporation and photolithographically patterned by lift-off, followed by an annealing step at 850 ºC. The in- and outlet channels were etched in the backside of the chip using the Bosch process, until the channels from both sides coalesced, which was confirmed by optical microscopy. The slits in the GaN epilayer were then sealed by electroplating approximately 7 μm of copper on top of the Ohmic contacts. For the electroplating process, a uniform seed layer of chromium-copper (20nm/70nm) was deposited on top of the device after the contact metallization step using e-beam evaporation, where chromium served as an adhesion layer and copper as the seed layer. Next, 10 μm of photoresist was patterned to define the area to be electroplated. Electrical contact was made to the chip, which functions as cathode, using electrically conductive adhesive that was applied over all edges of the chip. First, the chip was shortly dipped in H_2SO_4 to remove any surface oxidation. Then, electroplating was performed using a galvanostat at 1 A for 7 min minutes in a solution containing $CuSO_4$, H_2SO_4 and Cl^-, as well as an addition of Intervia 8510 (Dow), while using a CuP anode. As the galvanically deposited copper film grows conformally and isotropically, the incisions in the GaN layer seal as the copper layer bridges the gap and coalesces on top of the cavity. After electroplating, the photoresist was stripped, and the seed layer was etched by performing a short copper wet-etch ($(NH_4)_2S_2O_8$ + H_2SO_4), followed by a chromium etch that is selective over copper ($KMnO_4$ + Na_3PO_4). Finally, the individual dies were separated using a dicing saw. The video in the Supplementary Information illustrates the flow-path of the coolant through this mMMC heat sink structure.

Experimental setup for evaluation of cooling performance. An open loop single-phase liquid cooling setup, schematically shown in Extended Data Figure 2a was built underneath an IR camera in order to perform liquid cooling experiments, as can be seen in Extended Data Figure 2b. A reservoir of deionized (DI) water was pressurized with compressed air using a pressure controller (Elveflow OB1 MK2), causing it to flow towards the test section manifold machined out of polyetheretherketone (PEEK) (Extended Data Figure 2c). PEEK was chosen

because of its low thermal conductivity, preventing heat flux to leak out of the system by conduction, as well as because of its high glass-transition temperature of 143 ºC [50]. The flow rate of the coolant was measured using a thermal mass flow sensor (Sensirion SLQ-QT500). Chips are mounted on laser-cut Poly(methyl methacrylate) (PMMA) carriers with double-sided adhesive and connected to the test section using laser-cut silicone gaskets. A closed seal was obtained on these gaskets using 4 screws that push down on the PMMA carriers. This way, no force needs to be applied directly on the chips, preventing the chips from breaking during mounting. Two pressure sensors (Elveflow MPS) were used to measure the pressure at the inlet and outlet of the chip, and the inlet and outlet fluid temperatures are measured using a type-K thermocouple (THERMOCAOX), integrated right before the inlet and right after the outlet of the chip. The thermocouples were calibrated using a thermostatic bath (Lauda RP855). The chips were connected to a power supply (TTI QPX1200), which simultaneously applies a voltage and measures the current over the device under test (DUT). Electrical connection with the DUT was made using 6 high-current-rated spring-loaded pins, connected to a custom-made PCB with a hole in the center to allow infrared (R) measurements. Temperature rise on the surface of the chip was measured using a FLIR SRC3000 IR camera. A LabVIEW automation program was developed to automate the data acquisition. The program waits for the liquid outlet temperature to stabilize, then sends a trigger signal to the video card of the PC connected to the IR camera to record 20 snapshots, and increases the power dissipated on the chip until a critical surface temperature was reached. The surface of the chip was painted black using spray paint to increase emissivity. To further improve the accuracy of the IR thermography, a pixel-by-pixel emissivity calibration was performed by flowing water at a controlled temperature using the thermostatic bath following the method described in [51]. IR emission was measured at each temperature and a fit between temperature and IR emission was established for each pixel of the photodetector. Finally, a MATLAB script was developed in order to automate the post-processing of the IR data, which gave the mean surface temperature rise and the maximum surface temperature rise. The latter

was defined as the mean value of the 20 highest temperature readings, to be less susceptible to noise.

Pressure test. Before evaluating the cooling performance, pressure tests were performed by increasing the system pressure of up to 4 bar (above atmospheric) on each chip. This procedure was intended as a burst test, but no failure was observed up to the maximum pressure capability of the experimental facility. It should be noted that typical epitaxial growth of AlGaN/GaN on a silicon substrate using metal-organic chemical vapor deposition is performed at temperatures around 1000 ºC. Due to the mismatch in coefficient of thermal expansion, the resulting stress in the epilayer is in typically in the order of 0.3 GPa, whereas the critical cracking stress lies around 1.1 GPa [52]. Although the additional pressure inside the channels during liquid flow does contribute to the total stress in the epilayer, 1 bar (typical operation) equals to only 0.1 MPa. This stress is more than three orders of magnitude smaller than the typical residual stress in the epilayer, and is therefore not expected to cause failure. This finding agrees with our observations, as well as with other works in the literature [53], [54].

Data reduction. The cooling performance of all chips was analyzed for power dissipations up to 75 W and flow rates between 0.1-1.1 ml/s. Extended Data Fig. 3 shows an overview of the data reduction procedure for the 10x-manifold chip to obtain the relevant values in Fig. 3. The maximum surface temperature ($\Delta T_{surface}$) rise was calculated by subtracting the coolant inlet temperature from the maximum IR-measured surface temperature (Extended Data Fig. 3a). The liquid temperature rise (ΔT_{liquid}) was calculated by subtracting the inlet water temperature from the water outlet temperature, measured by thermocouple (Extended Data Fig. 3b). The wall temperature (ΔT_{wall}) was calculated by subtracting the mean water temperature between the inlet and outlet from the average surface temperature rise, and performing a correction for 1D conduction through the epilayer, thermal boundary resistance and silicon in case of the straight channels (Extended Data Fig. 3c). A thermal boundary resistance between the GaN and silicon substrate of 1.0×10^{-7} $W^{-1} \cdot m^2 \cdot K$ was assumed [55]–[57]. The effective applied power was calculated using an energy balance ($P = \rho \cdot c_p \cdot \Delta T_{liquid}$), where ρ and c_p are the density

and heat capacity of water, respectively. For all flow-rates, the total thermal resistance (R_{tot}), the caloric thermal resistance (R_{cal}) and convective thermal resistance (R_{conv}) were determined through a linear fit of the surface temperature rise (Fig. 3a), coolant temperature rise (Extended Data Fig. 4b) and wall temperature rise (Extended data fig. 4a) versus dissipated power, respectively. Thus, every point in Extended Data Fig. 3d was derived from a wide range of measurements to ensure a high accuracy. This figure was plotted against the inverse flow rate to highlight the linear relationship between R_{cal} and f^{-1}. As can be seen, most of the variation of R_{tot} with flow-rate can be accounted to $R_{cal,}$ whereas R_{conv} shows little dependence on the flow-rate. COP was calculated by dividing the maximum heat flux for a ΔT_{max} of 60 degrees temperature rise by the required pumping power (P_{pump}) to achieve this level of cooling [58] ($COP = \Delta T_{max}/P_{pump} \cdot R_{tot}$), where pumping power was calculated as the product of flow rate and pumping power ($P_{pump} = f \cdot \Delta p$). Effective base-area averaged heat transfer coefficient was calculated using $h = (R_{conv} \cdot A_{device})^{-1}$, where A_{die} represents the footprint area of the active area of the device, containing both the electric device and the cooling structure. Average local heat transfer coefficient (h_{wall}) was determined by taking the fin efficiency (η) into account, which was calculated using $\eta = 1$ as a starting point for iteratively solving [59], [60]

$$\eta = \frac{tanh\left(z\sqrt{\frac{2h_{wall}}{k_{si}w_w}}\right)}{z\sqrt{\frac{2h_{wall}}{k_{si}w_w}}}.$$

Here, z represents the channel depth, w_w the channel wall width and k_{si} is the thermal conductivity of the silicon substrate, which was chosen to be 150 W/m-K. Finally, based on h_{wall}, the average Nusselt number (Nu) was calculated for each measurement condition using $Nu = h_{wall} \cdot D_h/k_{water}$, where D_h is the hydraulic diameter of the channel ($D_h = (2 \cdot w_c \cdot z)/(w_c + z)$) and k_{water} the thermal conductivity of water at the mean measured temperature. Extended Data Fig. 5 shows a complete overview of the remaining datasets for temperature rise and thermal resistance of the 25 μm/50 μm/100 μm-SPMC and 4x-mMMC, and the full overview of the design parameters and derived values is presented in Extended Data Table 1. Extended data

Fig. 3e shows the Nusselt number and fin efficiency over the measured range of flow speeds, and Extended Data Fig. 3f shows both the effective base-area averaged and average local heat transfer coefficients. In thermally-developing laminar internal flow, the observed average Nusselt number is expected to increase with flow rate, due to the increased entrance length. At higher flow rates, a longer entrance length will result in a higher heat transfer coefficient. This general trend is observed in Extended Data Fig. 4(d). For the 10x manifold, this effect saturates, likely due to the short length of the channels, which in combination with a potential shift in coolant distribution over the chip at higher Reynolds number, causes the Nusselt number to peak. A complete overview of the fin efficiencies and Nusselt numbers for all devices can be found in Extended Data Fig. 4c-d. Extended Data Fig. 5 shows the additional thermo-hydraulic analysis on all evaluated devices used for deriving their cooling performance. Extended Data Table 1 summarizes all dimensions and cooling performance of the chips. The performance of the mMMC chips, as well as the SMPC chips evaluated in this work were benchmarked against a wide range of works in the literature that use water as a coolant (Extended Data Fig. 6). The cooling approaches were classified as SPMC ([19], [61]), Pin-fins ([61], [62]), Strip-fins ([61], [63], [64]), MMC ([29], [65]–[68][69]), Impinging jet ([37], [61], [70]–[72]), and mMMC (This work). A distinction was made between: techniques where the water is in direct contact with the die and the die contains cooling structures (embedded cooling), approaches where the water is in direct with the die, but the die itself does not contain cooling structures (bare-die cooling), and indirect cooling, which requires an additional thermal interface between the heat sink and the chip. A tabulated file with all data points used in the benchmarking study can be found in the supplementary data.

Impact of hydrostatic pressure on electrical performance. Due to the piezoelectric properties of GaN, changes in pressure and the resulting strain in the epilayer may affect the electrical performance of the device [53], [73]. In order to investigate this phenomena, the outlet of the test section in Extended Data Fig. 2 was plugged. The hydrostatic pressure applied to the test section was swept from 0 mbar to 1590 mbar and back. At each step in pressure, a

cyclic IV-measurement was performed, together with the measurement of the water temperature in the test section. After the water reached ambient temperature, the next measurement was performed. This was done to prevent any drift in temperature during the 3-hour-long measurement, which might affect the resistance of the chip. The 14 IV-characteristics (Extended Data Fig. 7a) show no clear impact on device performance. Next, the on-resistance was derived from the IV curves using a linear fit at each pressure condition. The observed variation in on-resistance remained within 1.5% of its initial value at atmospheric pressure (Extended Data Fig. 7b). These results show that the effect of the pressure range considered here on the electrical properties of the devices is negligible for the purpose of this work. The reason for the small impact of this effect on electrical performance could be accounted to the fact that the microchannels are positioned below the pads, and covered with metal. Any change in carrier density in this region of the chip due to strain would not significantly affect the device performance, as most contribution to the device's resistance is in the area between the pads.

AC-DC converter fabrication. Tri-anode SBD full-wave bridge rectifiers (FWBR) were fabricated on an AlGaN/GaN-on-silicon wafer with, from top to bottom: a 2.9nm GaN cap layer, 20 nm AlGaN barrier, 420 nm GaN channel and a 4.2 µm buffer layer on a 400 µm-thick silicon substrate. Tri-anode/tri-gate regions were first defined using e-beam lithography with a width and spacing of 200 nm, followed by a 200 nm-deep inductively coupled plasma etch following the process previously described in [46]. These dimensions have been shown to result in high breakdown voltage and excellent on-state performance [74]. After Ohmic metal deposition for the cathode contacts, 20 nm-thick SiO_2 was deposited by atomic layer deposition as the tri-gate dielectric, and then selectively removed in the tri-anode region. A Ni/Au metal stack was deposited on the tri-gate/tri-anode region to form the Schottky contact, as well as on the cathode. Extended Data Fig. 8d shows a SEM image of four scaled-up tri-gate SBDs forming the FWBR. The close-up SEM image shows the SBD structure. The channel length was 16.5 μm, corresponding to 1.2 kV of breakdown voltage [46]. Next, the wafer was temporarily

bonded to a carrier wafer before microchannels were etched in the backside using deep reactive ion etching to a depth of approximately 500 µm. After detaching the substrate from the carrier wafer and dicing, the individual liquid-cooled FWBR was attached to a 3-layer PCB using water-resistant adhesive with embedded coolant delivery channels. The top-layer PCB provides the electric circuit connections and the middle layer contains the coolant delivery channels (Extended Data Fig. 8a). The individual layers of the PCB were connected in an easy manner using laser cut adhesive (Extended Data Fig. 8b). Medical-grade pressure-sensitive double-sided adhesive was used from AR-Global (ARseal 90880), with water- and solvent-resistant properties as well as high temperature operation range (up to 120 ºC). A rectangular piece with inlet and outlet holes was laser-cut using a CO_2 laser. The double-sided adhesive was placed on the PCB, aligning the inlet and outlet holes of the adhesive with the PCB. Next, the chip was attached to adhesive on the PCB to create a seal. This approach emphasizes the possibility to assemble a prototype without the need of expensive machines. Alternatively, since the PCB contains a gold-plated metalized landing pad, conventional large-scale industrial processes can be utilized as well, such as (eutectic) solder bonding between a metallization layer on the backside of the chip and the PCB. Extended Data Fig. 8c shows the final assembled converter.

AC-DC converter evaluation. The cooling performance of the AC-DC converter was investigated by connecting all four SBDs in parallel, such that a uniform known DC power dissipation could be applied to the chip. For flow rates varying between 0.08 and 0.8 ml/s, the surface temperature rise was monitored increasing power dissipation up to 25 W (Extended Data Fig. 9b). The flow-rate dependent thermal resistance was derived from the slopes of surface-temperature versus power (Extended Data Fig. 9c). For each flow rate, pressure drop between the inlet and outlet was measured, and the corresponding pumping power was calculated (Extended Data Fig. 9d). Over the entire range of measured flow rates, the total pumping power stayed below 62 mW, which can be easily supplied by miniaturized piezoelectric micropumps to achieve a high system-level power density. To study the power-

conversion performance of the AC-DC converter, the device was connected to a full-bridge inverter with LC filter to supply a 100 kHz AC input, up to 200 V peak to peak. The DC output of the converter was connected to a load of 50 Ω, and flow-rate was fixed at 0.8 ml/s. Extended Data Fig. 9a shows the input AC and output DC waveforms of the converter at 70 W of transferred power. Surface temperature was monitored using an IR camera, while power was increased until a critical surface temperature rise of 60 K was observed. Following this approach, up to 120 W of output power could be delivered using this compact power converter.

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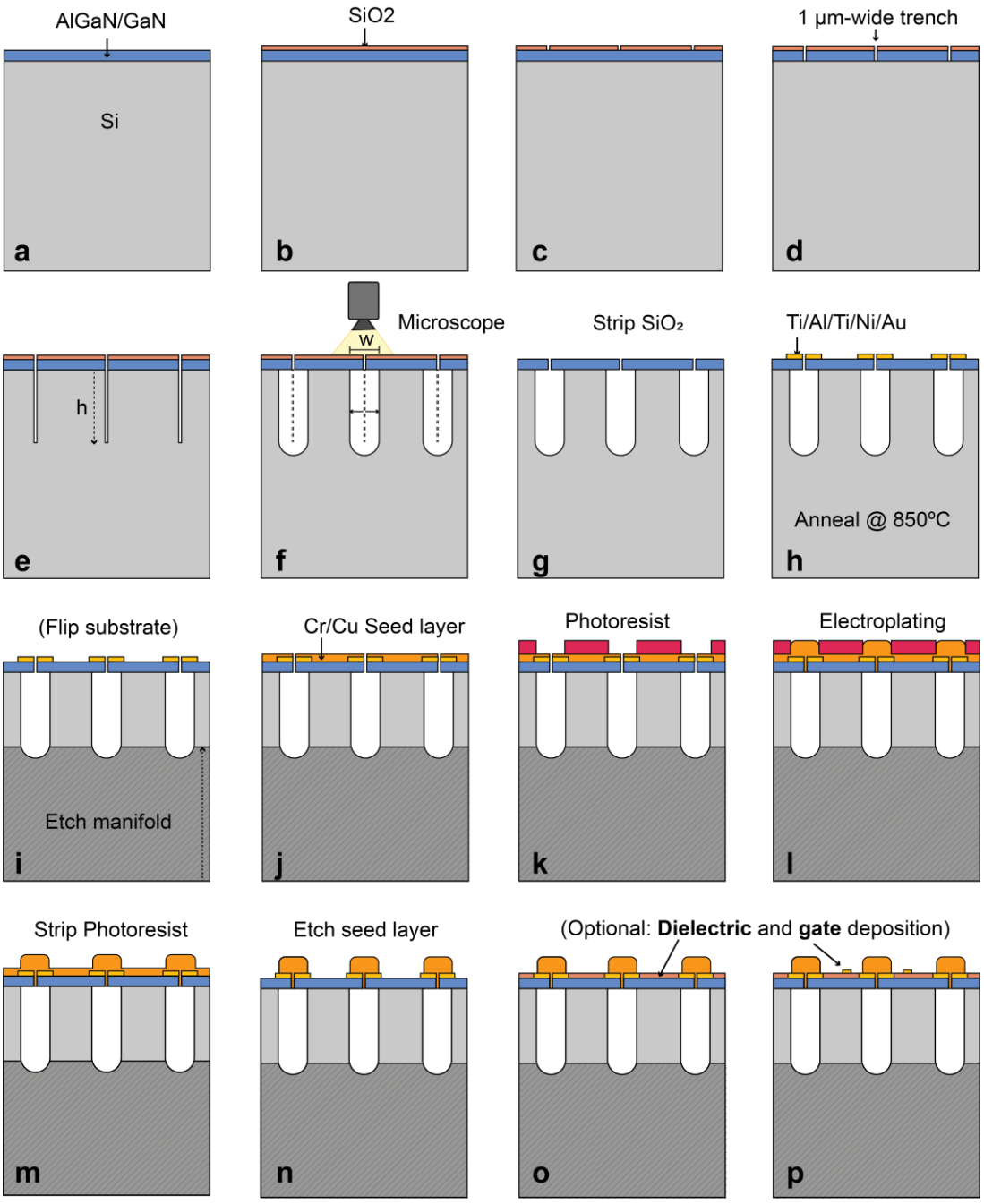
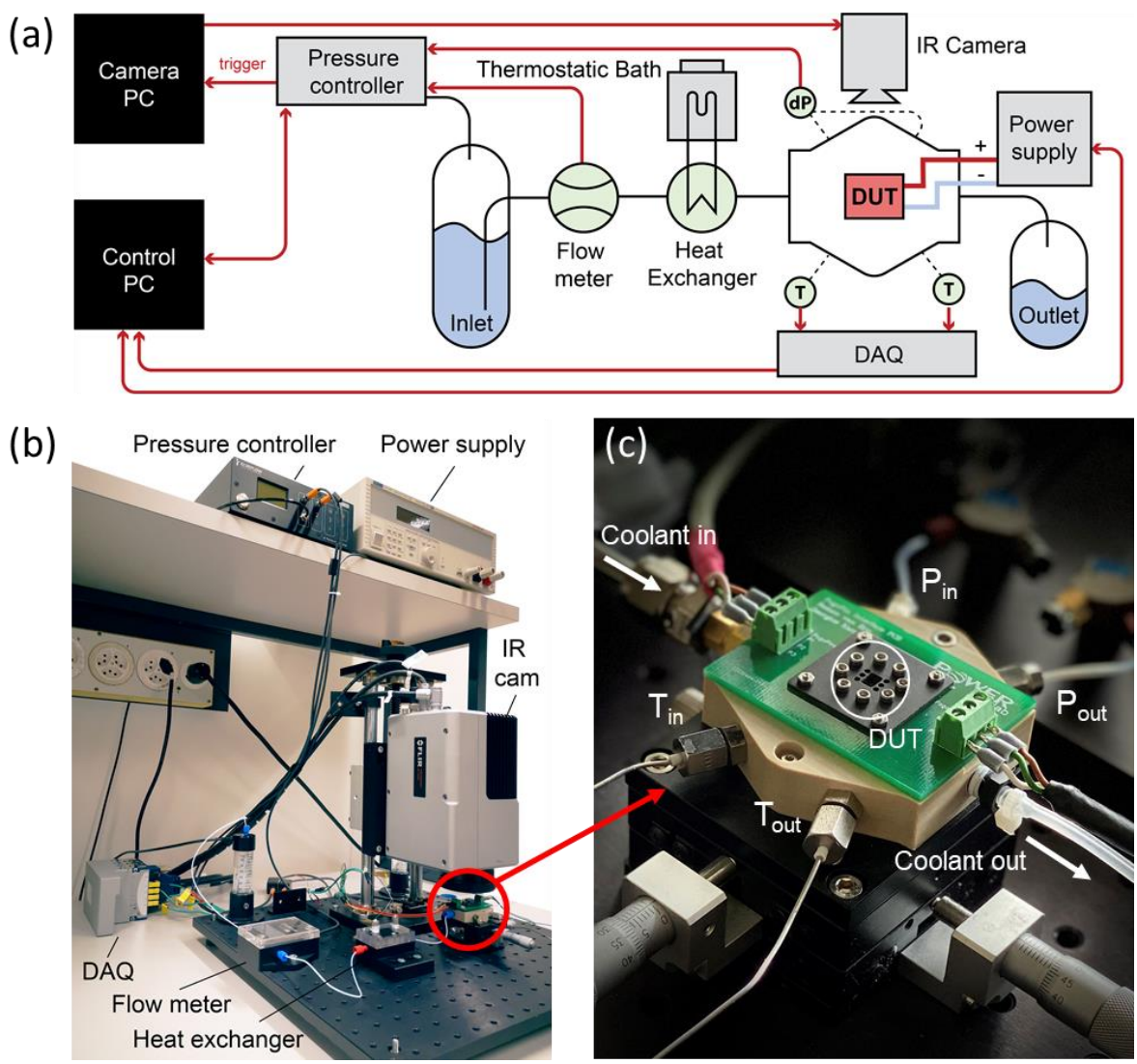
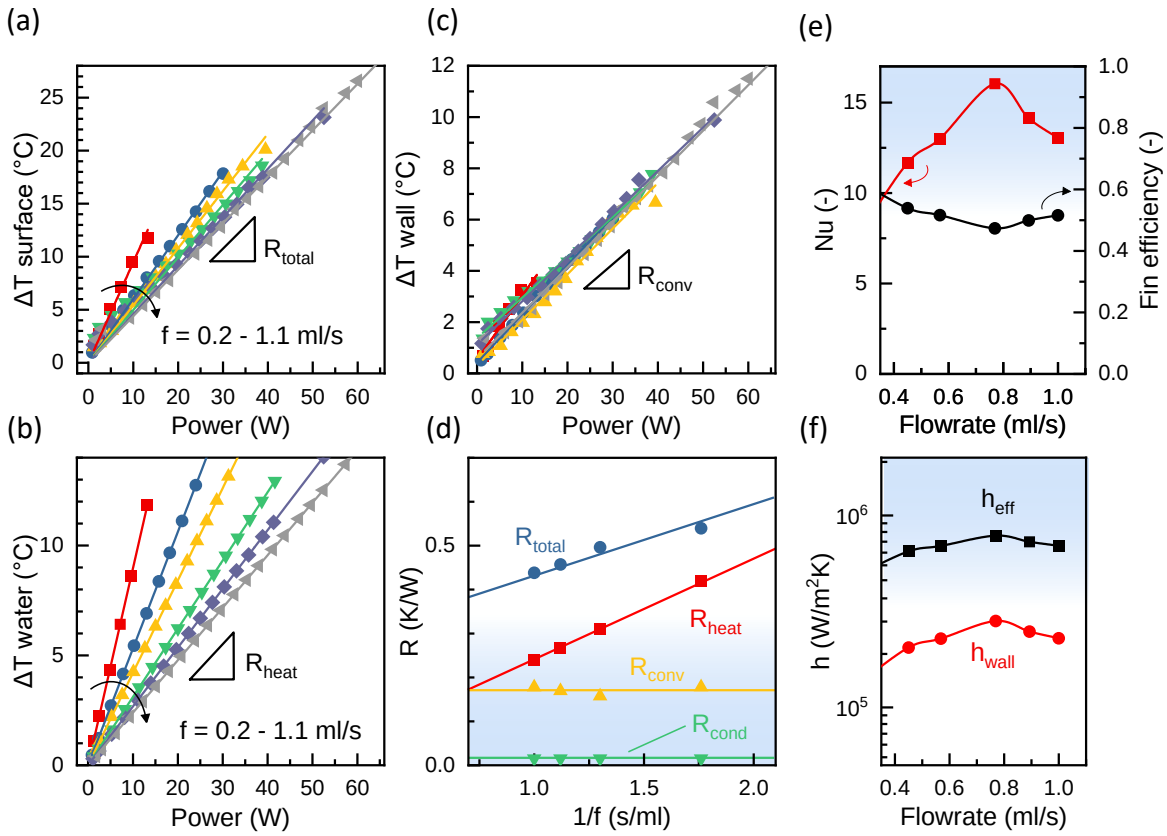
Extended data



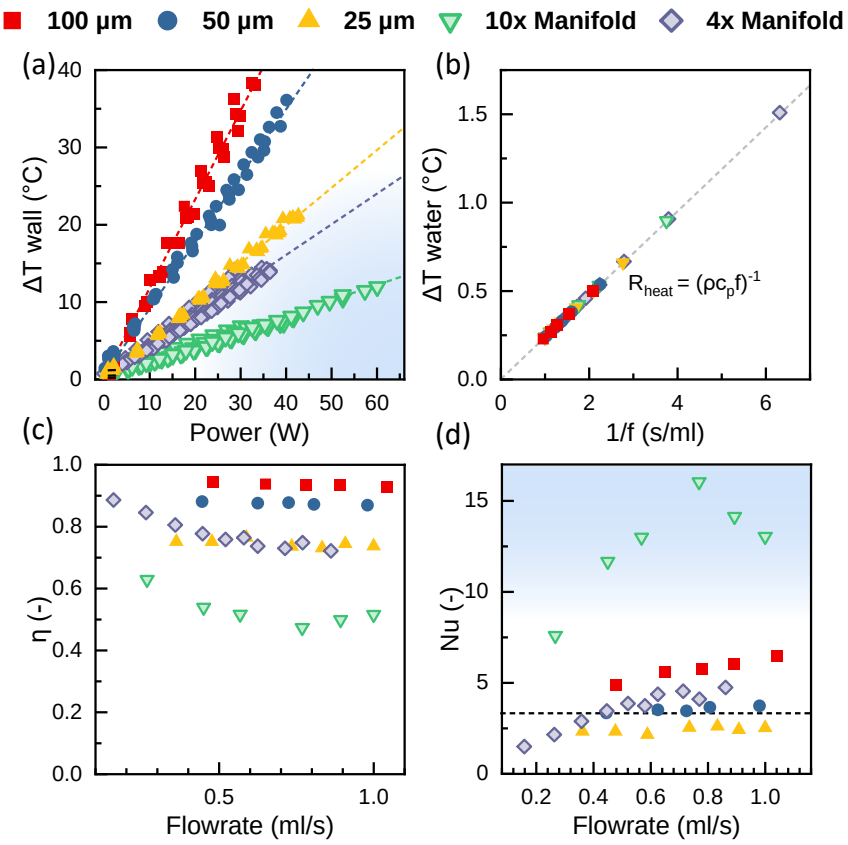
Extended Data Fig. 1 | Fabrication process of the co-designed microfluidic-electric device. a, AlGaN/GaN epilayer on a silicon substrate. **b,** hard-mask deposition. **c,** Hard mask patterning and opening. **d,** Epilayer etching until reaching the substrate. **e,** anisotropic deep etching of the silicon substrate through the epilayer opening. **f,** isotropic gas etching through the epilayer opening to widen the slits under the epilayer. An in-situ optical etching tracking was put in place to control the width of the channels. **g,** Hard-mask removal. **h,** Ohmic contact deposition and annealing, seed layer deposition for electroplating and patterning the electroplating mask. **i,** Manifolds channel etching from the back of the substrate. **j,** Cr/Cu seed layer deposition for electroplating. **k,** Lithography step to define electroplating openings. **l,** Electroplating to seal the epilayer openings. **m,** Photoresist removal. **n,** Wet etch to remove Cr/Cu seed layer. **o,** Finish device fabrication with dielectric deposition, **p,** and optional gate metal deposition.



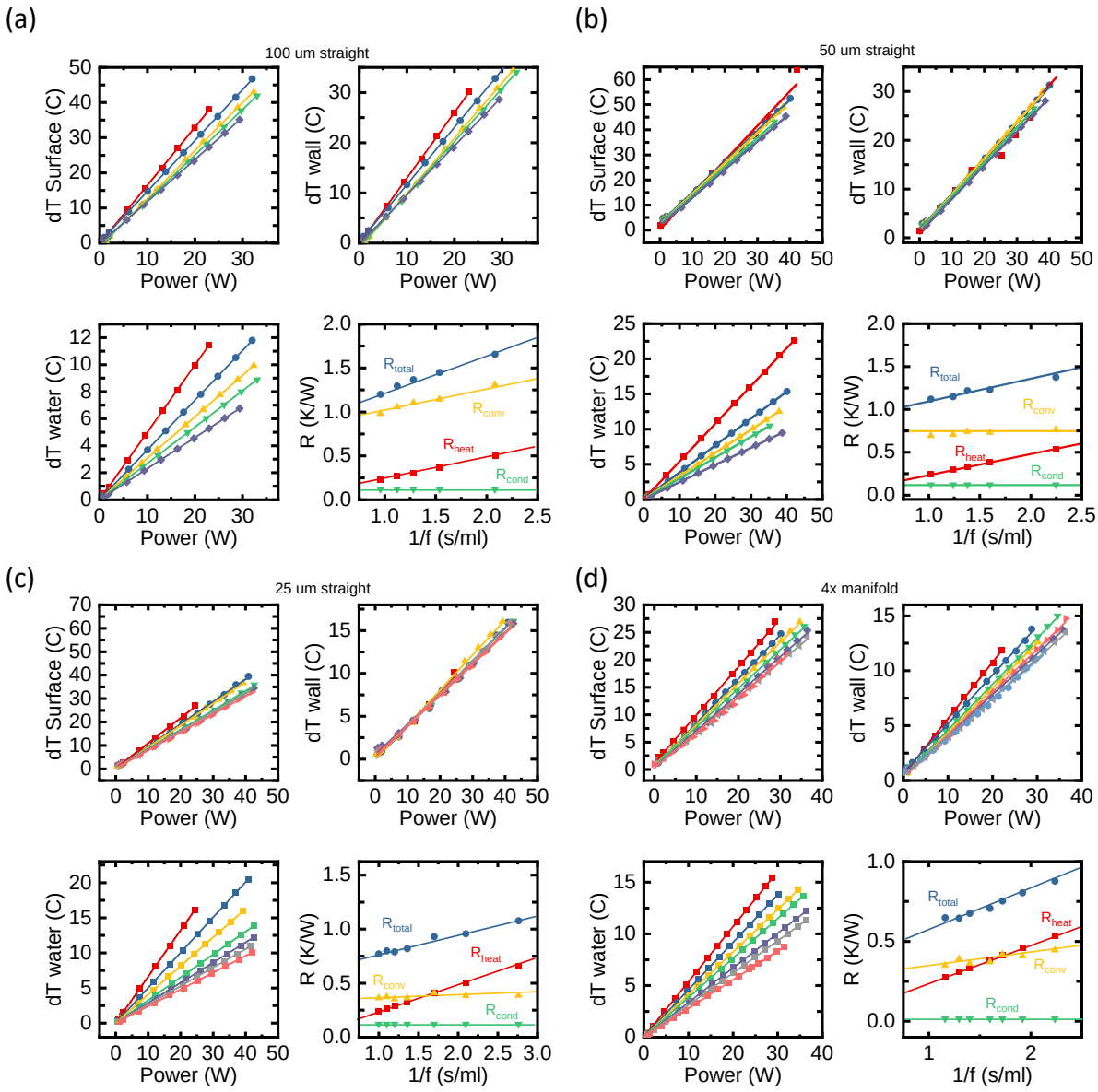
Extended Data Fig. 2 | Experimental setup for evaluating the thermo-hydraulic performance. a, Schematic overview of the measurement setup. An inlet reservoir of coolant is pressurized using a pressure controller, whereas the temperature is controlled using a thermostatic bath. Liquid flow through a flow-meter into the test section, containing the chip (DUT). Temperature of the chip is monitored using an IR camera, and coolant temperature is monitored using thermocouples (T). **b,** Picture of the experimental setup for characterizing the thermal performance. **c,** Close-up picture of the test section.



Extended Data Fig. 3 | Example data reduction of thermal characterization experiments for the 10x-manifold chip. a, Peak surface temperature rise above the inlet temperature, measured using IR-thermography at varying power dissipation. Slope of the linear fit through the data points gives the total thermal resistance (R_{tot}). **b,** Wall temperature rise. Slope through these data points gives the convective thermal resistance. **c,** Water temperature rise, measured between the inlet and outlet of the chip. Slope of the linear fit through the data points gives the contribution of the total thermal resistance due to the temperature rise of the water (R_{cal}). **d,** Total, caloric, convective and conductive thermal resistance versus the inverse flow rate. **e,** Nusselt number and fin efficiency. **f,** Effective base-area averaged heat transfer coefficient (h_{eff}) and wall-area averaged heat transfer coefficient (h_{wall}), taking the surface area of the microchannels as well as the fin efficiency into account.

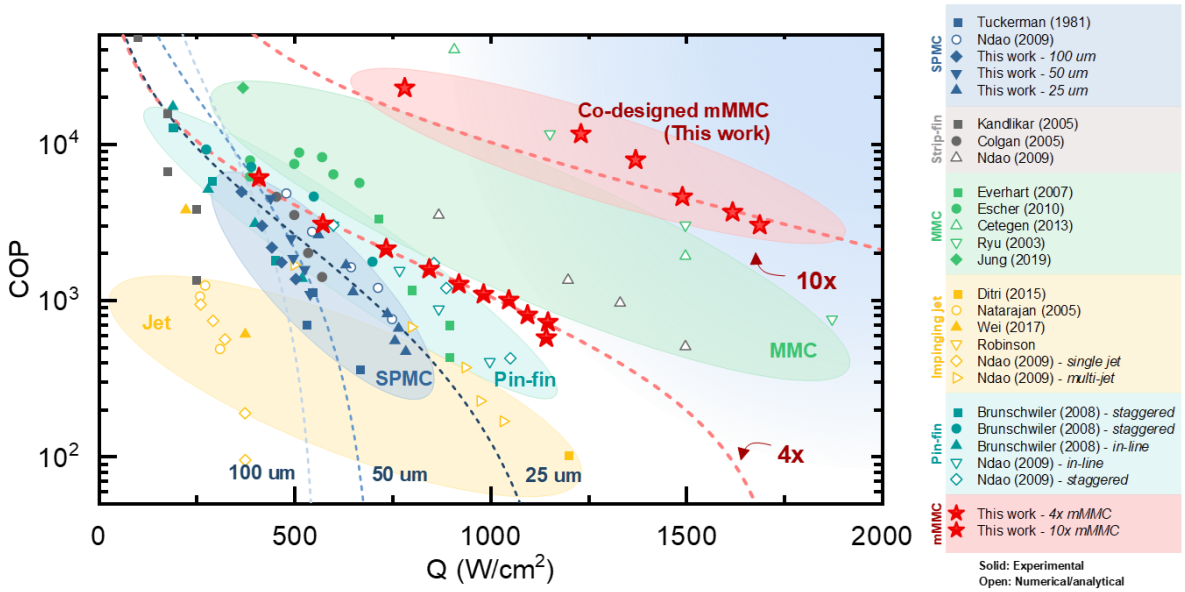


Extended Data Fig. 4 | Overview of derived values of the thermo-hydraulic analysis. a, Wall temperature for all devices. Each device shows a distinct slope in wall temperature rise versus power dissipation. **b,** Caloric thermal resistance for all evaluated flow rates, showing a clear $(\rho c_p f)^{-1}$ relationship over all devices. **c,** Fin efficiency over a range flow rates. **d**, Nusselt number versus inverse flow rate. Dashed line indicates Nu = 3.66 for fully developed internal flow.



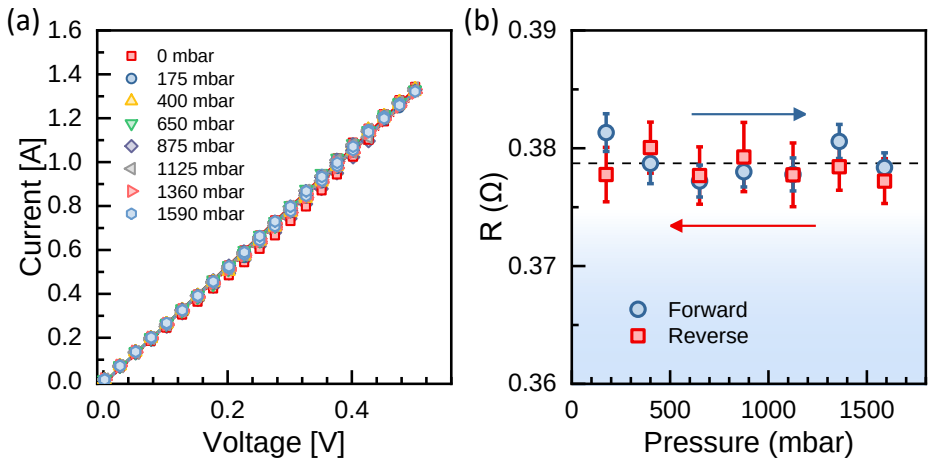
Extended Data Fig. 5 | Additional thermo-hydraulic data. Surface temperature rise, wall temperature rise, water temperature rise and thermal resistance for: **a**, 100 µm straight microchannels **b,** 50 µm straight microchannels. **c,** 25 µm straight microchannels. **d,** 4x manifold heat sink.

Extended Data Table 1 | Table of all design parameters and measured values per chip

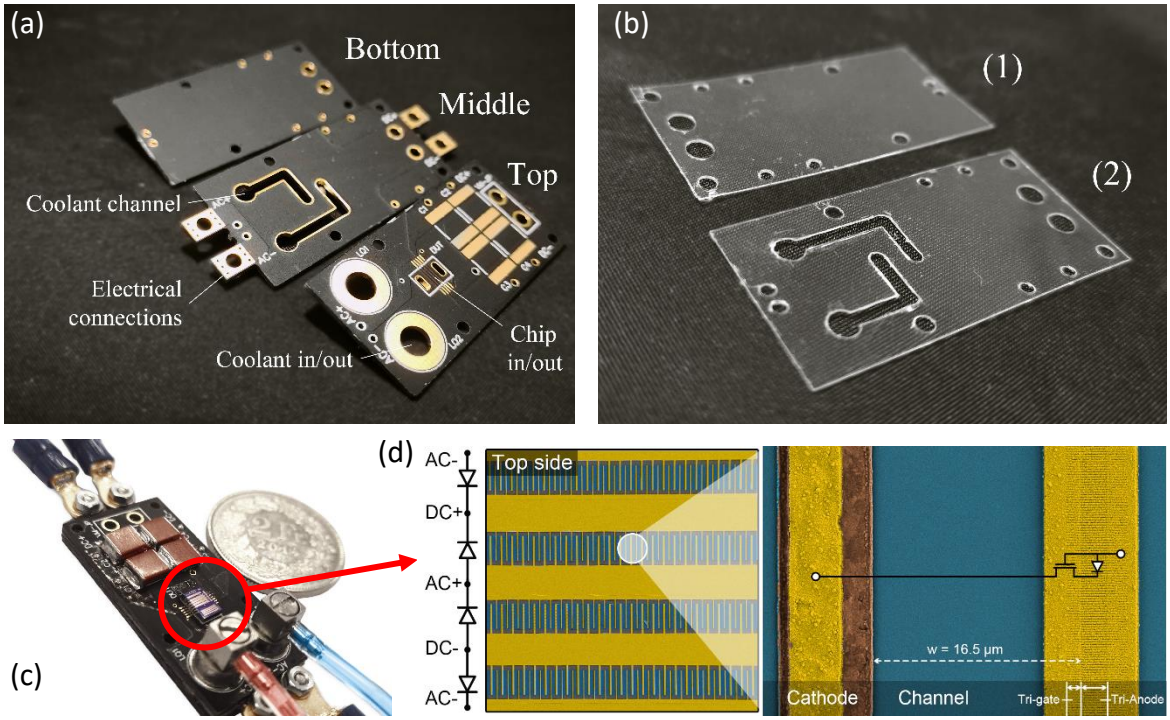


Extended Data Fig. 6 | Extensive benchmarking plot of micro-structured cooling approaches in the literature using water as a working fluid. COP versus heat flux for a maximum surface temperature rise of 60K. Solid markers indicate experimental results and open markers indicate numerical or analytical calculations. The results in this work are indicated by red stars. Dashed lines correspond to predictions based on a constant heat transfer. References to all used datasets can be found in Extended Data Table 2, and a tabulated data file with all used data is available in the supplementary data.

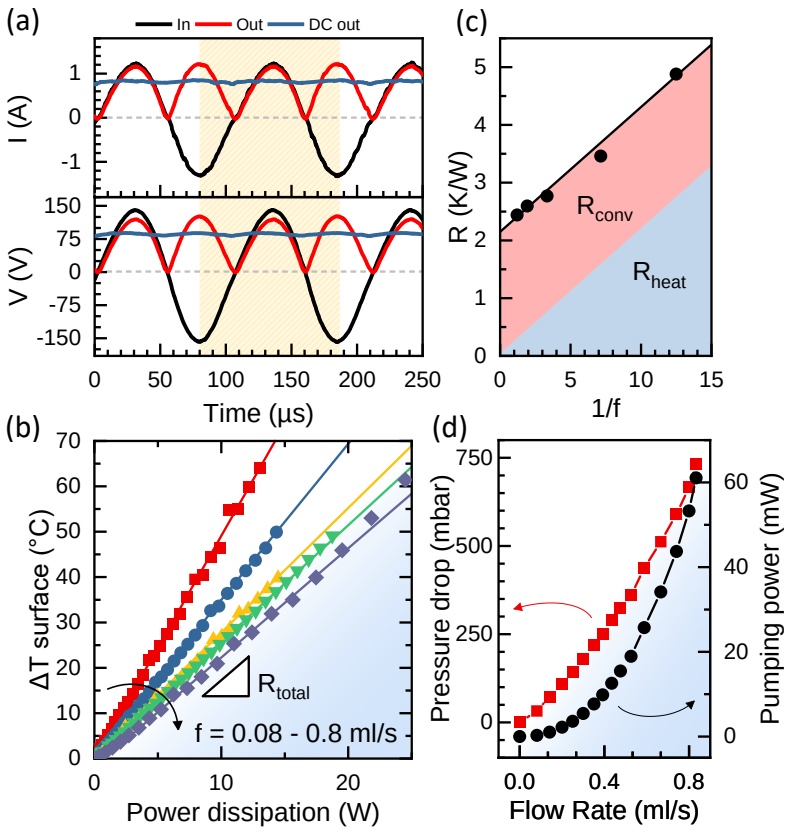
Extended Data Table 2 | Selected references for the benchmarking study in Extended Data Fig. 6



Extended Data Fig. 7 | Impact of pressure on electrical performance. a, IV characteristics at hydrostatic pressure between 0 mbar and 1590 mbar. **b**, Normalized change in R_{on} versus pressure during a sweep in pressure up to 1600 mbar and back. Each data point was extracted using a linear fit through a cyclic IV measurement from 0 V to 0.5 V and back.



Extended Data Fig. 8 | Structure of the integrated full-bridge rectifier with embedded cooling. a, Three PCBs that provide coolant delivery to the chip. **b**, Laser-cut adhesives used to bond the layers together. **c,** Converter after assembly, with electrical and fluidic connections. **d**, SEM image of the 4-diode structure, inset shows the polarity of each device and close up shows the structure of the tri-anode SBD diode.



Extended Data Fig. 9 | Operation of the ac-dc converter with embedded cooling. a, Input and output waveforms of 150 V / 1.2 A peak-to-peak rectification at 100 kHz. **b,** Surface temperature rise versus power dissipation for varying flow-rates. **c,** Thermal resistance versus inverse flow rate of the full converter. Pressure drop and pumping power versus flow-rate. **d,** Pressure drop and pumping power versus flow-rate.

Data availability statement

All data needed to evaluate the conclusions in the paper are present in the paper, in the extended data figures and in the supplementary data