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Keywords

≪Protection Device≫, ≪Marine≫, ≪DC Grid≫, ≪Solid-State≫.

Abstract

The desire to increase the voltage of DC shipboard power distribution networks to the medium voltage level derives from the pressure to reduce the operating costs of such systems by increasing their efficiency. Solid state bus-tie switches are accepted to be an essential component of such installations at the low voltage level, as they allow system reconfiguration and prevent fault propagation through ultrafast fault current identification and interruption. Nevertheless, the lack of standardisation in medium voltage DC shipboard power systems hinders the development of such technologies as custom, *ad hoc* solutions must be found according to the selected voltage level. This paper presents a solid state bus-tie switch topology that is scalable in both power and voltage rating and relies exclusively on existing, commercially available technologies. This provides a simple, readily employable solution with the flexibility needed to bridge the technological gap in the time required for medium voltage system operating voltages to become standardised. This paper presents the prototype of the bus-tie switch and validates its scalability through extensive experimental tests.

Introduction

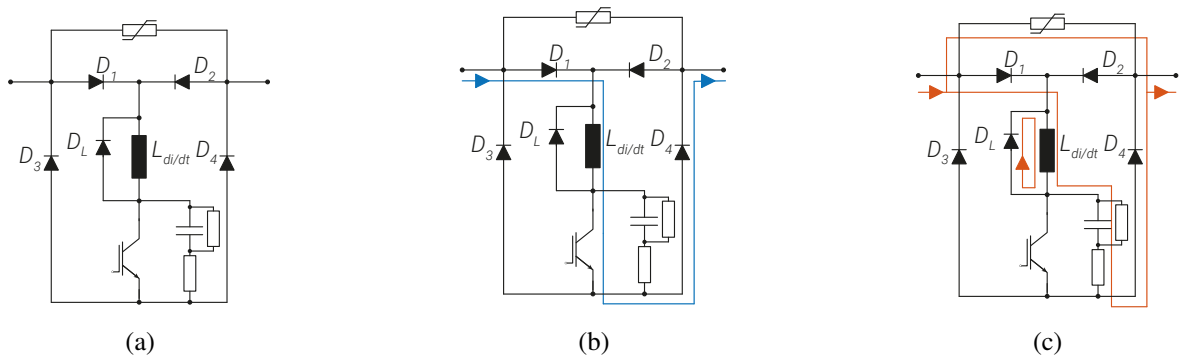
DC power distribution networks (PDNs) have been widely reported to provide increased flexibility of operation and efficiency in existing commercial applications [1, 2]. A voltage increase in such networks from the low voltage (LV) level to the medium voltage (MV) level would further increase the system efficiency, with the corresponding advantages in terms of operating costs, and enabling an increase of maximum installed power over the 20 MW - 30 MW that are generally accepted to be achievable in an LV system [3, 4, 5, 6]. Due to their safety critical role, shipboard PDNs at all voltage levels employ redundancy to avoid system-wide failures in the event of faults [7, 8]. To achieve this, the PDN is separated into multiple switchboards each clustering various loads and power supplies, that are then interconnected through the use of solid state bus tie switches (SSBTSs). In addition to the reconfigurability offered by the solutions, these devices prevent the propagation of a fault by quickly isolating the malfunctioning sector in the event of a fault, effectively acting as a first line of defence and providing selectivity as a part of the protection coordination scheme in which they operate [8, 9, 10]. There are several characteristics that an SSBTS must have in order to fulfil this role, differentiating it from a circuit breaker in the traditional sense:

- Provide current interruption in the range of a few µs.
- Have limited conduction losses, subordinated to its protection ability.
- Allow four-quadrant operation.
- Include on-board fault detection logic, to minimise reaction time.

Due to the lack of standardisation of MVDC shipboard PDNs, that include voltage ranging from 3 kV up to 25 kV, a standard SSBTS solution for bus interface is not available [11, 12]. In this context, a scalable SSBTS that can operate at increasing voltage and power ratings through series and parallel connection of standardised building blocks can provide significant advantages in terms of flexibility, providing a solution based on available technology that can accommodate the different needs of MVDC systems as the industry moves towards standardisation. This paper presents such a scalable SSBTS topology and it's implementation in two identical prototype units, evaluating their ability to achieve increased current and voltage ratings in parallel and series connection, respectively.

Scalable SSBTS Topology

Fig. 1a displays the proposed SSBTS topology, based on a well known four quadrant switch and including the addition of protective circuitry to enable SSBTS operation. This additional circuitry includes metal oxide varistors (MOVs) to limit the voltage on the device terminals, an *RC* snubber to limit voltage peaks on the active semiconductor device upon current interruption. Additionally, a current rate limiting inductor L_{didt} is inserted in the current path to limit the current rise rate in the event of a fault. This allows for controllable (depending on the selected inductor value) addition of reaction time for the control to detect the fault and turn off the device. A general rule for the sizing of this inductor, based on the system in which it operates, is provided. The antiparallel diode of the inductor, D_L, provides a self contained freewheeling path that allows for the dissipation of the stored energy of L_{didt} through the diode and inductor's own internal resistance upon the device opening. Note that the device only needs to be connected between the positive terminals of the DC bus, as shown in Fig. 2. Fig. 3 displays the operation of the topology during a fault, time instant by time instant. Before instant t_0, the device is in conduction and no fault condition is present. The current path is through two of the rectifier diodes (depending on the current direction), the IGBT and current rate limiting inductor. Then, at time t_0, a fault happens and a voltage appears across the SSBTS terminals as a consequence. This results in a progressive increase of the current in the device at a rate determined by the applied voltage and L_{didt}. At time t_1 the device has detected the fault and turned off the IGBT. This initiates the interruption process and the path of the current goes from being that represented in Fig. 1b, to that in Fig. 1c. The current that was conducted by the IGBT now flows through the parallel RC snubber, gradually increasing the voltage and slowing the current rise. At time t_2 the voltage on the snubber is sufficient to stop the current increase by reaching the same value as the DC voltage applied at the SSBTS terminals. This forward biases diode D_L that enters conduction allowing the current level in L_{didt} to remain almost constant for the duration for the rest of the interruption process. After t_2 the voltage on the snubber keeps increasing until at t_3 it reaches



(a) (b) (c)

Fig. 1: (a) Proposed scalable SSBTS topology; (b) SSBTS current path during conduction; (c) SSBTS current path during breaking.

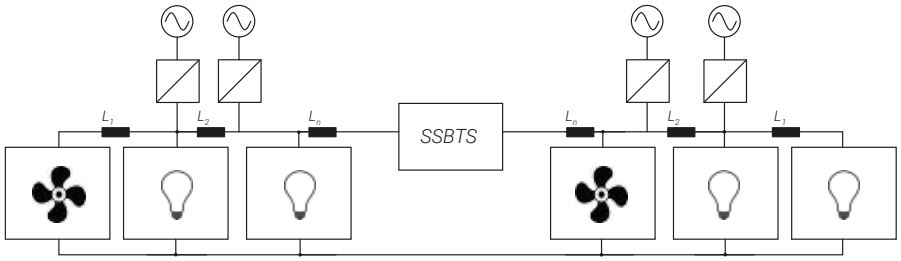
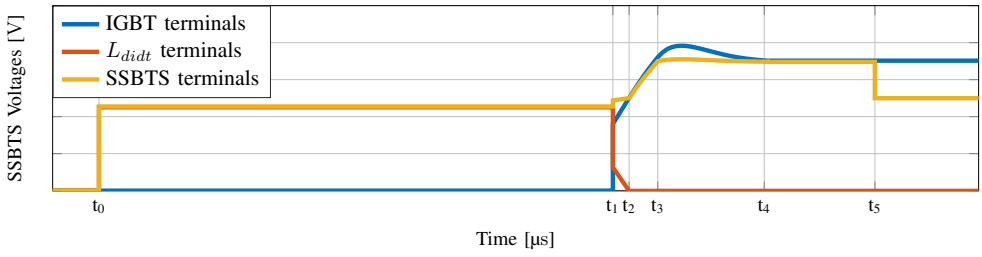
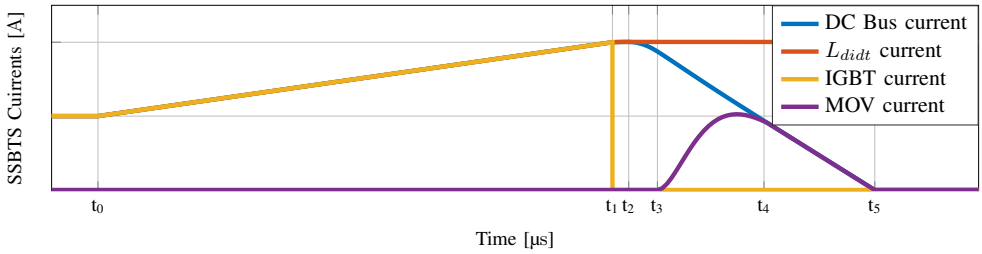


Fig. 2: The SSBTS separates switchboard clustering power courses and loads. The device is connected only to the positive terminals of the DC bus, and includes a current rate limiting inductor to limit current rise rate in the event of a fault.



(a)



(b)

Fig. 3: (a) View from above of the SSBTS prototype, without current rate limiting inductor; (b) Side view of the prototype with active cooling fans.

the clamping voltage of the MOV. The MOV therefore enters conduction maintaining the voltage at its terminals (and therefore at the SSBTS terminals) at a constant value. Between t_3 and t_4 the voltage on the snubber is higher than that at the MOV terminals. This is due to the internal stray inductance of the device. The DC bus current in this interval drops at a rate determined by the difference between the MOV clamping voltage and the voltage applied to the SSBTS terminals. From t_4 onwards the whole DC bus current is conducted through the MOV and none through the snubber, until at t_5 the current reaches 0 A and the interruption is complete.

The analysis of the operation of the topology highlights how its ability to be series connected in a simple and effective way makes it particularly suitable for operation at increased voltage ratings. This is mainly due to three characteristics:

- Connecting the terminals of the switch is a MOV able to clamp the voltage at a predetermined value. This guarantees correct voltage sharing of series connected SSBTS units during breaking.
- The current in the L_{didt} current rate limiting inductor is allowed to freewheel internally, without requiring access to the negative DC bus bars, as is the case in other topologies [8].
- The current rise rate in series or parallel connected devices at the time when the fault takes place

is determined by L_{didt}, and will ensure all SSBTS units are conducting the same current level. On the other hand, the diode bridge structure of the topology forces current flow through three semiconductor devices in the *ON* state, causing an increase of losses compared to other existing topologies. Nevertheless, as the SSBTS is first and foremost a protection device, an increase in losses is outweighed by an increased protection capability that allows an extended range of employment for the device. Additionally, the conducted current in the SSBTS is rarely equal to it's nominal current, as a balanced operation of the PDN with generated power similar to the load power in each switchboard is generally preferred [9]. Overall, the advantages offered by the simplicity of connection, single active semiconductor device and most importantly scalability result in the topology being a very suitable for the application. Note also that even in series or parallel connection the efficiency of the device remains the same, as the power conduction ability increases at the same rate as device losses.

SSBTS Prototype Units

Two SSBTS prototype units as in Fig. 4a and 4b are assembled with the goal of validating the scalability of current and voltage rating through parallel and series connection respectively. The prototypes result from the downscaling of an SSBTS operating in a 1 kV, 8 MW system. This full-scale device has a nominal current of 8 kA and a maximum interruption current of 16 kA, and this ratio of 2 : 1 is maintained in the presented prototype. The ratings for the device assembled in the laboratory are:

- A nominal voltage of the PDN of 500 V.
- A nominal device current I_{nom} of 100 A.
- A maximum breaking current I_{max} of 200 A.
- An interruption time $t_{reaction}$ of 10 µs.

It is worth noting that the relatively low value of I_{max} with respect to I_{nom} can be achieved thanks to the fast interruption time. Upon a fault taking place, the current in the SSBTS increases gradually limited by the inductance of L_{didt}. If the inductance is appropriately sized, the current in the device will still be below I_{max} once the SSBTS identifies the fault and interrupts. The inductor L_{didt} is sized according to:

$$L_{didt} = \frac{V_{DC}}{I_{max} - I_{nom}} t_{reaction} = \frac{500\,\text{V}}{100\,\text{A}} * 10\,\mu\text{s} = 50\,\mu\text{H} \tag{1}$$

In the prototype the values is adapted to 48 µH due to availability of components. The fact that an air core inductors is selected removes possible issues due to saturation. With the chosen L_{didt} value, the controller has 10 µs to interrupt after the fault takes place, under the hypothesis of a worst case scenario where the value of the current in the DC bus is already equal to the full nominal current I_{nom}. The reaction time $t_{reaction}$ is a parameter to be chosen by the system designer based on the specific needs of the application, and is selected here to be equal to 10 µs to demonstrate ultrafast interruption ability of the device. Upon interruption, the energy stored in the stray inductance of the DC bus and the internal stray inductance of the SSBTS needs to be dissipated. This task is shared between *RC* and MOV, where the former is charged with storing the energy in the stray inductance of the device itself, while the latter dissipates the energy in the DC bus inductance, by conducting at a clamped terminal voltage. As a 10 m DC bus has a stray inductance of approximately 10 µH according to [13], even at 200 A the energy stored will not exceed

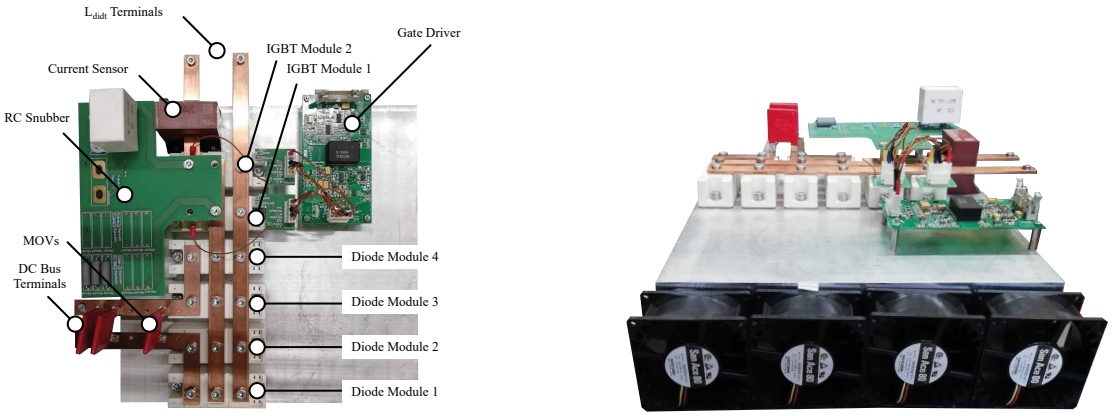
$$E_{bus} = \frac{1}{2} L_{bus} I_{max}^2 = \frac{1}{2} \times 10\,\mu\text{H} \times 200\,\text{A}^2 = 0.2\,\text{J} \tag{2}$$

This is a relatively modest amount of stored energy. Therefore, the MOVs are selected not based on their energy dissipation ability, but rather on their voltage to current characteristic to ensure the desired clamping voltage. The selected device is a *Littlefuse V421HG34*, of which three are paralleled to limit the clamping voltage below 1 kV at 200 A, as the semiconductors are rated for 1.2 kV. The sizing of the *RC* is more challenging as the internal stray inductance of the SSBTS is not well known. The capacitor is selected to have a value of 1 µF, which allows, with a voltage increase of 500 V over the DC bus voltage,

the storage of the energy contained in

$$L_{stray,max} = \frac{C_{snub} V_{DC}}{I_{max}^2} = \frac{1\,\mu\text{F} \times 500\,\text{V}}{200\,\text{A}^2} \approx 6\,\mu\text{H}, \tag{3}$$

which is the energy stored in more than half of the DC bus. In testing, the size of the capacitor proved to be comfortably sufficient and a smaller value could be chosen if needed. The value of the resistor is selected so that a current value of I_{max} through the snubber immediately results in the application of 500 V to the snubber terminals, which results in a resistor value of 2.5 Ω, but due to component availability, a value of 1.8 Ω is finally selected. Before series and parallel connection of the units is evaluated, the prototype is individually tested in its ability to conduct and interrupt current. A block schematic of the switching test setup for the characterisation of the prototype is shown in Fig. 5a and its results are in Fig. 5b. In this test, the level of current flowing through the SSBTS is sensed and sampled by the controller, which turns off the device if threshold of 100 A is exceeded. The setup is such that an artificial short circuit current is generated by charging capacitor $C = 230\,\mu\text{F}$ to 500 V, and then closing the SSBTS effectively short circuiting the capacitor. The current increases linearly through the device, until the controller detects the current value exceeding the set threshold and switches off. $L_{external}$ is added in the current path to reproduce the effect of DC bus stray inductance and has a value of 5 µH. In the results in Fig. 5b, sensed through oscilloscope connected voltage and current probes, one can see the linear current increase starting once the SSBTS turns on, and the interruption of the current after turn off. Note that during interruption the voltage on the device terminals and on the active switch is kept below 800 V. The voltage on the IGBT terminals remains at this level for an extended amount of time, as the snubber capacitor slowly discharges over a time significantly longer time interval (up to 10 ms). Note that in spite of the presence of the *RC* snubber in parallel with the IGBT position, there is a voltage spike at the moment of turn off before the charging of the snubber takes place. This is due to the stray inductance present in the snubber path, that reacts with an overvoltage as the snubber is forced to take over the IGBT current as they turn off. This overvoltage can likely be reduced through redesign of the snubber board, as the version used to obtain the results presented in this paper was designed for the adaptability of resistor and capacitor values, and not optimised for the reduction of stray inductance. Nevertheless, the voltage peak at the time of switching remains always smaller than the maximum voltage at the IGBT terminals reached through snubber capacitor charging, and therefore does not constitute an impediment to the operation of the device.



(a) (b)

Fig. 4: (a) View from above of the SSBTS prototype, without current rate limiting inductor; (b) Side view of the prototype with active cooling fans.

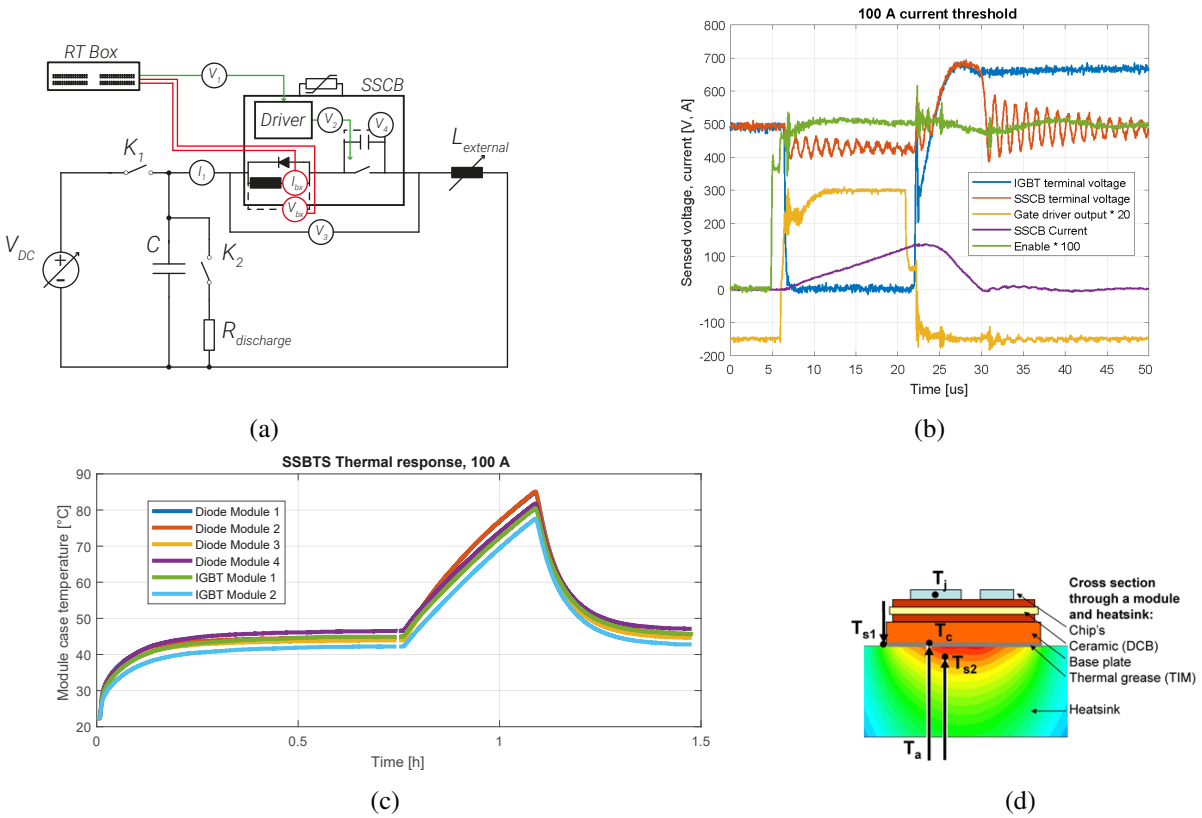
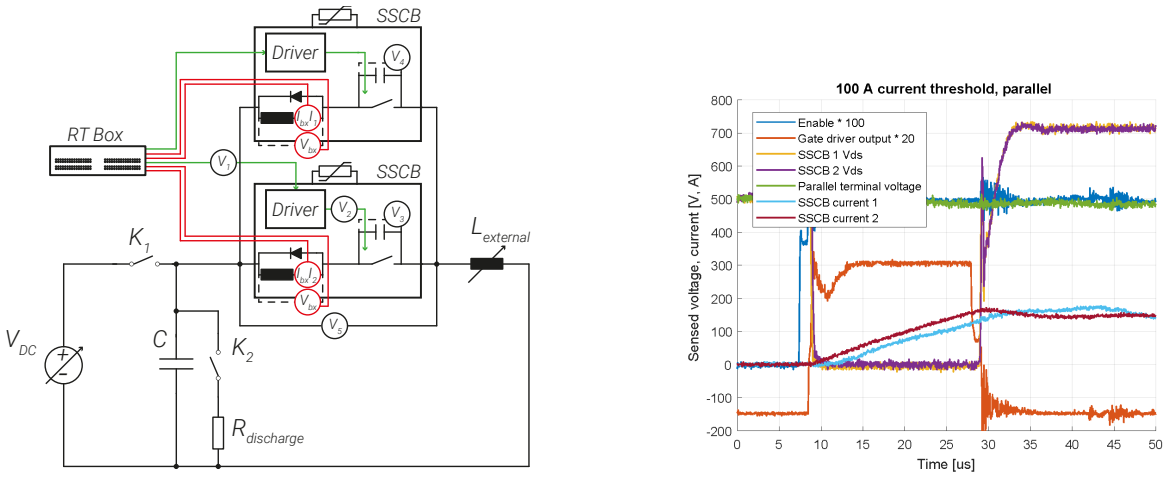


Fig. 5: (a) Block schematic of of the test setup for the characterisation of prototype switching; (b) Switching test results; (c) Thermal conduction test results; (d) Case temperature sensing is performed by inserting thermocouples in a channel in the heatsink reaching under the modules [14].

Fig. 5c displays the results of the thermal testing of the device, in which the nominal current of 100 A is circulated through the SSBTS and the case temperature of the semiconductor devices is sensed as in Fig. 5d. This is relevant as it was chosen that all positions in the device should be constituted by two paralleled semiconductor devices. The reason for this choice is that this is necessary in most full scale SSBTSs for marine applications. Interruption currents in the range of tens of kA can easily be reached, which are beyond the safe operating area (SOA) of individual commercially available semiconductor modules. Therefore, an SSBTS prototype employing paralleled semiconductors offers a more realistic solution than using individual devices. Fig. 5c shows that the temperature sharing between the semiconductor modules is satisfactory. The shape of the curve results from the way the test is performed. Initially, the devices starts cold and is allowed to reach steady state with cooling fans turned on. The fans are turned off and the case temperature is allowed to increase up to 85 °C, showing the temperature sharing of the modules is effective also at increased case temperature. Then, cooling fans are once again turned on bringing the temperatures back to the steady state initially achieved.

Parallel Operation

Having determined that the SSBTS prototype individually performs as desired, the two devices are tested in parallel to evaluate whether they can provide equivalent performance at twice the current ratings. Therefore, in parallel configuration the nominal current is considered to be $I_{nom,p} = 200\,\text{A}$, and the maximum breaking current $I_{max,p} = 400\,\text{A}$. The current interruption ability of the device is evaluated first. Fig. 6a shows how the test setup is adapted to accommodate for two parallel connected SSBTS units. The paralleling of the units is done through symmetric bus bars to avoid issues with current sharing linked to different resistance of the conductors. From the point of view of control, the controller is coded such that if the current in either of the devices exceeds the value of 100 A, then both units are tripped.



(a) (b)

Fig. 6: (a) The interruption test setup is expanded to accomodate two parallel connected SSBTSs units; (b) The results of the switching test show adequate current sharing.

This prevent units from tripping individually resulting in unwanted current peaks. Fig. 8b displays the results of this test. Here, one can see how, after the devices are turned on, the increase of current happens at the same rate in each SSBTS. This is determined by the equal value of L_{didt} in each unit, which are both equal to 48 µH. The equal rise rate of current in the devices results in correct fault current sharing, and tripping happens due to the current in the device 2, which is slightly higher than than in the device 1. Operation with less effective current sharing than that shown in Fig. 8b, while undesirable, is still possible as long as the maximum current in both devices is lower than their $I_{max} = 200\,\text{A}$.

Fig. 7 displays the results of thermal conduction tests for the two paralleled units. The goal of the test is to show that the temperature reached by the cases of the semiconductors is similar is the two paralleled units. This in turn shows that the current conducting capability of each unit is not decreased by paralleling. The results do not display the temperature of each individual semiconductor module, as was the case in Fig. 5c, but of the averaged temperature of the cases of IGBTs and diodes of each unit. The figure shows clearly that the temperature of both these modules are almost identical in the two units, and that therefore the conducted and interrupted current of the device can be linearly increased through paralleling.

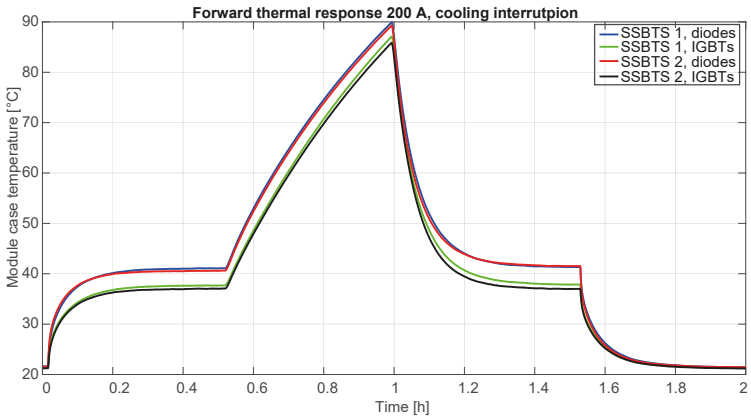


Fig. 7: The nominal current two parallel devices are able to conduct is 200 A, thanks to excellent temperature distribution of the modules in the two units.

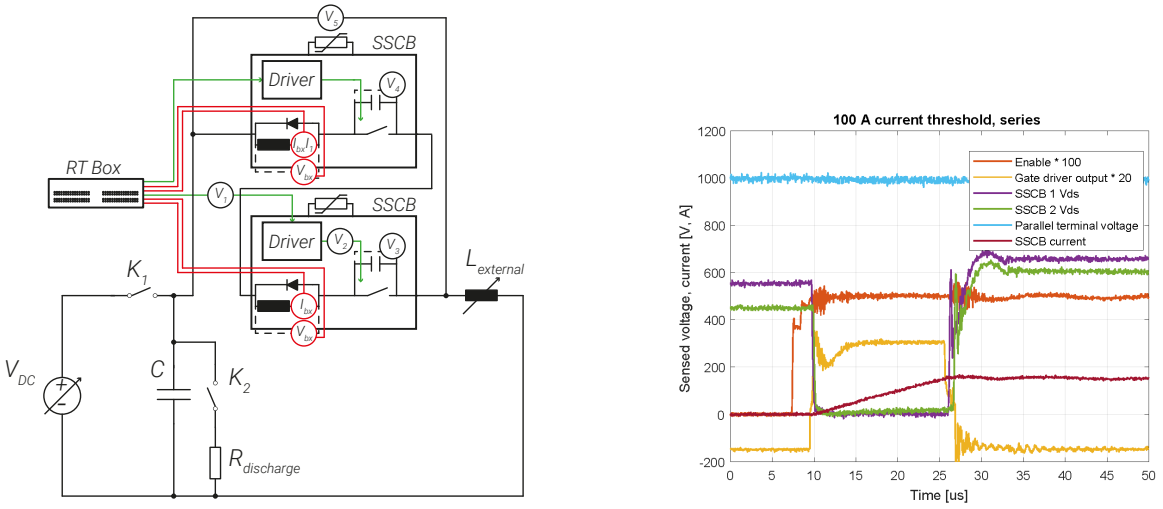
Series Operation

Finally, series operation of two units is evaluated. The test carried out in this section aims to determine whether the operating voltage of the SSBTS can be increased by connecting multiple prototype units in series. For this test, the series connected devices perform an interruption at the voltage level of 1 kV and the voltage sharing between the two is evaluated. Fig. 8a displays the series connection of the two units in the test setup. Unlike in the previous two tests, in this test capacitor C is loaded up to 1 kV instead of 500 V. Since each SSBTS unit contains a current rate limiting inductance of 48 µH, this results in a current rate of increase of:

$$\frac{di}{dt} = \frac{V_{DC}}{2L_{didt}} = \frac{1000\,\text{V}}{96\,\mu\text{H}} = \frac{500\,\text{V}}{48\,\mu\text{H}} \tag{4}$$

Therefore, in spite of the increase of DC voltage, the current rate of increase remains the same in this test as it was by using a single unit at 500 V. As in the previous parallel connected test, the two devices are both tripped if the current in either one exceeds $I_{nom} = 100\,\text{A}$. As the devices are series connected, the current in both is exactly the same. Nevetherless, due to sensing delays and noise one of the two devices will inevitably cause tripping before the other. In this case, both units need to be tripped to prevent a single one from blocking the full DC voltage of 1 kV.

Fig. 8b displays the results of the switching tests. The figure shows how the voltage of both units is kept below 800 V and that the voltage and current stresses in series connected operation are equivalent to those of a single device operating at 500 V, demonstrating that series connected operation is an effective way of scaling up the SSBTS voltage. Nevertheless, it can be seen that before the devices are turned on, the voltage sharing between the two is not perfect, with unit 1 blocking around 550 V and unit 2 only blocking around 450 V. The trend toward this disparity in blocking voltage is visible also after the devices have turned off, and the voltage gradually settles back to this level. This behaviour is due to the MOVs in parallel with each device. In particular, to the fact that the current to voltage characteristic of MOVs is very variable for low values of conducted current. Therefore, a small variation of conducted current results in a large terminal voltage variation. Due to manufacturing tolerances, it is unlikely for two MOVs to exhibit exactly the same characteristic. For series connected SSBTS units, this means that since the same leakage current in the present in the MOVs of the two devices, any variation in current to voltage characteristic is reflected on the terminal voltage.



(a) (b)

Fig. 8: (a) Block schematic of of the test setup for the characterisation of series connected prototype switching; (b) Switching test results.

Nevertheless, it should be noted that if the leakage current in the series connected devices were to increase because of this, then the relative difference of the terminal voltage of the SSBTSs would drop, due to the MOV characteristic flattening out at increased levels of current. Therefore, the voltage sharing between the units one can see in the figure is a stable configuration, and there is no risk of it increasing for varying values of leakage current.

Conclusion

This paper has presented a novel SSBTS topology for marine applications intended to operate in parallel and series connection to allow the increase of current and voltage rating of the shipboard PDNs in which it operates. The operating principles of the topology have been illustrated and the ability of the constructed prototype to conduct and interrupt its rated current at its rated voltage has been demonstrated experimentally. Additionally, the operation of the topology in series and parallel connection is also experimentally validated, demonstrating the desired ability to increase device's ratings through the connection of multiple units.

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