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Characterization and Modeling of Total Ionizing Dose Effects on Nanoscale MOSFETs for Particle Physics Experiments

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Nothing in life is to be feared,
it is only to be understood.
Now is the time to understand more,
so that we may fear less.
— Marie Curie

To my family,
for their unbounded love and unwavering support

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Abstract

Total ionizing radiation compromises electrical characteristics of microelectronic devices and even causes functional failures of integrated circuits. It has been identified as a potential threat to electronic components, especially those in high-energy physics experiments, space and avionic systems, and nuclear power plants. Among all harsh radiation environments, the future High Luminosity Large Hadron Collider (HL-LHC) at European Organization for Nuclear Research (CERN), is expected to have by far the highest levels of total ionizing dose (TID) with a peak of 1 Grad(SiO_2) in the innermost electronics. Also, the number of pileup events per bunch crossing can reach up to 200, challenging trigger and data acquisition systems of its particle experiments. To reach long-term reliable operation, the HL-LHC will require innovative detecting and tracking systems with a higher level of granularity and bandwidth as well as robust radiation-tolerant front-end electronics.

Complementary metal-oxide-semiconductor (CMOS) scaling allows extended circuit functionality and enhanced computing power. It also improves the TID tolerance of MOS field-effect transistors (MOSFETs) with relieved charge trapping related to ultrascaled gate dielectrics. To evaluate the potential use of highly scaled devices in the HL-LHC and eventually support circuit design for radiation-tolerant applications, this thesis characterizes and models the effects of TID up to 1 Grad(SiO_2) on a commercial 28-nm bulk CMOS process. The characterization part focuses on evaluating measurable radiation effects and identifying dominant physical mechanisms. The modeling part aims at improving the understanding of the observed radiation effects and developing a design-oriented compact model for comprehensively accounting for them.

Under various bias and temperature conditions, devices are irradiated, annealed, and tested after each irradiation and annealing step. Most of them demonstrate slight parametric shifts, confirming the very high TID tolerance of ultrathin gate dielectrics. TID-induced degradation in this technology primarily depends on charge trapping related to thick shallow trench isolation (STI) oxides. STI-trapped positive charges in *n*MOSFETs open parasitic channels along STI sidewalls and cause a significant increase in the drain leakage current, which however almost disappears after high-temperature annealing. STI-related charge trapping can even be strong enough to influence the central part of a narrow channel and is seen seriously degrading the performance of narrow-channel MOSFETs, which however can be relieved by shortening the channel.

Abstract

The TID-induced parasitic leakage current of *n*MOSFETs is modeled via a gateless charge-controlled transistor. To model the effects of TID on inversion operation, a generalized Enz-Krummenacher-Vittoz (EKV) charge-based MOSFET model is developed through the incorporation of radiation-induced trapped charges into the original EKV MOSFET model. Despite a small number of parameters, this model demonstrates an excellent match with measurement results over a wide range of device operation. The effects of TID on MOSFET characteristics are efficiently described by those few model parameters. This newly-developed radiation-aware EKV MOSFET model also demonstrates a width dependence of TID effects on 28-nm bulk MOSFETs, which can be explored for the model extension to a broad range of device dimensions even for a continuous range of TID levels.

Keywords

Charge trapping, compact modeling, EKV charge-based MOSFET model, gate oxide, HL-LHC, interface-trapped charges, nanoscale bulk CMOS, 1 Grad(SiO_2), oxide-trapped charges, parameter extraction, parasitic drain-to-source leakage current, radiation effects, radiation-induced narrow-channel effects, RINCE, radiation-induced short-channel effects, RISCE, shallow trench isolation, STI, total ionizing dose, TID.

Résumé

Les rayonnements ionisants compromettent les caractéristiques électriques des composants micro-électroniques et peuvent provoquer des dysfonctionnements des circuits intégrés. Ils ont été identifiés comme une menace pour les composants électroniques, en particulier dans les domaines de la physique des hautes énergies, l'aérospatial, et les centrales nucléaires. Parmi les environnements sujets à de sévères rayonnements, l'électronique du Grand Collisionneur de Hadrons à Haute Luminosité (HL-LHC de l'anglais High Luminosity Large Hadron Collider), qui sera prochainement mis en place par le CERN (Conseil Européen pour la Recherche Nucléaire), devra faire face aux niveaux les plus élevés de radiations, avec une dose ionisante cumulée (TID de l'anglais Total Ionizing Dose) de l'ordre de 1 Grad(SiO_2). Egalement, il pourra y avoir jusqu'à 200 évènements par collision, ce qui rendra très difficile le déclenchement et l'acquisition des données lors d'expérimentations. Pour atteindre un fonctionnement fiable à long terme, le HL-LHC nécessitera donc des détecteurs innovants dotés d'une granularité et d'une bande passante plus élevées, ainsi que des systèmes électroniques robustes et résistants aux rayonnements.

La réduction de la taille des technologies "complementary metal-oxide-semiconductor" (CMOS) permet d'augmenter l'efficacité et la puissance de calcul des circuits intégrés. Elle s'accompagne aussi d'une amélioration de la résistance des transistors à effet de champ à grille métal-oxyde (MOSFET de l'anglais Metal-oxide-semiconductor Field-effect Transistor) grâce à une diminution des charges piégées dans un diélectrique de grille de plus en plus fin. Afin d'évaluer le potentiel d'utilisation de technologies plus récentes dans le HL-LHC ainsi que d'aider la conception de circuits pour des applications soumises à de hauts rayonnements, la présente thèse caractérise et modélise les effets du TID jusqu'à 1 Grad(SiO_2) sur une technologie CMOS 28 nm bulk. La première partie de ce travail se concentre sur la caractérisation des effets des rayonnements ionisants et l'identification de leurs principaux mécanismes physiques. La deuxième partie vise à améliorer la compréhension des effets des rayonnements observés au travers du développement d'un modèle compact décrivant de manière exhaustive les effets des TID et pouvant être utilisé pour la conception de circuits intégrés.

De multiples composants intégrés ont été irradiés, recuits, et testés après chaque étape d'irradiation et de recuit sous différentes températures et tensions de polarisation. La plupart d'entre eux ne montrent que de légères variations de leurs paramètres principaux, confirmant la haute tolérance aux rayonnements des diélectriques de grille ultra-minces. Pour cette tech-

nologie CMOS 28 nm bulk, la dégradation induite par les rayonnements ionisants dépend principalement du piégeage de charges lié à l'épaisseur des oxydes d'isolation "shallow trench" (STI). Les charges positives piégées dans les oxydes STI des transistors MOSFET à canal n induisent un courant de fuite parasite le long des flancs du STI. Ceci conduit à une augmentation du courant de fuite du drain qui disparaît néanmoins après un recuit à haute température. La charge piégée peut être suffisamment grande pour influencer la partie centrale des canaux étroits et sérieusement dégrader le comportement des transistors MOSFET à canaux étroits, anomalie qui se résout en raccourcissant le canal.

Le courant de fuite parasite des transistors MOSFET à canal n a été modélisé par un transistor sans grille mais à contrôle par la charge. Pour modéliser les effets des rayonnements en situation d'inversion, un modèle du transistor MOSFET généralisé s'appuyant sur le modèle Enz-Krummenacher-Vittoz (EKV) a été développé, en injectant dans le modèle EKV original des charges piégées dans l'oxyde et dans l'interface du transistor MOSFET. Ce modèle montre une excellente capacité à prédire avec précision les résultats mesurés sur une large zone d'inversion malgré un nombre de paramètres très réduits. Ces derniers permettent une reproduction fidèle des effets des rayonnements sur les caractéristiques des composants intégrés. Ce nouveau modèle incorporant l'effet des rayonnements ionisants démontre aussi leur relation à la largeur du composant sur cette technologie CMOS 28 nm bulk. Enfin, ce modèle peut être généralisé à une large gamme de dimensions de composants et de niveaux de radiation.

Mots clés

Charges piégées, modélisation compacte, un modèle du transistor MOSFET s'appuyant sur le modèle EKV, oxyde de grille, HL-LHC, charges piégées dans l'interface, CMOS en masse à l'échelle nanométrique, 1 Grad(SiO_2), charges piégées dans l'oxyde, extraction de paramètres, courant de fuite parasite drain-source, effets des radiations, effets de canal étroit induits par les rayonnements, RINCE, effets de canal court induits par les rayonnements, RISCE, isolation de tranchée peu profonde, STI, dose ionisante totale, TID.

摘要

总剂量电离辐射会引起微电子器件电学性能退化，甚至导致集成电路功能失效。特别是在高能物理实验、航空航天系统、以及核电站等领域，总电离辐射已被视作电子元器件可靠性的潜在威胁。在所有苛刻的辐射环境中，欧洲核子中心（European Organization for Nuclear Research，CERN）未来的高亮度大型强子对撞机（High Luminosity Large Hadron Collider，HL-LHC）预计将具有最高的总电离辐射剂量–最中心的电子设备将面临高达1 Grad(SiO_2)的总剂量电离辐射。而且，每个交叉束要采样的事例数目可高达200个，这将使得粒子实验触发装置和数据采集系统的设计极具挑战性。为了确保系统长期可靠运转，HL-LHC的新型探测和追踪系统将需要具有更高粒度和带宽并有抗超高总剂量电离辐射能力的前端电子系统。

互补金属氧化物半导体（Complementary Metal-oxide-semiconductor，CMOS）工艺的持续发展拓展了集成电路的功能并加强了微电子系统的计算能力。而且，栅极电介质层的极度减薄可缓解相关的电荷俘获，进而改善金属氧化物半导体场效应管（Metal-oxide-semiconductor Field-effect Transistor，MOSFET）的抗总剂量电离辐射性能。为了评估先进CMOS工艺下微电子元器件在HL-LHC中的应用前景并最终支持抗辐射应用相关的电路设计，本论文对商用28纳米体硅CMOS工艺进行了高达1 Grad(SiO_2)的超高总剂量电离辐射效应的表征和建模研究。本论文的表征部分集中于可测量辐射效应的评估以及主要物理机制的识别。本论文的建模部分旨在完善对观察到的实验现象的理解，并且开发一个全面考虑总剂量电离辐射效应的面向设计的紧凑模型。

这部分工作在不同偏置和温度下对器件进行了辐照和退火，并在辐照和退火的每个步骤前后对器件进行了电学测试。实验结果表明，大多数MOS管的参数在辐射后呈现轻微变化，证实了超薄栅极电介质层的较强抗总剂量电离辐射的能力。28纳米体硅CMOS工艺下总剂量电离辐射造成的退化主要取决于较厚浅槽隔离（Shallow Trench Isolation，STI）氧化层相关的电荷俘获。在N型MOS管中，STI俘获的正电荷会开启沿着STI侧墙的寄生沟道，导致漏端泄漏电流明显增加，但此漏端泄漏电流增加在高温退火后基本消失。STI相关的电荷俘获甚至也会影响窄沟道器件的沟道中央部分，严重影响窄沟道MOS管的性能，但此严重影响可通过降低沟道长度来缓解。

总剂量电离辐射在N型MOS管中引起的寄生泄漏电流通过由电荷控制的无栅器件进行模拟。为了模拟总剂量电离辐射对器件反型区的影响，辐射导致的俘获电荷被引入原始的基于电荷的Enz-Krummenacher-Vittoz (EKV) MOSFET模型，最终得到一个广义的EKV MOSFET模型。尽管模型中参数数量较少，这个模型还是在器件工作的很大范围内与测试结果匹配良好。少数几个模型参数有效描述了总剂量电离辐射对MOS管特性的影响。

该基于辐射的最新EKV MOSFET模型还证明了总剂量电离辐射效应在28纳米体硅CMOS工艺中的器件沟道宽度相关性。此沟道宽度相关性可进而用于将该模型推广适用于更广泛的器件尺寸范围，甚至适用于连续的辐射总剂量。

关键字

电荷俘获，紧凑建模，基于电荷的EKV MOSFET模型，栅氧化层，HL-LHC，界面俘获电荷，纳米级体硅CMOS，1 Grad(SiO_2)，氧化层俘获电荷，参数提取，寄生漏-源泄漏电流，辐射效应，辐射引起的窄沟道效应，RINCE，辐射引起的短沟道效应，RISCE，浅槽隔离，STI，总剂量电离辐射，TID。

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Symbol	Description	Quantity/Unit
	Physical parameters	
q	Elementary charge	1.60×10^{-19} C
k	Boltzmann constant	1.38×10^{-23} J/K
T	Room temperature (unless stated otherwise)	298.15 K
$U_T = kT/q$	Thermodynamic voltage	0.026 V
ϵ_0	Vacuum permittivity	8.85×10^{-12} F/m
ϵ_{si}	Permittivity of silicon (Si)	$11.9\epsilon_0$
ϵ_{ox}	Permittivity of silicon dioxide (SiO_2)	$3.9\epsilon_0$
n_i	Intrinsic carrier concentration in Si	1.48×10^{16} m^{-3}
μ_0	Low-field channel mobility	m/(V·s)
	Process parameters	
N_b	Channel doping concentration	m^{-3}
$\Phi_F = U_T \ln(N_b/n_i)$	Fermi potential	V
v_{drift}	Drift velocity	m/s
v_{sat}	Saturated drift velocity	m/s
T_{sti}	Thickness of the shallow trench isolation (STI)	m
X_j	Junction depth	m
t_{ox}	Equivalent oxide thickness to SiO_2	m
$C_{ox} = \epsilon_{ox}/t_{ox}$	Gate oxide capacitance per unit area	F/m^2
$\Gamma_b = \sqrt{2qN_b\epsilon_{si}}/C_{ox}$	Substrate modulation factor	V$^{0.5}$
$\gamma_b = \Gamma_b/\sqrt{U_T}$	Normalized substrate modulation factor	–
	Geometry	
W	Channel width	m
N_F	Number of fingers	-
W_F	Channel width of each finger	m
W_{eff}	Effective channel width	m
ΔW	Channel width modification	m
L	Channel length	m

Symbol	Description	Quantity/Unit
L_{eff}	Effective channel length	m
ΔL	Channel length modification	m
x	Distance from the source along the channel	m
$\xi = x/L$	Normalized position along the channel	–
y	Distance across the channel	m
z	Vertical distance down from the surface	m
	Voltages and potentials	
Φ_{Fn}	Electron quasi-Fermi potential	V
Φ_{Fp}	Hole quasi-Fermi potential	V
Ψ_{s}	Surface potential	V
$\Psi_0 = 2\Phi_{\text{F}} + (2-4)U_{\text{T}}$	Constant potential slightly larger than $2\Phi_{\text{F}}$	V
Ψ_{P}	Pinch-off potential	V
Φ_{ms}	Metal-silicon work function difference	V
V_{FB}	Flatband voltage	V
V_{T}	Threshold voltage	V
V_{GB}	Gate-to-bulk voltage	V
V_{DS}	Drain-to-source voltage	V
V_{DD}	Power supply	V
V_{ox}	Voltage drop across the gate oxide	V
V_{ch}	Channel voltage	V
V_{P}	Pinch-off voltage	V
V_{mg}	Mid-gap voltage	V
$\phi_{\text{f}} = \Phi_{\text{F}}/U_{\text{T}}$	Normalized Fermi potential	–
$\psi_{\text{s}} = \Psi_{\text{s}}/U_{\text{T}}$	Normalized surface potential	–
$\psi_{\text{p}} = \Psi_{\text{P}}/U_{\text{T}}$	Normalized pinch-off potential	–
υ_{sh}	Threshold shift	–
$\upsilon = V_{\text{ch}}/U_{\text{T}}$	Normalized channel voltage	–
$\upsilon_{\text{p}} = V_{\text{P}}/U_{\text{T}}$	Normalized pinch-off voltage	–
	Currents	
I_{D}	Drain current	A
I_{Dleak}	Drain leakage current	A
I_{on}	Drive current	A
I_{S}	Source current	A
I_{nW}	Substrate current flowing from the n-well	A
$I_{\text{spec}_\square} = 2n\mu_0 C_{\text{ox}} U_{\text{T}}^2$	Specific current per square with n defined below	A
$I_{\text{spec}} = I_{\text{spec}_\square} W/L$	Specific current	A
$i_{\text{d}} = I_{\text{D}}/I_{\text{spec}}$	Normalized drain current	–
$IC = i_{\text{d}}$	Inversion coefficient	–

Symbol	Description	Quantity/Unit
	Charges	
Q_G	Gate charge density per unit area	C/m^2
Q_f	Fixed oxide-charge density per unit area	C/m^2
Q_{si}	Total silicon charge density per unit area	C/m^2
Q_i	Inversion charge density per unit area	C/m^2
Q_b	Depletion charge density per unit area	C/m^2
$Q_{spec} = -2nC_{ox}U_T$	Specific charge density with n defined below	C/m^2
$q_i = Q_i/Q_{spec}$	Normalized inversion charge density	–
q_s	Normalized inversion charge density at source	–
q_d	Normalized inversion charge density at drain	–
	Small signals	
G_m	Gate transconductance	S=A/V
G_{ms}	Source transconductance	S=A/V
G_{md}	Drain transconductance	S=A/V
G_{ds}	Output conductance	S=A/V
$A_v = -G_m/G_{ds}$	Intrinsic gain	–
$G_{spec} = I_{spec}/U_T$	Specific transconductance	S=A/V
$g_m = G_m/G_{spec}$	Normalized gate transconductance	–
$g_{ms} = G_{ms}/G_{spec}$	Normalized source transconductance	–
$g_{md} = G_{md}/G_{spec}$	Normalized drain transconductance	–
$G_m nU_T/I_D$	Normalized transconductance efficiency	–
f_t	Transit frequency	Hz
	Radiation-related parameters	
D	Total ionizing dose (TID) referred to SiO_2	rad
g_0	Charge pair density per unit volume per rad	pairs/[cm^3·rad]
ρ	Material density	g/cm^3
E_p	Electron-hole pair generation energy	eV
N_h	Initial hole yield	m^{-2}
Q_{it}	Interface-trapped charge density per unit area	C/m^2
D_{it}	Interface-trap density per unit area and energy	m^{-2}·eV^{-1}
g_t	Ground-state degeneracy factor	–
$C_{it} = q^2 D_{it}$	Interface-charge capacitance	F/m^2
$c_{it} = C_{it}/C_{ox}$	Normalized interface-charge capacitance	–
α_{it}	Interface-trap-related mobility reduction factor	m^2·eV/C
Q_{ot}	Oxide-trapped charge density per unit area	C/m^2
N_{ot}	Oxide-trap density per unit area	m^{-2}
ρ_{ox}	Oxide-trap density per unit volume	m^{-3}
W_{crit}	TID-related critical channel width	m
I_{Dleak0}	Pre-irradiation drain leakage current	A

Symbol	Description	Quantity/Unit
$I_{\mathrm{Dleak.par}}$	Parasitic drain-to-source leakage current	A
D_{crit}	Leakage-related critical total dose	rad
Q_{sti}	Equivalent STI-related trapped-charge density	$\mathrm{C/m^2}$
N_{sti}	Equivalent STI-related trap density	$\mathrm{m^{-2}}$
	Other parameters	
E_{x}	Longitudinal electric field	V/m
E_{i}	Intrinsic Fermi level	V/m
E_{c}	Critical longitudinal electric field	V/m
E_{z}	Vertical electric field	V/m
E_{s}	Vertical electric field at the surface channel	V/m
$\beta = \mu_0 C_{\mathrm{ox}} W/L$	Transconductance factor or transfer parameter	$\mathrm{A/V^2}$
SS	Subthreshold swing	mV/dec
n	Slope factor	–
$L_{\mathrm{sat}} = 2\mu_0 U_{\mathrm{T}}/v_{\mathrm{sat}}$	Channel length with velocity saturation	m
$\lambda_{\mathrm{c}} = L_{\mathrm{sat}}/L$	Velocity saturation parameter	–
α_{dibl}	Drain-induced barrier lowering parameter	mV/V

List of abbreviations

ALICE	A Large Ion Collider Experiment
ASIC	Application-specific Integrated Circuit
ATLAS	A Toroidal LHC ApparatuS
BJT	Bipolar Junction Transistor
BSIM	Berkeley Short-channel IGFET Model
BTI	Bias-temperature Instability
CAD	Computer-aided Design
CCD	Charge-coupled Device
CERN	European Organization for Nuclear Research
CGS	Centimeter-gram-second
CMOS	Complementary Metal-oxide-semiconductor
CMS	Compact Muon Solenoid
CTRW	Continuous-time Random Walk
CVD	Chemical Vapor Deposition
DIBL	Drain-induced Barrier Lowering
EKV	Enz-Krummenacher-Vittoz
ELT	Enclosed-layout Transistor
ESD	Electrostatic Discharge
ESR	Electron-spin-resonance
FDSOI	Fully-depleted Silicon-on-insulator
FE	Front-end
FET	Field-effect Transistor
FoM	Figure-of-merit
FoMs	Figures-of-merit
GIDL	Gate-induced Drain Leakage
HCI	Hot-carrier Injection
HDP	High-density Plasma
HEP	High-energy Physics
HKMG	High-κ Metal-gate
HL-LHC	High Luminosity Large Hadron Collider
IC	Integrated Circuit
IGFET	Insulated-gate Field-effect Transistor

LDD	Lightly-doped Drain
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LOCOS	Local Oxidation of Silicon
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
NCE	Narrow-channel Effect
PDK	Process Design Kit
RF	Radio-frequency
RHA	Radiation Hardness Assurance
RHBD	Radiation-hardness-by-design
RHBP	Radiation-hardness-by-process
RINCE	Radiation-induced Narrow-channel Effect(s)
RISCE	Radiation-induced Short-channel Effect(s)
ROC	Read-out Channel
SCE	Short-channel Effect
SEE	Single Event Effect
SI	International System
SMU	Source Measure Unit
SOI	Silicon-on-insulator
SPS	Super Proton Synchrotron
STI	Shallow Trench Isolation
TCAD	Technology Computer-aided Design
TDD	Total Displacement Damage
TEM	Transmission Electron Microscopy
TID	Total Ionizing Dose
TNID	Total Non-ionizing Dose
VS	Velocity Saturation

1 Introduction

1.1 Background and motivation

The Large Hadron Collider (LHC) at European Organization for Nuclear Research (CERN), as illustrated by the schematic layout in Fig. 1.1, is the world's largest and most powerful particle accelerator ever designed and built for scientific research [1,2]. It consists of a 27-km ring of superconducting magnets together with several accelerating structures to boost the energy of two beams of particles injected by the Super Proton Synchrotron (SPS). These two particle beams can be accelerated up to a center-of-mass energy of 6.5 TeV in opposite directions and then collide with a total energy of 13 TeV at four interaction points (IP1, IP2, IP5, and IP8). These points locate important particle detectors, called particle experiments in physics,

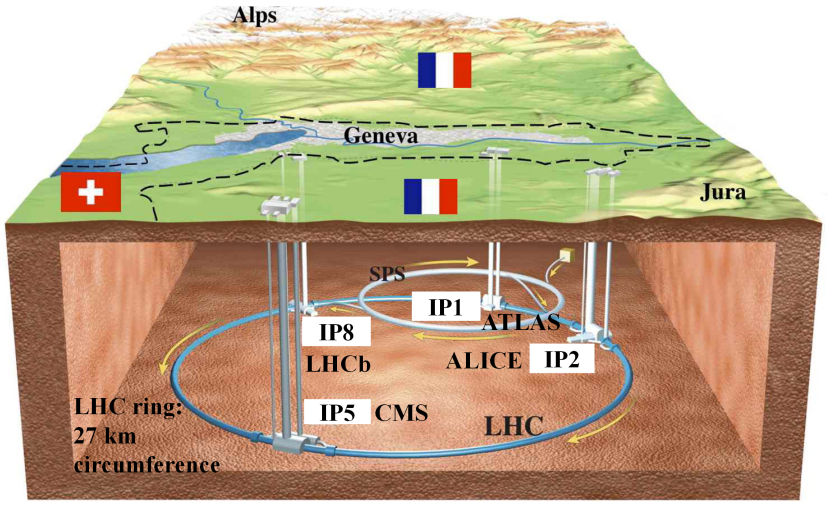


Figure 1.1 – Schematic layout of the Large Hadron Collider (LHC) with the Super Proton Synchrotron (SPS) providing two beams of particles and four interaction points (IP1, IP2, IP5, and IP8) locating four main particle detectors. These four particle experiments refer to A Toroidal LHC ApparatuS (ATLAS), A Large Ion Collider Experiment (ALICE), Compact Muon Solenoid (CMS), and Large Hadron Collider beauty (LHCb). (After O. Brüning, et al. [1].)

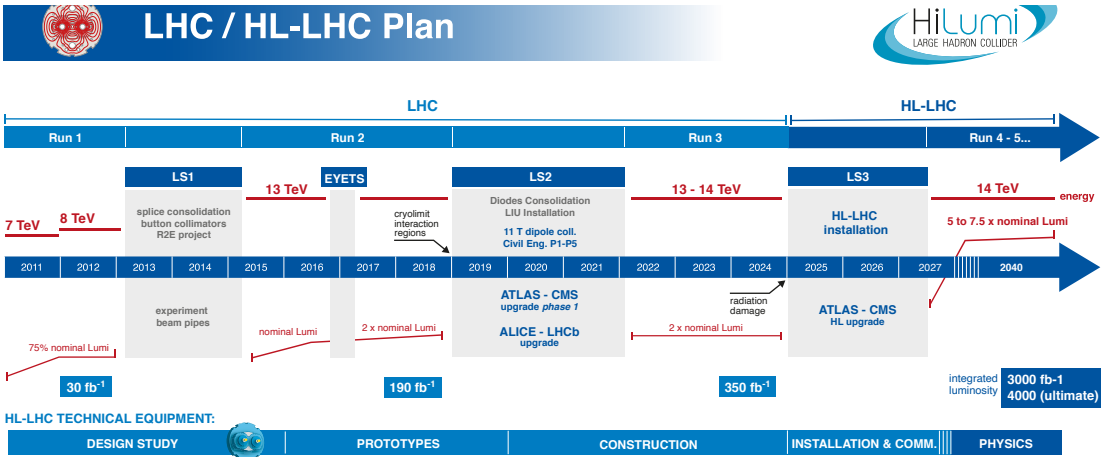
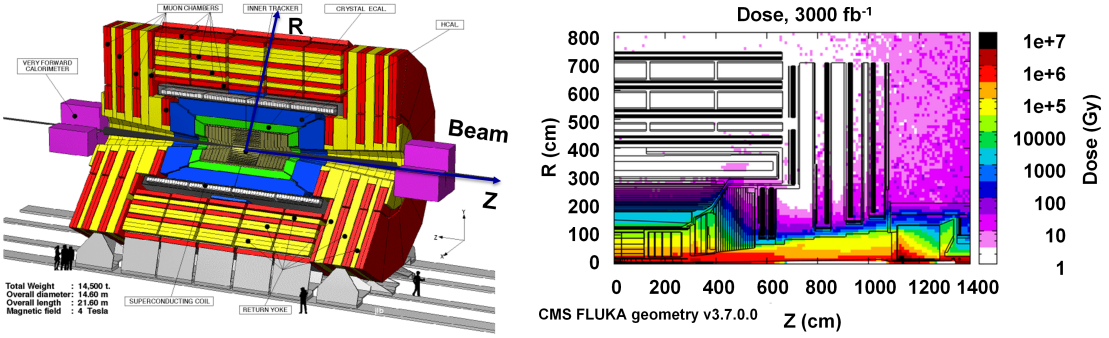


Figure 1.2 – Upgrade plan from the LHC to the High Luminosity LHC (HL-LHC). (After CERN [3].)

including A Toroidal LHC ApparatuS (ATLAS), A Large Ion Collider Experiment (ALICE), Compact Muon Solenoid (CMS), and Large Hadron Collider beauty (LHCb), for detecting and reconstructing collision processes. This powerful machine, attracting a global user community of more than 7,000 scientists spanning more than 60 countries, has been exploring the high-energy frontier since 2010, as summarized along its historical path in Fig. 1.2 [3]. After around one year of operation in July 2012, the ATLAS and CMS experiments had announced the first major discovery: the long-sought Higgs boson, the cornerstone of the Standard Model of particle physics [4]. This announcement heralded a giant leap in understanding our world and the origin of the universe.

To maintain the discovery potential of the LHC and explore its full capacity in high-energy physics (HEP) research, the LHC will receive a significant upgrade in the 2020s for an almost tenfold increase in the integrated luminosity from the first 10-year accumulation of 350 fb^{-1}* to an astonishing threshold of 3000 fb^{-1} and even 4000 fb^{-1} over 10-12 years of extended operation [3, 5, 6]. This groundbreaking machine would provide more accurate measurements of new particles and enable observation of rare events that occur below the current sensitivity level. It would allow scientists to explore a new energy frontier, pushing the limit of human knowledge. To produce more than 250 fb^{-1} of data per year, the peak instantaneous luminosity needs to be increased from 2×10^{34} $\text{cm}^{-2}\text{s}^{-1}$, which has been realized during the second run, to 5×10^{34} $\text{cm}^{-2}\text{s}^{-1}$ and even 7.5×10^{34} $\text{cm}^{-2}\text{s}^{-1}$ [6, 7]. Such a high luminosity will rely on many innovative technologies, including cutting-edge superconducting magnets for beam concentration, compact and ultra-precise superconducting radio-frequency (RF) crab cavities for beam rotation, new technology and physical processes for beam collimation, and 300-m superconducting links with zero energy dissipation [8,9]. Based on the new schedule in Fig. 1.2, some components have started to be installed during the second long shutdown (LS2) between

*The inverse femtobarn fb^{-1} is the conventional unit of the integrated luminosity ($1\,\text{fb} = 10^{-43}\,\text{m}^2$), measuring the number of particle collision events per target cross-section over a given period.



(a) Cross section.

(b) Dose distribution.

Figure 1.3 – Simulated total dose distribution over the cross section of the CMS experiment at an integrated luminosity of 3000 $^{-1}$, where R is the transverse distance from the beamline in the center of the experiment and Z is the distance along the beamline from the collision point. (After Schmidt [8].)

2019 and 2021, while most of the required equipment and major experiment upgrades will be installed during the third long shutdown (LS3) between 2025 and mid-2027.

The new machine, named High Luminosity LHC (HL-LHC), will generate many more collisions and accumulate ten times more data than the LHC. Meanwhile, the number of pileup events per bunch crossing at an instantaneous luminosity of 5×10^{34} cm^{-2}s^{-1} is expected to be around 150 and up to 200 [6–8]. This will result in a ten times higher average detector occupancy, which falls beyond the design parameters of the present detectors and trackers and is a challenge for their trigger and data acquisition systems. Also, energetic particles emerging from the huge amount of collisions can interact with electronic materials they pass through and even induce nuclear interactions that add cascades of energetic particles to the radiation load, damaging onboard electronics. The forthcoming HL-LHC is anticipated to experience unprecedented radiation levels up to 1 Grad* of total ionizing dose (TID) with an average dose rate of ~0.3 Mrad/d (12.5 krad/h = 208.3 rad/s) and 10^{16} neutrons/cm^2 of hadron fluence in the MeV range of energy. As simulated for the CMS experiment in Fig. 1.3, the total dose at an integrated luminosity of 3000 fb^{-1} ranges from 100 Mrad at a certain distance away from the collision point to 1 Grad in the innermost electronics [8]. Such high TID levels can seriously deteriorate the functionality of these electronics, including analog amplifiers, filters, analog-to-digital converters, and application-specific integrated circuits (ASICs). To fully exploit the increased amount of data under such a harsh radiation environment, the HL-LHC will require brand new high-performance radiation-tolerant detectors and trackers.

*The unit rad in the centimeter-gram-second (CGS) system of units measures the absorbed total dose with 1 rad = 100 erg/g = 6.24×10^{13} eV/g, where erg is a unit of energy with 1 erg=100 nJ and eV is the electronvolt with 1 eV=1.602×10^{-19} J. Since the absorbed total dose depends on solid targets and silicon dioxide (SiO_2) has been widely used as an important isolation material, the unit in this dissertation, rad, is an equivalent dose referred to SiO_2, unless indicated otherwise. The unit gray (Gy) is a derived unit of the absorbed total dose in the International System (SI) of Units. One gray is defined as the absorption of one joule of radiation energy per kilogram of matter (1 Gy = 1 J/kg = 10^4 erg/g). The units rad and Gy are linked through 1 rad = 0.01 Gy.

The higher detector occupancy and the harsher radiation environment imply major changes to today's particle detecting and tracking systems in the LHC. The present read-out channels (ROCs) were designed to perform at a spatial resolution of ~10 μm with hit rates up to 200 MHz/cm^2 and the current inner detectors were made to sustain radiation levels up to 100 Mrad of TID and 10^{14} neutrons/cm^2 of hadron fluence. These specifications are much more stringent than those for any other applications, such as space facilities and nuclear reactors, but still cannot meet the crucial requirements of the future HL-LHC. Moreover, today's silicon detectors and trackers in the LHC, especially their sensors and front-end (FE) electronics, would undergo serious performance degradation by the scheduled upgrade. Because of all these factors, CERN has decided to replace the entire detecting and tracking systems with new alternatives for an extended detecting capacity and an enhanced radiation tolerance. The future ROCs should perform at a much smaller spatial resolution down to ~1 μm with hit rates up to 2 GHz/cm^2. The upgraded inner detectors should be able to withstand much higher radiation levels up to 1 Grad of TID and 10^{16} neutrons/cm^2 of hadron fluence.

For long-term reliable operation, the future upgrade of the HL-LHC experiments will therefore require the development of innovative detectors and trackers with a higher level of granularity and bandwidth as well as robust radiation-tolerant FE electronics [6–9]. To achieve such stringent goals, it is of utmost importance to select the most appropriate complementary metal-oxide-semiconductor (CMOS) technologies because both device performance and radiation hardness are strongly process dependent. Fig. 1.4 summarizes the evolution of the minimum feature size of CMOS technologies since 1997 and the activities of radiation tolerance evaluation for CERN's particle experiments [10]. CMOS technologies have entered the nanoscale regime with the incorporation of new electronic materials and device structures, allowing extended circuit functionality with a higher chip density and enhanced computing power with a higher operation speed [10–13]. This can be seen in Fig. 1.5 from the increasing transistor density and the growing microprocessor clock frequency [13]. Moreover, the

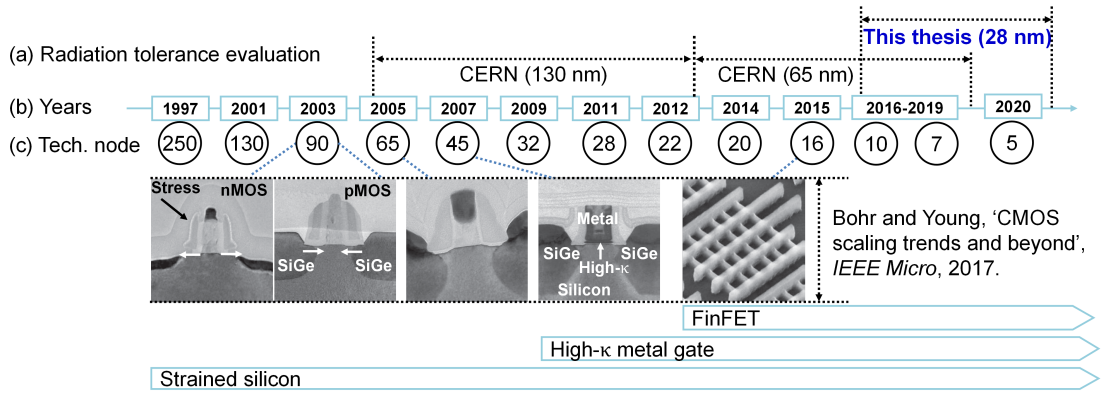


Figure 1.4 – (a) Radiation tolerance evaluation for CERN's particle experiments along with (c) the minimum feature size scaling of complementary metal-oxide-semiconductor (CMOS) technologies over (b) years. Transmission Electron Microscopy (TEM) pictures are from [10].

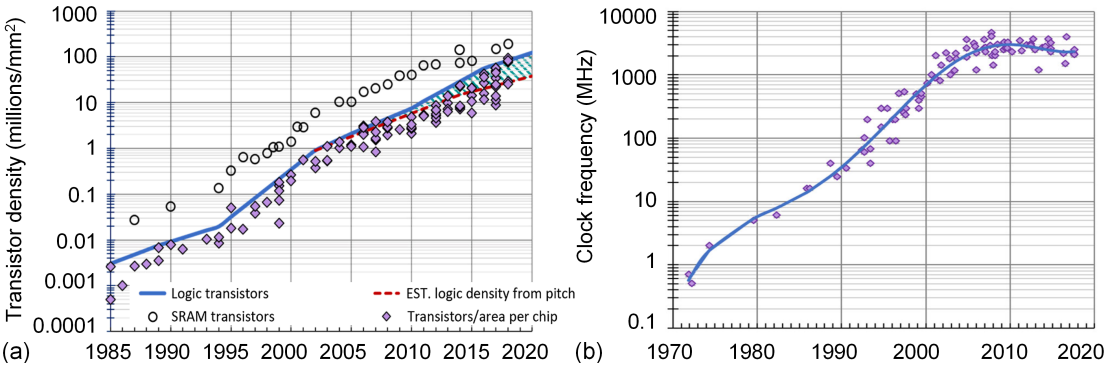


Figure 1.5 – Evolution of (a) the transistor density and (b) the microprocessor clock frequency over years. (After Rieger [13].)

continuous downscaling of CMOS technologies generally goes in the direction of improving the total dose tolerance with thinner dielectric materials [14, 15]. Therefore, CERN has been applying advanced commercial CMOS technologies with dedicated design techniques for its microelectronic components.

The majority of current electronics in the LHC experiments were designed with a commercial 250-nm bulk CMOS process using sophisticated techniques at design and layout levels [16, 17]. Aiming at guiding circuit designers to make optimal choices for the future upgrade of the LHC, CERN has intensively evaluated the radiation tolerance of commercial 130-nm and 65-nm bulk CMOS processes [18–21]. With the perspective of evaluating the potential use of further downscaled devices in particle experiments and providing predictable models for radiation-tolerant circuit design, this thesis investigates the effects of TID up to 1 Grad on a commercial 28-nm bulk CMOS process. When launching this research, it was the most advanced commercial CMOS process available at Europractice, i.e., a consortium of five renowned European research organizations, and expected to be more radiation tolerant. It should also be able to provide a higher bandwidth that can be exploited for the upgrade of CERN's particle experiments.

1.2 State of the art

1.2.1 Overview of radiation effects on solid-state electronics

Solid-state electronics operating under radiation environments are exposed to energetic particles. When such irradiating particles strike the electronics, they can modify the properties of electronic materials, alter the nominal response of microelectronic devices, and even induce circuit failures. The investigation of radiation effects on microelectronic devices and ICs has been widely carried out since the 1960s [22–26], mostly following the catastrophic loss of seven satellites after the high-altitude nuclear weapon tests of the USSR and the USA in 1962 [27]. Among those seven satellites, the communication satellite Telstar I was

launched one day after the explosion of the Starfish Prime device by the USA and failed after a few months of operation [28, 29]. One of its redundant command decoders first operated intermittently and then a malfunction occurred to its control system. It is believed to be a result of ionizing radiation damage of Starfish-generated excessive electrons to certain bipolar junction transistors (BJTs). Since then, energetic particles have often been seen temporarily or permanently compromising the normal operation of devices, circuits, and systems under harsh radiation environments [30]. Radiation effects have been identified as serious threats to electronic components, especially those working in HEP experiments [8, 9], space and avionic systems [31, 32], nuclear power plants [33, 34], and medical diagnostic imaging and radiation therapy equipment [35]. Even electronics in our daily life may not be exempt from the effects of energetic particles at ground level and radioactive contaminants in chip packaging materials [36–38].

To better understand radiation damage mechanisms and further support relevant radiation hardening, researchers have been continuously making efforts to characterize all kinds of devices, especially MOS field-effect transistors (MOSFETs) that have become the most common electronic components in solid-state electronics, under specific radiation environments [25, 39–46]. There are a variety of radiation sources, such as solar activities, nuclear explosions, fission reactions, microelectronic processes, and particle collisions [30]. These radiation sources give rise to three major groups of irradiating particles: photons (X-rays and γ-rays), charged particles (electrons, protons, alpha particles, and heavy ions), and neutrons. Depending on the properties of incident particles, the radiation energy can be partly or fully transferred to solid targets through ionizing or non-ionizing interactions [47]. Non-ionizing processes dislodge atoms, causing total displacement damage (TDD), while ionizing processes

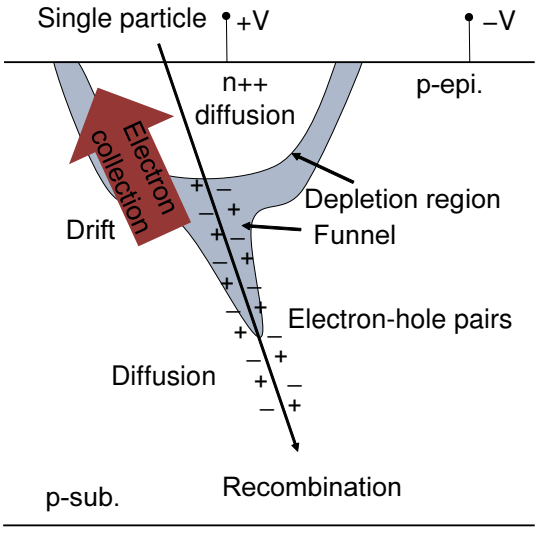


Figure 1.6 – Illustration of charge collection mechanisms that result in single-event upsets. (After Srour and McGarrity [25].)

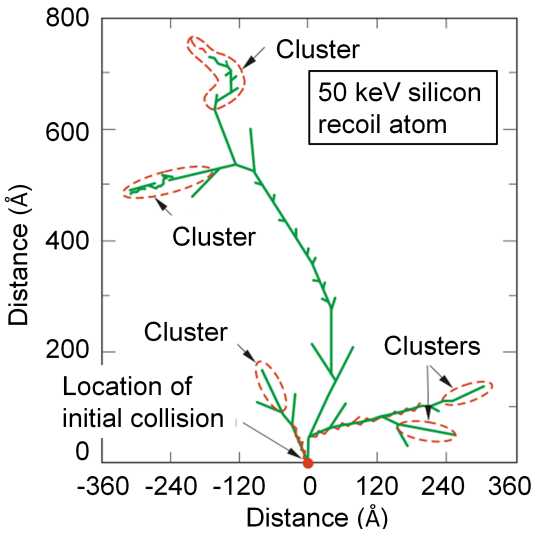


Figure 1.7 – Displacement cascade damage calculated from a theoretical model. (After van Lint, et al. [39].)

generate excessive carriers, inducing single event effects (SEEs) or total ionizing dose (TID) effects. The historically foundational work has uncovered three types of radiation effects:

- SEEs, which involve a single energetic particle striking a sensitive node and as exhibited in Fig. 1.6, generation of excessive charges along the particle penetration track [25]. These excessive charges can induce non-destructive effects (i.e., soft errors, such as single-event upsets, single-event interrupt, and single-event transients) [38, 48, 49] and even destructive effects (i.e., hard errors, such as single-event latch-up, single-event burnout, and single-event dielectric/gate rupture) [50–52]. As the technology node scales down, the area of a MOSFET sensitive to an energetic particle hit decreases while the critical charge required for single-event upsets to occur gets smaller [53]. Investigating the result of this completing effect and new important single-event players like multiple-bit upsets is getting important in advanced CMOS technologies but beyond the scope of this thesis.

- TDD effects, which belong to total non-ionizing dose (TNID) effects. They involve displacement of atoms from their lattice positions and as presented in Fig. 1.7, generation of isolated defects or defect clusters in bulk semiconductors [39, 54, 55]. The most sensitive semiconductor parameter to TDD is the minority carrier lifetime. It is critical for devices relying on volume carrier conduction, such as PN diodes, PIN diodes, BJTs, solar cells, active pixel sensors, charge-coupled devices (CCDs), and many other types of optoelectronic devices. CMOS technologies are largely immune to TDD since the conduction of MOSFETs occurs only at a tiny region close to the surface of the channel.

- TID effects, which involve radiation-induced charge generation, recombination, transport, and trapping over time. They lead to fully or partly recoverable device degradation and even circuit failures [40–46]. Telstar I's failures actually launched decades of studies

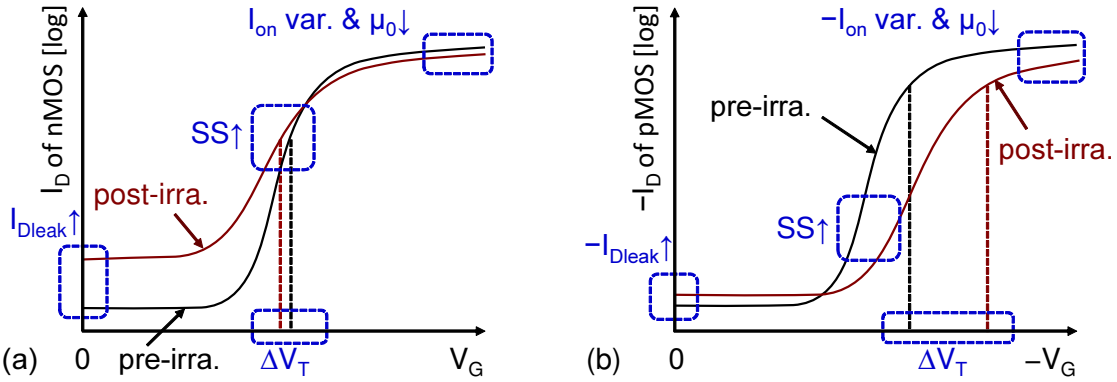


Figure 1.8 – Basic total ionizing dose (TID) effects on transfer characteristics ($|I_D| - |V_G|$) of n- and p-types of MOS field-effect transistors (MOSFETs), including variations of the drain leakage current I_{Dleak}, the threshold voltage V_T, the subthreshold swing SS, the low-field channel mobility μ_0, and the drive current I_{on}.

on TID effects. Hughes and Giroux initially investigated TID effects on MOS structures in 1964 [23]. Together with the work of Hughes and Kooi in [56, 57], key underlying physical mechanisms of TID effects have been uncovered: charge buildup in dielectrics and activation of hydrogen (H)-passivated interface traps. Oxide- and interface-charge trapping generally influences DC characteristics of a MOSFET through modifying critical device parameters, such as the drive current, the threshold voltage, the low-field channel mobility, the subthreshold swing, and the drain leakage current, as illustrated in Fig. 1.8. It has always been crucial to study the effects of TID on microelectronic devices, which is the focus of this thesis.

1.2.2 Overview of TID effects on nanoscale MOSFETs

The effects of TID on MOSFETs have been under investigation in parallel with the minimum feature size scaling of CMOS technologies to submicron during the 1980s-1990s [59, 60], deep-submicron during the 1990s-2000s [17, 18, 61], and nanometer nowadays [20, 62–66]. A large body of previous work has uncovered that TID-induced charge trapping is related to dielectric materials, such as the gate oxide, spacers, and isolation dielectrics, and their interfaces with the semiconductor body [41, 43], as shown in Fig. 1.9 for a generic deep-submicron bulk CMOS process [58]. In addition, there is also the buried oxide in silicon-on-insulator (SOI) MOSFETs, especially fully-depleted SOI (FDSOI) MOSFETs, contributing additional TID susceptibility [66, 67]. Bulk MOSFETs have been found more tolerant to TID than their SOI counterparts [68]. Among all dielectrics and their interfaces with the semiconductor body, the dominant contributors demonstrate a strong dependence on fabrication processes, device dimensions, and radiation levels.

The evolution of gate-oxide-related TID effects along with Moore's law scaling is summarized in Fig. 1.10 [45]. In addition to the increased computing power and the extended circuit functionality, CMOS scaling also reduces the gate-oxide thickness and increases the channel

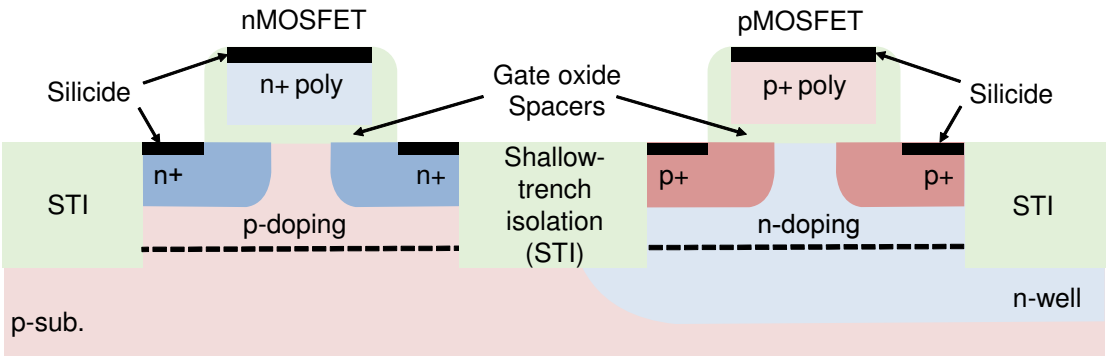


Figure 1.9 – Cross section of an *n*MOSFET and a *p*MOSFET from a generic deep-submicron bulk CMOS process, highlighting the gate oxide, spacers, and shallow trench isolation (STI) oxides. (After Taur and Ning [58].)

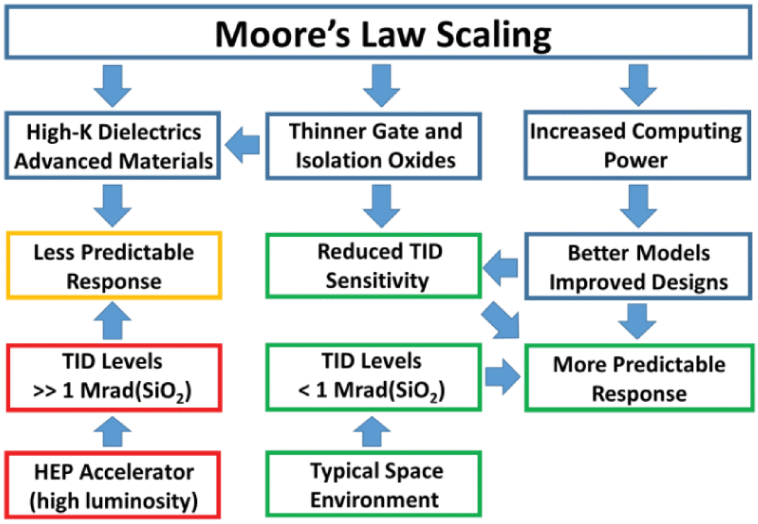


Figure 1.10 – Schematic illustration of the effects of Moore's law scaling on ionizing radiation response of MOSFETs. (After Fleetwood [45].)

doping concentration. Both factors potentially improve the inherent TID tolerance of advanced CMOS technologies. Especially, thanks to the first-order effect of gate-oxide-thickness scaling [14, 15], highly scaled CMOS technologies may inherently get rid of gate-oxide-related TID effects [18–21]. TID effects have become much less problematic for high-performance CMOS technologies at dose levels typical of space applications (<1 Mrad), as compared in Table 1.1 [8,16,29,30,69]. However, high-κ dielectrics, i.e., materials with high dielectric constants and often referring to hafnium dioxide (HfO_2), have been introduced into MOSFETs since the 45-nm technology node, as depicted in Fig. 1.4, to resolve the gate leakage issue of ultra-thin SiO_2-based gate dielectrics [70–72]. This can make the radiation response of nanoscale MOSFETs less predictable. The effects of TID on advanced high-κ metal-gate (HKMG) stacks remain to be further investigated [64, 65, 73, 74]. Besides, CERN's studies on 65-nm bulk CMOS processes demonstrate unexpected interferences of spacer-related charge trapping with the normal operation of short-channel MOSFETs [20, 21, 75]. Efforts should also be made to assess if similar phenomena occur to even further downscaled MOSFETs with new dielectric materials.

Recently published work on CMOS technologies from 180 nm to 65 nm has presented a considerable influence of TID-induced charge trapping related to thick shallow trench isolation (STI) oxides [19,20,61]. The dominant effects of STI-related charge trapping are the generation of a parasitic drain-to-source leakage current through opening parasitic conduction paths along channel edges [19, 59] and the performance degradation of narrow-channel MOSFETs through new narrow-channel effects [19, 20, 61]. Total ionizing radiation damage to thick dielectrics of two commercial 180-nm bulk CMOS technologies have been systematically investigated in [76] using dedicated test structures. It highlights that STI and pre-metal dielectrics trap radiation-induced charges quite differently from the thermally-grown gate oxide

Table 1.1 – Ionizing radiation levels for harsh radiation environments [8, 16, 29, 30, 69]

Radiation environments	Ground level	Satellites	LHC	HL-LHC
TID levels (rad)	–	10^3–10^6	80×10^3–30×10^6	10^6–10^9
Dose rate (rad/d)	$\leq10^{-3}$	10^{-3}–10^0	$\sim9\times10^3$	$\sim0.3\times10^6$

and STI oxides from two processes have large variations in TID-induced charge trapping. This evidences the strong influence of semiconductor material processing on the radiation response of MOSFETs. In addition to the way of fabricating STI structures, substrate doping profile has also proved to be a crucial factor for STI-related TID effects [77–79]. This strong dependence on CMOS processes increases the importance of investigating STI-related TID effects continuously from foundry to foundry and from technology to technology.

The total amount of radiation that an electronic component encounters during its life-cycle strongly depends on its electronic materials and working conditions. Among all harsh radiation environments, as partly summarized in Table 1.1, the LHC at CERN, and its future upgrade, the HL-LHC that should be operational in 2027, are expected to face by far the highest levels of TID. The extremely high TID levels foreseen for the future HL-LHC may seriously compromise device performance and even cause function failures by different degradation mechanisms, some of which may only appear at ultrahigh TID levels. However, most qualification processes, which have been designed for electronics working under much lower TID levels such as in space missions and nuclear facilities, may not suit the assessment of long-term degradation of HEP experiments. Only a few papers have been dedicated to the effects of ultrahigh TID levels, typically up to a few hundred Mrad [19, 66, 80]. Since 2012, quite some tests have been carried out at CERN on 65-nm bulk MOSFETs until 1 Grad of TID [20, 21, 75, 81]. Results of 65-nm bulk MOSFETs can serve as favorable references for the qualification of the 28-nm bulk CMOS process and the experimental analysis of measurement results.

1.2.3 Modeling of TID effects on nanoscale MOSFETs

Even though the intrinsic TID tolerance of nanoscale CMOS technologies can be high enough to meet the radiation requirements of most applications without any hardening effort, HEP experiments that usually experience much higher TID levels still require a careful design of their detecting and tracking systems. In general, radiation hardness assurance (RHA) involves 1) assessing radiation threats and their severity for the mission, 2) evaluating the radiation influence on targeted CMOS technologies, and 3) developing mitigation strategies to meet particular radiation requirements. This is compatible with the RHA approach of NASA presented in [82] for space missions. Since the radiation environment for HEP experiments has been well understood and defined, most RHA efforts will be made during step 2 and 3. Step 2 uncovers fundamental damage mechanisms of the radiation levels of interest for solid-state electronics. For components at risks of failing the specific radiation requirements, designers can harden them in step 3 by following two primary methods:

- Radiation-hardness-by-process (RHBP) using specialized manufacturing techniques, with which foundries have successfully supplied radiation-hardened components for space applications. RHBP has potential issues with product availability, process stability, and chip yield [84–86];
- Radiation-hardness-by-design (RHBD) using specialized layout (edgeless transistors, guard rings, etc.) and/or circuital techniques (triple modular redundancy, error-correcting code memory, etc.) to mitigate radiation effects on a commercial CMOS technology with a sacrifice of the chip area [16, 86–90]. However, due to the constraints of stringent design rules, some popular RHBD techniques, such as edgeless transistors, known also as enclosed-layout transistors (ELTs), have been rendered infeasible in some ultrascaled CMOS technology nodes [91].

Since commercial CMOS technologies generally aim at a broad range of applications at ground level, CMOS associated models, parameter extraction methodologies, and circuit design techniques are typically customized for normal working environments. This is perhaps the reason why, even though a lot of efforts have been invested in understanding the underlying physics of radiation effects, relatively little has been done in incorporating them into computer-aided design (CAD) frameworks. The effects of incident radiation are still absent from the industry-standard process design kits (PDKs), such as the traditional Berkeley Short-channel Insulated-gate FET (IGFET) Model 4 (BSIM4) that has been used for technology nodes down to 28 nm and its latest successor, the BSIM6 compact model [83, 92] that is fully scalable with geometry, bias, and temperature [93–95]. BSIM6, which has been developed especially

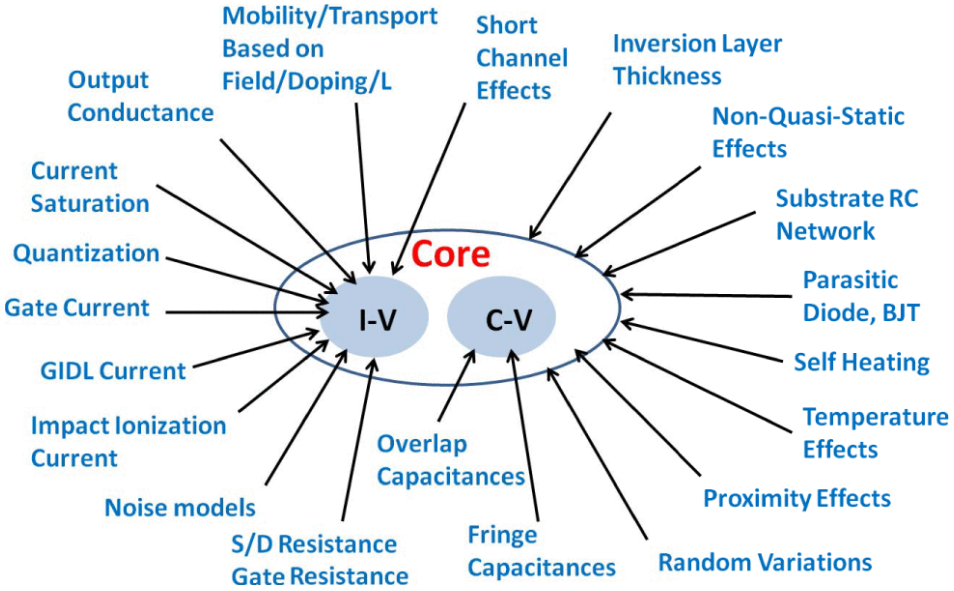


Figure 1.11 – Berkeley Short-channel Insulated-gate FET (IGFET) Model 6 (BSIM6) bulk MOSFET compact model composed of a charge-based core model and models of non-ideal effects. (After Chauhan, et al. [83].)

for analog and RF IC design, employs the Enz-Krummenacher-Vittoz (EKV) charge-based MOSFET model [96] as its core long-channel part, while models of non-ideal effects are taken from BSIM4. From Fig. 1.11, which summarizes all device effects that have been built into BSIM6, it is clear to see that radiation effects have not yet been implemented [83]. Design tools without accounting for radiation effects cannot help designers well predict the radiation response of their design ahead of time. To ensure the required radiation tolerance, an iterative process of step 2 and 3 usually takes place, which demands repetitive and expensive testing, analysis, and mitigation through trial and error [82, 97].

Implementing radiation effects into design environments enables designers to predict the radiation response of their design before fabrication. This can be helpful for reducing the number of iterations between step 2 and 3, alleviating the cost of time and expense for radiation-tolerant circuit design. To do so, highly accurate models should first be developed to account for the observed radiation effects. One option is treating critical radiation effects as additional circuit elements [98, 100, 101]. For example, Huang et al. [98] have proposed a TID-controlled variable resistor, which also performs as a gate-controlled switch, to represent the TID-induced parasitic drain-to-source leakage current in parallel with the original MOSFET model, as shown in Fig. 1.12. However, to be more intuitively predictive, models should better reflect the underlying physical mechanisms. It is then of great interest to develop physics-based models that can be implemented into commercial design environments or a simple physics-based compact model that can be used for circuit simulations independently [102]. The physics-based modeling approach is also advantageous from the perspective of circuit design since it provides better control over essential design parameters and does not require the modification of circuit schematics. Moreover, once radiation-aware physics-based models are obtained and implemented, parameter extraction methodologies and MOSFET characteristic calibrations can be defined and even extended for new CMOS technologies simply by updating model cards.

Nowadays, the radiation-enhanced modeling work is still in the phase of model development

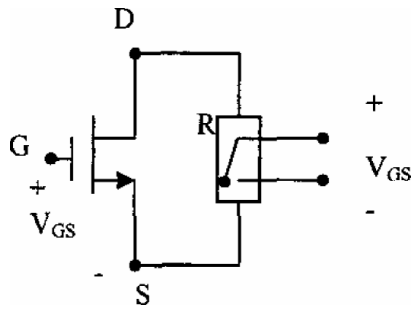


Figure 1.12 – Circuit schematic of a MOSFET with a TID-controlled variable resistor representing the TID-induced drain leakage current. (After Huang, et al. [98].)

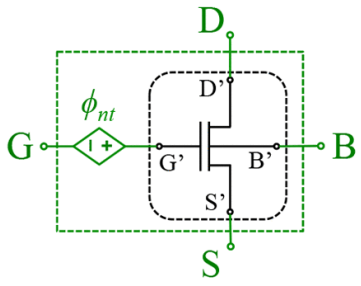


Figure 1.13 – Circuit schematic of a MOSFET with a voltage-controlled voltage source modeling the TID-induced voltage shift. (After Esqueda and Barnaby [99].)

and most publications focus on older CMOS technologies as well as much lower TID levels [103, 104]. Esqueda et al. have proposed a physics-based compact model in [103] that incorporates TID-induced charge contribution into the surface-potential equation [99] and links the solved surface potential to the drain current through a charge-sheet model [105, 106]. As depicted in Fig. 1.13, the derived TID-induced voltage shift is implemented as a voltage-controlled voltage source, which is compatible with standard design tools and existing MOSFET compact models [99]. To simplify the surface-potential calculation, this model uses the technique of the surface-potential-based (PSP) MOSFET compact model [107]. However, the model calculation still involves intensive computations and the model validation stops at 1 Mrad with a 90-nm bulk CMOS process.

Despite the high TID tolerance with the shrunken gate oxide and the tremendously fast speed along with the channel length reduction, as seen in Fig. 1.14, CMOS scaling compromises the intrinsic gain, particularly for devices with the minimum length, and results in much lower voltage parameters, with the purpose of avoiding high-electric-field effects [11, 12, 96]. Most analog FE electronics include a charge amplifier in the first stage, converting the signal from charge to voltage for further processing [108]. A very low intrinsic gain of the amplifier together with increased parasitic capacitances limits the charge-to-voltage gain, making the gain conversion less accurate and poorly controlled. Considering the sufficiently high transit frequency, this drawback can probably be circumvented by not necessarily using the minimum channel length for keeping the intrinsic gain at a reasonable level.

The continuous drop in the nominal power supply resulting from CMOS scaling, which in turn leads to a much lower overdrive voltage, has progressively pushed the operating point of highly scaled MOSFETs from strong inversion towards moderate and even weak inversion [109]. This brings new challenges to circuit designers for making optimal trade-offs among design parameters and makes the simple threshold-voltage-based quadratic model, which has been

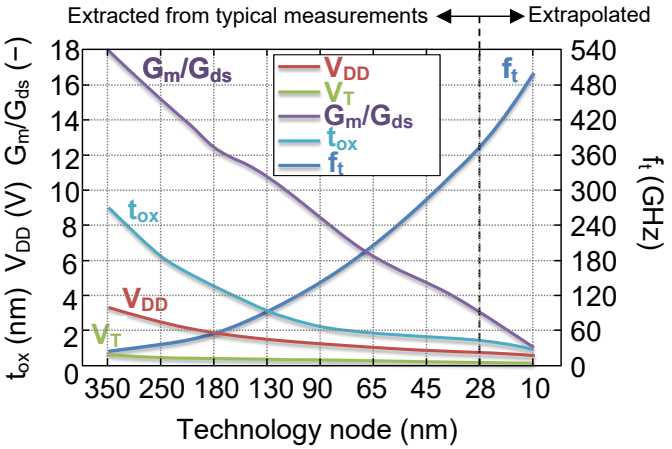


Figure 1.14 – Key device parameters, including the nominal supply voltage V_{DD}, the threshold voltage V_T, the intrinsic gain G_m/G_{ds}, the gate-oxide thickness t_{ox}, and the transit frequency f_t, versus CMOS generations. (After Ellinger, et al. [12].)

in use since the development of the MOSFET in the 1960s, no more valid [110–112]. The EKV MOSFET model, which is based on the inversion charge that is directly related to the gate transconductance and the drain current and describes device characteristics intuitively and physically [96]. This charge-based MOSFET model and the concept of inversion coefficient have demonstrated their effectiveness in describing large- and small-signal characteristics of nanoscale MOSFETs in all inversion conditions [110, 111, 113–115].

Except for the charge-related basis, the EKV MOSFET model has two other important features: simplicity and universality. The EKV MOSFET model employs only a few parameters and much simpler formulas [96, 114, 115]. This simplicity makes it advantageous for designers to explore the design space and identify the optimal operation before running more accurate simulations with the full PDKs. The EKV MOSFET model can also be fully normalized with its model parameters, which carry important technological information. Thus, the dependence on voltage, temperature, and technology can be stripped off from the model, making it suitable as a benchmark for CMOS technologies. These two features can be attractive for radiation-tolerant circuit design with nanoscale CMOS technologies. Some publications have made use of the existing BSIM or EKV compact model for investigating TID effects on 180-nm and 65-nm CMOS processes [104, 116, 117]. To better pinpoint crucial radiation damage mechanisms for nanoscale MOSFETs and finally support radiation-tolerant circuit design with nanoscale CMOS technologies, the modeling part of this thesis introduces the effects of TID on the 28-nm bulk CMOS process into the EKV MOSFET model.

The model development with the EKV MOSFET model could be done by adjusting the values of existing model parameters without changing the model equations, as previous work has done in [104, 116, 117]. However, it would probably be burdensome to extend the experimentally validated model to device sizes and TID steps that are not involved. In this case, circuit design would probably be limited to a certain range of devices for specific TID levels. Alternatively, the model development could rely on the introduction of radiation-related parameters directly into the model equations and the automatically generated link between radiation-related parameters and existing device parameters. The model extension would then simply be done through modeling radiation-related parameters as a function of device sizes and TID levels. Thus, the final model would allow designers to predict the radiation response of their design with a broad range of devices for the TID levels of interest. As the first step of characterizing TID effects on design parameters, this thesis applies the first option. Through the second approach, this thesis brings the eventual design-oriented compact model for supporting radiation-tolerant circuit design. Specific radiation requirements could finally be satisfied with dedicated design techniques using the radiation-aware EKV MOSFET model.

1.3 Goals and approach

The goals of this thesis are to evaluate the radiation tolerance of a commercial 28-nm bulk CMOS process for its potential use in the future HL-LHC and to develop radiation-aware

physics-based models of the observed radiation effects for supporting radiation-tolerant circuit design. One main focus is pinpointing important underlying physical processes that influence the normal device operation. This relies on performing and analyzing a comprehensive set of electrical measurements. The other is incorporating TID effects into the original EKV charge-based MOSFET model and extending the proposed model to a broad range of device dimensions for the TID levels of interest. The ultimate goal is to provide a radiation-aware design-oriented compact model so that circuit designers can predict the radiation response of their design before fabrication and explore the robustness of their design up to ultrahigh TID levels. The outcome aims at supporting but not limited to the future upgrade of the HL-LHC at CERN.

To better interpret experimental results, Chapter 2 presents a brief description of basic physical processes of TID effects on MOS structures, including ionizing interaction of incident energetic particles with electronic materials, radiation-induced electron-hole pair generation, hopping transport of remaining holes in the oxide bulk, deep hole trapping and annealing, and radiation-induced activation of H-passivated interface traps. Extending from gate-oxide-related physical processes, this chapter then summarizes the effects of CMOS scaling on the radiation response of MOSFETs together with a brief overview of STI- and spacer-related TID effects.

Chapter 3 enters the important characterization part of this thesis. It first introduces experimental details that relate the majority of measurement results, including test structures, experimental setup, and measurement protocol. The radiation response of 28-nm bulk MOSFETs are then intensively studied through an investigation of altered device parameters and post-irradiation annealing effects under various bias and temperature conditions. Finally, main experimental observations, including the TID-induced drain leakage current and the geometry dependence of TID effects, are addressed. This chapter mainly covers results published in [118–121].

Chapter 4 focuses on investigating the effects of TID on design parameters of 28-nm bulk MOSFETs and introducing the first attempt of modeling the observed radiation effects. The simplified EKV MOSFET model is first employed to study the effects of TID on analog parameters and to model the effects of TID on static characteristics. The effects of TID on the effective channel mobility is then investigated using the Y-function-based mobility extraction method. One of the primary TID effects on 28-nm bulk MOSFETs, the TID-induced drain leakage current, is finally investigated in detail through a comprehensive study of measurement results, semi-empirically modeling of the drain leakage current versus TID levels, and charge-based modeling of the parasitic drain-to-source leakage current via a gateless charge-controlled device. This chapter mainly covers results published in [122–124].

Chapter 5 summarizes main activities on charge-based physical modeling of TID effects on 28-nm bulk MOSFETs. The key idea is to introduce oxide- and interface-trapped charges into the original EKV MOSFET model. The crucial step is validating the inversion charge

linearization in the presence of oxide and interface traps for a generalized EKV MOSFET model. Following model validation with radiation measurements on 28-nm bulk MOSFETs, the effects of TID on the channel mobility and the effective channel width are further considered, leading to a design-oriented compact model that comprehensively accounts for the observed radiation effects. The newly-developed radiation-aware compact model demonstrates a width-dependence feature of TID effects on this 28-nm bulk CMOS process. It allows the modeling work to be extended to a broad range of devices even for a continuous range of TID levels. This chapter covers results published in [125, 126] and recent results for one future publication [127].

Chapter 6 summaries the results of this thesis about the radiation tolerance of this specific 28-nm bulk CMOS process and the modeling progress of TID effects on nanoscale MOSFETs. It also presents general remarks about this work and provides suggestions for future work.

The work in this thesis has been carried out within the GigaradMOST project funded by the Swiss National Science Foundation (SNSF) under grant number 200021_160185, in collaboration with the Electronics Systems for Experiments (ESE) Group of the Experimental Physics (EP) Department (EP-ESE group) at CERN and the ScalTech28 project funded by the Istituto Nazionale di Fisica Nucleare (INFN) involving University of Padova and University of Milano-Bicocca. Most results and discussions have been published in journals and conferences and recent results are in preparation for one future publication, as summarized in the list of publications.

2 Basic mechanisms of TID effects on MOS devices

When irradiating particles strike solid-state electronics, they can partly or fully transfer their energy to the target materials [30]. Non-ionizing processes dislodge atoms from their original lattice sites, causing TDD effects, while ionizing processes produce excessive electron-hole pairs in semiconductors and dielectrics, inducing SEEs and TID effects, respectively [24]. Both ionizing and non-ionizing processes can modify the properties of electronic materials, alter the nominal response of microelectronic devices, and induce functional failures of ICs. TID effects on MOS devices are associated with the ionization of dielectrics at sensitive device regions (such as the gate oxide, spacers, and isolation materials) and the subsequent charge evolution in dielectrics and at their interfaces with the semiconductor body. In the form of charge trapping in oxide traps and at radiation-activated interface traps, TID eventually influences DC characteristics of a MOSFET mainly through altering its crucial device parameters.

According to gate-oxide-related charge trapping, this chapter first summarizes main concepts about basic underlying physical processes of TID effects on MOS devices. As reviewed in several books [24, 26, 40] and papers [41–46], most of previous publications have focused on gate-oxide-related TID effects, since the gate oxide has been one of the most vulnerable factors. However, the continuous scaling of CMOS technologies can improve the inherent TID tolerance of nanoscale MOSFETs with ultrathin gate dielectrics while making the effects of TID related to STI oxides and spacers more crucial. Based on basic principles of gate-oxide-related TID effects, this chapter then addresses the influence of Moore's law scaling on radiation-induced charge trapping related to different dielectric components. Unless stated otherwise in this thesis, the semiconductor and the gate oxide refer to silicon (Si) and silicon dioxide (SiO_2), respectively.

2.1 Photon interactions with solid targets

Radiation sources, such as solar activities, nuclear explosions, fission reactions, microelectronic processes, and particle collisions [30], give rise to three main categories of irradiating particles: photons (X-rays and γ-rays), charged particles (electrons, protons, alpha particles,

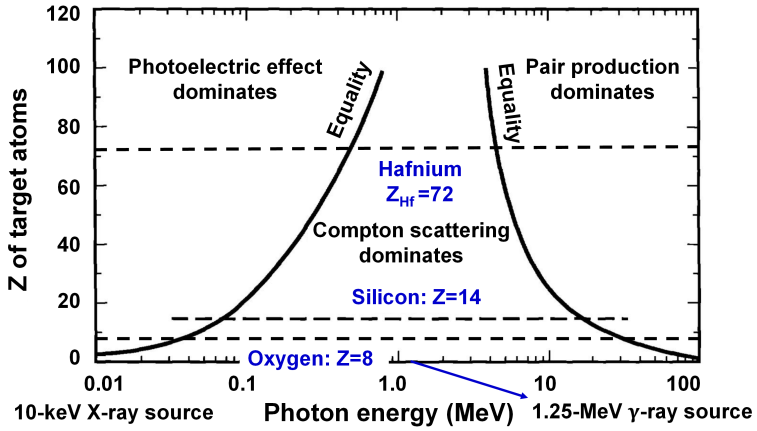


Figure 2.1 – Photon-matter interactions versus the atomic number and the photon energy. Solid lines correspond to equal cross sections for neighboring effects and dashed lines indicate three kinds of involved atoms. (After Evans [128].)

and heavy ions), and neutrons. High-energy radiation exposure primarily induces atomic displacement damage to electronic materials. Photons and low-energy charged particles passing energize valence electrons of electronic materials to the conduction band and leave their paired holes in the valence band, ionizing the solid targets and generating excessive electron-hole pairs.

Ionizing processes in electronic materials depend on many factors, such as 1) the mass, the charge state, and the kinetic energy of incident particles, and 2) the atomic mass, the atomic number, and the atomic density of solid targets [47]. As illustrated in Fig. 2.1, a photon can interact with a target atom through three possible processes: photoelectric effect, Compton scattering, and pair production, whose probabilities to occur are a function of the energy of incident photons and the atomic number of solid targets [24, 26, 128]. For hafnium ($Z_{\mathrm{Hf}} = 72$), silicon ($Z_{\mathrm{Si}} = 14$), and oxygen ($Z_{\mathrm{O}} = 8$), the photoelectric effect dominates at energies below 300 keV, 50 keV, and 30 keV, respectively, and the pair production gets critical at energies above 5 MeV, 20 MeV, and 30 MeV, respectively. Compton scattering plays a key role in the broad intervening energy region.

The most common radiation sources for laboratory radiation testing are low-energy X-rays at the peak of the spectrum density (10 keV) typically from an X-ray tube with a tungsten target and high-energy γ-rays typically at 1.25 MeV from cobalt-60 (^{60}Co) radioactive decay. Such low-energy X-rays interact with Hf, Si, and O atoms primarily through the photoelectric effect, as depicted in Fig. 2.2a [24, 26, 128]. In this case, the incident photon energy is completely absorbed by the target atom, which in turn releases a valence electron, called photoelectron, producing an electron-hole pair. If the incident photon energy is high enough to excite an electron from the K shell, i.e., the closest shell to the nucleus, most collisions would then happen with electrons there. Once a K-shell electron is liberated, an L-shell electron, which is from the external orbit of the K shell, will fall into the lower empty state either by emitting a

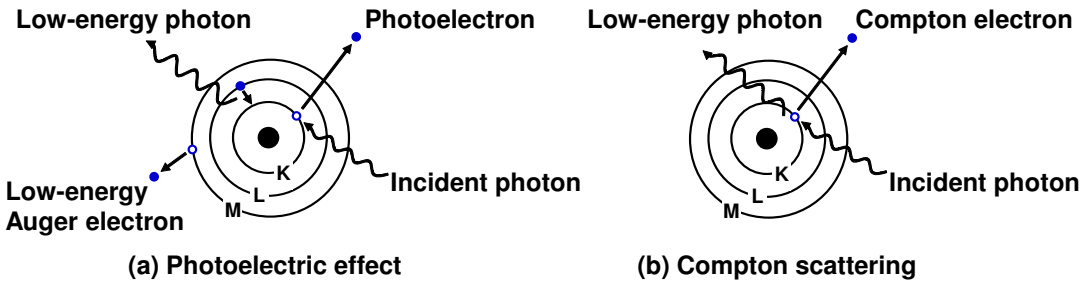


Figure 2.2 – Schematic representation of (a) the photoelectric effect and (b) Compton scattering.

characteristic photon or a low-energy Auger electron. In contrast, ^{60}Co γ-rays, which is the conventional standard radiation source for laboratory radiation testing, interact with Hf, Si, and O atoms predominantly through Compton scattering, as portrayed in Fig. 2.2b [24,26,128]. In this case, the photon energy is much greater than the binding energy of the valence electrons of these atoms and the incident photon does not lose its full energy within one strike. Along with the generation of the first Compton electron, the scattered low-energy photon continues to travel across the atomic neighborhood and generates more Compton electrons.

For both X-rays and γ-rays, the essential result of photon-matter interactions is a production of energetic secondary electrons. These electrons can be active enough to stimulate many other valence electrons and ionize many other atoms along their energy-losing paths, generating more electron-hole pairs than the direct interaction of the incident photons with the target atoms. Most of the final ionization occurs through a single type of intermediate processes involving collective movements of many valence electrons in a simple oscillatory motion against ionized atoms. These plasma vibrations or plasmons are correlated with the long-range nature of Coulomb interaction, which extends over adjacent regions through many atoms. For a Si atom, the binding energy of its K-shell electrons is around 1838.9 eV [129]. Once getting the full energy of 10-keV X-rays, these valence electrons can turn into secondary electrons. However, neither such low-energy X-rays nor the generated secondary electrons are energetic enough to significantly trigger non-ionizing processes. Displacement damage induced by such low-energy X-rays can therefore be considered negligible. However, ^{60}Co γ-rays are typically at the order of 1 MeV and this range of ionizing radiation can generate point or isolated defects, contributing to atomic displacement damage [55].

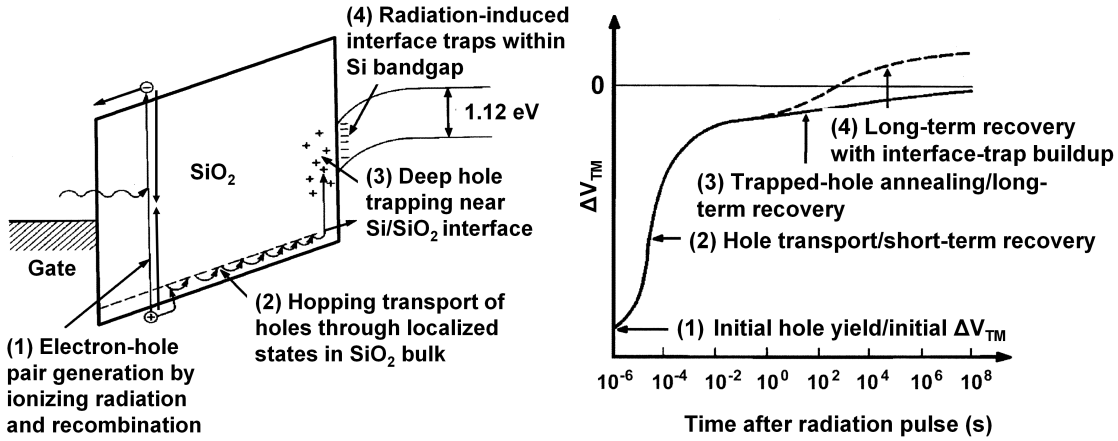
The total amount of radiation that dielectrics of an electronic component receive during its life-cycle is measured by total ionizing dose (TID). As explained in Section 1.1, both gray and rad are units of the absorbed total dose and the conversion of relevant units is summarized as $1\,\text{rad} = 0.01\,\text{Gy} = 100\,\text{erg/g} = 10^4\,\text{nJ/g} = 0.01\,\text{J/kg} = 6.24 \times 10^{13}\,\text{eV/g}$. Although the unit gray is one of the SI derived units, its equivalent unit rad from the CGS unit system is more often used in the space and particle physics communities. Therefore, the unit rad is used throughout the thesis for describing the total ionizing radiation level.

2.2 Basic physical processes of TID effects on MOS structures

Total ionizing radiation influences MOS devices through the following major physical processes:

- Electron-hole pair generation through the interaction of incident energetic particles with dielectrics and immediate recombination;
- Hopping transport of remaining holes through localized shallow trap states in dielectrics;
- Deep hole trapping in oxygen vacancies as well as reversible and permanent trapped-hole annealing;
- Radiation-induced activation of H-passivated interface traps.

Radiation-generated holes initially generate a maximum negative threshold voltage shift, which may shortly get relieved by hole hopping transport and gradually recovered by post-irradiation annealing. The long-term recovery of the threshold voltage shift usually happens with charge buildup at radiation-activated interface traps, which causes a positive threshold voltage shift for *n*MOSFETs and a negative threshold voltage shift for *p*MOSFETs. The band diagram of a p-substrate MOS capacitor under a positive gate bias in Fig. 2.3a and the time-dependent threshold voltage evolution of an *n*MOS device in Fig. 2.3b summarize these basic physical processes and relevant device behaviors [41]. Through the introduction of gate-oxide-related damage mechanisms, main concepts about TID effects on MOS devices are given in detail in the following subsections.



(a) Energy-band diagram of a p-substrate MOS capacitor under a positive gate bias.

(b) Illustration of the threshold voltage evolution of an *n*MOS device.

Figure 2.3 – Basic physical processes of TID effects on MOS structures, including radiation-induced charge generation, recombination, transport, and trapping. An *n*MOS device is taken as an example. (After Oldham and McLean [41].)

2.2.1 Electron-hole pair generation and recombination

Electron-hole pair generation and recombination are described together with their influence on device behaviors as step (1) in Fig. 2.3. When a MOS device is exposed to ionizing radiation, electron-hole pairs can be rapidly generated in the oxide bulk by the absorbed radiation energy. The average energy for creating an electron-hole pair E_p in SiO_2 has been determined to be (18 ± 3) eV [130] and (17 ± 1) eV [131]. As introduced in Section 2.1, one single particle may produce a shower of electron-hole pairs through its direct interaction with the target atom and the continuous energy transfer from secondary electrons to other atoms. The electron-hole pair density per unit volume per rad

$$g_0 = \frac{\frac{100\,\mathrm{erg}}{\mathrm{g{\cdot}rad}}\rho\left(\frac{\mathrm{g}}{\mathrm{cm}^3}\right)}{\frac{10^7\,\mathrm{erg}}{\mathrm{J}}\frac{1.6\times10^{19}\,\mathrm{J}}{\mathrm{eV}}E_\mathrm{p}(\mathrm{eV})} \tag{2.1}$$

is around 8.1×10^{12} pairs/[cm^3·rad] [24, 26, 132], where ρ is the density of the dielectric, i.e., SiO_2 here.

Since electrons are much more mobile than holes in SiO_2 [133–135], radiation-generated electrons will quickly drift away from generation points towards the gate electrode within picoseconds under a positive gate bias. The electron mobility in SiO_2 is around 20 cm^2/(V·s) at room temperature (300 K) and 40 cm^2/(V·s) at a low temperature (200 K) [133]. In contrast, the hole mobility is much lower, around 10^{-8} cm^2/(V·s) at 300 K and less than 10^{-10} cm^2/(V·s) at 200 K [135]. Therefore, holes can be considered immobile and remain close to their generation points, at least during the first picoseconds. Before radiation-generated electrons manage to leave the oxide bulk, the initial electron-hole pair density can be promptly reduced through immediate recombination. Two models have been proposed in the literature to interpret the recombination processes: the germinate recombination, which models electron-hole pairs with an average distance longer than the thermalization distance between two types of charges in the same pairs [136], and the columnar recombination, which involves electron-hole pairs with an average distance shorter than the thermalization distance of electrons and their partners [130]. In the latter model, several electrons can be around any given hole, resulting in a higher probability of recombination. In general, the actual recombination is a combination of both processes.

Holes that escape the initial recombination determine the maximum negative threshold voltage shift and are important for the final device behavior. Taking into account the electron-hole pair generation and recombination, the total number of remaining holes per unit area N_h can be roughly given by

$$N_\mathrm{h} = g_0 D t_\mathrm{ox} f(E_\mathrm{ox}), \tag{2.2}$$

where D is the total dose, t_ox is the physical gate-oxide thickness, E_ox is the oxide electric field, and $f(E_\mathrm{ox})$ is the remaining fraction of electron-hole pairs. The charge yield strongly

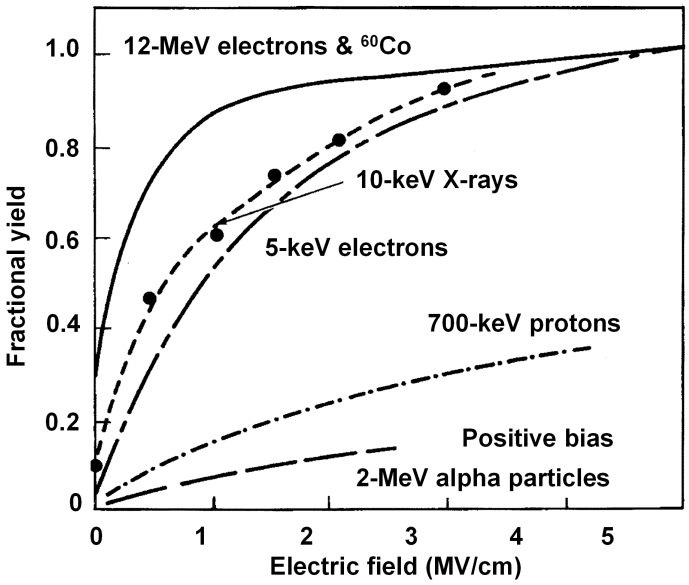


Figure 2.4 – Charge yield of various radiation sources in silicon dioxide (SiO_2) samples as a function of the electric field. (After Oldham and McGarrity [137].)

depends on the physical gate-oxide thickness, the magnitude of the oxide electric field, and the properties of incident particles [14, 137–139]. Fig. 2.4 summarizes the charge yield of various radiation sources in SiO_2, including alpha particles, low-energy protons, electrons, low-energy X-rays, and high-energy γ-rays [137]. The properties of incident particles determine the ionizing power and limit the pair line density. Incident particles with a higher ionizing power, such as 2-MeV alpha particles, tend to generate dense columns of excessive charges and consequently promote the initial recombination. Since the electric field separates electrons and holes, the charge yield increases with it for all radiation sources. At a sufficiently high electric field ($E_{ox} > 3.5\,MV/cm$), the charge yield of low-energy X-rays is on a par with that of high-energy γ-rays, indicating their comparable influence on MOS devices.

2.2.2 Hole transport in the oxide bulk

Hopping transport of remaining holes and the concomitant short-term recovery of the threshold voltage are described as step (2) in Fig. 2.3. In the presence of an electric field, holes escaping the initial recombination move from their generation points through the oxide bulk towards the negative electrode (i.e., the semiconductor/oxide interface under a positive gate bias and the gate/oxide interface under a negative gate bias). Hole transport following a short-pulse sample radiation is a rather complex phenomenon with special features: 1) It spreads over many orders of magnitude in time due to its highly dispersive behavior; 2) It is sensitive to many variables including the electric field, the operating temperature, the gate-oxide thickness, and even the oxide processing history; 3) It is universal with a characteristic dispersion of the recovery curves versus the scaled time under any bias or temperature conditions [41].

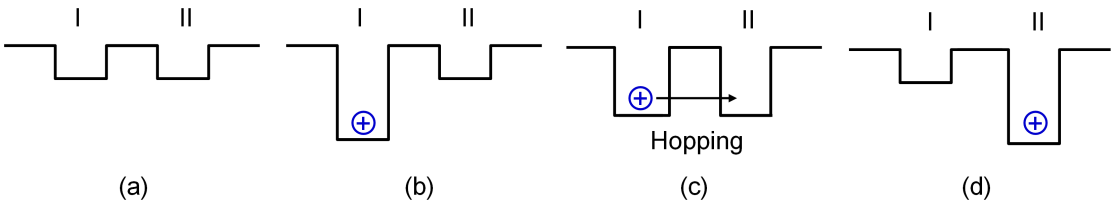
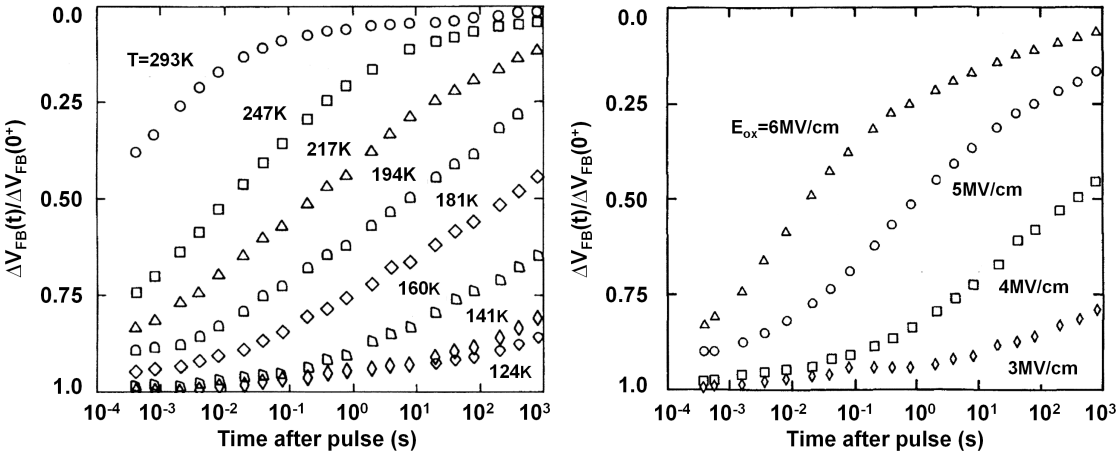


Figure 2.5 – Schematic illustration of polaron hopping between two nearby shallow trap states. (After McLean, et al. [140].)

Holes seem to move through amorphous dielectrics by continuous-time random walk (CTRW)-based stochastic hopping [141–145]. The specific transport mechanism is probably the polaron-like hopping between localized shallow trap states, having a random spatial distribution with an average distance of ~1 nm. The term polaron refers to a situation where a charge carrier, i.e., a hole in this case, strongly interacts with its surrounding medium and induces a significant local distortion of the lattice at its nearby region. This distortion of the local potential increases the trap depth and tends to confine the hopping hole in its immediate vicinity, as illustrated in Fig. 2.5 [140]. As a hole transports through the oxide bulk, it carries the local distortion with it. The features of hole transport, such as dispersion, universality, and sensitivity, can be attributed to a wide distribution of hole hopping times.

Fig. 2.6 shows the normalized flatband voltage shift $\Delta V_{FB}(t)/\Delta V_{FB}(0^+)$ at various temperature and field conditions [146]. The experiments correspond to a 40-μs fast pulse of radiation for minimizing the time between charge generation and electrical measurements. The horizontal



(a) Temperature dependence of hole transport with D = 30 krad, t_{ox} = 86.5 nm, and E_{ox} = 1 MV/cm.

(b) Field dependence of hole transport with D = 30 krad, t_{ox} = 86.5 nm, and T = 79 K.

Figure 2.6 – Flatband voltage evolution of MOS capacitors at various (a) temperature and (b) field conditions, highlighting a strong dependence of hole hopping transport on the operating temperature and the applied field. (After Boesch, et al. [146].)

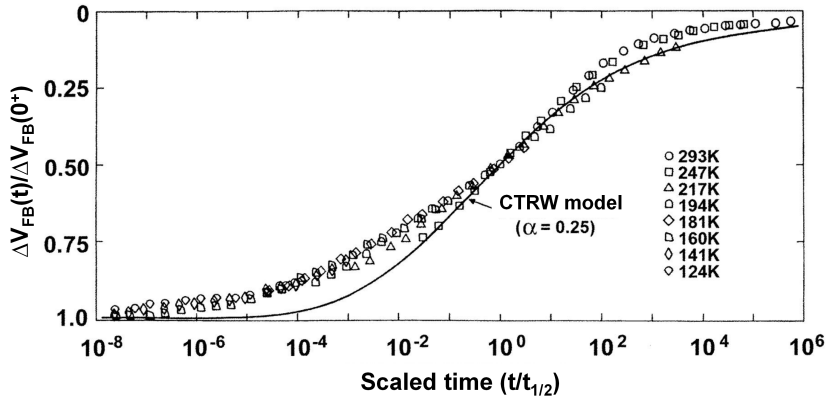


Figure 2.7 – Flatband voltage evolution of MOS capacitors as a function of the scaled time at various temperature conditions, presenting the universal and dispersive features of hole hopping transport. (After McLean, et al. [140].)

axis indicates the required time for a certain percentage of the recovery. The flatband voltage shift evolves through many orders of magnitude of the time and its recovery highlights the strong influence of the operating temperature and the applied electric field on hole transport [146]. The flatband voltage shift is almost completely removed at a high temperature and/or a high electric field, leaving quite a small number of holes eventually trapped in the gate oxide. Moreover, the hole transit time follows a power law of t_{ox}^4 [41]. This oxide thickness dependence implies that the farther a hole transports, the more likely for it to get trapped in a state where the next hop is more difficult and takes more time. Since modern CMOS technologies have a gate-oxide thickness less than 10 nm and an oxide electric field more than 2 MeV/cm, a large number of remaining holes can be swept out of the gate oxide, bringing a significant short-term recovery in the radiation-induced flatband voltage shift.

The universal and dispersive features of hole hopping transport are demonstrated in Fig. 2.7, which plots all the recovery curves of Fig. 2.6a in log-time scale as a function of the scaled time ($t/t_{1/2}$) [140]. The symbol $t_{1/2}$ defines the time when the flatband voltage shift recovers by 50%. The solid line is an analytical fit with the CTRW model, which describes hole transport in the functional form $F(\alpha; t/t_s)$ with α being an independent parameter around 0.25 for SiO_2 and t_s depending on the temperature, the electric field, and the gate-oxide thickness. As seen in Fig. 2.7, the entire process of hole transport extends over 14 orders of magnitude of the time and all the recovery curves almost overlap with each other versus the scaled-time. The influential variables do not influence the overall characteristic dispersion of the time-dependent flatband voltage shift.

2.2.3 Deep hole trapping and annealing

Deep hole trapping and long-term post-irradiation annealing are described as step (3) in Fig. 2.3. Under a positive gate bias, holes drift through the oxide bulk towards the semi-

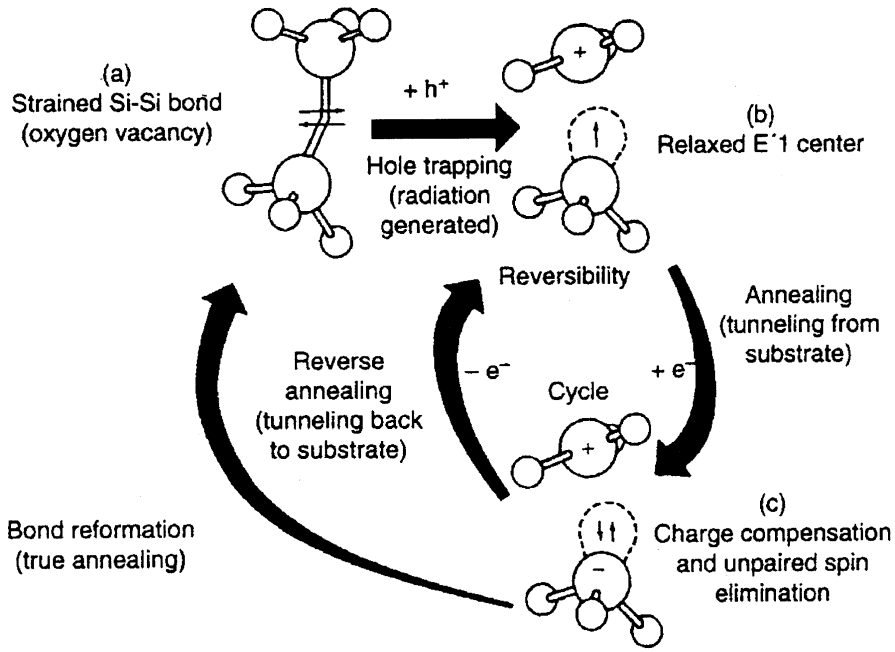


Figure 2.8 – A model of (a→b) deep hole trapping and (c→a) annealing together with (b→c) intermediate compensation and (c→b) reversible annealing. The E_1' center in crystalline alpha-quartz has a counterpart in amorphous SiO_2, i.e., the E_γ' center. (After Lelis, et al. [150].)

conductor/oxide interface and can get trapped there in relatively long-lived deep hole traps. Close to the interface in the transition region from the crystalline silicon to the amorphous oxide, there are numerous defects as a result of lattice mismatch, incomplete oxidation, and oxygen out-diffusion [147]. In particular, oxygen vacancies, which are the dominant type of intrinsic defects in amorphous SiO_2, can act as hole trapping centers [147–151]. In SiO_2, each Si atom is bonded with four O atoms and each O atom is shared by two Si atoms ($O_3{\equiv}Si{-}O{-}Si{\equiv}O_3$). When one O atom is missing, two neighboring Si atoms are weakly bonded together ($O_3{\equiv}Si{-}Si{\equiv}O_3$), as shown in Fig. 2.8a [150].

A radiation-generated hole approaching the defect-rich area may get trapped on one Si atom adjacent to an oxygen vacancy, recombine with one common electron between two bonded Si atoms, and break the strained Si-Si bond asymmetrically. This results in an E' center featuring an unpaired electron on a neutral Si atom ($O_3{\equiv}Si\bullet$) and a positively charged Si atom ($^+Si{\equiv}O_3$). If the unpaired electron is fully associated with the neutral Si atom, this hole trapping generates an E_γ' center [148–150] at an energy level around 3.5 eV above the oxide valence band [151]. As shown in Fig. 2.8b [150], the neutral Si atom stays in a tetrahedral structure, while the positively charged Si atom relaxes back into a planar configuration. If the remaining electron is shared by two Si atoms, an E_δ' center is generated [147, 150, 151] with energy levels between 0.5 eV and 1 eV and sometimes around (2.0 ± 0.1) eV above the oxide valence band [151].

Both E_γ'- and E_δ'-related traps play a role in radiation-induced hole trapping in the oxide bulk. E_δ' centers correspond to localized shallow trap states, which represent an important medium

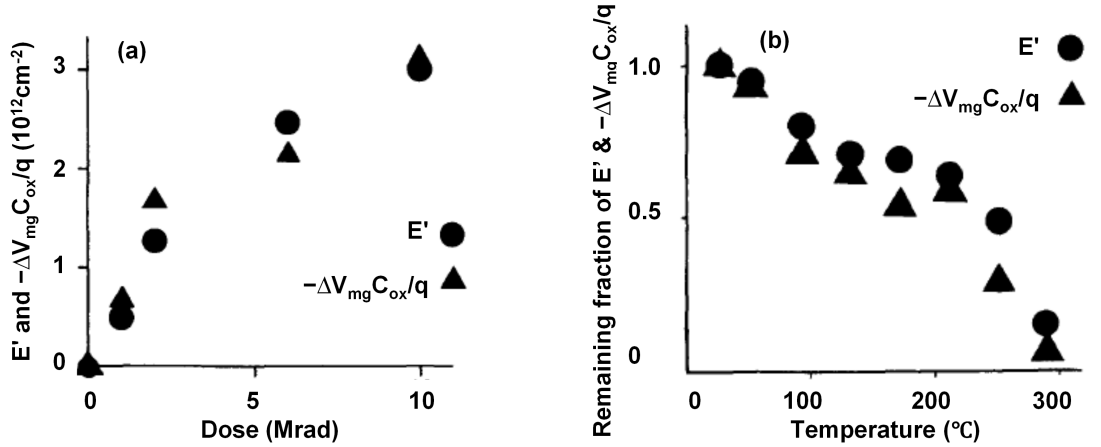


Figure 2.9 – Correlation between the density of E' centers obtained from electron-spin-resonance (ESR) measurements and the oxide-trapped charge density extracted from capacitance-voltage (CV) measurements: (a) density of E' centers and oxide-trapped holes as a function of the total dose; (b) remaining fraction of E' centers and oxide-trapped holes as a function of the annealing temperature. (After Lenahan and Dressendorfer [149].)

for hole hopping transport (Fig. 2.5). Some transporting holes eventually generate E'_γ centers when getting trapped in relatively long-lived deep hole traps near the semiconductor/oxide interface. The literature has recognized the close correlation between radiation-induced E' centers and the concomitant hole trapping in SiO_2. Fig. 2.9 plots the density of E' centers obtained from electron-spin-resonance (ESR) measurements and the oxide-trapped hole density extracted from capacitance-voltage (CV) measurements [149]. As discussed in Section 2.2.4, interface traps are neural when the Fermi level is at the mid-gap. Therefore, the mid-gap CV shift ΔV_{mg} relates oxide-trapped charges through $\Delta V_{mg} = -q\Delta N_{ot}/C_{ox}$, where q is the elementary charge, N_{ot} is the oxide-trap density per unit area, and C_{ox} is the gate-oxide capacitance per unit area. Fig. 2.9a demonstrates that the density of E' centers follows the oxide-trapped charge density at various TID levels. Furthermore, isochronal annealing results in Fig. 2.9b present an identical post-irradiation evolution of E' centers and oxide-trapped holes.

Oxide-trapped charges along with the concomitant voltage shift are relatively stable, but they do undergo long-term annealing with a complex dependence on the time, the electric field, and the operating temperature. In general, oxide-trapped charges anneal with either 1) charge neutralization of electron tunneling from the substrate to the oxide bulk (b→c in Fig. 2.8) or 2) true reformation of the broken Si-Si bonds through thermal excitation (c→a in Fig. 2.8) [147, 149–151].

Fig. 2.10a shows possible energy levels of oxide traps with shallow and deep hole traps corresponding to E'_δ- and E'_γ centers, respectively [151]. Charge compensation occurs through electron tunneling from the substrate to electron traps associated with trapped holes, restoring

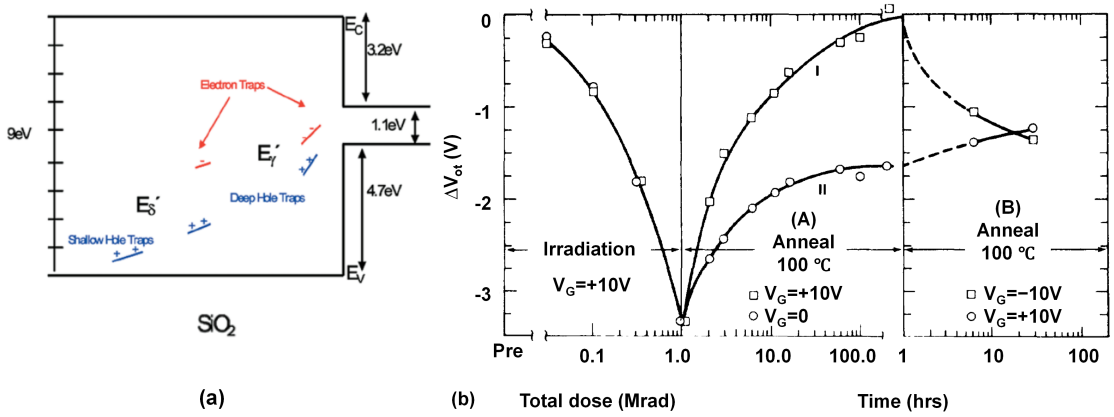


Figure 2.10 – (a) Energy level distribution of oxide traps (after Nicklaw, et al. [151]) and (b) bias-polarity dependence of trapped-hole annealing (after Schwank, et al. [152]).

the net electrical neutrality without reforming the microstructure (b→c in Fig. 2.8). An E' center may be located at one of those two energy levels that an electron can tunnel to [150]: 1) ground state close to the silicon valence band related to the neutral Si atom, where electron tunneling leads to the strongly suggested dipole structure having two electrons with anti-parallel spins in the same orbital; 2) excited state close to the silicon conduction band related to the positively charged Si atom, where electron tunneling results in two unpaired spins in a parallel alignment. Electron trapping in the excited state is unstable and soon decays to the ground state, generally within one second.

If a negative gate bias is applied before the broken Si-Si bond reforms, the compensating electron can tunnel back to the substrate, leaving a trapped hole again [147, 150, 152]. The annealing stage B in Fig. 2.10b confirms the reversible charge compensation with a change of the gate-bias polarity (b⇌c in Fig. 2.8) and the partial annihilation of oxide-trapped charges (c→a in Fig. 2.8) [150, 152]. Generally, reversible annealing through electron tunneling shows a weak temperature dependence and dominates at a low temperature (< 125 °C). This is because the probability of an electron tunneling through an energy barrier over a given period, to a first-order approximation, is a weak function of the temperature. At an elevated temperature, permanent annealing can happen with bond reformation either following an electron tunneling from the substrate to the oxide or a hole detrapping from the charged E' center to the oxide valence band.

Besides, there are quite some publications about border traps, i.e., oxide traps that exchange charges with the substrate [147, 153–155]. Fig. 2.11 distinguishes the physical location of oxide traps from their electrical properties [153]. The probability of charge neutralization through electron tunneling strongly depends on the relative distance of E' centers to the semiconductor/oxide interface. It is difficult for electrons from the silicon bulk to reach E' centers relatively far away from the interface. These E' centers, referring to oxide bulk traps, only get annealed over a long period. E' centers close to the semiconductor/oxide interface

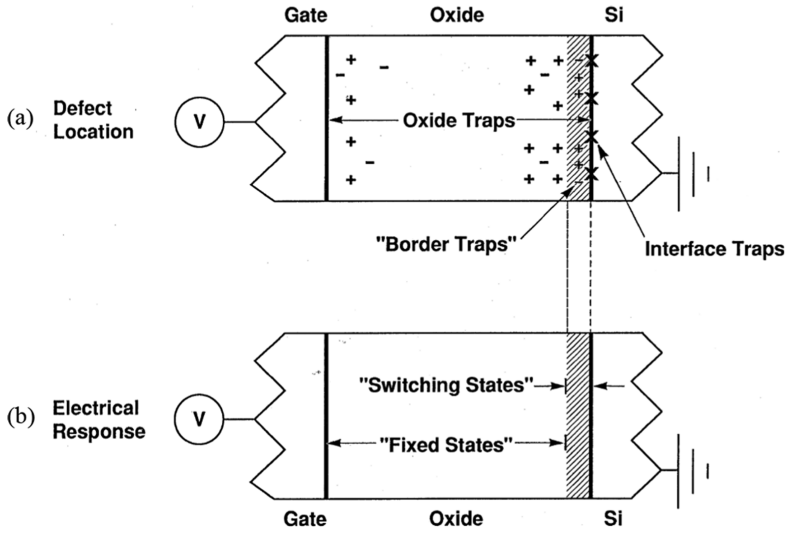


Figure 2.11 – Schematic diagram that distinguishes (a) the physical location of defects from (b) their electrical properties. (After Fleetwood, et al. [153].)

have proved to exchange charges with the substrate through electron tunneling [147, 150–155]. The corresponding oxide traps, generally within 3 nm from the semiconductor/oxide interface with the emission and capture time in the range of 0.01 s to 0.1 s, are defined as switching oxide traps or border traps [147, 153, 154]. The line between oxide bulk traps and border traps in Fig. 2.11a may vary with the annealing time and bias conditions [153, 155]. There are also traps exactly located at the semiconductor/oxide interface, called interface traps, as discussed in Section 2.2.4. As illustrated in Fig. 2.11b, fixed states refer to oxide bulk traps that do not communicate with the substrate, while switching states correspond to border traps and interface traps that exchange charges with the substrate. For MOS devices, fixed states only influence static characteristics through a negative threshold voltage shift, while switching states additionally affect low-frequency noise characteristics [46, 156].

2.2.4 Interface-trap formation

Step (4) in Fig. 2.3 describes interface-trap formation along with the long-term recovery and even the rebound of the threshold voltage. The most convincing precursors for radiation-induced interface traps are H-passivated P_b centers at the semiconductor/oxide interface [149, 157, 158]. Due to lattice mismatch, incomplete oxidation, and oxygen out-diffusion, the semiconductor/oxide interface in a MOS system is intrinsically imperfect with a large number of unpaired dangling bonds ($\sim 10^{13}\,\mathrm{cm}^{-2}$) from trivalent Si atoms ($Si_3{\equiv}Si\bullet$). A P_b center is microscopically characterized by a trivalent Si atom back bonded to three other Si atoms at the semiconductor/oxide interface, with a dangling bond extending into the oxide bulk [159–161]. A low-temperature post-oxidation treatment (~400 °C) has been adopted in commercial semiconductor processes to passivate these bonds through the formation of Si-H bonds ($Si_3{\equiv}Si{-}H$) in forming gas ($H_2 : N_2 = 1 : 9$). This can potentially reduce the density of P_b centers

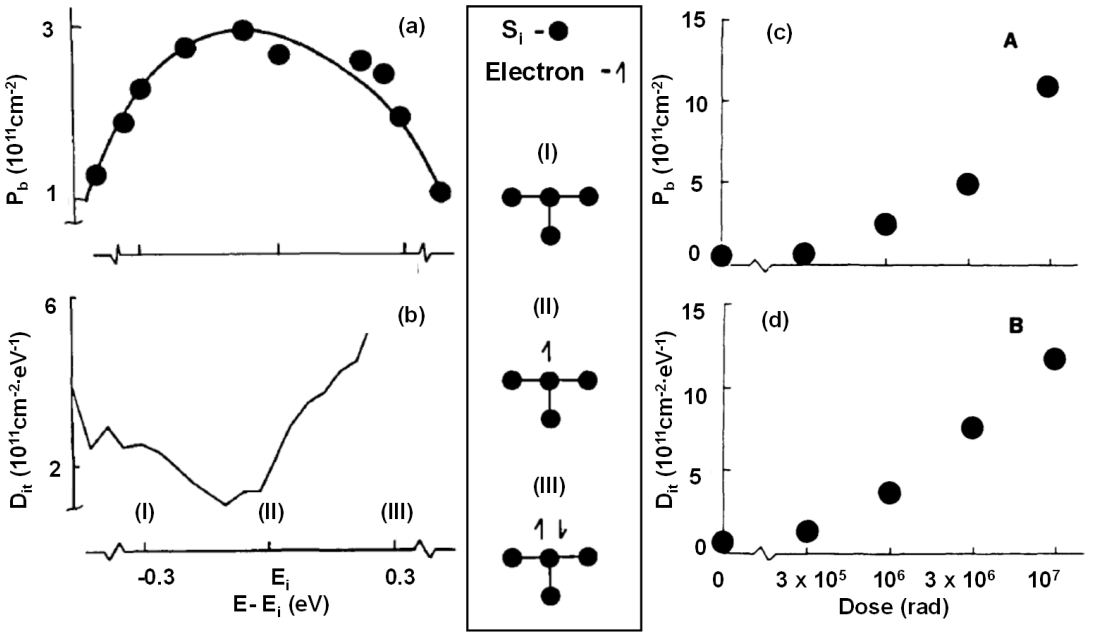


Figure 2.12 – Correlation between the density of P_b centers obtained from ESR measurements and the interface-trap density (D_{it}) extracted from CV measurements: densities of (a, c) P_b centers and (b, d) interface traps as a function of (a, b) the energy level (after Lenahan and Dressendorfer [157]) and (c, d) the total dose (after Lenahan and Dressendorfer [149]).

by one to two orders of magnitude [162, 163]. However, total ionizing radiation or long-term stress can break the Si-H bonds, making H-passivated P_b centers active again [159, 164–167]. A radiation-activated P_b center refers to an unpaired electron, allowing this paramagnetic defect to be detected through ESR measurements. A radiation-activated interface trap is positively charged below the mid-gap, neutral near to it, and negatively charged above it, enabling this amphoteric defect to be studied through CV measurements. The identical evolution of the density of P_b centers and interface traps in Fig. 2.12 demonstrates their close relation [149, 157].

The magnetic state of P_b centers is coherent with the charging state of interface traps, as seen from their corresponding response versus the energy level in Fig. 2.12a and Fig. 2.12b. In the lower part of the bandgap, the P_b center is a donor-like interface trap, contributing an electron and getting positively charged when the Fermi level is close to the valence band ($P_b \longrightarrow P_b^+ + e^-$ or $P_b + h^+ \longrightarrow P_b^+$), as illustrated in Fig. 2.12I. As the Fermi level moves toward the mid-gap, the positively charged P_b center accepts an electron and becomes neutral ($P_b^+ + e^- \longrightarrow P_b$), as indicated in Fig. 2.12II. As the Fermi level gets close to the conduction band, the P_b center picks up another electron and gets negatively charged ($P_b + e^- \longrightarrow P_b^-$), as depicted in Fig. 2.12III. In the upper part of the bandgap, the P_b center is an acceptor-like interface trap ($P_b + e^- \longrightarrow P_b^-$ or $P_b \longrightarrow P_b^- + h^+$). Overall, the P_b center is paramagnetic, converting to a diamagnetic state by accepting or donating an electron. The P_b population is thus maximized near the mid-gap when most interface traps are neutral and minimized around the band edges when most interface traps are charged. The energy-density distribution of P_b centers is also

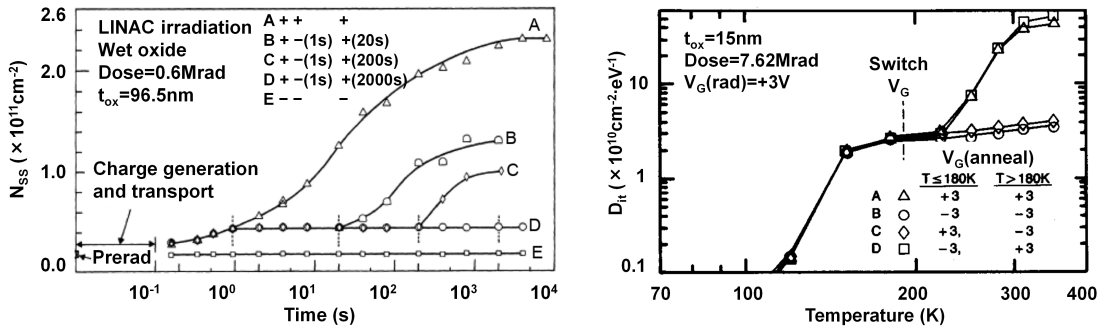
consistent with the typical U-shape distribution of interface traps, having two characteristic peaks about 0.25 eV and 0.85 eV above the silicon valence band [149, 158, 163, 168]. With an average calculation over the energy range, the densities of P_b centers and interface traps can be evaluated as a function of the total dose. As observed from Fig. 2.12c and Fig. 2.12d, they are proportional to each other at various TID levels, evidencing that H-passivated P_b centers are indeed a major source of radiation-induced interface traps.

There is quite some work in the literature describing the radiation-induced activation of interface traps as the removal of H atoms from H-passivated P_b centers [159, 164, 166, 167, 169–171]. Even though this H-removal process is explained differently in the literature, a consensus has been reached on the dominant mechanism: a two-stage process with proton transport [164,166,169,171]. In the first stage, positive protons are formed through the reaction of radiation-generated holes with H-contained oxide defects ($h^+ + H \longrightarrow H^+$) and transport to the semiconductor/oxide interface. More recent studies [171] believe that the second stage is a direct reaction of positive protons with H-passivated P_b centers through

$$Si_3{\equiv}Si{-}H + H^+ \longrightarrow Si_3{\equiv}Si^+ + H_2. \tag{2.3}$$

Hydrogen molecules transport away from the silicon/oxide interface and leave behind positively charged dangling bonds $Si_3{\equiv}Si^+$. The final charge state of TID-activated interface traps depends on the gate-to-bulk bias or the surface potential.

Field switching measurements have uncovered a strong dependence of the interface-trap generation on the gate-bias polarity [164, 166, 169]. Fig. 2.13a reveals the inhibiting effect of a negative gate bias on the interface-trap formation through five recovery curves with different bias conditions [169]. Curve A and E refer to positive and negative gate biases throughout the experiment, respectively. Curve B, C, and D correspond to a positive gate bias until 0.8 s, a negative gate bias until various moments (20 s, 200 s, and 2000 s), and a positive gate bias again



(a) Influence of the gate-bias polarity on the radiation response of hardened capacitors. (After McLean [169].)

(b) Influence of isochronal annealing on the radiation response of MOSFETs. (After Saks, et al. [166].)

Figure 2.13 – Field and temperature dependence of interface-trap formation, confirming the two-stage process with proton transport.

until the end of the experiment. As long as the gate bias is positive during the interface-trap buildup process (A), protons would drift towards the semiconductor/oxide interface, followed by the subsequent activation of interface traps. Once the gate bias is reversed (B, C, and D), protons would transport back to the oxide bulk and even to the gate terminal, prohibiting the interface-trap generation. Even the bias is switched positive again, the final interface-trap density may not reach the level corresponding to a constantly positive gate bias. If the gate bias is kept negative, the activation of interface traps can even be completely suppressed (E).

This two-stage proton transport model is robust but does not explain everything. Alternative models, such as the conversion of oxide traps to interface traps [167], the reaction of transporting holes with H-passivated P_b centers [170], and the reaction of neutral H atoms (H^0) with H-passivated P_b centers [165], have been proposed for explaining individual cases. Fig. 2.13b presents results of isochronal annealing with a field switch at 180 K [166]. The interface-trap buildup between 120 K and 150 K is almost independent of the gate-bias polarity, indicating the dominant effect of the H^0-related process. In contrast, the interface-trap generation above 200 K displays a strong dependence on the gate-bias polarity, implying the dominant influence of the H^+-related depassivation. Since the plot is in log scale, the H^0-related process only accounts for a low percentage of the total interface-trap buildup, evidencing the essential role of proton transport on the interface-trap formation.

Radiation-activated interface traps degrade device performance, basically through modifying the threshold voltage, degrading the subthreshold swing, and reducing the low-field channel mobility [172–175]. For *n*MOSFETs, negative interface-trapped charges cause a positive threshold voltage shift, compensating the negative threshold voltage shift induced by positive oxide-trapped charges. Hence, the buildup of radiation-induced interface traps (Fig. 2.3a) may lead to an ultimately positive threshold voltage shift (Fig. 2.3b). This is similar to the situation where the oxide-trapped hole annealing reduces the negative threshold voltage shift and eventually results in a rebound of the threshold voltage [152]. For *p*MOSFETs, positive interface-trapped charges simply add a negative threshold voltage shift to the negative threshold voltage shift induced by positive oxide-trapped charges. In addition to influencing static characteristics, radiation-activated interface traps, as part of switching states, also degrade low-frequency noise characteristics of MOS devices [46, 156, 156].

2.3 TID effects versus CMOS scaling

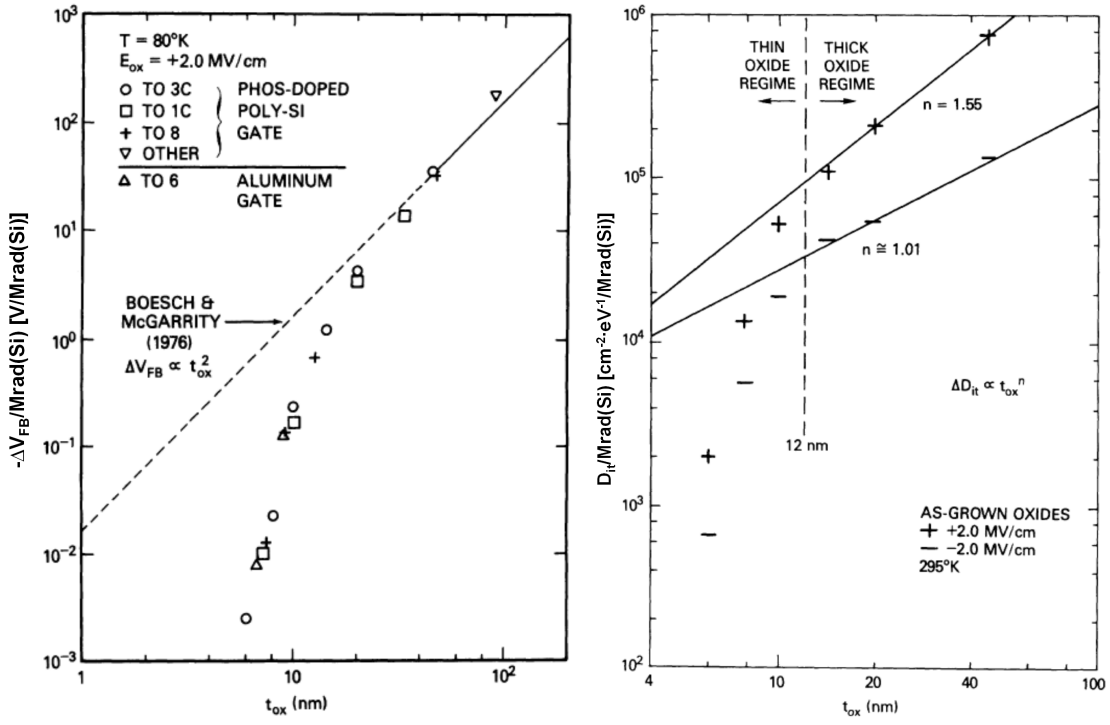
Section 2.2 has detailed fundamental physical processes of TID effects on MOS devices. Overall, through the ionization of dielectrics and the subsequent charge evolution, total ionizing radiation results in charge trapping in the oxide bulk and the activation of H-passivated interface traps. From a circuit design perspective, oxide- and interface-charge trapping influences MOSFET characteristics generally through modifying critical device parameters and degrading low-frequency noise characteristics. CMOS scaling has aggressively shrunk the gate oxide, relieving gate-oxide-related charge trapping [18–21]. However, STI oxides and

spacers have not scaled proportionally and relevant charge trapping has become influential in advanced CMOS technologies [19, 20, 61, 77]. Therefore, the following subsections discuss how CMOS scaling influences radiation-induced charge trapping related to the gate oxide and how STI- and spacer-related charge trapping impacts device behaviors through new TID-induced phenomena [20, 21, 75].

2.3.1 Gate-oxide-related TID effects

Gate-oxide-related charge trapping typically causes parametric shifts, such as a threshold voltage shift, a subthreshold swing degradation, and a low-field channel mobility reduction. Along with the continuous scaling of CMOS technologies, the gate-oxide thickness has entered the nanoscale regime and is getting close to 1 nm. This greatly relieves gate-oxide-related charge trapping and makes relevant parametric shifts much less problematic [41–45].

This radiation tolerance improvement along with CMOS scaling can be partly explained through a first-order estimation of the flatband voltage shift induced by gate-oxide-trapped positive charges ΔQ_{ot} [14, 138, 176, 177]. Assuming a uniform distribution of oxide-trapped charges throughout the gate oxide, the oxide-trapped charge density per unit area Q_{ot} can



(a) Flatband voltage shift per Mrad as a function of the gate-oxide thickness at 80 K. (After Saks, et al. [14].)

(b) Interface-trap density per Mrad as a function of the gate-oxide thickness at 295 K. (After Saks, et al. [15].)

Figure 2.14 – Effects of gate-oxide-thickness scaling on radiation-induced charge trapping in MOS capacitors irradiated with ^{60}Co γ-rays.

therefore be expressed as $Q_{ot} = q\rho_{ox}t_{ox}$, where ρ_{ox} is the oxide-trap density per unit volume. The gate-oxide capacitance per unit area C_{ox} is determined by $C_{ox} = \epsilon_{ox}/t_{ox}$, where ϵ_{ox} is the permittivity of the gate oxide. Introducing these two expressions into the approximate calculation of relevant flatband voltage shift leads to the well-known oxide-thickness-squared scaling law:

$$\Delta V_{ot} = -\frac{\Delta Q_{ot}}{C_{ox}} = -\frac{q\Delta\rho_{ox}t_{ox}^2}{\epsilon_{ox}}. \tag{2.4}$$

This simple formula addresses explicitly how oxide-trapped charges and relevant flabband voltage shift scale quadratically with the gate-oxide thickness. At a very low temperature, radiation-generated holes are essentially frozen near their generation points [141], preventing the activation of H-passivated interface traps. Experimental results in Fig. 2.14a therefore refer only to radiation-induced hole trapping in the gate oxide [14]. This t_{ox}^2 scaling law has been confirmed for the gate oxide thicker than 20 nm [138, 176]. For an even more scaled gate oxide, the flatband voltage shift gets much smaller than the t_{ox}^2 anticipation. This further reduction is largely due to the strengthened hole removal through enhanced tunneling [14, 177].

This radiation tolerance improvement along with CMOS scaling is also a result of the reduction of radiation-activated interface traps [15, 178]. As presented in Fig. 2.14b, radiation-activated interface traps also scale with the gate-oxide thickness [15]. A power scaling law of the interface-trap density has been confirmed for the gate oxide thicker than ~12 nm with the power relying on the gate-bias polarity. A positive gate bias leads to a higher density of radiation-activated interface traps than a negative gate bias, as referred to the respective power of 1.55 and 1.01. This dependence on the gate-bias polarity is associated with the formation and the transport of positive protons. The abrupt drop in the interface-trap density for thinner gate dielectrics appears to result from charge compensation through electron tunneling to trapped holes, which prevents the formation of positive protons needed for activating H-passivated interface traps [15, 164, 166, 169].

The continuous scaling of CMOS technologies does have the potential to enhance the TID tolerance of MOS devices, which is favorable for radiation-hardness applications. The gate-oxide thickness of commercial CMOS technologies has reached around 1 nm, which may allow nanoscale MOS devices to inherently get rid of most gate-oxide-related TID effects [18–21]. However, the particle physics community has gained interests in moving radiation tolerance evaluation to further scaled CMOS technologies, which use HKMG stacks to resolve the gate-leakage issue. High-κ dielectrics can make the effects of TID on nanoscale MOSFETs less predictable, which remains to be carefully studied [64, 65, 73, 74].

2.3.2 STI-related TID effects

Field isolation oxides, which have not been scaled proportionally and are typically in the range of 100 nm to 1000 nm, are much thicker than gate dielectrics. Field isolation structures with

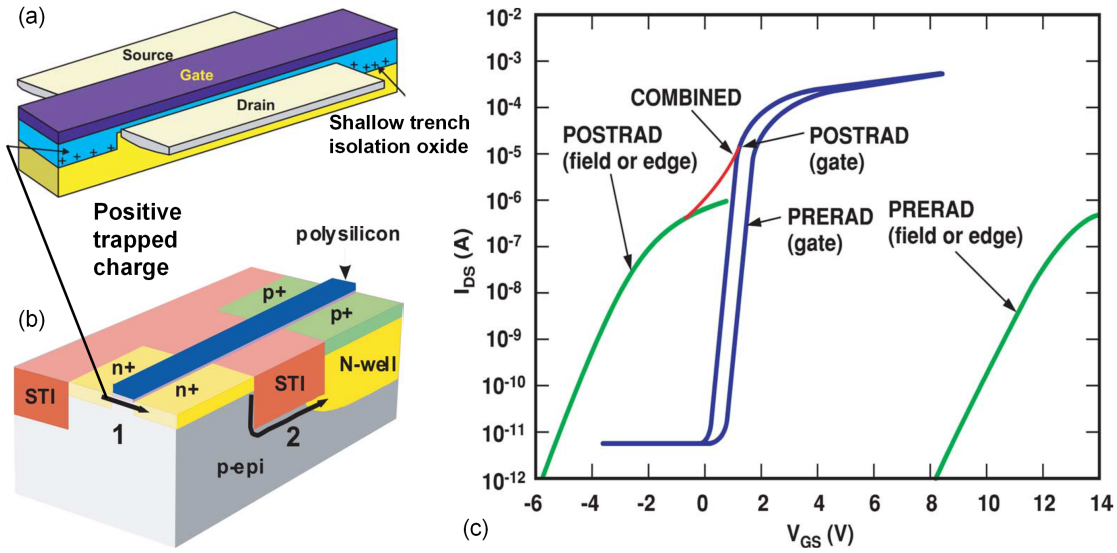


Figure 2.15 – Investigation of the TID-induced parasitic leakage current related to STI oxides: (a) cross section of a shallow-trench-isolated *n*MOSFET; (b) cross section of an *n*MOSFET and a *p*MOSFET isolated by a field oxide; (c) transfer characteristics of a gate-oxide transistor and a field-oxide transistor before and after irradiation. (After Shaneyfelt, et al. [59].)

the thermally local oxidation of silicon (LOCOS) are soft to total ionizing radiation mainly due to the positive charge buildup in thick field oxides and/or at the bird's beak regions [179]. High-density plasma chemical vapor deposition (HDP-CVD) STI oxides have been introduced into sub-0.5-µm technology nodes to eliminate the bird's beak problem of the LOCOS isolation and to serve for a higher integrated density of electronic components [180]. STI structures are planar with the silicon surface, free from lateral encroachment, and not affected by field oxide thinning. However, as depicted in Fig. 2.15a and Fig. 2.15b, STI structures also undergo the positive charge buildup in thick field isolation oxides [59]. These trapped positive charges can open corner/sidewall leakage paths in parallel with the main channel of an *n*MOSFET (path 1) and parasitic leakage paths underneath the trench from the n+ active region of an *n*MOSFET to the n-well substrate of a *p*MOSFET (path 2).

The TID-induced parasitic drain-to-source leakage current of *n*MOSFET can be investigated through the comparison of a gate-oxide transistor and a field-oxide transistor, as illustrated in Fig. 2.15c [59]. The irradiated gate-oxide transistor exhibits a slight threshold voltage shift thanks to relieved gate-oxide-related charge trapping. The field-oxide transistor uses a relatively thick field oxide as its gate dielectric and has a very high threshold voltage. Before irradiation, it is almost fully switched off with its IV curve far to the right of the range of the gate bias. Due to the oxide-thickness-squared scaling law, as expressed in Eq. (2.4), its threshold voltage shift is so large that its IV curve eventually passes that of the irradiated gate-oxide transistor to the left. As displayed by the broken line labeled as "COMBINED", a hump can appear at a certain range of the total drain current and the drain leakage current at a zero gate bias can increase by several orders of magnitude [19, 59, 60, 77].

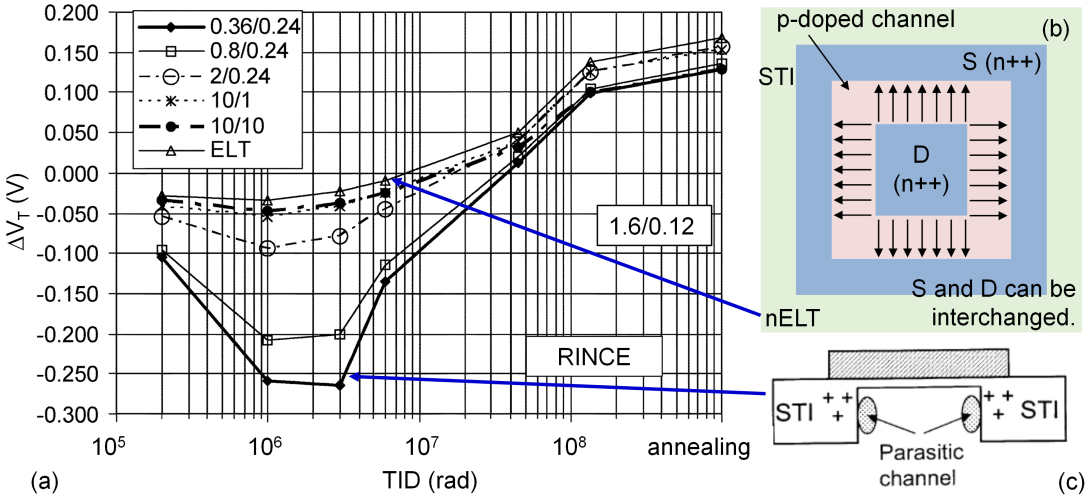


Figure 2.16 – Illustration of STI-related radiation-induced narrow-channel effects (RINCE) through an analysis of the threshold voltage shift versus TID up to 136 Mrad: (a) Threshold voltage shift of I/O *n*MOSFETs and an enclosed-layout transistor (ELT) from a 130-nm bulk CMOS process; (b) top-view of an ELT; (c) STI-related charge trapping. (After Faccio, et al. [19].)

In addition to inducing a parasitic drain-to-source leakage current, STI-related charge trapping can also be strong enough to influence the central part of a narrow channel. This seriously degrades the performance of narrow-channel MOSFETs, which is described as radiation-induced narrow-channel effects (RINCE) [19, 20, 61, 77]. For narrow-channel *n*MOSFETs, STI-trapped positive charges increase the channel potential and induce a negative threshold voltage shift, as shown in Fig. 2.16a. It is worth mentioning ELTs, which have the source or the drain fully enclosed by the gate, as illustrated in Fig. 2.16b. Due to the absence of STI edges between source and drain regions and the inherent immunity to STI-related charge trapping, the ELT in Fig. 2.16a undergoes a smaller threshold voltage shift. For a *p*MOSFET, STI-trapped positive charges attract electrons towards the sidewalls of STI oxides and prevent the formation of the local p-type channel. This leads to a significant negative threshold voltage shift and even reduces the effective channel width. When the channel gets narrower, the effective channel width reduction becomes even more significant and causes a substantial drive current loss.

Overall, STI-related charge trapping can be a very influential cause for ionizing radiation damage to nanoscale MOSFETs. It can lead to an increased drain leakage current for *n*MOSFETs and significant parametric shifts for narrow-channel MOSFETs. Besides, its impact strongly depends on semiconductor manufacturing processes [76, 179, 181]. Since CMOS processing varies so widely, it is impossible to make general statements about the radiation response of such dielectric materials. From this aspect, ionizing radiation effects on field oxides of each specific CMOS process would require a careful investigation. Bear in mind that due to stringent design rules, ELTs have become unavailable in commercial 28-nm bulk CMOS processes [16, 17, 91].

2.3.3 Spacer-related TID effects

Spacers are patterned after the formation of lightly-doped source and drain (LDD) regions along the edges of gate stacks. They serve as masks for the ion implantation of source and drain regions. Depending on CMOS processes, spacers may be fabricated with a combination of underlying SiO_2 and capping Si_3N_4 [182], as illustrated in Fig. 2.17a. As depicted in Fig. 2.17b, total ionizing radiation can produce electron-hole pairs in relatively thick spacers and result in buildup of oxide-trapped charges and interface traps above the LDD regions, impacting the radiation response of nanoscale MOSFETs. It is worth noting that the history of the study of TID effects on spacers is quite short. The first main discovery of spacer-related TID effects has only recently been made with 65-nm bulk MOSFETs at relatively high TID levels [20]. Faccio et

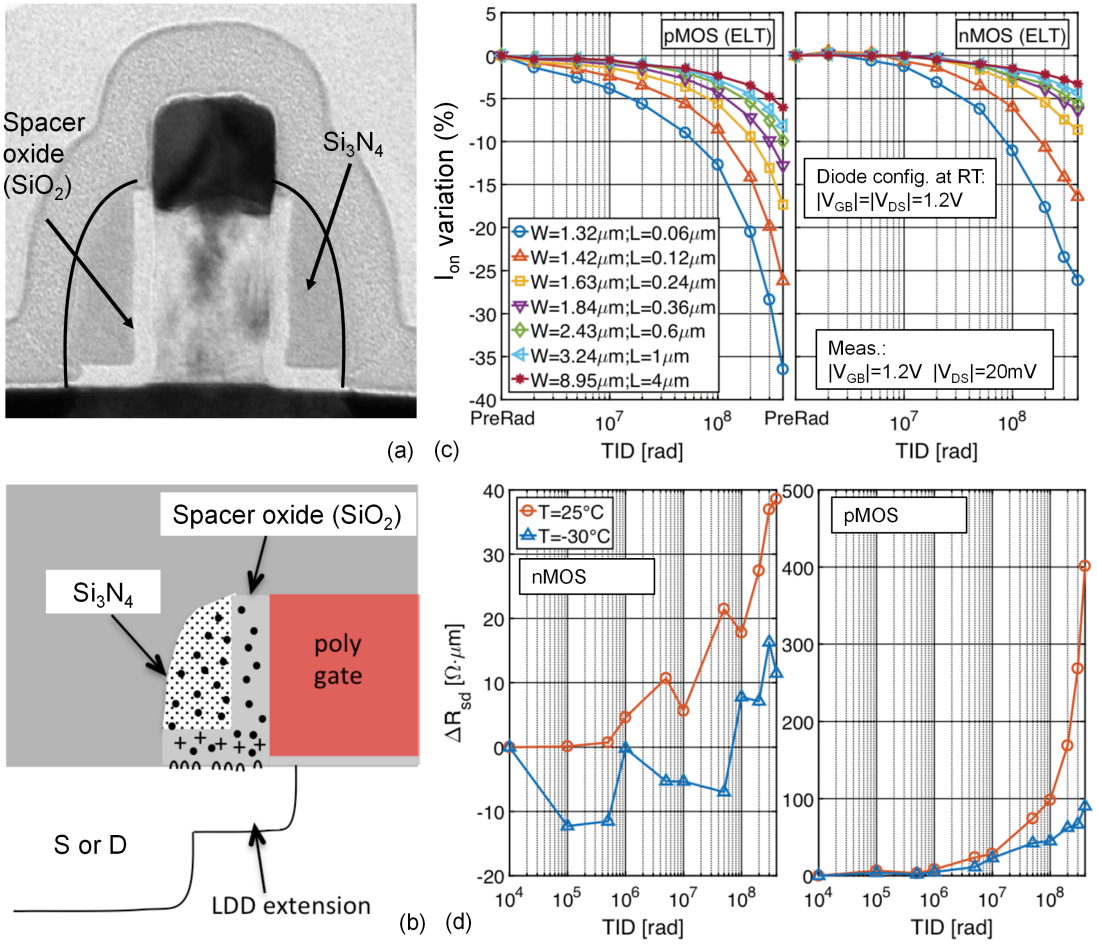


Figure 2.17 – Spacer-related TID effects on the on-current and the series resistance of diode-biased 65-nm bulk MOSFETs: (a) TEM image of a 65-nm transistor, highlighting the significant volume of spacer materials; (b) spacer-related charge trapping above a lightly-doped source or drain (LDD) extension; (c) on-current evolution of 65-nm MOS ELTs in linear operation at room temperature; (d) series resistance extracted from arrays of MOSFETs with a width of 20 μm. (After Faccio, et al. [21].)

al. have concluded spacer-related TID effects to be radiation-induced short-channel effects (RISCE) with a theory of charge generation in spacers and the subsequent evolution to the gate oxide [21, 69].

Spacer-related charge trapping has a strong channel length dependence and influences the series resistance of short-channel MOSFETs. As shown in Fig. 2.17c, the on-current loss of 65-nm MOS ELTs in linear operation gets higher when the channel becomes shorter. Since the enclosed layout of ELTs has eliminated STI-related TID effects and thin gate dielectrics relieve gate-oxide-related charge trapping, the observed on-current loss is mainly a result of ionizing radiation damage to spacers. Moreover, spacer-related charge trapping can influence the effective doping concentration in the LDD regions and thus modifies the series resistance of a MOSFET. As indicated in Fig. 2.17d, the series resistance of 65-nm bulk MOSFETs increases with TID levels, aligning with the substantial on-current loss of short-channel MOSFETs.

Spacer-trapped positive charges may further form positive protons with H-contained oxide defects. When the horizontal electric field and the ambient temperature are high enough, positive protons can transport to the semiconductor/gate-oxide interface and activate H-passivated interface traps at the side with a higher longitudinal bias. This results in a higher density of interface-trapped charges at the drain side of *n*MOSFETs and the source side of *p*MOSFETs. As seen in Fig. 2.18, the shortest-channel 65-nm *p*MOS ELT has a slight threshold voltage shift after 400 Mrad at room temperature and a significant negative threshold voltage shift during high-temperature annealing [69]. This worsened device behavior due to high-temperature annealing is believed to be a result of a higher interface-trap density from the aforementioned charge evolution. As observed from Fig. 2.18, high-temperature annealing also leads to asymmetric measurement results [69]. Normal measurements in saturation indicate a severer threshold voltage shift than their reverse counterparts with the source and the drain interchanged, while two sets of measurements in linear overlap each other. This

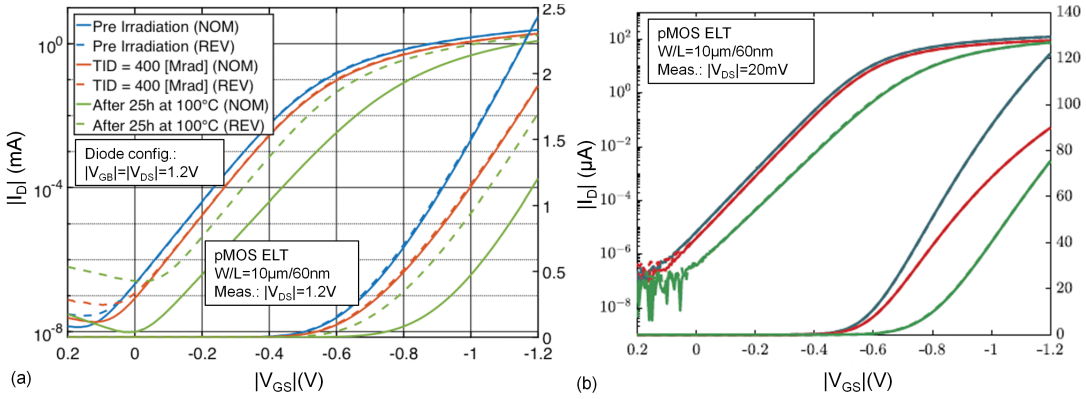


Figure 2.18 – Forward (NOM) and reverse (REV) transfer characteristics in (a) saturation and (b) linear operation of a diode-biased 65-nm bulk *p*MOSFET irradiated at room temperature and annealed at a high temperature, indicating spacer-related asymmetric effects. (After Borghello, et al. [69].)

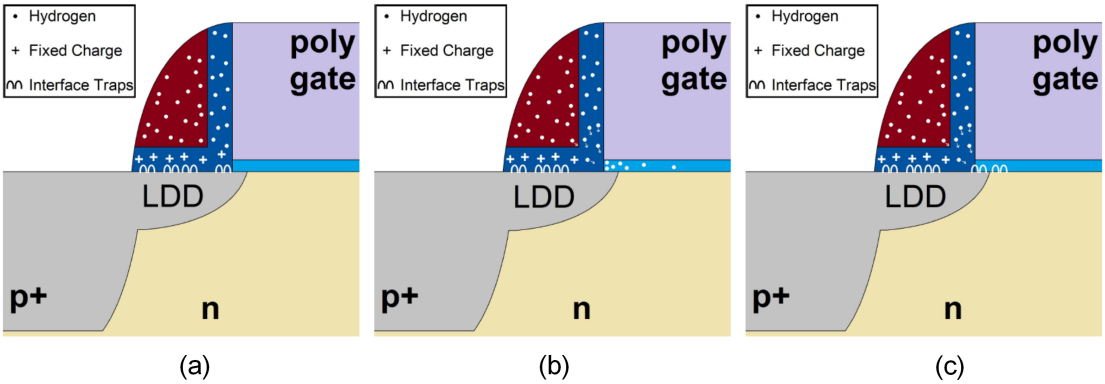


Figure 2.19 – Schematic representation of spacer-related TID effects: (a) radiation-induced charge trapping in spacers, which affects LDD regions and increases the series resistance; (b) proton transport from spacers to the gate oxide, which strongly depends on the ambient temperature and the electric field; (c) reaction between positive protons and H-passivated interface traps, causing the latent interface-trap formation. (After Borghello [69].)

asymmetry is believed to originate from the nonuniform distribution of radiation-induced interface traps. The substantial threshold voltage shift and the asymmetric device behavior can also occur during irradiation if the temperature is high enough.

The complex radiation response related to spacer materials is summarized with the proposed mechanism in Fig. 2.19 [69]:

- Fig. 2.19a. Total ionizing radiation generates an accumulation of oxide-trapped charges and releases hydrogen ions (H^+) in spacer materials. Spacer-trapped positive charges influence the underlying LDD extensions, increasing the series resistance.

- Fig. 2.19b. When the horizontal electric field and the ambient temperature are high enough, positive protons (H^+) drift from spacer materials to the gate oxide. This charge transport is promoted at the side with a higher longitudinal bias: the source side for *p*MOSFETs and the drain side for *n*MOSFETs.

- Fig. 2.19c. Once arriving in the gate oxide, positive protons react with H-passivated interface traps and result in active interface traps at the corner of the channel, contributing to the measurable threshold voltage shift and inducing asymmetric device behaviors.

Since their spacer widths are more comparable with their channel lengths, short-channel MOSFETs are more vulnerable to spacer-related TID effects. Due to the superposed effect of spacer-related oxide- and interface-trapped charges, *p*MOSFETs undergo more serious performance degradation, including a higher series resistance increase, a severer threshold voltage shift, and a more significant drive current loss, than *n*MOSFETs.

2.4 Summary

Basic mechanisms of TID effects on MOSFETs have been explained in detail. Briefly speaking, when a MOSFET is exposed to cumulative ionizing radiation, the absorbed radiation energy produces electron-hole pairs in dielectrics at sensitive device regions, such as the gate oxide, thick spacers, and thick STI oxides. Depending on the magnitude of the electric field and the energy of incident particles, some electron-hole pairs undergo immediate recombination. The remaining mobile electrons then drift away from the dielectric bulk toward the corresponding electrode within picoseconds or so. Some remaining holes hop through localized shallow trap sites arising from lattice disorder and a fraction of them get trapped into relatively long-lived deep hole traps. Some remaining holes form protons via the reaction with H-contained oxide defects. These positive protons move to the semiconductor/oxide interface under a positive gate bias, breaking H-passivated dangling bonds and generating electrically active interface traps.

This time-dependent charge generation and evolution are very sensitive to the operating temperature, the electric field, the gate-oxide thickness, and the oxide processing history. Despite complex physical processes, total ionizing radiation eventually influences device behaviors and circuit functions simply in the form of oxide- and interface-trapped charges. Following Moore's law scaling, CMOS technologies have entered the nanoscale regime, which greatly relieves gate-oxide-related charge trapping. However, high-κ dielectrics have been introduced into MOSFETs since the 45-nm technology node to resolve the gate leakage issue of ultrathin SiO_2-based gate dielectrics, which may introduce uncertainties in the radiation response of nanoscale MOSFETs. Besides, STI oxides and spacers have not scaled proportionally and relevant charge trapping has become influential in advanced CMOS technologies. Therefore, when coming to nanoscale MOSFETs, it is of importance to carefully evaluate the effects of radiation-induced charge trapping related to different dielectric components.

3 Experimental details and results

This chapter first introduces general experimental elements, aiming at a better understanding of measurement results. In particular, it details information about test structures, experimental setup, and measurement protocol that have been used to obtain the majority of experimental results. Total ionizing radiation and post-irradiation annealing influence static characteristics of MOSFETs through several types of parametric shifts. MOSFETs irradiated under different bias and temperature conditions may also respond differently as a result of the bias- and temperature-dependent charge generation and evolution. This chapter then summarizes TID effects on DC characteristics of 28-nm bulk MOSFETs through a comprehensive analysis of MOSFET transfer characteristics and various parametric shifts under different irradiation and annealing conditions. Finally, TID effects that have been seen crucial in advanced CMOS technologies, including the radiation-induced drain leakage current, RINCE, and RISCE, are briefly addressed in the context of the targeted 28-nm bulk CMOS process. This chapter mainly covers results published in [118–121].

3.1 Experimental details

For total dose radiation testing at ultrahigh levels, irradiation duration is one of the most important parameters. This thesis aims at exploring the effects of extremely high TID levels up to 1 Grad that is foreseen for the innermost detectors of the future HL-LHC experiments. For this purpose, it is of importance to maintain the duration of irradiation tests at a proper time span with a high enough dose rate. The most common laboratory radiation sources for total dose radiation testing are low-energy X-rays at the peak of the spectrum density (10 keV) generally from an X-ray tube with a tungsten target and high-energy γ-rays typically at 1.25 MeV from cobalt-60 (^{60}Co) radioactive decay. Low-energy X-rays can operate at higher dose rates thanks to a much more efficient energy transfer coefficient and can irradiate individual dies at the wafer level, allowing X-ray irradiation experiments to be done at a relatively low cost of time and expense [137, 139]. Using CERN's X-ray radiation system, irradiation measurements for this thesis have been carried out on commercial 28-nm bulk MOSFETs up to 1 Grad of TID.

3.1.1 Test structures

This thesis involves various sizes of MOSFETs fabricated with the HPL (high-performance low-power) flavor of a commercial 28-nm bulk CMOS process. This HPL process may use a dielectric bilayer, which is composed of ~2 nm of underlying SiO_2 and ~1.3 nm of overlying HfO_2, as its gate oxide. Fig. 3.1 summarizes the geometry information and the pad distribution of test structures [118]. Test chips are from two tape-outs of the Scaltech28 project and most experiments have been done on samples from the second one. As listed in Fig. 3.1a for the second tape-out, each chip contains three clusters of test structures (row 1-2, 3-4, and 5-6), including 14 single-finger and 8 multi-finger MOSFETs for each n- and p-type, together with a few other special devices such as low-threshold MOSFETs, MOS capacitors, and discrete diodes. The pads of these test structures are carefully arranged in 6 rows (row 1-6) of 24 columns (column 1-24) over an area of 3 mm × 1 mm, as pictured in Fig. 3.1b.

Main research objects in this thesis are 14 core MOSFETs from the second tape-out, as framed with the blue lines in Fig. 3.1a. These 14 core test structures, which are composed of 4 MOSFET arrays and 4 corner MOSFETs, have the channel width W from 3 µm to 100 nm and the channel length L from 1 µm to 30 nm, as depicted by the rectangular width-length plane in Fig. 3.1c. In addition to the extensive experimental campaign with the second tape-out, some preliminary tests have been originally performed on 10 core MOSFETs from the first tape-out, for which

Row\Column	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Device	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth			nch low Vth	diff. pair nch		diff. pair nch		diodes	varactor nch (10pF)	moscap nch (3.5pF)
Width	100n	100n	100n	100n	100n	500n	1u	2.75u	3u	3u	3u	3u	1u	500n			100n	100n		1u			729u	3.1725m
Length	30n	80n	200n	600n	1u	1u	1u	1u	600n	200n	80n	30n	30n	30n			1u	30n		1u			1u	30n
1	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	p-sub	vdd	gate	gate	source	gate	source	cathode	plus	plus
2	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	source	gnd	drain	drain 1	drain2	drain 1	drain 2	anode	minus	minus
Device	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth			pch low Vth	diff. pair pch		diff. pair pch		diodes	varactor pch (10pF)	moscap pch (3.5pF)
Width	100n	100n	100n	100n	100n	500n	1u	2.75u	3u	3u	3u	3u	1u	500n			100n	100n		1u			729u	3.1725m
Length	30n	80n	200n	600n	1u	1u	1u	1u	600n	200n	80n	30n	30n	30n			1u	30n		1u			1u	30n
3	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	nwell	vdd	gate	gate	source	gate	source	cathode	plus	plus
4	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	source	gnd	drain	drain 1	drain2	drain 1	drain 2	anode	minus	minus
Device	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth	nch std Vth					pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth	pch std Vth
Width	3u x 4	2u x 6	1.5u x 8	1u x 12	3u x 1	1.5u x 2	1u x 3	750n x 4	1u	1u					1u	1u	750n x 4	1u x 3	1.5u x 2	3u x 1	1u x 12	1.5u x 8	2u x 6	3u x 4
Length	100n	100n	100n	100n	100n	100n	100n	100n	30n	30n					30n	30n	100n	100n	100n	100n	100n	100n	100n	30n
5	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate	p-sub	vdd	vdd	nwell	gate	gate	gate	gate	gate	gate	gate	gate	gate	gate
6	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain	source	gnd	gnd	source	drain	drain	drain	drain	drain	drain	drain	drain	drain	drain

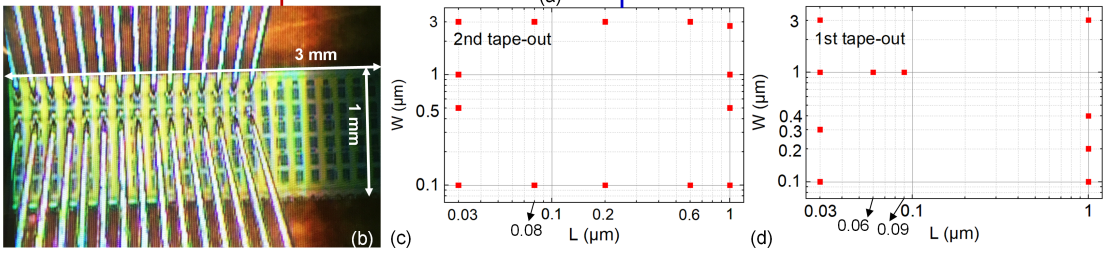


Figure 3.1 – Pad distribution and geometry information of test structures from a commercial 28-nm bulk CMOS process: (a) device matrix of the second tape-out; (b) a picture of a chip contacted by probe needles; (c) most investigated devices from the second tape-out; (d) most investigated devices from the first tape-out. (After Zhang, et al. [118].)

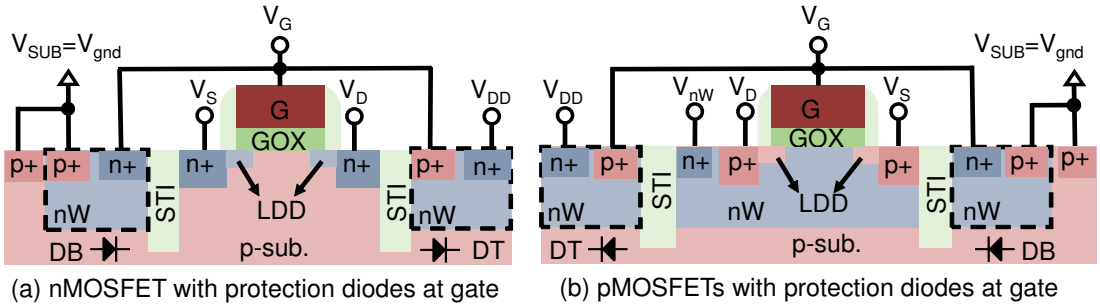


Figure 3.2 – Cross sections of 28-nm bulk MOSFETs from the second tape-out with two electrostatic discharge (ESD) protection diodes (top diode-DT and bottom diode-DB) implemented at each gate terminal. (After Zhang, et al. [120].)

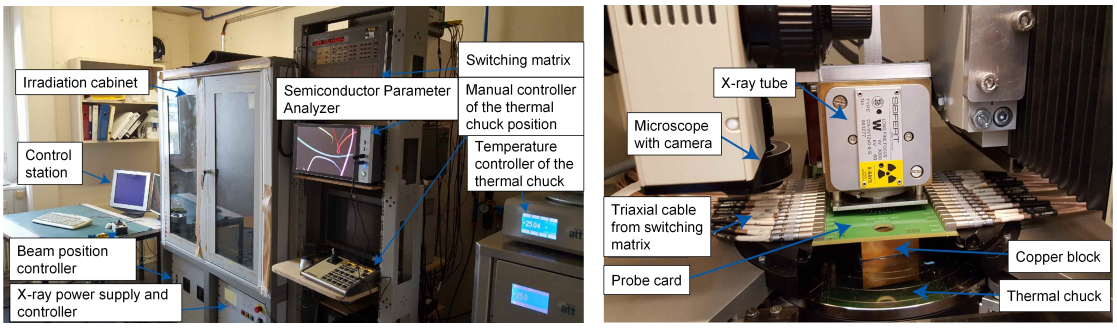
the geometry information is described through Fig. 3.1d.

The orange-filled cells in Fig. 3.1a mark the existence of two electrostatic discharge (ESD) protection diodes implemented at the gate terminal of some devices. The connection of these ESD protection diodes with the gate terminal is illustrated through the cross-sectional views of an *n*MOSFET and a *p*MOSFET in Fig. 3.2 [120]. To maximize the number of test structures on a limited area of the chip, ESD protection diodes in the same cluster are connected to the common power supply (V_{DD}) and the common substrate-shorted ground ($V_{gnd} = V_{SUB}$) and MOSFETs in the same cluster share the pads for the source (V_S), the substrate (V_{SUB}), and the n-well (V_{nW}). These common pads pose a challenge in isolating intrinsic current components flowing through the gate, the source, and the bulk of each MOSFET. Special measurement configurations are required when analyzing various current components.

3.1.2 Experimental setup

AsteriX, as presented in Fig. 3.3, is an X-ray irradiation facility of CERN's EP-ESE group [183]. It has been used to irradiate 28-nm bulk MOSFETs up to 1 Grad for evaluating the potential use in the upcoming HL-LHC. This irradiation system is equipped with a 10-keV X-ray machine (Seifert RP149) with a 50-kV 60-mA 3-kW X-ray generator using a tungsten target. The dose rate is defined as the absorbed total dose divided by irradiation duration and is measured in Mrad/h for the convenience of this work. By adjusting the supplied power to the X-ray tube and changing the tube-target distance, it is possible to select an appropriate dose rate for specialized irradiation tests. Shortening the tube-target distance to the greatest extent at 2 cm and setting the input voltage and the tube current respectively to 40 kV and 50 mA, this X-ray machine can reach very high dose-rate levels up to ~10 Mrad/h, with which it takes approximately 100 hours or around 4 days to reach 1 Grad.

This irradiation system is equipped with a semi-automatic probe station (Karl SUSS PA200) mounting an externally controlled 8-inch thermal chuck, a cooling element to set and maintain the temperature of the thermal chuck, a probe card with 2 rows of 16 needles connected



(a) Irradiation cabinet and measurement instruments.

(b) Probe card inside the irradiation cabinet.

Figure 3.3 – CERN's X-ray machine and associated measurement instruments. (After CERN [183].)

through triaxial cables to a switching matrix (Keithley 707A), a microscope with a CCD camera for verifying the distance between probe needles and test chips, an advanced semiconductor parameter analyzer (Keithley 4200A-SCS) for characterizing test structures, and a LabVIEW software for automating the experiment, as pictured in Fig. 3.3 [183]. The prompt communication between the LabVIEW interface and the whole experimental setup enables chip irradiation and electrical measurements to be performed in a completely automated manner. The temperature-controlling elements allow irradiation tests and post-irradiation annealing to be carried out at a temperature between –50 °C and 200 °C. Test structures have been mainly irradiated at room temperature (25 °C) and annealed at a high temperature (100 °C).

To explore this powerful facility to a large extent and investigate as many devices as possible within one experiment, the pad distribution in Fig. 3.1a and Fig. 3.1b has been customized according to the tailored probe card. Each array of MOSFETs consists of 2 rows of pads and each pad is connected to one MOSFET terminal. The contact between probe needles and test chips is manually conducted, thanks to the CCD camera for prompt and safe alignment. Fig. 3.1b is a picture of the screen showing 2 rows of 16 needles approaching the first cluster of test structures in Fig. 3.1a. The switching matrix linking the probe card and the semiconductor parameter analyzer hosts 3 7072 matrix cards with 12 outputs for each and a total of 36 outputs, as illustrated in Fig. 3.4 [69]. It essentially routes electrical signals from test structures to 6

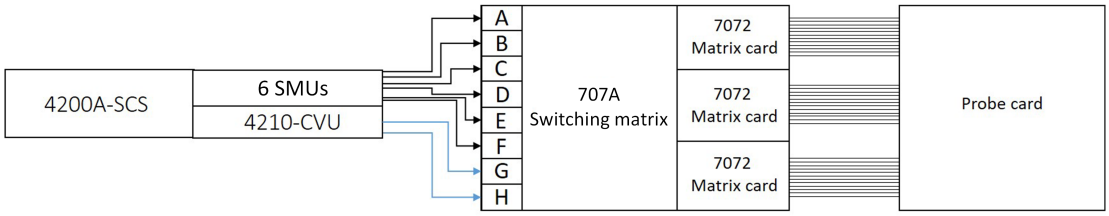


Figure 3.4 – Switching matrix and its connection with the probe card and the semiconductor parameter analyzer. (After Borghello [69].)

Source Measure Units (SMUs) of the semiconductor parameter analyzer. Each of these SMUs allows both sourcing and measuring a device at the same time. In the case of this thesis, they have been mostly applied for sweeping a voltage and measuring the relevant current.

As depicted in Fig. 3.4, the switching matrix has 2 more input channels, sometimes connected to the capacitance-voltage unit (CVU) of the semiconductor parameter analyzer for CV measurements, but more often connected to a voltage generator to bias test chips [69]. During irradiation and annealing, test structures in the same cluster have been biased altogether through the switching matrix under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$), the switched-on condition ($|V_{GB}| = 1.1\,V$ and $V_{DS} = 0\,V$), or the switched-off condition ($V_{GB} = 0\,V$ and $|V_{DS}| = 1.1\,V$) with common biases for the power supply and the bulk ($V_{DD} = V_{nW} = 1.1\,V$ and $V_{SUB} = V_{gnd} = 0\,V$).

3.1.3 Measurement protocol

A systematic experiment generally includes sequential steps of irradiation and annealing together with associated measurements. Thanks to the customized LabVIEW software and its prompt talk with the experimental setup, it becomes possible to set up the whole experiment systematically and run it continuously until the last measurement step. Fig. 3.5 describes the typical procedure that has been applied to obtain the majority of measurement results. Irradiation measurements mainly correspond to the highest dose rate of 10 Mrad/h to reach a proper time span. The radiation exposure stops temporarily and test structures are measured individually when the absorbed total dose reaches certain levels (0-, 0.5-, 1-, 5-, 10-, 50-, 100-, 200-, 400-, 600-, 800-, and 1000 Mrad). To measure the post-irradiation evolution of device behaviors, irradiated chips are removed from the probe card inside the irradiation cabinet after the last TID step and placed into the external setup for annealing with steps of 2 hours. The external setup is very similar to the X-ray irradiation system but with an HP-4155B semiconductor parameter analyzer.

Corresponding to the pad distribution in Fig. 3.1a and Fig. 3.1b, Fig. 3.6 illustrates measurement configurations of *n*- and *p*MOSFET arrays from the second tape-out [127]. Immediately

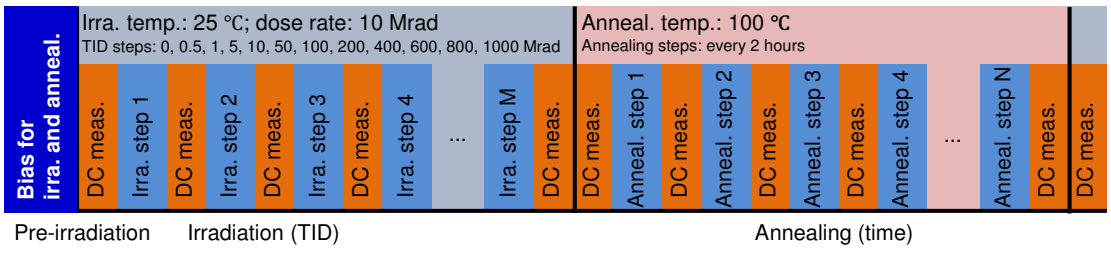
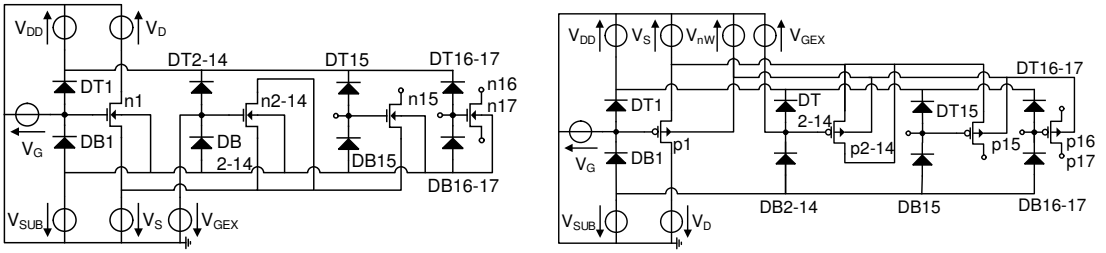


Figure 3.5 – Typical procedure for obtaining test results, including sequential steps of irradiation at room temperature and annealing at a high temperature with associated static electrical measurements.



(a) Circuit schematic of an array of *n*MOSFETs.

(b) Circuit schematic of an array of *p*MOSFETs.

Figure 3.6 – Circuit schematics of both (a) *n*- and (b) *p*MOSFET arrays under test, highlighting common pads between test structures. These circuit schematics correspond to the first and second clusters of devices in Fig. 3.1a and Fig. 3.1b from the second tape-out. (Zhang, et al. [127].)

after each step of irradiation and annealing, a large amount of static electrical measurements have been conducted for investigating TID effects on all regions of device operation. Transfer characteristics $I_D(V_{GB})$ have been measured from linear ($|V_{DS}| = 0.01\,V$) to saturation ($|V_{DS}| = 1.1\,V$) by sweeping the gate voltage from the switched-off state to strong inversion ($|V_{GB}| = -0.2\,V$–$1.1\,V$). Output characteristics $I_D(V_{DS})$ have been tested from the depletion region ($|V_{GB}| = 0.1\,V$) to strong inversion ($|V_{GB}| = 1.1\,V$) by sweeping the drain voltage from linear to saturation ($|V_{DS}| = 0\,V$–$1.1\,V$). To better understand the radiation damage phenomena, source and drain terminals have been interchanged for checking the device asymmetry and shortened for identifying the external leakage contribution.

As oxide-trapped charges may anneal with time [184], a voltage step of 25 mV has been chosen as a suitable compromise between limiting the measurement duration and providing a sufficient measurement resolution. In addition, while measuring one device (n1 or p1), all the others (n2–14 or p2–14) have been held under the switched-off condition with four terminals biased at the same potential ($V_G = V_D = V_S = V_{SUB} = 0\,V$ for *n*MOSFETs and $V_G = V_D = V_S = V_{nW} = 1.1\,V$ for *p*MOSFETs) to limit post-irradiation annealing. Circuit schematics in Fig. 3.6 also highlight common pads of test structures in the same cluster and imply the difficulty in isolating certain intrinsic current components. Floating terminals of test structures out of the range of the probe card make the current isolation even more challenging. Even with special measurement configurations, a complete analysis of all current components requires careful data processing.

3.2 Overview of TID effects on 28-nm bulk MOSFETs

Despite complex physical processes of charge generation and evolution, the eventual consequence of total ionizing radiation can be simply summarized as charge trapping related to dielectrics at sensitive device regions, including the gate oxide, spacers, and STI oxides, as explained in Chapter 2. Fig. 3.7a illustrates the top view of a general bulk MOSFET, Fig. 3.7b

shows the cross section along its length and illustrates charge trapping related to the gate oxide and spacers, and Fig. 3.7c shows the cross section along its width and presents charge trapping related to STI oxides [120]. Oxide-trapped charges Q_{ot}, as labeled by the red symbol "+" in Fig. 3.7, are positive for both *n*- and *p*MOSFETs. Depending on the energy difference between the mid-gap energy level and the Fermi level, interface traps are negatively charged in inverted *n*MOSFETs and positively charged in inverted *p*MOSFETs, as indicated in Fig. 3.7 by the red symbol "x" for interface-trapped charges Q_{it}.

In the form of oxide- and interface-trapped charges, total ionizing radiation may cause several types of parametric shifts of MOSFET characteristics, including a drain leakage current increase, a threshold voltage shift, a low-field channel mobility reduction, an effective channel width reduction, a drive current loss, a radiation-enhanced drain-induced barrier lowering (DIBL) effect, and a subthreshold swing degradation. The main effect of positive oxide-trapped charges is reducing the threshold voltage. Negative interface-trapped charges in *n*MOSFETs cause a positive threshold voltage shift, while positive interface-trapped charges in *p*MOSFETs add up a negative threshold voltage shift. Interface-trapped charges can also degrade the low-field channel mobility through Coulomb scattering and influence the switching performance by degrading the subthreshold swing. The effects of TID on the drain leakage current, the DIBL parameter, and the effective channel width are more complex, involving radiation-induced charge contribution at specific dielectric regions.

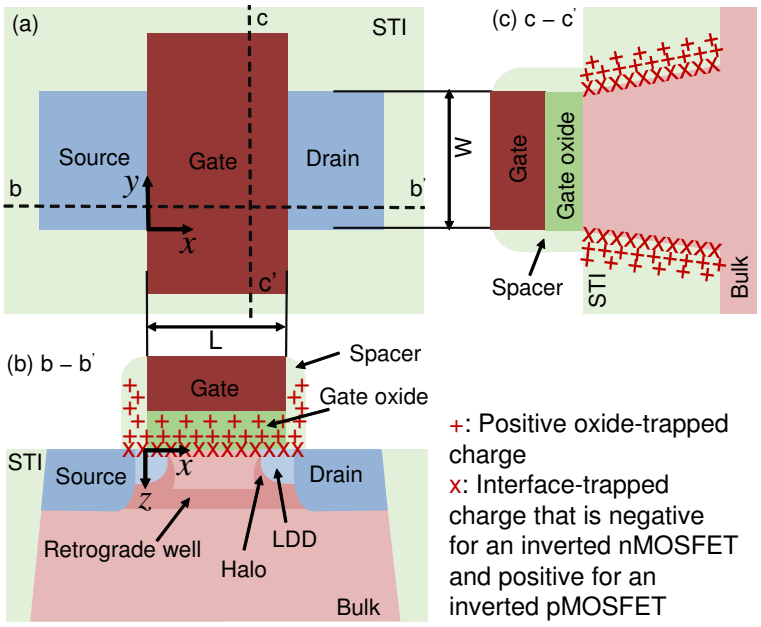


Figure 3.7 – Schematic illustration of TID-induced charge trapping in the oxide bulk and at the silicon/oxide interface of a bulk MOSFET: (a) top view of a general bulk MOSFET; (b) cross-section along the length (b–b'); (c) cross-section along the width (c–c'). (After Zhang, et al. [120].)

Based on this background, the following subsections are devoted to a comprehensive investigation of experimental results of 28-nm bulk MOSFETs. The following analysis mainly focuses on four corner MOSFETs with W_{max}/L_{max}, W_{max}/L_{min}, W_{min}/L_{max}, and W_{min}/L_{min}, where W_{max} is the maximum channel width, W_{min} is the minimum channel width, L_{max} is the maximum channel length, and L_{min} is the minimum channel length. Due to limited access to CERN's irradiation system, MOSFETs of each dimension were only tested once for each experimental condition. There is no data for a direct comparison to statistically verify each set of measurement results. However, through a comparison among MOSFETs of the same cluster, it is still possible to identify unrepresentative jumping behaviors and conclude reasonable trends of the parametric evolution. In addition, MOSFETs are biased in saturation with a nonzero V_{DS} in most analog circuits and particularly analog FE electronics. Therefore, unless noted otherwise, the experimental analysis uses measurement results of two chips irradiated up to 1 Grad under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$) at room temperature (25 °C) and then annealed with the same bias condition at a high temperature (100 °C). The chips for *n*- and *p*MOSFETs have been annealed for 100 hours and 38 hours, respectively.

3.2.1 TID effects on transfer characteristics

Fig. 3.8a-d report the measured $I_D - V_{GB}$ curves in saturation operation ($V_{DS} = 1.1\,V$) of four corner *n*MOSFETs irradiated up to 1 Grad under the diode condition ($V_{GB} = V_{DS} = 1.1\,V$) at room temperature (25 °C). Total ionizing radiation increases the drain leakage current of *n*MOSFETs by a maximum of more than three orders of magnitude. Except for the significant drain leakage current increase, the wide/long-channel *n*MOSFET (Fig. 3.8a) remains almost unaffected. The wide/short-channel *n*MOSFET (Fig. 3.8b) present a negative threshold voltage shift and an improved drive current. Narrow-channel *n*MOSFETs (Fig. 3.8c and Fig. 3.8d) go through a rebound of the threshold voltage and display worse performance at high TID levels.

Similarly to Fig. 3.8a-d, Fig. 3.8e-h report the measured transfer characteristics in saturation operation ($V_{DS} = -1.1\,V$) of four corner *p*MOSFETs irradiated up to 1 Grad under the diode condition ($V_{GB} = V_{DS} = -1.1\,V$) at room temperature (25 °C). The drain leakage current of *p*MOSFETs increases slightly by a maximum of tenfold. Despite the slight drain leakage current increase, all *p*MOSFETs are more sensitive to total ionizing radiation than their n-type counterparts. Compared with wide-channel *p*MOSFETs (Fig. 3.8e and Fig. 3.8f), narrow-channel ones (Fig. 3.8g and Fig. 3.8h) suffer much more serious performance degradation with a significant threshold voltage shift and a dramatic drive current loss. Short-channel *p*MOSFETs (Fig. 3.8f and Fig. 3.8h) demonstrate a higher radiation tolerance than their long-channel counterparts (Fig. 3.8e and Fig. 3.8g).

Once the threshold voltage V_T is extracted from the linear interpolation of $\sqrt{|I_D|} - |V_{GB}|$ curves (Section 3.2.2), measurement results are plotted as a function of the overdrive voltage $|V_{GB} - V_T|$ in Fig. 3.9 for distinguishing the influence of the threshold voltage shift from other parametric evolution. The $|I_D| - |V_{GB} - V_T|$ curves in the switched-on operation of

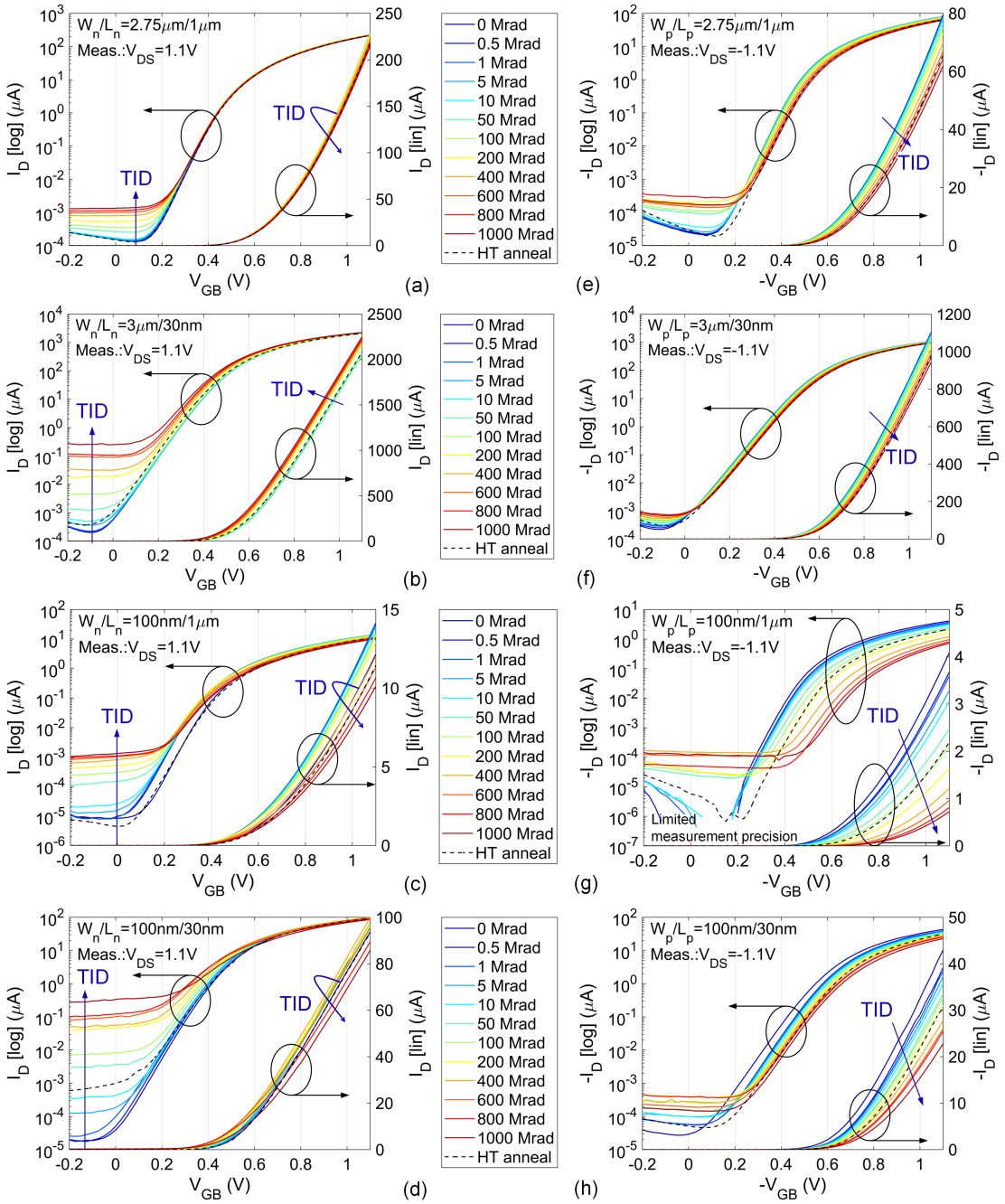


Figure 3.8 – Measured drain current $|I_D|$ versus the gate-to-bulk voltage $|V_{GB}|$ in saturation operation ($|V_{DS}| = 1.1\,V$) of four corner (a-d) *n*- and (e-h) *p*MOSFETs irradiated at room temperature (25 °C) and annealed at a high temperature (100 °C) under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$): (a, e) $W = 2.75\,\mu m, L = 1\,\mu m$; (b, f) $W = 3\,\mu m, L = 30\,nm$; (c, g) $W = 100\,nm, L = 1\,\mu m$; (d, h) $W = 100\,nm, L = 30\,nm$.

wide-channel MOSFETs (Fig. 3.9a, Fig. 3.9b, Fig. 3.9e, and Fig. 3.9f) remain almost unaffected, indicating the sole influence of the slight threshold voltage shift. Narrow-channel MOSFETs

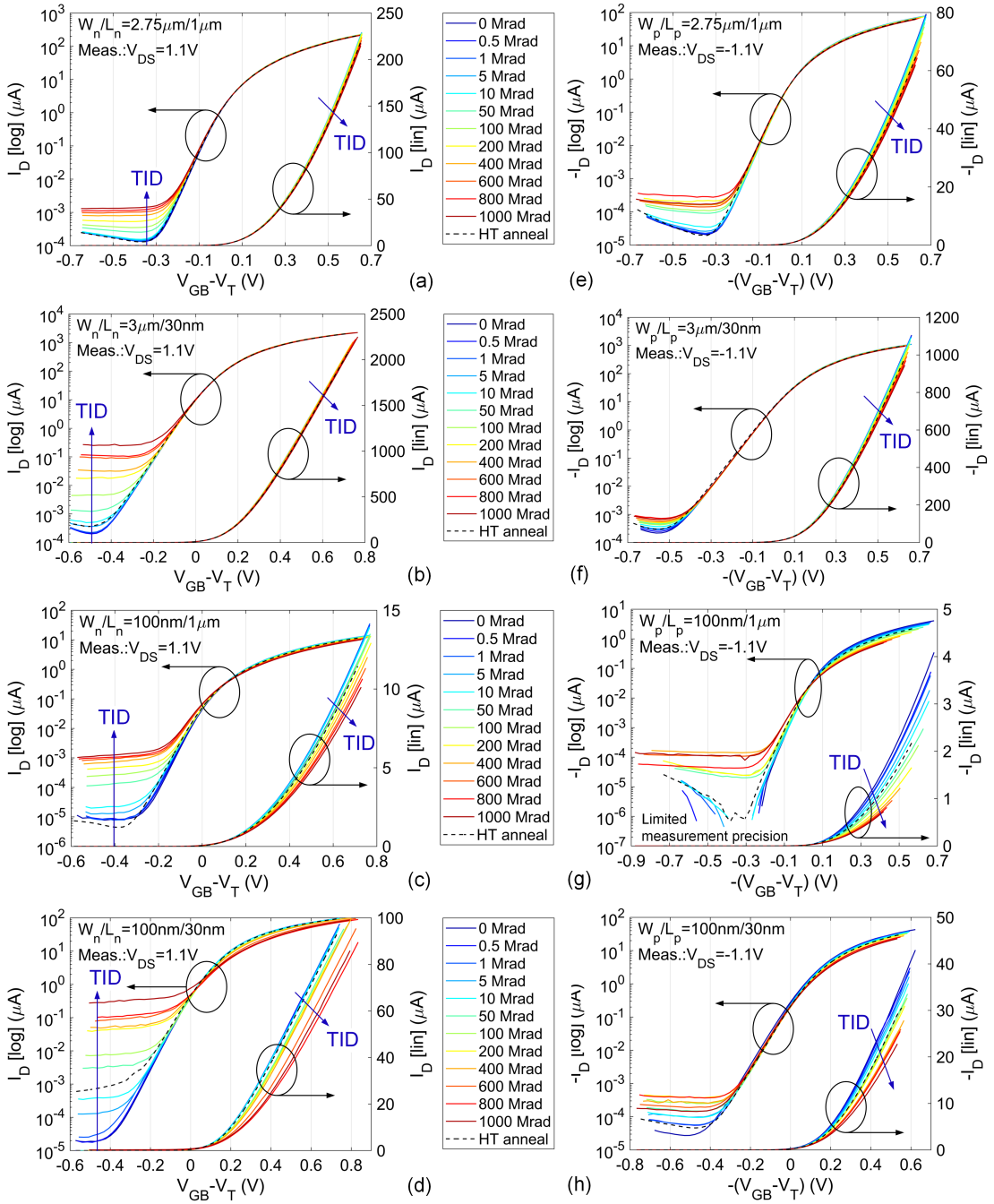


Figure 3.9 – Measured drain current $|I_D|$ versus the overdrive voltage $|V_{GB} - V_T|$ in saturation operation ($|V_{DS}| = 1.1\,V$) of four corner (a-d) *n*- and (e-h) *p*MOSFETs irradiated at room temperature (25 °C) and annealed at a high temperature (100 °C) under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$): (a, e) $W = 2.75\,\mu m, L = 1\,\mu m$; (b, f) $W = 3\,\mu m, L = 30\,nm$; (c, g) $W = 100\,nm, L = 1\,\mu m$; (d, h) $W = 100\,nm, L = 30\,nm$.

(Fig. 3.9c, Fig. 3.9d, Fig. 3.9g, and Fig. 3.9h) still suffer an on-current loss as a result of a reduction in the low-field channel mobility and/or the effective channel width. The $|I_D| - |V_{GB} - V_T|$

curves of narrow/long-channel MOSFETs (Fig. 3.9c and Fig. 3.9g) stretch out in the subthreshold region, indicating an increased subthreshold swing and a worsened switching capability.

Overall, test structures of this 28-nm bulk CMOS process are radiation tolerant except for the significant drain leakage current increase of *n*MOSFETs and the considerable performance degradation of narrow-channel MOSFETs. Besides, various sizes of MOSFETs respond to total ionizing radiation differently, suggesting their different levels of sensitivity to STI-related charge trapping. To better understand how ultrahigh TID levels influence 28-nm bulk MOSFETs and pinpoint the dominant damage mechanisms, crucial device parameters are extracted and analyzed in Section 3.2.2 together with an experimental investigation of post-irradiation annealing effects in Section 3.2.3 and bias dependence of TID effects in Section 3.2.4.

3.2.2 TID effects on device parameters

Parameter extraction

Crucial device parameters, including the on-current I_{on}, the off-current I_{off}, the DIBL parameter α_{dibl}, the threshold voltage V_T, the low-field channel mobility μ_0, the subthreshold swing *SS*, and the maximum transconductance $G_{m.max}$, are defined and extracted, as shown in Fig. 3.10, using DC measurements of an *n*MOSFET [185, 186]. Here, the transconductance factor or the transfer parameter $\beta = \mu_0 C_{ox} W/L$ reflects information about the low-field channel mobility μ_0. As briefly mentioned in Section 3.2.1, these parameters are sensitive to TID and their evolution with TID is useful for the understanding of radiation damage mechanisms. Extracted parameters are generally compared with their pre-irradiation references by difference, such as the threshold voltage shift

$$\Delta V_T(\text{TID}) = V_T(\text{TID}) - V_T(\text{pre-irra.}), \tag{3.1}$$

or by percentage, such as the on-current variation

$$I_{on.var}(\text{TID}) = 100\left[\frac{I_{on}(\text{TID})}{I_{on}(\text{pre-irra.})} - 1\right], \tag{3.2}$$

for assessing the effects of TID on them and overall DC characteristics.

Specifically, the on-current I_{on} and the off-current I_{off} are defined and extracted at a zero volt ($V_{GB} = 0\,\text{V}$) and the maximum value ($V_{GB} = 1.1\,\text{V}$) of the gate-to-bulk voltage V_{GB}, respectively, as labeled in Fig. 3.10a for both linear and saturation. The DIBL parameter refers to a short-channel effect, indicating a threshold voltage reduction at a high drain-to-source voltage, as shown in Fig. 3.10a. Here, it is approximated through two different values of V_{GB} corresponding to a constant I_D in linear ($V_{DS} = 0.01\,\text{V}$) and saturation ($V_{DS} = 1.1\,\text{V}$) and is measured in mV/V:

$$\frac{\alpha_{dibl}}{1000} = -\frac{V_{T.sat} - V_{T.lin}}{V_{DS.sat} - V_{DS.lin}} = -\frac{V_{GB}(V_{DS.sat}) - V_{GB}(V_{DS.lin})}{V_{DS.sat} - V_{DS.lin}}. \tag{3.3}$$

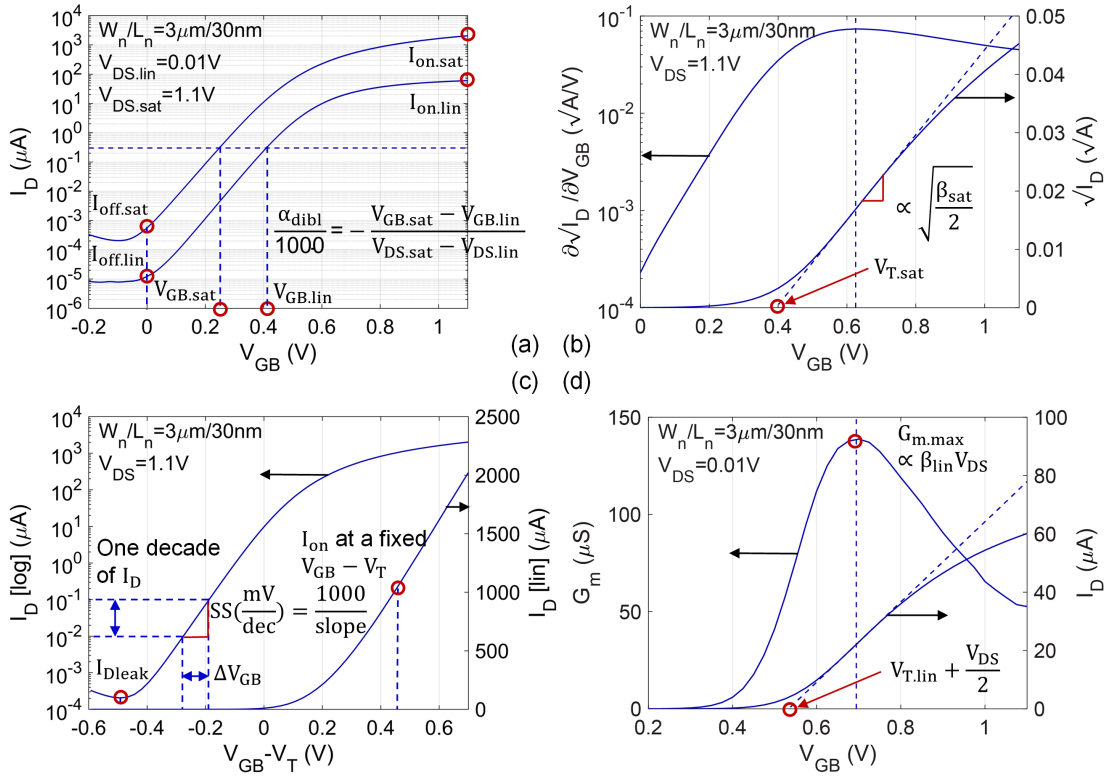


Figure 3.10 – Definitions and extractions of crucial device parameters for investigating the radiation response of test structures: (a) $I_D - V_{GB}$ curves in linear and saturation for extracting the on-current I_{on}, the off-current I_{off}, and the drain-induced barrier lowering (DIBL) parameter α_{dibl}; (b) $\sqrt{I_D} - V_{GB}$ curve in saturation for extracting the threshold voltage $V_{T.sat}$ and the mobility-related parameter β_{sat}; (c) $I_D - (V_{GB} - V_T)$ curve in saturation for extracting the subthreshold swing SS as well as the on-current I_{on} and the drain leakage current I_{Dleak} at a constant $V_{GB} - V_T$; (c) $I_D - V_{GB}$ curve in linear for extracting the maximum transconductance $G_{m.max}$, the threshold voltage $V_{T.lin}$, and the mobility-related parameter β_{lin}.

Together with the mobility-related parameter β_{sat}, the threshold voltage in saturation $V_{T.sat}$ is extracted using the linear extrapolation of the square root of the drain current $\sqrt{I_D}$ at the steepest point, as depicted in Fig. 3.10b. This method originates from the simple threshold-voltage-based quadratic model in strong inversion of saturation operation:

$$I_{D.sat} = \frac{\beta_{sat}}{2}(V_{GB} - V_{T.sat})^2. \tag{3.4}$$

This linear fit of $\sqrt{I_D}$ intercepts the V_{GB} axis ($I_D = 0\,A$) at the threshold voltage in saturation $V_{T.sat}$, while its slope $\sqrt{\beta_{sat}/2}$ is related to the low-field channel mobility in saturation.

The subthreshold swing SS is another important device parameter, defining how much V_{GB} should be increased to get a decade increase of I_D, as indicated in Fig. 3.10c. Here, it is approximated as the inverse of the maximum slope of the $\lg I_D - V_{GB}$ curve and measured in

mV/dec :

$$\frac{1000}{SS} = \max\left(\frac{\partial \lg I_D}{\partial V_{GB}}\right). \tag{3.5}$$

From the $I_D - (V_{GB} - V_T)$ curve, the on-current I_{on} can be extracted at the same channel inversion condition at a constant $V_{GB} - V_T$, distinguishing the influence of the threshold voltage shift from the low-field channel mobility degradation and/or the effective channel width reduction. Besides, the drain leakage current I_{Dleak} is extracted at a constant $V_{GB} - V_T$ to isolate the influence of the threshold voltage shift from the parasitic drain-to-source leakage current $I_{Dleak.par}$.

Together with the mobility-related parameter β_{lin}, the threshold voltage in linear $V_{T.lin}$ is extracted using the linear extrapolation of I_D at the maximum value of the transconductance $G_{m.max}$, as illustrated in Fig. 3.10d. This method originates from the simple threshold-voltage-based quadratic model in strong inversion of linear operation:

$$I_{D.lin} = \beta_{lin}\left[V_{GB} - V_{T.lin} - \frac{V_{DS}}{2}\right]V_{DS}. \tag{3.6}$$

This linear fit of I_D intercepts the V_{GB} axis ($I_D = 0\,A$) at $V_{T.lin} + V_{DS}/2$, which can be approximated as $V_{T.lin}$ at a small value of V_{DS}. Ideally, the transconductance G_m in strong inversion of linear operation is constant and can be expressed as $G_m = \partial I_{D.lin}/\partial V_{GB} = \beta_{lin} V_{DS}$. In reality, it is degraded by parasitic series resistances and mobility degradation effects at high V_{GB} values. Still, $G_{m.max}$ is useful for the evaluation of TID effects on the low-field channel mobility.

On-current, threshold voltage, carrier mobility, peak transconductance

Fig. 3.11 reports the TID-induced evolution of (a) the maximum drive current extracted at $V_{GB} = V_{DS} = 1.1\,V$, (b) the threshold voltage extracted in saturation, (c) the on-current extracted at a constant $V_{GB} - V_T$, and (d) the peak transconductance extracted in linear for four corner *n*MOSFETs. The maximum drive current depends on both the threshold voltage and the low-field channel mobility, while the on-current extracted at a constant $V_{GB} - V_T$ depends only on the low-field channel mobility. The V_T-shift-isolated on-current and the peak transconductance carry information about the low-field channel mobility and their values are consistent with each other.

Wide-channel *n*MOSFETs maintain all these four parameters close to their pre-irradiation references up to 100 Mrad, confirming the strong radiation tolerance of ultrascaled gate dielectrics. For narrow-channel *n*MOSFETs, TID levels up to 100 Mrad reduce the threshold voltage and slightly increase the low-field channel mobility, leading to an on-current improvement. The narrow/long-channel *n*MOSFET is sensitive to total ionizing radiation, showing a most negative threshold voltage shift of −40 mV, a maximum mobility increment of 5%, and a maximum on-current increase of 15%. This suggests the influence of STI-related positive charge buildup close to the surface channel.

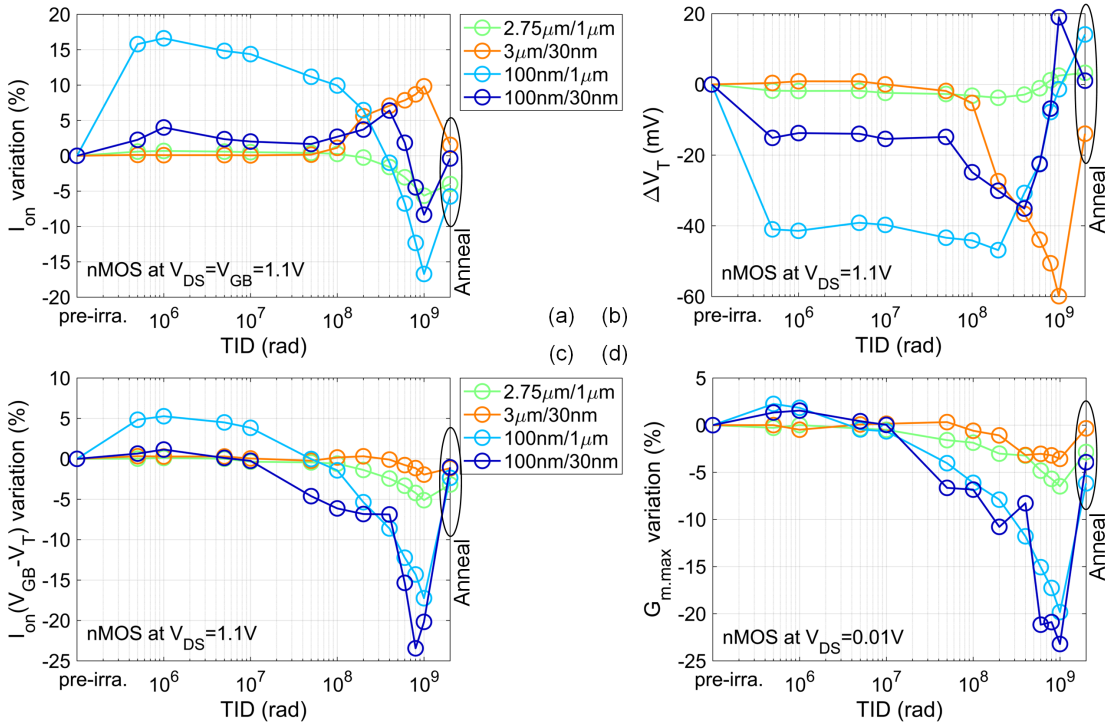


Figure 3.11 – TID effects on extracted parameters of four corner *n*MOSFETs, including (a) the on-current I_{on}, (b) the threshold voltage V_T, (c) the V_T-shift-isolated on-current $I_{on}(V_{GB}-V_T)$, and (d) the peak transconductance $G_{m.max}$.

When TID is more than 100 Mrad, most *n*MOSFETs show a positive threshold voltage shift, a degraded low-field channel mobility, and a drive current loss. The slight change in the threshold voltage and the low-field channel mobility of the wide/long-channel *n*MOSFET suggests interface-charge trapping along the gate oxide. The narrow/long-channel *n*MOSFET suffers a maximum on-current loss of 17%. Considering its ultimately negligible threshold voltage shift, this on-current loss is mainly a result of the radiation-induced mobility reduction. The rebound of the threshold voltage and the concomitant mobility reduction of narrow-channel *n*MOSFETs reveal the buildup of negative interface-trapped charges near the surface channel along STI-sidewalls. The wide/short-channel *n*MOSFET behaves quite differently from the others eventually with a negative threshold voltage shift of −60 mV and an on-current increase up to 10%. This is correlated with a radiation-enhanced DIBL effect induced by STI-trapped positive charges, as discussed later in this subsection.

Overall, 28-nm bulk *n*MOSFETs are radiation tolerant at the switched-on region with a maximum on-current variation of 15% for narrow-channel ones. This highlights the strong radiation tolerance of ultrathin gate dielectrics and indicates the dominant influence of STI-related charge trapping. It is worth noting that despite the presence of STI-related trapped charges, the compensation of negative interface-trapped charges and positive oxide-trapped charges in *n*MOSFETs eventually leads to a slight threshold voltage shift and a low on-current variation.

Fig. 3.12 reports the TID-induced evolution of those parameters of four corner *p*MOSFETs. Compared with *n*MOSFETs, *p*MOSFETs are much more sensitive to total ionizing radiation. This is because both oxide- and interface-trapped charges are positive for *p*MOSFETs, inducing a more negative threshold voltage shift. Even with the combined effect of oxide- and interface-trapped charges, wide-channel *p*MOSFETs are still relatively radiation tolerant, showing an on-current loss of 20%, a negative threshold voltage shift of −50 mV, and a peak transconductancedegradation of 10%. The slight performance degradation of wide-channel *p*MOSFETs refers to charge trapping related to ultrascaled gate dielectrics.

Both narrow-channel *p*MOSFETs demonstrate serious performance degradation and eventually lose more than 50% of their drive current. This is partly due to a significant threshold voltage shift, i.e., −260 mV and −100 mV for long- and short-channel *p*MOSFETs, respectively. The V_T-shift-isolated on-current evolves as the peak transconductance. However, these two parameters are subject to both the low-field channel mobility degradation and the effective channel width reduction. The effects of TID on the effective channel width are related to RINCE and discussed in detail in Section 3.3.2. Short-channel *p*MOSFETs are more radiation tolerant than their long-channel counterparts. Compared with the narrow/long-channel *p*MOSFET, the narrow/short-channel one presents a 30% less on-current loss, a 160 mV less threshold voltage shift, and a 20% less reduction in the effective channel width and/or the

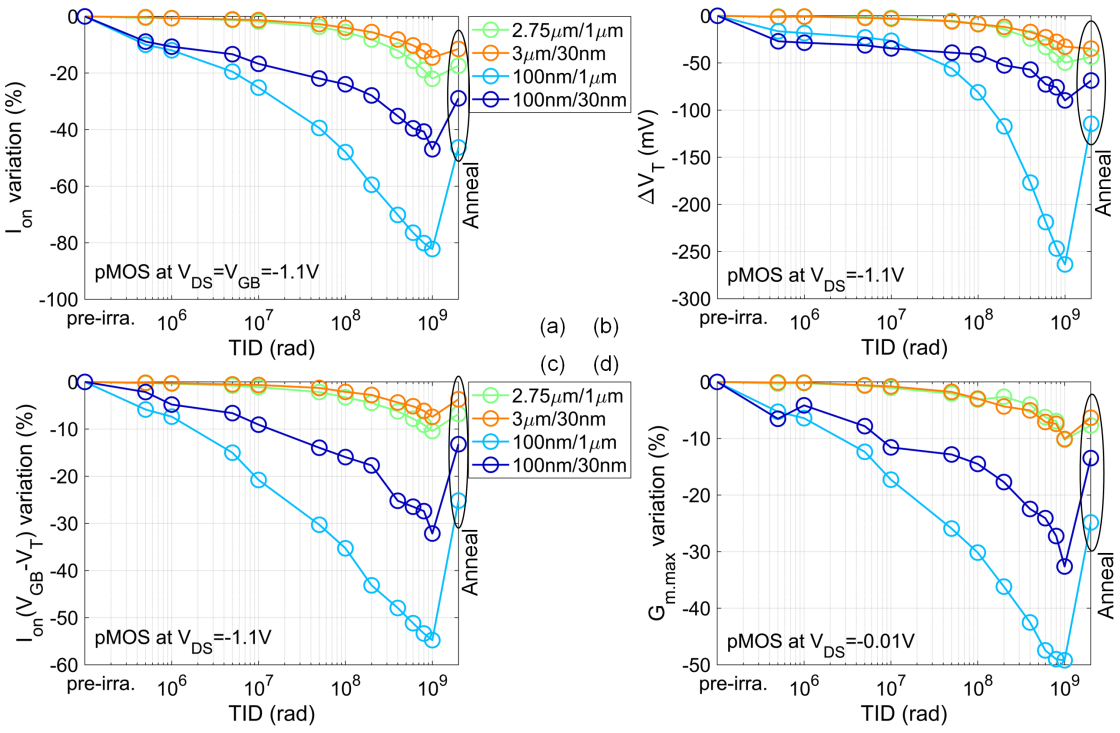


Figure 3.12 – TID effects on extracted parameters of four corner *p*MOSFETs, including (a) the on-current I_{on}, (b) the threshold voltage V_T, (c) the V_T-shift-isolated on-current $I_{on}(V_{GB}-V_T)$, and (d) the peak transconductance $G_{m.max}$.

low-field channel mobility. This improvement of the radiation tolerance with a short channel is related to reverse RISCE and is discussed in Section 3.3.2.

Off-current, subthreshold swing, DIBL, and on-to-off current ratio

Fig. 3.13 reports the TID-induced evolution of (a) the off-current extracted at a zero volt of V_{GB}, (b) the DIBL parameter, (c) the subthreshold swing, and (d) the on-to-off current ratio in saturation for four corner *n*MOSFETs. TID influences significantly the drain leakage current and the subthreshold region of the narrow/short-channel *n*MOSFET (Fig. 3.8d and Fig. 3.9d). This compromises the accuracy of the extraction of the DIBL parameter and the subthreshold swing, which are not included for the discussion of the smallest *n*MOSFET.

Four corner *n*MOSFETs undergo an off-current increase by a maximum of more than three orders of magnitude. The off-current is width independent and length dependent at high TID levels roughly from 10 Mrad for short-channel *n*MOSFETs and 50 Mrad for long-channel *n*MOSFETs. The width independence and the length dependence indicate the dominant contribution of the parasitic drain-to-source leakage current. The concept of the parasitic transistor induced by STI-trapped positive charges is elaborated in Section 3.3.1. The off-

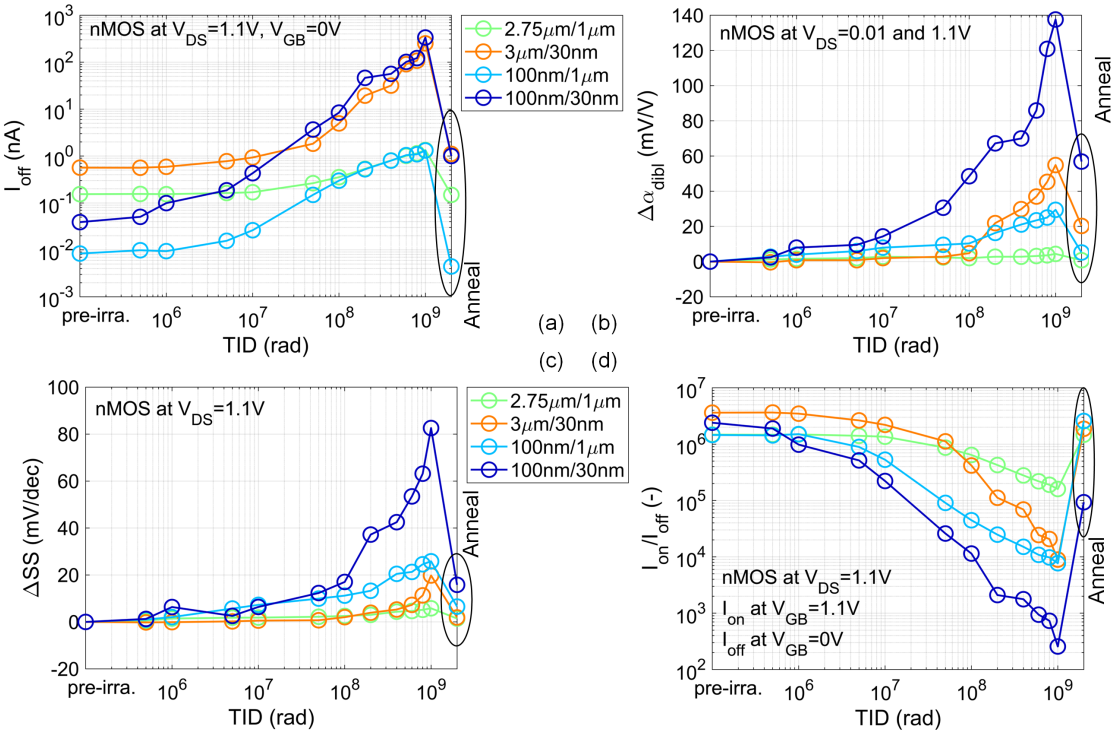
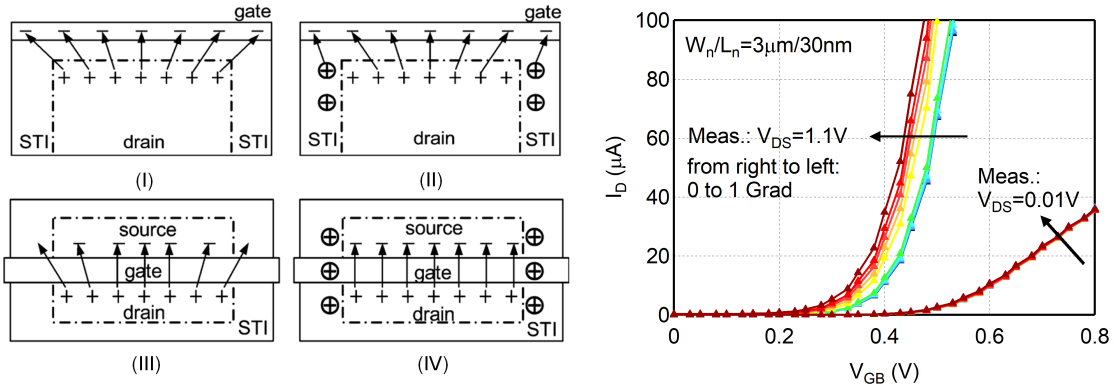


Figure 3.13 – TID effects on extracted parameters of four corner *n*MOSFETs, including (a) the off-current I_{off}, (b) the DIBL parameter α_{dibl}, (c) the subthreshold swing *SS*, and (d) the on-to-off current ratio I_{on}/I_{off}.



(a) Dipole theory of (I, II) the drain-to-gate coupling and (III, IV) the electric field pattern along STI sidewalls (I, III) before and (II, IV) after irradiation. (After Liu, et al. [187].)

(b) Measured $I_D - V_{GB}$ curves of the diode-biased wide/short-channel *n*MOSFET irradiated up to 1 Grad at room temperature. (After Zhang, et al. [121].)

Figure 3.14 – (a) Dipole theory illustrating the increased drain-to-source coupling and the more compact electric field pattern as a result of STI-trapped positive charges; (b) measured $I_D - V_{GB}$ curves of the wide/short-channel *n*MOSFET, highlighting the radiation-enhanced DIBL effect.

current of *n*MOSFETs increases slightly at low TID levels. This may be because STI-trapped positive charges are not yet strong enough to turn on the parasitic channels. The off-current at low TID levels is therefore likely to be mainly from the main channel.

DIBL is one of the most fundamental short-channel effects in nanoscale MOSFETs. The observed radiation-enhanced DIBL effect of *n*MOSFETs can be explained through an STI-related dipole theory proposed by Troutman [188] and an analysis of electrostatics near STI sidewalls [189]. As illustrated in Fig. 3.14a [187], positive charges trapped in STI oxides cut off the drain-to-gate fringing field and the weakened drain-to-gate coupling in turn enhances the drain-to-source coupling. Besides, these positive charges enhance electric field lines in the channel region near STI sidewalls and make the electric field lines near the center of the channel more compact. This may explain the radiation-enhanced DIBL effect in general cases.

Narrower- and shorter-channel *n*MOSFETs undergo an even higher increase in the DIBL parameter. For narrow-channel *n*MOSFETs, STI-trapped positive charges may be strong enough to lower down the nearby potential, significantly reducing the carrier barriers and further enhancing the DIBL effect. For short-channel *n*MOSFETs, STI-induced parasitic depletion regions may merge source and drain depletion regions, compromising short-channel engineering [185, 190] and increasing the DIBL parameter. Fig. 3.14b presents a negligible threshold voltage shift in linear and a continuously shifted threshold voltage in saturation for the wide/short-channel *n*MOSFET, suggesting the radiation-enhanced DIBL effect [121].

The subthreshold swing of *n*MOSFETs remains almost constant below 100 Mrad and eventually increases by a maximum of 25 mV/dec. This behavior of the subthreshold swing is consistent with the concomitant evolution of the threshold voltage, the low-field channel mobility, and

the drive current, corresponding to the buildup of negative interface-trapped charges along the gate oxide and STI-sidewalls. The significant drain leakage current increase reduces the on-to-off current ratio of the narrow/short-channel *n*MOSFET to less than three orders of magnitude, challenging its logic functions. Except the narrow/short-channel *n*MOSFET, all other *n*MOSFETs still have an on-to-off current ratio of more than three orders of magnitude, which can be sufficient for circuit design.

Fig. 3.15 reports the TID-induced evolution of those parameters of four corner *p*MOSFETs. Some measurement points in the switched-off state of the narrow/long-channel *p*MOSFET are not representative (Fig. 3.8g and Fig. 3.9g), making the extraction of its off-current at low TID levels inaccurate. Other *p*MOSFETs present a slight off-current increase by a maximum of tenfold. The off-current of *p*MOSFETs is neither width nor length dependent. As briefly explained in Section 3.3.1, the off-current increase of *p*MOSFETs is mainly attributed to a peripheral substrate-to-drain junction leakage current. In terms of the DIBL effect, STI-trapped positive charges influence *n*- and *p*MOSFETs oppositely. For *p*MOSFETs, both STI-trapped charges and image charges at the gate are positive, weakening the drain-to-source coupling and suppressing the DIBL effect. Especially, short-channel *p*MOSFETs display a reduced DIBL parameter. The subthreshold swing of short-channel *p*MOSFETs remains

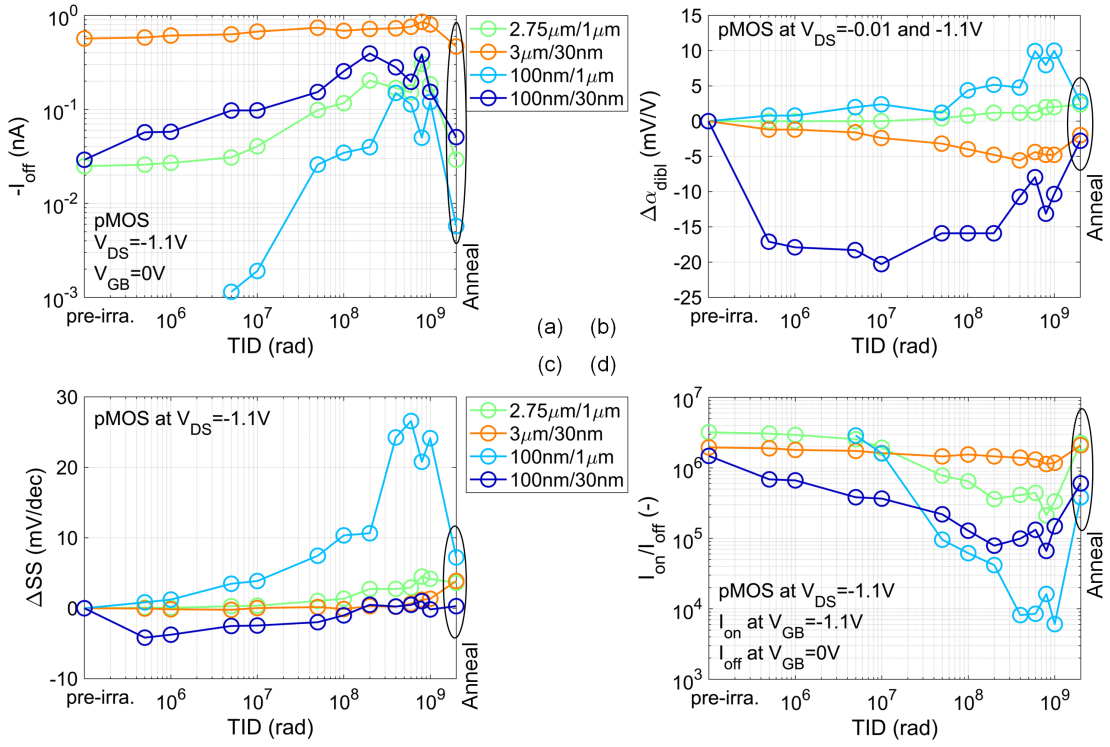


Figure 3.15 – TID effects on extracted parameters of four corner *p*MOSFETs, including (a) the off-current I_{off}, (b) the DIBL parameter α_{dibl}, (c) the subthreshold swing *SS*, and (d) the on-to-off current ratio $I_{\text{on}}/I_{\text{off}}$.

almost unaffected, indicating the strong radiation tolerance of highly scaled gate stacks. Long-channel *p*MOSFETs, especially the narrow/long-channel one, exhibit a slight subthreshold swing degradation at high TID levels, suggesting the buildup of positive interface-trapped charges near the surface channel along STI-sidewalls. Even though *p*MOSFETs suffer a high drive current loss, the on-to-off current ratio is still more than three orders of magnitude, leaving a sufficient margin for circuit design.

3.2.3 Post-irradiation annealing effects

Post-irradiation annealing is believed to annihilate oxide-trapped charges through bond reformation or neutralize them through electron tunneling [150, 152]. This annealing process can be accelerated by a positive gate-to-bulk bias and a high temperature [150, 152]. In some cases, interface-trap annealing happens below 100 °C [191]. However, a higher temperature is generally required to anneal interface traps efficiently [192]. The annealing of trapped charges in 28-nm bulk MOSFETs is seen relatively slow at room temperature in [120]. This allows us to neglect the annealing effect that may happen during less than one hour of measurements. Fig. 3.8 and Fig. 3.9 include results of the last room-temperature test after high-

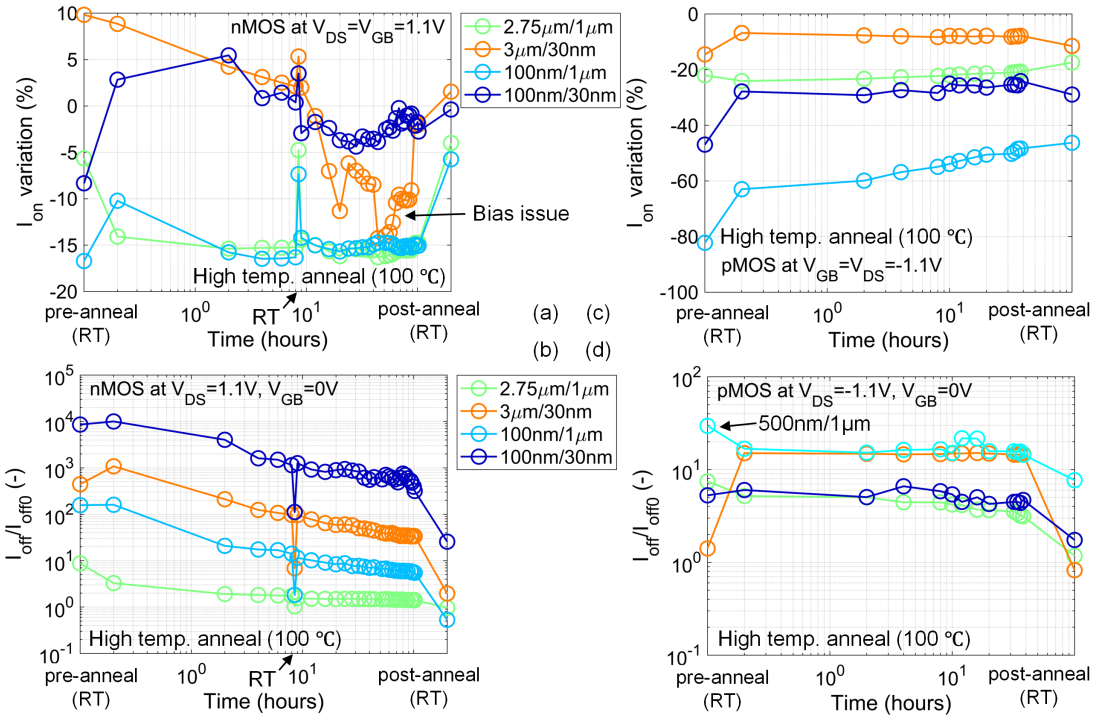


Figure 3.16 – Post-irradiation annealing effects on (a, c) the on-current I_{on} and (b, d) the off-current I_{off} of diode-biased (a, b) *n*- and (c, d) *p*MOSFETs at a high temperature (100 °C). Room-temperature (RT) results before and after annealing are included for a convenient comparison. Both I_{on} and I_{off} are referred to their pre-irradiation references at RT.

temperature annealing. The annealing almost completely recovers the radiation response of *n*MOSFETs and partly restores the electrical characteristics of *p*MOSFETs. This corresponds to the slight differences between pre-irradiation references and post-annealing values of crucial device parameters, as presented in Fig. 3.11, Fig. 3.12, Fig. 3.13, and Fig. 3.15. The less efficient annealing of the radiation response of *p*MOSFETs may be due to the negative gate-to-bulk bias, which is generally unfavorable for electrons to tunnel from the substrate to the gate oxide or STI oxides near the surface channel.

Fig. 3.16 summarizes the annealing-induced evolution of the on-current and the off-current of *n*- and *p*MOSFETs. The off-current of the *p*MOSFET with $W_p/L_p = 500\,\text{nm}/1\,\mu\text{m}$ is plotted, since the narrow/long-channel one does not have a pre-irradiation reference for the off-current. Room-temperature results before and after annealing are included to identify the effectiveness of high-temperature annealing. Unlike causing a more negative threshold voltage shift for 65-nm bulk MOSFETs [20, 21, 69, 75], high-temperature annealing recovers the performance of 28-nm bulk MOSFETs. In addition, the on-current and the off-current evolve very fast during the first hours of high-temperature annealing. For example, 8 hours of annealing has almost made long-channel *n*MOSFETs reach the final condition: an on-current loss of 5% and a negligible off-current increase. In contrast, short-channel *n*MOSFETs require 100 hours of annealing to reach a negligible on-current loss and an off-current increase by a maximum of 20 times. For *p*MOSFETs, 38 hours of high-temperature annealing recovers the on-current loss roughly by 50%. Especially, the on-current of the narrow/long-channel *p*MOSFET is recovered from 20% to 55% of the original level. High-temperature annealing also brings the off-current of *p*MOSFETs almost back to pre-irradiation references. However, narrow/long-channel *p*MOSFETs still demonstrate a slight off-current increase after high-temperature annealing. Overall, the performance recovery of 28-nm bulk MOSFETs can be explained by the annealing of STI-trapped positive charges.

3.2.4 Bias dependence of TID effects

In most analog circuits and particularly analog FE electronics, MOSFETs are biased in saturation with a nonzero V_{DS}. Therefore, irradiation experiments have been conducted first with the diode condition ($V_{GB} = V_{DS} = V_{DD}$ for *n*MOSFETs and $V_{GB} = V_{DS} = -V_{DD}$ for *p*MOSFETs). This bias condition applies a maximum electric field in both longitudinal and vertical directions, which can probably lead to a higher charge yield. It actually causes more damage to 65-nm bulk MOSFETs than other bias conditions [20] and is different from the historically worst bias case ($V_{GB} = V_{DD}$, $V_{DS} = 0\,\text{V}$ for *n*MOSFETs and $V_{GB} = V_{DS} = 0\,\text{V}$ for *p*MOSFETs) [193].

MOSFETs conduct a high drain current under the diode condition. To differentiate the effects from radiation and stress, control tests have been done under the same bias for a comparable period without irradiation. As presented in Fig. 3.17, non-irradiation stress barely damages the wide/short-channel *n*MOSFET or the narrow/long-channel *p*MOSFET [121]. The observed performance degradation is therefore attributed only to TID effects.

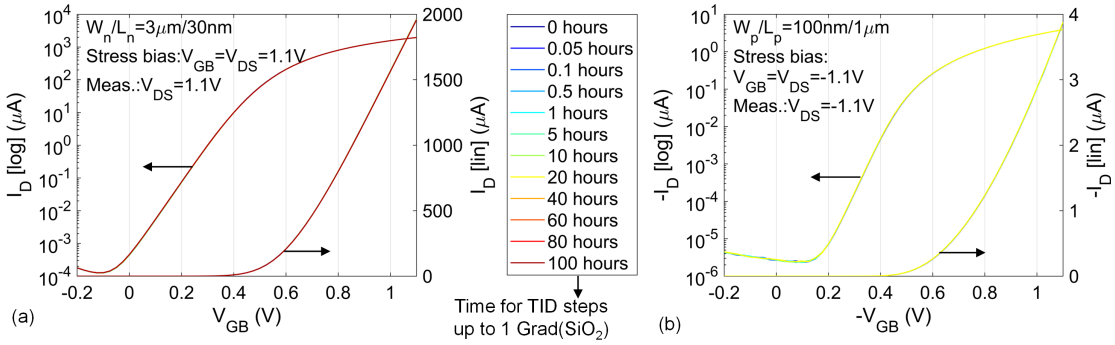


Figure 3.17 – Measured $|I_D| - |V_{GB}|$ curves in saturation operation ($|V_{DS}| = 1.1\,V$) of (a) the wide/short-channel *n*MOSFET and (b) the narrow/long-channel *p*MOSFET at room temperature (25 °C), indicating negligible non-irradiation stress-induced effect under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$). (After Zhang, et al. [121]).

Except for the diode condition, irradiation tests have also been done under other bias conditions, targeting the worse bias scenario for this 28-nm bulk CMOS process. The other two bias conditions are the switched-on condition ($|V_{GB}| = 1.1\,V$ and $V_{DS} = 0\,V$) with a maximum vertical electric field and the switched-off condition ($V_{GB} = 0\,V$ and $|V_{DS}| = 1.1\,V$) with a maxi-

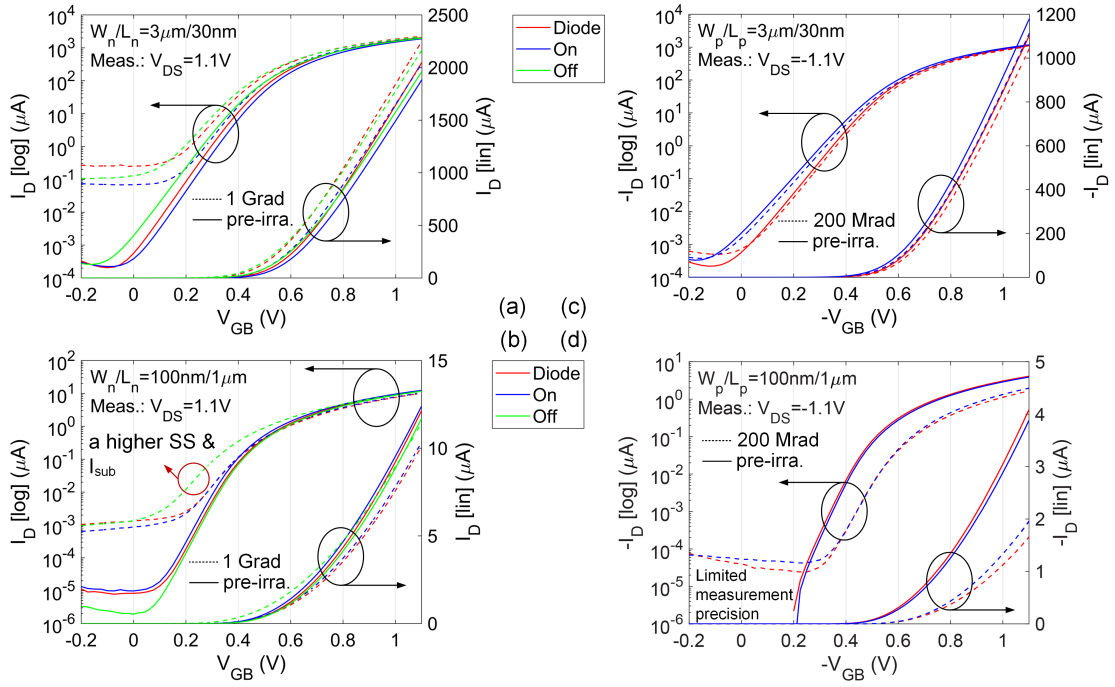


Figure 3.18 – Measured $|I_D| - |V_{GB}|$ curves in saturation operation ($|V_{DS}| = 1.1\,V$) of (a, c) wide/short- and (b, d) narrow/long-channel (a, b) *n*- and (c, d) *p*MOSFETs irradiated at room temperature (25 °C) under various bias conditions: diode ($|V_{GB}| = |V_{DS}| = 1.1\,V$), on ($|V_{GB}| = 1.1\,V$ and $V_{DS} = 0\,V$), and off ($V_{GB} = 0\,V$ and $|V_{DS}| = 1.1\,V$). (After Zhang, et al. [121]).

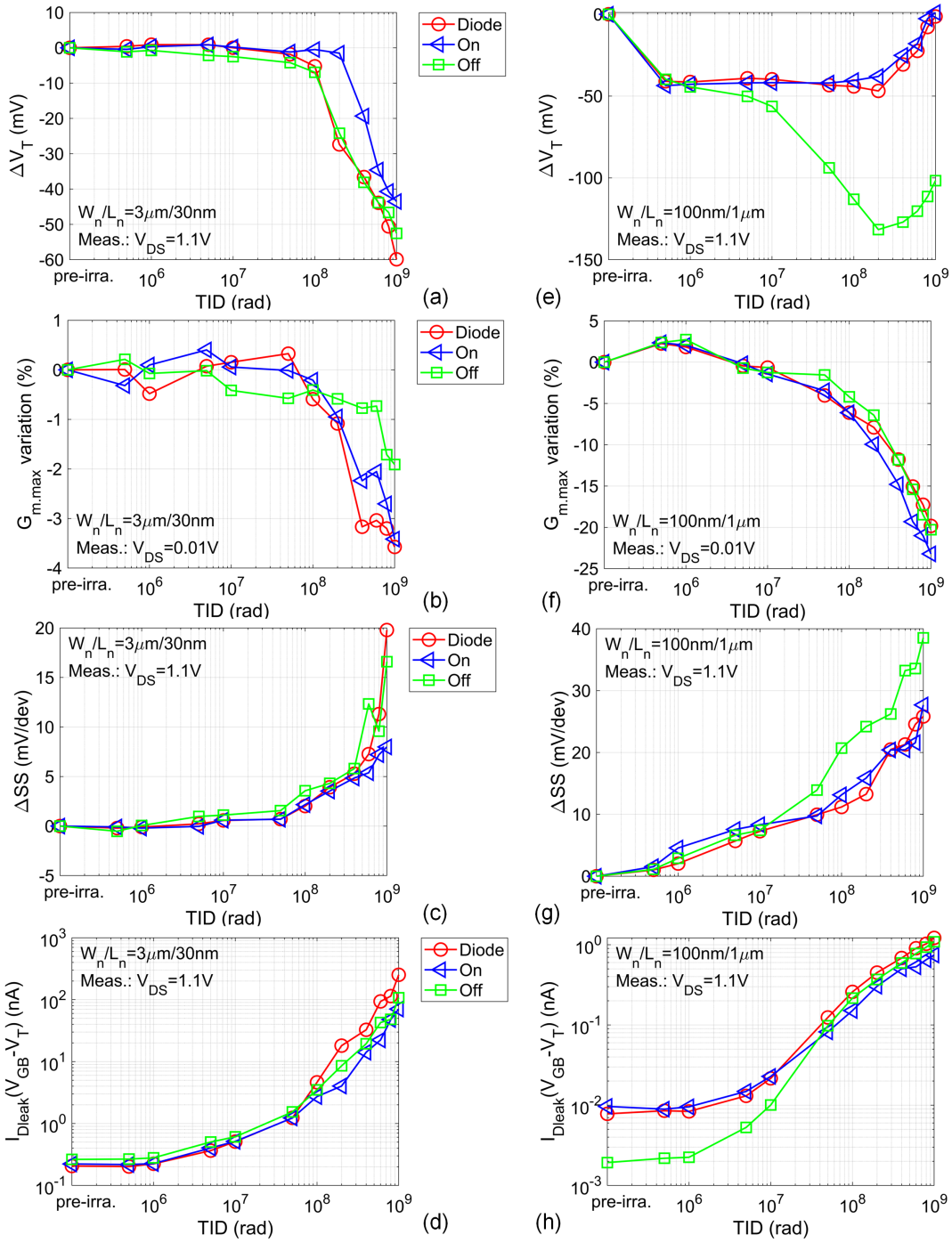


Figure 3.19 – Bias dependence of TID effects on parameters of (a-d) wide/short- and (e-h) narrow/long-channel *n*MOSFETs, including (a, e) the threshold voltage V_{T}, (b, f) the peak transconductance $G_{\mathrm{m.max}}$, (c, g) the subthreshold swing *SS*, and (d, h) the drain leakage current I_{Dleak}. (After Zhang, et al. [121].)

mum longitudinal electric field. Bear in mind that the initial chip-to-chip variability is around

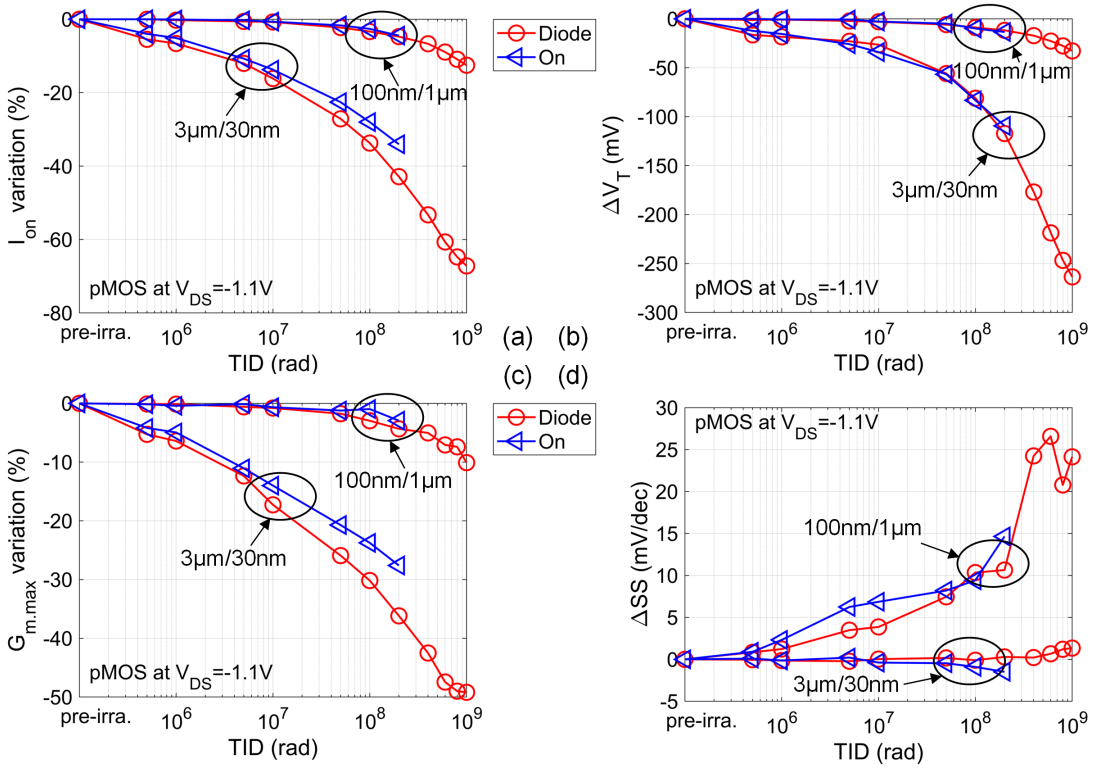


Figure 3.20 – Bias dependence of TID effects on parameters of wide/short- and narrow/long-channel *p*MOSFETs, including (a) the on-current I_{on}, (b) the threshold voltage V_T, (c) the subthreshold swing *SS*, and (d) the peak transconductance $G_{m.max}$. (After Zhang, et al. [121].)

6%. Fig. 3.18 reports the measured $|I_D| - |V_{GB}|$ curves in saturation operation ($|V_{DS}| = 1.1$ V) of wide/short- and narrow/long-channel *n*- and *p*MOSFETs irradiated under different bias conditions [121]. Experimental results of these bias conditions display slight differences for both geometries of *n*- and *p*MOSFETs except for a more stretched-out subthreshold region of *n*MOSFETs irradiated under the switched-off condition.

Fig. 3.19 summarizes the extracted device parameters, including the threshold voltage, the peak transconductance, the subthreshold swing, and the drain leakage current, of wide/short- and narrow/long-channel *n*MOSFETs irradiated under three bias conditions [121]. Fig. 3.20 reports the TID-induced evolution of the on-current, the threshold voltage, the peak transconductance, and the subthreshold swing of the same sizes of *p*MOSFETs irradiated under the diode and switched-on conditions [121]. In general, a longitudinal electric field affects the distribution of radiation-induced charge buildup along the channel length. However, the results of the diode and switched-on conditions present slight differences within the chip-to-chip variability. In contrast, the switched-off condition induces a more negative threshold voltage shift (Fig. 3.19e) and a more serious subthreshold swing degradation (Fig. 3.19f) for the narrow/long-channel *n*MOSFET. The switched-off condition can therefore be considered as the worst bias case for 28-nm bulk *n*MOSFETs.

This is probably because under a zero gate bias, radiation-generated holes in STI oxides tend to get trapped near the surface channel along STI sidewalls. Positive charges trapped in this region can be more effective in impacting the surface potential and thus reduce the threshold voltage more significantly. Moreover, together with moderate values of the gate bias, these positive charges can activate the parasitic channels close to the surface, adding a significant drain-to-source leakage to the subthreshold region. Considering the negligible difference in the peak transconductance variation under three bias conditions (Fig. 3.19h), the more serious subthreshold swing degradation under the switched-off condition (Fig. 3.19g) is attributed to

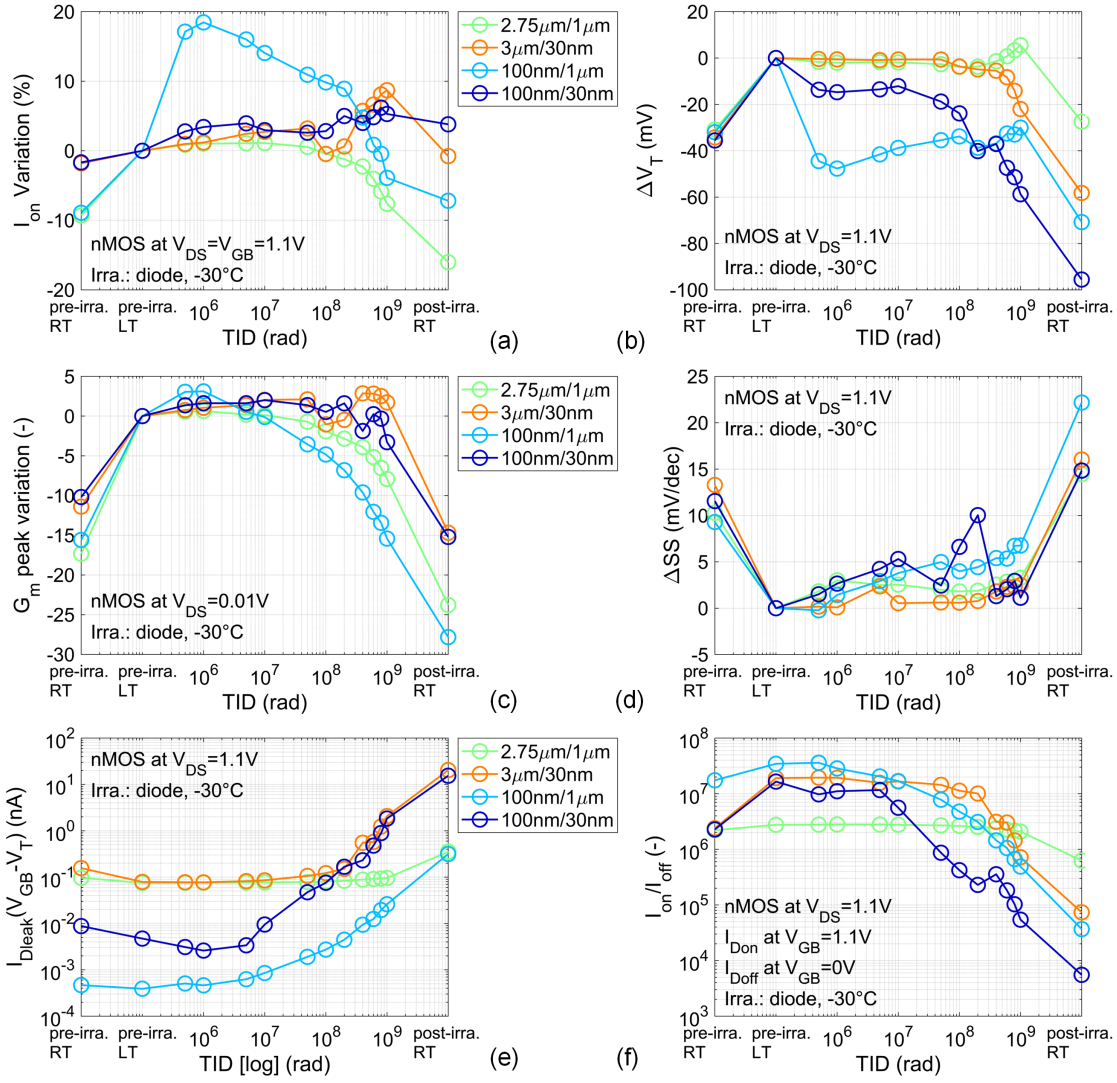


Figure 3.21 – TID effects on parameters of four corner *n*MOSFETs irradiated under the diode condition ($V_{GB} = V_{DS} = 1.1$ V) at a low temperature (–30 °C), including (a) the on-current I_{on}, (b) the threshold voltage V_T, (c) the peak transconductance $G_{m.max}$, (d) the subthreshold swing *SS*, (e) the drain leakage current I_{Dleak}, and (f) the on-to-off current ratio I_{on}/I_{off}.

STI-trapped positive charges near the surface channel instead of STI-related interface-charge trapping.

3.2.5 Temperature dependence of TID effects

Some components of CERN's experiments, especially the innermost detectors closest to collision points, operate at low temperatures between –30 °C and –20 °C. Therefore, another two irradiation experiments have been performed at –30 °C to examine the radiation response

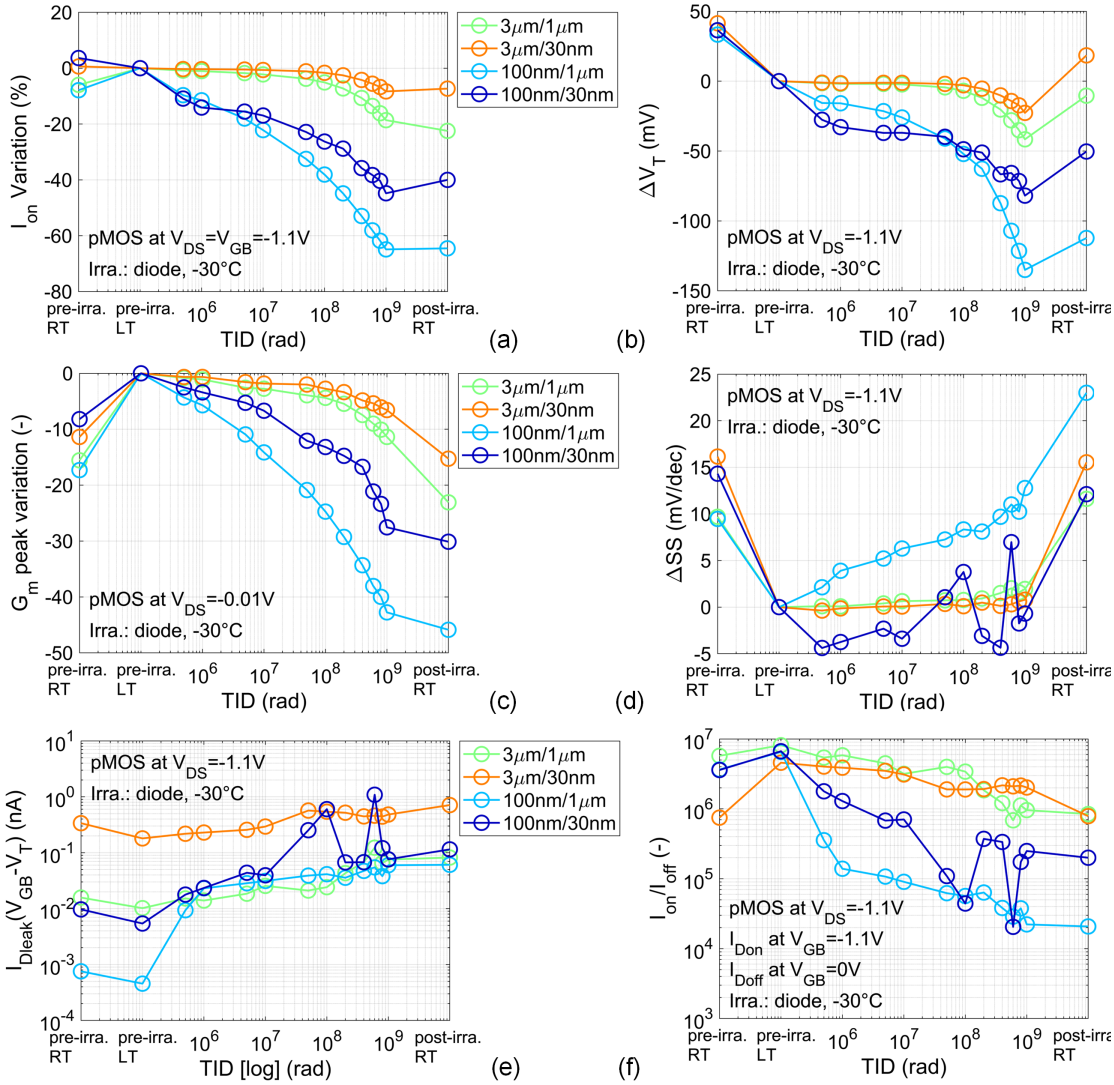


Figure 3.22 – TID effects on parameters of four corner *p*MOSFETs irradiated under the diode condition ($V_{GB} = V_{DS} = -1.1$ V) at a low temperature (–30 °C), including (a) the on-current I_{on}, (b) the threshold voltage V_T, (c) the peak transconductance $G_{m.max}$, (d) the subthreshold swing SS, (e) the drain leakage current I_{Dleak}, and (f) the on-to-off current ratio I_{on}/I_{off}.

of 28-nm bulk MOSFETs under operation conditions close to the real situation. Fig. 3.21 and Fig. 3.22 summarize crucial device parameters of *n*- and *p*MOSFETs extracted from low-temperature irradiation tests with the first and last points corresponding to room temperature. The differences between room- and low-temperature results originate from the temperature parameter itself, which will not be discussed here. Extracted results are referred to pre-irradiation low-temperature values.

When TID levels are below 100 Mrad, 28-nm bulk *n*MOSFETs demonstrate similar parametric shifts at two temperatures, indicating the common influence of STI-trapped positive charges. However, narrow-channel *n*MOSFETs irradiated at –30 °C for ultrahigh TID levels still have a negative threshold voltage shift and present a better current condition, implying less effective STI-related interface-charge trapping. In contrast, wide-channel *p*MOSFETs behave similarly at two temperatures, while narrow-channel *p*MOSFETs irradiated at –30 °C undergo smaller parametric shifts, indicating relieved STI-related interface-charge trapping. This is probably because radiation-generated holes tend to get trapped near their generation points at –30 °C, limiting the subsequent hole transport to the sensitive surface area and eventually the activation of H-passivated interface traps. Overall, both *n*- and *p*MOSFETs demonstrate a weak temperature dependence of TID effects and low-temperature ionizing irradiation generates a minor influence on 28-nm bulk MOSFETs.

3.3 Main experimental phenomena

28-nm bulk MOSFETs are seen radiation tolerant up to 1 Grad, except for some narrow-channel MOSFETs that go through considerable performance degradation and some *n*MOSFETs that suffer an undesirably high drain leakage. Since STI-related charge trapping is the dominant cause for ionizing radiation damage to 28-nm bulk MOSFETs, the observed radiation effects exhibit a strong channel width dependence. Even though measurement results do not reveal spacer-related TID effects that have been discovered for 65-nm bulk MOSFETs [20, 21, 69, 75], short-channel engineering results in a channel length dependence of TID effects. This section elaborates on major experimental observations, including the TID-induced drain leakage current and geometry dependence of TID effects.

3.3.1 TID-induced drain leakage current

28-nm bulk *p*MOSFETs present a slight off-current increase. As shown by the $|I_{D,S}| - |V_{GB}|$ curves of the wide/short-channel *p*MOSFET in Fig. 3.23a, the source current and the drain current are unequal at the switched-off state. Fig. 3.23b illustrates the detailed bias condition and possible leakage components at a maximum of V_{GB} ($V_{GB} = 0.2\,V$) in saturation ($V_{DS} = -1.1\,V$). The drain leakage current increase of *p*MOSFETs is believed to come from the peripheral substrate-drain junction leakage current. This current is associated with the surface generation at the intersection of the substrate-drain depletion region and STI sidewalls [194, 195], which is quantitatively discussed in Section 4.3.1.

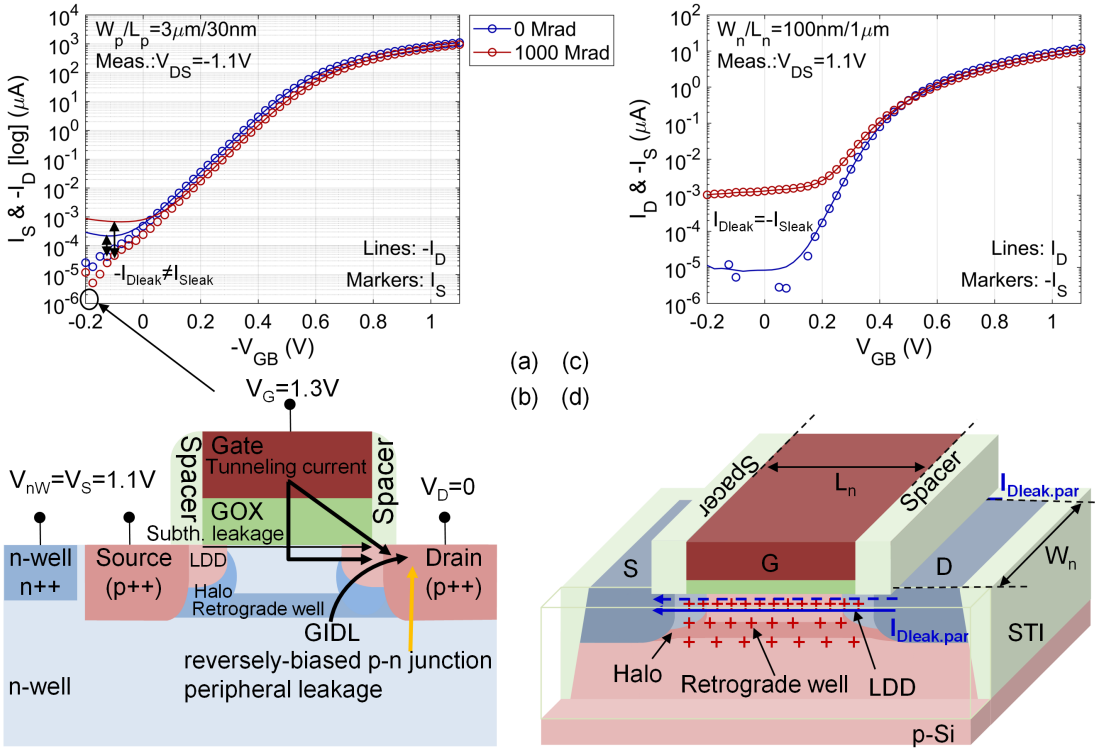


Figure 3.23 – Measurement results and schematic illustration of the TID-induced drain leakage current of 28-nm bulk MOSFETs: measured $|I_{D,S}|-|V_{GB}|$ curves in saturation operation ($|V_{DS}| = 1.1\,V$) of (a) the wide/short-channel *p*MOSFET and (c) the narrow/long-channel *n*MOSFET; cross sections of (b) *p*- and (d) *n*MOSFETs, illustrating the possible origins of the drain leakage current. In (d), the front face of the STI structure is represented by the light-green frame for making the channel doping profile and the distribution of STI-trapped positive charges (+ markers) visible. (After Zhang, et al. [120, 127].)

The off-current of *n*MOSFETs increases by a maximum of more than three orders of magnitude. As shown by the $I_{D,S} - V_{GB}$ curves of the narrow/long-channel *n*MOSFET in Fig. 3.23c, the drain current is equal to the source current, confirming the dominant drain-to-source leakage path. The width independence and the length dependence of the off-current at high TID levels, as indicated in Fig. 3.13a, suggest the dominant parasitic drain-to-source leakage current from both sides of the main channel. As illustrated in Fig. 3.23d, radiation-generated holes can get trapped in STI oxides, increasing the nearby surface potential and even inverting the channel edges. This forms a parasitic channel on each side of an *n*MOSFET, allowing two parasitic leakage currents to flow from the drain to the source along STI sidewalls [19, 59, 77, 78]. At low TID levels, STI-trapped positive charges may not be strong enough to generate parasitic channels.

The formation of TID-induced parasitic channels strongly depends on substrate doping profile and STI-trapped charge distribution [62, 196, 197]. Substrate doping profile is nonuniform

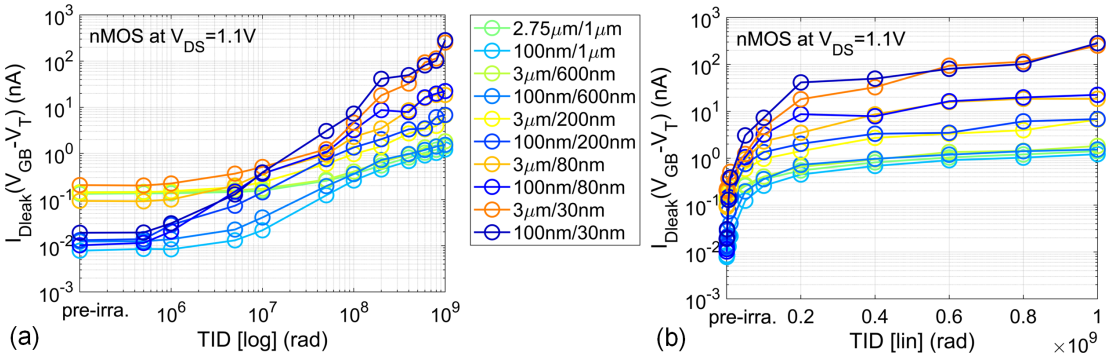


Figure 3.24 – Extracted drain leakage current of *n*MOSFETs as a function of TID, indicating the dominant contribution of the parasitic drain-to-source leakage current at high TID levels. (After Zhang, et al. [124].)

in both longitudinal and vertical directions in advanced CMOS technologies. The lower the doping concentration, the easier for STI-trapped positive charges to invert the adjacent semiconductor body. Therefore, special doping steps in advanced CMOS technologies, including the surface channel implantation for adjusting the threshold voltage and short-channel engineering with retrograde wells and halo implants, can be advantageous for inhibiting the drain leakage current increase of *n*MOSFETs. But clearly, these special doping techniques are still insufficient to prevent the STI-induced parasitic leakage. STI-trapped charge distribution is nonuniform as a result of the bias condition during irradiation. Moreover, the higher the gate bias, the more deeply radiation-generated holes may transport. This can explain the more stretched-out subthreshold region of narrow-channel *n*MOSFETs under the switched-off condition, as displayed by Fig. 3.18b. With a zero gate bias during irradiation, radiation-generated holes tend to be trapped near the surface channel. Parasitic channels at this location can then be activated together with the gate bias, adding a substantial leakage current to the subthreshold region and inducing a serious subthreshold swing degradation.

To better understand the leakage components, the drain leakage current of *n*MOSFETs is extracted at a constant $V_{GB} - V_T$ and plotted versus TID in log-log scale (Fig. 3.24a) and log-lin scale (Fig. 3.24b) [124]. Fig. 3.24a demonstrates a channel-width-dependent leakage at low TID levels, which flows through the main channel, and a channel-length-dependent leakage at high TID levels, which comes from the parasitic channels. In addition, the drain leakage current of *n*MOSFETs tends to saturate at certain TID levels, as presented in Fig. 3.24b. This saturation of the drain leakage current indicates the nearly complete filling of oxide traps in STI oxides and/or the compensation of STI-related negative interface-charge trapping.

3.3.2 Geometry dependence of TID effects

The radiation response of 28-nm bulk MOSFETs demonstrates a strong geometry dependence. The channel width dependence refers to STI-related charge trapping along channel edges,

while the channel length dependence can be explained by the influence of short-channel engineering [198, 199].

Channel width dependence

Fig. 3.25 reports the channel width dependence of the on-current variation versus TID in saturation operation ($|V_{DS}| = 1.1$ V) of long-channel MOSFETs. For long-channel *n*MOSFETs (Fig. 3.25a), it first increases and then decreases, corresponding to STI-trapped positive charges and negative interface-charge trapping along the gate oxide and STI sidewalls, respectively. As the channel narrows, *n*MOSFETs become more sensitive to STI-related charge trapping. The worst scenario is the narrowest/longest-channel *n*MOSFET with an on-current variation of 15%. In contract to *n*MOSFETs, the on-current of long-channel *p*MOSFETs (Fig. 3.25b) degrades continuously with TID. When the channel gets narrower, *p*MOSFETs go through a dramatic on-current loss due to STI-related charge trapping. The worst case is also the narrowest/longest-channel *p*MOSFET with an on-current loss of 15%. This substantial on-current loss is believed to be mainly a result of an effective channel width reduction.

The channel width dependence of TID effects is closely related to the dominant influence of STI-related charge trapping. Moreover, high total doses severely degrade the performance of narrow-channel MOSFETs through impacting the center of the channel. This is consistent with RINCE reported for 130-nm and 65-nm bulk CMOS technologies [18–21]. RINCE induced by STI-related charge trapping is illustrated in Fig. 3.26. In addition to contributing parasitic leakage currents to *n*MOSFETs, STI-trapped positive charges near the surface channel at the early radiation stage also interact with the region towards the center of the channel through depletion (Fig. 3.26a and Fig. 3.26e). When the channel gets narrower (Fig. 3.26c and Fig. 3.26g), an even larger portion of the channel is influenced. For narrow-channel *n*MOSFETs (Fig. 3.26c), RINCE makes the inversion of the corresponding channel region easier with a negative threshold voltage shift and contribute a considerable leakage to the

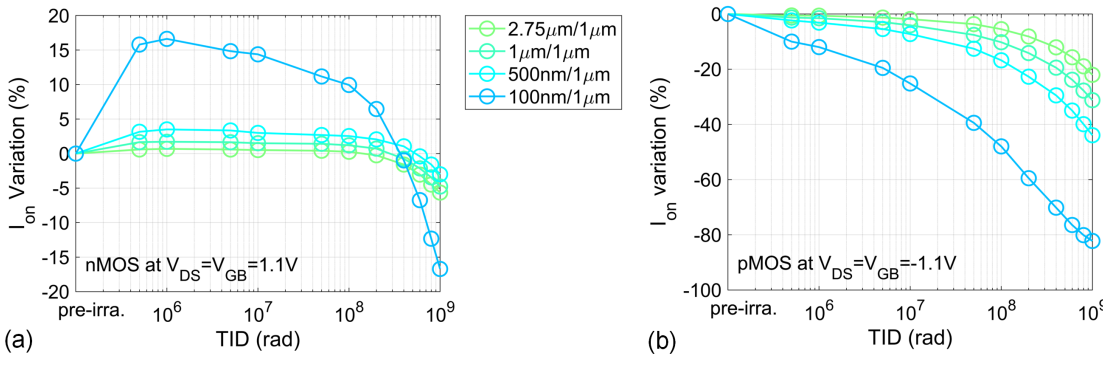


Figure 3.25 – TID-induced on-current variation in saturation operation ($|V_{DS}| = 1.1$ V) of long-channel (a) *n*- and (b) *p*MOSFETs, indicating the channel width dependence of TID effects and RINCE.

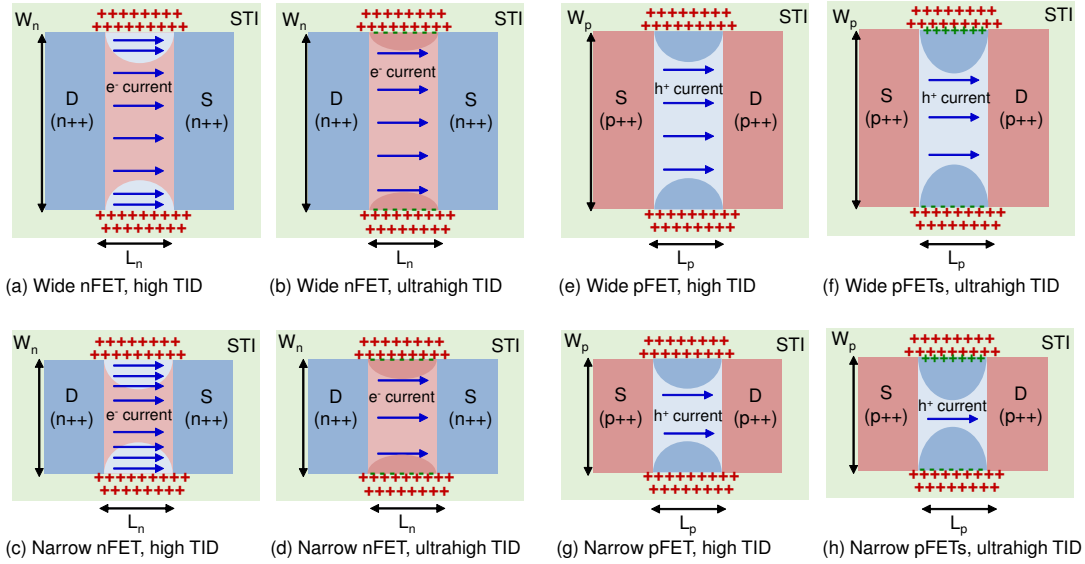


Figure 3.26 – Top views of (a, b, e, f) wide- and (c, d, g, h) narrow-channel (a-d) *n*- and (e-h) *p*MOSFETs along a longitudinal cut-plane right below the gate oxide, illustrating RINCE at (a, c, e, g) high and (b, d, f, h) ultrahigh TID levels. Blue arrowed lines represent the flowing current density. Curved areas identify inverted or non-inverted channel regions sensitive to STI-related charge trapping. Red symbols represent STI-trapped positive charges. Green symbols stand for interface-trapped charges, which are negative for *n*MOSFETs and positive for *p*MOSFETs.

subthreshold region. For narrow-channel *p*MOSFETs (Fig. 3.26g), RINCE makes the inversion of the corresponding channel region more difficult with a negative threshold voltage shift and possibly reduces the effective channel width. As depicted in Fig. 3.26b, Fig. 3.26d, Fig. 3.26f, and Fig. 3.26h for the later radiation stage, STI-related interface-charge trapping starts to influence MOSFET characteristics and makes the channel inversion more difficult. Since both oxide- and interface-trapped charges tend to cause a negative threshold voltage shift and reduce the effective channel width, narrow-channel *p*MOSFETs suffer a dramatic drive current loss. This explains the serious performance degradation of the narrowest/longest-channel *p*MOSFET. The effective channel width of *p*MOSFETs is quantitatively evaluated in Section 5.1.5.

Channel length dependence

Fig. 3.27 reports the channel length dependence of the on-current variation versus TID in saturation operation ($|V_{DS}| = 1.1\,V$) of narrow-channel MOSFETs. For narrow-channel *n*MOSFETs (Fig. 3.27a), it first increases and then decreases, corresponding to STI-trapped positive charges at the early radiation stage and STI-related negative interface-charge trapping at the later radiation stage. As the channel shortens, *n*MOSFETs get less sensitive to STI-related charge trapping. The narrowest/shortest-channel *n*MOSFET exhibits the strongest radiation tolerance with an

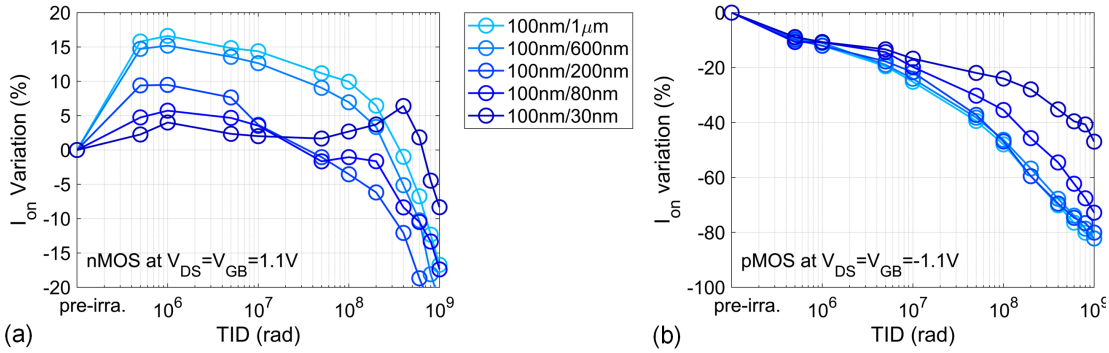


Figure 3.27 – TID-induced on-current variation in saturation operation ($|V_{DS}| = 1.1$ V) of narrow-channel (a) *n*- and (b) *p*MOSFETs, indicating the channel length dependence of TID effects and reverse radiation-induced short-channel effects (RISCE).

on-current loss of 9%. The on-current of narrow-channel *p*MOSFETs (Fig. 3.27b) degrades continuously with TID. When the channel gets short enough ($L < 100$ nm), *p*MOSFETs present a smaller on-current loss at high TID levels [$D > 1$ Mrad]. The narrowest/shortest-channel *p*MOSFET demonstrates the strongest radiation tolerance with an on-current loss of 50%.

Faccio et al. have discovered new RISCE related to spacers and explained these effects with a theory of charge generation in spacers and the subsequent evolution from spacers to the gate oxide [21,69]. The longitudinal bias during high-temperature annealing is believed to facilitate interface-charge trapping at one side of a MOSFET and lead to nonuniform interface-trapped charge distribution. This further degrades device performance through a more negative threshold voltage shift and results in asymmetric device behaviors. To examine if 28-nm bulk MOSFETs undergo the same effects, additional measurements have been carried out and analyzed under the diode condition. As shown in Fig. 3.16, neither types of 28-nm bulk MOSFETs present worse performance after high-temperature annealing. Forward (NOM)

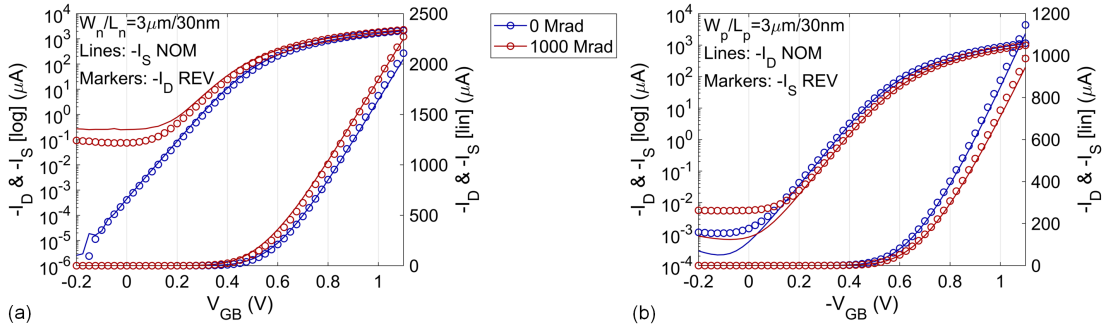


Figure 3.28 – Forward (NOM) and reverse (REV) transfer characteristics in saturation operation ($|V_{DS}| = 1.1$ V) of the wide/short-channel MOSFET of both (a) *n*- and (b) *n*-types, indicating no significant asymmetric behavior. Reverse measurements have the roles of the source and the drain interchanged. (After Zhang, et al. [121].)

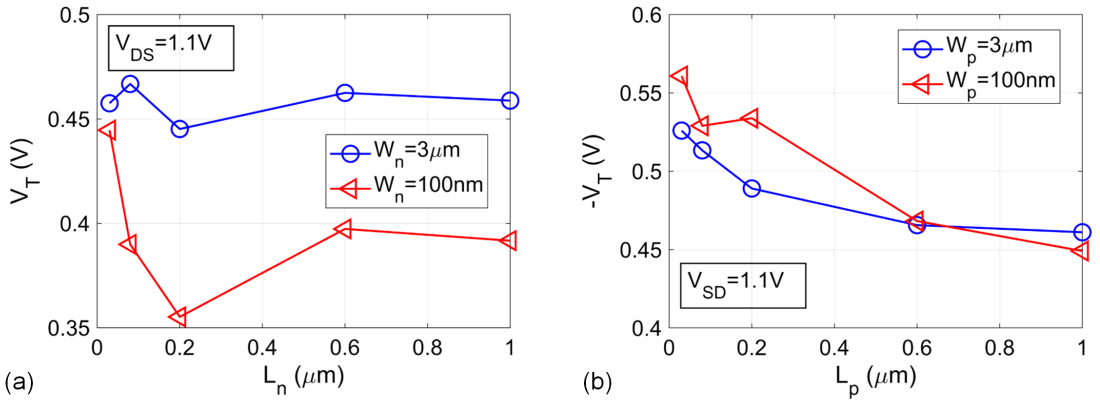


Figure 3.29 – Threshold voltage V_T versus the channel length L of fresh (a) *n*- and (b) *p*MOSFETs, indicating the halo-induced V_T roll-off. The V_T extraction uses measurements in saturation operation ($|V_{DS}| = 1.1\,V$) of MOSFETs at room temperature.

and reverse (REV) measurements of 28-nm bulk MOSFETs almost overlap each other, except for the asymmetric leakage current found at the switched-off state, as seen in Fig. 3.28. This asymmetry is probably related to the nonuniform distribution of STI-trapped positive charges under the longitudinal electric field. RISCE that occurs to 65-nm bulk MOSFETs does not notably influence 28-nm bulk MOSFETs. This may be due to improved spacer fabrication processes or a higher energy barrier between spacer materials and gate dielectrics. Since the fabrication information is absent, it is difficult to conclude this aspect.

Since device behaviors strongly depend on channel doping profile, a full understanding of the observed channel length dependence would require knowledge of the channel doping engineering adopted by a specific CMOS technology. In advanced CMOS technologies, special doping steps have been adopted for improving the performance of highly scaled MOSFETs. This channel doping engineering sometimes generates unexpected impacts on electrical behaviors of MOSFETs of typical sizes. For example, halo implants have been included in semiconductor processes to suppress the punchthrough of source and drain depletion regions [185, 190]. In the meantime, they induce the V_T roll-off, which is evident among short-channel MOSFETs [72]. Fig. 3.29 reports the threshold voltage of fresh wide- and narrow-channel 28-nm MOSFETs versus the channel length. These MOSFET arrays exhibit a higher $|V_T|$ when the channel gets short enough. This confirms the occurrence of the V_T roll-off in this 28-nm bulk CMOS process and suggests a higher average channel doping for short-channel MOSFETs.

Bonaldo et al. has proposed to explain the observed channel length dependence, which is particularly evident for *p*MOSFETs, through the halo-increased channel doping [198,199]. Fig. 3.30 illustrates the underlying mechanisms of the halo-induced reverse RISCE. For narrow-channel *n*MOSFETs, STI-trapped positive charges near the surface channel at the early radiation stage can be strong enough to interact with the region towards the center of the channel (Fig. 3.30a),

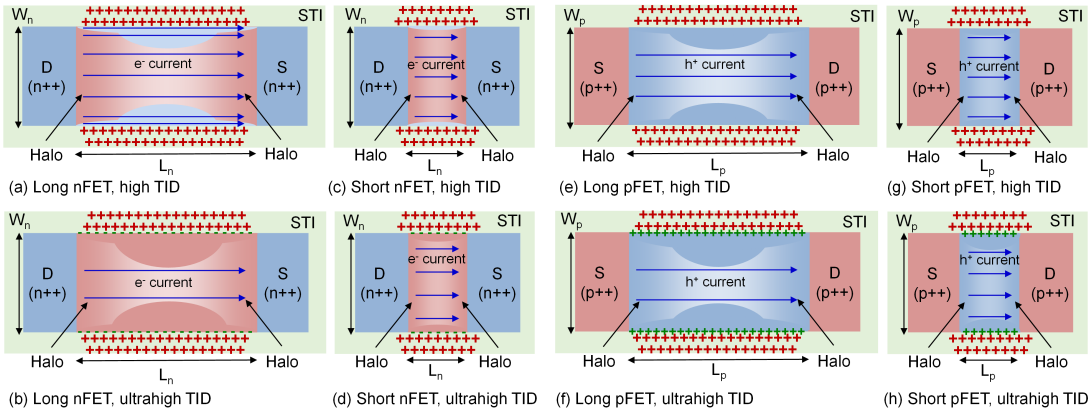


Figure 3.30 – Top views of (a, b, e, f) long- and (c, d, g, h) short-channel (a-d) *n*- and (e-h) *p*MOSFETs along a longitudinal cut-plane right below the gate oxide, illustrating the reverse RISCE at (a, c, e, g) high and (b, d, f, h) ultrahigh TID levels. Blue arrowed lines represent the flowing current density. Curved areas identify inverted or non-inverted channel regions sensitive to STI-related charge trapping. Red symbols represent STI-trapped positive charges. Green symbols stand for interface-trapped charges, which are negative for *n*MOSFETs and positive for *p*MOSFETs.

inducing a negative threshold voltage shift and a subthreshold current stretch-out. However, STI-trapped positive charges may not be strong enough to substantially influence the surface potential of short-channel *n*MOSFETs that have a halo-induced higher channel doping (Fig. 3.30c). Thus, short-channel *n*MOSFETs go through smaller parametric variations than their long-channel counterparts. Compared with long-channel *p*MOSFETs (Fig. 3.30e), the halo-increased channel doping of short-channel *p*MOSFETs (Fig. 3.30g) reduces the depleted lateral region induced by STI-trapped positive charges, suppressing RINCE. Halo implants also relieve the sensitivity of both *n*- and *p*MOSFETs to STI-related interface-charge trapping at the later radiation stage, as illustrated in Fig. 3.30b, Fig. 3.30d, Fig. 3.30f, and Fig. 3.30h.

3.4 Summary

Test structures, experimental setup, and measurement protocol have been detailed. Using CERN's X-ray irradiation system, test structures from a commercial 28-nm bulk CMOS process have been irradiated, annealed, and tested after each step of irradiation and annealing. Important experimental information is summarized here:

- Common pads between test structures in the same cluster make the isolation of intrinsic current components challenging. A complete analysis of all current components requires special measurement configurations and careful data processing.

- Test structures have been irradiated at room temperature (25 °C) and a low temperature (–30 °C) mainly at a dose rate of 10 Mrad/h for 4 days to reach 1 Grad and annealed at a

high temperature (100 °C) for at least 38 hours.

- During irradiation and annealing, test structures have been biased under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$), the switched-on condition ($|V_{GB}| = 1.1\,V$ and $V_{DS} = 0\,V$), or the switched-off condition ($V_{GB} = 0\,V$ and $|V_{DS}| = 1.1\,V$).
- DC measurements have been conducted after TID steps of 0-, 0.5-, 1-, 5-, 10-, 50-, 100-, 200-, 400-, 600-, 800-, and 1000 Mrad and every 2 hours during high-temperature annealing. For each measurement, a large amount of IV curves have been collected for investigating TID effects on all regions of device operation, including transfer characteristics $I_D(V_{GB})$ from linear ($|V_{DS}| = 0.01\,V$) to saturation ($|V_{DS}| = 1.1\,V$) and output characteristics $I_D(V_{DS})$ from depletion ($|V_{GB}| = 0.1\,V$) to strong inversion ($|V_{GB}| = 1.1\,V$).

The TID tolerance of this 28-nm bulk CMOS process has been studied through an investigation of the radiation response of MOSFETs of various sizes under different experimental conditions. Following the grasp of dominant damage mechanisms, main experimental observations, including the TID-induced drain leakage current, RINCE, and RISCE, are discussed. Important experimental results are summarized here:

- This 28-nm bulk CMOS process is quite tolerant to TID up to 1 Grad, except for the significant drain leakage current of *n*MOSFETs and the serious performance degradation of narrow-channel *p*MOSFETs. Wide-channel MOSFETs present slight parametric shifts at the switched-on region, suggesting insignificant charge trapping related to ultrathin gate dielectrics. Spacer-related charge trapping does not show an obvious influence on 28-nm bulk MOSFETs probably due to improved spacer fabrication processes or high energy barriers between spacer materials and gate dielectrics. STI-related charge trapping mainly explains ionizing radiation damage to 28-nm bulk MOSFETs.
- TID effects on 28-nm bulk MOSFETs demonstrate a strong geometry dependence, which is particularly evident for *p*MOSFETs. Due to the dominant influence of STI-related charge trapping, the radiation response of 28-nm bulk MOSFETs presents a channel width dependence and narrow-channel MOSFETs degrade more as a result of RINCE. The overlapped halo implants in short-channel MOSFETs lead to reverse RISCE, making short-channel MOSFETs more radiation tolerant than their long-channel counterparts.
- The rebound behavior of narrow-channel *n*MOSFETs suggests the dominant influence of STI-trapped positive charges below 100 Mrad and negative interface-trapped charges along the gate oxide and STI sidewalls at ultrahigh TID levels. The compensation of oxide- and interface-trapped charges at ultrahigh TID levels enables *n*MOSFETs to function well up to 1 Grad. In contrast, STI-related charge trapping contributes a significant parasitic drain-to-source leakage current to the drain leakage current of *n*MOSFETs, which however can be efficiently removed by high-temperature annealing.
- Both oxide- and interface-trapped charges are positive for *p*MOSFETs, making them more sensitive to total ionizing radiation. Due to RINCE, narrow-channel *p*MOSFETs

undergo the severest performance degradation with a drive current loss by more than 50%, which however can be partly recovered by high-temperature annealing. Besides, STI-related RINCE can be relieved by shortening the channel thanks to the halo-induced reverse RISCE.

- The switched-off condition ($V_{GB} = 0\,V$ and $V_{DS} = 1.1\,V$), inducing a more negative threshold voltage shift and a considerable subthreshold current, may be the worst bias case for *n*MOSFETs. However, it is not straightforward to tell which bias condition is the worst for *p*MOSFETs. Besides, irradiation tests at –30 °C, which is close to the real working temperature of the innermost electronics in the HL-LHC experiments, show an overall minor influence of TID on 28-nm bulk MOSFETs.

- The geometry dependence of TID effects on 28-nm bulk MOSFETs provides useful information for designers to choose appropriate devices for their design. For both *n*- and *p*MOSFETs, it is suggested to avoid using the narrowest channel ($W_{min} = 100\,nm$). If the narrowest channel is necessary, the width-to-length ratio should be over one ($W/L > 1$) to take advantage of the halo-induced higher channel doping.

4 Investigation of TID effects on design parameters

Previous studies have shown the effects of ultrahigh TID levels on crucial device parameters of 28-nm bulk MOSFETs. These parametric shifts are attributed to radiation-induced charge trapping particularly related to the gate oxide and thick STI oxides. This chapter investigates the effects of TID on design parameters of 28-nm bulk MOSFETs and introduces the first attempt of modeling the observed radiation effects. The simplified EKV MOSFET model is employed to study the effects of TID on analog parameters and to evaluate the influence of TID on static characteristics. The effects of TID on the effective channel mobility is then investigated using Y-function. Total ionizing radiation increases the drain leakage current of both *n*- and *p*MOSFETs, whose origins are identified through an experimental investigation of MOSFETs of various sizes. The parasitic drain-to-source leakage current may be the most serious problem when it comes to the use of 28-nm bulk *n*MOSFETs in radiation-tolerant circuits. To better account for its influence on power consumption, a semi-empirical physics-based model is proposed to simulate the leakage level as a function of TID. The parasitic drain-to-source leakage current is also investigated through a gateless charge-controlled model. This chapter is mainly based on results published in [122–124].

4.1 Investigation of TID effects on inversion operation

Since the experimental characterization focuses on parametric variations, device parameters have been extracted individually without considering the practical aspect of circuit design. Extracted parameters do not necessarily complete the calculation of the drain current. As a first step towards the characterization of design parameters and static characteristics in the radiation scenario, this section utilizes the simplified EKV MOSFET model for describing the large- and small-signal characteristics of 28-nm bulk MOSFETs over the whole inversion region [122]. This section first describes the main features of the simplified EKV MOSFET model and explains the associated parameter extraction methodology. It then illustrates the TID-induced evolution of model parameters, intrinsic gain, and transconductance efficiency. This section exploits measurements on two chips from the first tape-out irradiated under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$) at room temperature (25 °C).

4.1.1 The simplified EKV MOSFET model

In saturation, which is the most exploited region for analog circuits, the EKV charge-based MOSFET model can be simplified for helping designers explore the design space and make optimal trade-offs [110, 111, 114, 115]. The simplified EKV MOSFET model uses only four parameters and is expressed with very simple formulas. It introduces the inversion coefficient *IC* as an essential design parameter that spans the entire range of operating points from weak to strong inversion. As opposed to the conventional degrees of freedom in circuit design–the overdrive voltage $V_{GB} - V_T$, the channel width W, and the channel length L, the inversion coefficient *IC* provides a direct measure of the channel inversion level and offers an efficient way to evaluate the transconductance efficiency, allowing circuit design to be freely done in any inversion region [112]. Some design work in the literature has been conducted for low-power analog and RF circuits using this concept [200–202].

Definition of the inversion coefficient

The inversion coefficient *IC* is defined as the normalized drain current in saturation at a high drain bias [114]:

$$IC \triangleq i_d \triangleq \frac{I_D|_{saturation}}{I_{spec}}, \tag{4.1}$$

based on which the saturation operation of a MOSFET is classified as

$$\begin{aligned} IC &\leq 0.1 \quad \text{weak inversion (WI)} \\ 0.1 < IC &\leq 10 \quad \text{moderate inversion (MI)} \\ IC &> 10 \quad \text{strong inversion (SI).} \end{aligned}$$

In Eq. (4.1), the normalizing factor I_{spec}, called the specific current, is one of the most important model parameters. It is defined as

$$I_{spec} = 2n\beta U_T^2 = I_{spec\square}\frac{W}{L} \qquad \text{with} \tag{4.2a}$$

$$\beta = \mu_0 C_{ox}\frac{W}{L} \qquad \text{and} \tag{4.2b}$$

$$I_{spec\square} \triangleq 2n\mu_0 C_{ox} U_T^2, \tag{4.2c}$$

where $I_{spec\square}$ is defined as the specific current per square, n is the slope factor linking to the subthreshold swing by $SS = nU_T \ln 10$, $U_T = kT/q$ is the thermal voltage, k is the Boltzmann constant, and T is the operating temperature. The specific current per square $I_{spec\square}$ is referred to as the technology current since it is a constant for a given technology, a certain temperature, and any device dimensions. Therefore, The normalized drain current i_d, i.e., the inversion coefficient *IC*, is stripped off any geometry, temperature, and technology dependence.

Current-charge relation

One of the most important model equations in the EKV charge-based MOSFET model is the current-charge relation. In the EKV MOSFET model, the derivation of the drain current relies on the classical drift-diffusion transport model. One key step is to linearize the inversion charge density Q_i as a function of the surface potential Ψ_s [96]:

$$-\frac{Q_\mathrm{i}}{C_\mathrm{ox}} = n(\Psi_\mathrm{P} - \Psi_\mathrm{s}), \tag{4.3}$$

where Ψ_P is the pinch-off potential at which the inversion charge density Q_i becomes zero. This is an approximate expression of the solution solved from boundary conditions. Substituting the surface potential with the linearized inversion charge density in the normalized drift-diffusion transport expression and integrating the normalized drain current from the source to the drain in the charge domain give the expression of the net normalized drain current [96]:

$$i_\mathrm{d} \triangleq i_\mathrm{f} - i_\mathrm{r} = q_\mathrm{s} + q_\mathrm{s}^2 - \left(q_\mathrm{d} + q_\mathrm{d}^2\right), \tag{4.4}$$

where $i_\mathrm{f,r} = q_\mathrm{s,d} + q_\mathrm{s,d}^2$ corresponds to the normalized forward or reverse component of the drain current, $q_\mathrm{s,d} \triangleq Q_\mathrm{iS,iD}/Q_\mathrm{spec}$ is the normalized inversion charge density at the source or drain end of the channel, and Q_spec is the specific charge

$$Q_\mathrm{spec} \triangleq -2nU_\mathrm{T}C_\mathrm{ox}. \tag{4.5}$$

The square term, i.e., $q_\mathrm{s}^2 - q_\mathrm{d}^2$, corresponds to strong inversion and the linear term, i.e., $q_\mathrm{s} - q_\mathrm{d}$, refers to weak inversion.

This full current-charge equation can be simplified in saturation, where the drain side of a long channel is depleted of carriers and the carrier velocity saturates close to the drain side of a short channel. More specifically, the inversion charge density at the drain side of a long channel is pinched-off to zero ($q_\mathrm{d} = 0$) and the drain current only relies on the inversion charge density at the source end of the channel ($i_\mathrm{d} = q_\mathrm{s}^2 + q_\mathrm{s}$). When the channel shortens, the carrier velocity saturates at a particular value v_sat and the inversion charge density at the drain approaches a saturated value q_dsat. In a velocity saturated device, the channel current at the drain saturates at i_dsat, limiting the current in the entire channel to be i_dsat due to the current continuity and degrading the transconductance in strong inversion of saturation operation. The "sat" subscript of q_dsat and i_dsat is only for emphasizing the situation of velocity saturation (VS), which are interchangeable with q_d and i_d, respectively.

The effect of VS is certainly one of the most important short-channel effects. It has been included in the simplified EKV MOSFET model via the VS parameter and is defined as [113,203]

$$\lambda_\mathrm{c} \triangleq \frac{L_\mathrm{sat}}{L}, \tag{4.6}$$

which scales with the inverse of the channel length. Here, L_sat represents the portion of the

channel where the drift velocity of the inversion charge fully saturates and is defined as

$$L_{\mathrm{sat}} \triangleq \frac{2\mu_0 U_{\mathrm{T}}}{v_{\mathrm{sat}}}. \tag{4.7}$$

Introducing the simple piecewise mobility model into the classical drift-diffusion transport model and repeating the derivation for Eq. (4.4) yield the expressions of the saturated inversion charge at the drain side of the channel q_{dsat} and the saturated drain current i_{dsat} [113, 203]:

$$q_{\mathrm{dsat}} = \frac{2\lambda_{\mathrm{c}}\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2\right)}{2 + \lambda_{\mathrm{c}} + \sqrt{4\left(1+\lambda_{\mathrm{c}}\right) + \lambda_{\mathrm{c}}^2\left(1+2q_{\mathrm{s}}\right)^2}}, \tag{4.8a}$$

$$i_{\mathrm{dsat}} = \frac{4\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2\right)}{2 + \lambda_{\mathrm{c}} + \sqrt{4\left(1+\lambda_{\mathrm{c}}\right) + \lambda_{\mathrm{c}}^2\left(1+2q_{\mathrm{s}}\right)^2}}. \tag{4.8b}$$

Two asymptotes of i_{dsat} can be obtained from Eq. (4.8b) in weak and strong inversion:

$$\text{weak inversion}\left(q_{\mathrm{s}} \ll 1\right): \qquad i_{\mathrm{dsat}} \approx \frac{q_{\mathrm{s}}}{1+\lambda_{\mathrm{c}}/2}, \tag{4.9a}$$

$$\text{strong inversion}\left(\lambda_{\mathrm{c}} q_{\mathrm{s}} \gg 1\right): \qquad i_{\mathrm{dsat}} \approx \frac{2q_{\mathrm{s}}}{\lambda_{\mathrm{c}}}. \tag{4.9b}$$

When accounting for the effect of VS, the saturated drain current in strong inversion becomes proportional to q_{s} instead of q_{s}^2.

Charge-voltage relation

The EKV charge-based MOSFET model has another important equation that links the inversion charge density to the applied voltages. It is solved from 1-D Poisson's equation with the approximate solution to boundary conditions [96]. The normalized form of the charge-voltage relation is given by

$$2q_{\mathrm{i}} + \ln q_{\mathrm{i}} = v_{\mathrm{p}} - v, \tag{4.10}$$

where $q_{\mathrm{i}} \triangleq Q_{\mathrm{i}}/Q_{\mathrm{spec}}$ is the normalized inversion charge density, $v_{\mathrm{p}} \triangleq V_{\mathrm{P}}/U_{\mathrm{T}}$ is the normalized pinch-off voltage with

$$V_{\mathrm{P}} \cong \frac{V_{\mathrm{GB}} - V_{\mathrm{T}}}{n} \tag{4.11}$$

approximating the pinch-off voltage, V_{T} is the equilibrium threshold voltage at a zero volt of the channel voltage ($V_{\mathrm{ch}} = 0\,\mathrm{V}$), and $v \triangleq V_{\mathrm{ch}}/U_{\mathrm{T}}$ is the normalized channel voltage. The channel voltage V_{ch} expresses the split of quasi-Fermi levels with $V_{\mathrm{ch}} = (E_{\mathrm{Fn}} - E_{\mathrm{Fp}})/q$. It is equal to the source-to-bulk voltage V_{SB} at the source and the drain-to-bulk voltage V_{DB} at the drain. The linear term, i.e., $2q_{\mathrm{i}}$, corresponds to strong inversion and the logarithmic term, i.e., $\ln q_{\mathrm{i}}$, refers to weak inversion.

In saturation, $q_d = 0$ for a long-channel device and q_{dsat} is expressed as a function of q_s through Eq. (4.8a) for a short-channel device. Therefore, the drain current can be solved through the inversion charge density at the source side of the channel q_s, which links to the external voltages by

$$2q_s + \ln q_s = v_p - v_s \tag{4.12}$$

with $v_s \triangleq V_{SB}/U_T$ as the normalized source-to-bulk voltage. However, Eq. (4.12) cannot be inverted to express q_s as a function of v_s and v_g, where $v_g \triangleq V_{GB}/U_T$ is the normalized gate-to-bulk voltage.

Current-voltage relation

To obtain an expression of the drain current versus the external voltages from Eq. (4.4) or Eq. (4.8b), an expression of the inversion charge density versus the external voltages is needed, which however cannot be obtained analytically from Eq. (4.12). The current-voltage relation is therefore obtained reversely from Eq. (4.4) or Eq. (4.8b) to Eq. (4.12).

Reverting Eq. (4.8b) gives an expression of the inversion charge density at the source end of the channel q_s versus the saturated drain current i_{dsat} [113, 203]:

$$q_s = \frac{\sqrt{4i_{dsat} + (1 + \lambda_c i_{dsat})^2} - 1}{2}. \tag{4.13}$$

The combination of Eq. (4.12) and Eq. (4.13) generates the current-voltage expression that accounts for the effect of VS:

$$v_p - v_s = \sqrt{4i_{dsat} + (1 + \lambda_c i_{dsat})^2} + \ln\left[\sqrt{4i_{dsat} + (1 + \lambda_c i_{dsat})^2} - 1\right] - (1 + \ln 2). \tag{4.14}$$

Setting $\lambda_c = 0$ in Eq. (4.14) brings Eq. (4.14) back to its long-channel counterpart, which can be obtained by solving Eq. (4.4) and Eq. (4.12). Hence, the drain current in saturation is modeled through the simple equation Eq. (4.14) with only four model parameters, i.e., the slope factor n, the specific current per square $I_{spec\square}$, the threshold voltage V_T, and the VS parameter λ_c.

Small-signal characteristics

Small-signal characteristics of a MOSFET have been well considered in the EKV charge-based MOSFET model. Small-signal parameters and related figures-of-merit (FOMs) together with their asymptotes provide an efficient approach for the extraction of model parameters. To make the parameter extraction methodology in Section 4.1.2 more comprehensible, important steps of the small-signal model derivation are summarized here.

The most important small-signal parameter is the gate transconductance $G_m = \partial I_D/\partial V_{GB}$.

Since the terminal voltages in the EKV MOSFET model are all referred to the bulk, two other transconductances are defined, i.e., the source transconductance $G_{ms} = \partial I_D/\partial V_{SB}$ and the drain transconductance $G_{md} = \partial I_D/\partial V_{DB}$. Taking into account the first-order derivative of Eq. (4.10), the normalized form of these transconductances is defined as [96]

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = -\frac{\partial i_d}{\partial v_s} = -\frac{\partial i_d}{\partial q_s}\frac{\partial q_s}{\partial v_s}, \tag{4.15a}$$

$$g_{md} \triangleq \frac{G_{md}}{G_{spec}} = \frac{\partial i_d}{\partial v_d} = \frac{\partial i_d}{\partial q_d}\frac{\partial q_d}{\partial v_d}, \tag{4.15b}$$

$$g_m \triangleq \frac{G_m}{G_{spec}} = \frac{\partial i_d}{\partial v_g} = \frac{\partial i_d}{\partial v_p}\frac{\partial v_p}{\partial v_g} = \frac{\partial v_p}{\partial v_g}\left(\frac{\partial i_d}{\partial q_s}\frac{\partial q_s}{\partial v_p} + \frac{\partial i_d}{\partial q_d}\frac{\partial q_d}{\partial v_p}\right) = \frac{g_{ms} - g_{md}}{n}, \tag{4.15c}$$

where G_{spec} is the specific transconductance and defined as

$$G_{spec} \triangleq \frac{I_{spec}}{U_T} = 2n\beta U_T. \tag{4.16}$$

In saturation, $g_{md} = 0$ and $g_{ms} = ng_m$. In the case of VS, the normalized source transconductance g_{ms} is solved as a function of q_s by introducing the first-order derivative of Eq. (4.8b) and Eq. (4.12) into Eq. (4.15a) [113, 203]:

$$g_{ms} = \frac{2q_s}{\sqrt{4(1+\lambda_c) + \lambda_c^2(1+2q_s)^2}}. \tag{4.17}$$

Two asymptotes of g_{ms} can be obtained from Eq. (4.17) in weak and strong inversion:

$$\text{weak inversion}\,(q_s \ll 1): \qquad g_{ms} \approx \frac{q_s}{1+\lambda_c/2}, \tag{4.18a}$$

$$\text{strong inversion}\,(\lambda_c q_s \gg 1): \qquad g_{ms} \approx \frac{1}{\lambda_c}. \tag{4.18b}$$

where the weak inversion asymptote of g_{ms} is equal to that of i_{dsat} in Eq. (4.9a), leading to $g_{ms}/i_{dsat} = 1$ in weak inversion.

The transconductance efficiency is one of the most important FoMs for low-power analog and RF IC design. It is a direct measure of how much transconductance is produced for a given drain current. The normalized transconductance efficiency is defined as the actual transconductance G_m or the normalized source transconductance g_{ms} with respect to the corresponding maximum reached in weak inversion, i.e., $I_D/(nU_T)$ or i_{dsat}, respectively.

Before deriving the normalized transconductance efficiency, the source transconductance g_{ms} is first expressed as a function of i_{dsat} by introducing Eq. (4.13) into Eq. (4.17):

$$g_{ms} = \frac{\sqrt{4i_{dsat} + (1+\lambda_c i_{dsat})^2} - 1}{2 + \lambda_c(1+\lambda_c i_{dsat})}. \tag{4.19}$$

Hence, the normalized transconductance efficiency can be expressed as a function of the normalized drain current [113, 203]:

$$\frac{g_{\mathrm{ms}}}{i_{\mathrm{dsat}}} = \frac{G_{\mathrm{m}} n U_{\mathrm{T}}}{I_{\mathrm{D}}} = \frac{\sqrt{4 i_{\mathrm{dsat}} + (1+\lambda_{\mathrm{c}} i_{\mathrm{dsat}})^2} - 1}{\left[2+\lambda_{\mathrm{c}}(1+\lambda_{\mathrm{c}} i_{\mathrm{dsat}})\right] i_{\mathrm{dsat}}}, \tag{4.20}$$

which corresponds to the following asymptotes in weak and strong inversion:

$$\text{weak inversion}\,(i_{\mathrm{dsat}} \ll 1): \qquad \frac{g_{\mathrm{ms}}}{i_{\mathrm{dsat}}} \approx 1, \tag{4.21a}$$

$$\text{strong inversion}\,(\lambda_{\mathrm{c}} i_{\mathrm{dsat}} \gg 1): \qquad \frac{g_{\mathrm{ms}}}{i_{\mathrm{dsat}}} \approx \frac{1}{\lambda_{\mathrm{c}} i_{\mathrm{dsat}}}. \tag{4.21b}$$

Setting $\lambda_{\mathrm{c}} = 0$ in Eq. (4.19) and Eq. (4.20) yields model expressions for a long-channel device:

$$g_{\mathrm{ms}} = \frac{\sqrt{1+4 i_{\mathrm{d}}} - 1}{2}, \tag{4.22a}$$

$$\frac{g_{\mathrm{ms}}}{i_{\mathrm{d}}} = \frac{G_{\mathrm{m}} n U_{\mathrm{T}}}{I_{\mathrm{D}}} = \frac{\sqrt{1+4 i_{\mathrm{d}}} - 1}{2 i_{\mathrm{d}}}. \tag{4.22b}$$

Their asymptotoes can be obtained from Eq. (4.22) in weak and strong inversion as

$$\text{weak inversion}\,(i_{\mathrm{d}} \ll 1): \qquad g_{\mathrm{ms}} \approx i_{\mathrm{d}}, \qquad \frac{g_{\mathrm{ms}}}{i_{\mathrm{d}}} \approx 1; \tag{4.23a}$$

$$\text{strong inversion}\,(i_{\mathrm{d}} \gg 1): \qquad g_{\mathrm{ms}} \approx \sqrt{i_{\mathrm{d}}}, \qquad \frac{g_{\mathrm{ms}}}{i_{\mathrm{d}}} \approx \frac{1}{\sqrt{i_{\mathrm{d}}}}. \tag{4.23b}$$

The weak and strong inversion asymptotes in Eq. (4.21) and Eq. (4.23) are important from the perspectives of both circuit design and parameter extraction. The normalized transconductance efficiency of long- and short-channel MOSFETs is plotted in Fig. 4.1 with the corresponding asymptotoes. In weak inversion, the normalized transconductance efficiency remains invariant. However, in strong inversion, it takes on a $1/(\lambda_{\mathrm{c}} i_{\mathrm{dsat}})$ dependence for a velocity saturated device, which is different from the $1/\sqrt{i_{\mathrm{d}}}$ dependence for a long-channel device.

As also illustrated in Fig. 4.1, two strong inversion asymptotes intersect at $i_{\mathrm{dsat}} = 1/\lambda_{\mathrm{c}}^2$ which marks the onset of VS. This corresponds to the critical inversion coefficient parameter IC_{crit} of the empirical inversion coefficient model proposed by Binkley [112]:

$$IC_{\mathrm{Binkley}} = IC\left(1 + \frac{IC}{4 IC_{\mathrm{crit}}}\right). \tag{4.24}$$

However, two additional intersection points might be of higher interest for semiconductor device modeling. Two asymptotes in Eq. (4.21) intersect at a point where the normalized drain current is equal to $1/\lambda_{\mathrm{c}}$ ($IC = I_{\mathrm{D}}/I_{\mathrm{spec}} = 1/\lambda_{\mathrm{c}}$), while two asymptotes in Eq. (4.23) intersect at a point where the normalized drain current is equal to 1 ($IC = I_{\mathrm{D}}/I_{\mathrm{spec}} = 1$). These two intersection points provide an efficient approach of extracting the specific current I_{spec} and

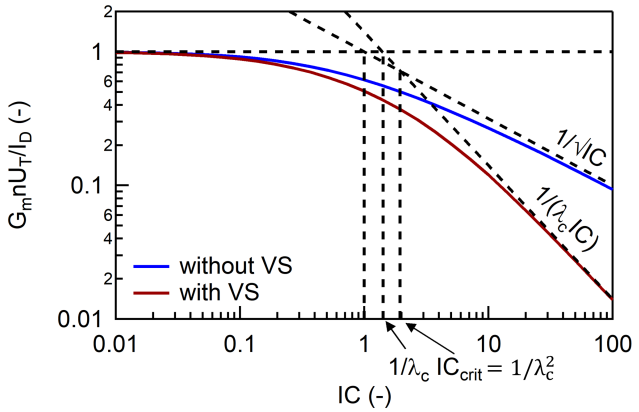


Figure 4.1 – Description of the asymptotoes of the normalized transconductance efficiency $G_m nU_T/I_D$ with respect to the inversion coefficient IC.

the VS parameter λ_c from the normalized transconductance efficiency ($g_{ms}/i_d = G_m nU_T/I_D$).

4.1.2 Parameter extraction

The experimental characterization has shown that TID influences the radiation response of 28-nm bulk MOSFETs by causing a drain leakage current increase, a slope factor degradation, a threshold voltage shift, a low-field channel mobility reduction, an effective channel width reduction, and a radiation-enhanced DIBL effect. The effective channel width reduction and the radiation-enhanced DIBL effect are not included in this first attempt of the modeling work are considered in detail in Chapter 5. The drain leakage current of 28-nm bulk MOSFETs is approximated as a constant current, which constitutes an additional parameter I_{Dleak} to the simplified EKV MOSFET model. These five EKV model parameters, including the drain leakage current I_{Dleak}, the slope factor n, the μ_0-included specific current per square $I_{spec_\square}$, the VS parameter λ_c, and the threshold voltage V_T, are extracted at the TID levels of interest, following the parameter extraction procedure in Fig. 4.2 [122].

The process begins with the extraction of the slope factor n and the specific current I_{spec} from measurement results of a wide/long-channel device, as described in Fig. 4.2a. After calculating the transconductance G_m, the slope factor n is extracted from the plateau of the $I_D/(G_m U_T) - I_D$ curve in weak inversion. The specific current I_{spec} is then obtained from the intersection of the strong inversion asymptote ($\propto \sqrt{I_D}$) and the slope factor horizontal line. Having I_{spec} extracted from this wide/long-channel device, the technology-dependent specific current per square $I_{spec_\square}$ can be derived through dividing I_{spec} by the aspect ratio W/L.

For a short-channel device, the slope factor n is usually affected by short-channel effects and needs to be extracted accurately. Due to a slightly different low-field channel mobility, the specific current per square $I_{spec_\square}$ extracted from a wide/long-channel device also needs adjustment. Having n and I_{spec} extracted, the normalized transconductance efficiency $G_m nU_T/I_D$

and the inversion coefficient $IC = I_D / I_{spec}$ of a short-channel device is calculated and plotted for extracting the VS parameter λ_c. As shown in Fig. 4.2b, the strong inversion asymptote of $G_m n U_T / I_D$, i.e., being proportional to $1/(\lambda_c IC)$, intersects with the weak inversion asymptote, i.e., the unity horizontal line, at $IC = 1/\lambda_c$, from which the VS parameter λ_c is extracted.

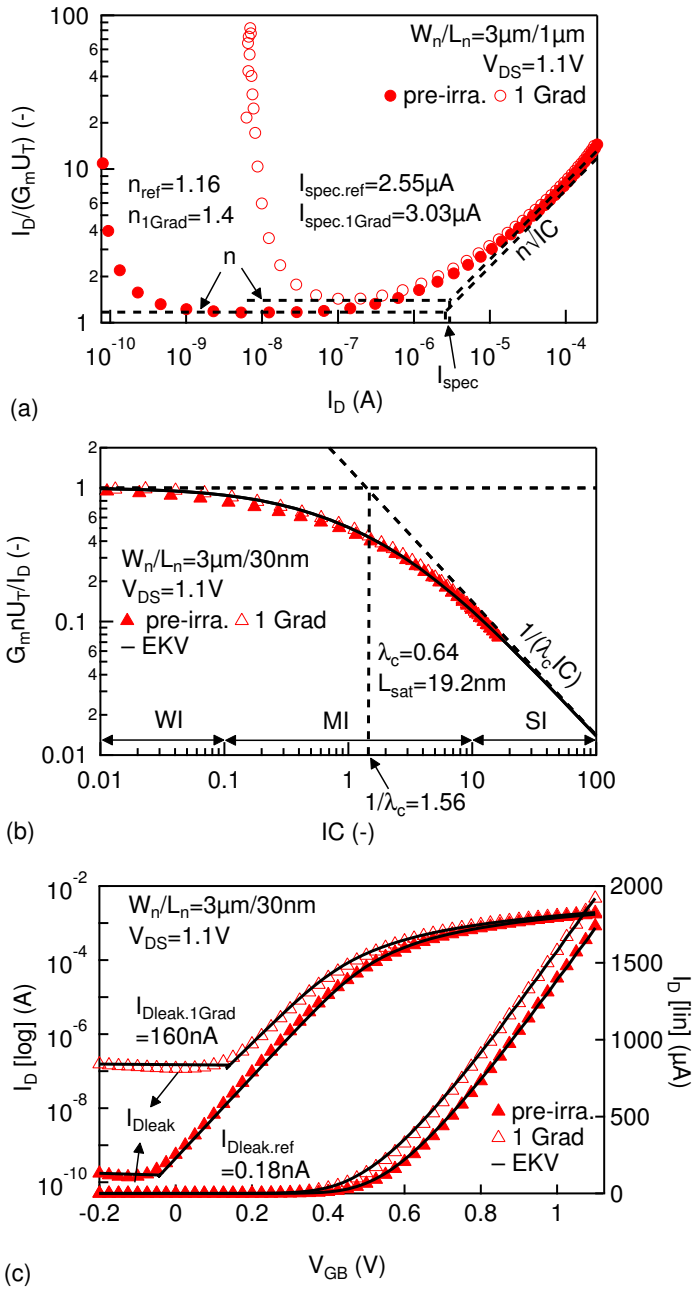


Figure 4.2 – Extraction of EKV model parameters: (a) the slope factor n and the specific current I_{spec}; (b) the velocity saturation parameter λ_c; (c) the threshold voltage V_T and the drain leakage current I_{Dleak}. (After Zhang, et al. [122].)

Having now extracted n, I_{spec}, and λ_c, the threshold voltage V_T is extracted by fitting the EKV MOSFET model with measured data, as depicted in Fig. 4.2c. To help understand the V_T extraction, Eq. (4.14) is rewritten as a function of the drain current with model parameters:

$$\frac{V_{GB}-V_T-nV_{SB}}{nU_T}=\sqrt{4\frac{I_D}{I_{spec}}+\left(1+\lambda_c\frac{I_D}{I_{spec}}\right)^2}+\ln\left[\sqrt{4\frac{I_D}{I_{spec}}+\left(1+\lambda_c\frac{I_D}{I_{spec}}\right)^2}-1\right]-(1+\ln 2). \tag{4.25}$$

The last parameter is the drain leakage current I_{Dleak}, which can be easily extracted from the plateau of the $I_D - V_{GB}$ curve at the switched-off state, as indicated in Fig. 4.2c.

With accurately extracted parameters, it is expected that all EKV model equations can be properly normalized. The normalization should allow the simplified EKV MOSFET model to be independent of technology, temperature, geometry, and TID, while leaving five model parameters (n, I_{spec}, λ_c, V_T, and I_{Dleak}) to carry the stripped-off dependencies.

4.1.3 TID effects on large-signal characteristics

TID effects on transfer characteristics

Fig. 4.3 compares the simplified EKV MOSFET model to the measured transfer characteristics of four corner *n*- and *p*MOSFETs before irradiation and after an ultrahigh TID. The simplified EKV MOSFET model matches pre-irradiation measurements very well in all regions of device operation, demonstrating its capability of fully capturing this 28-nm bulk CMOS technology with only five model parameters. The excellent agreement extends to all levels of TID up to 1 Grad, as presented by the results corresponding to the highest TID level in Fig. 4.3. This confirms the promising use of this simplified EKV MOSFET model in radiation-tolerant circuit design with nanoscale CMOS processes.

TID effects on EKV model parameters

The comparison of measurements before irradiation and at an ultrahigh TID in Fig. 4.3 indicates the significant drain leakage current increase of *n*MOSFETs and the substantial drive current loss of *p*MOSFETs, as well as the threshold voltage shift and the slope factor increase [122]. Extracted EKV model parameters are summarized in Fig. 4.4 as a function of TID. Unlike in Chapter 3 with results of *n*- and *p*MOSFETs plotted separately, the corresponding values of EKV model parameters are now plotted in the same figures with the same scales, making the comparison between *n*- and *p*MOSFETs straightforward and efficient. Besides, TID is shown in linear scale, making data points at ultrahigh TID levels more visible. The VS parameter λ_c remains almost constant with respect to TID, which is not shown here.

Fig. 4.4a presents the significant drain leakage current increase of *n*MOSFETs and the slight drain leakage current increase of *p*MOSFETs. The smallest *n*MOSFET has the highest drain

leakage current increase by four orders of magnitude. The drain leakage current of *n*MOSFETs increases fast at TID levels below 200 Mrad as a result of the activation of parasitic channels along STI sidewalls and tends to saturate at ultrahigh TID levels due to the almost complete filling of oxide traps or the compensation of interface-trapped charges [19, 59, 77].

Fig. 4.4b shows the threshold voltage shift in absolute values with respect to TID. Due to the superposed effect of oxide- and interface-trapped charges, *p*MOSFETs undergo a higher

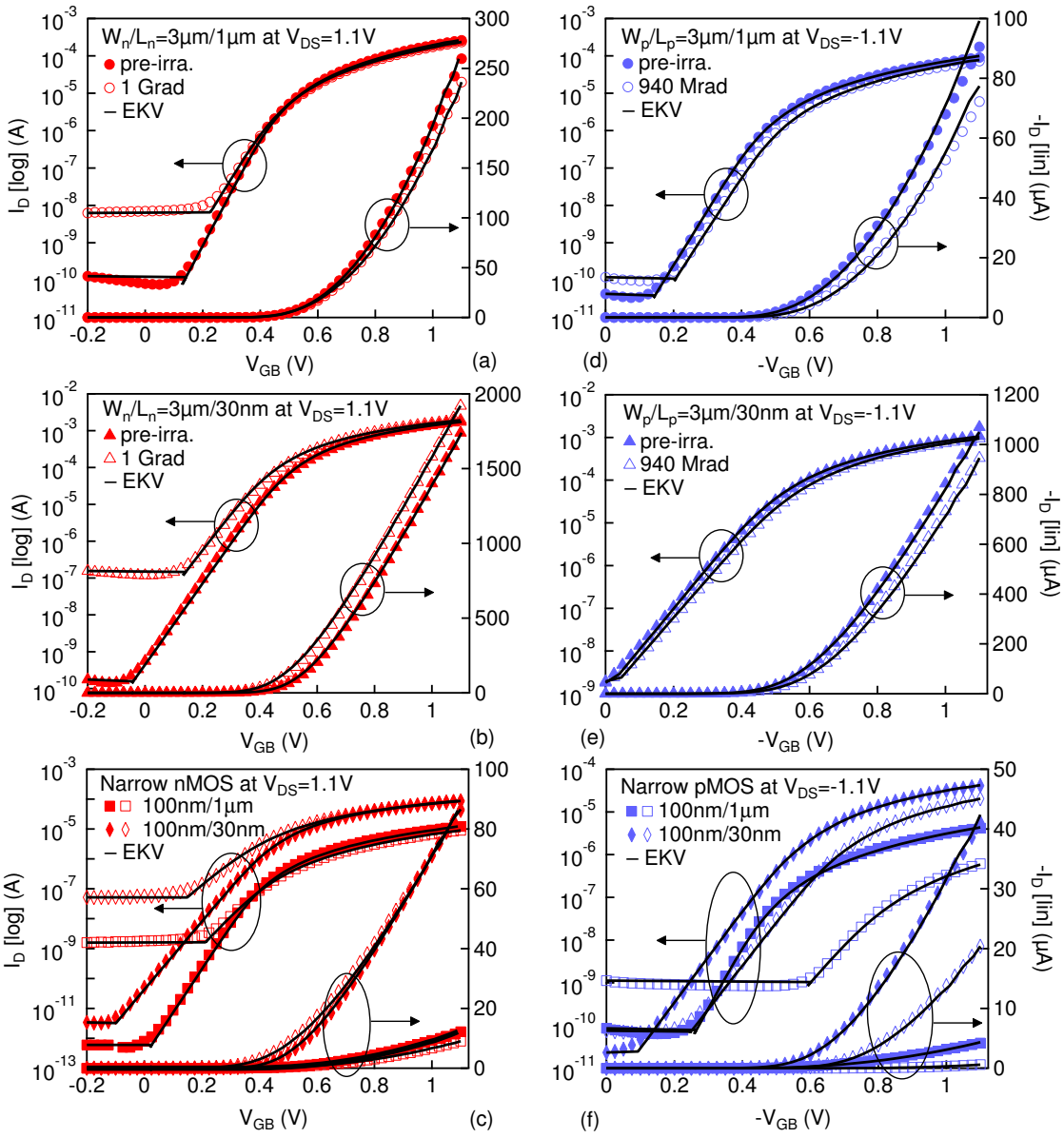


Figure 4.3 – The simplified EKV MOSFET model versus the measured $|I_D| - |V_{GB}|$ curves of four corner (a-c) *n*- and (d-f) *p*MOSFETs with respect to pre-irradiation (solid markers) and an ultrahigh TID (open markers). (After Zhang, et al. [122].)

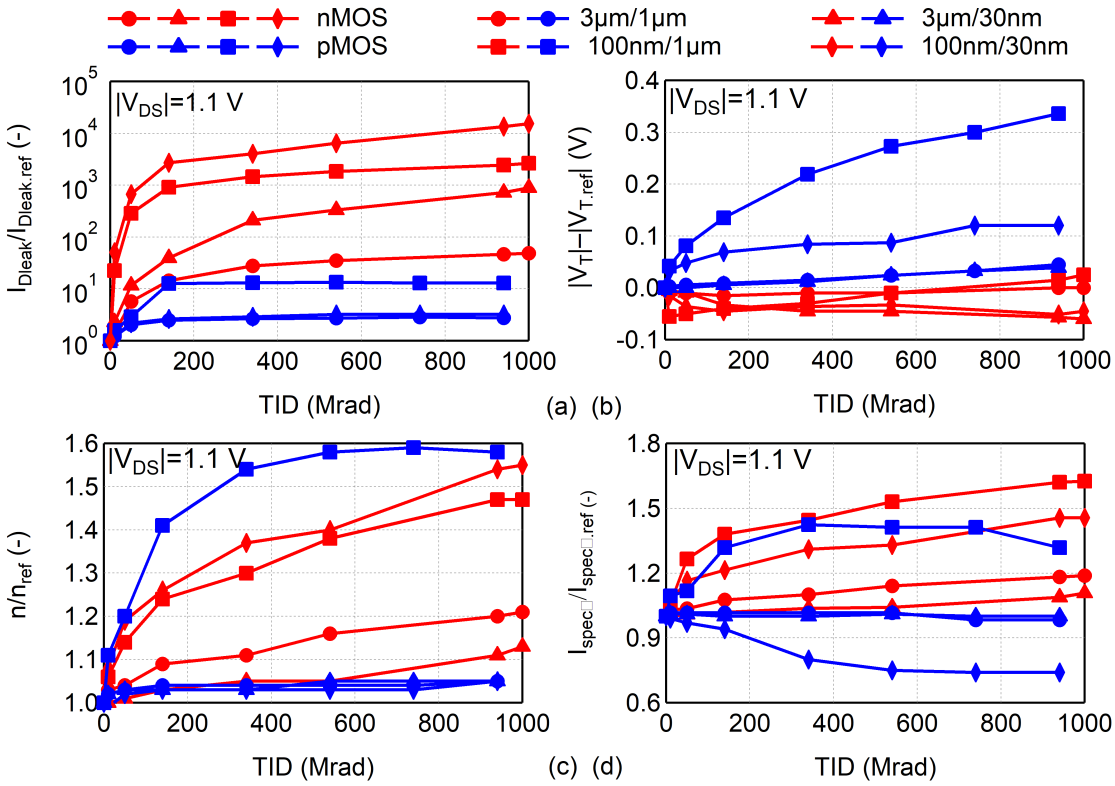


Figure 4.4 – TID effects on (a) the drain leakage current I_{Dleak}, (b) the threshold voltage V_{T}, (c) the slope factor n, and (d) the specific current per square $I_{\mathrm{spec}\square}$ of four corner 28-nm bulk n- and pMOSFETs. (After Zhang, et al. [122].)

threshold voltage shift than nMOSFETs. The superposed effect of oxide- and interface-trapped charges in pMOSFETs also induces severe RINCE, making the narrow/long-channel pMOSFET suffer a dramatic threshold voltage shift (-350 mV). In contrast, due to the compensated effect of oxide- and interface-trapped charges, nMOSFETs present a moderate threshold voltage shift and narrow-channel nMOSFETs go through a V_{T} rebound.

As observed from Fig. 4.4c, pMOSFETs, except the narrow/long-channel one, have a negligible slope factor increase, while the slope factor of nMOSFETs, especially two narrow-channel ones, is generally sensitive to TID. The smaller slope factor change of pMOSFETs is probably due to the negative gate bias during irradiation, which is unfavorable for proton transport to the semiconductor/oxide interface. For narrow-channel MOSFETs, the slope factor increase mainly results from STI-related interface-charge trapping. Note that the drain leakage current increase of narrow-channel MOSFETs compromises the accuracy of the slope factor extraction, which may overestimate the contribution of STI-related interface-trapped charges. The influence of the drain leakage current on the slope factor extraction is therefore carefully considered in Chapter 5.

Fig. 4.4d plots the specific current per square of n- and pMOSFETs. For most MOSFETs,

this parameter follows the increasing trend of the slope factor. However, this parameter of *p*MOSFETs starts to decrease at certain TID levels, indicating the low-field channel mobility degradation and/or the effective channel width reduction.

As observed from the measured transfer characteristics and the extracted EKV model parameters, the simplified EKV MOSFET model and measurement results demonstrate a high TID tolerance for 28-nm bulk MOSFETs, except for some narrow-channel MOSFETs. Designers should therefore take special care when using narrow-channel MOSFETs for their radiation-tolerant circuit design.

4.1.4 TID effects on small-signal characteristics

TID effects on intrinsic gain

The correct operation of many analog circuits relies on a sufficient intrinsic gain of MOSFETs. Therefore, it is crucial to investigate the effects of TID on this FoM. Fig. 4.5 reports (a) the transconductance G_m, (c) the output conductance G_{ds}, and (d) the intrinsic gain $A_v = G_m/G_{ds}$ at the same operating point ($|V_{DS}| = 1.1\,V$ and $|V_{GB}| = 0.7\,V$) of four corner *n*- and *p*MOSFETs

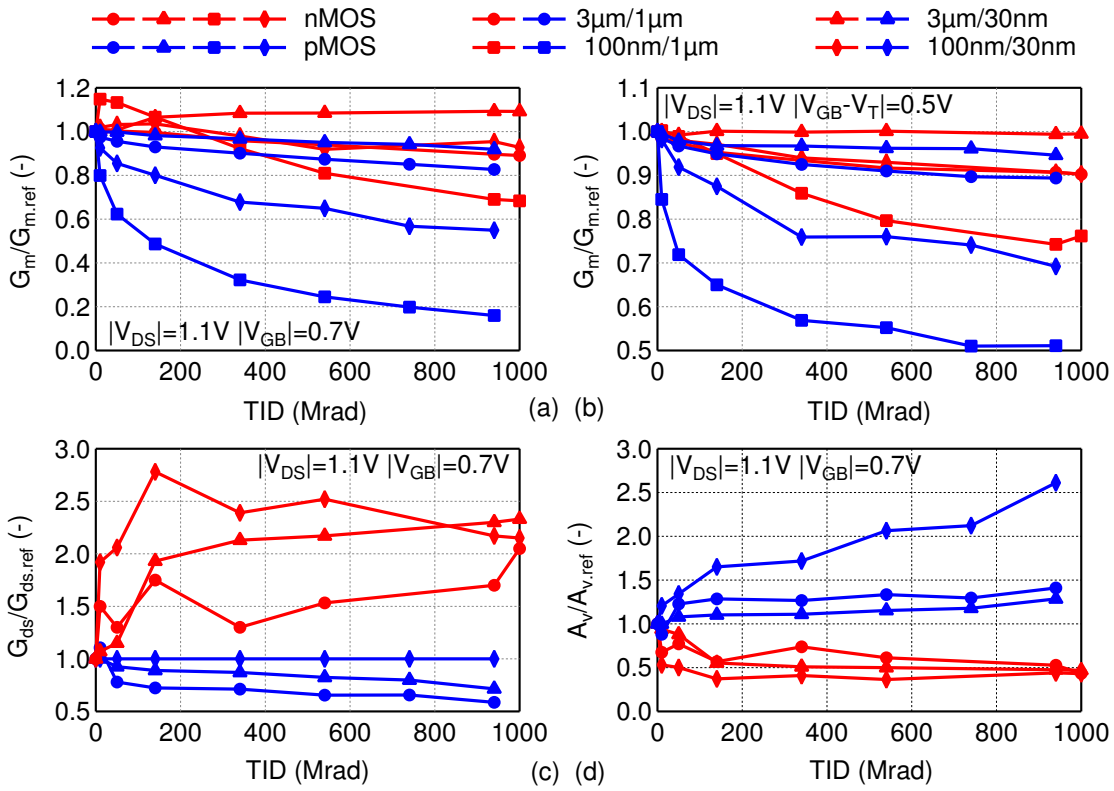


Figure 4.5 – TID effects on (a, b) the transconductance G_m, (c) the output conductance G_{ds}, and (d) the intrinsic gain A_v of four corner *n*- and *p*MOSFETs. (After Zhang, et al. [122].)

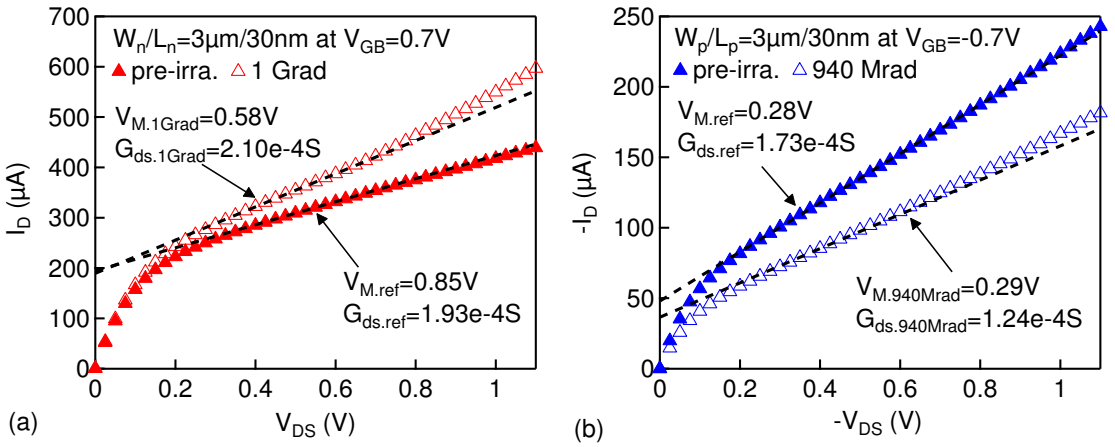


Figure 4.6 – Output characteristics of the wide/short-channel MOSFET of both types with respect to pre-irradiation (solid markers) and an ultrahigh TID (open markers). (After Zhang, et al. [122].)

as a function of TID [122]. The transconductance in Fig. 4.5a basically follows the TID-induced evolution of the threshold voltage shift. It continuously increases for the wide/short-channel *n*MOSFET, whereas it first increases then decreases for other *n*MOSFETs. Due to the significant threshold voltage shift, *p*MOSFETs present a substantial transconductance loss. To eliminate the influence of the threshold voltage shift, the transconductance is also extracted at a constant overdrive voltage ($|V_{GB} - V_T| = 0.5\,V$). As shown in Fig. 4.5b, these MOSFETs are still having a transconductance loss. The remaining transconductance loss can be attributed to a radiation-induced mobility reduction and/or an effective channel width reduction.

As shown in Fig. 4.5c, the output conductance increases for *n*MOSFETs and decreases for *p*MOSFETs with respect to TID. This behavior can be seen from Fig. 4.6, which plots the output characteristics of a wide/short-channel MOSFET of both types [122]. After an ultrahigh TID, the wide/short-channel *n*MOSFET shows a lower Early voltage and hence a higher output conductance, whereas the wide/short-channel *p*MOSFET presents a higher Early voltage and a lower output conductance. This observation of the output conductance is consistent with the radiation-enhanced DIBL effect for *n*MOSFETs and the radiation-suppressed DIBL effect for *p*MOSFETs, as discussed in Section 3.2.2. The transconductance loss and the output conductance increase eventually result in a degraded intrinsic gain for *n*MOSFETs, while *p*MOSFETs obtain a slightly improved intrinsic gain due to the reduced output conductance, as shown in Fig. 4.5d.

TID effects on transconductance efficiency

The normalized form of the transconductance efficiency G_m/I_D is expressed as a function of the normalized drain current in Eq. (4.20) and is rewritten as a function of the inversion

coefficient IC:

$$\frac{g_{ms}}{i_d} = \frac{G_m n U_T}{I_D} = \frac{\sqrt{4IC + (1+\lambda_c IC)^2} - 1}{[2 + \lambda_c(1+\lambda_c IC)]\, IC}. \tag{4.26}$$

Fig. 4.7 presents the normalized transconductance efficiency of wide/long- and wide/short-channel MOSFETs, highlighting the VS-induced degradation in strong inversion. The $G_m n U_T / I_D$ versus IC characteristics of short-channel MOSFETs degrade faster as $1/(\lambda_c IC)$ than that of long-channel MOSFETs with a $1/\sqrt{IC}$ dependence. This behavior is well modeled by the VS parameter λ_c over a large range of operating points in strong inversion.

Moreover, after a proper normalization with extracted parameters, all the measured points before irradiation and after a high TID level nicely fall on the curves of the simplified EKV MOSFET model. This demonstrates the negligible effects of TID on the normalized transcon-

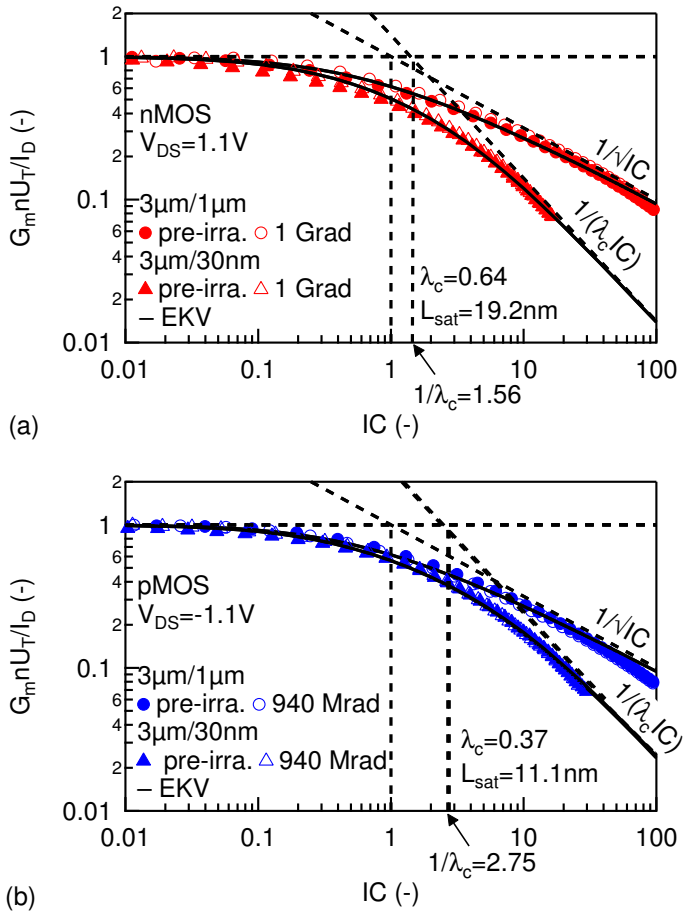


Figure 4.7 – Normalized transconductance efficiency $G_m n U_T / I_D$ of wide/long- and wide/short-channel (a) n- and (b) pMOSFETs with respect to pre-irradiation and an ultrahigh TID. (After Zhang, et al. [122].)

ductance efficiency while confirming the efficiency of five EKV model parameters in capturing the effects of TID on this 28-nm bulk CMOS technology. Although total ionizing radiation affects analog parameters of 28-nm bulk MOSFETs, the normalization strips off the effects of TID from the normalized transconductance efficiency. This *IC*-based simplified EKV MOSFET model can therefore be promising for radiation-tolerant circuit design.

4.2 Investigation of TID-induced mobility degradation

The effective channel mobility is among the most important parameters for characterizing device behaviors and evaluating circuit performance. Under harsh radiation environments, oxide- and interface-charge trapping may strongly affect the carrier transport in the inversion layer, compromising the drive capability and the switching speed of MOSFETs. Previous results

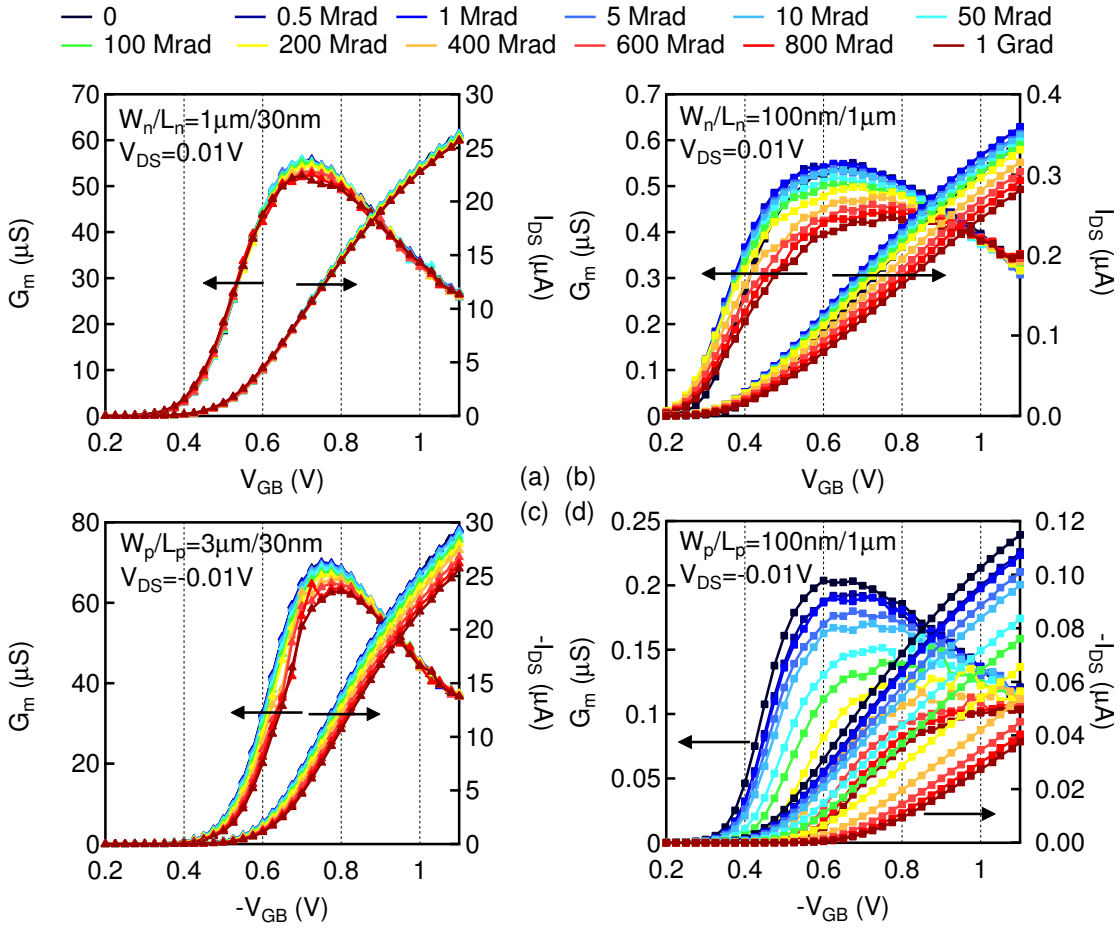


Figure 4.8 – Measured $|I_{DS}|$ and calculated G_m versus $|V_{GB}|$ curves in linear operation ($|V_{DS}|$ = 0.01 V) of (a, c) wide/short- and (b, d) narrow/long-channel (a, b) *n*- and (c, d) *p*MOSFETs irradiated under the diode condition ($|V_{GB}| = |V_{DS}|$ = 1.1 V) at room temperature (25 °C). (After Zhang, et al. [123].)

have shown a drive current variation in saturation operation of 28-nm bulk MOSFETs, which is believed to be a result of a threshold voltage shift, a low-field channel mobility reduction, and in some cases an effective channel width reduction [122].

Fig. 4.8 presents the measured $|I_{DS}|$ and the calculated G_m versus $|V_{GB}|$ curves in linear operation of wide/short- and narrow/long-channel MOSFETs up to 1 Grad of TID [123]. These irradiated MOSFETs, including the wide/short-channel *n*MOSFET that has a drive current improvement in saturation, demonstrate an on-current loss in linear. The on-current loss is partly attributed to the threshold voltage shift, as observed from the shifted $|I_{DS}|$ and G_m versus $|V_{GB}|$ curves. It is also correlated with the radiation-induced mobility degradation, as inferred from the degraded peak transconductance. To investigate the TID-induced mobility degradation of 28-nm bulk MOSFETs, this section uses a very simple model, i.e., the Ghibaudo's Y-function, to extract the effective channel mobility and related device parameters from the linear transfer characteristics [204].

4.2.1 Y-function-based mobility extraction

The Y-function-based mobility extraction method requires measurement results in strong inversion region of linear operation of a MOSFET at a very small drain voltage [204]. Relying on the drift-diffusion transport model $I_{DS} = \mu_{eff} C_{ox} W (V_{GB} - V_T) V_{DS} / L$ and considering the first-order mobility degradation model $\mu_{eff} = \mu_0 / [1 + \theta (V_{GB} - V_T)]$, the drain-to-source current in linear is expressed as

$$I_{DS} = \frac{W}{L} \frac{\mu_0}{1 + \theta (V_{GB} - V_T)} C_{ox} (V_{GB} - V_T) V_{DS}, \tag{4.27}$$

where μ_{eff} is the effective channel mobility with the mobility reduction due to the vertical electric field, θ is the effective mobility degradation coefficient, and V_T is the charge threshold voltage that is generally larger than the extrapolated threshold voltage.

Once G_m is derived from Eq. (4.27), the well-known Y-function $I_{DS}/\sqrt{G_m}$ can be obtained as [204]

$$\frac{I_{DS}}{\sqrt{G_m}} = \sqrt{\mu_0 C_{ox} \frac{W}{L} V_{DS}} (V_{GB} - V_T), \tag{4.28}$$

which is independent of θ and linearly dependent on V_{GB} in strong inversion. This is evidenced by the $|I_{DS}|/\sqrt{G_m}$ versus $|V_{GB}|$ curves of wide-channel *n*MOSFETs in Fig. 4.9a and narrow-channel *p*MOSFETs in Fig. 4.9c [123]. The linear extrapolation of $I_{DS}/\sqrt{G_m}$ in strong inversion intercepts the V_{GB} axis at the charge threshold voltage V_T and its slope $\sqrt{\mu_0 C_{ox} W V_{DS} / L}$ provides information about the low-field channel mobility μ_0. This Y-function-based mobility extraction allows us to decouple the effects of TID on the threshold voltage and the low-field channel mobility.

For a correct extraction of V_T and μ_0, this linear extrapolation has to be applied at high gate

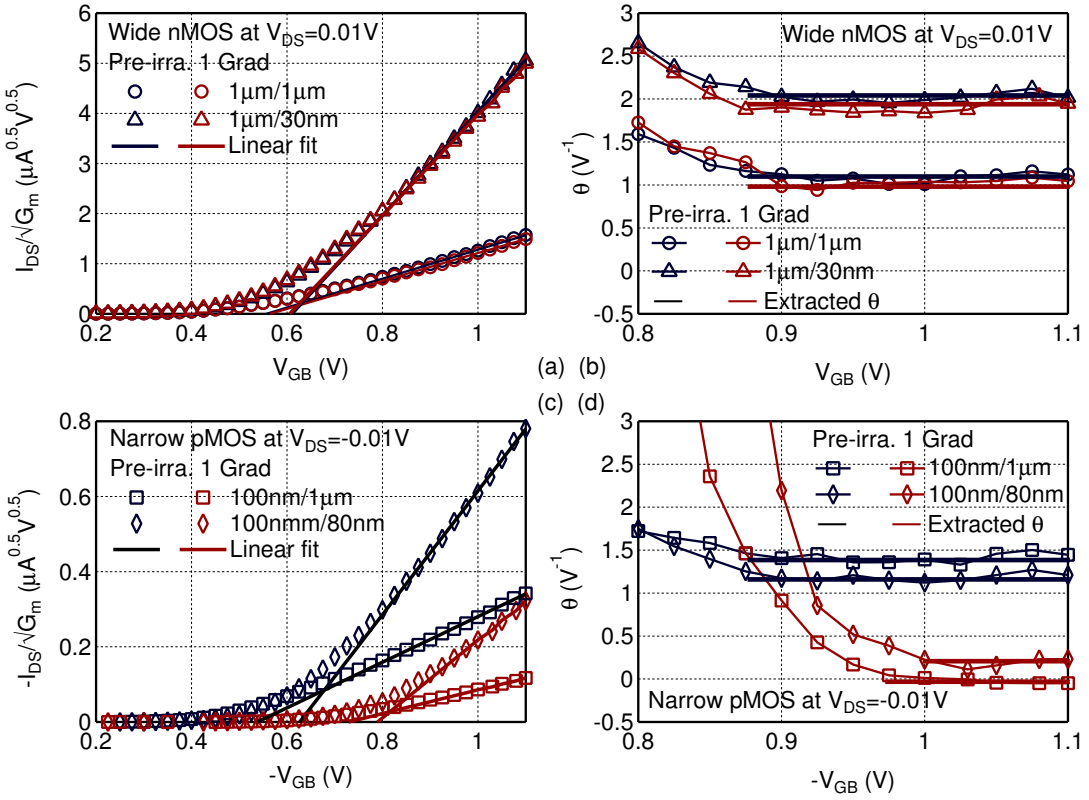


Figure 4.9 – (a, c) Y-function $|I_{DS}|/\sqrt{G_m}$ and (b, d) mobility degradation coefficient θ of (a, b) wide-channel *n*MOSFETs and (c, d) narrow-channel *p*MOSFETs as a function of $|V_{GB}|$ with respect to pre-irradiation and 1 Grad of TID. The thick horizontal lines in (b) and (d) correspond to the values of θ in the region of $|V_{GB}|$ where it can be approximated as a constant. (After Zhang, et al. [123].)

voltages in sufficiently strong inversion to avoid the proximity effect of the moderate inversion region [204]. This can be checked by the occurrence of a plateau in the $\theta(V_{GB})$ characteristics. Combining the derived G_m with Eq. (4.27) yields the $\theta(V_{GB})$ expression:

$$\theta = \left[\frac{I_{DS}}{G_m(V_{GB}-V_T)} - 1\right]\frac{1}{V_{GB}-V_T}. \tag{4.29}$$

Fig. 4.9b and Fig. 4.9d [123] present that before radiation, θ is indeed independent of V_{GB} between 0.9 V and 1.1 V. However, after irradiation, narrow/long-channel *p*MOSFETs have a significant threshold voltage shift and a smaller strong inversion region, reducing the valid V_{GB} range and resulting in an almost zero θ. The ultimate zero of θ of narrow-channel *p*MOSFETs also implies that the effective gate bias is not strong enough to set them in strong inversion or significantly degrade their channel mobility. Hence, the drain current I_{DS} becomes linear and the transconductance G_m tends to be constant, as indicated by $I_{DS} = \mu_0 C_{ox} W(V_{GB}-V_T)V_{DS}/L$ and evidenced by the red curves in Fig. 4.8d.

4.2.2 TID effects on effective channel mobility

The effective channel mobility μ_{eff} can be now calculated with the first-order mobility degradation model using V_T, μ_0, and θ extracted in strong inversion region of linear operation. Fig. 4.10 reports the effective channel mobility μ_{eff} of four corner n- and pMOSFETs versus the overdrive voltage $|V_{GB} - V_T|$ [123]. Except for narrow-channel pMOSFETs, all other MOSFETs present the V_{GB}-induced mobility degradation. Besides, the effective channel mobility of narrow-channel MOSFETs degrades more than their long-channel counterparts. It is worth noting that the low-field channel mobility μ_0 corresponds to the effective channel mobility μ_{eff} at a zero $V_{GB} - V_T$. As expected, the low-field electron mobility is around three times the low-field hole mobility.

The variation of the low-field channel mobility μ_0 and the effective mobility degradation coefficient θ is plotted as a function of TID in Fig. 4.11 [123]. The effective mobility degradation coefficient is actually related to the low-field channel mobility by a linear relationship $\theta = \theta_0 + C_{ox} R_{SD} \mu_0 W/L$ [205], where θ_0 is the intrinsic mobility degradation coefficient and R_{SD} is the source/drain series resistance. Assuming that R_{SD} is constant throughout all TID

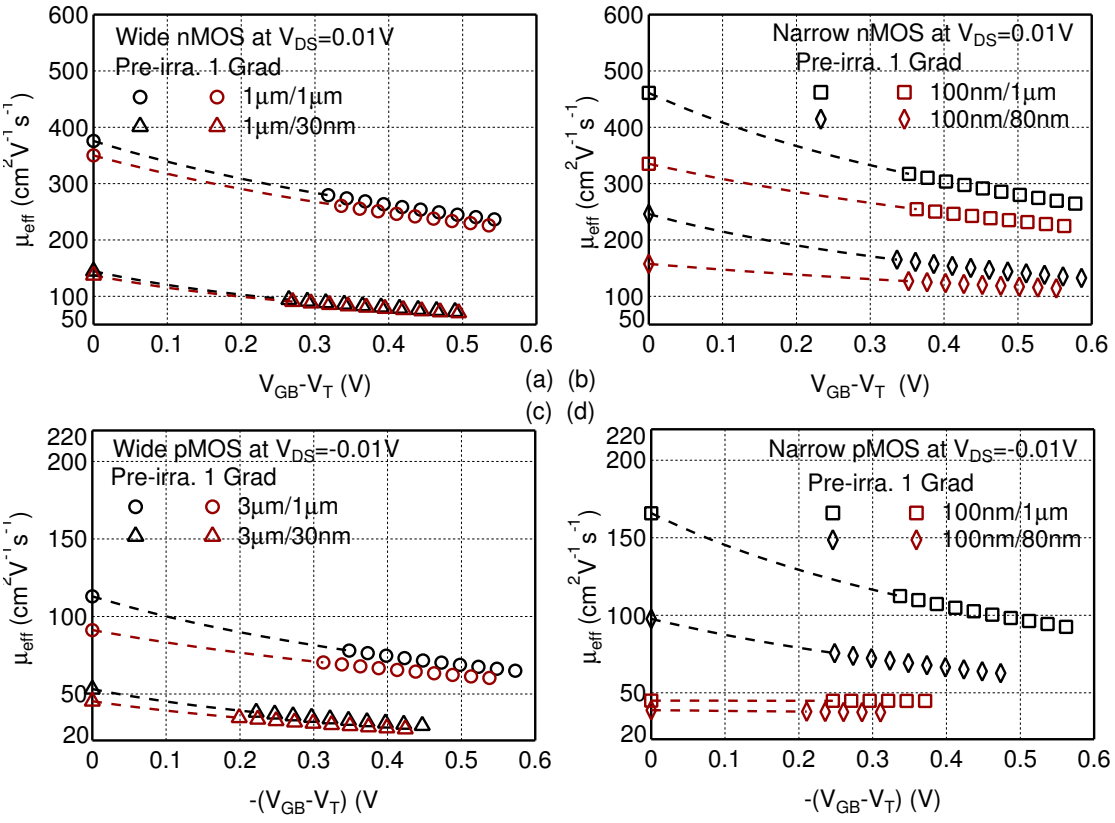


Figure 4.10 – Effective channel mobility μ_{eff} of four corner (a, b) n- and (c, d) pMOSFETs versus the overdrive voltage $|V_{GB} - V_T|$ with respect to pre-irradiation and 1 Grad of TID. (After Zhang, et al. [123].)

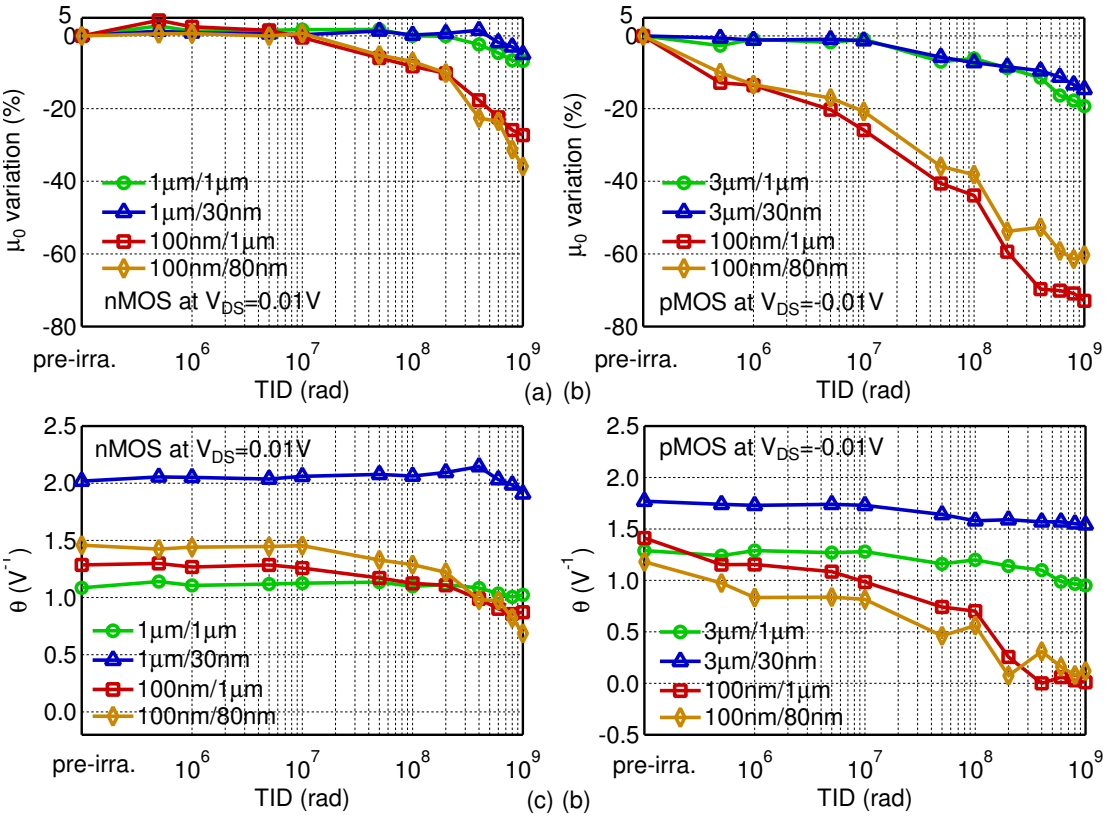


Figure 4.11 – TID-induced evolution of (a, b) the low-field channel mobility μ_0 and (c, d) the effective mobility degradation coefficient θ of four corner (a, c) *n*- and (b, d) *p*MOSFETs. (After Zhang, et al. [123].)

levels, θ becomes linear with respect to μ_0, as evidenced from their concomitant evolution in Fig. 4.11 [123].

The low-field channel mobility reduction demonstrates a channel width dependence. It is believed that interfacial charges, including charges trapped in oxide traps close to the surface channel and at the semiconductor/oxide interface, act as Coulomb scattering centers and degrade the low-field channel mobility [153, 206]. The low-field channel mobility of wide-channel MOSFETs degrades slightly with respect to TID, indicating the improved radiation tolerance of advanced gate stacks. However, narrow-channel MOSFETs undergo a significant low-field channel mobility reduction up to 36% for *n*MOSFETs (Fig. 4.11a) and 73% for *p*MOSFETs (Fig. 4.11c). This channel width dependence indicates the dominant influence of STI-related charge trapping near the surface channel.

In addition, the low-field channel mobility of *p*MOSFETs degrades more than that of *n*MOSFETs. This may lead to the conclusion that TID generates more interfacial charges in *p*MOSFETs. However, a higher density of interfacial charges generally refers to a more serious subthreshold swing degradation, which is inconsistent with the slightly influenced subthreshold swing of

*p*MOSFETs, as shown in Fig. 3.15. The observed low-field channel mobility reduction probably reflects the effective channel width reduction, as further discussed in Section 5.1.5.

4.3 Investigation of TID effects on drain leakage current

28-nm bulk MOSFETs are radiation tolerant at the switched-on region with slight parametric shifts. However, TID induces a drain leakage current increase in both *n*- and *p*MOSFETs. The drain leakage current of *p*MOSFETs increases slightly, by a maximum of tenfold. However, that of *n*MOSFETs increases significantly by a maximum of more than three orders of magnitude. Section 3.3.1 discusses briefly the drain leakage current of *n*- and *p*MOSFETs. The drain leakage current increase of *p*MOSFETs is unequal to the evolution of the source leakage current and is believed to originate from the gate or the n-well [194, 195]. The drain leakage current increase of *n*MOSFETs is generally a result of the STI-induced parasitic channels [19, 59, 77, 78]. Most of other TID effects such as the threshold voltage shift can be compensated by proper circuit biasing techniques, leaving the drain leakage current increase of *n*MOSFETs to be one of the most serious problems in terms of radiation-tolerant applications.

This section focuses on characterizing the radiation-induced drain leakage current and developing predictive models for evaluating radiation-induced static power consumption. The origins of the drain leakage current of both *n*- and *p*MOSFETs are first quantitatively identified with various sizes of MOSFETs. Based on the main experimental observations and the known dominant physical mechanisms, a semi-empirical physics-based model with only three parameters is proposed to describe the drain leakage current of *n*MOSFETs as a function of TID. The lateral parasitic transistor has been investigated in the literature using TCAD device simulations [60, 196, 197], compact models [207], or a combination of these two approaches [78, 208]. However, these models involve complex device structures and intensive analytical computations. Aiming at a simpler approach, the parasitic transistor is modeled as a gateless charge-controlled device and the parasitic drain-to-source leakage current is calculated through an adapted simplified EKV MOSFET model.

4.3.1 Experimental analysis

This part of experimental investigation exploits single-finger and multi-finger 28-nm bulk MOSFETs irradiated under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$) at room temperature (25 °C). The involved dose rates, i.e., 8.82 Mrad and 10 Mrad, are quite close and make no big difference in the radiation response of 28-nm bulk MOSFETs.

Drain leakage current of *p*MOSFETs

For a *p*MOSFET, STI-trapped positive charges tend to accumulate electrons near the surface body and prevent the formation of the conductive channel along STI sidewalls. This is opposite

to the formation of the parallel parasitic leakage paths in an *n*MOSFET. In addition, the drain leakage current of *p*MOSFETs is unequal to the source leakage current and may come from the gate or the n-well (Fig. 3.23). A comparison between different leakage components can help us trace the origin of the drain leakage current. However, shared pads between test structures in the same cluster make isolating intrinsic current components a challenge. To compare the drain leakage current with other leakage components and identify the dominant contribution, *p*MOSFETs are investigated through a customized measurement configuration.

As shown in Fig. 3.6b, when measuring p1, four terminals of those unmeasured test structures (p2-14) have been held at the same potential except those out of the range of the probe card (p15-17). This allows us to simplify the normal measurement configuration in Fig. 4.12a to Fig. 4.12b [127]. To obtain the intrinsic currents of p1, additional current components have to be deducted, such as $I_{\mathrm{DT15-17}}$ and $I_{\mathrm{DB15-17}}$ flowing through all top and bottom ESD protection diodes, respectively, $I_{\mathrm{nWG15-17}}$ representing the substrate-to-gate tunneling current, and I_{SG15} referring to the source-to-gate tunneling current. Fig. 4.12c illustrates the schematic of a customized measurement configuration with the source of each *p*MOSFET shorted to the drain [127]. It can be simplified to Fig. 4.12d, in which all SMUs are measuring the leakage components that are not fully under control [127].

Fig. 4.13 presents the TID-induced evolution of these leakage components by a series of colors and the evolution with respect to TID by the numeration of 14 MOSFETs. The current flowing through two groups of ESD protection diodes increases significantly. Without evaluating them carefully, it is impossible to get reliable information about the gate leakage current. For test

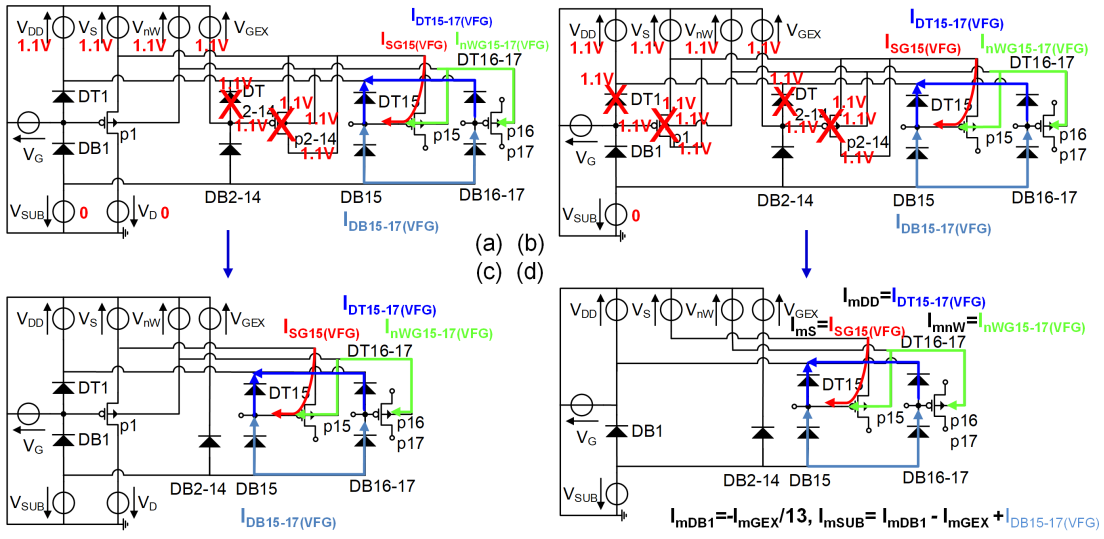


Figure 4.12 – Circuit schematics of *p*MOSFETs in the same cluster for extracting intrinsic leakage components: (a) normal measurement configuration and (c) its equivalent circuit; (b) measurement configuration with the drain of each *p*MOSFET shorted to the source and (d) its equivalent circuit. (Zhang, et al. [127].)

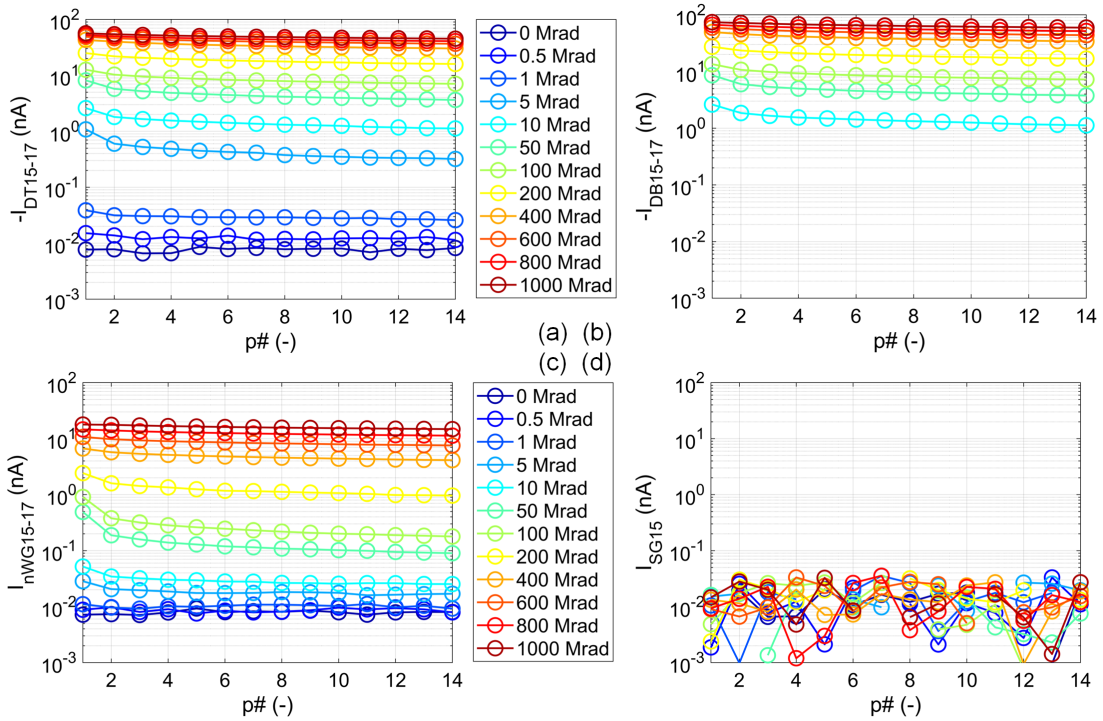


Figure 4.13 – Extracted additional leakage components versus TID for identifying the intrinsic leakage components of each *p*MOSFET.

structures out of the range of probe needles, total ionizing radiation increases their substrate-to-gate tunneling current but does not influence their source-to-gate tunneling current. For each TID step, these four components remain almost constant when the measurements go from p1 to p14, indicating no dependence on individual MOSFETs and negligible annealing effects during one hour of measurements.

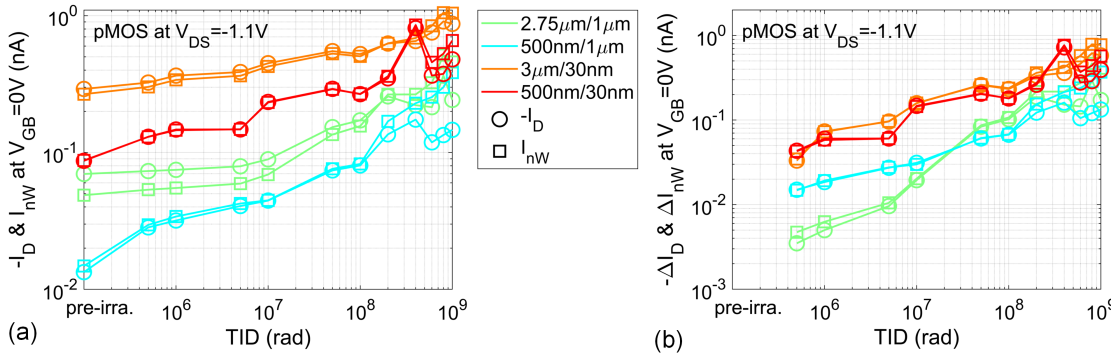


Figure 4.14 – (a) Drain current I_D and n-well current I_{nW} of *p*MOSFETs extracted at $V_{GB} = 0$ V as well as (b) their net increase as a function of TID, suggesting the dominant contribution of the n-well leakage to the off-current. (Zhang, et al. [127].)

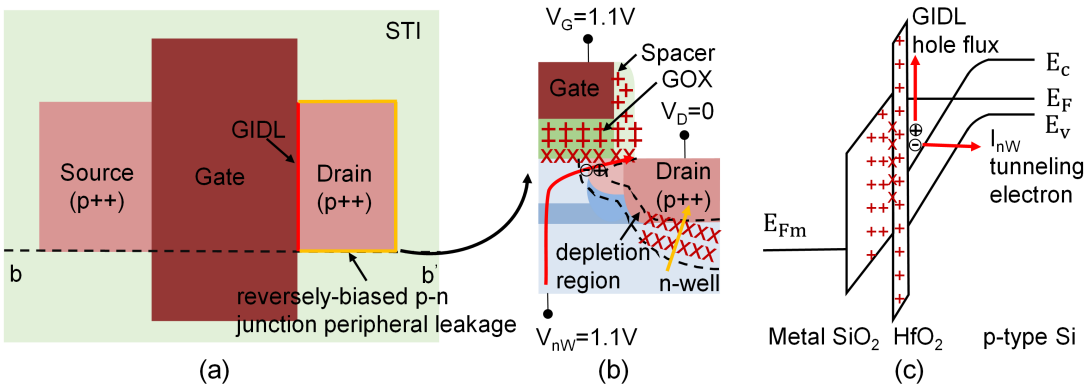


Figure 4.15 – Schematic illustration of the origin of the drain leakage current of an irradiated *p*MOSFET: (a) top view of a *p*MOSFET; (b) charge trapping that enhances the gate-induced drain leakage (GIDL) and the peripheral substrate-drain junction leakage; (c) energy band diagram that explains the radiation-enhanced GIDL. (Zhang, et al. [127].)

Deducting these additional leakage components from the normal measurement results provides information about the intrinsic leakages flowing through the gate and the n-well of each MOSFET. As displayed in Fig. 4.14, the drain leakage current increases with the n-well leakage up to 1 nA in (a) and their relative increase in (b) is almost equal for all TID levels [127]. This confirms the dominant contribution of the n-well leakage to the total drain leakage current.

As illustrated in Fig. 4.15a and Fig. 4.15b, both the gate-induced drain leakage (GIDL) and the peripheral substrate-drain junction leakage flow from the n-well to the drain and can be influenced by radiation-induced charge trapping. As shown in Fig. 4.15c, charge trapping related to the gate oxide increases the electric field above the LDD region and makes the corresponding energy bands bend more. This facilitates the band-to-band tunneling at the LDD region and increases the GIDL current. The peripheral substrate-drain junction leakage surrounds the drain active region, as presented in Fig. 4.15a, and is related to interface-trapped charges at the intersection of the substrate-drain depletion region and STI sidewalls [194, 195]. Since STI-related charge trapping dominates the effects of TID on 28-nm bulk MOSFETs, the peripheral substrate-drain junction leakage current is probably the main contributor to the drain leakage current increase of *p*MOSFETs.

Drain leakage current of *n*MOSFETs

For an *n*MOSFET, STI-trapped positive charges invert the p-type substrate along STI sidewalls and open two parallel parasitic leakage paths [19, 59, 77, 78]. As shown in Fig. 4.16a and Fig. 4.16c [124], this contributes two parallel leakage components to the total drain leakage current even when the main *n*MOSFET is switched off [19,59,77,78]. The situation worsens for a multi-finger *n*MOSFET, since the number of parasitic channels scales with the number of fingers [156], as illustrated in Fig. 4.16b and Fig. 4.16d [124].

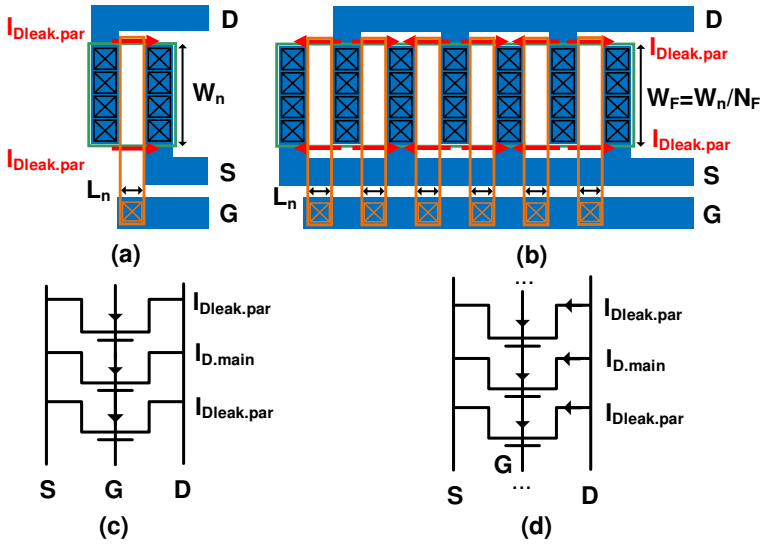


Figure 4.16 – (a, b) Layouts and (c, d) schematics of irradiated single-finger (a, c) and multi-finger (b, d) *n*MOSFETs, illustrating the scaling property of the parasitic drain-to-source leakage current with the number of fingers. The total width of a multi-finger *n*MOSFET W_n is the width per finger W_F times the number of fingers N_F. (After Zhang, et al. [124].)

Fig. 4.17 plots the measured $I_D - (V_{GB} - V_T)$ curves in saturation operation ($V_{DS} = 1.1$ V) of single-finger and multi-finger *n*MOSFETs with respect to TID up to 1 Grad [124]. Both single-

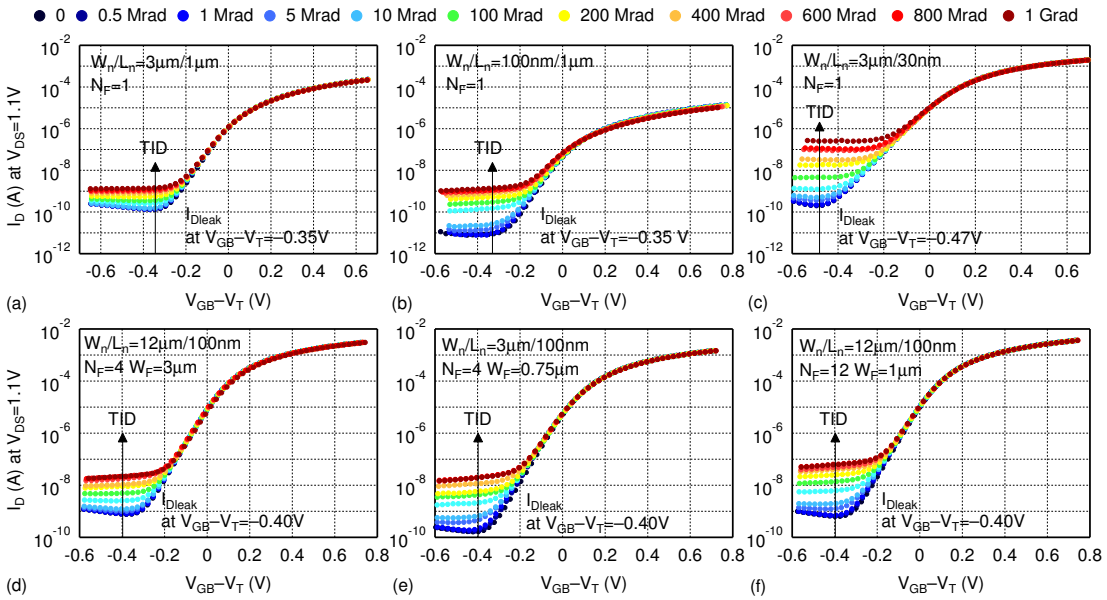


Figure 4.17 – Measured $I_D - (V_{GB} - V_T)$ curves in saturation operation ($V_{DS} = 1.1$ V) of (a-c) single-finger and (d-f) multi-finger *n*MOSFETs. The threshold voltage V_T is extracted from the linear extrapolation of $\sqrt{I_D}$ at the steepest point. The vertical arrow lines indicate the location where the drain leakage current I_{Dleak} is extracted. (After Zhang, et al. [124].)

finger and multi-finger *n*MOSFETs demonstrate a substantial increase in the drain leakage current. Even though the drain leakage current increase slows down at ultrahigh TID levels, the rebound effect of interface-trapped charges does not appear [19, 152], suggesting the dominant influence of STI-trapped positive charges on the drain leakage current of 28-nm bulk *n*MOSFETs.

Additionally, the drain leakage current of single-finger *n*MOSFETs presents a width independence and a length dependence at high TID levels. The drain leakage current of single-finger *n*MOSFETs of the same length is similar (Fig. 4.17a and Fig. 4.17b), while that of single-finger MOSFETs of the same width is quite different (Fig. 4.17a and Fig. 4.17c). This width independence and length dependence jointly indicate the dominant contribution of the lateral parasitic devices.

The drain leakage current is also proportional to the number of fingers. At high TID levels, multi-finger *n*MOSFETs of the same gate length and the same number of fingers present almost the same amount of drain leakage current (Fig. 4.17d and Fig. 4.17e). However, those of the same device geometry have a drain leakage current proportional to the number of fingers (Fig. 4.17d and Fig. 4.17f). This scalability also suggests the primary contribution of the lateral parasitic devices.

4.3.2 Semi-empirical modeling of drain leakage current

As shown in Fig. 4.18, this modeling work mainly studies single-finger *n*MOSFETs at four corners of the $W_n - L_n$ plane, a multi-finger *n*MOSFET with $W_n = 3\,\mu m$ and $N_F = 4$, and multi-finger *n*MOSFETs with $W_n = 12\,\mu m$ and $N_F = [4,6,8,12]$, where N_F is the number of fingers [124]. Fig. 3.8a and Fig. 3.8c show that when the total dose is low, a zero V_{GB} still biases short-channel *n*MOSFETs in the V_T-sensitive subthreshold region. To avoid the influence of the subthreshold leakage on the following analysis, the total drain leakage current I_{Dleak} is extracted from the $I_D - (V_{GB} - V_T)$ curves at a constant $V_{GB} - V_T$.

Fig. 4.18a and Fig. 4.18e respectively plot the extracted I_{Dleak} of single-finger and multi-finger *n*MOSFETs as closed markers. They demonstrate a width dependence of the drain leakage current at low TID levels. In addition to the parasitic drain-to-source leakage current, the drain leakage current of an *n*MOSFET also consists of the subthreshold current, the drain-to-gate tunneling current, the GIDL, and the drain-to-substrate junction leakage [185]. These leakage components of the same length of *n*MOSFETs in general scale with the channel width. The observed width dependence suggests the dominant leakage contribution of the main channel at low TID levels.

Despite the width dependence at low TID levels, the drain leakage current of *n*MOSFETs with the same gate length and the same number of fingers is quite close at high TID levels. This confirms the width independence and the dependence on the gate length and the number of fingers, demonstrating the main contribution of the parasitic drain-to-source leakage current.

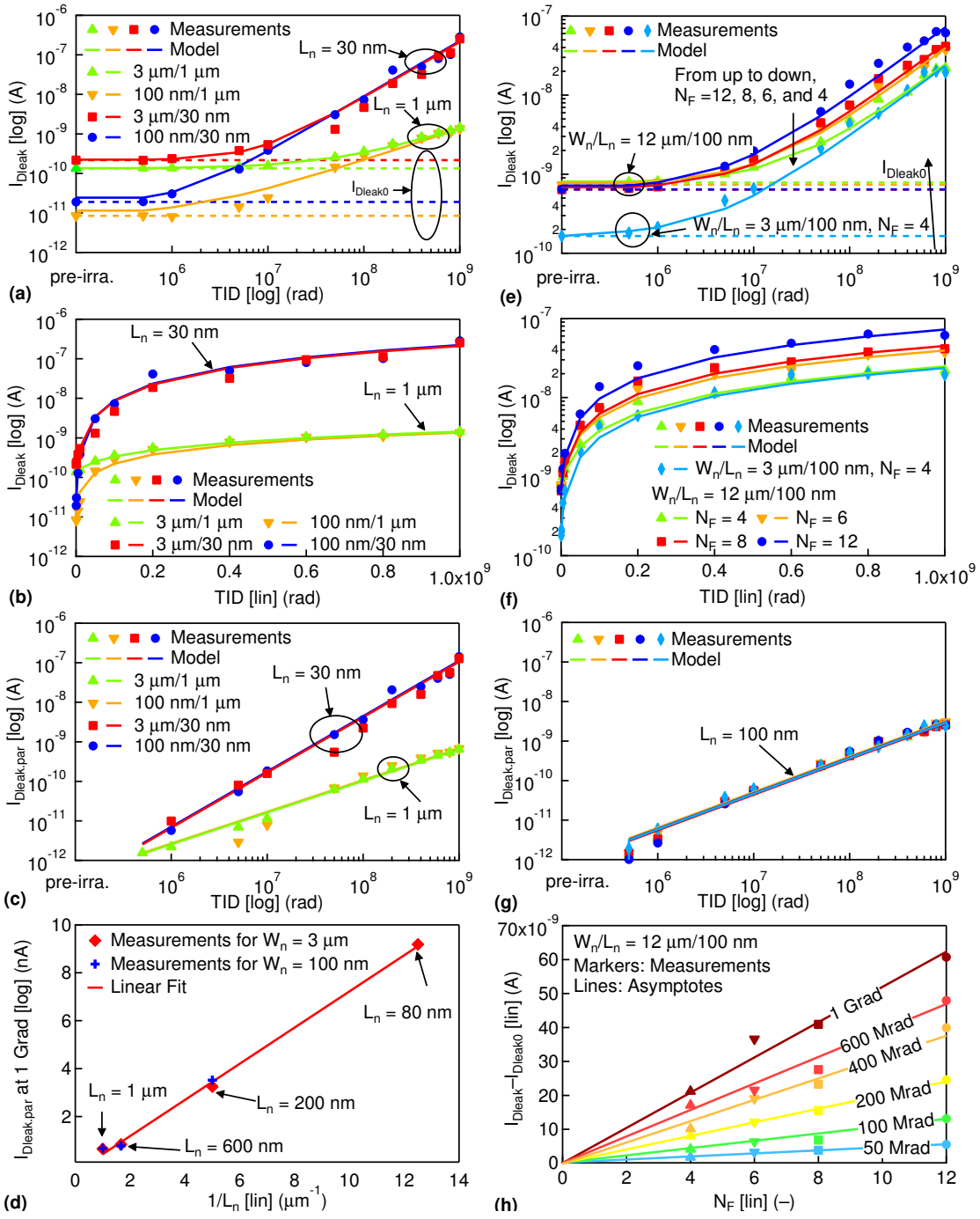


Figure 4.18 – Validation of the models for the drain leakage current I_{Dleak} of (a, b) single-finger and (e, f) multi-finger *n*MOSFETs in (a, e) log-log scale and (b, d) log-lin scale as a function of TID; (c, g) Validation of the models for the parasitic drain-to-source leakage current $I_{\mathrm{Dleak.par}}$ as a function of TID; (d) Extracted $I_{\mathrm{Dleak.par}}$ at 1 Grad of TID as a function of the channel length L_{n}; (h) total parasitic drain-to-source leakage current $I_{\mathrm{Dleak}} - I_{\mathrm{Dleak0}}$ of multi-finger *n*MOSFETs of the same size versus the number of fingers N_{F}. (After Zhang, et al. [124].)

The log-lin plots with closed markers in Fig. 4.18b and Fig. 4.18f indicate the fast drain leakage current increase before 200 Mrad and the saturating tendency of the drain leakage current at higher TID levels [124].

These experimental observations uncover the contribution of both the main channel ($I_{\mathrm{Dleak.main}}$) and the parasitic channels ($2N_{\mathrm{F}}I_{\mathrm{Dleak.par}}$) to the drain leakage current of an *n*MOSFET:

$$I_{\mathrm{Dleak}} = I_{\mathrm{Dleak.main}} + 2N_{\mathrm{F}}I_{\mathrm{Dleak.par}}, \tag{4.30}$$

as illustrated in Fig. 4.16. The drain leakage current of the main *n*MOSFET dominates at low TID levels. In addition to the subthreshold leakage, the drain-to-gate tunneling current and the GIDL are also linked to the threshold voltage, which is sensitive to TID. However, extracting I_{Dleak} at a constant $V_{\mathrm{GB}} - V_{\mathrm{T}}$ has eliminated the influence of the TID-induced V_{T} shift. The drain leakage current flowing through the main channel can therefore be assumed constant, corresponding to the plateau at low TID levels in Fig. 4.18a and Fig. 4.18e. Besides, the parasitic drain-to-source leakage current before irradiation is neglected, since neither the oxide-trapped charge density from the semiconductor processing nor the fringing field from the gate bias is strong enough to activate the parasitic channels [106].

Hence, the pre-irradiation drain leakage current I_{Dleak0} measures the drain leakage current of the main channel $I_{\mathrm{Dleak.main}}$. Solving Eq. (4.30) gives the average parasitic drain-to-source leakage current $I_{\mathrm{Dleak.par}}$:

$$I_{\mathrm{Dleak.par}} = \frac{I_{\mathrm{Dleak}} - I_{\mathrm{Dleak0}}}{2N_{\mathrm{F}}}. \tag{4.31}$$

Closed markers in Fig. 4.18c and Fig. 4.18g exhibit a significant $I_{\mathrm{Dleak.par}}$ increase and *n*MOSFETs of the same gate length reach the same level of $I_{\mathrm{Dleak.par}}$. As shown in Fig. 4.18d, the parasitic drain-to-source leakage current is linearly dependent on $1/L_{\mathrm{n}}$ when having $L_{\mathrm{n}} > 30\,\mathrm{nm}$. The parasitic drain-to-source leakage current of the shortest gate length ($L_{\mathrm{n}} = 30\,\mathrm{nm}$) falls beyond the linear fit due to short-channel effects. The linearity in Fig. 4.18h demonstrates the scaling property of the total parasitic drain-to-source leakage current with the number of fingers.

Considering a constant $I_{\mathrm{Dleak.main}}$ at all TID levels and a linear relation between I_{Dleak} and TID in log-log scale at high TID levels, as shown in Fig. 4.18a and Fig. 4.18e, a simple semi-empirical physics-based model is proposed to model the drain leakage current:

$$I_{\mathrm{Dleak}} = I_{\mathrm{Dleak0}}\left[1 + \left(\frac{D}{D_{\mathrm{crit}}}\right)^{l}\right], \tag{4.32}$$

where D_{crit} refers to critical total doses at which the lateral parasitic devices contribute the same amount of current as the main channel and l is the slope of the log-log plot at relatively high TID levels. The slope l is calculated by $(\log_{10} I_{\mathrm{Dleak2.par}} - \log_{10} I_{\mathrm{Dleak1.par}})/(\log_{10} D_2 - \log_{10} D_1)$ with two sets of measured data $I_{\mathrm{Dleak1.par}}(D_1)$ and $I_{\mathrm{Dleak2.par}}(D_2)$. Solving Eq. (4.31) and Eq. (4.32) finally leads to a semi-empirical physics-based model for the parasitic drain-to-

Table 4.1 – Parameters of the semi-empirical physical model for the drain-to-source leakage current (After Zhang, et al. [124])

W_n/L_n	N_F	I_{Dleak0}(A)	l	D_{crit} (Mrad)
3 µm/1 µm	1	1.34×10^{-10}	0.8	58.6
100 nm/1 µm	1	8.47×10^{-12}	0.8	1.78
3 µm/30 nm	1	2.17×10^{-10}	1.4	7.35
100 nm/30 nm	1	1.90×10^{-11}	1.4	1.24
3 µm/100 nm	4	1.65×10^{-10}	0.9	4.10
12 µm/100 nm	4	7.84×10^{-10}	0.9	22.4
12 µm/100 nm	6	7.37×10^{-10}	0.9	12.3
12 µm/100 nm	8	6.37×10^{-10}	0.9	8.95
12 µm/100 nm	12	6.42×10^{-10}	0.9	5.29

source leakage current:

$$I_{Dleak.par} = \frac{I_{Dleak0}}{2N_F}\left(\frac{D}{D_{crit}}\right)^{l}. \tag{4.33}$$

Fitting Eq. (4.32) with measurements determines the values of D_{crit} and l. Together with I_{Dleak0}, three model parameters are listed in Table 4.1. The power l shows a width dependence, whereas the pre-irradiation drain leakage current I_{Dleak0} and the critical total dose D_{crit} depend on the device geometry and the number of fingers. Model results are plotted as solid lines in Fig. 4.18. Using only three parameters, the proposed semi-empirical physics-based model matches measurements very well. This efficiency makes it a practical method for evaluating the parasitic drain-to-source leakage current and the total drain leakage current with respect to TID. The parameter D_{crit} indicates a specific TID level above which the total parasitic drain-to-source leakage current dominates over the drain leakage current of the main channel.

Measurement results under various bias conditions present similar levels of the drain leakage current, as observed from Fig. 3.19d and Fig. 3.19h. This demonstrates the promising use of this simple model in accurately predicting the drain leakage current of *n*MOSFETs working across the whole range of V_{DS} and V_{GB} from zero volt to V_{DD}. By extracting the corresponding values of three model parameters, this model can be easily adapted to simulate the TID-induced parasitic drain-to-source leakage current of alternative CMOS technologies.

4.3.3 Modeling of a gateless charge-controlled device

Concept of a gateless charge-controlled device

At high TID levels, the drain current at low values of the overdrive voltage is almost independent of the gate bias, as shown in Fig. 4.17. This weak or even negligible gate control is one distinctive feature of the lateral parasitic leakage path. It motivates us to model the parallel

parasitic transistor as a gateless charge-controlled device, as shown by the equivalent circuit in Fig. 4.19a [124]. Since this lateral parasitic device is assumed to be fully controlled by STI-related trapped charges, it is named *n*QFET.

The applied bias condition and the dynamic charge evolution during irradiation make the electrostatics inside the device complex. This results in a nonuniform charge buildup along STI sidewalls [60, 196], as shown in Fig. 3.23d. Moreover, complex channel doping engineering has been widely used in modern CMOS technologies, including the retrograde well for preventing the latch-up effect, the threshold voltage adjustment by ion implantation at the surface channel, the LDD region for suppressing the hot-carrier degradation, and the halo implantation for inhibiting the punchthrough effect [185, 190]. This leads to a nonuniform substrate doping profile [78, 196], as also illustrated in Fig. 3.23d. Both aspects influence the electrical characteristics of the lateral parasitic *n*QFET.

To simplify the modeling task, an equivalent structure is introduced for the lateral parasitic *n*QFET, as illustrated by the 3D schematic in Fig. 4.19b [124]. It has a uniform channel doping concentration N_{b} that is the same as the main channel. It also has an equivalent STI-related trapped-charge density $Q_{\mathrm{sti}} = qN_{\mathrm{sti}}$ that models the complex charge distribution:

$$Q_{\mathrm{sti}} = \frac{\int_0^{W_{\mathrm{sti}}} \int_0^{L_{\mathrm{sti}}} Q(x,y)\mathrm{d}x\mathrm{d}y}{W_{\mathrm{n.par}} L_{\mathrm{n.par}}}, \tag{4.34}$$

where N_{sti} is the equivalent STI-related trap density per unit area, $Q(x,y)$ is the local STI-related trapped-charge density per unit area, W_{sti} is the local width, L_{sti} is the local length, $W_{\mathrm{n.par}}$ is the equivalent channel width, and $L_{\mathrm{n.par}}$ is the equivalent channel length. The equivalent STI-related trapped-charge density per unit area Q_{sti} is uniform over a certain width $W_{\mathrm{n.par}}$ and length $L_{\mathrm{n.par}}$. The parasitic drain-to-source leakage current $I_{\mathrm{Dleak.par}}$ is assumed to spread across the whole depth of source and drain extensions. Here, $L_{\mathrm{n.par}}$ is

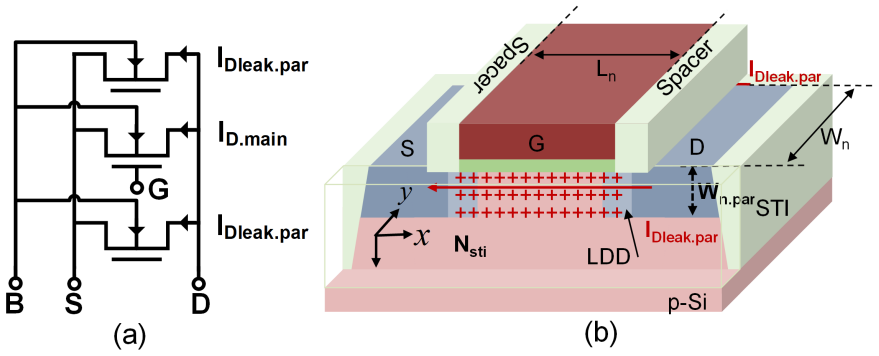


Figure 4.19 – (a) Equivalent circuit of an irradiated *n*MOSFET with two gate-independent parallel parasitic devices; (b) schematic illustration of the irradiated *n*MOSFET with two parasitic leakage paths formed by uniformly distributed STI-trapped positive charges. (After Zhang, et al. [124].)

assumed equal to the gate length of the main channel L_n and $W_{n.par}$ is assumed equal to the junction depth of source and drain extensions X_j.

Utilization of the simplified EKV MOSFET model

The simplified EKV MOSFET model has been seen capable of fully describing large- and small-signal characteristics over a wide range of inversion operation with only four parameters, i.e., the slope factor n, the specific current per square $I_{spec\square}$, the VS parameter λ_c, and the threshold voltage V_T [114, 122]. Since the gateless charge-controlled concept involves no gate voltage or gate-oxide capacitance, the simplified EKV MOSFET model needs to be adapted for the lateral parasitic *n*QFET.

Solving Gauss's law and 1-D Poisson's equation gives the relation between the local silicon charge density Q_{si} and the surface potential Ψ_s:

$$Q_{si} = -\Gamma_{b.par}\sqrt{U_T}\sqrt{\exp\frac{\Psi_s - 2\Phi_F - V_{ch}}{U_T} + \frac{\Psi_s}{U_T}}, \tag{4.35}$$

where $\Gamma_{b.par} = \sqrt{2q\epsilon_{si}N_b}$ is defined as the substrate modulation factor, ϵ_{si} is the silicon permittivity, $\Phi_F = U_T \ln(N_b/n_i)$ is the Fermi potential, and n_i is the intrinsic carrier concentration. The original substrate modulation factor is defined as $\Gamma_b = \sqrt{2q\epsilon_{si}N_b}/C_{ox}$ [96] that links $\Gamma_{b.par}$ by $\Gamma_{b.par} = \Gamma_b C_{ox}$.

The charge neutrality condition provides the key bridge between the STI-related trapped-charge density Q_{sti} and the total silicon charge density Q_{si}:

$$Q_{sti} = -Q_{si}. \tag{4.36}$$

Solving Eq. (4.35) and Eq. (4.36) gives the link between Q_{sti} and Ψ_s. Fig. 4.20a shows that for

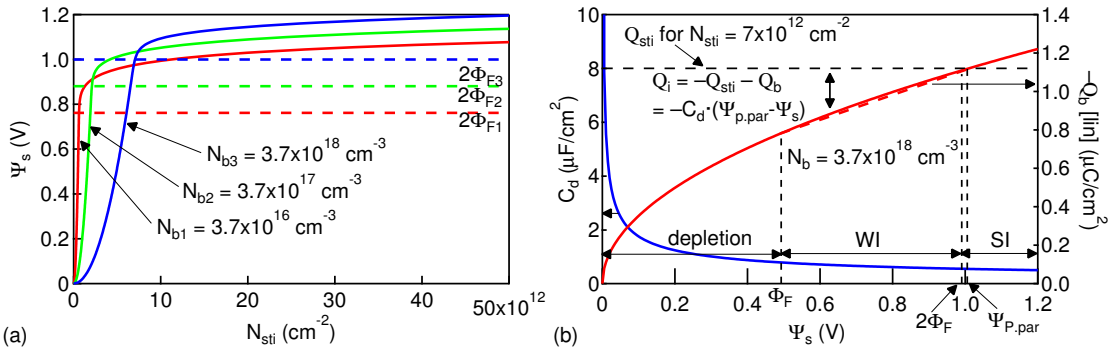


Figure 4.20 – (a) Surface potential Ψ_s versus the equivalent STI-related trap density per unit area N_{sti}; (b) linearization of the inversion charge density Q_i with respect to the surface potential Ψ_s. (After Zhang, et al. [124].)

a higher channel doping concentration N_b, a higher Q_{sti} is needed to switch on the lateral parasitic *n*QFET [124]. Since 28-nm bulk *n*MOSFETs may have $N_b = 3.7 \times 10^{18}\,cm^{-3}$ and $\Phi_F = 0.5\,V$, N_{sti} needs to be higher than $4.94 \times 10^{12}\,cm^{-2}$ for biasing the lateral parasitic *n*QFET in weak inversion ($\Phi_F < \Psi_s < 2\Phi_F$) and $7.06 \times 10^{12}\,cm^{-2}$ in strong inversion ($\Psi_s \geq 2\Phi_F$). The channel doping concentration increases along with CMOS scaling, which can be helpful for MOSFETs from advanced CMOS technologies to withstand high TID levels before having a significant parasitic drain-to-source leakage current.

Using the charge-sheet approximation, the depletion charge density can be expressed as $Q_b = -\Gamma_{b.par}\sqrt{\Psi_s}$. The differentiation of Q_b versus Ψ_s gives the expression of the depletion capacitance $C_d = \Gamma_{b.par}/(2\sqrt{\Psi_s})$. As shown in Fig. 4.20b, the depletion capacitance C_d slightly depends on the surface potential Ψ_s in inversion region [124]. This enables us to linearize the depletion charge density Q_b, as shown by the approximated red dashed line. The length of the vertical arrowed line represents the inversion charge density $Q_i = -Q_{sti} - Q_b$ that can be linearized as well in inversion region

$$Q_i = -C_d(\Psi_{P.par} - \Psi_s), \tag{4.37}$$

where $\Psi_{P.par}$ is the pinch-off potential. Once Ψ_s reaches $\Psi_{P.par}$, Q_i becomes 0 and Q_b is equal to $-Q_{sti}$, allowing us to express the pinch-off potential $\Psi_{P.par}$ as $\Psi_{P.par} \triangleq Q_{sti}^2/\Gamma_{b.par}^2$. In [96], the slope factor n is defined as $n = 1 + \Gamma_b/(2\sqrt{\Psi_s})$ that links the depletion capacitance C_d by $C_d = (n-1)C_{ox}$.

Subtracting the depletion charge density Q_b from the total silicon charge density Q_{si} gives the expression of the inversion charge density Q_i:

$$Q_i = -\Gamma_{b.par}\sqrt{U_T}\left[\sqrt{\exp\frac{-2\Phi_F - V_{ch}}{U_T}\left(\exp\frac{\Psi_s}{U_T} - 1\right) + \frac{\Psi_s}{U_T}} - \sqrt{\frac{\Psi_s}{U_T}}\right]. \tag{4.38}$$

When an *n*QFET is at the flatband, the surface potential Ψ_s and the inversion charge density Q_i become zero. Combining Eq. (4.37) and Eq. (4.38) and following the same derivation from (3.40) to (3.48) in [96] yield the revised expression of the charge-voltage relation

$$2q_i + \ln q_i = v_{p.par} - v, \tag{4.39}$$

where $q_i \triangleq Q_i/Q_{spec.par}$ is the normalized inversion charge density, $Q_{spec.par} \triangleq -2C_dU_T$ is the specific charge, and $v_{p.par} \triangleq V_{P.par}/U_T$ is the normalized pinch-off voltage

$$V_{P.par} \triangleq \frac{Q_{sti}^2}{\Gamma_{b.par}^2} - 2\Phi_F - U_T\ln 2. \tag{4.40}$$

Relying on the classical drift-diffusion transport model, the charge-current formula can still be derived as Eq. (4.4) but with a redefined specific current $I_{spec.par} \triangleq 2\mu_0 C_d W_{n.par} U_T^2/L_{n.par}$, where the low-field channel mobility μ_0 is assumed equal to that of the main channel. Combin-

ing Eq. (4.4) with Eq. (4.39) in saturation operation and introducing the effect of VS eventually result in the expression of the current-voltage relation for the lateral parasitic *n*QFET:

$$\begin{aligned} v_{\mathrm{p.par}} - v_{\mathrm{s}} = & \sqrt{4i_{\mathrm{dleak.par}} + \left(1 + \lambda_{\mathrm{c}} i_{\mathrm{dleak.par}}\right)^2} \\ & + \ln\left[\sqrt{4i_{\mathrm{dleak.par}} + \left(1 + \lambda_{\mathrm{c}} i_{\mathrm{dleak.par}}\right)^2} - 1\right] - (1 + \ln 2), \end{aligned} \tag{4.41}$$

where $i_{\mathrm{dleak.par}} \triangleq I_{\mathrm{Dleak.par}} / I_{\mathrm{spec.par}}$ is the normalized parasitic leakage current and the VS parameter λ_{c} is assumed equal to that of the main channel.

The proposed charge-controlled concept is similar to the work of Zebrev et al. in [209]. Zebrev et al. focus on modeling the inter-device parasitic leakage current underneath the STI oxide between the *n*-well of a *p*MOSFET and the n+ active region of the nearby *n*MOSFET, whereas this work is devoted to the parasitic drain-to-source leakage current in parallel with the main channel. Moreover, the work of Zebrev et al. is limited to linear operation and validated at low TID levels, whereas this work addresses the parasitic drain-to-source leakage current from linear to saturation and extends to high TID levels up to 1 Grad.

Weak inversion approximation

Solving Eq. (4.31) and Eq. (4.41) allows us to extract N_{sti} from measurements. Combining Eq. (4.33) with Eq. (4.41) enables us to model N_{sti} as a function of TID. Fig. 4.21a and Fig. 4.21b plot the square of the STI-related trap density N_{sti}^2 obtained from the extraction and the model [124]. Extracted and modeled results demonstrate a good agreement. The lateral parasitic *n*QFET of the same length have almost the same amount of STI-related trapped charges and the parasitic drain-to-source leakage current.

To have the surface potential Ψ_{s} higher than $2\Phi_{\mathrm{F}}$ and to bias the parasitic *n*QFET in strong inversion, the equivalent STI-related trap density N_{sti} needs to be higher than $7.06 \times 10^{12}\ \mathrm{cm}^{-2}$ for this 28-nm bulk CMOS technology. However, as shown in Fig. 4.21a and Fig. 4.21b, the highest value of N_{sti} is around $6.95 \times 10^{12}\ \mathrm{cm}^{-2}$ [124]. It indicates that even after 1 Grad of TID, the lateral parasitic *n*QFET works in weak inversion and might eventually enter the moderate inversion. Therefore, the weak inversion operation is considered for an approximated solution to the equivalent STI-related trap density.

In weak inversion, Eq. (4.39) is simplified to $\ln q_{\mathrm{i}} = v_{\mathrm{p.par}} - v_{\mathrm{s}}$. Substituting the normalized terms with the corresponding parameters brings the original charge-voltage expression: $Q_{\mathrm{i}} / (-2C_{\mathrm{d}} U_{\mathrm{T}}) = \exp[(V_{\mathrm{P.par}} - V_{\mathrm{ch}}) / U_{\mathrm{T}}]$. Introducing it into the drift-diffusion transport model and performing the integration over the range of V_{ch} result in the expression of the parasitic drain-to-source leakage current in weak inversion:

$$I_{\mathrm{Dleak.par}} = I_{\mathrm{spec.par}} \left(\exp \frac{V_{\mathrm{P.par}} - V_{\mathrm{S}}}{U_{\mathrm{T}}} - \exp \frac{V_{\mathrm{P.par}} - V_{\mathrm{D}}}{U_{\mathrm{T}}} \right). \tag{4.42}$$

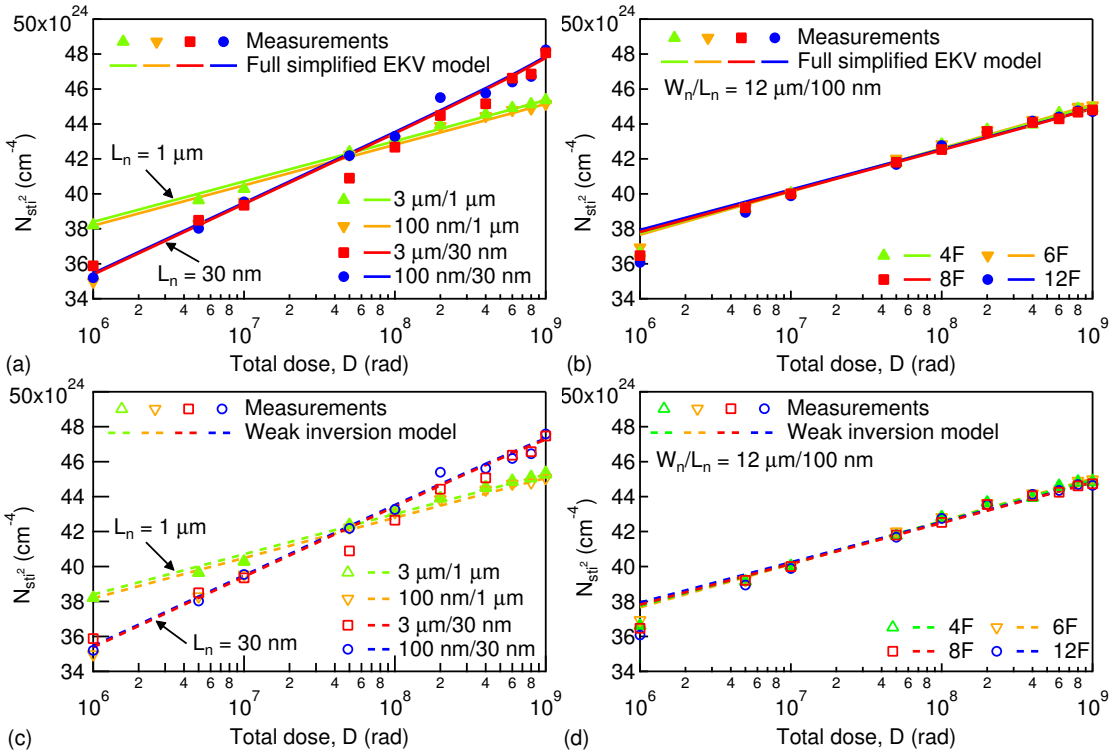


Figure 4.21 – The square of the STI-related trap density per unit area N_{sti}^2 obtained from measurements (markers) and the models (lines) as a function of total dose D corresponding to (a, c) single-finger and (b, d) multi-finger nMOSFETs. (a) and (b) rely on the full simplified EKV MOSFET model, while (c) and (d) correspond to weak inversion approximation. (After Zhang, et al. [124].)

Now the approximated solution to the STI-related trapped-charge density Q_{sti}^2 can be obtained by combining Eq. (4.33) and Eq. (4.42), introducing the saturation bias condition ($V_{\text{D}} > V_{\text{P.par}}$ and $V_{\text{S}} = 0\text{V}$), replacing $V_{\text{P.par}}$ with its full expression, and incorporating the effect of VS through the VS parameter:

$$Q_{\text{sti}}^2 = \Gamma_{\text{b.par}}^2 U_{\text{T}} \left[\ln\left(\frac{(2+\lambda_{\text{c}}) I_{\text{Dleak0}}}{2 I_{\text{spec.par}}} \right) + l \ln\left(\frac{D}{D_{\text{crit}}} \right) + \frac{2\Phi_{\text{F}}}{U_{\text{T}}} + \ln 2 \right]. \tag{4.43}$$

The square of the STI-related trap density N_{sti}^2 obtained from the weak inversion approximation is plotted in Fig. 4.21c and Fig. 4.21d [124]. The weak inversion approximation almost leads to the same results as the full simplified EKV MOSFET model, except for the slight mismatch at ultrahigh TID levels where the lateral parasitic nQFETs approach the moderate inversion. In addition, the straight lines fit the relation of $Q_{\text{sti}}^2 \propto l \ln(D/D_{\text{crit}})$ in Eq. (4.43). The weak inversion model therefore provides a very good approximation for the parasitic drain-to-source leakage current.

Replacing the defined terms in Eq. (4.42) with their full expressions provides a direct link

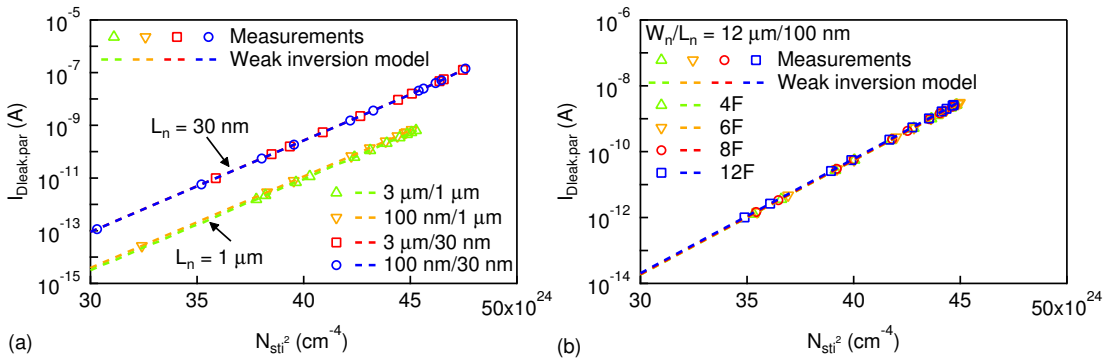


Figure 4.22 – Extracted and modeled parasitic drain-to-source leakage current $I_{\mathrm{Dleak.par}}$ as a function of the square of the equivalent STI-related trap density N_{sti}^2 corresponding to (a) single-finger and (b) multi-finger *n*MOSFETs. (After Zhang, et al. [124].)

between the parasitic drain-to-source leakage current $I_{\mathrm{Dleak.par}}$ and the channel doping concentration N_{b}:

$$I_{\mathrm{Dleak.par}} \propto \exp \frac{Q_{\mathrm{sti}}^2}{2q\epsilon_{\mathrm{si}} N_{\mathrm{b}} U_{\mathrm{T}}}. \tag{4.44}$$

Here, $I_{\mathrm{Dleak.par}}$ is an exponential function of Q_{sti}^2, as shown by the straight lines in the log-lin plots in Fig. 4.22. For a higher channel doping concentration N_{b}, the lateral parasitic *n*QFET needs a higher Q_{sti} for reaching the same amount of $I_{\mathrm{Dleak.par}}$. Advanced CMOS technologies with a higher channel doping concentration can therefore be advantageous to suppress radiation-induced static power consumption to a certain extent.

4.4 Summary

This chapter has presented a modeling-based investigation of the observed radiation effects on 28-nm bulk MOSFETs.

The simplified EKV MOSFET model is applied in saturation operation of 28-nm bulk MOSFETs to investigate the effects of TID up to 1 Grad on their analog parameters. Both large- and small-signal models demonstrate an excellent match with measurement results over the whole range of device operation. Five model parameters, including the slope factor, the threshold voltage, the specific current per square, the VS parameter, and the drain leakage current, efficiently capture the effects of TID on 28-nm bulk MOSFETs. The normalized transconductance efficiency calculated from pre- and post-irradiation measurements nicely falls on the same curves of the simplified EKV MOSFET model. Although TID affects design parameters of 28-nm bulk MOSFETs, the normalization strips off the effects of TID from the transconductance efficiency. This study shows that overall, this 28 nm bulk CMOS process is radiation tolerant at the switched-off region and it is promising to use the simplified EKV MOSFET model for radiation-tolerant circuit design.

The influence of TID on the effective channel mobility, which is one of the most important parameters for evaluating device performance, is investigated in strong inversion of linear operation using the Y-function approach. The majority of 28-nm bulk MOSFETs demonstrate a moderate degradation in the effective channel mobility. The low-field channel mobility reduction of wide-channel MOSFETs mostly originates from Coulomb scattering of interfacial charges related to the gate oxide. The low-field channel mobility of narrow-channel *n*MOSFETs degrades even more, indicating the additional influence of STI-related interface-trapped charges near the surface channel. Extracted results demonstrate a dramatic mobility reduction for narrow-channel *p*MOSFETs, which can actually be a result of the effective channel width reduction.

This chapter also experimentally and analytically investigates the TID-induced drain leakage current increase of 28-nm bulk MOSFETs. Through an experimental investigation of various sizes of MOSFETs, the slight drain leakage current increase of *p*MOSFETs is attributed to the peripheral substrate-drain junction leakage. This leakage is sensitive to STI-related interface-trapped charges surrounding the drain active region. At high TID levels, the drain leakage current of *n*MOSFETs is independent of the channel width but dependent on the gate length and the number of fingers. It indicates the dominant contribution of the parasitic channels induced by STI-trapped positive charges. To better account for the radiation-induced static power consumption, a semi-empirical physics-based model with only three parameters is proposed to simulate the leakage level as a function of TID. Considering the independence of the drain leakage current on the gate bias, the lateral parasitic transistor is modeled as a gateless charge-controlled device using a revised EKV MOSFET model. The weak inversion model provides a direct link between the STI-related trapped-charge density and the parasitic drain-to-source leakage current, indicating the suppressing effect of a higher channel doping concentration on radiation-induced static power consumption.

5 Charge-based physical modeling of TID effects

With adjusted values of existing parameters, the simplified EKV MOSFET model has demonstrated an excellent match with measurement results of 28-nm bulk MOSFETs, indicating its capability of characterizing nanoscale CMOS technologies and its promising use in simulating TID effects. This chapter focuses on modeling the observed radiation effects through the incorporation of TID-induced charge contribution into this simplified EKV MOSFET model. Further consideration of the low-field channel mobility degradation and the effective channel width reduction leads to a design-oriented compact model, which comprehensively accounts for TID effects on this 28-nm bulk CMOS process. The observed width dependence of TID effects is finally investigated for the introduction of device scalability into this radiation-aware physics-based model. This chapter exploits measurement results of two chips from the second tape-out irradiated under the diode condition ($|V_{GB}| = |V_{DS}| = 1.1\,V$) at room temperature (25 °C). It covers results published in [125] and recent results for one future publication [127].

5.1 A generalized EKV MOSFET model including traps

Despite complex physical processes of charge generation and evolution, TID eventually leads to charge trapping in critical dielectrics [130, 149] and active interface traps [166, 171]. Oxide- and interface-trapped charges can seriously degrade MOSFET characteristics and even cause circuit failures [45, 86]. Irradiation measurements have demonstrated several types of parametric shifts of 28-nm bulk MOSFETs and serious performance degradation of MOSFETs of typical dimensions in Section 3.2. To gain deeper insights about how charge trapping influences device performance and ultimately provide a predictive model for radiation-tolerant circuit design, this section focuses on modeling TID effects through the incorporation of radiation-induced charge trapping into the simplified EKV MOSFET model.

The benefits of using the simplified EKV MOSFET model has been addressed in Section 1.2.3. The simplified EKV MOSFET model with only a few parameters has demonstrated its capability of fully capturing electrical characteristics of 28-nm bulk MOSFETs in Section 4.1, motivating us to explore its further use in the comprehensive simulation of the observed radiation effects.

Introducing oxide- and interface-trapped charges into it extends its simple and efficient assets to defect-related device modeling. Its simplicity strongly relies on the inversion charge linearization with respect to the surface potential. It is truly this crucial step that enables a simple formulation of the current as a function of the inversion charge densities at the source and drain ends of the channel. These charge densities are directly proportional to the transconductance, which is among the most important parameters for circuit design. It is therefore key to find out how to include the effects of oxide- and interface-trapped charges while still being able to perform inversion charge linearization.

This section starts with a short review of oxide- and interface-charge trapping and their various effects on MOSFET electrostatics. It is then followed by the central part of this modeling work, where the inversion charge linearization is validated in the presence of oxide- and interface-trapped charges. While accounting for radiation-induced charge trapping, EKV MOSFET model equations, including 1) the equation relating the inversion charge density to the terminal voltages, 2) the equation expressing the drain current versus the inversion charge densities at the source and drain ends of the channel, and 3) the velocity saturation (VS)-related expressions, are revised accordingly. The developed model is finally validated with irradiation measurements of 28-nm bulk MOSFETs and utilized for investigating TID effects on crucial model parameters.

5.1.1 Incorporation of oxide- and interface-trapped charges

General remarks on charge trapping

Unlike in Section 2.2.4, where interface-charge trapping is described through the conversion of a P_b center between paramagnetic and diamagnetic states, it is here explained through charging and discharging an interface trap located within the forbidden band. Interface traps above the neutral trap energy level E_0 are of acceptor type and below it are of donor type [210]. Depending on the trap energy level E_t with respect to the Fermi level E_F, interface traps can be positively or negatively charged or remain neutral. Assuming E_0 to be at the intrinsic Fermi level E_i, interface traps above it are acceptors (green circles in Fig. 5.1) and those below it are donors (blue circles in Fig. 5.1) [126]. Acceptor-like interface traps are negatively charged when accepting an electron if below the electron quasi-Fermi level E_{Fn} and electrically neutral when being empty if above it. Donor-like interface traps are positively charged when emitting an electron if above the hole quasi-Fermi level E_{Fp} and electrically neutral when being occupied if below it. In inversion operation, interface-trapped charges are negative for an *n*MOSFET and positive for a *p*MOSFET, as shown in Fig. 5.1 [126].

Integrating the interface-trap density per unit area per unit energy D_{it} and its corresponding Fermi-Dirac occupation probability $f(E_t) = 1/\{1+g_t \exp[(E_t-E_F)/kT]\}$ over the whole bandgap gives the interface-trapped charge density per unit area Q_{it}, where g_t is the ground-state degeneracy factor [125]. Under the non-equilibrium condition, E_F corresponds to the quasi-Fermi level. Unfortunately, neither this integral nor a discretized summation of single-trap

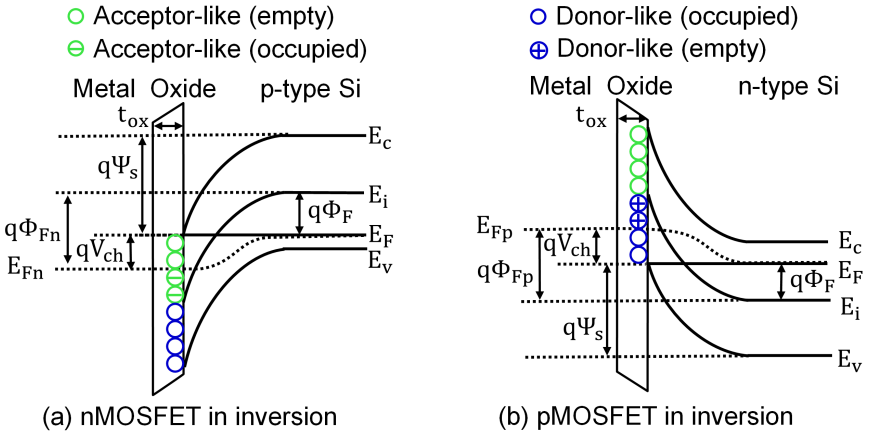


Figure 5.1 – Energy band diagrams illustrating interface-charge trapping in (a) an *n*MOSFET and (b) a *p*MOSFET in inversion. The quasi-Fermi level of the minority carriers, E_{Fn} or E_{Fp}, is split from that of the majority carriers E_F by the channel voltage V_{ch}. (After Zhang, et al. [126].)

energy levels can lead to a closed-form analytical solution [125]. To obtain a simple model for supporting circuit design while accounting for the effects of interface-trapped charges, interface traps are assumed uniform across the bandgap and their occupation probability is assumed to be unity. These assumptions provide a direct link between defects and key device parameters while showing representative device behaviors of double-gate MOSFETs in [125]. They can also yield sufficiently accurate expressions for describing defect-related effects and supporting circuit-level simulations [103]. Under these assumptions, Q_{it} can be expressed as [103, 125, 210]

$$Q_{it} = -qD_{it}(E_F - qV_{ch} - E_{is}) = -q^2 D_{it}(\Psi_s - \Phi_F - V_{ch}), \tag{5.1}$$

where $\Psi_s = (E_{ib} - E_{is})/q$ is the surface potential, E_{ib} is the bulk intrinsic Fermi level, E_{is} is the surface intrinsic Fermi level, and $\Phi_F = (E_{ib} - E_F)/q$ is the Fermi potential.

Oxygen vacancies from incomplete oxidation can trap holes generated by ionizing radiation or tunneling from the channel [149, 150]. Deep oxide-trapping centers generally do not interfere with the bias condition. Their slow charge-state transitions result in a fixed oxide-trapped charge density per unit area $Q_{ot} = qN_{ot}$, where N_{ot} is the oxide-trap density per unit area. Oxide-trapping centers near the silicon/oxide interface with trap energy levels close to the intrinsic Fermi level (i.e., border traps or switching oxide traps [46]) may respond promptly to external bias changes and therefore are included into interface traps. It should be mentioned that interface traps respond much faster to changes in the surface potential than border traps. Lumping border traps into interface traps can compromise the model accuracy for frequency-dependent characteristics. This thesis focuses on the investigation of DC characteristics, for which this simplification should not be a concern. However, special care should always be taken for the modeling work on frequency-dependent characteristics.

Impact of trapped charges on MOS electrostatics

The model development begins with a long-channel *n*MOSFET, for which the gradual channel approximation remains valid [96]. Trapped charges are assumed to be in a charge sheet of negligible thickness at the oxide side of the silicon/oxide interface and hence, do not need to be included in Poisson's equation [105, 211]. Solving 1-D Poisson's equation for the total silicon charge density $Q_{si} = Q_i + Q_b$, subtracting the depletion charge density $Q_b = -\Gamma_b C_{ox}\sqrt{\Psi_s}$ solved from the charge-sheet approximation, and neglecting the hole contribution gives the inversion charge density per unit area Q_i, as (3.38) in [96]:

$$-\frac{Q_i}{C_{ox}} = \Gamma_b\sqrt{U_T}\left[\sqrt{\exp\frac{\Psi_s - 2\Phi_F - V_{ch}}{U_T} + \frac{\Psi_s}{U_T}} - \sqrt{\frac{\Psi_s}{U_T}}\right]. \tag{5.2}$$

Here, neglecting holes makes this charge-based model invalid in accumulation region of a MOSFET.

The equivalent scheme of a MOSFET in Fig. 5.2 can be referred to during the following steps of solving boundary conditions. Introducing oxide- and interface-trapped charges into the charge balance equation yields

$$Q_G + Q_f + Q_{si} = -(Q_{ot} + Q_{it}), \tag{5.3}$$

where $Q_G = C_{ox}V_{ox}$ is the gate charge density per unit area, $V_{ox} = V_{GB} - \Phi_{ms} - \Psi_s$ is the voltage drop across the gate oxide, Φ_{ms} is the metal-silicon work function difference, and Q_f is the fixed oxide-charge density per unit area. Substituting each charge contribution with its full expression and solving for the inversion charge density per unit area leads to

$$-\frac{Q_i}{C_{ox}} = V_{GB} - \left[V_{FB} + c_{it}(\Psi_s - V_{ch}) + \Psi_s + \Gamma_b\sqrt{\Psi_s}\right], \tag{5.4}$$

where $c_{it} \triangleq C_{it}/C_{ox}$ is defined as the normalized interface-charge capacitance with $C_{it} = q^2 D_{it}$ being the interface-charge capacitance. The importance of c_{it} becomes clearer through the investigation of the influence of interface-trapped charges on crucial device parameters. Here, V_{FB} is the flatband voltage defined under the equilibrium condition ($V_{ch} = 0\,\mathrm{V}$) as the particular

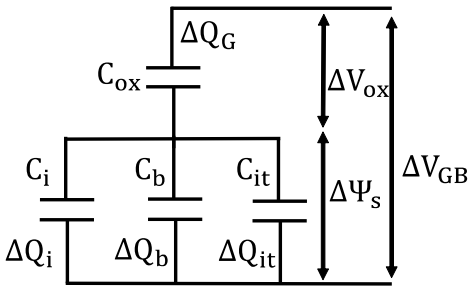


Figure 5.2 – Equivalent scheme of a MOSFET for CV characteristics.

value of the gate-to-bulk voltage at which the silicon energy band is flat ($\Psi_s = 0\,\mathrm{V}$) [99]:

$$V_{FB} \triangleq \Phi_{ms} - \frac{Q_f}{C_{ox}} - \left(\frac{qN_{ot}}{C_{ox}} + c_{it}\Phi_F\right). \tag{5.5}$$

Unfortunately, Eq. (5.2) and Eq. (5.4) cannot be reversed, making it impossible to solve the surface potential and the inversion charge density directly from the terminal voltages in a

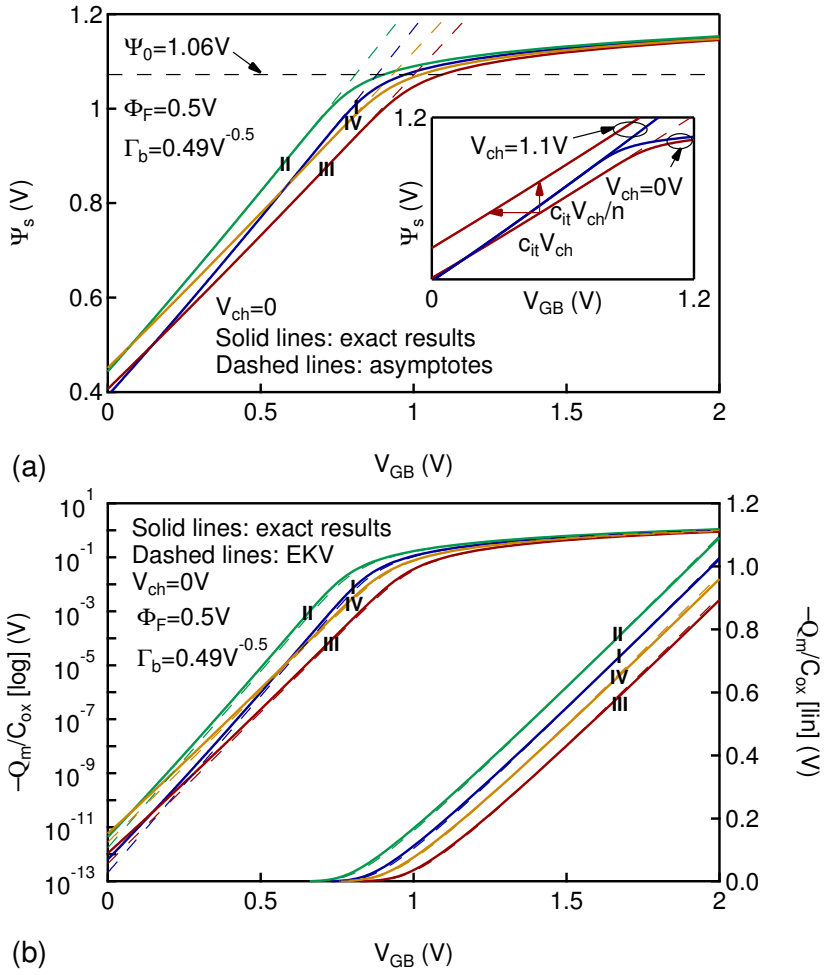


Figure 5.3 – (a) Surface potential Ψ_s and (b) inversion-charge-density-related potential $-Q_i/C_{ox}$ versus the gate-to-bulk voltage V_{GB} at different values of the oxide-trap density N_{ot} and the interface-trap density D_{it} for an *n*MOSFET, illustrating the impact of oxide- and interface-trapped charges on MOS electrostatics. Case I: $N_{ot} = D_{it} = 0, V_{FB} = -0.7\,\mathrm{V}$; case II: $N_{ot} = 1\times10^{12}\,\mathrm{cm}^{-2}, D_{it} = 0, V_{FB} = -0.77\,\mathrm{V}$; case III: $N_{ot} = 0, D_{it} = 3\times10^{12}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}, V_{FB} = -0.81\,\mathrm{V}$; case IV: $N_{ot} = 1\times10^{12}\,\mathrm{cm}^{-2}, D_{it} = 3\times10^{12}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}, V_{FB} = -0.88\,\mathrm{V}$. Solid lines plot the exact results solved from Eq. (5.2) and Eq. (5.4). Dashed lines plot the strong and weak inversion asymptotes of the surface potential in (a) and the results of the charge-voltage formula Eq. (5.20) in (b). (After Zhang, et al. [126].)

closed-form expression. The surface potential is therefore set in Eq. (5.2) to solve for the inversion charge density. The corresponding values of the surface potential and the inversion charge density are then put into Eq. (5.4) to solve for the gate-to-bulk voltage. The surface potential and the inversion charge density are now plotted with respect to the gate-to-bulk voltage in Fig. 5.3 as solid lines for four typical cases: case I, no charge trapping; case II, oxide-charge trapping only; case III, interface-charge trapping only; case IV, both oxide- and interface-charge trapping [126].

One important defect-related effect is the subthreshold swing degradation due to interface-trapped charges [210]. This is usually observed from MOSFET transfer characteristics. It can also be perceived from the relation of the surface potential and the inversion charge density versus the gate-to-bulk voltage. Another important defect-related effect is the threshold voltage shift. For an *n*MOSFET, positive oxide-trapped charges shift the curves to the left and negative interface-trapped charges move the curves to the right. However, two types of charges tend to counterbalance each other and eventually result in a moderate threshold voltage shift. For a *p*MOSFET, both types of charges are positive, leading to a significant threshold voltage shift. The discrepancy between the exact results and the model calculation at low values of V_{GB} refers to the invalidity of this model in the accumulation region.

5.1.2 Inversion charge linearization

Eq. (5.2) and Eq. (5.4) have been solved from 1-D Poisson's equation and boundary conditions, respectively. The inversion-charge-density-related potential $-Q_{\mathrm{i}}/C_{\mathrm{ox}}$ can be solved individually from these two equations as a function of the surface potential Ψ_{s} and the channel voltage V_{ch} at a given gate-to-bulk voltage V_{GB} and a given interface-trap density D_{it}, corresponding to those two surfaces in Fig. 5.4. The intersection of these two surfaces demonstrates the final solution to the inversion charge density under a certain bias condition. However, solving Eq. (5.2) and Eq. (5.4) does not yield an analytical expression of the inversion charge density versus the external biases. To reach a closed-form expression including interface traps, we propose to first find an approximate expression of Eq. (5.4) through inversion charge linearization and then introduce it into Eq. (5.2) for eventually deriving an approximate solution, as done for the original EKV MOSFET model [96].

Linearizing the inversion charge density versus the surface potential is a fundamental step towards the development of the original EKV MOSFET model, which however does not include defect-related effects [96, 212]. In this part of the modeling work, it is demonstrated that in the presence of oxide- and interface-trapped charges, the inversion charge density can still be linearized. This enables us to obtain explicit model equations similar to those of the original EKV MOSFET model but with an additional scaling factor and revised device parameters. Since oxide-trapped charges simply reduce the flatband voltage without influencing the linear behavior of the inversion charge density, the following discussion will focus on the incorporation of interface-trapped charges into the inversion charge linearization using Fig. 5.5 [126].

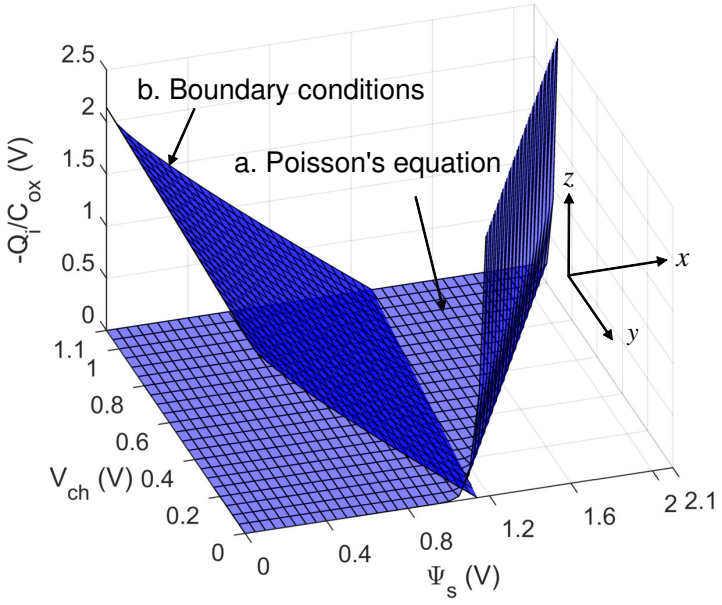


Figure 5.4 – Inversion-charge-density-related potential $-Q_\mathrm{i}/C_\mathrm{ox}$ versus the surface potential Ψ_s and the channel voltage V_ch solved from (a) 1-D Poisson's equation and (b) boundary conditions at a given gate-to-bulk voltage ($V_\mathrm{GB} = 1.1\,\mathrm{V}$) and a given interface-trap density ($D_\mathrm{it} = 3\times10^{12}\,\mathrm{cm^{-2}eV^{-1}}$).

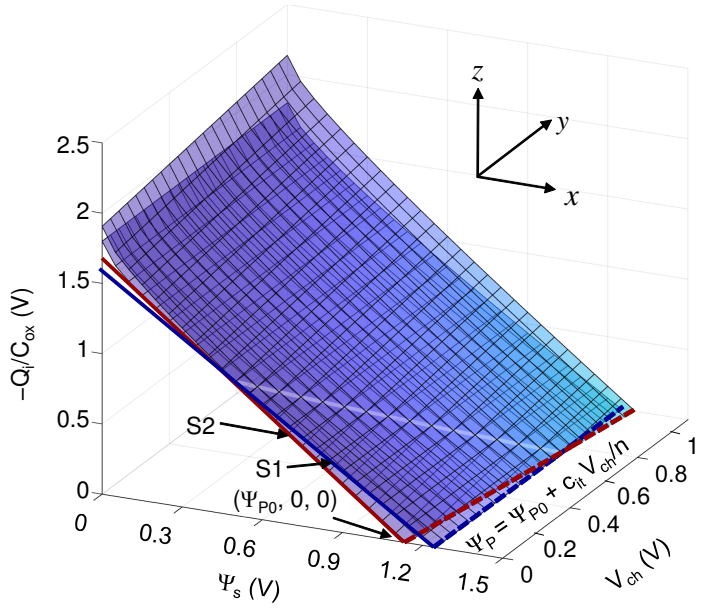


Figure 5.5 – Inversion-charge-density-related potential $-Q_\mathrm{i}/C_\mathrm{ox}$ versus the surface potential Ψ_s and the channel voltage V_ch at a given gate-to-bulk voltage ($V_\mathrm{GB} = 1.1\,\mathrm{V}$) for an nMOSFET, illustrating the validation of inversion charge linearization. S1 and S2 refer to a zero value and $3\times10^{12}\,\mathrm{cm^{-2}eV^{-1}}$ of the interface-trap density D_it, respectively. (After Zhang, et al. [126].)

In the absence of interface-charge trapping and at a given gate-to-bulk voltage, the inversion charge density given by Eq. (5.4) is independent of the channel voltage, as shown by the surface S1 in Fig. 5.5. The surface potential at which the inversion charge density becomes zero is defined as the pinch-off potential Ψ_P [96]. It is also independent of the channel voltage, as illustrated in Fig. 5.5 by the blue dashed line, which is the intersection of the surface S1 and the floor plane at a zero Q_i. Furthermore, the inversion charge density is almost linear with respect to the surface potential [96], as evidenced by the blue solid line in Fig. 5.5, which is the intersection of the surface S1 and the vertical plane at a zero V_{ch}. This is consistent with the weak dependence of the slope factor $n(\Psi_s) = d(-Q_i/C_{ox})/d\Psi_s = 1 + \Gamma_b/(2\sqrt{\Psi_s})$ on the surface potential in inversion, as demonstrated by the blue line in Fig. 5.6 for a zero D_{it} [126].

Except for the dependence on the surface potential, interface-charge trapping makes the inversion charge density also depend on the channel voltage. Hence, the pinch-off potential becomes also a function of the channel voltage, as illustrated in Fig. 5.5 by the red dashed line, which is the intersection of the surface S2 and the floor plane. This red dashed line corresponds to a function that relates the pinch-off potential to the gate-to-bulk voltage:

$$V_{GB} \cong V_{FB} + c_{it}(\Psi_P - V_{ch}) + \Psi_P + \Gamma_b\sqrt{\Psi_P}. \tag{5.6}$$

The pinch-off potential can be solved from Eq. (5.6) as

$$\Psi_P = \frac{1}{\theta}\left[V^*_{GB} - \Gamma_b^2\left(\sqrt{\frac{V^*_{GB}}{\theta\,\Gamma_b^2} + \frac{1}{(2\theta)^2}} - \frac{1}{2\theta}\right)\right], \tag{5.7}$$

where $V^*_{GB} \triangleq V_{GB} - V_{FB} + c_{it}V_{ch}$ and $\theta \triangleq 1 + c_{it}$. Setting $c_{it} = 0$ or equivalently $\theta = 1$ in Eq. (5.7) brings the original pinch-off potential Ψ_P, i.e., (3.37) in [96]. Setting a zero V_{ch} or equivalently $V^*_{GB} = V_{GB} - V_{FB}$ in Eq. (5.7) gives the pinch-off potential under the equilibrium condition Ψ_{P0}.

Since the surface S2 in Fig. 5.5 remains "flat" in the regions of interest, the inversion charge density in Eq. (5.4) can be linearized but with respect to both the surface potential Ψ_s and the channel voltage V_{ch}. Linearizing Eq. (5.4) versus Ψ_s and V_{ch} around the point ($\Psi_s = \Psi_{P0}$, $V_{ch} = 0$, and $Q_i = 0$) results in

$$-\frac{Q_i}{C_{ox}} \cong -n(\Psi_s - \Psi_{P0}) + c_{it}V_{ch}, \tag{5.8}$$

where

$$n \triangleq -\left.\frac{\partial(-Q_i/C_{ox})}{\partial\Psi_s}\right|_{\Psi_s=\Psi_{P0},V_{ch}=0} = 1 + \frac{\Gamma_b}{2\sqrt{\Psi_{P0}}} + c_{it} \tag{5.9}$$

is the slope factor $n(\Psi_s) = 1 + \Gamma_b/(2\sqrt{\Psi_s}) + c_{it}$ including the influence of interface-trapped charges and evaluated at the pinch-off potential under the equilibrium condition. The slope factor $n(\Psi_s)$ corresponding to a high density of interface traps is plotted versus the surface potential Ψ_s as the red line in Fig. 5.6 [126]. In inversion, it is still a weak function of the surface

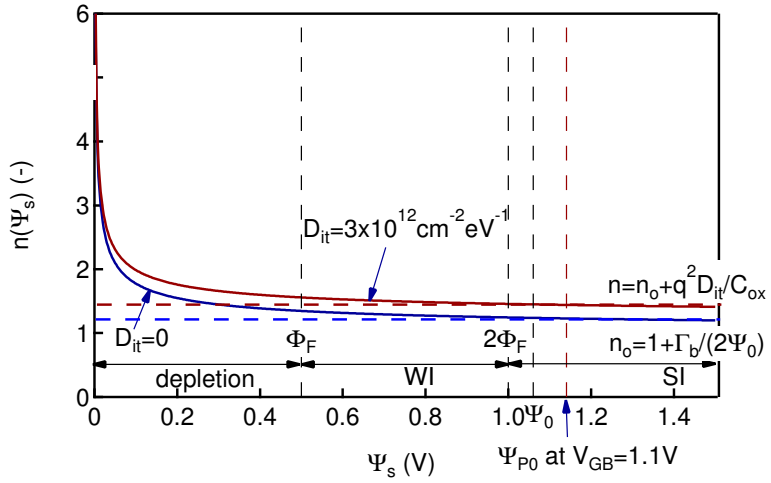


Figure 5.6 – Slope $n(\Psi_s)$ of the inversion-charge-density-related potential $-Q_i/C_{ox}$ versus the surface potential Ψ_s at a given gate-to-bulk voltage ($V_{GB} = 1.1\,V$) and different values of the interface-trap density D_{it} for an nMOSFET, illustrating the validation of inversion charge linearization. (After Zhang, et al. [126].)

potential and can therefore be approximated as a constant:

$$n \cong 1 + \frac{\Gamma_b}{2\sqrt{\Psi_0}} + c_{it} = n_0 + \frac{q^2 D_{it}}{C_{ox}}, \tag{5.10}$$

where $n_0 = 1 + \Gamma_b/(2\sqrt{\Psi_0})$ is the slope factor in the absence of interface-charge trapping and $\Psi_0 = 2\Phi_F + mU_T$ is a constant slightly larger than $2\Phi_F$ (m is typically between 2 and 4) [96].

Setting a zero Q_i in Eq. (5.8) and solving for the surface potential leads to an approximation of the pinch-off potential:

$$\Psi_P \cong \Psi_{P0} + \frac{c_{it}}{n} V_{ch}, \tag{5.11}$$

which corresponds to the intersection of the approximated surface of S2 and the floor plane, as plotted by the red dashed line in Fig. 5.5. Introducing it into Eq. (5.8) yields

$$-\frac{Q_i}{C_{ox}} \cong -n(\Psi_s - \Psi_P), \tag{5.12}$$

which is identical to the original expression, i.e., (3.39) in [96], except that the pinch-off potential now depends on the channel voltage, according to Eq. (5.7) or Eq. (5.11).

In weak inversion, the inversion charge density remains negligible compared to the depletion charge density. Combining Eq. (5.2) and Eq. (5.4) and neglecting the exponential term leads to an approximate expression of the gate-to-bulk voltage versus the surface potential [190]:

$$V_{GB} \cong V_{FB} + c_{it}(\Psi_s|_{wi} - V_{ch}) + \Psi_s|_{wi} + \Gamma_b\sqrt{\Psi_s|_{wi}}, \tag{5.13}$$

which is identical to Eq. (5.6). Solving it for $\Psi_s|_{wi}$ gives the weak inversion asymptote of the Ψ_s versus V_{GB} curves, as plotted by the colored dashed lines in Fig. 5.3a. By definition, the pinch-off potential solved from Eq. (5.6) actually falls on this weak inversion asymptote. The inserted figure in Fig. 5.3a presents the dependence of the pinch-off potential on the channel voltage in the presence of interface-charge trapping.

5.1.3 Revised EKV MOSFET model equations

Inversion charge linearization has proved to be valid in the presence of oxide- and interface-trapped charges. Implementing it in the derivation of the charge-voltage relation, the current-charge relation, and the VS model leads to the generalized EKV MOSFET model that accounts for defect-related effects.

Charge-voltage relation

An explicit expression of the surface potential can be obtained in the form of the inversion charge density and the channel voltage from Eq. (5.8) and introduced into Eq. (5.2) for deriving an explicit expression of the charge-voltage relation. To do this, it is convenient to first rewrite Eq. (5.2) in its normalized form:

$$\psi_s - 2\phi_f - v = \ln\left[q_i \frac{2n}{\gamma_b}\left(q_i \frac{2n}{\gamma_b} + 2\sqrt{\psi_s}\right)\right], \tag{5.14}$$

where $q_i \triangleq Q_i/Q_{spec}$ with $Q_{spec} \triangleq -2nU_T C_{ox}$ still defined as the specific charge, $\psi_s \triangleq \Psi_s/U_T$, $\phi_f \triangleq \Phi_F/U_T$, and $\gamma_b \triangleq \Gamma_b/\sqrt{U_T}$. The surface potential solved from Eq. (5.8) is normalized as

$$\psi_s = \psi_{p0} + \frac{c_{it}}{n} v - 2q_i \tag{5.15}$$

with $\psi_{p0} \triangleq \Psi_{P0}/U_T$ as the normalized pinch-off potential.

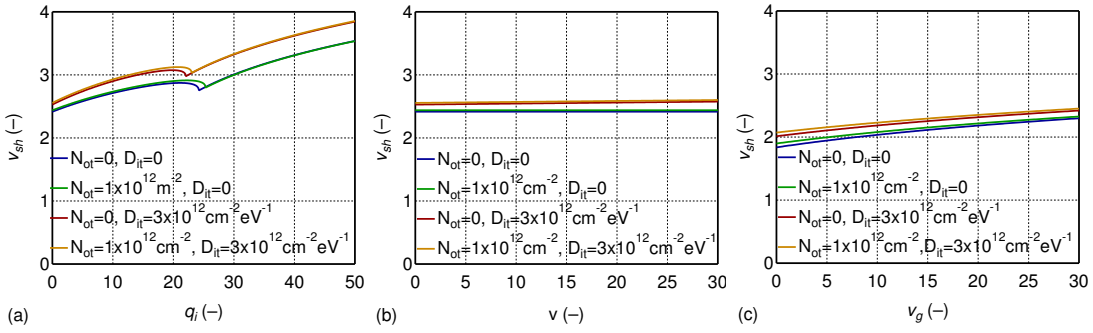


Figure 5.7 – Normalized threshold shift v_{sh} as a function of (a) the normalized inversion charge density q_i, (b) the normalized channel voltage v, and (c) the normalized gate-to-bulk voltage v_g at different values of the oxide-trap density N_{ot} and the interface-trap density D_{it}.

Substituting the normalized surface potential in Eq. (5.14) with Eq. (5.15) and rearranging the mathematical terms results in

$$2q_\mathrm{i} + \ln q_\mathrm{i} = \psi_\mathrm{p0} - 2\phi_\mathrm{f} - \frac{n_0}{n}\upsilon - \underbrace{\ln\left[\frac{2n}{\gamma_\mathrm{b}}\left(q_\mathrm{i}\frac{2n}{\gamma_\mathrm{b}} + 2\sqrt{\psi_\mathrm{p0} + \frac{c_\mathrm{it}}{n}\upsilon - 2q_\mathrm{i}}\right)\right]}_{\upsilon_\mathrm{sh}}, \tag{5.16}$$

where υ_sh is the threshold shift. Due to the simplifications for Eq. (5.2), this expression is valid only when $\psi_\mathrm{p} \geq 2q_\mathrm{i}$ ($\psi_\mathrm{p} = 2q_\mathrm{i}$ corresponds to $\psi_\mathrm{s} = 0$). Fig. 5.7a shows the υ_sh variation with respect to q_i. The υ_sh variation never exceeds unity, allowing us to neglect the q_i term:

$$\upsilon_\mathrm{sh} \approx \ln\left(\frac{4n}{\gamma_\mathrm{b}}\sqrt{\psi_\mathrm{p0} + \frac{c_\mathrm{it}}{n}\upsilon}\right), \tag{5.17}$$

which is seen almost independent of υ in Fig. 5.7b, enabling us to further neglect the υ term:

$$\upsilon_\mathrm{sh} = m \approx \ln\left(\frac{4n}{\gamma_\mathrm{b}}\sqrt{\psi_\mathrm{p0}}\right). \tag{5.18}$$

Fig. 5.7c plots Eq. (5.18) as a function of υ_g and demonstrates a weak function of $\psi_\mathrm{p0}(\upsilon_\mathrm{g})$. Eventually, the threshold shift υ_sh is approximated as a constant at 2.8 for this 28-nm bulk CMOS process.

The normalized pinch-off voltage is defined as the particular value of the normalized channel voltage at which the left hand side of Eq. (5.16) is equal to zero:

$$\upsilon_\mathrm{p} = \frac{n}{n_0}(\psi_\mathrm{p0} - 2\phi_\mathrm{f} - \upsilon_\mathrm{sh}). \tag{5.19}$$

Introducing Eq. (5.19) into Eq. (5.16) eventually leads to the explicit charge-voltage equation

$$2q_\mathrm{i} + \ln q_\mathrm{i} = \frac{n_0}{n}(\upsilon_\mathrm{p} - \upsilon). \tag{5.20}$$

Compared to the original equation, i.e., Eq. (4.10) [96], Eq. (5.20) includes a scaling factor $n_0/n = 1/(1 + c_\mathrm{it}/n_0)$ to account for the effects of interface-trapped charges. Solving Eq. (5.20) with υ equal to $\upsilon_\mathrm{s} \triangleq V_\mathrm{SB}/U_\mathrm{T}$ or $\upsilon_\mathrm{d} \triangleq V_\mathrm{DB}/U_\mathrm{T}$ gives the normalized inversion charge density at the source or the drain end of the channel (q_s or q_d).

To further simplify Eq. (5.20), an approximate expression of the pinch-off voltage is obtained using the strong inversion approximation. The pinch-off voltage in strong inversion is defined as the particular value of the channel voltage at which the inversion charge density becomes zero. With oxide- and interface-charge trapping, the surface potential still tends to saturate around $\Psi_\mathrm{s}|_\mathrm{si} \cong \Psi_0 + V_\mathrm{ch}$, as shown by the horizontal dashed line in Fig. 5.3a. Introducing this strong inversion approximation into Eq. (5.4) and solving it with a zero Q_i leads to a function relating the gate-to-bulk voltage to the pinch-off voltage:

$$V_\mathrm{GB} \cong V_\mathrm{FB} + (1 + c_\mathrm{it})\Psi_0 + V_\mathrm{P} + \Gamma_\mathrm{b}\sqrt{\Psi_0 + V_\mathrm{P}}. \tag{5.21}$$

This equation is plotted in Fig. 5.8, which demonstrates an almost linear relation between the gate-to-bulk voltage and the pinch-off voltage for any of those four typical cases investigated in Fig. 5.3 [126]. This is consistent with the almost constant first-order derivative of Eq. (5.21) versus the pinch-off voltage $\mathrm{d}V_{\mathrm{GB}}/\mathrm{d}V_{\mathrm{P}} = 1+\Gamma_{\mathrm{b}}/(2\sqrt{\Psi_0+V_{\mathrm{P}}}) \cong 1+\Gamma_{\mathrm{b}}/(2\sqrt{\Psi_0})$, which corresponds to the slope factor in the absence of interface-charge trapping n_0.

The threshold voltage is now defined under the equilibrium condition as the particular value of the gate-to-bulk voltage when the inversion charge density becomes zero:

$$V_{\mathrm{T}} = \underbrace{\Phi_{\mathrm{ms}} - \frac{Q_{\mathrm{f}}}{C_{\mathrm{ox}}} + \Psi_0 + \Gamma_{\mathrm{b}}\sqrt{\Psi_0}}_{\mathrm{V_{T0}}} + \underbrace{c_{\mathrm{it}}(\Psi_0 - \Phi_{\mathrm{F}}) - \frac{qN_{\mathrm{ot}}}{C_{\mathrm{ox}}}}_{\Delta \mathrm{V_T}}, \tag{5.22}$$

where V_{T0} is the threshold voltage in the absence of oxide and interface traps and ΔV_{T} is the threshold voltage shift induced by the compensated effect of oxide- and interface-trapped charges. Unlike for an *n*MOSFET, both types of trapped charges are positive for a *p*MOSFET and influence its threshold voltage in the same direction.

The pinch-off voltage can now be approximated as

$$V_{\mathrm{P}} \cong \frac{V_{\mathrm{GB}} - V_{\mathrm{T}}}{n_0}, \tag{5.23}$$

which demonstrates a linear relation with the gate-to-bulk voltage. This approximate pinch-off voltage is influenced by oxide- and interface-charge trapping only through the threshold voltage. Its constant slope versus the gate-to-bulk voltage is consistent with the derivatives of Eq. (5.6) and Eq. (5.19): $\mathrm{d}V_{\mathrm{GB}}/\mathrm{d}V_{\mathrm{P}} = (n_0/n)(\mathrm{d}V_{\mathrm{GB}}/\mathrm{d}\Psi_{\mathrm{P0}}) = (n_0/n)(\mathrm{d}V_{\mathrm{GB}}/\mathrm{d}\Psi_{\mathrm{P}}) = n_0$. The

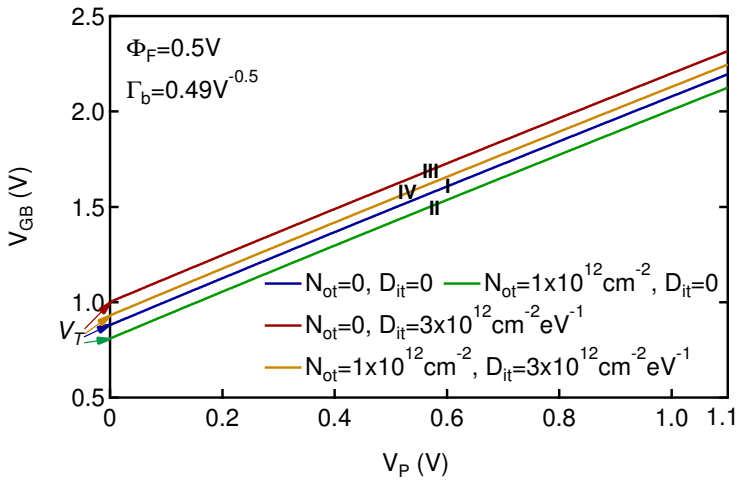


Figure 5.8 – Gate-to-bulk voltage V_{GB} versus the pinch-off voltage V_{P} at different values of the oxide-trap density N_{ot} and the interface-trap density D_{it} for an *n*MOSFET, illustrating the influence of oxide- and interface-trapped charges on the threshold voltage. (After Zhang, et al. [126].)

dashed lines in Fig. 5.3b plot the approximate solution of the inversion charge density solved from Eq. (5.20) and Eq. (5.23). The approximate solution demonstrates a slight variation with respect to its exact counterpart at low values of V_{GB} for all of those four cases, which can be a result of approximating v_{sh} to be a constant, as derived from Fig. 5.7. Except for this region, the approximate solution matches very well with its exact counterpart, demonstrating the sufficient accuracy of this explicit expression for a simple model that accounts for the effects of oxide- and interface-trapped charges.

Current-charge relation

The drain-to-source current still relies on the classical drift-diffusion transport model [96]

$$I_D = \mu_0 W \left(-Q_i \frac{d\Psi_s}{dx} + U_T \frac{dQ_i}{dx} \right), \tag{5.24}$$

where μ_0 is the low-field channel mobility that is assumed constant along the channel and x is the position along the channel from the source to the drain. Solving Eq. (5.8) for the surface potential and introducing it into Eq. (5.24) yields

$$I_D = \mu_0 W \left[\left(U_T - \frac{Q_i}{nC_{ox}} \right) \frac{dQ_i}{dx} - \frac{c_{it}}{n} Q_i \frac{dV_{ch}}{dx} \right], \tag{5.25}$$

which can be written in its normalized form

$$i_d \triangleq \frac{I_D}{I_{spec}} = -\left(1 + 2q_i\right) \frac{dq_i}{d\xi} + \frac{c_{it}}{n} q_i \frac{dv}{d\xi} \tag{5.26}$$

with $\xi \triangleq x/L$ describing the relative position along the channel from the source. In the presence of oxide- and interface-charge trapping, $I_{spec} \triangleq I_{spec_\square} W/L$ is still defined as the specific current with $I_{spec_\square} \triangleq 2n\mu_0 C_{ox} U_T^2$ defined as the specific current per square. Eq. (5.26) is almost identical to the original expression, i.e., Eq. (4.21) in [96], except for the additional last term representing the effect of interface-charge trapping.

To obtain a full charge expression of the current that can then be integrated in the charge domain as in the original EKV MOSFET model, a charge expression of the last term in Eq. (5.26) needs to be found. This can be done by differentiating Eq. (5.20) with respect to ξ:

$$\frac{dv}{d\xi} = -\frac{n}{n_0} \left(2 + \frac{1}{q_i} \right) \frac{dq_i}{d\xi}. \tag{5.27}$$

Introducing Eq. (5.27) into Eq. (5.26) results in a fully charge-based expression of the drain current that includes the effects of oxide- and interface-trapped charges

$$i_d = -\frac{n}{n_0} \left(1 + 2q_i\right) \frac{dq_i}{d\xi}. \tag{5.28}$$

The drain current is then simply obtained as in the original EKV MOSFET model by integrating

Eq. (5.28) from the source to the drain in the charge domain:

$$i_{\mathrm{d}} = \frac{n}{n_0}\left[q_{\mathrm{s}} + q_{\mathrm{s}}^2 - \left(q_{\mathrm{d}} + q_{\mathrm{d}}^2\right)\right]. \tag{5.29}$$

This equation is almost identical to the original expression, i.e., Eq. (4.4) [96], except for the additional scaling factor n/n_0 that accounts for the effects of interface-trapped charges. Here, q_{s} and q_{d} are linked to the terminal voltages through Eq. (5.20) by replacing q_{i} and v with q_{s} and v_{s} at the source and q_{d} and v_{d} at the drain. Thus, solving the corresponding expressions with Eq. (5.29) relates the drain current to the terminal voltages for a long-channel MOSFET.

Velocity saturation effect

The effect of VS is among the most important short-channel effects and has been included in the original EKV MOSFET model via the VS parameter λ_{c}, as explained in Section 4.1.1. In the absence of oxide and interface traps, Mangla has detailed the derivation of the VS model in [203] with both the drift and diffusion terms. The same derivation procedure is now carried out for incorporating defect-related effects into the original model equations.

The effective mobility μ_{eff}, which relates the drift velocity of free carriers v_{drift} to the combined effect of the longitudinal and vertical electric field E_{x}, is defined as

$$\mu_{\mathrm{eff}} \triangleq \frac{v_{\mathrm{drift}}(E_{\mathrm{x}})}{|E_{\mathrm{x}}|}, \tag{5.30}$$

as shown in Fig. 5.9a [96]. When the electrical field E_{x} reaches a critical value E_{c}, the carrier velocity v_{drift} saturates to a particular value v_{sat}, corresponding to

$$\mu_{\mathrm{z}} \triangleq \frac{v_{\mathrm{sat}}}{E_{\mathrm{c}}}. \tag{5.31}$$

Normalizing the carrier velocity v_{drift} and the electric field E_{x} respectively to v_{sat} and E_{c} yields

$$u_{\mathrm{eff}} \triangleq \frac{\mu_{\mathrm{eff}}}{\mu_{\mathrm{z}}} = \frac{\nu(e)}{e} = \begin{cases} 1 & \text{for } e < 1 \\ 1/e & \text{for } e \geq 1 \end{cases}, \tag{5.32}$$

where $e = |E_{\mathrm{x}}|/E_{\mathrm{c}}$ is the normalized electric field and $\nu(e) = v_{\mathrm{drift}}/v_{\mathrm{sat}}$ is the normalized carrier velocity. This modeling work uses the piecewise linear velocity-field model, which is illustrated by the blue lines in Fig. 5.9a [96]. Unlike the low-field channel mobility μ_0, μ_{z} increases with the vertical electrical field E_{z}, as seen in Fig. 5.9b from three solid lines corresponding to different values of E_{z} [96].

Since $|E_{\mathrm{x}}| = \mathrm{d}\Psi_{\mathrm{s}}/\mathrm{d}x$, the drift-diffusion transport expression Eq. (5.24) can be written as

$$I_{\mathrm{D}} = \mu_{\mathrm{eff}} Q_{\mathrm{i}} |E_{\mathrm{x}}| + \mu_{\mathrm{eff}} U_{\mathrm{T}} \frac{\mathrm{d}Q_{\mathrm{i}}}{\mathrm{d}x}, \tag{5.33}$$

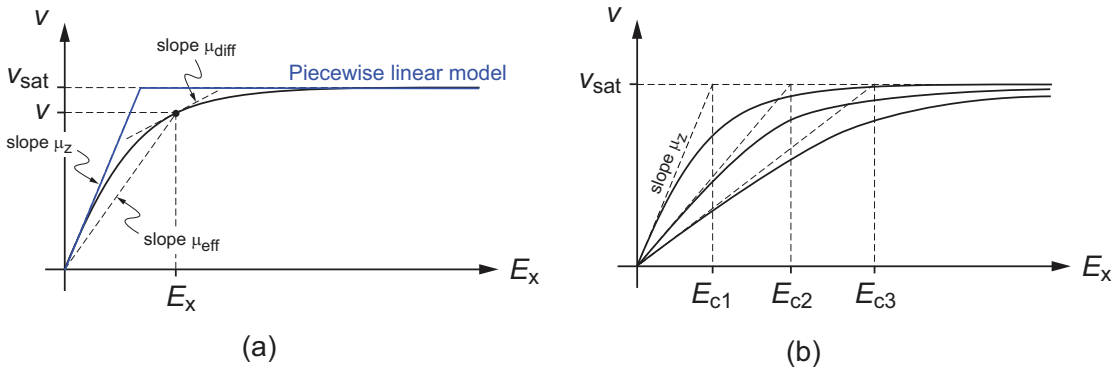


Figure 5.9 – (a) Definitions of the carrier mobility; (b) dependence of the carrier mobility μ_z on the vertical field E_z at a low longitudinal field. (After Enz [96].)

whose normalized form is given by

$$i_d = 2q_i \frac{ue}{\lambda_c} - u\frac{dq_i}{d\xi}. \tag{5.34}$$

Here, the term u refers to the effective mobility normalized to the low-field channel mobility as

$$u \triangleq \frac{\mu_{eff}}{\mu_0} = \frac{\mu_{eff}}{\mu_z}\frac{\mu_z}{\mu_0}. \tag{5.35}$$

Since the mobility reduction due to the vertical electric field is not considered at this stage of the modeling work, $\mu_z = \mu_0$ and $u = u_{eff}$. In a velocity saturated device, the condition at the drain end of the channel can now be described as

$$q_i = q_{dsat}, \tag{5.36a}$$

$$v = ue = 1, \tag{5.36b}$$

$$\frac{\partial q_i}{\partial \xi} = 0, \tag{5.36c}$$

with which Eq. (5.34) can be simplified to

$$i_{dsat} = \frac{2q_{dsat}}{\lambda_c}. \tag{5.37}$$

This equation is the same as the original expression that does not account for defect-related effects [113, 203].

Linking the $2e/\lambda_c$ term in Eq. (5.34) to $d\psi_s/d\xi$ through

$$\frac{2e}{\lambda_c} = \frac{E_c L}{U_T}\frac{|E_x|}{E_c} = \frac{L}{U_T}\frac{d\Psi_s}{dx} = \frac{d\Psi_s/U_T}{dx/L} = \frac{d\psi_s}{d\xi}, \tag{5.38}$$

solving the first-order derivative on both sides of Eq. (5.19) as

$$\frac{\mathrm{d}\psi_\mathrm{s}}{\mathrm{d}\xi} = \frac{c_\mathrm{it}}{n}\frac{\mathrm{d}v}{\mathrm{d}\xi} - 2\frac{\mathrm{d}q_\mathrm{i}}{\mathrm{d}\xi}, \tag{5.39}$$

and repeating the same procedure for Eq. (5.28) leads to an expression of the drain current flowing through the channel region where the carrier velocity does not saturate:

$$i_\mathrm{d} = -u\frac{n}{n_0}\left(1+2q_\mathrm{i}\right)\frac{\mathrm{d}q_\mathrm{i}}{\mathrm{d}\xi}. \tag{5.40}$$

Assuming that the longitudinal electric field remains smaller than the critical value at each point along the channel and the carrier velocity saturates right at the drain side, there is $u = 1$ throughout the channel from the source to the drain. Solving Eq. (5.40) as Eq. (5.28) and considering Eq. (5.36) leads to

$$i_\mathrm{dsat} = \frac{n}{n_0}\left[q_\mathrm{s} + q_\mathrm{s}^2 - \left(q_\mathrm{dsat} + q_\mathrm{dsat}^2\right)\right]. \tag{5.41}$$

The saturated inversion charge density at the drain end of the channel and the accordingly saturated drain current can now be solved in the normalized form from Eq. (5.37) and Eq. (5.41) as

$$q_\mathrm{dsat} = \frac{2\frac{n}{n_0}\lambda_\mathrm{c}\left(q_\mathrm{s}+q_\mathrm{s}^2\right)}{2+\frac{n}{n_0}\lambda_\mathrm{c}+\sqrt{4\left(1+\frac{n}{n_0}\lambda_\mathrm{c}\right)+(\frac{n}{n_0}\lambda_\mathrm{c})^2\left(1+2q_\mathrm{s}\right)^2}}, \tag{5.42a}$$

$$i_\mathrm{dsat} = \frac{4\frac{n}{n_0}\left(q_\mathrm{s}+q_\mathrm{s}^2\right)}{2+\frac{n}{n_0}\lambda_\mathrm{c}+\sqrt{4\left(1+\frac{n}{n_0}\lambda_\mathrm{c}\right)+(\frac{n}{n_0}\lambda_\mathrm{c})^2\left(1+2q_\mathrm{s}\right)^2}}, \tag{5.42b}$$

in which the scaling factor n/n_0 in front of the VS parameter and the inversion charge density at the source end of the channel represents the effects of interface-charge trapping.

Reverting Eq. (5.42b) gives an expression of the inversion charge density at the source end of the channel as a function of the saturated drain current:

$$q_\mathrm{s} = \frac{\sqrt{4\frac{n_0}{n}i_\mathrm{dsat}+\left(1+\lambda_\mathrm{c}i_\mathrm{dsat}\right)^2}-1}{2}. \tag{5.43}$$

To derive the current-voltage expression, it can be introduced into Eq. (5.20) for the source end of the channel:

$$\frac{n_0}{n}(v_\mathrm{p}-v_\mathrm{s}) = \sqrt{4\frac{n_0}{n}i_\mathrm{dsat}+\left(1+\lambda_\mathrm{c}i_\mathrm{dsat}\right)^2} + \ln\left[\sqrt{4\frac{n_0}{n}i_\mathrm{dsat}+\left(1+\lambda_\mathrm{c}i_\mathrm{dsat}\right)^2}-1\right] - (1+\ln 2), \tag{5.44}$$

which accounts for the effect of VS for a short-channel MOSFET.

Hence, the drain current in inversion region of saturation operation is modeled through the simple equation Eq. (5.44) with only five model parameters, i.e., the slope factor n_0 in the absence of interface-trapped charges, the slope factor n that accounts for the effect of interface-trapped charges, the specific current per square $I_{\mathrm{spec}_\square}$, the threshold voltage V_T, and the VS parameter λ_c. Setting $\lambda_\mathrm{c} = 0$ in Eq. (5.44) brings back the long-channel model, which is obtained through solving Eq. (5.20) and Eq. (5.29) at the source end of the channel.

Compared to the original expression, i.e., Eq. (4.14) [96], interface-charge trapping introduces a scaling factor $n_0/n = 1/(1+c_\mathrm{it}/n_0)$ in front of the normalized current i_dsat and the normalized saturation voltage $v_\mathrm{p} - v_\mathrm{s}$, in addition to the shifted threshold voltage and the degraded slope factor. Newly developed explicit expressions in the presence of oxide and interface traps are quite similar to their original counterparts and therefore maintain many properties of the original EKV MOSFET model.

Small-signal characteristics

The derivation of small-signal model equations has been partly presented in Section 4.1.1. Following the same procedure, the corresponding expressions that account for the effects of oxide- and interface-trapped charges are given below:

$$\frac{G_\mathrm{ms}}{G_\mathrm{spec}} = g_\mathrm{ms} = \frac{\sqrt{4\frac{n_0}{n} i_\mathrm{dsat} + (1+\lambda_\mathrm{c} i_\mathrm{dsat})^2} - 1}{2 + \frac{n}{n_0}\lambda_\mathrm{c}(1+\lambda_\mathrm{c} i_\mathrm{dsat})} \begin{cases} \text{weak inversion}: & g_\mathrm{ms} \approx \dfrac{n_0}{n} i_\mathrm{dsat}, \\ \text{strong inversion}: & g_\mathrm{ms} \approx \dfrac{i_\mathrm{dsat}}{\frac{n}{n_0}\lambda_\mathrm{c}}. \end{cases} \tag{5.45}$$

$$\frac{G_\mathrm{m} n U_\mathrm{T}}{I_\mathrm{D}} = \frac{\sqrt{4\frac{n_0}{n} i_\mathrm{dsat} + (1+\lambda_\mathrm{c} i_\mathrm{dsat})^2} - 1}{\left[2\frac{n_0}{n} + \lambda_\mathrm{c}(1+\lambda_\mathrm{c} i_\mathrm{dsat})\right] i_\mathrm{dsat}} \begin{cases} \text{weak inversion}: & \dfrac{G_\mathrm{m} n U_\mathrm{T}}{I_\mathrm{D}} \approx 1, \\ \text{strong inversion}: & \dfrac{G_\mathrm{m} n U_\mathrm{T}}{I_\mathrm{D}} \approx \dfrac{1}{\lambda_\mathrm{c} i_\mathrm{dsat}}. \end{cases} \tag{5.46}$$

$$\frac{G_\mathrm{ms}}{G_\mathrm{spec}} = g_\mathrm{ms} = \frac{\sqrt{1+4\frac{n_0}{n} i_\mathrm{d}} - 1}{2} \begin{cases} \text{weak inversion}: & g_\mathrm{ms} \approx \dfrac{n_0}{n} i_\mathrm{d}, \\ \text{strong inversion}: & g_\mathrm{ms} \approx \sqrt{\dfrac{n_0}{n} i_\mathrm{d}}. \end{cases} \tag{5.47}$$

$$\frac{G_\mathrm{m} n U_\mathrm{T}}{I_\mathrm{D}} = \frac{\sqrt{1+4\frac{n_0}{n} i_\mathrm{d}} - 1}{2\frac{n_0}{n} i_\mathrm{d}} \begin{cases} \text{weak inversion}: & \dfrac{G_\mathrm{m} n U_\mathrm{T}}{I_\mathrm{D}} \approx 1, \\ \text{strong inversion}: & \dfrac{G_\mathrm{m} n U_\mathrm{T}}{I_\mathrm{D}} \approx \dfrac{1}{\sqrt{\frac{n_0}{n} i_\mathrm{d}}}. \end{cases} \tag{5.48}$$

Eq. (5.45) and Eq. (5.46) account for the effect of VS on small-signal characteristics of short-channel MOSFETs, while Eq. (5.47) and Eq. (5.48) are the corresponding long-channel model

equations. Both sets of equations include the effects of oxide- and interface-charge trapping through the scaling factor n_0/n and the normalizing factor I_{spec}. Their strong and weak inversion asymptotes are also summarized here and should be updated accordingly when performing parameter extraction.

5.1.4 Model validation with wide-channel MOSFETs

The experimental investigation in Section 3.2 demonstrates that total ionizing radiation influences 28-nm bulk MOSFETs through radiation-induced oxide- and interface-charge trapping. Irradiation measurements can therefore be used for validating the newly developed generalized EKV MOSFET model, which in turn serves for a better understanding of the main experimental phenomena. To avoid the interfered effects of charge trapping related to different dielectric components, this step of model validation is conducted against wide-channel MOSFETs, whose degradation is mainly attributed to gate-oxide-related charge trapping.

Model parameters are extracted from measurements using an approach similar to that in Section 4.1.2 with updated asymptotes summarized in Section 5.1.3. The drain leakage current of 28-nm bulk *n*MOSFETs is a weak function of the gate-to-bulk voltage and modeled as a constant current flowing through a gateless charge-controlled device. For 28-nm bulk

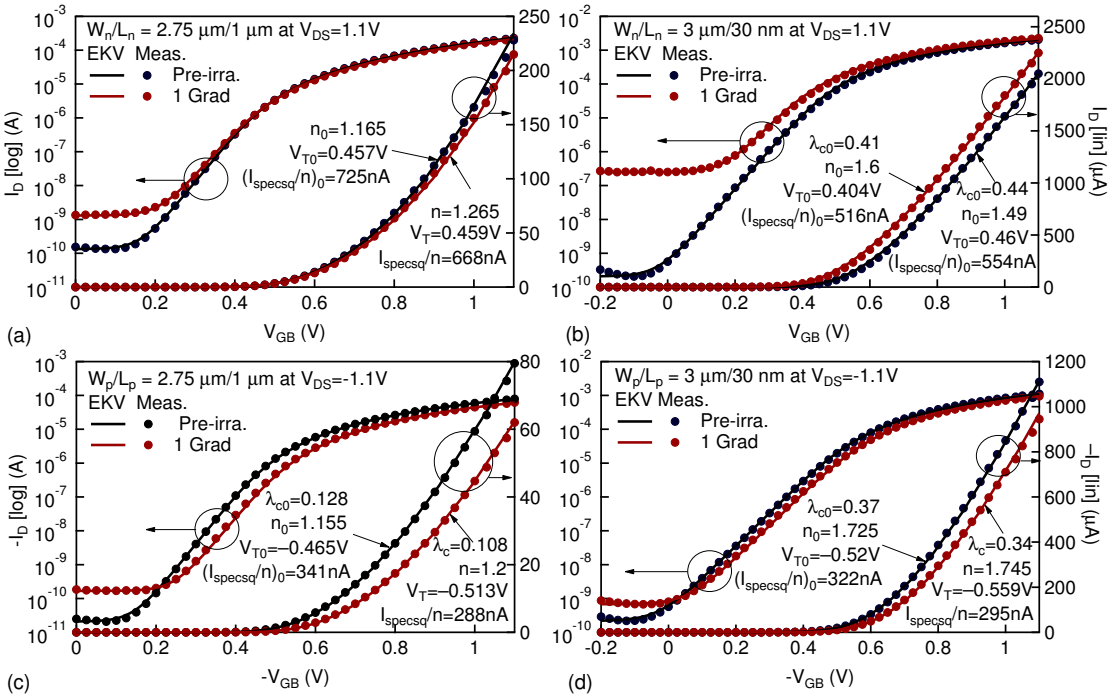


Figure 5.10 – Validation of the generalized EKV MOSFET model with the measured $|I_D| - |V_{GB}|$ curves in saturation operation ($|V_{DS}| = 1.1$V) of (a, c) long- and (b, d) short-channel (a, b) *n*- and (c, d) *p*MOSFETs corresponding to pre-radiation and 1 Grad of TID. (After Zhang, et al. [126].)

Table 5.1 – Parameters of the generalized EKV MOSFET model for wide-channel MOSFETs [126]

Device type	W (µm)	L (µm)	Δn	ΔV_T	N_{ot} (cm^{-2})	D_{it} ($cm^{-2}eV^{-1}$)
n	2.75	1	0.1	2	7.8×10^{11}	1.4×10^{12}
n	3	0.03	0.11	-56	9.1×10^{11}	1.6×10^{12}
p	2.75	1	0.045	-48	3.2×10^{11}	6.3×10^{11}
p	3	0.03	0.02	-39	3.9×10^{11}	2.8×10^{11}

pMOSFETs, the drain leakage current is believed to originate from the peripheral substrate-drain junction leakage and also weakly depends on the gate-to-bulk voltage. Therefore, for both n- and pMOSFETs, a constant leakage is added to the generalized EKV MOSFET model at each TID step for considering the effects of TID on the switched-off state.

With properly extracted parameters, the generalized EKV MOSFET model is compared to pre- and post-irradiation measurements of long- and short-channel n- and pMOSFETs in Fig. 5.10 [126]. Despite a small number of parameters, this newly developed model demonstrates an excellent agreement with measurement points in a broad range of device operation. The effects of TID are efficiently captured by ΔI_{Dleak} for the drain leakage current increase, $\Delta n = c_{it}$ for the subthreshold swing degradation, ΔV_T for the threshold voltage shift, and $(I_{spec_\square}/n)/(I_{spec_\square}/n)_0$ or λ_c/λ_{c0} for the low-field channel mobility reduction, whose values are partly listed in Table 5.1 [126].

Explicit expressions of model parameters provide an efficient approach for the extraction of the densities of oxide- and interface-trapped charges at each TID step, which serve for the modeling work of introducing device scalability in Section 5.3. Oxide and interface-trapped charges are assumed negligible in fresh 28-nm bulk MOSFETs. According to the definition of the slope factor in Eq. (5.10), the interface-trap density can be extracted from the slope factor increase as

$$D_{it} = \frac{c_{it}C_{ox}}{q^2} = \frac{\Delta n C_{ox}}{q^2}. \tag{5.49}$$

Since $\Psi_0 = 2\Phi_F + 2.8U_T$ for this 28-nm CMOS process, the threshold voltage shift defined in Eq. (5.22) can be expressed as

$$\Delta V_{Tn} = \underbrace{\frac{q^2 D_{it}}{C_{ox}}(\Phi_F + 2.8U_T)}_{\Delta V_{it}} \underbrace{-\frac{qN_{ot}}{C_{ox}}}_{\Delta V_{ot}}, \tag{5.50a}$$

$$\Delta V_{Tp} = \underbrace{-\frac{q^2 D_{it}}{C_{ox}}(\Phi_F + 2.8U_T)}_{\Delta V_{it}} \underbrace{-\frac{qN_{ot}}{C_{ox}}}_{\Delta V_{ot}}. \tag{5.50b}$$

Eq. (5.50a) and Eq. (5.50b) correspond to n- and pMOSFETs, respectively. The slope factor increase Δn or the interface-trap density D_{it} enables us to calculate the threshold voltage shift due to interface-trapped charges ΔV_{it}. Deducting it from the total threshold voltage shift

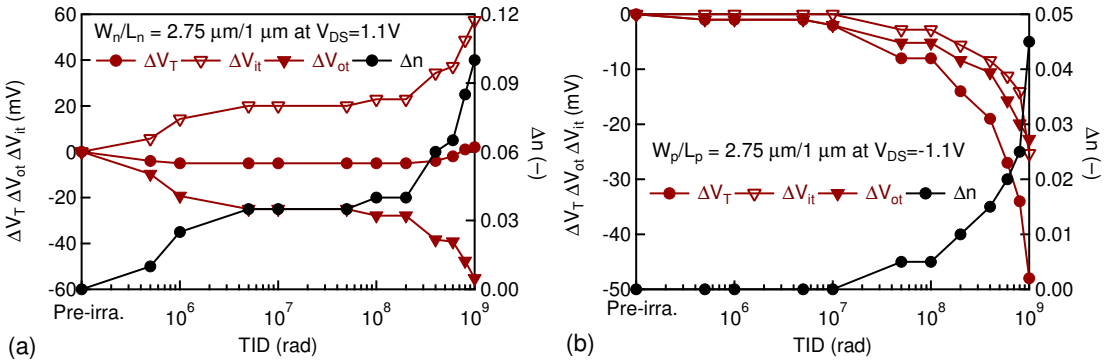


Figure 5.11 – Threshold voltage shift ΔV_T (on the left axis) and slope factor increase Δn (on the right axis) with respect to TID for a long-channel MOSFET of (a) *n*- and (b) *p*-types. (After Zhang, et al. [126].)

ΔV_T gives the contribution of oxide-trapped charges ΔV_{ot}, from which the oxide-trap density N_{ot} can be extracted. The oxide- and interface-trap densities extracted from long-channel MOSFETs, as shown in Table 5.1, are within the range reported in the literature [209, 213]. For short-channel *n*MOSFETs, the oxide-trapped charge density should be extracted after removing the influence of the radiation-enhanced DIBL effect. This will be accounted for later in this section when using this generalized EKV MOSFET model for a comprehensive discussion of the observed radiation effects.

Fig. 5.11 plots the slope factor increase Δn and the threshold voltage shift ΔV_T with respect to TID for long-channel MOSFETs, indicating radiation-induced oxide- and interface-charge trapping [126]. For the long-channel *n*MOSFET, the threshold voltage first decreases and then increases, suggesting the counterbalancing effect of oxide- and interface-trapped charges. Even though the ultimate threshold voltage shift is small, the extracted oxide- ($7.8 \times 10^{11}\,\mathrm{cm}^{-2}$) and interface-trap densities ($1.4 \times 10^{12}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$) still imply the effects of TID-induced charge

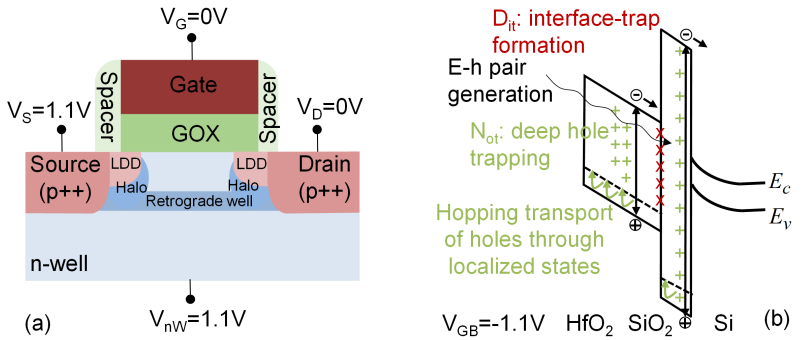


Figure 5.12 – (a) Cross section of a high-κ *p*MOSFET along the channel width and (b) its schematic illustration of TID-induced charge trapping under the diode condition. (Zhang, et al. [127].)

trapping. The long-channel *p*MOSFET has a smaller oxide-trap density ($3.2 \times 10^{11}\,\mathrm{cm}^{-2}$) and a moderate interface-trap density ($6.3 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$). However, due to the accumulated effect of oxide- and interface-trapped charges, its threshold voltage shift is still high.

Both Table 5.1 and Fig. 5.11 present a smaller slope factor increase for *p*MOSFETs. This is probably a result of the negative gate bias during irradiation. According to the basic processes explained in Section 2.2, Fig. 5.12 illustrates TID-induced charge generation and evolution in a 28-nm bulk high-κ *p*MOSFET under the diode condition ($V_G = V_D = 0\,V$ and $V_S = V_{nW} = 1.1\,V$) [127]. When $V_{GB} = -1.1\,V$, positive protons in both SiO_2 and HfO_2 transport away from the semiconductor/oxide interface towards the gate electrode. Their chance to react with H-passivated interface traps close to the surface channel is very low, leading to a slight influence on the subthreshold swing. Though positive protons may get trapped at the interface of SiO_2 and HfO_2, influencing device behaviors to a certain extent.

5.1.5 Main observations about model parameters

This generalized EKV MOSFET model including defect-related effects has demonstrated its capability of capturing the effects of TID up to 1 Grad on wide-channel 28-nm bulk MOSFETs. It is now applied to investigate TID effects on various sizes of 28-nm bulk MOSFETs and to provide insights into where to improve for a comprehensive radiation-aware compact model.

Parameter extraction

Based on previous observations, such as 1) the considerable influence in the subthreshold region or reduced bias points in inversion due to the TID-induced drain leakage current increase and 2) the correlation of the VS parameter and the specific current through the low-field channel mobility, special care is taken for extracting model parameters more precisely and efficiently. The parameter extraction relies on fitting Eq. (5.44) with measured data using a nonlinear least-squares solver in Matlab. Fig. 5.14 summarizes the extraction procedure, including pre-processing of raw data, optimization of initial guesses, curve fitting with the nonlinear least-squares solver, and extraction finalization with the normalized transconductance efficiency [127]. Each step with the corresponding purpose is explained as follows.

The TID-induced drain leakage current increase ΔI_{Dleak} of 28-nm bulk MOSFETs is dominated by external leakage components and is modeled as a V_{GB}-independent constant. For a switched-on device, this leakage is considered negligible compared to the main channel current I_{Dmain}. However, for some MOSFETs, such as the smallest *n*MOSFET (Fig. 3.8d) and the narrow/long-channel *p*MOSFET (Fig. 3.8g), the significant drain leakage current increase interferes device operation in weak inversion and covers the real evolution of some parameters. To ensure a higher extraction accuracy and obtain information close to the real case, the drain leakage current I_{Dleak} is first carefully extracted and its increase ΔI_{Dleak} is then removed from all measurement points, as illustrated in Fig. 5.13a. Since ΔI_{Dleak} comes from the parasitic

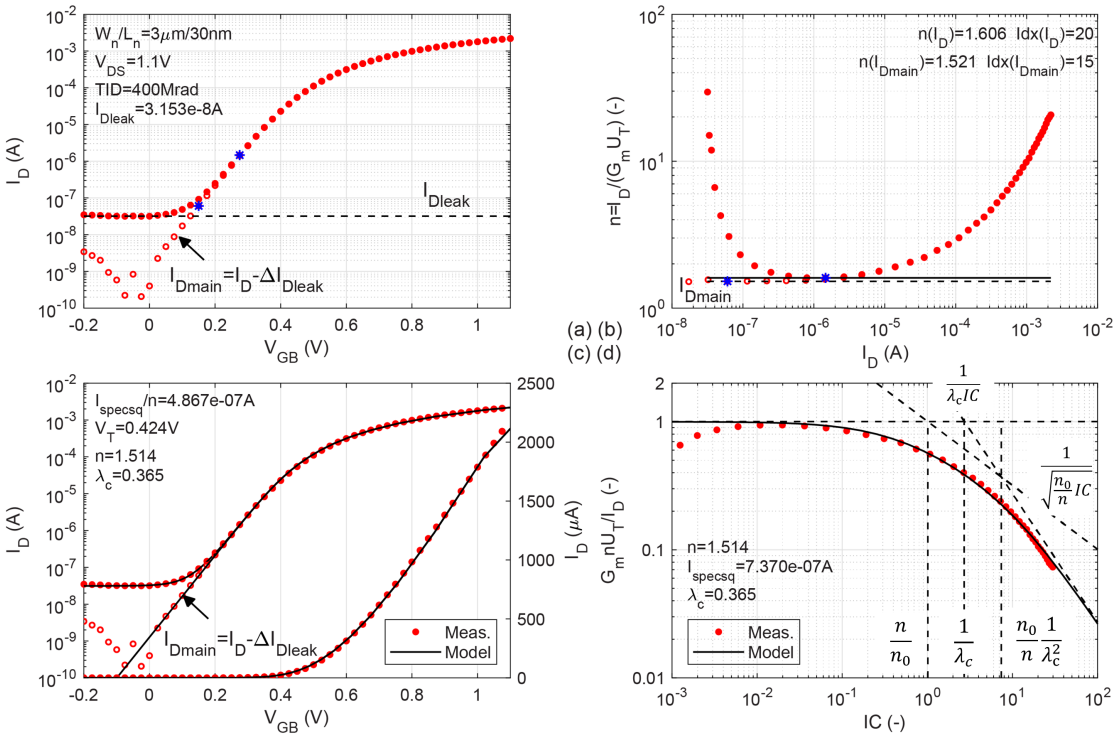


Figure 5.13 – Parameter extraction with the generalized EKV MOSFET model using an *n*MOSFET as an example. (Zhang, et al. [127].)

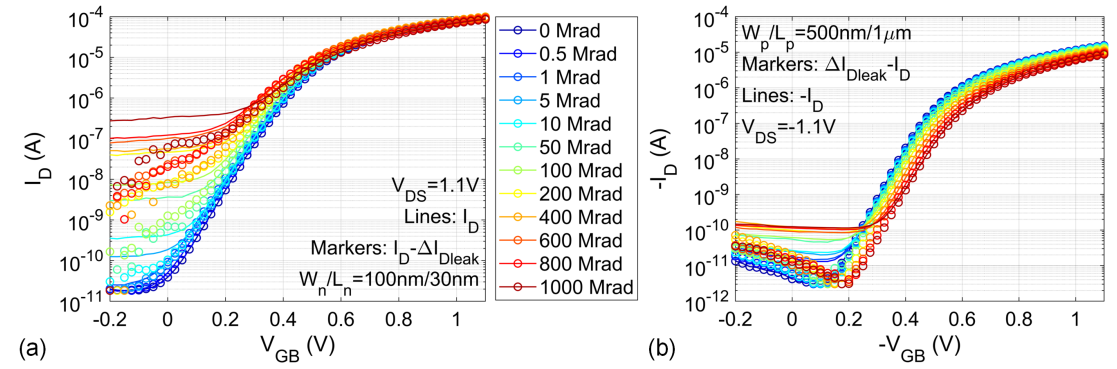


Figure 5.14 – Measured $|I_D|$ and calculated $|I_D - \Delta I_{Dleak}|$ versus $|V_{GB}|$ curves of (a) an *n*MOSFET and (b) a *p*MOSFET, showing the influence of the drain leakage current increase on device performance.

channels or the reversely biased drain-substrate junction, removing ΔI_{Dleak} from I_D brings the switched-off region almost back to the pre-irradiation condition, as shown in Fig. 5.14. The remaining V_{GB}-dependent leakage of some *n*MOSFETs is due to the crude assumption of the V_{GB}-independent parasitic leakage current, despite that the parasitic channel may spread across the whole depth of the STI sidewall with a gradually fading gate control from the surface channel to the bottom of the STI oxide.

Curve fitting with the nonlinear least-squares solver requires appropriate initial guesses and bound limits for all parameters. The extraction of EKV model parameters starts with pre-irradiation measurement results. Once the initial guess of the pre-irradiation slope factor is obtained from the $I_D/(G_m U_T) - I_D$ curve in weak inversion (Fig. 5.13b), the measured data is then fed into the nonlinear least-squares solver for extracting n_0, $I_{spec\square 0}$, λ_{c0}, and V_{T0} (Fig. 5.13c). The drain leakage current increase ΔI_{Dleak0} is added back after extracting all other parameters. Extracted parameters are eventually evaluated with the normalized transconductance efficiency using those updated asymptotes in Fig. 5.13d. From now on, each irradiation step takes the extracted values from the previous step as initial guesses and bound limits are set carefully for model parameters to evolve in a reasonable direction.

Intercorrelations among some parameters are also considered when setting initial guesses and bound limits. For example, instead of using $I_{spec\square}$ that is a function of both n and μ_0, the parameter extraction applies

$$\frac{I_{spec\square}}{n} = 2\mu_0 C_{ox} U_T^2 \tag{5.51}$$

for separately guiding their evolution. Since both $I_{spec\square}/n$ and λ_c are related to the low-field channel mobility, their ratio

$$\frac{I_{spec\square}}{n\lambda_c} = C_{ox} U_T v_{sat} L \tag{5.52}$$

is maintained constant at the pre-irradiation value. Thus, all μ_0-related parameters can be extracted through the extraction of the low-field channel mobility at the same time.

TID effects on trap-linked parameters

The slope factor increase and the threshold voltage shift allow us to extract the oxide- and interface-trapped charge densities, which in turn help us comprehend the observed radiation effects and facilitate the future model extension to more device dimensions. To serve for the next step of the modeling work, it is important to ensure the extraction accuracy of the slope factor and the threshold voltage. Fig. 5.15 summarizes the shift of these two parameters for four corner n- and pMOSFETs with respect to TID up to 1 Grad [127]. As compared to Fig. 3.13c, Fig. 3.11b, Fig. 3.15c, and Fig. 3.12b correspondingly, both parameters evolve as the individually extracted subthreshold swing and threshold voltage but showing slightly different values. From Fig. 5.15c, it is clearer to see the negligible slope factor increase of short-channel pMOSFETs, as explained through Fig. 5.12.

TID-induced low-field channel mobility reduction

Radiation-induced interfacial charges can act as Coulomb scattering centers and affect the motion of carriers in the conductive channel [153, 206], degrading the low-field channel

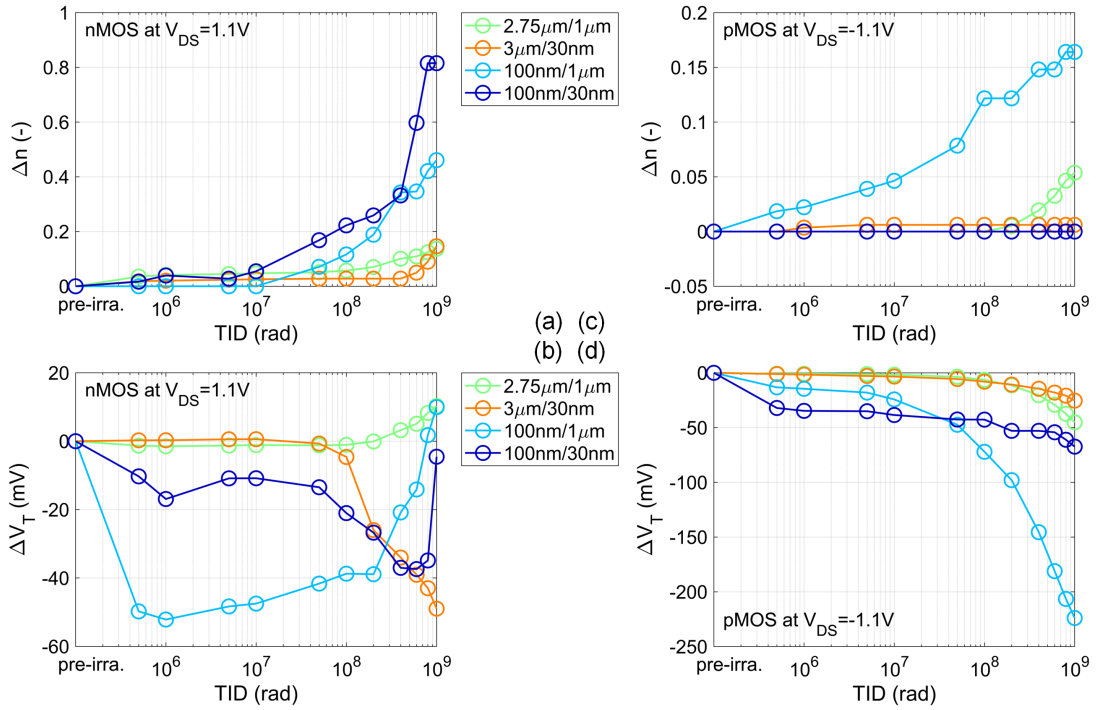


Figure 5.15 – Extracted (a, c) slope factor increase Δn and (b, d) threshold voltage shift ΔV_{T} of four corner (a, b) *n*- and (c, d) *p*MOSFETs using the generalized EKV MOSFET model. (Zhang, et al. [127].)

mobility. Oxide bulk traps lie further away from the inversion layer, whose influence on the low-field channel mobility is considered negligible compared to that of interfacial traps. As explained in Section 5.1.1, border traps have been lumped into interface traps when deriving the generalized EKV MOSFET model. Following the Sun-Plummer mobility reduction model [214], the effective low-field channel mobility μ_0 is simply related to the buildup of interface-trapped charges through the equation

$$\mu_0 \triangleq \frac{\mu_{00}}{1+\alpha_{\mathrm{it}} D_{\mathrm{it}}}, \tag{5.53}$$

where μ_{00} is the low-field channel mobility without the influence of interface-trapped charges and α_{it} is the radiation-induced mobility reduction parameter. This simple mobility model has also been applied by Fleetwood et al. to develop a dual-transistor model, which features midgap and mobility charge-separation analysis of identically processed *n*- and *p*MOSFETs, for evaluating the radiation response of MOSFETs.

For each MOSFET, this newly introduced parameter α_{it} should be constant throughout all TID levels. Based on the parameter definition, D_{it} and μ_0 can be extracted from each set of n and $I_{\mathrm{spec}_\square}$. These two parameters can be then introduced into Eq. (5.53) for calculating α_{it}. The calculated α_{it} demonstrates a TID independence in Fig. 5.16a, as expected. Its constant value

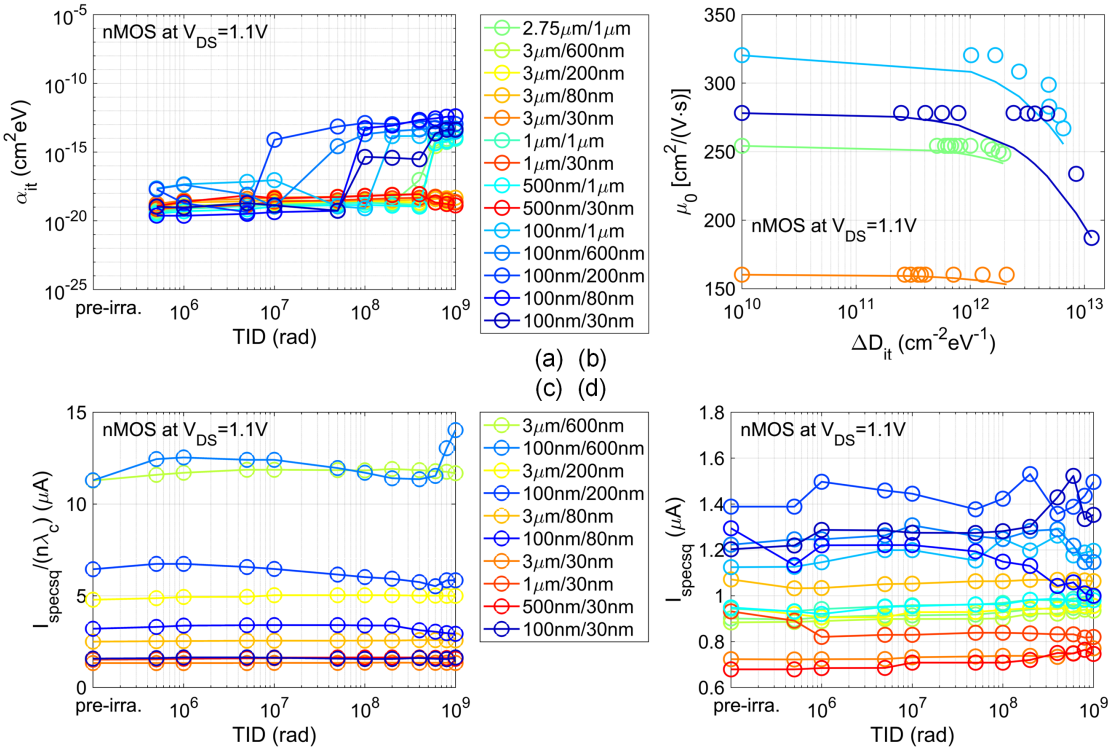


Figure 5.16 – TID-induced evolution of mobility-related parameters of 28-nm bulk MOSFETs: (a) calculated radiation-induced mobility reduction parameter α_{it}; (b) α_{it} extraction through fitting the mobility reduction model with the extracted μ_0; (c) calculated $I_{spec_\square}/(n\lambda_c)$; (d) extracted $I_{spec_\square}$. (Zhang, et al. [127].)

for narrow-channel *n*MOSFETs at high TID levels is $\sim 1 \times 10^{-13}$ cm^{2}eV, which falls within the range reported in the literature [173, 215]. Its much lower value for narrow-channel *n*MOSFETs at low TID levels and wide-channel *n*MOSFETs throughout all TID levels is probably due to the less accurate extraction from the slight mobility variation. To obtain a constant α_{it} for each MOSFET, Eq. (5.53) is applied to fit the extracted μ_0, as illustrated in Fig. 5.16b. The mobility reduction model with the obtained α_{it} can be then introduced back to model the specific current per square $I_{spec_\square}$ and the VS parameter λ_c.

When not fixing $I_{spec_\square}/(n\lambda_c)$ across different TID levels, this term can be calculated from extracted values of two μ_0-related parameters, i.e., $I_{spec_\square}/n$ and λ_c. As shown in Fig. 5.16c, it is almost constant for each *n*MOSFET with slight fluctuations, indicating the proportional relation of these two parameters and confirming our procedure of setting it to be constant. Since interface-trapped charges increase the slope factor and degrade the low-field channel mobility, the specific current per square $I_{spec_\square}$ falls around average values and does not show a unidirectional variation, as observed from Fig. 5.16d. This behavior of $I_{spec_\square}$ is implemented later directly into the parameter extraction procedure for linking different parameters, as explained in Section 5.2.

TID-induced effective channel width reduction

Narrow-channel *p*MOSFETs demonstrate a dramatic drive current loss (Fig. 3.12a) partly due to a significant threshold voltage shift (Fig. 3.12b). They also present a significant reduction in the peak transconductance (Fig. 3.12d), which however does not necessarily link to a low-field channel mobility reduction in consideration of the slight subthreshold swing degradation. As described qualitatively in Section 3.3.2, this serious performance degradation is mainly a result of an effective channel width reduction in addition to the considerable threshold voltage

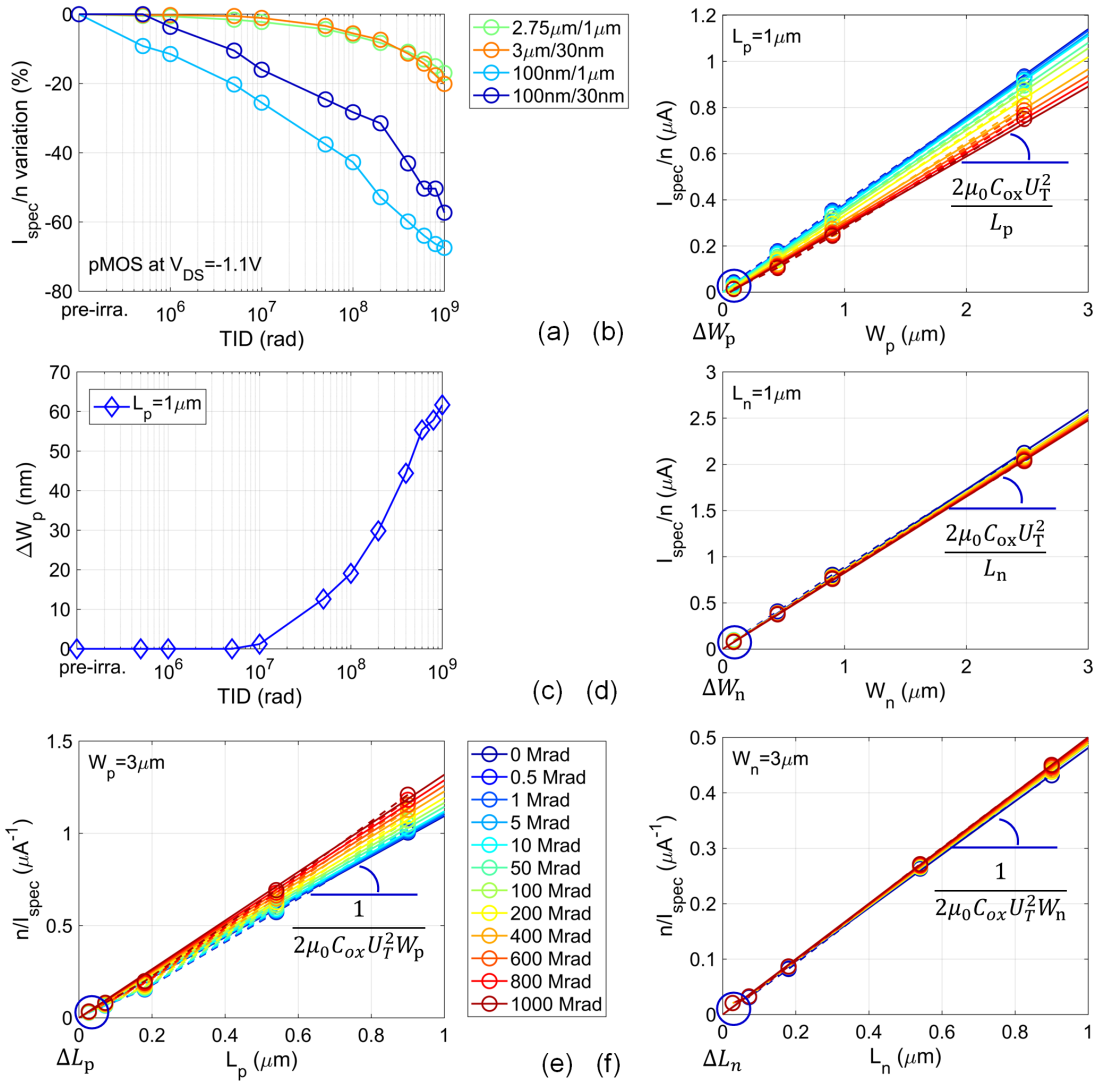


Figure 5.17 – TID-induced evolution of geometry-related model parameters: (a) I_{spec}/n variation; (b) extraction of the reduced channel width ΔW_{p} by a linear fit of I_{spec}/n versus the channel width W_{p}; (c) extracted ΔW_{p} versus TID; (d) ΔW_{n} extraction by a linear fit of I_{spec}/n versus the channel width W_{n}; (e, f) extraction of the reduced channel length ΔL by a linear fit of n/I_{spec} versus the channel length L. (Zhang, et al. [127].)

shift. From the design perspective, the following analysis aims at a quantitative evaluation of the effective channel width reduction in *p*MOSFETs, as summarized in Fig. 5.17 [127].

Instead of using the dimensionless term $I_{\mathrm{spec}_\square}/n$, the following analysis involves a geometry-dependent term I_{spec}/n. This term of narrow-channel *p*MOSFETs displays a significant variation by more than 50% in Fig. 5.17a, which is consistent with the considerable drive current loss. To gain insights about the relative contribution of the effective channel width reduction, we first consider the I_{spec}/n term of long-channel *p*MOSFETs, for which we can neglect possible effects on the channel length. Introducing a new parameter for the reduced channel width ΔW, the I_{spec}/n term can be expressed as

$$\frac{I_{\mathrm{spec}}}{n} = 2\mu_0 C_{\mathrm{ox}} U_{\mathrm{T}}^2 \frac{W_{\mathrm{eff}}}{L} = 2\mu_0 C_{\mathrm{ox}} U_{\mathrm{T}}^2 \frac{W-\Delta W}{L}. \tag{5.54}$$

When plotting it versus the channel width W, its intersection on the horizontal axis represents the reduced channel width ΔW and its slope provides insights about the low-field channel mobility μ_0, as illustrated in Fig. 5.17b. To extract ΔW, this equation is applied to fit the extracted I_{spec}/n of long-channel *p*MOSFETs versus the channel width W. As shown in Fig. 5.17c, the reduced channel width ΔW eventually goes up to 60 nm for long-channel *p*MOSFETs. This is more than half of the total channel width of the narrowest-channel *p*MOSFETs, explaining their dramatic I_{spec}/n variation. To better simulate the radiation response of narrow-channel *p*MOSFETs, it is therefore of great interest to introduce this effect into the generalized EKV MOSFET model.

The same approach can be applied to evaluate the effective channel width of *n*MOSFETs. As observed from Fig. 5.17d, the $I_{\mathrm{spec}}/n - W_{\mathrm{n}}$ curves do not show an obvious change in the horizontal intersection. The effective channel width of *n*MOSFETs is believed to remain constant at the nominal value. Inverting the term I_{spec}/n gives an expression of n/I_{spec}:

$$\frac{n}{I_{\mathrm{spec}}} = \frac{1}{2\mu_0 C_{\mathrm{ox}} U_{\mathrm{T}}^2} \frac{L_{\mathrm{eff}}}{W} = \frac{1}{2\mu_0 C_{\mathrm{ox}} U_{\mathrm{T}}^2} \frac{L-\Delta L}{W}, \tag{5.55}$$

which can be used similarly for evaluating the effective channel length of irradiated MOSFETs. The n/I_{spec}-related analysis with wide-channel MOSFETs is illustrated in Fig. 5.17e and Fig. 5.17f. Total ionizing radiation does not influence the effective channel length of 28-nm bulk MOSFETs as 65-nm bulk MOSFETs, suggesting again the insignificant influence of spacer-related charge trapping.

5.2 Design-oriented compact modeling of TID effects

5.2.1 A radiation-aware design-oriented compact model

The generalized EKV MOSFET model captures the slope factor increase Δn through Q_{it} and the threshold voltage shift ΔV_{T} via Q_{ot} and Q_{it}. Both the specific current per square divided

by the slope factor $I_{\mathrm{spec}\square}/n$ and the VS parameter λ_{c} are related to the low-field channel mobility μ_0. TID-induced mobility degradation is modeled through an additional curve fitting with already extracted parameters, which introduces discrepancies between model results and measurements of MOSFETs of typical dimensions. Besides, the I_{spec}/n term provides a quantitative method of extracting the effective channel width. However, this approach relies on an assumption of the same low-field channel mobility and provides an average channel width reduction for MOSFETs of the same length. Due to the channel-width-dependent effects, MOSFETs of the same length but different widths may have different values of the low-field channel mobility and the reduced channel width. To comprehensively model the effects of TID on 28-nm bulk MOSFETs, it is proposed to account for these two additional effects directly during parameter extraction.

The effective channel width reduction is simply modeled through an additional parameter ΔW that characterizes the portion of the reduced channel width. Introducing the effective channel width

$$W_{\mathrm{eff}} \triangleq W - \Delta W, \tag{5.56}$$

directly into the parameter extractor allows us to extract ΔW together with all other parameters. This parameter is only added for *p*MOSFETs, which suffer the significant effect of the radiation-induced effective channel width reduction.

We now model the TID-induced mobility reduction. Introducing Eq. (5.10) and Eq. (5.53) into the definition of the specific current per square leads to

$$I_{\mathrm{spec}\square} = 2\left(n_0 + \frac{q^2}{C_{\mathrm{ox}}} D_{\mathrm{it}}\right) \frac{\mu_{00}}{1+\alpha_{\mathrm{it}} D_{\mathrm{it}}} C_{\mathrm{ox}} U_{\mathrm{T}}^2 = I_{\mathrm{spec}\square 0}\left(1 + \frac{q^2}{n_0 C_{\mathrm{ox}}} D_{\mathrm{it}}\right) \frac{1}{1+\alpha_{\mathrm{it}} D_{\mathrm{it}}}. \tag{5.57}$$

Since $I_{\mathrm{spec}\square}$ remains almost constant throughout all TID levels, as shown in Fig. 5.16, it is worth setting

$$\alpha_{\mathrm{it}} \triangleq \frac{q^2}{n_0 C_{\mathrm{ox}}}. \tag{5.58}$$

Thus, TID-induced mobility degradation is simply modeled with Eq. (5.53) through relating the mobility reduction parameter α_{it} to the pre-irradiation slope factor n_0, extracting the low-field channel mobility μ_{00} from the pre-irradiation specific current per square $I_{\mathrm{spec}\square 0}$, and obtaining the interface-trap density D_{it} from the slope factor increase Δn. When Eq. (5.53) is complete with the extraction of these three parameters, all μ_0-related parameters can be modeled accordingly.

By now, all crucial effects of TID on 28-nm bulk MOSFETs have been considered, including 1) the drain leakage current increase $\Delta I_{\mathrm{Dleak}}$, 2) the radiation-enhanced DIBL effect $\Delta\alpha_{\mathrm{dibl}}$, 3) the effective channel width reduction ΔW, 4) the subthreshold swing degradation $\Delta n U_{\mathrm{T}} \ln(10)$, 5) the threshold voltage shift ΔV_{T}, and 6) the low-field channel mobility reduction through

Eq. (5.53). Except for $\Delta I_{\mathrm{Dleak}}$, $\Delta\alpha_{\mathrm{dibl}}$, ΔW, the effects of TID on all other parameters can be modeled as a function of D_{it} and N_{ot}. With five more parameters than the original EKV MOSFET model, this design-oriented compact model comprehensively accounts for the effects of TID on 28-nm bulk MOSFETs and provides an efficient approach for predicting their radiation response.

With proper initial guesses and bound limits, all model parameters can be extracted together through the parameter extractor programmed in the Matlab environment. To complete the analysis of TID effects on design parameters, Fig. 5.18 summarizes the extraction of parameters related to newly introduced models for the low-field channel mobility and the effective channel width [127]. The reduced channel width of four corner *p*MOSFETs plotted in Fig. 5.18a is consistent with their initial threshold voltage or equivalently their average channel doping concentration, as compared to Fig. 3.29. Narrow- or short-channel *p*MOSFETs have a smaller channel width reduction than wide- or long-channel ones. However, due to RINCE, narrow-channel *p*MOSFETs demonstrate a higher percentage of channel width reduction, as shown in Fig. 5.18b, corresponding to their dramatic drive current loss. Fig. 5.18c and Fig. 5.18d present the TID-induced evolution of the low-field channel mobility. The modeled and extracted values of the low-field channel mobility are equal since the parameter extraction is forced to respect the mobility reduction model.

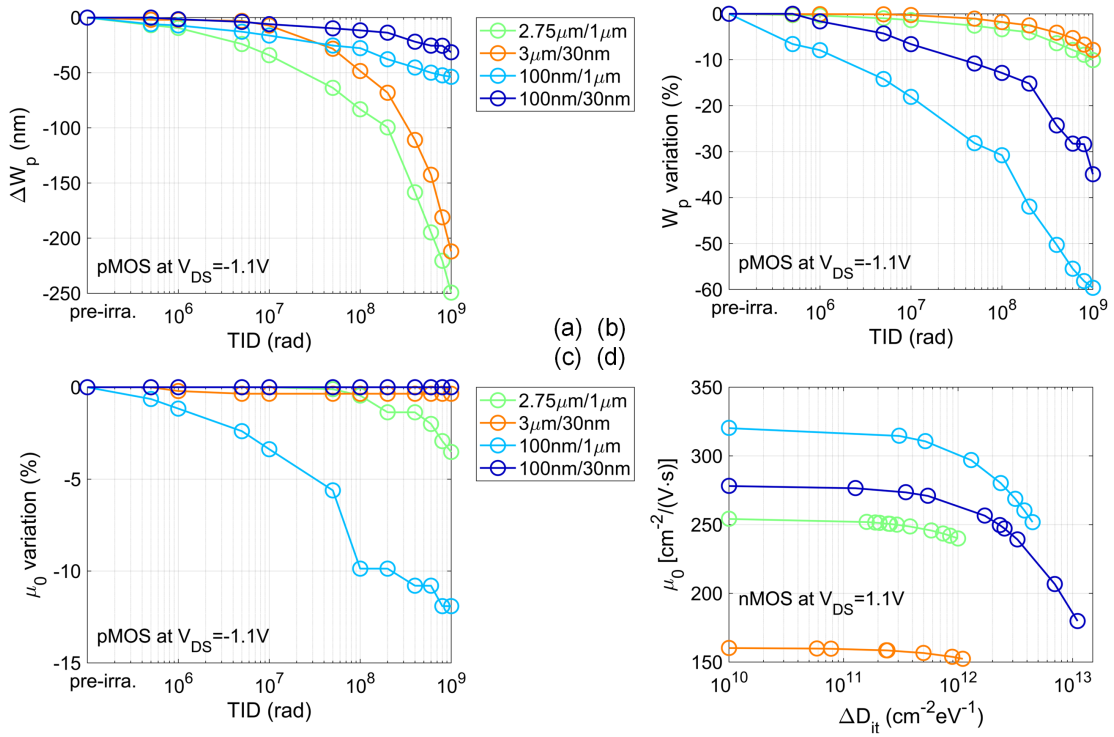


Figure 5.18 – Extraction of (a, b) the reduced channel width ΔW_{p} of *p*MOSFETs and (c, d) the low-field channel mobility μ_0 of both *n*- and *p*MOSFETs using the design-oriented compact model. (Zhang, et al. [127].)

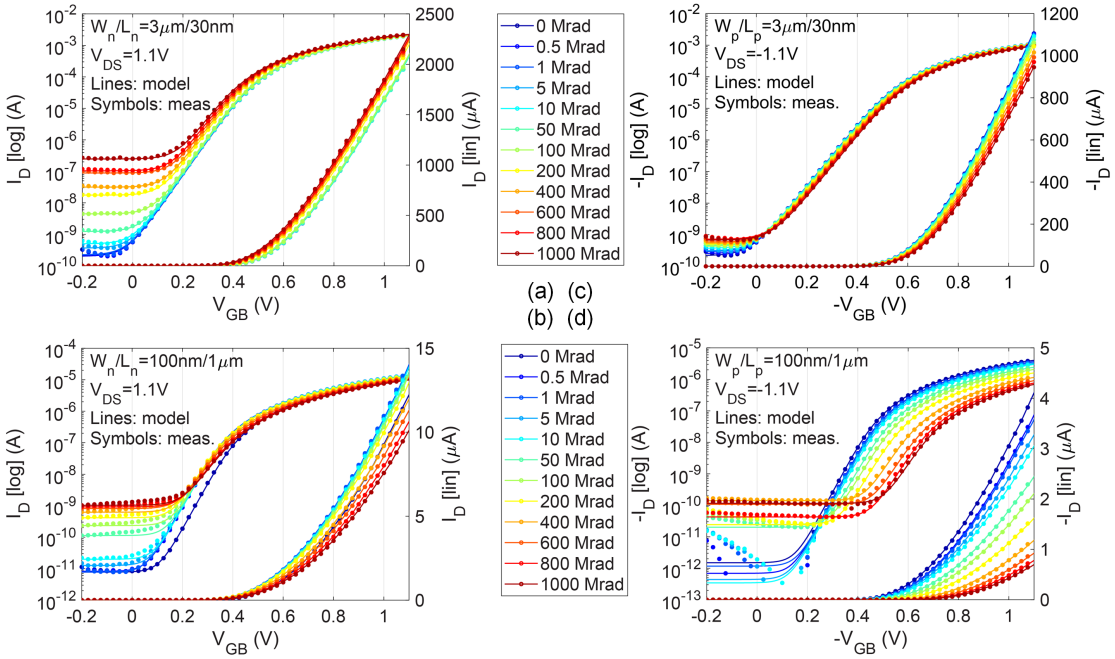


Figure 5.19 – Validation of the design-oriented compact model with the measured $|I_D| - |V_{GB}|$ curves of two corner (a, b) *n*- and (c, d) *p*MOSFETs with respect to TID up to 1 Grad. (Zhang, et al. [127].)

5.2.2 TID effects on large-signal characteristics

This radiation-aware design-oriented compact model is compared to the measured transfer characteristics of 28-nm bulk MOSFETs. Fig. 5.19 demonstrates an excellent match between the model and measurement results for TID levels up to 1 Grad in the whole operation range of wide/short- and narrow/long-channel *n*- and *p*MOSFETs [127]. With five more parameters that are introduced for modeling the observed radiation effects, the proposed model demonstrates its capability of fully capturing this 28-nm bulk CMOS process and predicting the radiation response of 28-nm bulk MOSFETs. This simple compact model can be promising for radiation-tolerant circuit design with this low-power high-performance CMOS process.

5.2.3 TID effects on small-signal characteristics

The transconductance and the transconductance efficiency are two important parameters for low-power analog and RF IC design and have been well considered in EKV charge-based MOSFET models. In the presence of oxide- and interface-trapped charges, their expressions in the normalized form have been derived using an approach similar to that for the original EKV MOSFET model and summarized in Section 5.1.3 with their updated asymptotes. The newly developed small-signal model includes an additional scaling factor that represents the influence of interface-trapped charges and appears in some asymptotes.

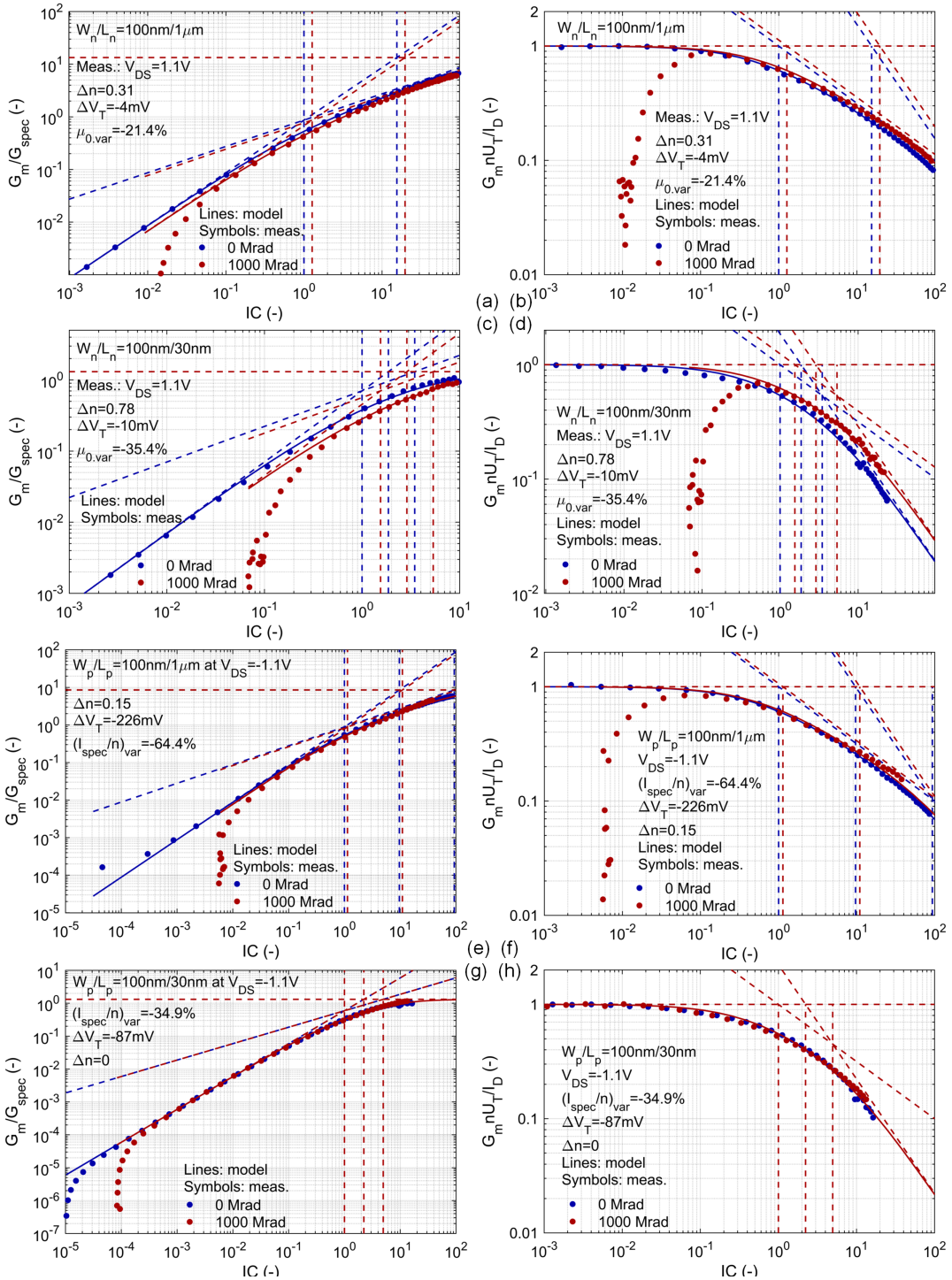


Figure 5.20 – Modeled and measured results of (a, c, e, g) the normalized transconductance G_m/G_{spec} and (b, d, f, h) the normalized transconductance efficiency $G_m nU_T/I_D$ of narrow-channel (a-d) *n*- and (e-h) *p*MOSFETs with respect to pre-irradiation and 1 Grad of TID. (Zhang, et al. [127].)

Since wide-channel MOSFETs show a slight slope factor increase, their small-signal characteristics in the normalized form remain almost unchanged after irradiation. Whether or not accounting for the influence of interface-trapped charges will not make a big difference in the normalized form of the smalls-signal model. Therefore, Fig. 4.5 that corresponds to the original EKV MOSFET model can still be referred to for evaluating TID effects on small-signal characteristics of wide-channel MOSFETs.

The validation of the newly developed small-signal model is therefore conducted only with measurement results of narrow-channel MOSFETs that have a higher slope factor increase. As shown in Fig. 5.20, model results match the measurements very well in the operation region of interest [127]. The shifting behavior of asymptotes and intercepts corresponds to the Q_{it}-induced scaling factor. As a result of the TID-induced drain leakage current increase, most narrow-channel MOSFETs demonstrate a serious degradation in weak inversion of their small-signal characteristics. When performing circuit design using this 28-nm bulk CMOS process, the influence of the drain leakage current increase should be carefully evaluated.

5.3 Scalability of the radiation-aware MOSFET model

Through the slope factor increase and the threshold voltage shift, the densities of oxide- and interface-trapped charges can be extracted for each MOSFET at each TID step. Some *n*MOSFETs demonstrate a radiation-enhanced DIBL effect, as shown in Fig. 3.13d, which is removed before the extraction of the oxide-trapped charge density. Fig. 5.21a and Fig. 5.21b respectively plot the TID-induced evolution of the interface- and oxide-trap densities extracted from wide- and narrow-channel *n*MOSFETs [127]. This design-oriented compact model demonstrates a width dependence of TID-induced trapped charges in 28-nm bulk MOSFETs, indicating the dominant influence of STI-related charge trapping and the unproblematic impact of gate-related charge buildup. MOSFETs of the same width have their charge-radiation curves almost overlapping each other, suggesting the possibility of finding an average charge-radiation curve for the same width of MOSFETs.

The total number of interface and oxide traps over the gate area, i.e., $D_{\mathrm{it}}WL$ and $N_{\mathrm{ot}}WL$, is now investigated as a function of the channel width. This brings interesting information about TID-induced charge contribution of different dielectric components. Assuming that radiation-induced oxide- and interface-trapped charges uniformly spread across the gate area and STI sidewalls, $D_{\mathrm{it}}WL$, D_{it}, $N_{\mathrm{ot}}WL$, and N_{ot} can be expressed as

$$D_{\mathrm{it}}WL = D_{\mathrm{it.sti}}T_{\mathrm{sti}}L + D_{\mathrm{it.gox}}WL, \tag{5.59a}$$

$$D_{\mathrm{it}} = D_{\mathrm{it.sti}}\frac{T_{\mathrm{sti}}}{W} + D_{\mathrm{it.gox}}, \tag{5.59b}$$

$$N_{\mathrm{ot}}WL = N_{\mathrm{ot.sti}}T_{\mathrm{sti}}L + N_{\mathrm{ot.gox}}WL, \tag{5.59c}$$

$$N_{\mathrm{ot}} = N_{\mathrm{ot.sti}}\frac{T_{\mathrm{sti}}}{W} + N_{\mathrm{ot.gox}}, \tag{5.59d}$$

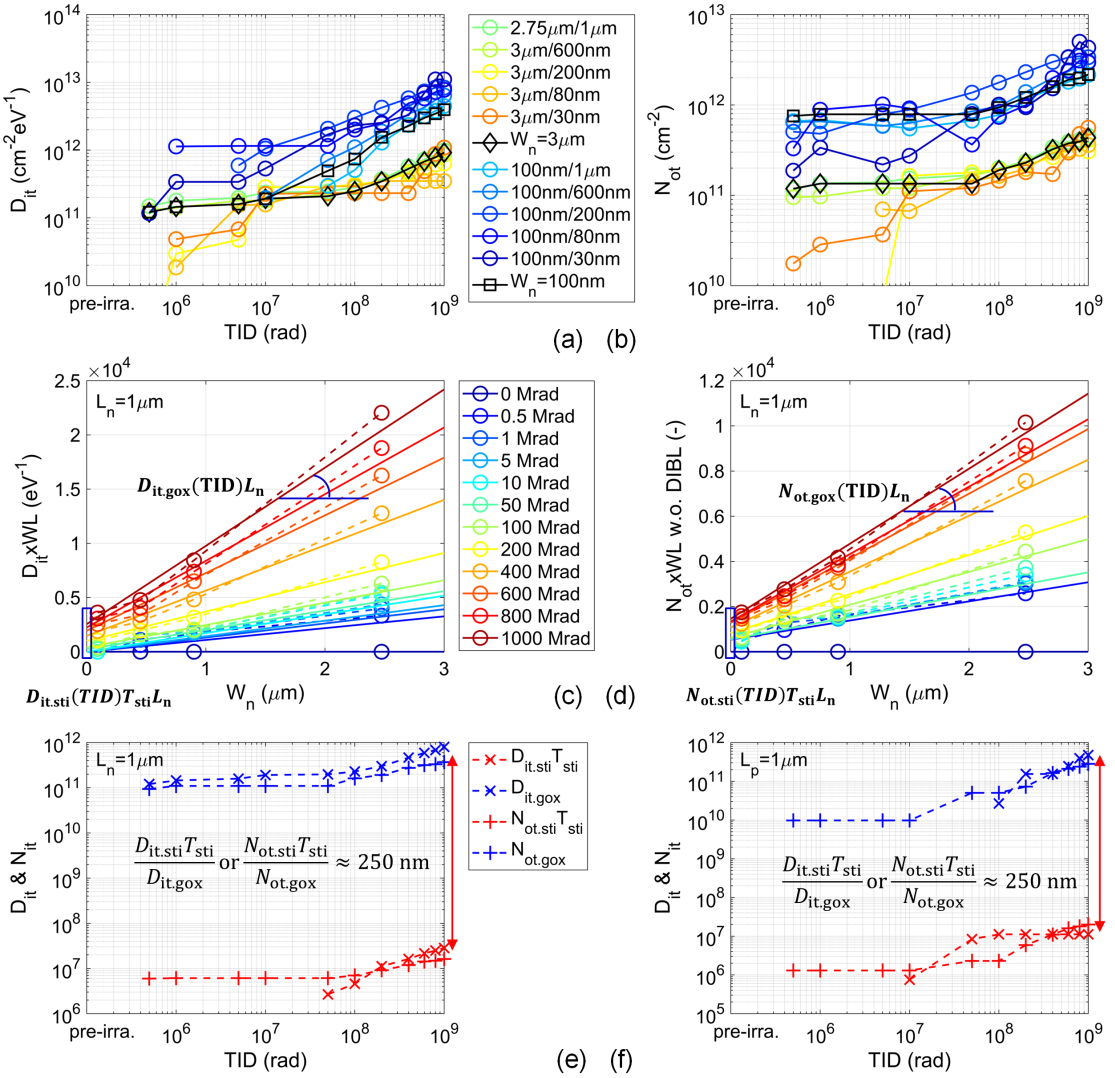


Figure 5.21 – Width dependence of TID-induced trapped charges and trapped-charge scaling over device dimensions: (a) D_{it} and (b) N_{ot} of wide- and narrow-channel *n*MOSFETs versus TID; linear fitting of the total number of (c) oxide and (d) interface traps versus the channel width; (e) D_{it} and (f) N_{ot} related to the gate oxide and STI oxides versus TID. (Zhang, et al. [127].)

where T_{sti} is the equivalent depth of STI sidewalls, $D_{it.sti}$ and $D_{it.gox}$ are the equivalent interface-trap densities related to STI oxides and the gate oxide, respectively, and $N_{ot.sti}$ and $N_{ot.gox}$ are the equivalent oxide-trap densities related to STI oxides and the gate oxide, respectively. When plotting the total number of oxide or interface traps versus the channel width, their intersection points on the vertical axis correspond to the total number of oxide or interface traps related to STI oxides ($D_{it.sti}T_{sti}L$ or $N_{ot.sti}T_{sti}L$) and their slopes refer to the oxide- or interface-trap density per channel width ($D_{it.gox}L$ or $N_{ot.gox}L$). Imagining that we shrink the channel width to zero, the only charge contribution will be from the vertical STI sidewalls

along the channel. Widening the channel then will increase linearly the charge contribution of the gate oxide.

Fig. 5.21c and Fig. 5.21d respectively plot the total number of interface and oxide traps extracted from measurement results of long-channel *n*MOSFETs as a function of the channel width [127]. Both the intersection points and the slopes of the trap-width curves are increasing with TID, indicating the increasing charge contribution related to both STI oxides and the gate oxide. These curves are quite linear with respect to the channel width, allowing us to fit the extracted values with Eq. (5.59a) and Eq. (5.59c). By performing this curve fitting, $D_{\text{it.sti}}T_{\text{sti}}$ ($\text{cm}^{-1}\text{eV}^{-1}$), $N_{\text{ot.sti}}T_{\text{sti}}$ (cm^{-1}), $D_{\text{it.gox}}$($\text{cm}^{-2}\text{eV}^{-1}$), and $N_{\text{ot.gox}}$ (cm^{-2}), which correspond to the interface- and oxide-trapped charge contribution related to STI oxides and the gate oxide, can be extracted for each TID step, as shown in Fig. 5.21e and Fig. 5.21f [127].

When the channel continuously narrows, the relative charge contribution related to STI oxides increases and eventually exceeds that of the gate oxide, resulting in influential RINCE. To ensure device performance and circuit function, it is suggested not to enter this critical range of device dimension. By evaluating the difference of charge contribution related to STI oxides and the gate oxide, it is possible to define a critical channel width W_{crit}. It is around 250 nm for both 28-nm bulk *n*- and *p*MOSFETs, as illustrated in Fig. 5.21e and Fig. 5.21f [127].

The equivalent interface- and oxide-trap densities are dependent on the width and indepen-

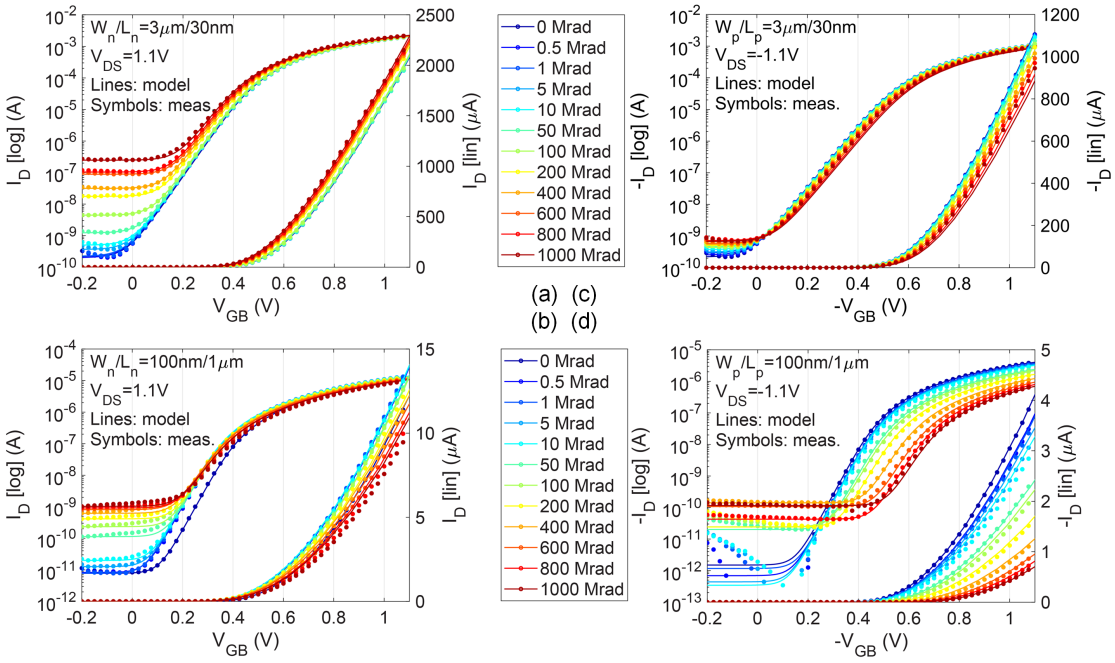


Figure 5.22 – Validation of the design-oriented compact model with the measured $|I_{\text{D}}| - |V_{\text{GB}}|$ curves of two corner (a, b) *n*- and (c, d) *p*MOSFETs using approximated oxide- and interface-trapped charge densities. (Zhang, et al. [127].)

dent of the length, as observed from Eq. (5.59b) and Eq. (5.59d). Using the extracted values of $D_{\text{it.sti}}T_{\text{sti}}$, $N_{\text{ot.sti}}T_{\text{sti}}$, $D_{\text{it.gox}}$, and $N_{\text{ot.gox}}$, these two equations can be utilized for evaluating the TID-induced charge trapping in 28-nm bulk MOSFETs of any dimension for these 12 TID steps. The black lines in Fig. 5.21a and Fig. 5.21b plot the approximate values of the interface- and oxide-trap densities for wide- and narrow-channel *n*MOSFETs. They represent a good approximation for MOSFETs of the same channel width. Building up an empirical model for $D_{\text{it.sti}}T_{\text{sti}}$, $N_{\text{ot.sti}}T_{\text{sti}}$, $D_{\text{it.gox}}$, and $N_{\text{ot.gox}}$ as a function of TID allows us to further predict the radiation response of 28-nm bulk MOSFETs for any TID level.

Fig. 5.22 compares the design-oriented compact model using the oxide- and interface-trap densities calculated from Eq. (5.59b) and Eq. (5.59d) to measurement results of wide/short- and narrow/long-channel *n*- and *p*MOSFETs [127]. Approximate values of the oxide- and interface-trap densities still lead to a good agreement between model results and measurement points for the majority of the tested 28-nm bulk MOSFETs, except for short-channel *p*MOSFETs that undergo reverse RISCE and narrow-channel MOSFETs that suffer RINCE. This step of the modeling work on introducing device scalability is still at the preliminary stage and requires more efforts to reach a more accurate scalable model.

5.4 Summary

This chapter presents a generalized EKV charge-based MOSFET model that includes the effects of oxide- and interface-trapped charges. Oxide-charge trapping simply reduces the effective gate-to-bulk voltage without influencing the linear behavior of the inversion charge density with the surface potential. Interface-charge trapping introduces a dependence of the pinch-off potential on the channel voltage. Using a two-dimensional approximation, the inversion charge density at a given gate-to-bulk voltage is linearized versus both the surface potential and the channel voltage, in the presence of oxide- and interface-trapped charges. This allows the derivation of closed-form expressions for the charge-voltage relation and the current-charge relation. Finally, the effect of velocity saturation is included to model short-channel devices. The newly derived expressions are similar to those of the original EKV MOSFET model, with an additional scaling factor and revised device parameters representing the effects of oxide- and interface-trapped charges. The influence of oxide-trapped charges is captured by a threshold voltage shift, while the effects of interface-trapped charges are manifested as a slope factor increase and a threshold voltage shift. Through the slope factor increase and the threshold voltage shift, the oxide- and interface-trapped charge densities can be extracted at each TID step for providing deeper insights about the observed radiation effects and facilitating the model extension to a broad range of devices.

Targeting a more comprehensive model for radiation-tolerant circuit design, further efforts are made to introduce the effects of TID on the low-field channel mobility and the effective channel width into the proposed model. The mobility reduction model makes use of available parameters, including the pre-irradiation slope factor, the pre-irradiation low-field channel

mobility, and the extracted interface-trapped charge density. Linking all mobility-related parameters allows us to obtain them together through the extraction of the low-field channel mobility. The effective channel width reduction is simply modeled through a newly introduced channel width reduction parameter. This completes the development of a design-oriented compact model for simulating all crucial effects of TID on this 28-nm bulk CMOS process. With five more parameters than the original EKV MOSFET model, including the drain leakage current increase, the radiation-enhanced DIBL parameter, the reduced channel width, the oxide-trap density, and the interface-trap density, the proposed model presents an excellent fit with measurement results over a very wide range of device operation up to 1 Grad of TID, demonstrating its capability of efficiently simulating the effects of TID on 28-nm bulk MOSFETs. Besides, the extracted trapped-charge densities demonstrate a width dependence, implying the dominant influence of STI-related charge trapping. Investigating them as a function of the channel width allows us to isolate the charge contribution of the gate oxide and STI oxides, which in turn enables us to evaluate TID-induced charge contribution in MOSFETs of any device dimension. TID-induced Charge contribution related to different dielectric components can also be semi-empirically modeled as a function of TID, which eventually extends the proposed model for a broad range of devices to a continuous range of TID levels.

6 Conclusions and perspectives

With the perspective of evaluating its potential use in the HL-LHC experiments, this thesis has characterized the radiation response of MOSFETs from a commercial 28-nm bulk CMOS process up to 1 Grad of TID. Overall, this 28-nm bulk CMOS process is very radiation tolerant, indicating its promising use for radiation-tolerant circuits. Since CMOS scaling improves the TID tolerance of highly scaled MOSFETs, radiation-hardness-by-design, which relies on standard CMOS processes and uses innovative design techniques, has become more popular in hardening integrated circuits. CERN has been applying this approach in designing micro-electronic components for its particle experiments. The premise for using design techniques is being aware of the radiation effects on targeted commercial CMOS processes against which electronic components have to be hardened. Therefore, what has been tested, summarized, and concluded can convert into guiding information for the future radiation-tolerant circuit design.

In addition to an extensive understanding of radiation effects on targeted CMOS technologies, a combination of sophisticated design techniques and radiation-aware compact models can make radiation-tolerant circuit design more efficient. With a compact model of the observed radiation effects, circuit designers can predict the radiation response of their design and harden their circuits in the meantime before fabrication. This reduces the iteration of designing, testing, and analyzing, alleviating the repetitive cost of time and expense. For supporting their potential use in particle experiments, this thesis has modeled the observed radiation effects on 28-nm bulk MOSFETs through the incorporation of TID-induced charge contribution into the original EKV charge-based MOSFET model. Introducing the observed typical features eventually leads to a radiation-aware design-oriented compact model that comprehensively accounts for TID effects on this 28-nm bulk CMOS process.

6.1 Conclusions of this work

The conclusions of this work have been documented in the main body of this thesis and the most important points are summarized here.

6.1.1 TID tolerance of 28-nm bulk MOSFETs

The characterization part of this thesis focuses on evaluating measurable radiation effects and identifying dominant damage mechanisms. The radiation tolerance of this 28-nm bulk CMOS process has been studied through an investigation of the radiation response of MOSFETs of various sizes under different experimental conditions. Overall, this 28-nm bulk CMOS process is very tolerant to TID up to 1 Grad, indicating its promising use for radiation-tolerant applications. Wide-channel MOSFETs present slight parametric shifts at the switched-on region, suggesting insignificant charge trapping related to ultrathin gate dielectrics. Spacer-related charge trapping does not show an obvious influence on 28-nm bulk MOSFETs probably due to improved spacer fabrication processes or high energy barriers between spacer materials and gate dielectrics. STI-related charge trapping primarily explains ionizing radiation damage to 28-nm bulk MOSFETs, such as the significant drain leakage current increase of *n*MOSFETs and the serious performance degradation of narrow-channel *p*MOSFETs.

Narrow-channel *n*MOSFETs demonstrate the dominant influence of STI-trapped positive charges below 100 Mrad and negative interface-trapped charges along the gate oxide and STI sidewalls at ultrahigh TID levels. The compensation of oxide- and interface-trapped charges enables *n*MOSFETs to function well even after 1 Grad of TID. However, STI-related charge trapping in *n*MOSFETs contributes a significant parasitic drain-to-source leakage current and results in a considerable drain leakage current increase. Even though the drain leakage increase is tenfold lower at –30 °C, which is close to the real operating condition for the innermost electronics of the HL-LHC experiments, that of narrow-channel *n*MOSFETs is still around two orders of magnitude. High-temperature annealing has been seen efficiently removing the parasitic drain-to-source leakage current. How the latter will evolve over a long period at –30 °C is however unclear. From the power consumption perspective, the drain leakage current increase of *n*MOSFETs should be carefully considered.

In *p*MOSFETs, both oxide- and interface-trapped charges are positive, making *p*MOSFETs more sensitive to TID. Moreover, STI-related charge trapping induces radiation-induced narrow-channel effects (RINCE), which further degrade the performance of narrow-channel MOSFETs. Therefore, narrow-channel *p*MOSFETs undergo the severest performance degradation with a drive current loss by more than 50%, a threshold voltage shift up to −260 mV, and an effective channel width reduction by more than half of their channel width, which however can be partly recovered by high-temperature annealing. Owing to a halo-induced higher average channel doping, short-channel *p*MOSFETs demonstrate a higher TID tolerance than their long-channel counterparts. From the design perspective, it is strongly suggested to avoid using the narrowest-channel *p*MOSFETs with a relatively long channel.

6.1.2 Physics-based modeling of TID effects

The modeling part of this thesis aims at improving the comprehension of the observed radiation effects and developing a design-oriented compact model for radiation-tolerant circuit

design. The modeling work starts with a combination of the original simplified EKV MOSFET model and a newly developed drain leakage current model for simulating the effects of TID on the whole operation range of 28-nm bulk MOSFETs. Following this first attempt of modeling TID effects, a generalized EKV MOSFET model is obtained through the incorporation of oxide- and interface-trapped charges into the original simplified EKV MOSFET model and extended through an investigation of typical damage features of 28-nm bulk MOSFETs.

The simplified EKV MOSFET model is first employed to simulate the inversion operation of 28-nm bulk MOSFETs. With a proper parameter extraction, both of its large- and small-signal models demonstrate an excellent match with measurement results. Those four model parameters efficiently capture the effects of TID on 28-nm bulk MOSFETs. When it comes to radiation-tolerant applications, one of the most serious problems is the significant drain leakage current increase. To better account for its influence on power consumption, a semi-empirical physics-based model with only three parameters is proposed to predict the drain leakage level versus TID. Considering its independence on the gate bias, the parasitic transistor is modeled through a gateless charge-controlled device using a revised EKV MOSFET model. Combing the drain leakage current model with the simplified EKV MOSFET model enables us to predict the effects of TID on the whole operation range of 28-nm bulk MOSFETs.

Targeting a radiation-aware design-oriented compact model for radiation-tolerant circuit design, a generalized EKV charge-based MOSFET model is then derived through the incorporation of oxide- and interface-trapped charges into the original simplified EKV MOSFET model. In the presence of oxide- and interface-trapped charges, the inversion charge density at a given gate-to-bulk voltage can still be linearized but with respect to both the surface potential and the channel voltage. This allows us to derive closed-form expressions for the inversion charge density and the drain current, even in the condition of velocity saturation. These simple formulations demonstrate the effects of TID-induced charge trapping on MOSFET characteristics and crucial parameters. Despite a small number of parameters, the proposed model is capable of matching measurement results over a wide range of device operation. Explicit expressions of device parameters allow us to extract the oxide- and interface-trapped charge densities at each TID step, which provide deeper insights about the observed radiation effects and facilitating the model extension to a broad range of devices.

The generalized EKV MOSFET model captures the impact of oxide-trapped charges by a threshold voltage shift and the effects of interface-trapped charges via a threshold voltage shift and a subthreshold swing degradation. To obtain a more comprehensive model, additional efforts are made to account for the TID-induced reduction in the low-field channel mobility and the effective channel width. The proposed mobility reduction model makes use of available parameters and allows us to extract all mobility-related parameters at the same time. The effective channel width reduction is simply modeled through a newly introduced channel width reduction parameter. This brings us the design-oriented compact model that accounts for all crucial effects of TID on this 28-nm bulk CMOS process with only five radiation-related parameters. With a proper parameter extraction, the proposed model presents an excellent

fit with measurement results over a very wide range of device operation up to 1 Grad of TID, demonstrating its capability of efficiently characterizing and modeling the effects of TID on 28-nm bulk MOSFETs.

This model also demonstrates a width dependence of the extracted oxide- and interface-trapped charge densities, which is consistent with the dominant influence of STI-related charge trapping. Studying the total number of oxide and interface traps as a function of the channel width enables us to isolate the charge contribution of the gate oxide and STI oxides, which in turn provides us with a straightforward way for evaluating TID-induced charge contribution in MOSFETs of any device dimension. The extracted charge contribution of the gate oxide and STI oxides can also be semi-empirically modeled as a function of TID. The introduction of this scalability allows the radiation-aware design-oriented compact model to predict the radiation response of a broad range of devices for a continuous range of TID levels.

6.1.3 General remarks

Investigating this 28-nm bulk CMOS process for its future use in the HL-LHC experiments is beneficial to the whole particle physics community. Targeting the HL-LHC experiments means in fact setting the most stringent specifications, particularly in terms of integration density, circuit functionality, power consumption, and radiation hardness, and hence serves the purpose of setting benchmarks for many others applications. Synchrotron light facilities, nuclear reactors, space applications, and many other applied experiments are looking forward to lower-power ultrahigh-performance radiation-tolerant electronics.

This 28-nm bulk CMOS process allows significant advancements in power consumption and chip integration, which is a must for multi-frame embedded memory, in-pixel data storage, and stronger trigger and data acquisition systems. The radiation tolerance evaluation up to such high TID levels uncovers the knowledge of underlying physical damage mechanisms and provides a sound reference for its application in any conceivable experimental environment. The outcome of the modeling work based on this 28-nm bulk CMOS process can also be implemented into design environments, allowing designers to perform their tasks accounting for the worst case of TID.

Through an extensive experimental investigation, this thesis has demonstrated the high TID tolerance of this 28-nm bulk CMOS process, although the drain leakage current increase of *n*MOSFETs should be carefully accounted for and *p*MOSFETs with the narrowest channel should be avoided for extremely harsh radiation conditions. This nanoscale CMOS process has the same RINCE mechanism with 130-nm and 65-nm CMOS technologies. This may not be a big concern since narrow-channel MOSFETs are not often used in integrated circuits. Short-channel MOSFETs are more radiation tolerant than long-channel ones, allowing digital designers to freely use them for high-performance circuit design. This is opposite with 130-nm and 65-nm CMOS technologies, for which short-channel MOSFETs demonstrate a worse radiation tolerance. This thesis also presents a newly developed design-oriented compact

model that includes all critical effects of TID on this 28-nm bulk CMOS process, which can be used to predict the radiation response of MOSFETs of various sizes. Even though CERN has decided to design radiation-tolerant electronics for this upgrade of the LHC with 130-nm and 65-nm bulk CMOS technologies, this 28-nm bulk CMOS process is still an excellent candidate for the next generation of the HL-LHC experiments and many other radiation-tolerant applications.

6.2 Suggestions for future work

When CMOS technologies continuously scale for reducing cost and improving performance, mismatch in device parameters and variability in transistor performance grow significantly and can play an important role in analog circuits. Unfortunately, due to the lack of samples and limited access to CERN's irradiation systems, this thesis could not cover statistical analysis for evaluating or modeling them. Total ionizing radiation may influence 28-nm MOSFETs of the same size similarly, in consideration of the slight parametric shifts and the insignificant bias dependence. For example, two matched MOSFETs may go through the same value of threshold voltage shift and remain matched under harsh radiation environments. However, studies should still be conducted to investigate the mismatch and variability of this 28-nm bulk CMOS process at least prior to irradiation.

The dose rate used for irradiation measurements is set high, i.e., 10 Mrad/h, to reach a proper time span. It is almost three orders of magnitude higher than the expected level in the future HL-LHC. Such a high dose rate in irradiation tests may underestimate the performance degradation in real applications, which have been well known as dose-rate effects for lowly-biased BJTs with defect-rich thick oxides [44, 45, 184]. The radiation response of CMOS technologies has usually been considered to be dose-rate independent. However, dose-rate effects have unexpectedly appeared in 350-, 250-, 180-, 130-, and 65-nm bulk CMOS processes probably due to charge trapping related to thick STI oxides and spacers [69, 81, 216]. Studies are suggested to estimate low-dose-rate effects of 28-nm bulk MOSFETs.

Until now, experimental investigations and modeling efforts have been devoted to TID effects on DC characteristics of 28-nm bulk MOSFETs. TID-induced gate-oxide-related charge trapping affects low-frequency noise characteristics and compromises analog performance of microelectronic components. Low-frequency noise measurements should therefore be carried out to access the effects of TID on low-frequency noise performance. Bonaldo et al. have published some results of low-frequency noise measurements on the same 28-nm bulk samples in [199], providing the first insight into the low-frequency noise performance and relevant gate-oxide-related charge trapping. Further efforts can be made to evaluate the low-frequency noise performance of more MOSFETs and investigating the trap-energy distribution.

Total displacement damage (TDD) effects involving non-ionizing processes in semiconductors are of the main concern for devices relying on volume carrier conduction. MOSFETs

conducting only at a tiny region near the surface channel are believed to be immune to TDD effects. However, single event effects such as single-event upsets and single-event transient can still play an important role in degrading electronics fabricated with nanoscale CMOS technologies [53] and should be carefully evaluated for digital cells in the context of this 28-nm bulk CMOS process.

This thesis has presented a radiation-aware design-oriented compact model that considers all kinds of TID effects on this 28-nm bulk CMOS process. For designers to run circuit simulations while accounting for TID effects, this newly developed model should be properly implemented into design environments. This modeling work aims at simulating the effects of TID, but the outcome is not limited to the radiation world. General reliability issues that challenge highly scaled MOSFETs, such as bias-temperature instability (BTI) and hot-carrier injection (HCI), also involve oxide- and interface-trapped charges. This defect-included EKV-based MOSFET model may also be adapted for the investigation of BTI and HCI effects.

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List of publications

Journal papers

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Chunmin Zhang

Information

Chinese, born 1988
2000 Neuchâtel, Switzerland
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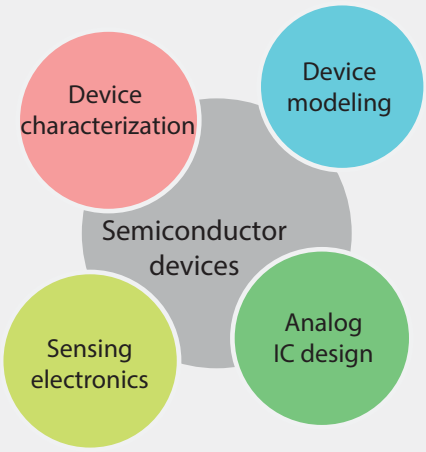
About me

With a systematic education from materials via devices to circuits, my previous research has focused on designing, characterizing, and modeling semiconductor devices as well as investigating radiation effects on CMOS technologies for radiation-hard ICs.
People generally describe me as energetic, proactive, organized, resilient, dependable, and hard-working.

Interests



Expertise

Device characterization
Device modeling
CMOS technologies
Radiation effects on electronics
Scripting, programming, analysis

Honors and awards

2021 Doctorate Award Nomination
2013 Excellent Graduate Student
2011 Best Thesis Award
2010 Outstanding Student
2009 Encouragement Scholarship
2008 Comprehensive Scholarship

Education

10/2015-06/2021 **PhD in Microsystems and Microelectronics**
EPFL, Lausanne, Switzerland

09/2011-06/2014 **MSc Microelectronics and Solid-state Electronics**
Fudan University, Shanghai, China

09/2007-06/2011 **BE in Microelectronics**
Jiangnan University, Wuxi, China

Experience

10/2015-06/2021 Doctoral Assistant — EPFL, Neuchâtel, Switzerland
Characterization and modeling of radiation effects on nanoscale MOSFETs
- Extracted original parameters with the BSIM6 bulk MOSFET model
- Investigated crucial radiation effects on device characteristics
- Performed physics-based compact modeling for radiation-hard circuits
- 5 journal papers, 6 conference reports, and 1 ongoing journal article

Team support
- Conference organizer: administration, logistics, and session assistance
- Teaching assistant: exercise sessions for analog circuits and systems

03/2016-11/2018 Visiting Researcher — CERN, Geneva, Switzerland
X-ray irradiation and annealing measurements on 28-nm bulk MOSFETs

10/2013-07/2015 Research Assistant — Fudan University, Shanghai, China
Development of novel semi-floating-gate transistors
- Developed fabrication processes of U-shape DRAM cells with tunnel FETs
- Evaluated the influence of device scaling through TCAD simulations
- Developed and simulated GaN-based HEMTs with a normally-off state
- 1 journal article about 1T-1D semi-floating-gate DRAMs

03/2012-09/2013 Master's Student — Fudan University, Shanghai, China
Growth and characterization of ruthenium and ruthenium oxide thin filmss
- Developed thin-film growth recipes with atomic layer deposition
- Characterized material properties using electrical and optical tests
- Evaluated potential uses for front- and back-end-of-line applications
- 3 conference papers, among which 1 won the Best Poster Award

Course projects
- Designed, verified, synthesized, and optimized ALUs and multipliers

Competencies

Coursework

Semiconductor process technology
Nano CMOS devices and technologies
Analog and digital IC design
Practical aspects in mixed-signal ICs
Radiation effects on CMOS technologies
Physics of semiconductor devices
Modeling micro- and nanoelectronic devices
Advanced analog and RF IC design
Energy autonomous wireless smart systems
ICs for detector signal processing

Technical skills

Characterization: X-ray irradiation system, Keithley 4200A-SCS, XPS, XRD, AFM, ICCAP
CAD/EDA: Synopsys TCAD, Cadence Virtuoso, Synopsys DC, Mentor ModelSim
Scripting: MATLAB, HSpice, VHDL, Verilog, Tcl, C, UNIX, LaTex

Languages

English (professional at C1-C2) French (conversational at A2-B1) Chinese (native)

Activities and interests

Activities

2018-2020 President of the Chinese Students and Scholars Association in Neuchâtel
Organized career seminars, outdoor activities, and community supports
2017 Member of the EPFL-Microcity team for the yearly BCN Tour Challenge
2013 Member of the Expedition Student Association for voluntarily tutoring a kid

Interests

Languages, reading; cooking, traveling; skiing, hiking, climbing, volleyball, ping-pong