Multi-channel nanowire devices for efficient power conversion

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Nanowire-based devices can potentially be of use in a variety of electronic applications, from ultra-scaled digital circuits to 5G communication networks. However, the devices are typically restricted to low-power applications due to the relatively low electrical conductivity and limited voltage capability of the nanowires. Here, we show that wide-band-gap AlGaN/GaN nanowires containing multiple two-dimensional electron gas channels can be used to create high-electron-mobility tri-gate transistors for power conversion applications. The multiple channels lead to improved conductivity in the nanowires, and a three-dimensional field-plate design is used to manage the high electric field. Power devices made with 15-nm-wide nanowires are shown to exhibit low specific on-resistances of 0.46 mΩ·cm^{-2}, enhancement-mode operation, improved dynamic behavior, and breakdown voltages as high as 1300 V.

Due to their unique properties, nanowire-based electronic devices are being adopted in an increasing number of applications including microelectronics, sensing, and RF communications[1,2]. In particular, their increased surface-to-volume ratio provides enhanced channel controllability compared with more conventional setups, allowing significant device miniaturization and performance improvement. However, typical applications of nanowire-based devices are limited to low-power applications, and the potential of nanowires in the field of high-power devices for energy conversion remains relatively unexplored.

The key challenge is to try to reduce the device resistance in the on-state (R_{ON}) while maintaining high voltage blocking capability (V_{BR}) in the off-state, which is typically summarized in a device figure-of-merit proportional to V_{BR}^2/R_{ON} [3,4]. R_{ON} is ultimately limited by the semiconductor mobility (μ) and carrier density (N_s), whose product defines the channel electric conductivity. While μ is determined, to a large extent, by the semiconductor structure, increasing N_s is a much more effective approach to reduce the R_{ON}. However, a large N_s typically reduces μ, increases the threshold voltage (V_{TH}) due to the more challenging electrostatic gate control[5], and reduces the V_{BR} because of the more difficult electric field management[6]. The large surface-to-volume ratio of nanowires, which results in a larger number of carriers (with respect to the device width) and improved electrostatics channel control, can help address these issues. In addition, their three-dimensional geometry[7,8] facilitates strategies to manage high electric fields compared to conventional approaches for high-voltage devices, which typically rely on bulky drift layers and planar field plates.

In this article, we report a multi-channel nanowire-based high-electron-mobility transistor (HEMT), in which multiple quantum wells[9–16] with high-mobility two-dimensional electron gas (2DEG) channels are grown and stacked within the same semiconductor platform. The multi-channel heterostructure allows a large number of carriers to be distributed in several high-mobility

parallel channels, overcoming the major semiconductor trade-off between the channel carrier concentration (N_s) and their mobility (μ). This leads to a significant enhancement in N_s independently from μ, and results in a reduction in sheet resistance (R_{sh}) with respect to conventional single quantum-well structures.

Device structure and operation

Figure 1 outlines the architecture, operation, and key performance metrics of the device. The multi-channels are structured into nanowires in the gate region of the device, on which a 3-dimensional gate electrode (tri-gate)[17,18] is formed to control the parallel channels through the sidewall portions of the nanowire (Fig. 1(b)). The nanowire width on the source side is tuned to shift the V_{TH} to positive values and achieve enhancement-mode (e-mode) operation, which is an important requirement for power devices and extremely challenging to achieve in high conductivity materials. The drain-side termination of the nanowire is designed with an angled shape to form a slanted field plate that effectively distributes the high electric fields (Fig. 1(c)), resulting in a large V_{BR}.

This is particularly important in such high-conductivity structures due to the difficulty in creating depletion regions at small enough gate voltages to hold high voltages.

With this judicious nanowire design on highly-conducting multichannel structures, high-performance power devices with normally-off behavior, low on-resistance, and high-voltage operation were achieved demonstrating a figure-of-merit that significantly surpasses the state-of-the-art. This device concept offers a promising pathway for future efficient power conversion.

Design of the multi-channel heterostructure

Multi-channel nanowire MOSHEMTs were realized on a 4x-channel AlGaN/GaN epitaxy grown on Silicon substrate. This structure takes advantage of the excellent material capabilities of GaN for power devices integrated on large-area Si substrates through heteroepitaxy[4,19], rendering a cost-effective platform that has a tremendous prospect for efficient energy conversion[20–22]. The

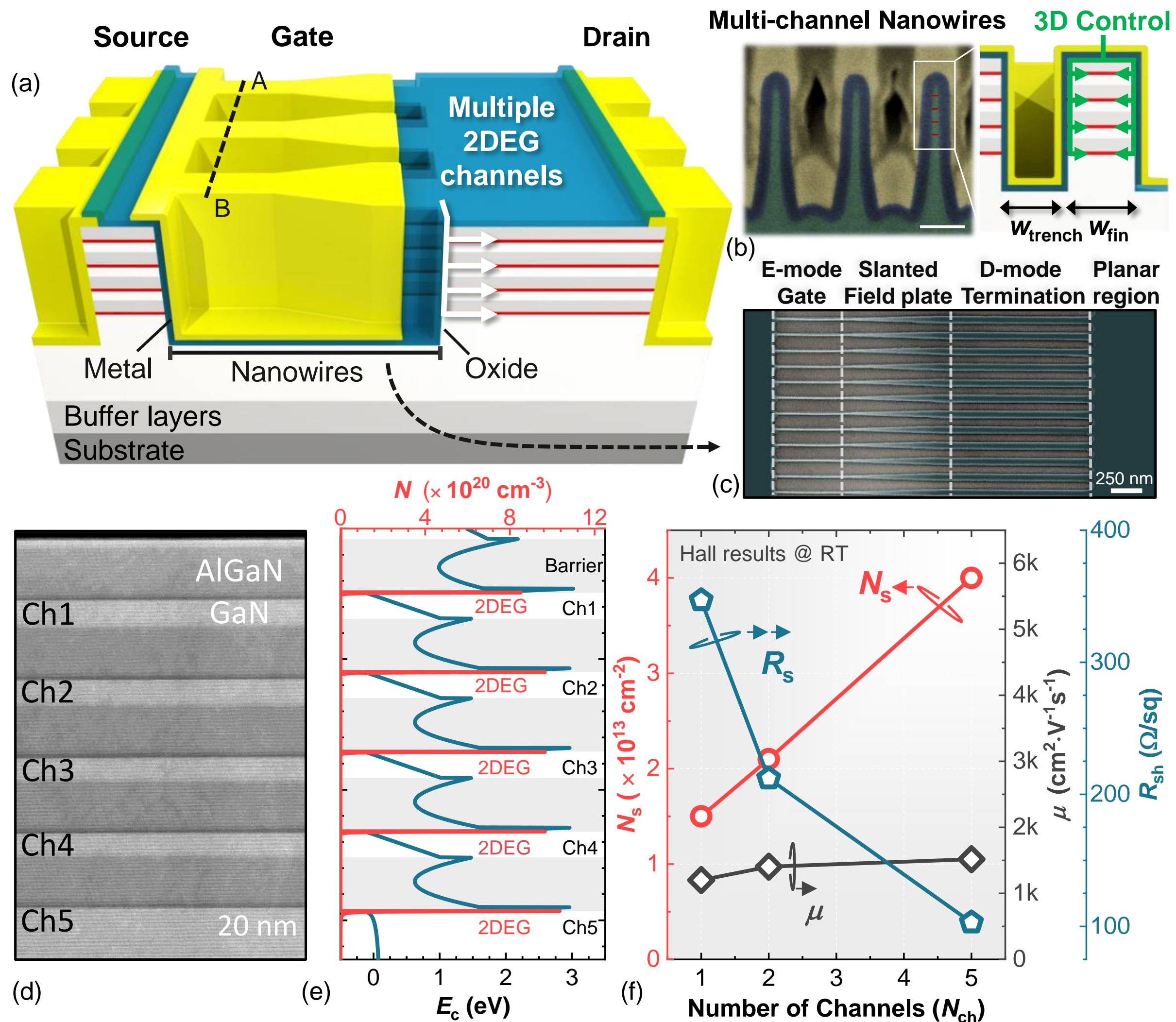

Figure 1. Concept of multi-channel tri-gate devices. (a) Three-dimensional schematics of the proposed multi-channel device, featuring multiple parallel channels, to yield extremely low R_{ON}, controlled 3-dimensionally by a tri-gate electrode. The tri-gate is terminated in the nanowire region, rather than on the planar region, to better distribute the electric field and result in high V_{BR}. (b) FIB cross-section and schematics of the multi-channel nanowires covered by the tri-gate structure along the AB line in figure (a). The tri-gate enables a simultaneous 3D control over all the multiple channels in the nanowire. The scale bar is 100 nm. (c) Top SEM image of the nanostructured gate area (before the gate oxide and electrode deposition) which includes, starting from the source side, an e-mode region achieved by 15 nm-wide nanowires, and a slanted region terminated on 100 nm-wide d-mode nanowires for optimal electric field management. (d) HAADF STEM image of multi-channel AlGaN/GaN heterostructure with five parallel channels (Test-epi-A in Supplementary data Table s1), whose simulated energy band diagram is shown in (e). (f) Dependence of the N_s, μ, and R_{sh} on the number of channels (N_{ch}), which were grown on sapphire substrates with undoped $Al_{0.3}GaN$ barrier layers (Test-epi-B in Supplementary data Table s1).

heterostructure was carefully designed to yield low R_{sh} in a small thickness, which is important to facilitate the fabrication of tri-gates around the nanowires, and also results in a negligible increase in epitaxial growth time and cost. Figures 2(a) and (b) show the schematic of the structure containing 4 channels, in which the top 3 channels were formed by 20 nm $Al_{0.25}GaN$ barrier layers, selectively doped with a Si concentration of 1×10^{19} cm^{-3} (Type I) (Fig. 2(c)), followed by 1 nm AlN spacer and 20 nm-thick GaN channel layers. It should be noted that, while beneficial for the electron mobility, the AlN spacer does not considerably influence the N_s concentration, which instead was determined by the doped AlGaN barrier layers. The bottom channel consisted of a 10 nm $Al_{0.25}GaN$ barrier, selectively doped with Si concentration of 5×10^{18}cm^{-3} (Type II) (Fig. 2(d)). design resulted in a low R_{sh} of 83 ohm/sq and a large N_s of 3.9×10^{13} cm^{-2}, which is nearly 4-times higher compared to conventional AlGaN/GaN single-channel structures. Thanks to the carrier spreading in the four channels, a very high μ of 1930 cm$^{2}\cdot$V^{-1}s^{-1} was achieved despite such high N_s, rendering a significant enhancement in channel conductivity over counterpart single-channel structures, even when compared to different barrier materials (Fig. 2(e)). In addition, after optimizing the epitaxial structure (Fig. 2(f)), the small R_{sh} was achieved using only 4 channels with a small total thickness of ~130 nm, thanks to the Type I barrier layers. This facilitates the tri-gate fabrication by reducing the aspect ratio of the nanowires. The bottom barrier was thinner and less doped to enable the control of the bottom-most channel, which is the farthest from the top gate and the most prone to possible punch-through in OFF state.

The enhanced channel conductivity in multi-channel structures is even more pronounced when they are structured into nanowires. Fig. 2(g) shows the μ and N_s extracted from Hall-Bar measurements for multi-channel nanowires of different widths (w_{NW}). While a mobility decrease is expected in narrow nanowires due to roughness scattering[1,23] and donor-like states on the

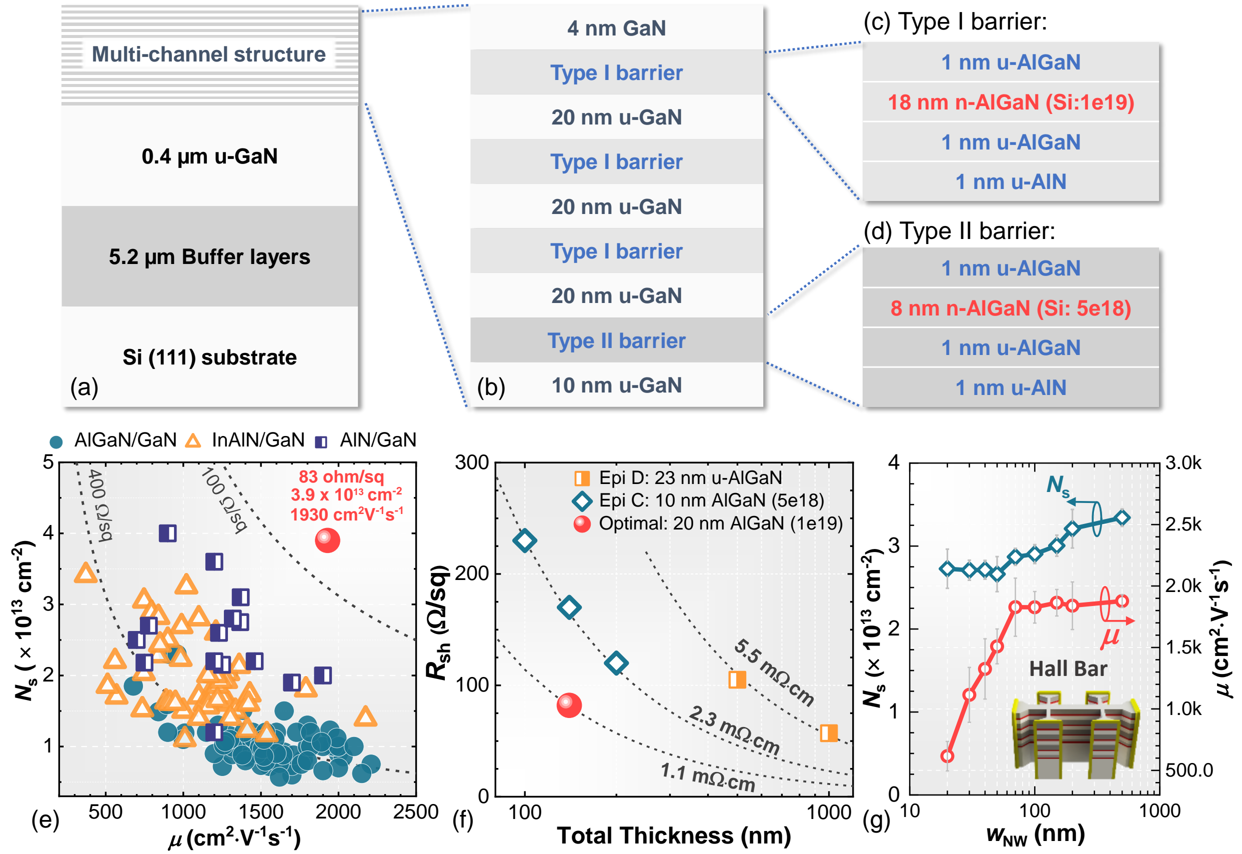

Figure 2. Design of multi-channel epitaxial structures for power devices. (a)-(d) Schematics of the design of the multi-channel AlGaN/GaN grown on 6-inch Silicon substrate. (e) Benchmark of the sheet resistance (R_{sh}) of the 4-channel heterostructure in this work against conventional single-channel GaN-based heterostructures in the literature, with AlGaN, InAlN, and AlN barriers. High μ of 1930 $cm^2 \cdot V^{-1}s^{-1}$ was achieved in combination with a large N_s of 3.9 x 10^{13} cm^{-2}, resulting in R_{sh} of 83 Ω/sq. (f) Dependence of R_{sh} on the heterostructure thickness in different multi-channel structures (Test-epi-C and Test-epi-D in Supplementary Tab. s1). The optimized design resulted in a very low R_{sh} of 83 Ω/sq with a total heterostructure thickness of only 130 nm. (g) N_s and μ for multi-channel nanowires with different widths, measured by Hall Bars at room temperature (inset in (g)). High μ above 1800 $cm^2 \cdot V^{-1}s^{-1}$ was maintained down to 70 nm-wide nanowires along with a large N_s, in the range of 2.8 – 3 x 10^{13} cm^{-2}. Details about the Hall bar geometry and experimental setup can be found in Supplementary data Figure s1. Detailed results of the Hall measurements on the multi-channel nanowires can be found in Supplementary data Table s2-s4.

sidewalls[24,25], a high μ above 1800 $cm^2 \cdot V^{-1}s^{-1}$ was maintained down to 70 nm-wide nanowires, along with a large N_s, in the range of 2.8 – 3 x 10^{13} cm^{-2}. Besides, large mobility above 1200 $cm^2 \cdot V^{-1}s^{-1}$ was measured for nanowires as narrow as 20 nm at a gate voltage of 5 V. This results in extremely small R_{sh} even for e-mode nanowires, which is still much lower than in conventional single-channel planar structures. Detailed measurement results regarding the R_{sh}, N_s, and μ can be found in Supplementary data Table s2-s4. Additional electron mobility measurements in multi-channel nanowires as a function of the gate voltage are presented in Extended data Figure 1.

Gate control and enhancement-mode operation

Such excellent conductivity achieved with multi-channel structures would be of little value unless it can be electrostatically controlled and modulated. Conventional planar gate electrodes cannot turn off all the embedded multi-channels due to the electric field shielding from the top channel to the ones underneath and to the large gate-to-channel distance. The tri-gate structure around the multi-channel nanowires[5,11,26] offers instead a superior electrostatic control thanks to its 3D architecture which enables simultaneous side gate control on all of the embedded channels. As shown in Fig. 3(a), the planar-gate devices could not be turned off even at a high gate voltage (V_G) of -50 V. In contrast, the tri-gate is far more effective in controlling the multi-channel structures and results in high I_{ON}/I_{OFF} ratio ~ 10^{10}. In addition to pinching off the channels, the tri-gate enabled the simultaneous modulation of all the parallel 2DEGs. As shown in Fig. 3(a), the flat and small transconductance (g_m) characteristics in wide nanowires, exhibiting multiple peaks, is caused by the successive turn-on of the parallel channels by V_G. However, in narrow nanowires (50 nm and below), the distinct peaks merged into a single large and sharp peak, indicating the simultaneous modulation of all parallel channels thanks to the dominant sidewall gate control, relative to the top

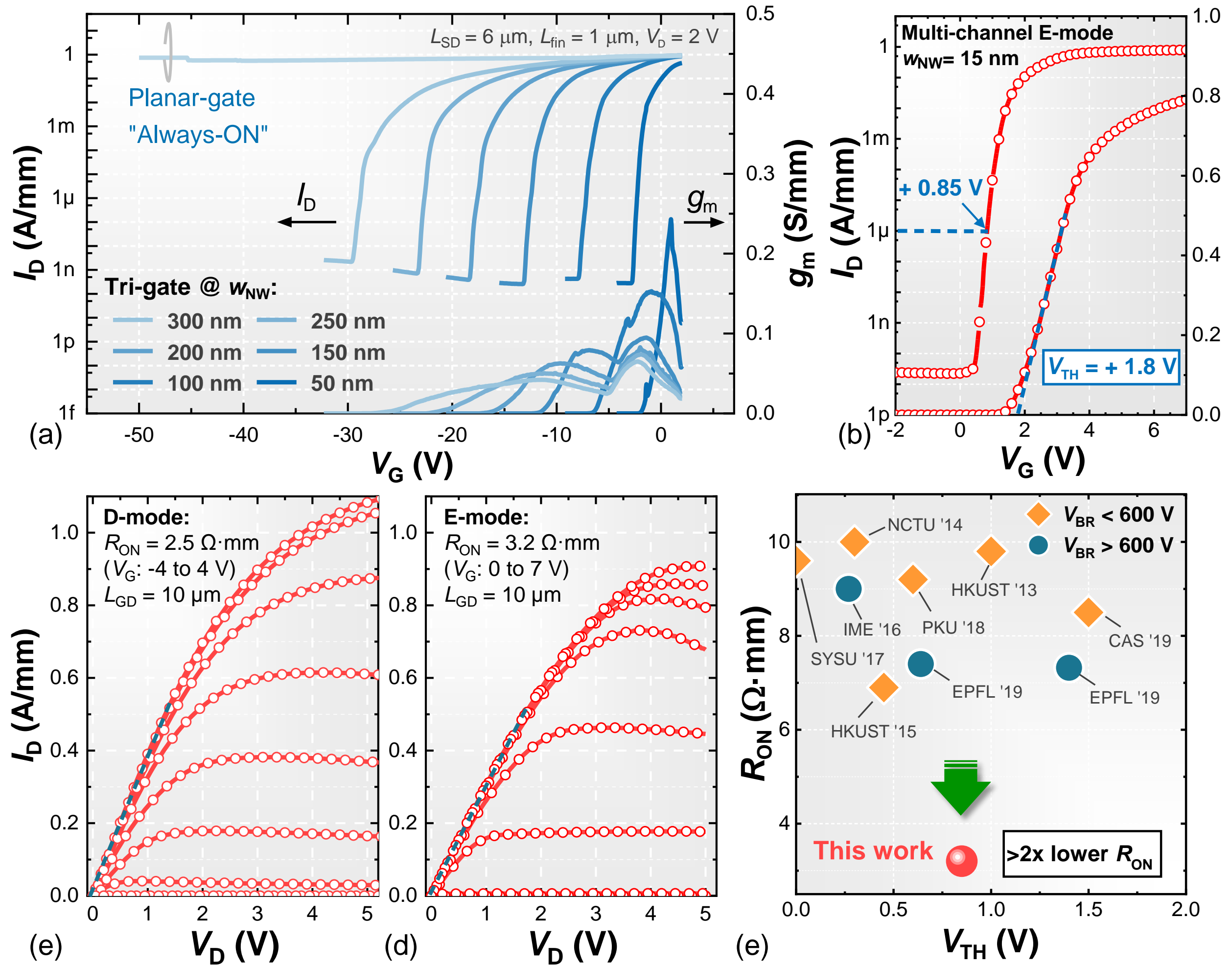

Figure 3. Multi-channel tri-gate device characteristics. (a) Transfer characteristics of multi-channel MOSHEMTs based on a planar gate and on tri-gates with different w_{NW}. (b) Transfer characteristics of an e-mode multi-channel MOSHEMT, with nanowire width (w_{NW}) of 15 nm in the e-mode gate region (see Fig. 1(c)), L_{GD} of 10 µm, and Pt/Au gate metals, showing V_{TH} of 1.8 V. Output characteristics of (c) d-mode and (d) e-mode multi-channel MOSHEMTs showing the very low on-resistance for both devices. The current and all other values were normalized by the entire width of the device. (e) R_{ON} versus V_{TH} benchmark for the presented multi-channel e-mode devices compared to state-of-the-art single-channel devices present in the literature. Multi-channel devices show a more than 2x-lower R_{ON} for the same V_{TH} with respect to the single-channel counterpart. V_{TH} has been defined at 1µA/mm.

gate. Besides providing excellent electrostatic control on the multi-channel heterostructure, the tri-gate architecture enables to tune the device V_{TH} by changing the width of the nanowires (w_{NW}), which allows to precisely design the electric field within the device. V_{TH} decreased drastically when w_{NW} was reduced, thanks to the enhanced tri-gate control and the sidewall depletion contribution in narrower nanowires, and even enabled e-mode operation in multi-channel devices despite the much larger carrier density with respect to conventional single-channel structures (Extended data Figure 2). Figure 3(b) shows the transfer characteristics of e-mode multi-channel devices, based on 15 nm-wide nanowires in the gate region (see Fig. 1(c)) with Pt/Au as tri-gate metals instead of the commonly used Ni/Au gates[6]. The use of high work-function Pt metallization was crucial to shift the V_{TH} to more positive values[27] (Extended data Figure 2), which is of great importance for the fail-safe operation of power devices. Despite the high N_s of 3.9×10^{13} cm^{-2} in the epitaxy, a V_{TH} of +1.8 V evaluated by linear extrapolation of the I_D-V_G curve (+0.85 V at 1 μA/mm) was achieved, along with a low I_{OFF} of only 57 pA/mm at $V_G = 0$ V and a high ON/OFF ratio over 10^{10}, revealing excellent e-mode operation. Excellent stability of the device V_{TH} was demonstrated both during high-frequency switching by gate lag measurements[28] and during high-temperature operation up to 150 ºC (Extended data Figure s3). Most importantly, these e-mode multi-channel nanowire devices presented extremely low R_{ON}, which is highly desirable for efficient power devices. With a gate-to-drain distance (L_{GD}) of 10 μm, the R_{ON} was 2.5 Ω·mm for d-mode (50 nm-wide tri-gate) and 3.2 Ω·mm for e-mode (15 nm-wide tri-gate) multi-channel tri-gate devices, respectively (Figs. 3(c) and (d)). This resulted in a more than a two-fold reduction in the R_{ON} with respect to the best performing single-channel e-mode power device with similar V_{TH}, as shown in Fig. 3(e). In addition, the multi-channel platform enables the monolithic integration of e-mode and depletion-mode (d-mode) devices for integrated circuits, since both share the same

process flow and can be simply co-fabricated on the same chip. Further information regarding the threshold voltage in multi-channel nanowires and the multi-channel nanowires width uniformity can be found in Extended data Figure 2-3 and Supplementary information Figure s2. For a fair comparison with other devices, all the current and resistance values shown in Figs. 3 and 4 were normalized by the width of the entire device footprint (w_{device}), which includes the width of the nanowires (with 2DEG) and the trenches (without 2DEG).

High electric-field management strategy

For power conversion applications, in addition to small R_{ON} and e-mode operation, high V_{BR} is of major importance. For this reason, a reduced R_{ON} is a little value unless it is combined with large voltage blocking capabilities, which is more challenging in highly-conductive structures. This was achieved in multi-channel devices by engineering the termination of the tri-gate electrode. While planar field plates (FPs) are usually implemented in single-channel devices to address the uneven distribution of the electric field in OFF state and reach higher V_{BR}, they are less suited for high-conductivity multi-channel devices. Figure 4(a) shows the deterioration of the measured V_{BR} from single-channel to multi-channel d-mode devices, as the conductivity of the heterostructure was increased (R_{sh} reduced). While the V_{BR} in single-channel devices with R_{sh} of 280 Ω/sq was 1.3 kV, it dropped to ~40 V in multi-channel structures with R_{sh} below 170 Ω/sq. Such a decrease is due to the inability of the planar FP to deplete all the multi-channels beneath as a result of the high N_s and the shielding effect previously discussed, which limits its effectiveness as a field plate and causes premature device breakdown. This shows that planar FPs are not adapted for multi-channel structures and reveals the need for novel 3D field plates. By replacing the FP termination on the planar region with a tri-gate field plate termination on the D-mode portion of the nanowires (see Fig. 1 (c)), the V_{BR} was greatly enhanced to about 600 V (Fig. 4(a)). In addition, the introduction

of a 3D field plate based on a slanted nanowire design (slanted field plate region in Fig. 1 (c)) resulted in a further V_{BR} enhancement to 1300 V (below 1 μA/mm), along with a small I_{OFF} below 20 nA/mm at V_D = 600 V (Fig. 4(b)). This high V_{BR} value represents a more than 35x-times improvement with respect to the conventional planar FP architecture. Such significant enhancement is due to two main reasons: i. the gate electrode terminated in the nanowire region with a 3D architecture (Fig. 1(a)), instead of a planar structure on top of the multi-channels, which can more effectively deplete the all of the channels and avoid early oxide breakdown; ii. the tri-gate structure based on a slanted nanowire design effectively distributes the electric field, enhancing the V_{BR}[7]. More details regarding the design of the nanowire termination and the comparison between planar and tri-gate based field plates can be found in Supplementary information Figure s3. Additional measurements on the dynamic performance of multi-channel devices passivated by low-pressure chemical vapor deposition (LPCVD) Si_3N_4[29] are presented in Extended data Figure 4 and demonstrate that the multi-channel technology can offer not only improved DC performance but also reduced current collapse up to large operating voltage.

The unique combination of the ultra-low R_{ON} and high V_{BR} in e-mode multi-channel nanowire devices renders a significant advance in performance from conventional single-channel devices. Firstly, the multi-channel devices surpassed the observed limit of R_{ON} for lateral GaN power devices (Fig. 4(c)), by considerably reducing the R_{ON} from ≧ 7 Ω·mm in 600/650 V-rated single-channel devices to 2.5 Ω·mm for d-mode and 3.2 Ω·mm for e-mode multi-channel devices, while keeping a high V_{BR} of 1300 V. This resulted in a more than 4-fold decrease in specific on-resistance $R_{ON,SP}$ with respect to the best performing single-channel device with the same blocking performance (Fig. 4(d)). The multi-channel devices achieved a record figure-of-merit of 4.6 GW/cm^2 for d-mode devices and 3.8 GW/cm^2 for e-mode devices, which represents a substantial

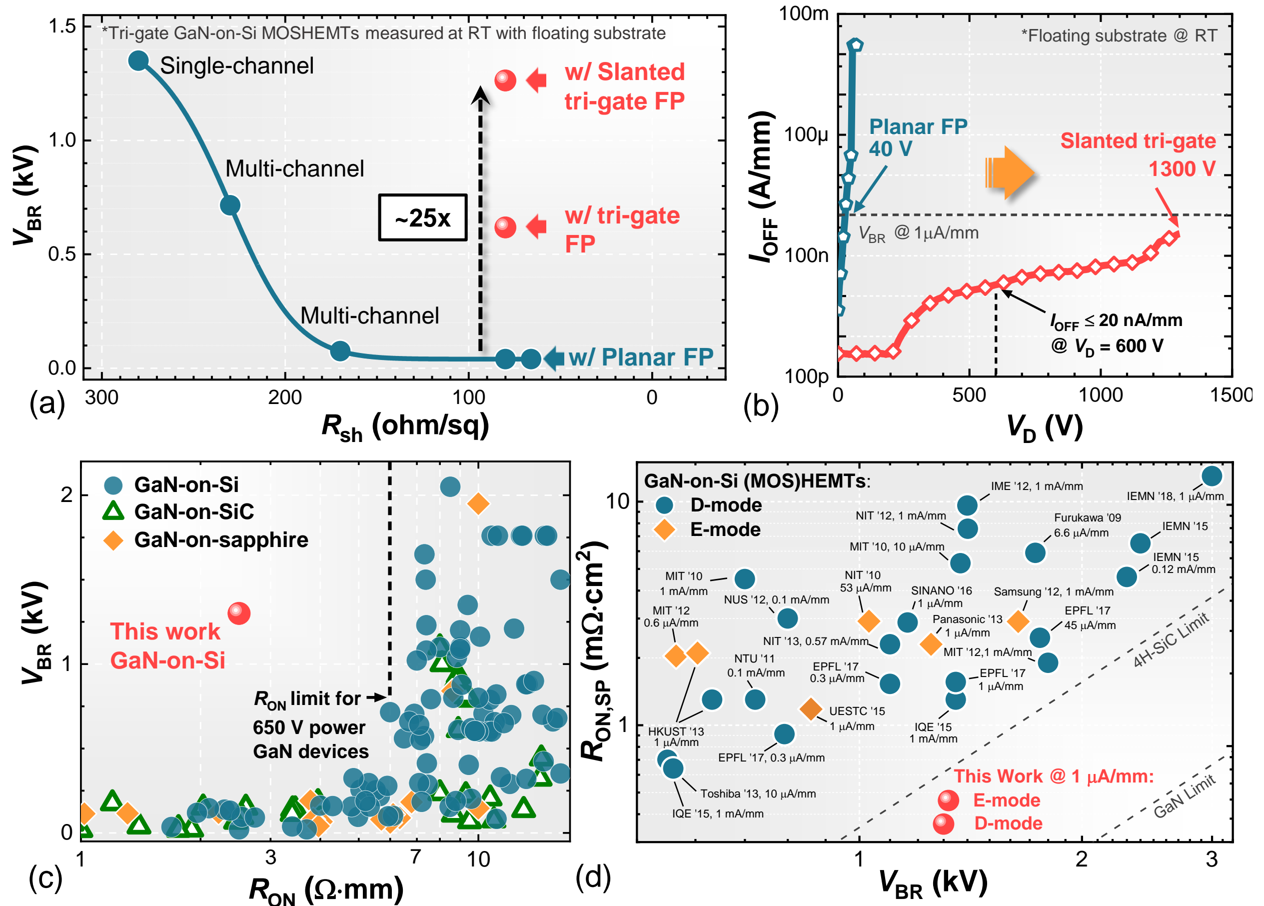

Figure 4. Achieving high breakdown voltage and low on-resistance on multi-channel structures. (a) Dependence of hard V_{BR} versus R_{sh} in different multi-channel structures. A significant enhancement in V_{BR} was achieved by introducing a tri-gate and slanted tri-gate 3D field plate with respect to conventional planar designs. (b) Comparison of OFF-state breakdown characteristics of multi-channel tri-gate MOSHEMTs with planar FP and slanted tri-gate FP. The slanted tri-gate FP led to an improved potential distribution, resulting in a high V_{BR} of 1300 V. The V_{BR} has been defined at 1 µA/mm. (c) V_{BR} versus R_{ON} and (d) $R_{ON,SP}$ versus V_{BR} benchmarks of the slanted tri-gate multi-channel MOSHEMTs against conventional single-channel GaN (MOS)HEMTs in the literature. Multi-channel devices surpass the material figure-of-merit limit of 4H-SiC, showing a substantial improvement with respect to single-channel devices and a record figure-of-merit of 4.6 GW/cm^2 for d-mode devices and 3.8 GW/cm^2 for e-mode devices. A transfer length of 1 µm from each side has been considered to evaluate $R_{ON,SP}$.

improvement with respect to the single-channel counterpart (Fig. 4(d)). This is the first time that GaN lateral devices, both d-mode and e-mode, surpass the figure-of-merit limit of 4H-SiC semiconductors. These results reveal the potential of multi-channel nanowire-based devices for high-efficiency and ultra-compact power applications.

Conclusions

The capabilities and advantages of our device result from the unique combination of a multi-channel platform and carefully designed nanowires, addressing various important trade-offs, while offering state-of-the-art performance with respect to current technologies. The proposed technology also offers opportunities for further innovation in electronic devices. The reduction of R_{ON} via the inclusion of more device channels is an approach that could be applied to other types of electronic devices, including Schottky barrier diodes[30], RF switches, and amplifiers[11,26,31], ultra-wide-band-gap semiconductor materials, such as Ga_2O_3[32–34], and high-mobility III-Vs, such as InGaAs and InAs[35].

Methods

Fabrication of multi-channel tri-gate HEMTs.

The device fabrication started with e-beam lithography to define the nanowires and mesa of the device using hydrogen silsesquioxane (HSQ) as a resist. The HSQ was converted into SiO_x by the electron beam and then used as the hard mask for nanowires and mesa etching. Proximity error correction techniques were used to properly adjust the electron dose and achieve dense arrays of nanowires. The mesa and nanowires were patterned by Ar/Cl_2 inductively coupled plasma (ICP) dry etching with a depth of 250 nm. After that, 5 cycles of O_2 plasma/HCl treatment was implemented to reduce the damages caused by the dry etching, especially at the nanowire sidewalls.

In each of the cycles, the devices were exposed to O_2 plasma for 1 minute in a barrel plasma stripper, at a power of 600 W, and then dipped into 37% HCl solution for 1 minute. During this process, the remaining HSQ-based SiOx from the etching served as the mask to protect the surface of the heterostructures from the plasma and was later removed by buffer oxide etching (BOE). Then ohmic metals stack (Ti/Al/Ti/Ni/Au) was evaporated in source/drain regions, and alloyed at 780 ℃ for 30 seconds in N_2 atmosphere. 25 nm of SiO_2 were deposited by atomic layer deposition as the gate dielectric, which was selectively removed by wet etching in source/drain regions to open the contacts. Finally, the gate electrode was defined by e-beam lithography using a double layer PMMA resist, followed by the deposition of a Pt (40 nm) - Au (100 nm) metal stack by evaporation.

STEM characterization and specimen preparation

The tri-gate structure was prepared for transmission electron microscopy (TEM) by focused ion beam milling of a cross-sectional lamella (FIB, Zeiss NVision 40). Scanning TEM (STEM) was performed at 200 kV with a spherical aberration-corrected TEM (FEI Titan Themis 60-300) equipped with a high brightness source and an energy dispersive X-ray spectrometer (EDS) comprising of four silicon drift detectors (SDDs). Imaging was performed by collecting incoherently scattered electrons with the high-angle annular dark-field (HAADF) detector. Incoherently scattered electrons are sensitive to the atomic number and thus the contrast in the HAADF STEM images reflects compositional information.

Hall measurement

Hall measurements were performed in 6-lead MOS-gated Hall bar geometry following the procedure from *Lake Shore 7500/9500 Series Hall System User's Manual*, using Keithley 6221 current source, 2182A nano-voltmeter, 2612B source-measurement unit as picoammeter and gate

bias unit (also monitoring the gate leakage), 3765 Hall Effect card as a switch and permanent 0.345 T magnet (field measured by gauss meter on the chuck). Current, field reversal, and homogeneity checks were performed in order to minimize errors. All the measurements were performed at a low current density of 20 mA/mm to probe the device in the linear regime and extract the low-field mobility. Distance between voltage sensing leads was 2 µm for all nanowires and the leads were 60 nm wide while the nanowire width was swept from 20 nm to 500 nm. Nanowires were extended 0.5 µm from voltage measurement leads in order to prevent shortening of Hall voltage by current injecting contacts. The leakage between contact pads and the gate leakage were at least 3 orders of magnitude lower than the lowest current forced in the nanowires. For the gated hall-bar structures, the gate bias was set by a Keithley 2612B voltage source.

Data and materials availability

All data is available in the main text or the supplementary materials.

Supplementary Materials:

Figures s1-s3

Table s1-s4

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Author Contributions

All authors have given approval to the final version of the manuscript. E.M, L.N and J.M conceived the project. L.N, J.M and C.E fabricated the devices, performed and analyzed the electrical measurements. K.C, P.X and J.M grew the epitaxy structures. V.T, T.-H.S., T.W. performed and analyzed the STEM measurements. E.M, L.N and J.M wrote the paper, an all authors have given approval to the final version of the manuscript.

Competing interests

Authors declare no competing interests.

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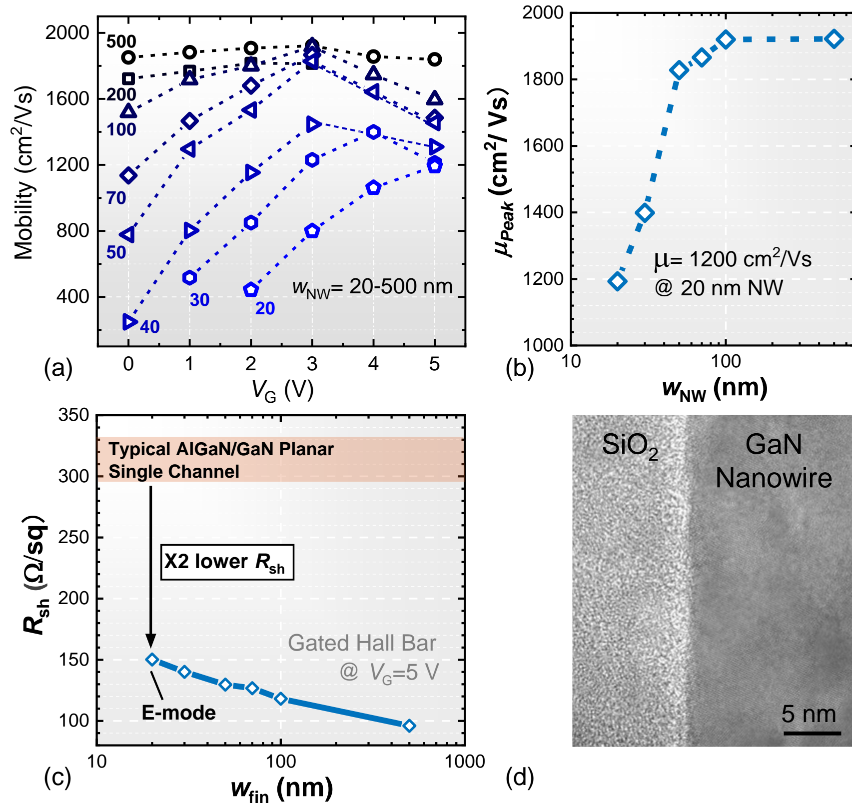
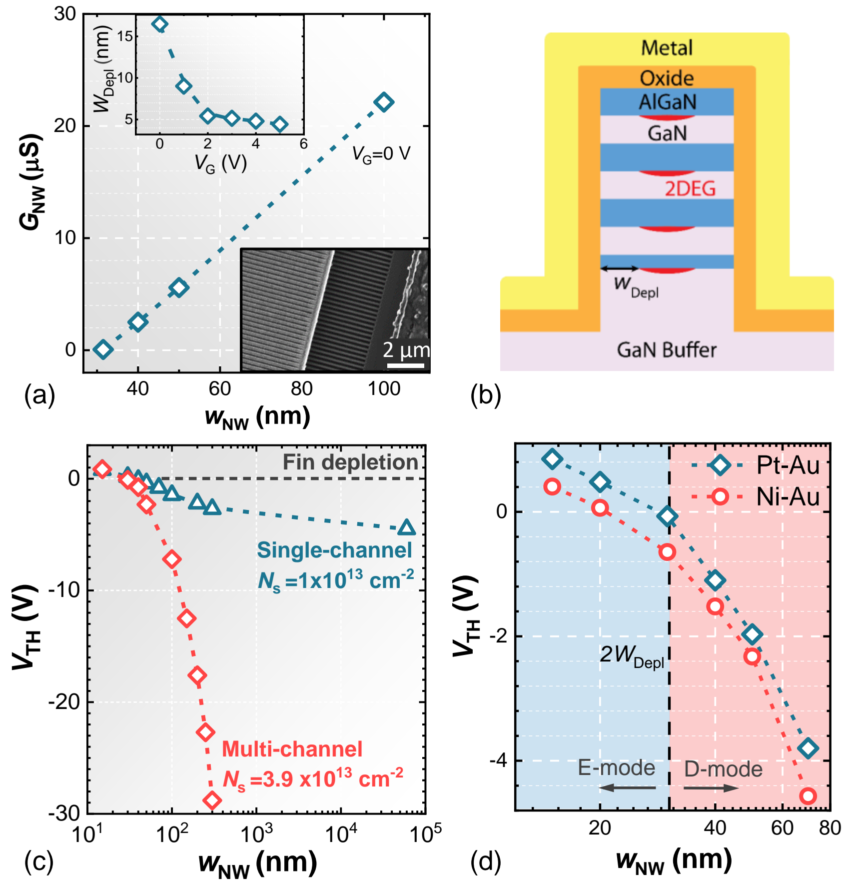
Extended Data



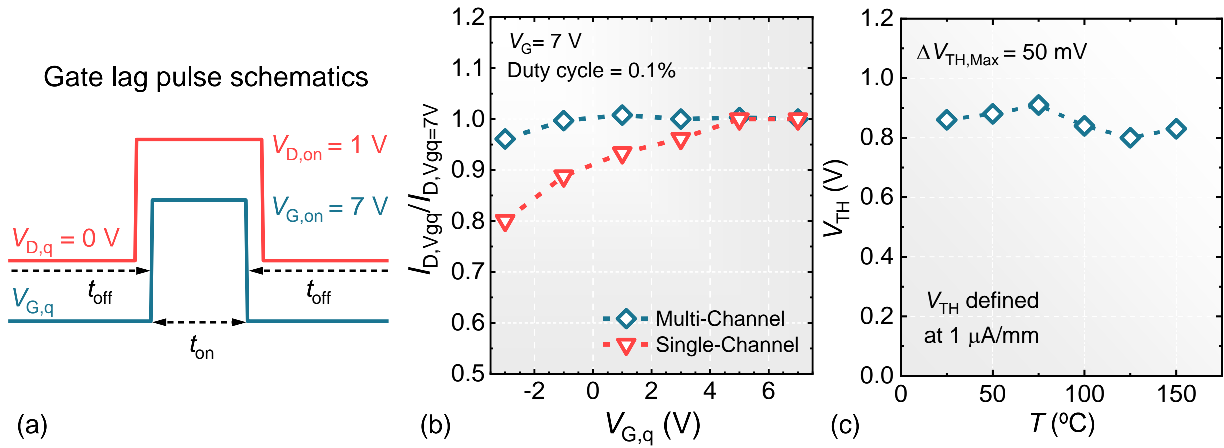
Extended Data Fig. 1. Electron transport in multi-channel nanowires. (a) Electron mobility in multi-channel nanowires measured by gated hall bar at different gate voltages (V_G) and nanowire width (w_{NW}). The mobility peak depends on the nanowire width and shifts to higher V_G as w_{NW} decreases. (b) Peak mobility as a function of w_{NW}, extracted from figure (a). 20 nm-wide nanowires still present a high mobility value of 1200 cm^2/Vs. This is of great importance as it demonstrates excellent electron conduction despite the small nanowire dimensions and the sidewalls scattering contributions. The excellent mobility results in a very low sheet resistance R_s of 150 Ω/sq for 20 nm e-mode nanowires (c). Such value is half of the typical sheet resistance of conventional planar single-channel heterostructures. (d) TEM cross-section showing the

interface between the multi-channel nanowire and the ALD SiO_2 gate oxide. A smooth surface with no evident roughness above ~ 1 nm can be observed.



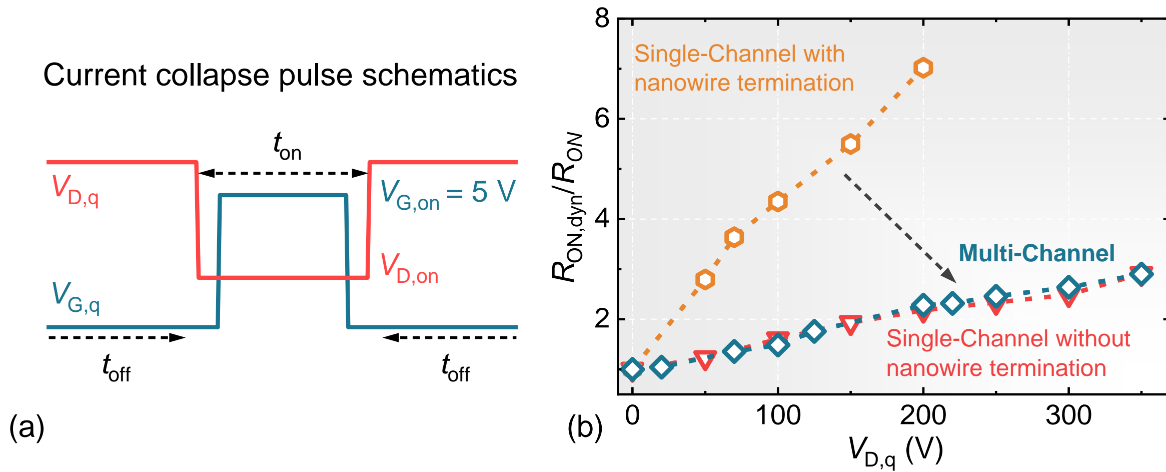
Extended Data Fig. 2. Threshold voltage in multi-channel nanowires. (a) The minimum nanowire width to achieve e-mode operation was extracted by employing the conductance method. The I-V characteristics of Fat-FET with different nanowire width (w_{NW}) was measured, from which the nanowire conductance (G_{NW}) was extracted. By linear fit of the G_{NW} versus w_{NW} plot, a nanowire sidewalls depletion (w_{Depl}) of 16.5 nm was calculated for gate voltage (V_G) of 0 V. As V_G increased, w_{Depl} decreased showing the effective gate control over the nanowire. (b)

The depletion width indicates the minimum nanowire width to achieve e-mode operation since for $w_{NW} < 2w_{Depl}$ the depletion regions from the two sidewalls merge in the center and eliminate the 2DEG. (c) It should be noted that while in general a much higher gate voltage is required to turn off a multi-channel nanowire with respect to a single-channel one due to its larger carrier density, for small nanowire widths such difference becomes smaller and multi-channel devices show very similar V_{TH} with respect to single-channel counterpart for w_{NW} below 50 nm, despite the much larger N_s. This is due to the predominant side gate control and to the strong sidewalls depletion at such narrow widths, which is similar for multi- and single-channel nanowires. (d) The evaluation of the sidewalls depletion width is consistent with the device transfer curves, which indicate 30 nm as the minimum nanowire width to achieve positive V_{TH}. To further shift V_{TH} to positive values, the conventional Ni-Au gate metal stack was replaced by a Pt-Au gate metal, which resulted in a threshold voltage increase of about 0.5 V. Such improvement, which is consistent for different w_{NW}, derives from the higher work-function of Pt with respect to Ni and allows to increase V_{TH} without any degradation of the channel, resulting in large V_{TH} of 0.85 V for 15 nm-wide nanowires.



Extended Data Fig. 3. Threshold voltage stability. (a) Schematics of the gate lag measurement employed to determine the device V_{TH} stability. First, the device is stressed for a time t_{off} = 5 ms during which a quiescent gate voltage $V_{G,q}$ is applied to cause trapping in the gate stack. The quiescent drain voltage $V_{D,q}$ is 0 V to avoid any drain lag contribution or device heating. Then the gate voltage V_G is set to 7 V and the drain voltage V_D to 1 V for a short time t_{on} = 5 μs, during which the drain current (I_D) is measured. Trapping in the gate stack and instability of the device V_{TH} result in a variation of the measured I_D depending on the value of the applied $V_{G,q}$. (b) Gate lag measurement as a function of $V_{G,q}$ for the presented multi-channel devices, and for a reference single-channel device having similar V_{TH}. The measured I_D has been normalized to the value obtained at $V_{G,q}$ = 7 V, i.e. when the gate voltage is kept constant and thus no stress is applied. A negligible gate lag effect is observed for the multi-channel devices with a current reduction of less than 4 % in the whole measurement range, which proves their excellent V_{TH} stability. Moreover, multi-channel devices show much-reduced gate lag with respect to the single-channel references, which instead present a current decrease of 20 % at $V_{G,q}$ of -3 V. Such behavior is due to the multi-channel larger carrier concentration which results in a weaker influence of the traps in the gate dielectric on the device V_{TH}. (c) V_{TH} as a function of temperature

(T) for the presented multi-channel devices. A very constant V_{TH} behavior can be observed in the whole measurement range up to 150 ºC with the device maintaining full E-mode operation and showing only a minor V_{TH} shift of 50 mV.



Extended Data Fig. 4. Current collapse in multi-channel tri-gate HEMTs. (a) Schematics of the double pulse measurement employed to determine the device current collapse. The device is first stressed in the off-state for a time t_{off} = 5 ms at a large quiescent drain bias $V_{D,q}$, and then it is suddenly turned on for a short time t_{on} = 50 µs during which its on-resistance is measured. (b) Normalized $R_{ON,dyn}$ as a function of $V_{D,q}$ for the multi-channel devices and for two different single-channel reference devices, co-fabricated in the same batch, with 1) gate termination in the nanowire region and same design with respect to the multi-channel case 2) gate termination on the planar region as for conventional single-channel device architectures. All devices present a low-pressure chemical vapor deposition (LPCVD) Si_3N_4 passivation layer. Single-channel devices with the gate termination in the nanowire region show a highly degraded $R_{ON,dyn}$ as a

consequence of the increased surface area at the nanowire sidewalls, which result in more severe electron trapping during the off-state stress. This is not the case, instead, for multi-channel devices, whose much larger carrier density (N_s) and 3D structure significantly reduce the virtual gate effect due to sidewalls traps. Most importantly, multi-channel devices show very similar performance with respect to conventional single-channel devices with gate termination on the planar region, which represents the optimal architecture for such single-channel heterostructures. This demonstrates that multi-channel devices can be effectively passivated despite their 3D architecture and can provide not only outstanding DC performance but also excellent dynamic behavior.