Performance of GaN Power Devices for Cryogenic Applications down to 4.2 K

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Abstract- **Gallium nitride (GaN) power devices are employed in an increasing number of applications thanks to their excellent performance. Nevertheless, their potential for cryogenic applications, such as space, aviation, and superconducting systems, has not yet been fully explored. In particular, little is known on the device performance below liquid nitrogen temperature (77 K) and the behavior of popular GaN architectures such as Gate Injection Transistor (GIT) and Cascode below room temperature has not yet been reported. Most importantly, it is still unclear how the different device loss contributions, i.e. conduction, soft- and hard-switching losses, change at cryogenic temperatures. In this work, we investigate and compare the performance of four GaN commercial power devices in a wide temperature range between 400 K and 4.2 K. All of the tested devices can successfully operate at cryogenic temperature with an overall performance improvement. However, different GaN HEMT technologies lead to significant variations in device gate control and loss mechanisms, which are discussed based on the device structure. The presented results prove the promising potential of the GaN technology for low-temperature applications and provide precious insights to properly design power systems operating under cryogenic temperatures and maximize their efficiency.**

Index terms- **Gallium Nitride, HEMTs, cryogenic temperature, low-temperature power electronics**

I. Introduction

Gallium Nitride (GaN) High-Electron-Mobility Transistors (HEMTs) have emerged as a promising technology for power conversion thanks to their excellent performance [1], [2]. However, while the potential of such devices in power electronic circuits has been the focus of an extensive research effort, typical characterizations occur at room temperature or, at most, up to 150°C. Yet, numerous applications require the power devices to effectively operate between room temperature down to extreme cryogenic temperatures of ~ 4 K. Some of the most interesting examples are found in the space and aviation domain [3], [4], and in superconducting machines such as superconducting magnets, energy storage systems and superconducting motors [4]–[6]. While for such applications the power systems are typically thermally insulated and maintained at room temperature, this greatly increases their cost, size, and complexity. It would thus be highly beneficial to operate the power converter at cryogenic temperature, which however requires a clear understanding of the power devices' behavior in such conditions.

This work was supported in part by the European Research Council under the European Union's H2020 program/ERC Grant Agreement No. 679425, in part by the Swiss National Science Foundation under Assistant Professor (AP) Energy Grant PYAPP2_166901, and in part by the Swiss Office of Energy (SFOE) Grant Number SI501887-01 (MEPCO). Authors are with the Power and Wide-Band-Gap Electronics Research Laboratory, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland (e-mail: luca.nela@epfl.ch, nirmana.perera@epfl.ch, catherine.erine@epfl.ch, elison.matioli@epfl.ch).

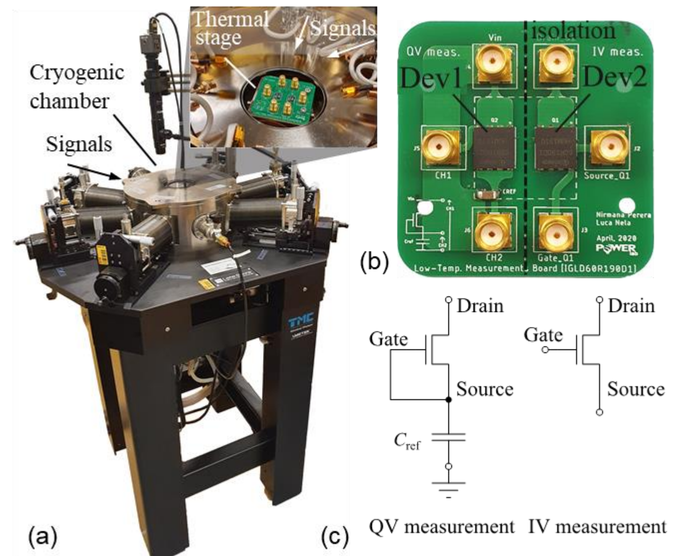

Fig. 1. (a) Cryogenic probe station used for the device characterization. The inset shows the testing PCB mounted on the probe station thermal stage (b) Two identical devices were mounted on the same PCB to allow their switching and DC characterization according to the circuit schematics shown in (c)

Typical Si and SiC power devices, along with emerging GaN vertical devices, rely on doping of the semiconductor material and show two main effects as the operating temperature is decreased [4], [7], [8]. On the one side, the carrier mobility increases due to the reduced electron-phonon interaction, which is highly beneficial for device performance. On the other side, however, the freeze-out of dopants results in a decrease of the carrier density, leading to a positive shift of the threshold voltage and increased channel resistance. The predominant effect depends on the exact operating temperature but their partial compensation leads to Si and SiC power devices that present, depending on the particular device structure, only a mild improvement or even degradation of the low-temperature performance [4]. GaN HEMTs, instead, do not require any doping to achieve a large concentration of electrons in the channel as the carriers are generated by the polarization mismatch between the AlGaN barrier and the GaN layer [9]. Since this phenomenon is independent of temperature, GaN HEMTs benefit from the increased carrier

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Index	Producer	Name	Gate technology	R_{ON} [mΩ]	V_{DS} [V]	Q_{oss} [nC]
T1	GaN Systems	GS66502 B	Schottky *p*-GaN	200	650	16
T2	Transphorm	TPH3206 PSB	Cascode	150	650	44
T3	Panasonic	PGA26E1 9BA	Ohmic *p*-GaN (GIT)	140	600	17
T4	Infineon	IGLD60R 190D1	Ohmic *p*-GaN (GIT)	140	600	16

Table. 1. Devices investigated in this work and their typical ratings reported in the datasheet. Q_{oss} is extracted for V_{DS}=400 V.

mobility at low temperatures, without suffering any carrier freeze-out.

Despite the promising potential of the GaN technology for cryogenic applications, very few works have investigated the performance of GaN HEMTs in such conditions. In particular, some interesting papers have focused on the characterization of a single commercial device (e.g. GaN Systems [10] and EPC [11]), confirming a significant performance improvement. However, these studies were typically performed down to 77 K, leaving the large temperature range below this value unexplored. Moreover, the low-temperature performance of common GaN HEMT architectures, such as Gate Injection Transistor (GIT) and Cascode, has never been reported, posing questions on their behavior in such conditions. Finally, it is still unclear how the device conduction, soft- and hard-switching losses vary at cryogenic temperature and which contribution becomes dominant.

In this work, we characterize and compare the performance of four GaN commercial power devices based on the most common device technologies, i.e. *p*-GaN Schottky gate, GIT and Cascode, in the wide temperature range between 400 K and 4.2 K. The different losses contributions (conduction, hard- and soft- switching) as well as the device gate control are analyzed and compared as a function of temperature. Significant variations are observed depending on the technology considered, which are discussed and explained based on the device architecture. The presented results clearly show the potential of GaN power devices at cryogenic temperatures and provide insightful guidelines for the design of power converters operating in such conditions.

II. Experimental Setup

The device characterization was performed in a Lakeshore CPX-VF cryogenic probe station (Fig. 1 (a)). Two identical transistors were soldered on a PCB (Fig. 1 (b)) and mounted on the probe station thermal stage, whose temperature (T) was varied between 400 K and 4.2 K. Liquid helium refrigerant was used to lower the stage temperature, which was controlled by a PID feedback loop for optimal stabilization within 0.1 K. The measurements were performed under vacuum conditions (10^{-4} mbar at 300 K) to avoid any condensation. Two transistors were used to provide the device DC and switching characterization simultaneously. The gate and source terminals of one device were shorted and a 10 nF (C0G multi-layer ceramic) capacitor C_{ref} was added to perform Sawyer-Tower (ST) measurements [12] to determine the device switching losses (Fig. 1 (c)). The input sinusoidal voltage was provided by a 33600A Keysight waveform generator and amplified by a WMA-300 Falco Systems high-voltage amplifier. The voltage signals were read by an MDO3104 Tektronix oscilloscope. It should be noted that the C_{ref} value was monitored with temperature and showed no variation. The three terminals of the other transistor were individually connected to a Keysight B1505 analyzer to perform the DC characterization of the device (Fig. 1 (c)). Four commercial devices (DUTs) presenting similar current and voltage ratings but different device technology were characterized and compared (Table 1). While the presented results shed light on the main device trends in a wide temperature range, which depend on the physical properties of the different GaN HEMTs investigated, further statistical analysis on a large number of devices may be necessary to determine precise low-temperature specifications.

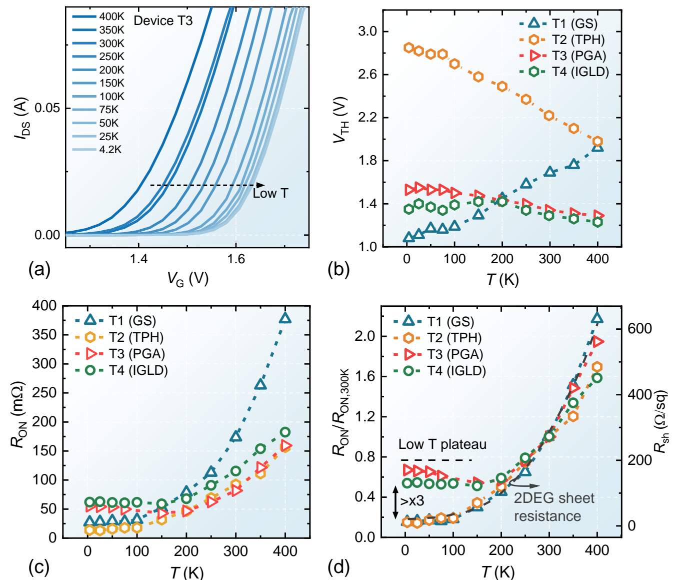

Fig. 2 (a) Transfer characteristics for T3 from 400 K to 4.2 K (b) V_{TH} as a function of temperature for the four DUTs. V_{TH} was uniformly defined at a drain-to-source current of 1 mA (c) Comparison of the devices on-resistance as a function of temperature (d) Normalized R_{ON} with respect to the room temperature value for the four DUTs. The right y-axis shows the typical temperature dependence of the 2DEG sheet resistance (R_{sh}).

III. Results and Discussion

A. Gate Control mechanisms and Conduction losses

Figure 2 (a) shows the GIT T3 transfer curve as a function of temperature, from which a noticeable positive shift of the characteristic is observable. The device threshold voltage (V_{TH}) was extracted at a drain-to-source current (I_{DS}) of 1 mA, as suggested in the datasheet, and compared with the one from the other HEMTs technologies. A significant discrepancy between the devices in the value and behavior of V_{TH} versus T is observed (Fig. 2 (b)). GIT devices (T3 and T4) present a quite constant but slowly increasing V_{TH} as the temperature is decreased, with the smallest variation among all of the devices, which confirms the excellent V_{TH} stability of such technology [13]. T2 shows, instead, a large increase of the threshold voltage at cryogenic temperatures, which well agrees with the

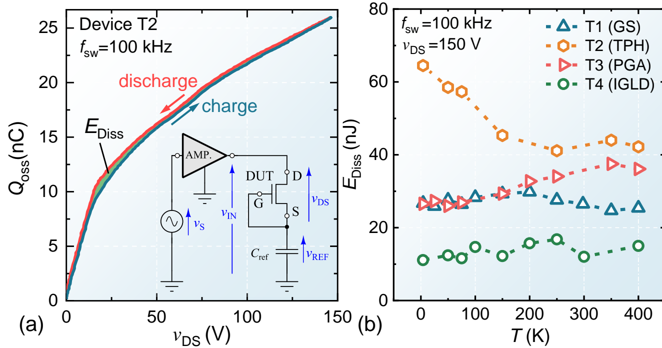

Fig. 3. (a) Sawyer-Tower measurement for T2. The circuit schematics of the measurement setup is shown in the bottom right inset. (b) E_{Diss} as a function of temperature for the four DUTs.

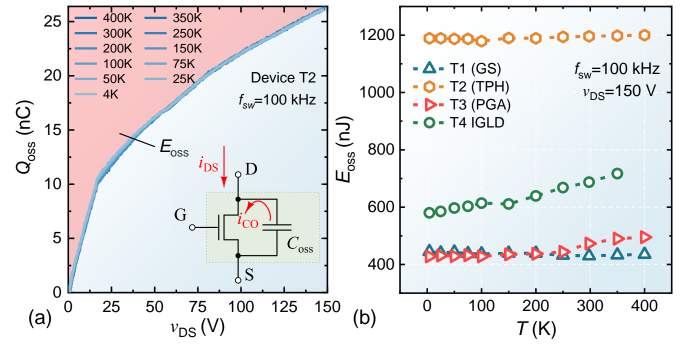

Fig. 4. (a) E_{oss} extraction from the Q_{oss} versus v_{DS} characteristic. In the bottom right inset, the circuit schematics of a device under hard-switching operation is shown. (b) E_{oss} as a function of temperature for the four DUTs

behavior of the Si device employed to achieve enhancement-mode operation. However, thanks to the gate robustness of such architecture, cascode devices can be driven with large gate voltages (V_G), allowing to compensate the V_{TH} drift by increasing the driving V_G. On the other side, T1 presents a significant V_{TH} decrease from 1.6 V at room temperature (RT) down to ~1 V at 4.2 K. Such effect, which is consistent with Ref. [10], should be carefully considered when designing the gate driving system as the reduced off-state margin may result in dangerous false turn-on events.

Figure 2 (c) illustrates the behavior of the DUTs on-resistance (R_{ON}) as a function of temperature. Thanks to the electron mobility (μ) increase, all of the transistors show a considerable R_{ON} reduction as the temperature is decreased. This is followed by a plateau region for lower T due to the μ saturation as a consequence of crystal defects. Yet, while the trend is similar for all of the devices, the amount of such reduction strongly depends on the HEMT technology, which can be better appreciated by considering the normalized R_{ON} value to the room temperature one (Fig. 2 (d)). T1 and T2 show a very large R_{ON} decrease of ~ 6 times with respect to the RT value, with the onset of the low-temperature plateau region around 100 K. Such a trend agrees well with the sheet resistance (R_{sh}) reduction of the AlGaN/GaN two-dimensional electron gas (2DEG) as a result of the carrier mobility increase. On the other hand, the two GIT devices present only a ~ 2-fold R_{ON} reduction at cryogenic temperatures and show a premature onset of the low-temperature plateau. This behavior may be due to the introduction of defects in the gate region during the AlGaN partial recess, which limits the low-temperature mobility. Such diverse behavior among different technologies directly reflects on the device conduction losses and driving circuit, and should be carefully taken into account when choosing the most suitable power transistor for low-temperature applications.

B. Switching losses

Depending on the operation conditions of the circuit, power devices are subjected to either soft- or hard- switching losses. While these loss mechanisms are broadly studied at RT conditions, their behavior at cryogenic temperature is yet to be fully investigated.

In particular, soft-switching losses occur due to the non-ideal charging and discharging of the device output capacitance (C_{oss}) and become relevant in high-frequency power electronic circuits, such as resonant and quasi-resonant converters [14]. Soft-switching losses are typically characterized by a Sawyer Tower measurement (Fig. 3 (a)), which allows to determine the discrepancies between the C_{oss} charging and discharging processes. To this end, the transistor source and gate terminals were shorted and a reference linear capacitor (C_{ref}) was introduced between the source of the device and the circuit ground. By applying a large-signal sinusoidal input voltage (v_{IN}) and measuring the voltage over the reference capacitor (v_{REF}), the transistor output charge (Q_{oss}) versus drain-to-source voltage (v_{DS}) was obtained. It was thus possible to extract the energy dissipated at each switching cycle (E_{Diss}) by considering the hysteresis loop between the charging and discharging paths (Fig. 3 (a)). An important feature of this technique is represented by the use of a purely sinusoidal excitation, which avoids the use of signals containing higher frequency harmonics (e.g. square waves). This allows to accurately characterize the DUTs inside the cryogenic chamber at frequencies in the range of several hundreds of kHz despite the long interconnections required in such measurement.

The value of E_{Diss} as a function of temperature for four DUTs is shown in Fig. 3 (b), where different trends can be observed. While T1 shows quite independent behavior in temperature, T3 presents about a 30 % decrease in E_{Diss} at 4.2 K with respect to the RT value. T2 displays, instead, a significant increase of more than 70 % of the RT value. Finally, T4 exhibits relatively small E_{Diss} values, within the measurement setup accuracy (estimated to be ±5 nJ), and thus will not be considered. It should be noted that the variation of the soft-switching losses does not agree with any channel dependencies reported in Fig. 2. This confirms the recently proposed theories [15]–[17] in which the causes of soft-switching losses are attributed to the GaN resistive buffer and the Si substrate, rather than to the channel properties or the presence of stray charges (as for Super Junction Si devices). The consistent E_{Diss} increase for T2 may be due to the more efficient electron trapping in the GaN buffer at low temperatures [15]. However, the different behavior among the DUTs suggests that such mechanisms strongly depend on the exact energy level of the trapping sites. Since each manufacturer typically employs a custom epi-

Device	$R_{ON,RT}$ [mΩ]	$R_{ON,4K}$/ $R_{ON,RT}$	$E_{Diss,RT}$ [nJ]	$E_{Diss,4K}$/ $E_{Diss,RT}$	$E_{oss,RT}$ [nJ]	$E_{oss,4K}$ / $E_{oss,RT}$
T1	200	0.14	27	1	430	1
T2	150	0.15	42	1.73	1196	1
T3	140	0.66	35	0.76	473	0.9
T4	140	0.54	-	-	687	0.85

Table. 2. Comparison of R_{ON}, E_{Diss}, and E_{oss} at 300 K and 4.2 K for the DUTs.

structure, the switching loss values and temperature behavior are expected to vary significantly according to the exact GaN buffer composition and Si substrate choice. It is however possible to safely assume that soft-switching losses present a weaker temperature dependence with respect to conduction losses.

Hard-switching losses occur when a transistor is switched on while it still holds a large voltage at its drain-to-source terminals. Standard methods to evaluate these losses are based on a double-pulse test (DPT) circuit [18], [19]. Nevertheless, such a technique is very challenging at cryogenic temperatures due to the long wiring required to connect the device inside the cryogenic chamber [10], which has a significant impact on the measurement accuracy. It is however possible to draw important conclusions on the temperature behavior of hard-switching losses by exploiting the presented results, without the use of a DPT measurement.

While hard-switching losses comprise a turn-on and turn-off loss term, turn-off losses can typically be neglected for GaN devices due to their large transconductance and dv/dt capability [20], [21]. The main hard-switching losses contribution is thus represented by turn-on losses, which can be expressed as a sum of two terms [18], [19]:

$$P_{sw,hard} = f \times E_{oss} + P_{VI}\left(g_m\right) \quad (1)$$

where f is the switching frequency, E_{oss} is the energy stored in the transistor output capacitance at a certain off-state v_{DS} value (Fig. 4 (a)) and P_{VI} is the loss term associated with the external load current flowing from the circuit through the device channel during the discharging of C_{oss}. Figure 4 (a) shows the extraction of the device E_{oss} values for different temperatures, obtained from the integration of the transistor Q_{oss} versus v_{DS} curve. A comparison of E_{oss} as a function of temperature for the four DUTs is shown in Fig. 4 (b). T1 and T2 present a very constant E_{oss} value throughout the whole temperature range, which is in agreement with the temperature-independent behavior of the 2DEG concentration. On the other hand, T3 and T4 show a mild E_{oss} decrease to about 90 % of the RT value at 4.2 K. The contribution of E_{oss} to hard-switching losses is thus quite constant in a wide temperature range. On the other hand, the second term in (1), P_{VI}, is proportional to the external load current and is linked to the time required to discharge C_{oss} through the device channel by the current i_{CO} (inset in Fig. 4 (a)). The discharging time strongly depends on device trans-conductance g_m, which increases significantly with decreasing temperature [18] due to its linear dependence on the carrier mobility (Fig. 2 (c-d)). Hence, while the E_{oss} contribution is fairly independent of temperature, the value of the P_{VI} term decreases considerably at cryogenic conditions with a behavior similar to what is shown in Fig. 2 (d). Hard-switching losses thus decrease at low temperatures with a reduction becoming more pronounced as the load current increases.

Overall, some important trends in the different losses contributions at cryogenic temperatures can be identified (Table 2). Conduction losses show the most significant decrease, which is larger (~6x) for conventional HEMT technologies (T1 and T2) with respect to the GIT devices (~2x). Soft-switching losses present a weaker temperature dependence without any common trend between the different technologies. For hard-switching losses, while the E_{oss} component demonstrated to be temperature insensitive, the total loss value decreases due to the enhanced device g_m. Thus, while the precise improvement depends on the circuit operation, GaN power devices show much-enhanced efficiency at cryogenic temperatures.

IV. Conclusion

In this work, we characterized and compared the performance of the most common GaN commercial power devices in a wide temperature range between 400 K and 4.2 K. All of the tested devices can successfully operate at cryogenic temperature with an overall performance improvement. However, the different GaN HEMT technologies lead to significant variations in the device gate control and loss mechanisms, which have been explained according to the device structure. The presented results prove the promising potential of the GaN technology for low-temperature applications and provide the circuit designers with precious insights to maximize converters' efficiency in such conditions.

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