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High-Speed ADC Design and Optimization for Wireline Links

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To my family...

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Abstract

The ever-growing global internet traffic has increased demand for higher speed data transmission. As the bandwidth requirements of wireline links increase, extensive digital equalization techniques are required to compensate for the high-frequency channel loss. Analog-to-digital converter (ADC) based links consisting of high-speed ADCs and digital signal processors enable the implementation of powerful equalization algorithms in the digital domain. Such systems are implemented using advanced technology nodes to benefit from the power and area advantages that the advanced technology nodes provide for the digital blocks. In addition to the speed, the power efficiency and the compatibility with technology scaling are important parameters in the design of ADCs used in such systems. Successive approximation register (SAR) ADCs have become a popular choice in wireline applications because of their power efficiency and compatibility with advanced technology nodes due to consisting of mostly digital blocks.

This thesis focuses on high-speed SAR ADC design techniques to improve both conversion speed and power efficiency. First, a single-channel asynchronous SAR ADC design using a single comparator is presented to find out the achievable sampling rate with only one comparator. The 9-bit asynchronous SAR ADC prototype in 65 nm CMOS achieves 47.6 dB SNDR and 29.6 fJ/conv.-step figure-of-merit near Nyquist frequency at 222 MS/s and occupies an area of 0.017 mm^2. Then, the use of comparator delay information for quantization is analyzed and a self-calibrated delay-based least significant bit extraction circuit, which achieves 3.35 dB SNDR for a 9-bit 200 MS/s with insignificant degradation in power consumption, speed, and area, is presented.

Next, loop-unrolled (LU) SAR ADC topology, which uses multiple comparators to improve the SAR loop delay, and comparator offset calibration techniques in LU-SAR ADCs are reviewed. Common-mode voltage variation in LU-SAR ADCs due to comparator kickback and the common-mode dependency of the comparator offset are addressed. A common-mode adaptive background offset calibration for LU-SAR ADCs is proposed. The proposed calibration scheme ensures that the comparators are calibrated at the same input common-mode voltage at which they each operate during the SAR conversion to prevent the common-mode dependent offset mismatch between the comparators. Besides, the common-mode variation immunity of the proposed calibration scheme is exploited to optimize the figure-of-merit of

the LU-SAR ADC. The prototype 8-bit LU-SAR ADC manufactured in 28 nm FDSOI achieves 42.57 dB SNDR and 22.8 fJ/conv.-step figure-of-merit at 800 MS/s with near Nyquist frequency input and occupies an area of only 0.0037 mm^2.

Lastly, an ADC-based receiver analog front-end (AFE) design in 28 nm FDSOI is presented and the feasibility of high order pulse amplitude modulation (PAM) is examined for a moderate-loss channel. The high order PAM compatible ADC-based AFE consists of a continuous-time linear equalizer and an 8 GS/s 8-way time-interleaved 7-bit SAR ADC with an embedded 2-tap feed-forward equalizer. All the equalization is implemented in the analog domain to avoid the circuit complexity and high power consumption of the digital equalization with high order modulation. The ADC-based AFE consumes 49.36 mW at 8 Gbaud, which corresponds to 1.54 pJ/bit at 32 Gb/s with PAM-16 and 2.06 pJ/bit at 24 GS/s with PAM-8.

Keywords: Analog-to-digital converter, ADC, successive approximation register, SAR, asynchronous clocking, loop-unrolling, offset calibration, time-interleaving, ADC-based receiver, wireline links, pulse amplitude modulation, PAM, feed-forward equalizer, FFE.

Résumé

Le trafic internet mondial en constante augmentation a accru la demande de transmission de données à plus grande vitesse. À mesure que les besoins en bande passante des liaisons filaires augmentent, des techniques d'égalisation numérique extensives sont nécessaires pour compenser la perte de canal haute fréquence. Les liaisons basées sur un convertisseur analogique-numérique (CAN) composées de CAN à grande vitesse et de processeurs de signaux numériques permettent la mise en œuvre d'algorithmes d'égalisation puissants dans le domaine numérique. De tels systèmes sont mis en œuvre à l'aide de nœuds de technologie avancée pour bénéficier des avantages de puissance et de surface que les nœuds de technologie avancée fournissent pour les blocs numériques. Outre la vitesse, l'efficacité énergétique et la compatibilité avec la mise à l'échelle de la technologie sont des paramètres importants dans la conception de CAN utilisés dans ces systèmes. Les CAN à registres d'approximation successifs (SAR) sont devenus un choix populaire dans les applications filaires en raison de leur efficacité énergétique et de leur compatibilité avec les nœuds de technologie de pointe en raison de leur composition principalement numérique.

Cette thèse se concentre sur les techniques de conception CAN SAR à haute vitesse pour améliorer à la fois la vitesse de conversion et l'efficacité énergétique. Tout d'abord, une conception CAN SAR asynchrone à canal unique utilisant un seul comparateur est présentée pour déterminer la fréquence d'échantillonnage réalisable avec un seul comparateur. Le prototype CAN SAR asynchrone 9 bits en CMOS 65 nm atteint un SNDR de 47,6 dB et un facteur de mérite de 29,6 fJ/conv.-step près de la fréquence de Nyquist à 222 MS/s et occupe une zone de 0,017 mm^2. Ensuite, l'utilisation des informations de retard du comparateur pour la quantification est analysée et un circuit d'extraction de bits les moins significatifs basé sur un retard auto-calibré, qui atteint 3,35 dB SNDR pour une résolution de 9 bits et une vitesse de 200 MS/s avec une dégradation insignifiante de la consommation d'énergie, de la vitesse et la surface, est présenté.

Ensuite, la topologie CAN SAR en boucle déroulée (LU), qui utilise plusieurs comparateurs pour améliorer le délai de boucle SAR, et les techniques d'étalonnage de décalage de comparateur dans les CAN LU-SAR sont examinées. La variation de tension en mode commun dans les CAN LU-SAR due au rebond du comparateur et à la dépendance de mode commun du décalage du comparateur est traitée. Un calibrage du décalage de fond adaptatif en mode

commun pour les CAN LU-SAR est proposé. Le schéma de calibration proposé garantit que les comparateurs sont calibrés à la même tension de mode commun d'entrée à laquelle ils fonctionnent chacun pendant la conversion SAR pour éviter le décalage dépendant du mode commun entre les comparateurs. En outre, l'immunité aux variations de mode commun du schéma d'étalonnage proposé est exploitée pour optimiser la figure de mérite du CAN LU-SAR. Le prototype de CAN LU-SAR 8 bits fabriqué en FDSOI 28 nm atteint un SNDR de 42,57 dB et un facteur de mérite par pas de 22,8 fJ/conv.-step à 800 MS/s avec une entrée de fréquence proche de Nyquist et occupe une zone de seulement 0,0037 mm^2.

Enfin, une conception de récepteur analogique frontal (AFE) basé sur CAN en 28 nm FDSOI est présentée et la faisabilité de la modulation d'impulsion en amplitude d'ordre élevé (PAM) est examinée pour un canal à perte modérée. L'AFE basé sur CAN compatible PAM d'ordre élevé se compose d'un égaliseur linéaire en temps continu et d'un CAN SAR 7 bits à 8 voies entrelacées 8 Géch/s avec un égaliseur à anticipation à 2 prises intégrés. Toute l'égalisation est mise en œuvre dans le domaine analogique pour éviter la complexité du circuit et la consommation d'énergie élevée de l'égalisation numérique avec une modulation d'ordre élevé. L'AFE basé sur CAN consomme 49,36 mW à 8 Gbauds, ce qui correspond à 1,54 pJ/bit à 32 Gb/s en PAM-16 et 2,06 pJ/bit à 24 GS/s en PAM-8.

Mots-clés : Convertisseur analogique-numérique, CAN, registre d'approximation successive, SAR, cadencement asynchrone, déroulement de boucle, étalonnage d'offset, entrelacement temporel, récepteur basé sur CAN, liaisons filaires, modulation d'amplitude d'impulsion, PAM, égaliseur par anticipation, FFE.

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1 Introduction

Global IP traffic has experienced massive growth in recent years. By 2022, the global IP traffic is expected to reach 4.8 zettabytes per year, which is nearly 11 times more than all IP traffic generated in 2012 [2]. This massive growth in IP traffic increased the demand for higher speed data transmission. Increasing the bandwidth to meet the demand for faster data transmission in wireline links increased the amount of channel-loss that needs to be equalized as well. As a result, circuit designers move from two-level pulse amplitude modulation (PAM-2) signaling, also known as non-return-to-zero (NRZ), to more spectrally efficient PAM-4 signaling [3, 4, 5, 6, 7, 8]. This way the Nyquist frequency is halved and the corresponding channel loss is decreased. However, PAM-4 is more sensitive to residual inter-symbol interference (ISI) because it has a smaller vertical opening. Therefore, it requires more robust equalizers with many number of taps. To perform complex equalization algorithms in the digital domain, implementations using an analog-to-digital converter (ADC) and a digital signal processor (DSP) have become more common [3, 4, 5, 6, 7, 8].

Figure 1.1 shows a block diagram of a wireline link that employs an ADC and DSP in the receiver side [9]. Employing DSP to implement the equalization algorithms in the digital domain provides various advantages. First, DSP has less sensitivity to process, voltage, and temperature (PVT) variations. Second, advanced technology nodes offer reduced power consumption and area advantage for DSP. Third, the DSP has the advantage of portability to new technology nodes. High-speed moderate resolution ADCs play an important role in ADC-based receivers. The ADC and the DSP in these systems are implemented on the same chip to avoid additional power consumption for transferring the ADC data to DSP. Therefore, the ADCs are implemented in the same advanced technology nodes as well.

Both ADC and DSP consume a significant amount of power in ADC-based designs [9]. Consequently, ADC-based receivers are less energy efficient compared to their mixed-signal counterparts [10]. Therefore, improving the energy efficiency of the ADC is desirable to improve the energy efficiency of the wireline links.

The resolution requirement of the ADCs used in ADC-based receivers is dependent on the

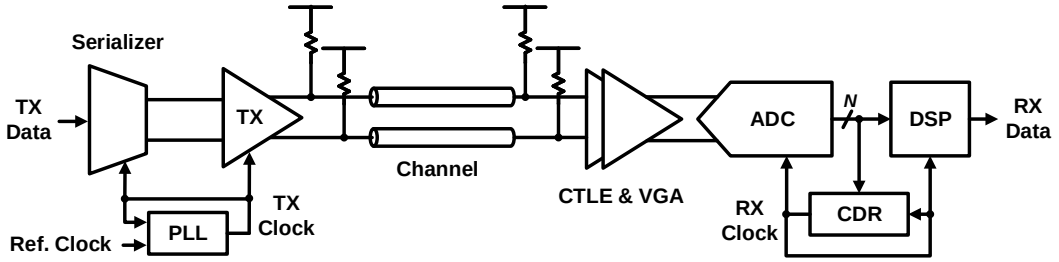


Figure 1.1: Block diagram of a wireline transceiver with an ADC-based receiver.

channel loss, equalization capability of the transmitter and receiver analog front-end, modulation order, and the targeted bit error rate (BER). Typical ADC resolution in PAM-4 ADC-based receivers is generally 6-8 bits [4, 5, 6, 7, 8, 11].

The need for medium-resolution ADCs operating at multi-GS/s sampling rates has increased with the use of ADC-based receivers. Time-interleaving is commonly employed to reach multi-GS/s sampling rates. The successive approximation register (SAR) ADC architecture has become a popular choice in time-interleaving, thanks to its energy efficiency and suitability to advanced technology nodes [12, 13, 14].

Figure 1.2, Figure 1.3, and Figure 1.4 are plotted using the data from ADC designs presented at the IEEE International Solid-State Circuits Conference (ISSCC) and the VLSI Circuit Symposium between 1997 and 2020 [1]. Figure 1.2 shows the improvement of energy per conversion of ADCs over the years. In the last two decades, energy per conversion has reduced significantly. The reason for such reduction is due to both technology scaling and architectural innovations. This plot shows the increasing popularity of SAR ADCs in the last decade and the energy efficiency of the SAR ADCs compared to other architectures. However, energy efficiency itself is not the only criterion for the choice of ADC architecture. Certain applications have certain resolution and sampling-rate requirements. Therefore, architectural comparison requires to examine these parameters as well. Figure 1.3 shows the energy efficiency versus SNDR plot and Figure 1.4 shows the Walden figure-fo-merit (FoM_W) versus sampling rate (f_s) plot for different ADC architectures. In Figure 1.3, SAR ADC designs achieves lower energy per conversion starting from low resolution to medium-to-high resolution. Some of the medium-to-high resolution SAR ADC designs achieve even lower than 10 fJ/conversion-step FoM_W. In Figure 1.4, from 1 MS/s to 90 GS/s, SAR ADC designs achieve significantly lower FoM_W compared to other architectures. As a result, SAR ADCs have become the architecture of choice in many different applications with their energy efficiency.

1.1 Thesis Goal

The goal of this thesis is to investigate the high-speed ADC design techniques, design, and implement a high-speed and low-power ADC with moderate-resolution for wireline applica-

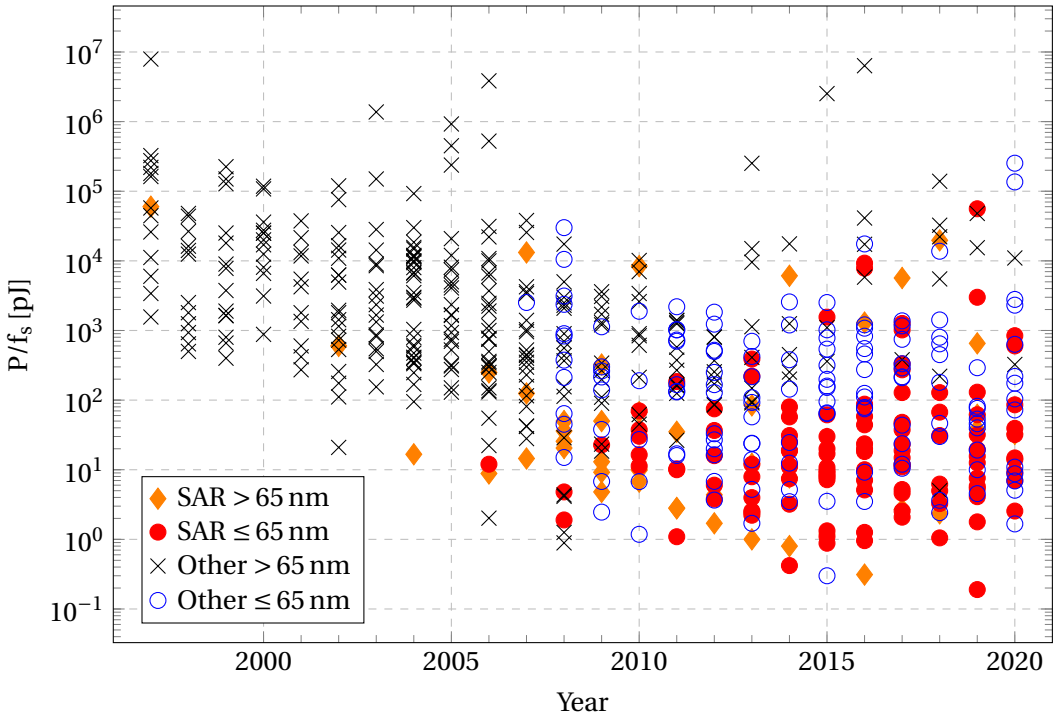


Figure 1.2: Energy efficiency trend of ADCs over the years [1].

tions. Considering the speed and energy efficiency advancements in SAR ADCs fueled by both technology scaling and new design techniques in recent years, the SAR architecture is chosen as the starting point.

1.2 Thesis Organization

Chapter 2 gives the theory review of the SAR ADCs. First, it explains the fundamentals of SAR ADCs and important ADC metrics. Then, gives a summary of the innovative design techniques that are used in state-of-the-art high-speed SAR ADC.

Chapter 3 presents an asynchronous SAR ADC design in 65 nm CMOS. A SAR ADC architecture with a single comparator is chosen as the starting point because it is relatively simple and does not require any calibration. The proposed 9-bit asynchronous SAR ADC design uses a combination of design techniques summarized in Chapter 2 to minimize the SAR loop delay and power consumption.

Chapter 4 presents a self-calibrated delay-based LSB extraction circuit for SAR ADCs. The proposed circuit can be implemented on a SAR ADC to improve the resolution without compromising the speed and with a negligible increase in power consumption and area.

Chapter 5 presents an 8-bit loop-unrolled SAR ADC design with common-mode adaptive background offset calibration in 28 nm FDSOI. Since the sampling-rate that can be achieved

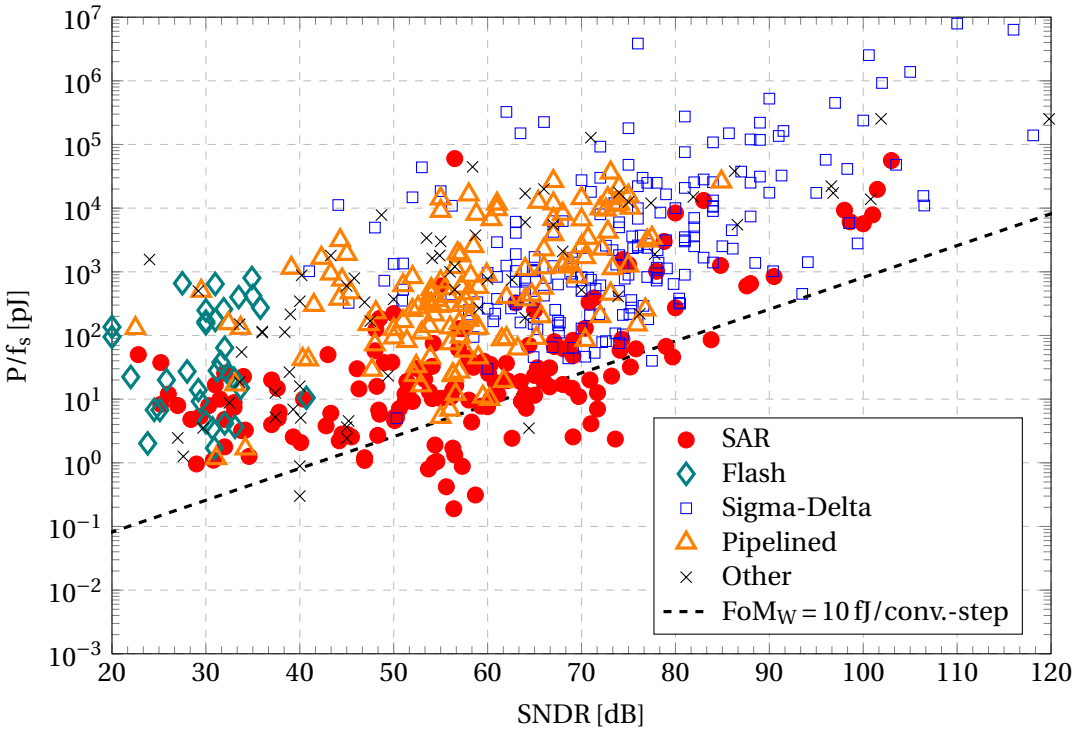


Figure 1.3: Energy efficiency versus SNDR plot for different ADC architectures [1].

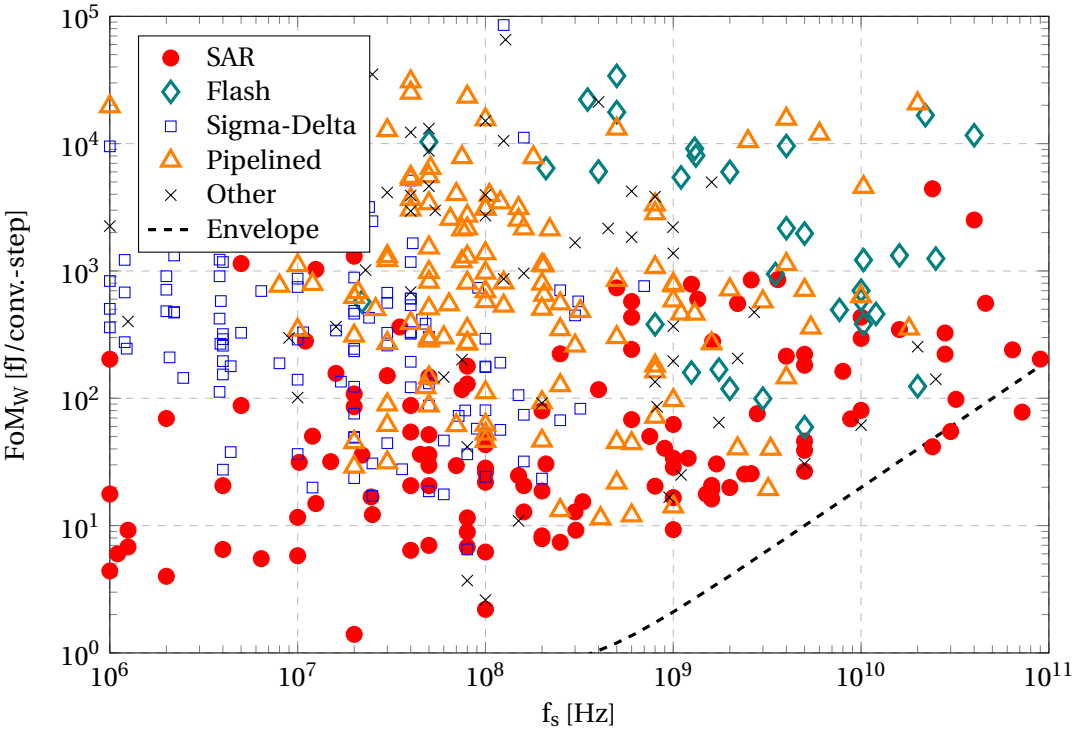


Figure 1.4: Walden FoM versus sampling rate plot for different ADC architectures [1].

using only one comparator is limited, the chapter focuses on the loop-unrolling technique which uses multiple comparators. In this chapter, the common-mode variation in loop-unrolled SAR ADCs and the common-mode mismatch between the comparators due to common-mode dependency of offset is addressed. To solve the addressed issues, a common-mode adaptive background offset calibration is proposed.

Chapter 6 presents an ADC-based receiver analog front-end design and examines the feasibility of high order PAM for moderate loss channel. The presented analog front-end consists of a CTLE and an 8×TI 7-bit SAR ADC with 2-tap embedded analog FFE. The details of the embedded FFE implementation are provided in the chapter.

Finally, conclusions are given and the future work is discussed in Chapter 7.

2 Overview

This chapter summarizes the error sources limiting ADC performance, lists important ADC metrics, reviews the recent innovations on high-speed ADC design.

2.1 ADC Errors

2.1.1 Quantization Noise

ADCs converts continuous-amplitude input signal into discrete values with quantization. Quantization noise due to the finite resolution N of an ADC limits the SNR of an ADC. Figure 2.1 shows the ideal input-output characteristic of a 3-bit ADC. For an ideal N-bit ADC, each quantization step is equal and given by

$$V_{LSB} = \frac{V_{FS}}{2^N}, \tag{2.1}$$

where V_{FS} is the full-scale analog input range. Quantization error is bounded by -V_{LSB}/2 and +V_{LSB}/2 for input voltages within the full-scale input range as shown in Figure 2.2. Average power of quantization noise is [15]

$$P_Q = \frac{V_{LSB}^2}{12} = \frac{V_{FS}^2}{2^{2N}.12}. \tag{2.2}$$

The signal-to-quantization noise ratio (SQNR) of an ideal N-bit quantizer with full-scale sinusoidal input signal is given by

$$SQNR_{dB} = 10\log\frac{P_{signal}}{P_Q} = 10\log\frac{\frac{V_{FS}^2}{8}}{\frac{V_{FS}^2}{2^{2N}.12}} = 6.02N + 1.76. \tag{2.3}$$

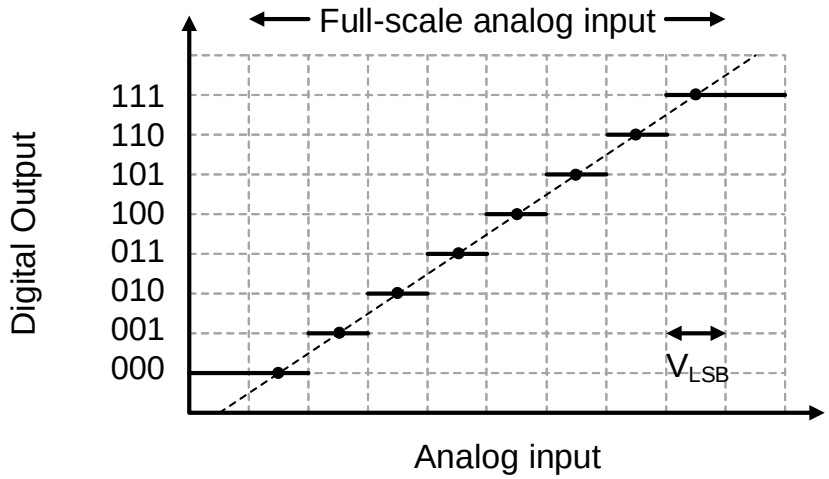


Figure 2.1: Ideal input-output characteristic of a 3-bit ADC.

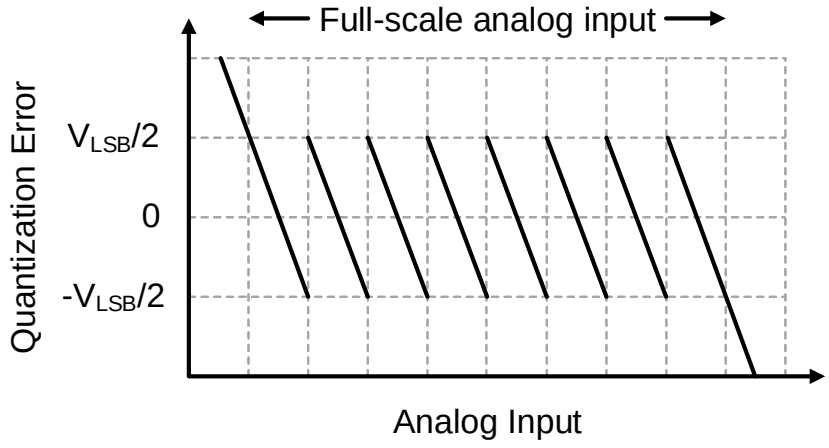


Figure 2.2: Quantization error of a 3-bit ADC.

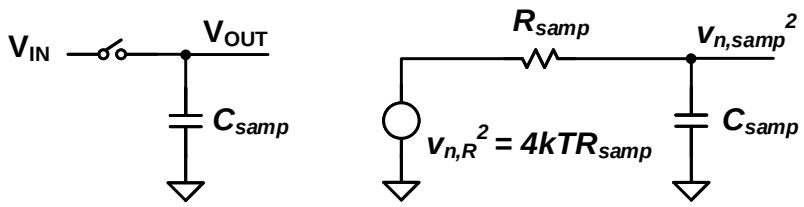


Figure 2.3: Simple sampler circuit and its noise equivalent.

2.1.2 Sampling Noise

Sampling noise is a fundamental limit in sampled-data systems. kT/C sampling noise occurs because of the thermal noise of the sampling switch. Figure 2.3 shows a simple sampler circuit and the equivalent circuit for the noise estimation. The thermal noise of the equivalent sampling resistor $4kTR_{samp}$ is multiplied by the square of the transfer function to find the noise spectrum across the sampling capacitor as

$$v_{n,samp}^2(f) = \frac{4kTR_{samp}}{1+\left(2\pi f R_{samp}C_{samp}\right)^2}. \tag{2.4}$$

The total noise power stored on the sampling capacitor is calculated by the integral of Equation 2.4 over all the folded bands as [16]

$$P_{n,samp} = \int_0^\infty \frac{4kTR_{samp}}{1+\left(2\pi f R_{samp}C_{samp}\right)^2} df. = \frac{kT}{C_{samp}}. \tag{2.5}$$

$P_{n,samp}$ is independent from R_{samp}. As R_{samp} increases, the white noise floor increases as well. But $P_{n,samp}$ is not effected since the bandwidth of the low-pass filtering decreases as well. Therefore, this noise is commonly referred to as kT/C noise.

For example, for V_{FS} = 500 mV at 100 C, if the kT/C sampling noise is equal to the quantization noise, the total sampling capacitance should be 256 fF for a 10-bit ADC and 16 fF for an 8-bit ADC. Having the kT/C noise equal to the quantization noise means SNR decreases by 3 dB.

2.1.3 Sampling Jitter

The maximum SNR value that an ADC can achieve with RMS timing jitter of σ_{jitter} is given by

$$\text{SNR}_{\text{jitter,dB}} = 20\log\frac{1}{2\pi \text{f}_{\text{in}}\sigma_{\text{jitter}}}, \tag{2.6}$$

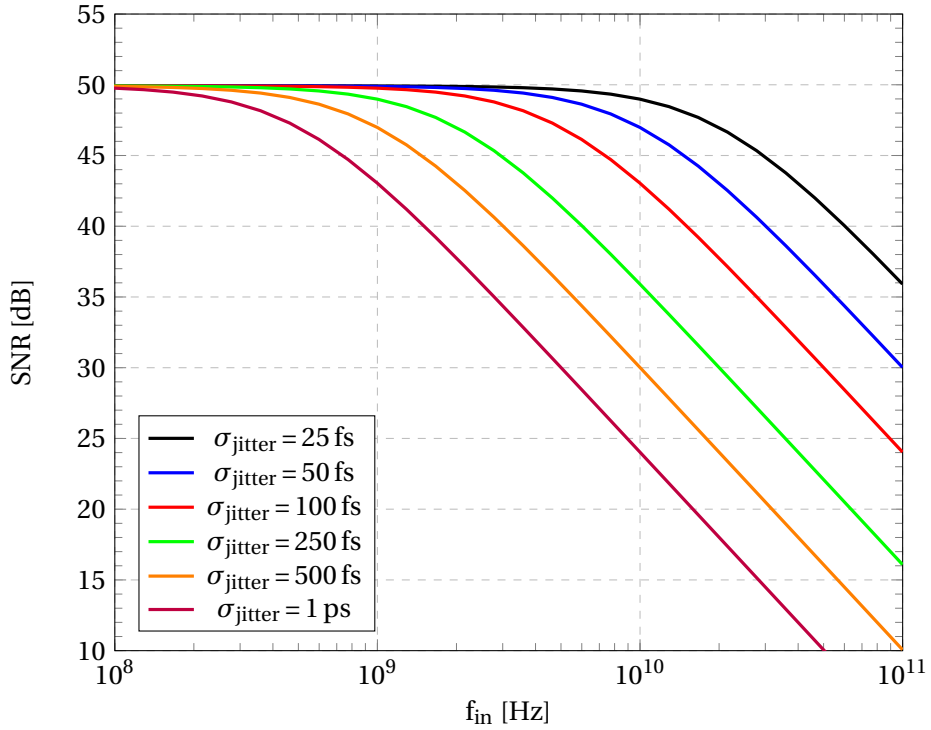


Figure 2.4: SNR vs. input frequency plot of an 8-bit ADC with only the effect of jitter included.

where f_{in} is the frequency of the sinusoidal input signal.

SNR of an N-bit ADC with only the effect of jitter can be calculated by adding the quantization noise in addition to the power of jitter as

$$SNR_{jitter,N-bit,dB} = -10\log\left(\frac{2}{3.2^{2N}} + \left(2\pi f_{in}\sigma_{jitter}\right)^2\right). \tag{2.7}$$

The corresponding SNR versus input frequency plot for an 8-bit ideal ADC is provided in Figure 2.4 for various RMS jitter values.

2.2 ADC Performance Metrics

Several terms, which are used in other chapters in this thesis to characterize the ADC performance are defined in this section.

Sampling rate (f_s) is the rate at which the ADC converts the analog input into a digital output. It is also referred to as sampling frequency. The unit of sampling rate is samples per second (S/s).

Resolution (N) is the number of bits that corresponds to the 2^N different quantization levels

of the ADC.

Signal-to-noise ratio (SNR) is the ratio between the signal power and the total noise power including the quantization noise and the noise of the circuit and expressed as

$$\mathrm{SNR_{dB}} = 10\log\frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}}}. \tag{2.8}$$

Signal-to-noise-and-distortion ratio (SNDR) is the ratio between the signal power and the total power of noise and distortion and expressed as

$$\mathrm{SNDR_{dB}} = 10\log\frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}} + \mathrm{P_{distortion}}}. \tag{2.9}$$

It is a commonly used metric to describe the effective resolution of the ADC. It is commonly expressed in dB.

Spurious free dynamic range (SFDR) is the ratio of the carrier signal power to the power of the highest spurious signal in the output.

Effective number of bits (ENOB) is derived from the SNDR, as

$$\mathrm{ENOB} = \frac{\mathrm{SNDR_{dB}} - 1.76\,\mathrm{dB}}{6.02\,\mathrm{dB}}. \tag{2.10}$$

Generally, it is derived from the peak SNDR value or when a full-scale input signal is applied to the ADC.

Figure-of-merit (FoM) is a metric that is commonly used to compare the performance of an ADC. ADCs have many different performance metrics related to speed, resolution, and power. FoM combines several performance metrics into a single number. There are two commonly used FoM expressions for ADCs: Walden FoM [17] and Schreier FoM [18]. Walden FoM is more commonly used for low-to-medium resolution ADCs while the Schreier FoM for high-resolution ADCs. Walden FoM is expressed as

$$\mathrm{FoM_W} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}}\,\mathrm{f_s}}. \tag{2.11}$$

The unit of Walden FoM is joules per conversion-step (J/conv.-step). The lower the Walden FoM, the better the ADC performance. In this thesis, FoM refers to the Walden FoM.

Differential non-linearity (DNL) is used to measure the deviation of the analog input range from the ideal LSB voltage as shown in Figure 2.5. DNL is calculated after gain and offset

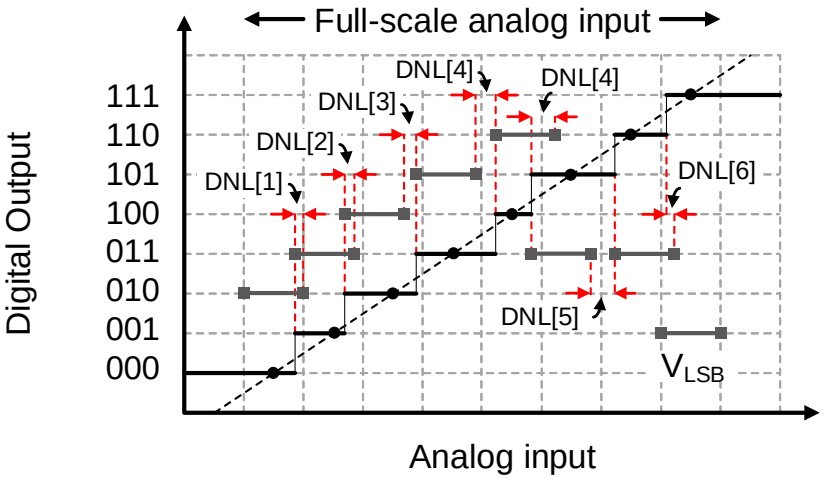


Figure 2.5: DNL of a 3-bit ADC.

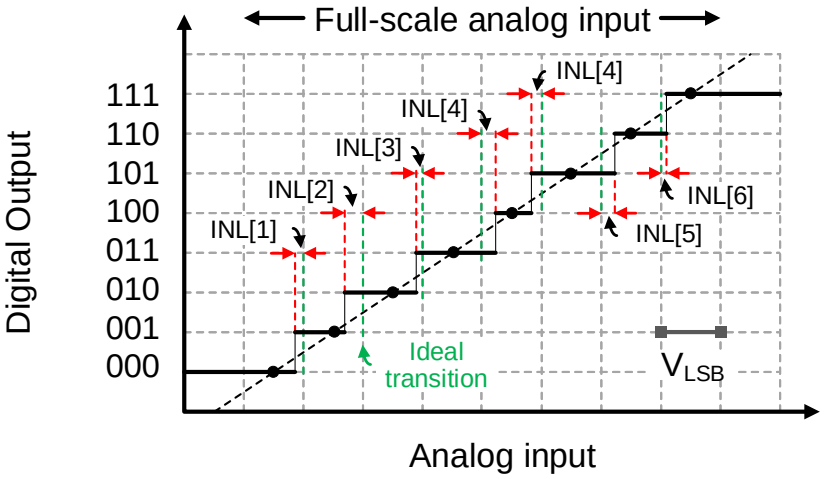


Figure 2.6: INL of a 3-bit ADC.

correction. DNL[i] which corresponds to the i th ADC output code is calculated as

$$\mathrm{DNL}[i] = \frac{\mathrm{V}[i+1] - \mathrm{V}[i]}{\mathrm{V_{LSB}}} - 1, \tag{2.12}$$

where $\mathrm{V_{LSB}}$ is the average step width and V[i] is the voltage that the transition from (i-1)th ADC output code to i th occurs. DNL is specified in LSBs. Positive DNL means the step width is larger than the average while negative means it is smaller. DNL[i] can be minimum -1 LSB, which means that the i th ADC output code is missing in the ADC input-output characteristic. The sum of the DNL[i] values should be zero:

$$\sum_{i=1}^{2^N-1} \mathrm{DNL}[i] = 0, \tag{2.13}$$

where N is the resolution of the ADC in bits. DNL data of the first code (DNL[0]) and the last code (DNL[2^N-1]) are not defined.

Integral non-linearity (INL) is the deviation of the actual transition points from the ideal in the ADC input-output characteristic as shown in Figure 2.6. Similar to DNL, INL is also given in LSBs. INL[k] can be calculated from the cumulative sum of the DNL vectors as

$$\mathrm{INL}[k] = \sum_{i=1}^{k-1} \mathrm{DNL}[i] = 0. \tag{2.14}$$

Generally, the maximum and minimum values of DNL and INL are given while specifying the performance of an ADC.

The input-output characteristic of an ADC can be measured by applying a ramp input signal. DNL and INL can also be measured with a sinusoidal input signal when an accurate ramp signal is not available. Since DNL and INL show the static performance of the ADC, generally a low-frequency input signal is used in these measurements. Code transition points for testing with sinusoidal input are calculated as [19]

$$\mathrm{V}[i] = C - A\cos\frac{\pi\,\mathrm{H_c}[i-1]}{S} \qquad \text{for} \quad i = 1, 2, ..., (2^N - 1), \tag{2.15}$$

where C is the offset, A is the amplitude of the measured sinusoidal signal, and S is the total number of samples used in the histogram. $\mathrm{H_c}[j]$ is the number in the j th bin of the cumulative histogram of samples given as

$$\mathrm{H_c}[j] = \sum_{i=0}^{j} \mathrm{H}[i], \tag{2.16}$$

where H[i] is the number of histogram samples in code bin i.

2.3 Conventional SAR ADC

The conventional 5-bit charge-redistribution SAR ADC is shown in Figure 2.7 for single-ended implementation [20]. It consists of a binary-weighted capacitive array, switches, a comparator, and a logic. A conversion is composed of three main operation modes. The first one is the sample mode shown in Figure 2.7. In sample mode, the top plate is connected to the ground and all the bottom plates of the capacitors in the capacitive array are connected to the input. The second mode is the hold mode shown in Figure 2.8. In the hold mode, the switch connecting the top plate to the ground is opened and the bottom plates are connected to the ground. Therefore, the top plate voltage becomes -V_{IN} because the sampled charge is conserved. The third mode is the redistribution mode. As a first step of the redistribution mode, the bottom plate of the largest capacitor is connected to V_{REF} as shown in Figure 2.9 and the voltage at the top plate becomes

$$V_X = -V_{IN} + \frac{V_{REF}}{2}. \tag{2.17}$$

Then the first comparison takes place. If V_X>0, the MSB of the output code B[4] is logic-1, else B[4] is logic-0. In the case V_X>0, then SW1 is returned to the ground and the SW2 is connected to V_{REF}.In the case V_X<0, then SW4 is returned to the ground; in the case V_X>0, then SW1 is kept connected to $_{REF}$. Then the next switch SW3 is connected to V_{REF}. Therefore, the voltage at the top plate becomes

$$V_X = -V_{IN} + B[4]\frac{V_{REF}}{2} + \frac{V_{REF}}{4}. \tag{2.18}$$

The conversion continues in the same way until the LSB is decided. Towards the end of the conversion, the voltage at the top plate converges to zero. The switch configuration at the end of the conversion for ADC output code "01001" is provided in Figure 2.10. An N-bit SAR ADC requires N steps to find the N-bit code corresponding to the sampled input voltage.

2.4 High-Speed SAR ADC Design Techniques

In the last decades, several techniques have been proposed to enhance the sampling rate and the power consumption of SAR ADCs. These techniques and the technology scaling have enabled the sampling rates of SAR ADCs to exceed 1 GS/s. Most of the techniques summarized in this section are used in the ADC designs presented in the following chapters. Therefore, this section provides the basis for them.

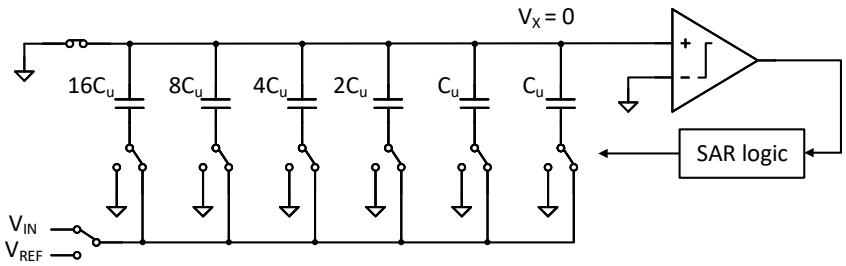


Figure 2.7: A conventional 3-bit charge-redistribution SAR ADC in sample mode.

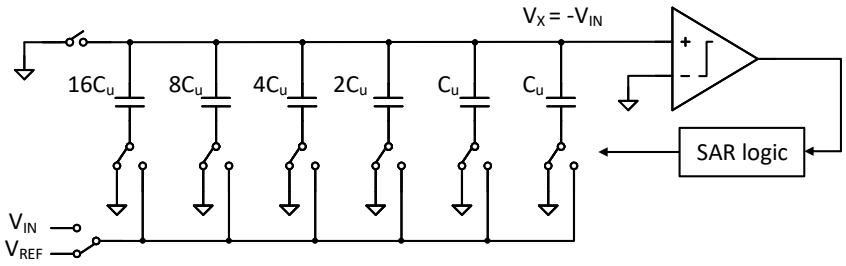


Figure 2.8: A conventional 3-bit charge-redistribution SAR ADC in hold mode.

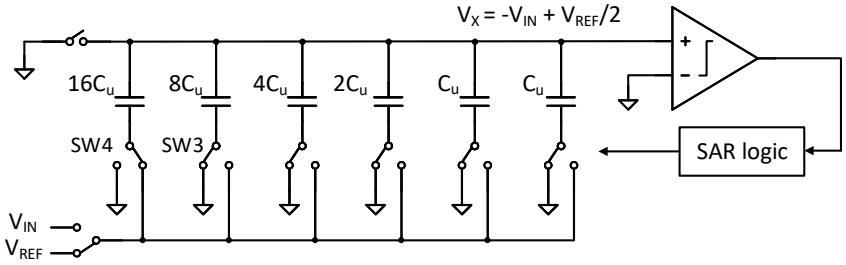


Figure 2.9: A conventional 3-bit charge-redistribution SAR ADC after the first step of the redistribution mode.

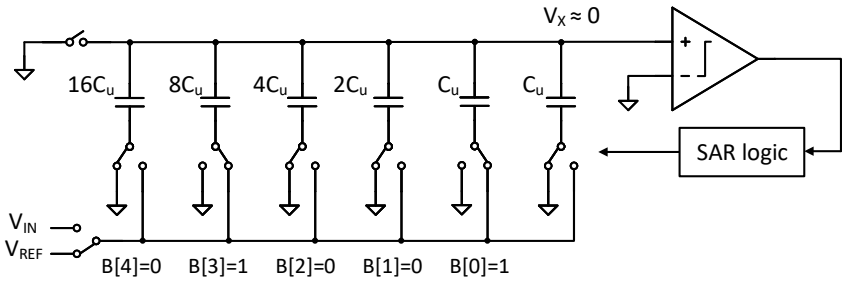


Figure 2.10: Final switch configuration of a conventional 3-bit charge-redistribution SAR ADC for output code of "01001".

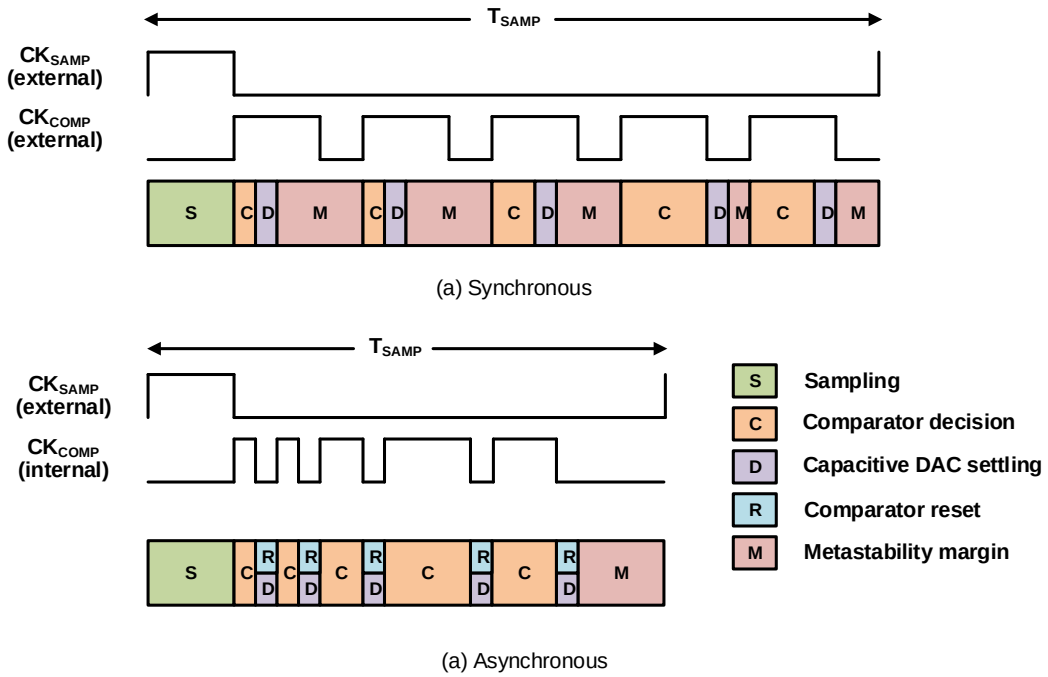


Figure 2.11: Timing of a 5-bit (a) synchronous and (b) asynchronous SAR ADC.

2.4.1 Asynchronous Clocking

The comparator delay in a SAR ADC depends on the input voltage. In a conventional SAR ADC with a synchronous clock, the clock that initiates the comparison cycles is externally provided and limited by the worst-case comparator delay. Only one of the comparisons performed for each sample experiences a decision with input voltage less than 1/2 LSB in a binary search SAR ADC, considering the nature of the SAR algorithm. Therefore, there could be only one comparison in each conversion cycle with this worst-case delay in a binary search SAR ADC. Therefore, the synchronous clocking of the comparator in the conventional SAR architecture does not offer the optimal use of the conversion time. The asynchronous SAR architecture, first proposed in [21], improves the sampling rate by triggering the comparator asynchronously depending on the completion of the previous decision.

If the input voltage is small and comparison cannot be completed in the given time interval, the comparison is called metastable. The probability of metastable comparison increases towards the LSB decisions during the SAR conversion. By providing additional time, the probability of metastability can be improved. But in a synchronous ADC, this additional time is provided for every decision and even though only one of the comparisons can be metastable. For asynchronous SAR ADCs, the additional time to improve the metastability is added for only one comparison per conversion period and it is allocated to that metastable decision. Therefore, improving the metastability is not as costly as the synchronous ADC design in

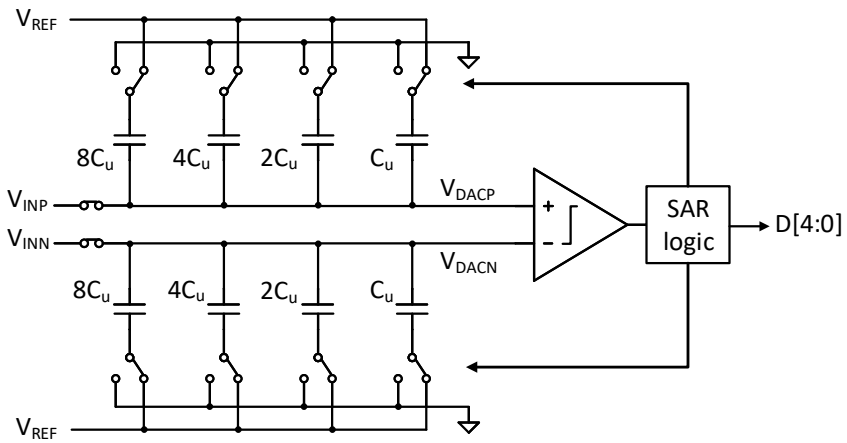


Figure 2.12: A 5-bit SAR ADC with monotonic capacitor switching (in sample mode).

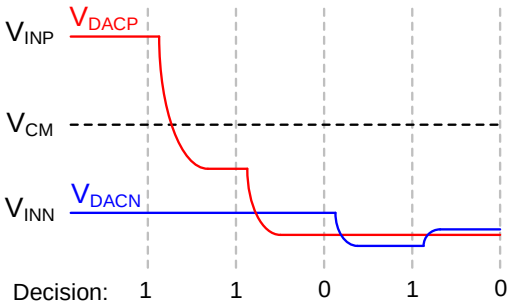


Figure 2.13: Common-mode change in a 5-bit SAR ADC with monotonic capacitor switching during SAR conversion.

terms of sampling speed [22]. The timing of synchronous and asynchronous SAR ADCs with additional time to provide metastability margin is shown in Figure 2.11.

Besides optimizing the timing, the internally generated asynchronous clock eliminates the need for a high-frequency clock. In time-interleaved ADC designs, routing of the high-speed external clock becomes harder and requires additional power consumption.

2.4.2 Monotonic Switching

Monotonic switching, also known as the set-and-down switching, is an energy-efficient switching method to lower the switching energy of the capacitive DAC in SAR ADCs [23, 24, 25]. It has been shown that this switching method reduces the power consumption by 81%, and the total capacitance of the capacitive DAC by 50% [23].

Figure 2.12 shows a SAR ADC with monotonic switching. The analog input voltage is sampled on the top plates of the capacitive DAC while all the bottom plates are connected to V_{REF}

and after the top plate sampling switch turns off, the first comparison starts immediately without any prior switching. Depending on the MSB comparison, the bottom plate of the largest capacitor ($8C_u$) on the higher voltage side is switched to the ground while the bottom plate of the largest capacitor ($8C_u$) on the lower voltage side remains unchanged. Then, then the MSB-1 comparison takes place. Depending on the MSB-1 decision, the same procedure is applied to the second-largest capacitor ($4C_u$), and the same procedure continues until the LSB is decided. The common-mode voltage of the top plates decreases at each switching step as shown in Figure 2.13.

Compared to the conventional SAR ADC switching described in Section 2.3, the monotonic switching is faster because the first comparison starts immediately after the sampling without prior switching, which saves from switching energy as well. The monotonic switching requires less switching power and reduces the logic complexity of the SAR logic since only one capacitor switches for each bit cycle. Considering that a comparator with two outputs is employed in the SAR ADC with monotonic switching, the comparator outputs are reset to the same logic level initially and one of the outputs changes its logic level depending on the comparator decision. Therefore, the bottom plates of the capacitors are controlled by the outputs of the comparator stored in a memory. Other than storing the comparator in a memory, no additional logic operation is required. Therefore logic complexity, the SAR loop delay is reduced. Furthermore, inverters can be used as the bottom plate switches since the bottom plate switching is performed only between V_{REF} and the ground.

The disadvantage of the monotonic switching is that the charge injection of the sampling switch at the top-plate causes degradation in SNDR for high-resolution ADCs. The input voltage dependent charge injection problem of the top plate sampling in monotonic switching can be improved by employing a bootstrapped sampling switch.

Another disadvantage of the monotonic switching is that the common-mode of the comparator input changes during the SAR conversion, and the common-mode dependency of the comparator offset causes dynamic offset that results in a degradation in the comparator precision. Also, the comparator decision time might increase as the common-mode decreases towards the end of the SAR conversion cycle.

Splitting Monotonic Switching

The dynamic offset problem in the monotonic switching due to common-mode variation can be solved by splitting the capacitors [26, 27, 28, 29] as shown in Figure 2.14. By splitting all the capacitors in the capacitive DAC into two halves, constant common-mode can be provided for all the comparisons [27] or only some of the capacitors can be split to keep the common-mode in a small range that does not degrade the comparator precision severely [28, 29]. In Figure 2.14, all the capacitors in the capacitive DAC except for the LSB is split into two halves. During the sampling, bottom plates of the upper row of the split capacitors are connected to V_{REF} while the bottom plates of the lower row are connected to the ground. Depending of

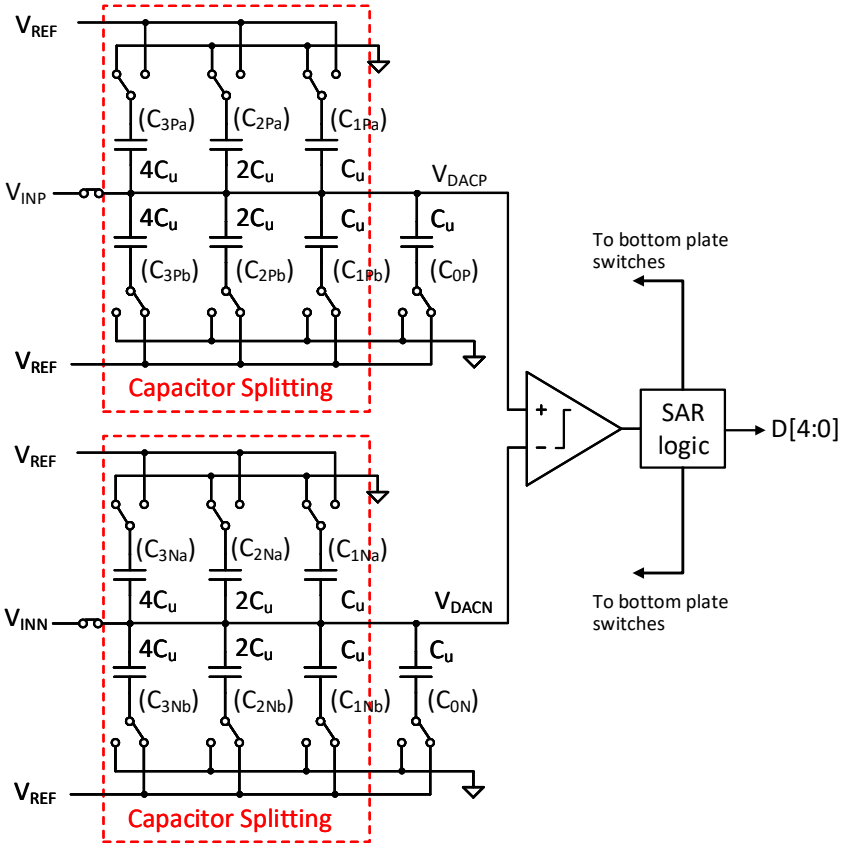


Figure 2.14: A 5-bit SAR ADC with split monotonic capacitor switching (in sample mode).

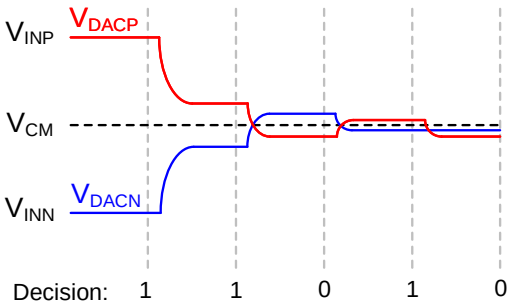


Figure 2.15: Common-mode change during SAR conversion in a 5-bit SAR ADC with split monotonic capacitor switching.

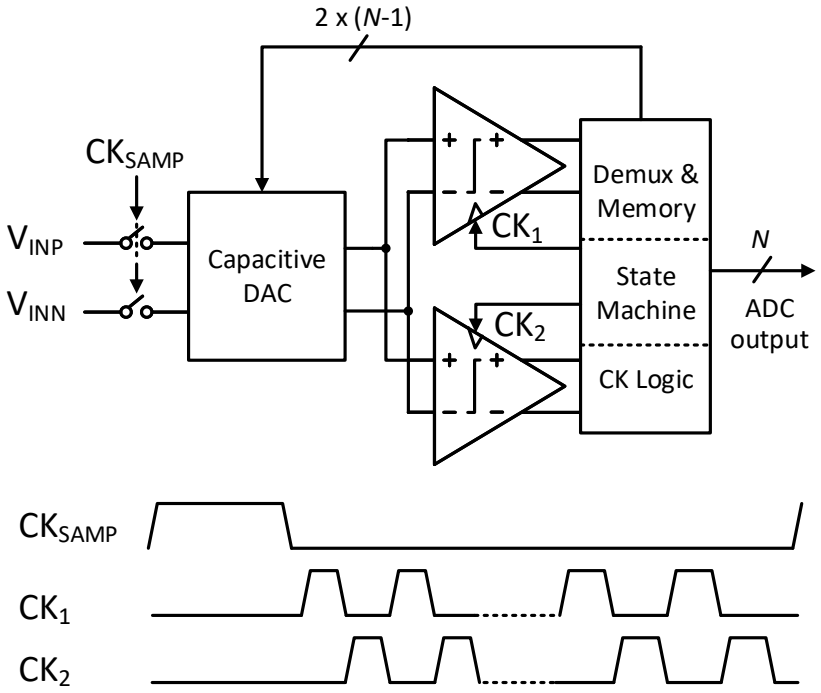


Figure 2.16: A 5-bit Loop-Unrolled SAR ADC with monotonic capacitor switching.

the comparator decision, either (C_{XPa} and C_{XNb}) or (C_{XPb} and C_{XNa}) switch while the others remain unchanged. Therefore, the voltage changes in V_{DACP} and V_{DACP} are symmetrical and the common-mode is constant for the split capacitor switchings as shown in Figure 2.15.

2.4.3 Two Alternating Comparators

In a SAR ADC design with a single comparator, the comparator needs to be reset to remove the history from the previous decision after the comparator decision is complete. While the comparator is reset, capacitive DAC settles in parallel. In a SAR ADC design with a short capacitive DAC settling time, the sampling rate is limited by the reset time of the comparator.

SAR ADC design presented in [27] employs two comparators to remove the reset time of the comparator from the critical path. Two comparators alternate; while one of them is being reset, the other makes its decision as shown in Figure 2.16. Since this architecture uses more than one comparator, any offset mismatch between the comparators causes dynamic offset errors; therefore, comparator offset calibration should be included in the design.

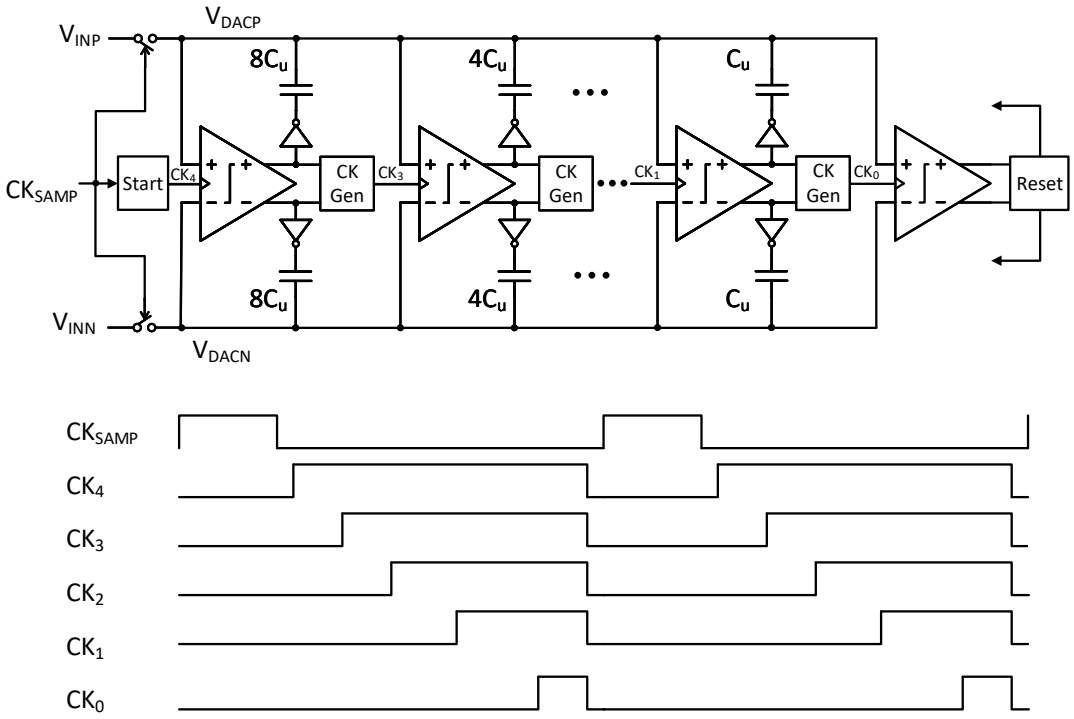


Figure 2.17: A 5-bit Loop-Unrolled SAR ADC with monotonic capacitor switching.

2.4.4 Loop-Unrolling

The loop-unrolled (LU) SAR architecture, also known as domino-SAR, first proposed in [30], uses N comparators for N-bit conversion and the outputs of the comparators control the capacitive digital-to-analog converter (DAC) directly without any additional logic operation as shown in Figure 2.17. The 6-bit SAR ADC in [30] combines loop-unrolling with the monotonic switching to minimize the SAR loop delay. Unlike the architecture with two alternating comparators, the LU-SAR architecture does not require demultiplexing of the comparator outputs to generate the capacitive DAC control bits. Because the additional delay due to demultiplexing is avoided, loop-unrolling enables smaller SAR loop delay with minimal logic complexity. Moreover, loop-unrolling also mitigates electro-migration issues since each comparator is triggered only once per SAR conversion. Similar to the architecture with two alternating comparators, LU-SAR architecture requires comparator offset calibration to prevent errors due to dynamic offset during the SAR conversion.

2.4.5 DAC Redundancy

Conventional SAR ADC uses binary-weighted capacitive DAC. Each voltage step at the output of the capacitive DAC scales down by two with each capacitive switching. Capacitive DAC should settle within 1/2 LSB before the next decision is made to prevent errors. Settling time

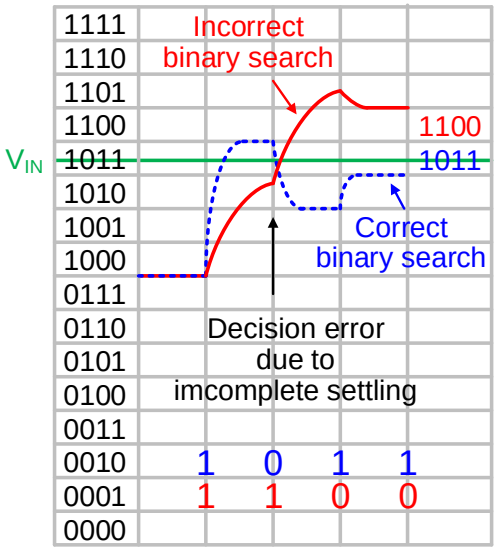


Figure 2.18: Binary search with decision error due to incomplete capacitive DAC settling.

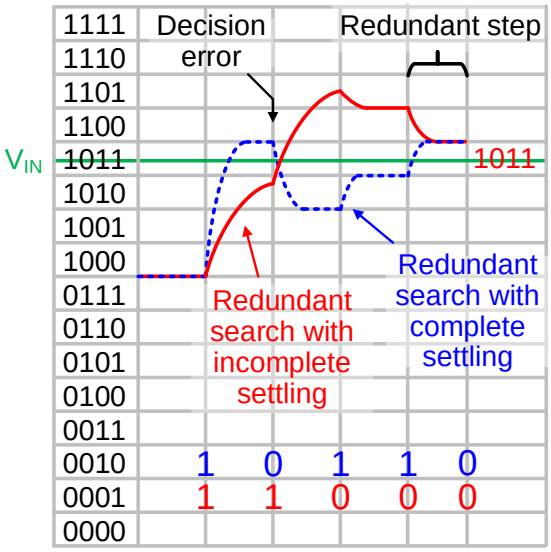


Figure 2.19: Redundant search with decision error due to incomplete capacitive DAC settling.

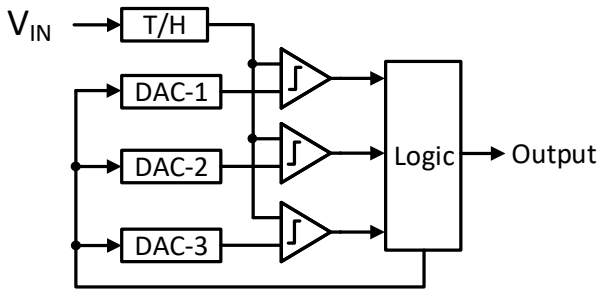


Figure 2.20: 2-bit per conversion step SAR ADC.

depends on the capacitor size, the resistance of the switches, and the output impedance of the voltage reference, and it might take significant time for large capacitive DACs. Figure 2.18 shows the output voltage of a binary capacitive DAC during SAR conversion without and with error due to incomplete settling. The error causes the conversion error to be larger than $\pm 1/2$ LSB which is the boundary of the quantization error.

The settling time of the capacitive DAC can be the bottleneck in high-speed SAR ADCs, especially the settling time of the MSB capacitor. Implementing redundancy in the capacitive DAC allows us to recover errors due to incomplete DAC settling [31, 32]. Redundancy can be implemented by using radix < 2 [33, 34] or radix $= 2$ with redundant steps [35, 27]. In Figure 2.19, the output voltage of a redundant capacitive DAC with one additional redundant step during SAR conversion (weights $= 4, 2, 1, 1$) is shown. Since the total weight of the remaining steps is greater than the erroneous step, it is possible to recover the error and reach the correct code. Redundancy makes it possible to reach a code level from multiple paths as opposed to the binary search where reaching a code is possible using only one path.

Redundancy in capacitive DAC can correct other dynamic errors such as decision errors due to noise and or errors due to offset mismatch in loop-unrolled SAR ADCs. However, redundancy might cause the number of decisions with input voltage less than $1/2$ LSB and might increase the probability of metastable decisions.

2.4.6 Multi-bit per Conversion Step

Conventional SAR ADCs convert only one bit per conversion step. By increasing the number of bits resolved in each step, the number of conversion steps can be reduced, and the sampling rate can be increased as a result [36, 37, 38]. To resolve multiple bits in one conversion step, multiple comparators are employed as in flash ADC architecture. Figure 2.20 shows the block diagram of a 2-bit per conversion step SAR ADC. Since multiple comparators are employed, the comparator offset should be matched for the conversion accuracy.

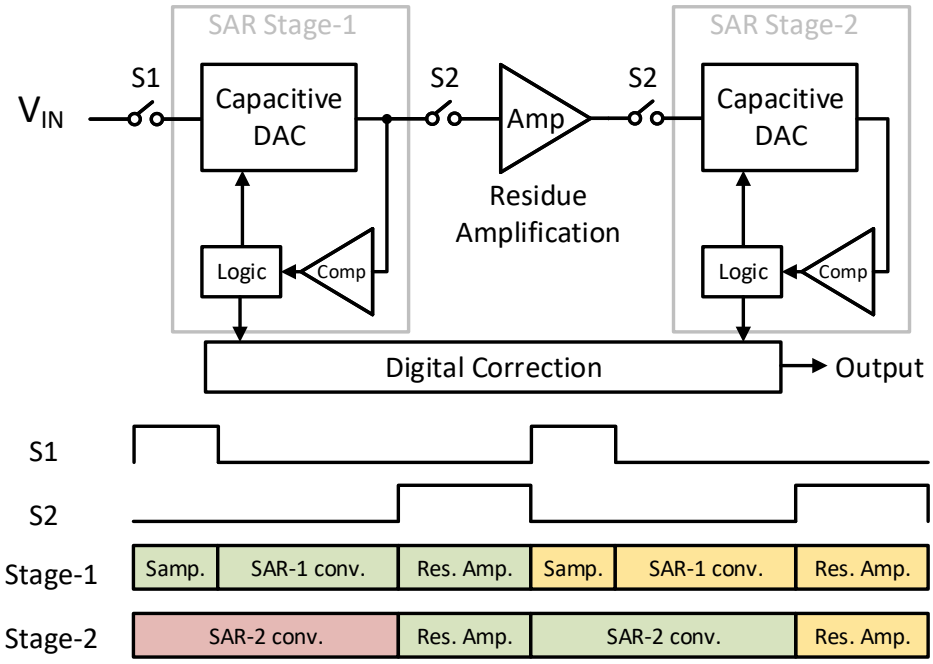


Figure 2.21: Two-Stage Pipelined SAR ADC.

2.4.7 Pipelined SAR

Pipelined SAR ADC architecture is based on pipelining two or more stages with residue amplifiers between them. Figure 2.21 shows the block diagram and timing of a two-stage pipelined SAR ADC. Pipelining SAR stages increase the sampling rate because the two SAR stages operate in parallel while resolving different samples. Amplification of the residue between the stages decreases the comparator noise requirements of the following stages. Therefore, pipelined SAR architecture is useful in achieving high resolution in addition to a higher sampling rate. In [39], a single-channel 10-bit two-stage pipelined SAR ADC achieving 50 dB SNDR at 1.5 GS/s is presented.

2.4.8 Time-Interleaving

Time-interleaving is a technique that combines multiple ADCs in an interleaved fashion to increase the conversion rate where the conversion rate of a single-channel ADC is not sufficient. In Figure 2.22, 4-way time-interleaved ADC is shown as an example. The sampling rate of f_s can be achieved using M channels with the sampling rate of f_s/M in a time-interleaved configuration.

Mismatches between the interleaved channels, such as offset, gain, timing, and bandwidth mismatches, degrade the linearity of the time-interleaved ADC.

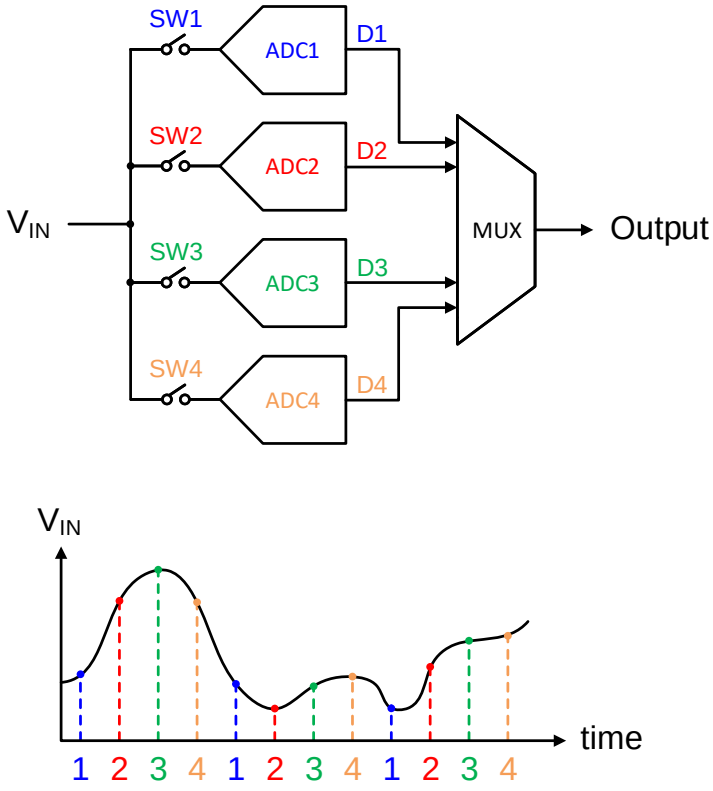


Figure 2.22: Time-Interleaving.

Offset mismatch between the ADC channels causes spurs in the output spectrum of the interleaved ADC system located at [40]

$$f_{spur,offset} = k \times \frac{f_s}{M} \qquad k = 1,2,...,M. \tag{2.19}$$

In SAR ADCs, the gain of the ADC depends on the capacitive DAC, its parasitics, and the capacitive DAC reference voltage. **Gain mismatch** between the time-interleaved ADC channels causes spurs dependent on the frequency of the input signal located at [40]

$$f_{spur,gain} = \pm f_{in} + \frac{k}{M} f_s \qquad k = 1,2,...,M. \tag{2.20}$$

The time intervals between the consecutive sampling instances are equal in an ideal time-interleaved ADC system. However, **timing skew mismatch** occurs when the timing instant is skewed compared to its ideal value. This timing skew is not random as jitter. Spurs due to skew mismatch depends on the frequency of the input signal and are at the same frequencies

as the spurs due to gain mismatch [40]:

$$f_{spur,skew} = \pm f_{in} + \frac{k}{M} f_s \qquad k = 1,2,...,M. \tag{2.21}$$

Bandwidth mismatch between the sampling networks of the ADC channels causes input frequency dependent amplitude and phase errors. Similar to gain and skew mismatch, bandwidth mismatch causes spurs in the spectrum also at [40]

$$f_{spur,bandwidth} = \pm f_{in} + \frac{k}{M} f_s \qquad k = 1,2,...,M. \tag{2.22}$$

Offset and gain mismatch errors can be corrected by post-processing the digital ADC output [41]. But digital correction after the quantization is not as precise as the analog correction and reduces the dynamic range of the system [42]. In [13], the offset of each ADC channel is internally auto-zeroed by background calibration, the gain of each channel can be adjusted by changing the reference voltage of the capacitive DAC using R-3R ladder driving the reference buffer, and the skew between the clock phases is digitally trimmed [13].

3 Asynchronous SAR ADC[1]

This chapter presents a low-power 9-bit 222 MS/s single-bit/cycle asynchronous SAR ADC design. The proposed design combines asynchronous clocking, top plate sampling, binary-weighted custom-designed capacitive digital-to-analog converter (CDAC) with small unit capacitors, splitting monotonic capacitor switching with constant capacitive DAC common-mode except for the last switching, and dynamic SAR memory to optimize both power consumption and SAR loop delay using a single comparator in 65 nm. Measurement results show that the 9-bit SAR ADC achieves 47.6 dB SNDR and 29.6 fJ/conversion-step figure-of-merit (FoM) near Nyquist frequency at 222 MS/s, consuming 1.07 mA from a 1.2 V supply. All the building blocks in the SAR ADC are dynamic, it does not consume any static current, and the power consumption scales linearly with the sampling rate over a wide range. Therefore, it can operate at sampling rates up to 222 MS/s with almost constant figure-of-merit (FoM), providing flexibility in terms of power consumption.

Outline

This chapter is organized as follows. Section 3.1 describes the proposed SAR ADC architecture with circuit details, and explains the techniques used to achieve faster sampling rate and lower power consumption. Section 3.2 summarizes the measurement results and Section 3.3 concludes the chapter.

3.1 ADC Architecture

3.1.1 Overview

Figure 3.1 shows the block diagram, and Figure 3.2 shows the timing scheme of the proposed 9-bit SAR ADC. The ADC consists of two bootstrapped sampling switches, a sampling clock

[1] This chapter is based on: A. Akkaya, F. Celik, and Y. Leblebici, "A Low-Power 9-Bit 222 MS/s Asynchronous SAR ADC in 65 nm CMOS," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sevilla, 2020, pp. 1-5, (©IEEE) [29].

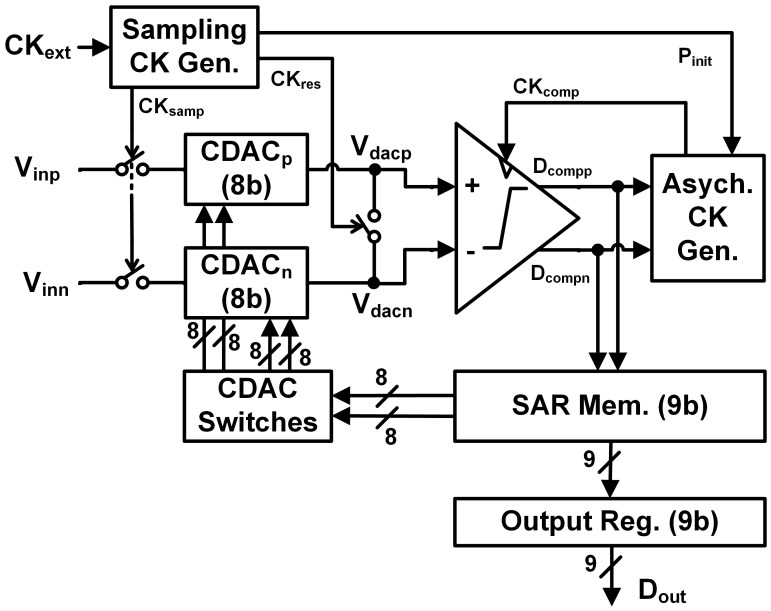


Figure 3.1: Block diagram of the proposed asynchronous SAR ADC.

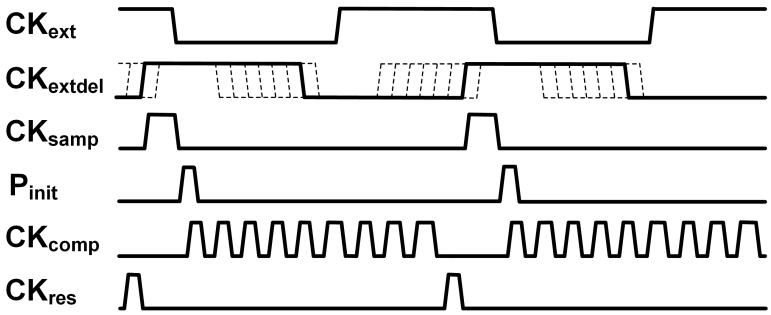


Figure 3.2: Timing scheme of the proposed asynchronous SAR ADC.

generation block, two 8-bit capacitive DACs, capacitive DAC switches that drive the bottom plates of the capacitive DAC capacitors, a reset switch that shorts the top plates of the capacitive DAC capacitors after each SAR conversion, a dynamic comparator, an asynchronous clock generation block, a SAR memory to control the capacitive DAC switches, and an output register.

The differential input signal is sampled by the sampling clock CK_{samp} via top plate sampling; therefore, the first comparison starts immediately after the sampling without any charge redistribution, saving both energy and time. Bootstrapping is applied to the sampling switches to sample the differential input signal with sufficient linearity over a wide input voltage range. CK_{samp} which controls the bootstrapped sampling switches is generated internally in the sampling clock generator block using the external clock with 50% duty cycle CK_{ext} and the delayed CK_{ext}, namely CK_{extdel}. As shown in Figure 3.2, CK_{samp} is generated by the AND operation of CK_{ext} and CK_{extdel}. The duration of the sampling interval can be adjusted by

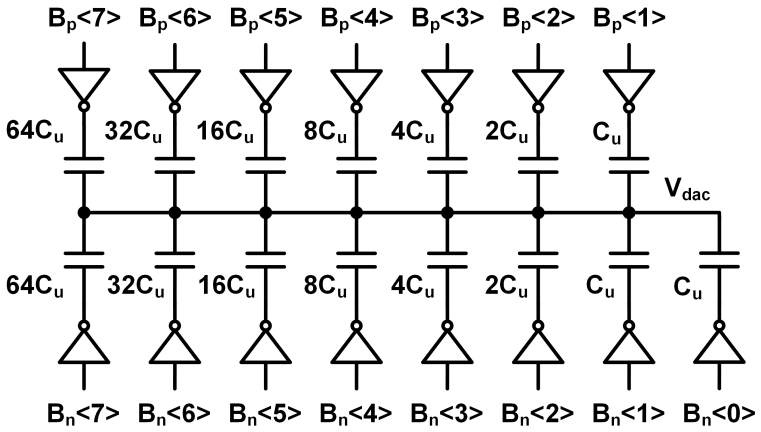


Figure 3.3: capacitive DAC with bottom plate switches.

selecting different delay line outputs. The beginning of the tracking is decided by the rising edge of CK_{extdel}, and the input tracking always ends with the falling edge of CK_{ext}. Since the sampling precision depends on the falling edge jitter of the sampling clock which does not depend on CK_{extdel}, the jitter requirement of the delay line is relaxed.

A StrongARM latch [43] is used as a comparator. Since it is fully dynamic, it does not consume any static power. Because only one comparator is used for all decisions and the comparator input common-mode is almost constant, its offset does not degrade the precision; therefore, offset calibration is not required. The comparator clock is generated asynchronously to shorten the overall SAR conversion time and to avoid a fast external clock.

A SAR memory block replaces the SAR logic in this design. It generates the control signals of the capacitive DAC switches that drives the bottom plates of the capacitive DAC capacitors and provides the ADC output bits which correspond to the result of the successive-approximation. Then, the ADC output bits are sampled by the output registers.

3.1.2 Capacitive DAC

Top plate sampling with monotonic capacitor switching provides the advantage of using 8-bit capacitive DACs in a 9-bit SAR ADC. Binary-weighted capacitive DACs also serve as the sampling capacitors. The splitting monotonic capacitor switching [26] which provides constant common-mode voltage is applied in the capacitive DAC except for the last capacitor, as shown in Figure 3.3. Since the comparator offset is dependent on the input common-mode, constant common-mode switching provides better comparator precision. The last capacitor is switched only on the single side, in $CDAC_p$ or $CDAC_n$, to decrease the total number of unit capacitors in the capacitive DAC from 510 to 255. Because the common-mode shift generated by the single side switching of the last capacitor is small, its effect on the comparator precision is negligible. capacitive DAC switches are implemented using inverters and they only use

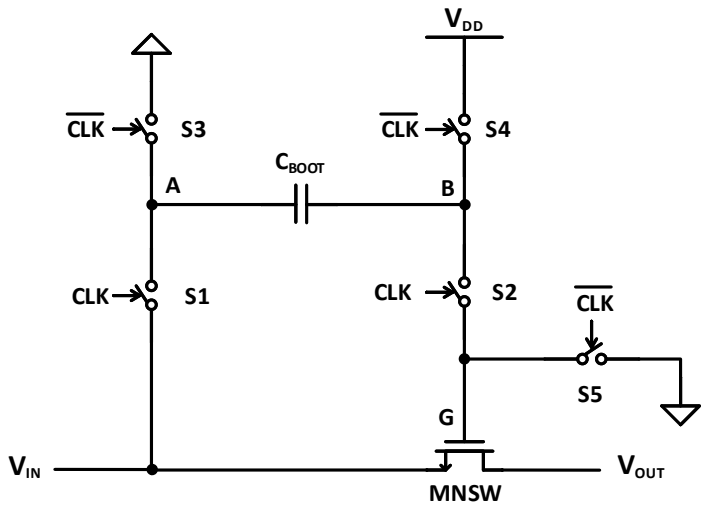


Figure 3.4: Bootstrapping with ideal switches.

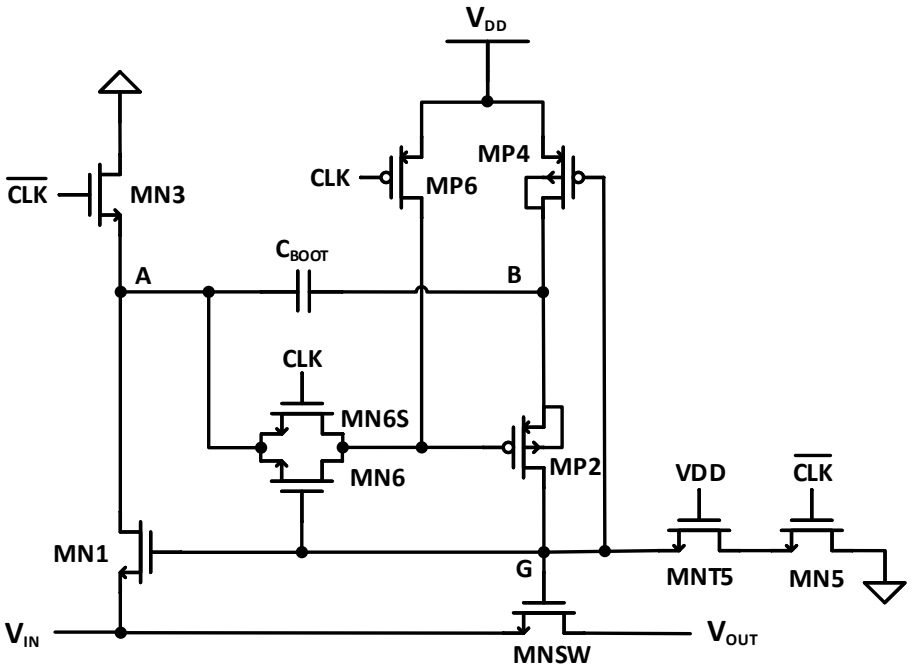


Figure 3.5: Schematic of the bootstrapped switch.

the supply voltage provided off-chip as reference voltage. Besides being a power efficient switching scheme, splitting monotonic switching provides faster SAR loop operation with reduced logic complexity because the bottom plates of the capacitors in capacitive DAC are directly controlled by the comparator decisions stored in a memory. The capacitive DAC is custom-designed to keep the size of the unit capacitor small (0.7 fF). Small unit capacitor size helps to have a smaller area, less parasitics, less routing, less switching energy, and faster capacitive DAC settling although it degrades the capacitor matching. Moreover, the total sampling capacitance is large enough to meet the kT/C noise requirement for 9-bit resolution.

3.1.3 Bootstrapped Sampling Switch

Bootstrapped switches are used for sampling the input signal with better linearity. Sampling linearity of a simple NMOS switch or a T-gate switch is limited because both on-resistance and the amount of charge injected when the switch is turned off depend on the input voltage. Since top plate sampling is employed in the capacitive DAC, the input voltage dependent charge injection affects the sampling linearity negatively. The bootstrapping technique ensures a constant gate-source voltage for a wide range of input voltages and achieves better sampling linearity.

Figure 3.4 shows the implementation of bootstrapping on an NMOS switch with ideal switches [44]. Bootstrapping the sampling switch provides a constant gate-source voltage of V_{DD} during the sampling. When the clock (CLK) is low, the bootstrapped switch is in the precharging phase. In the precharging phase, S3 connects node-A to the ground and S4 connects node-B to V_{DD}; therefore, the bootstrapping capacitor C_{BOOT} is precharged to V_{DD}. The gate of the sampling switch, node-G is connected to the ground via S5, hence the sampling switch MNSW is turned-off. In the sampling phase, S3, S4, and S5 turn off; S1 and S2 turn on. Since C_{BOOT} is precharged to V_{DD} and node-A is connected to V_{IN}, node-G becomes V_{DD}+V_{IN}. As a result, the gate-source voltage of the sampling switch MNSW is equal to V_{DD}, independent of the V_{IN}.

The schematic of the bootstrapped switch is depicted in Figure 3.5 [44]. MN1, MP2, MN3, MP4, and MN5 correspond to the switches S1, S2, S3, S4, and S5 in Figure 3.4, respectively. This bootstrapped switch supports rail-to-rail input. The following modifications provide reliable operation even when $V_{IN} = V_{DD}$, which is the worst case. The gate of MN1 is controlled by the boosted voltage to ensure conductivity even when $V_{IN} \geq V_{DD}$-V_{TH}. MP6 connects the gate of MP2 to V_{DD} to turn MP2 off in the precharging phase.

Unlike the simple implementation given in Figure 3.4, the gate of MP2 is not controlled by $\overline{CLK}$ or connected to the ground to turn it on to prevent the gate-source voltage of MP2 to become -2V_{DD} when $V_{IN} = V_{DD}$. MN6S connects node-A to the gate of MP2 at the beginning of the sampling phase to initiate the conductivity of MP2. MNS6 is not conductive when node-A rises above V_{DD}-V_{TH}. The addition of MN6 ensures that the gate of MP2 could reach up to $_{DD}$. The conductivity of MN6 is loop dependent; therefore, it is turned on after the voltage on node-G rises. To ensure that MP4 is off during the sampling phase, its gate is controlled by the

voltage on node-G instead of CLK. MNT5 is added to prevent the gate-drain voltage of MN5 to exceed V_{DD}. The bulks of MP4 and MP2 are connected to the node-B, which has the highest potential, instead of V_{DD}.

The parasitic capacitance at node-B could be large due to the well capacitance. Due, to this large parasitic capacitance at node B, the gate-source voltage of the sampling switch MNSW becomes less than V_{DD} during the sampling phase. To achieve a gate-source voltage closer to V_{DD}, a larger C_{BOOT} is required.

Since bootstrapping the sampling switch provides a gate-source voltage of V_{DD}, a smaller sampling switch can be employed. Using a smaller switch decreases the non-linear junction parasitic capacitance at the top plate of the capacitive DAC. This non-linear parasitic capacitance introduces dynamic gain error during the SAR conversion and decreases the conversion accuracy of the SAR ADC.

3.1.4 SAR Memory

Thanks to the splitting monotonic switching method, differential comparator outputs should only be stored and fed to the capacitive DAC switches without any complex logic operation. Therefore, a SAR memory can replace the SAR logic implemented with the state machine approach in the traditional SAR architecture. The block diagram of the SAR memory is shown in Figure 3.6, and each SAR memory cell is implemented in dynamic logic to improve the speed and the power efficiency, as shown in Figure 3.7. The proposed memory cell is based on [27]; however, there are some modifications applied to prevent potential problems with the implementation of this memory cell with the proposed SAR ADC design. Writing to the memory cell is enabled by the C_{wr} signal generated internally. The logic circuitry that generates C_{wr} is modified by adding M_3 and M_4 in series. Therefore, it is ensured that the writing to a cell is activated after the comparator is reset to prevent the previous decision to be written to the current cell.

The memory cell operates by pulling up one of the output nodes, D_{capp} or D_{capn}, which are reset to logic-0 previously. The SAR memory cell in the literature [27] is modified also by adding cross-coupled NMOS transistors, M_1 and M_2 in Figure 3.7, between the dynamic nodes D_{dynp} and D_{dynn} to prevent both of the dynamic nodes to be pulled-up at the same time. Since it is implemented using dynamic logic, once the D_{dynp} or D_{dynn} is pulled-up, they cannot be pulled-down until the next SAR conversion, if the cross-coupled NMOS transistors are not added. In this case, any incorrect pull-up cannot be recovered; if both D_{dynp} and D_{dynn} are pulled-up, the SAR conversion cannot continue properly, and the ADC gives a wrong output code. This problem might happen especially when the differential input voltage of the comparator is very small; the comparator cannot resolve the input quickly and the waveform of the comparator outputs becomes similar to the waveforms shown in Figure 3.8. Since both comparator outputs might be discharged together, the following logic might propagate this as logic-0 to the memory. Modifying the SAR memory cell by adding the cross-coupled NMOS

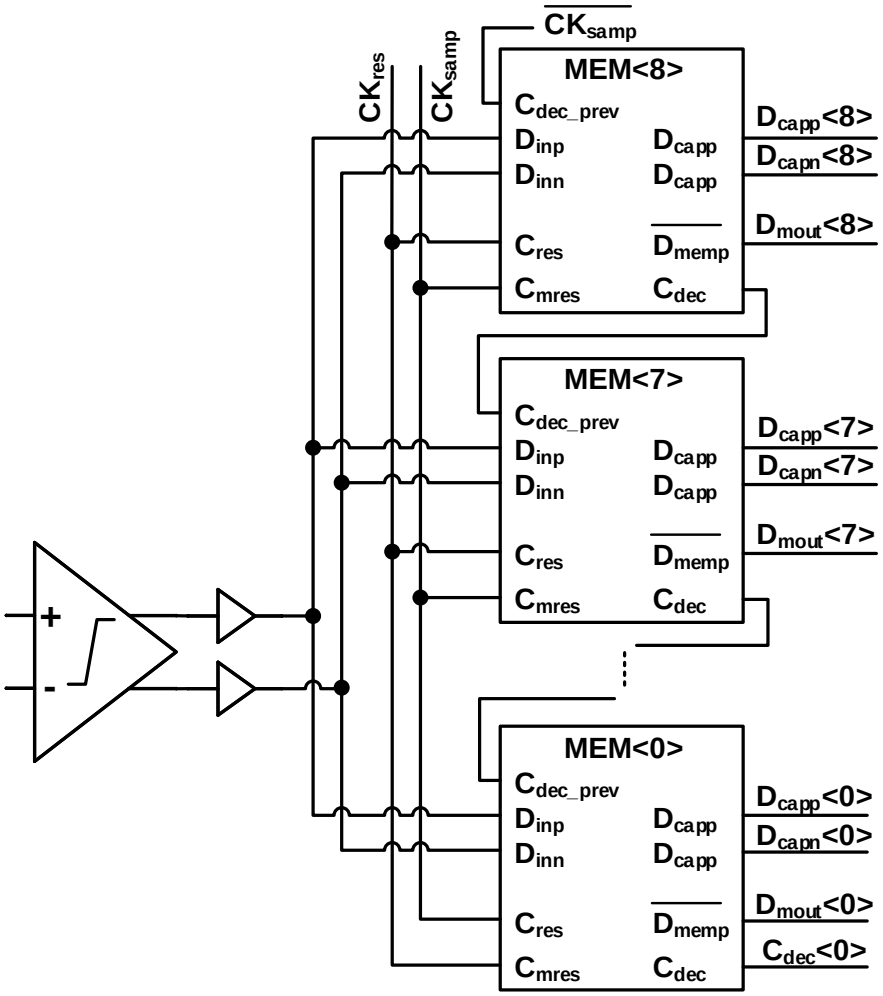


Figure 3.6: SAR memory.

transistors prevents this error.

The bottom plate switches of the differential capacitive DACs are controlled by D_{capp}, D_{capn} and the inverted versions of them. Before each sampling phase, CK_{res} resets the outputs of the SAR memory which control the capacitive DAC switches, also the differential capacitive DAC outputs are shorted before each input tracking starts. The latch loops that store the comparator decisions in the memory cells are reset with the rising edge of the CK_{samp} allowing enough time margin for the SAR ADC outputs to be sampled by the output registers before a new conversion begins.

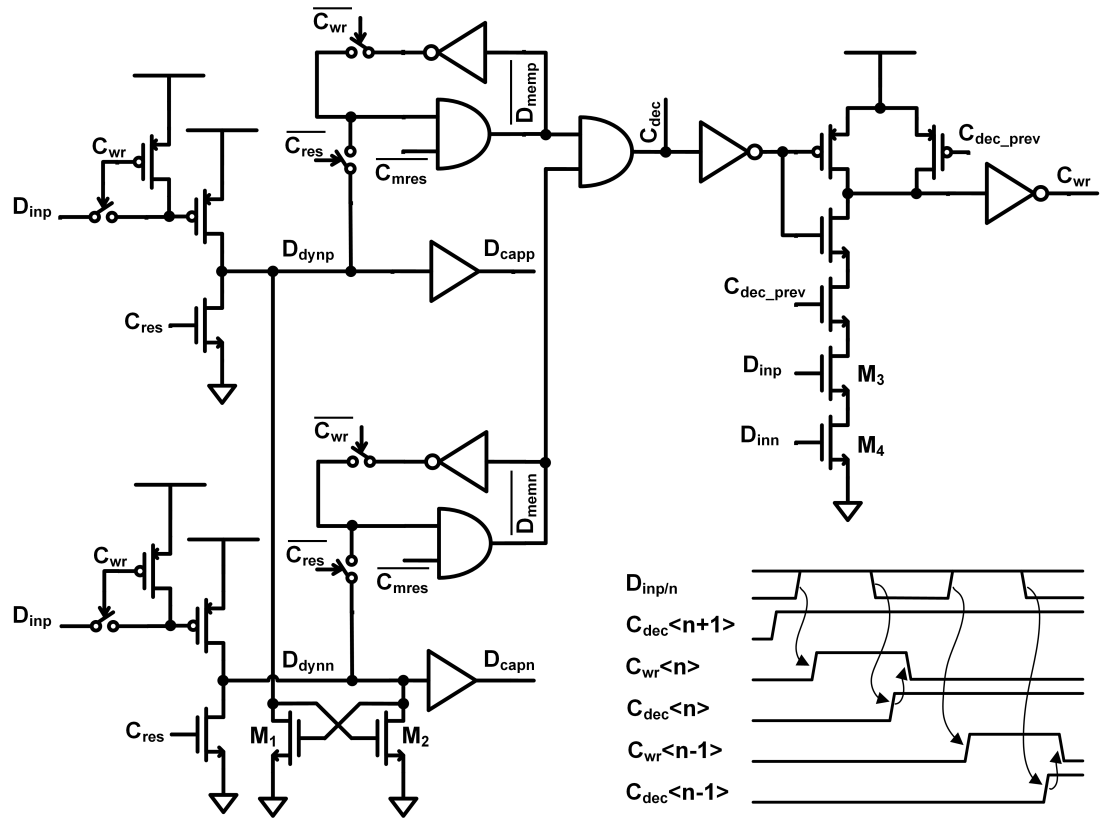


Figure 3.7: Proposed modified SAR memory cell.

3.1.5 Asynchronous Clock Generation

Asynchronous clock generation circuitry shown in Figure 3.9 generates the asynchronous comparator clock CK_{comp} using the comparator outputs. The first rising edge of the asynchronous comparator clock is generated with the P_{init} signal after the sampling of the input. Then, after one of the comparator outputs, D_{comp} or D_{comn}, goes to logic-0, the CK_{comp} is pulled down. After both comparator outputs are reset to logic-1, CK_{comp} rises again. It is verified by the simulation results that the rising edge of the clock is generated after the capacitive DACs settle. After the last comparator decision, C_{dec}<0> signal generated in the SAR memory goes to logic-1 and CK_{comp} is kept at logic-0 until resetting the SAR memory before the next conversion. While the sampling clock CK_{samp} or the reset signal CK_{res} is high, CK_{comp} is also forced to be logic-0.

3.2 Measurement Results

The prototype ADC is fabricated in 65 nm CMOS and it occupies an active area of 92 μm × 180 μm (0.017 mm^2) as shown in the micrograph in Figure 3.10.

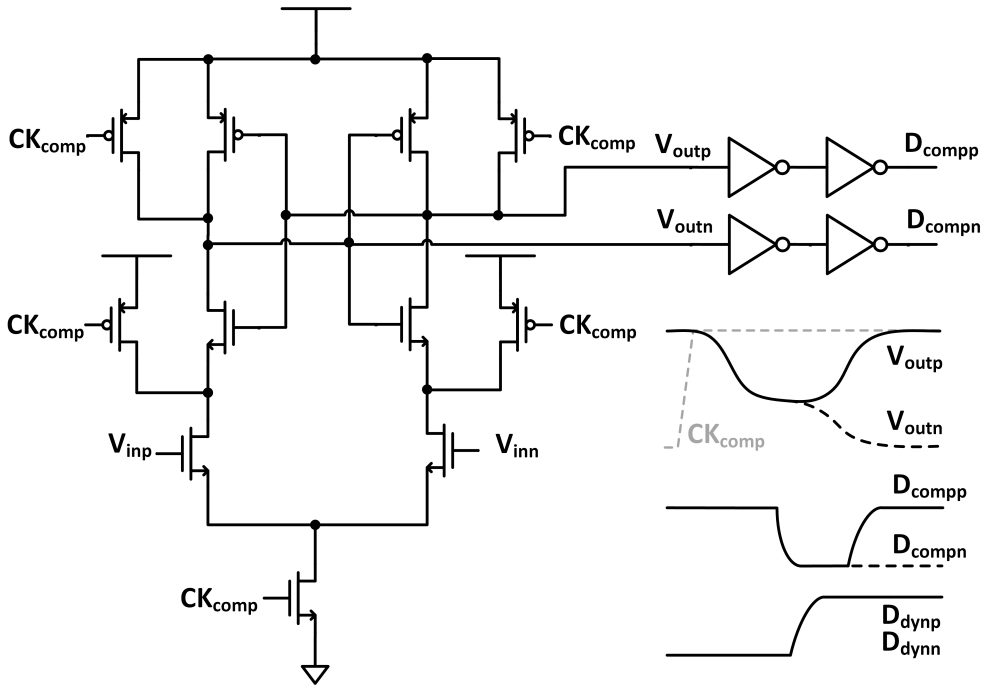


Figure 3.8: Comparator and the potential SAR memory error without the cross-coupled NMOS transistors.

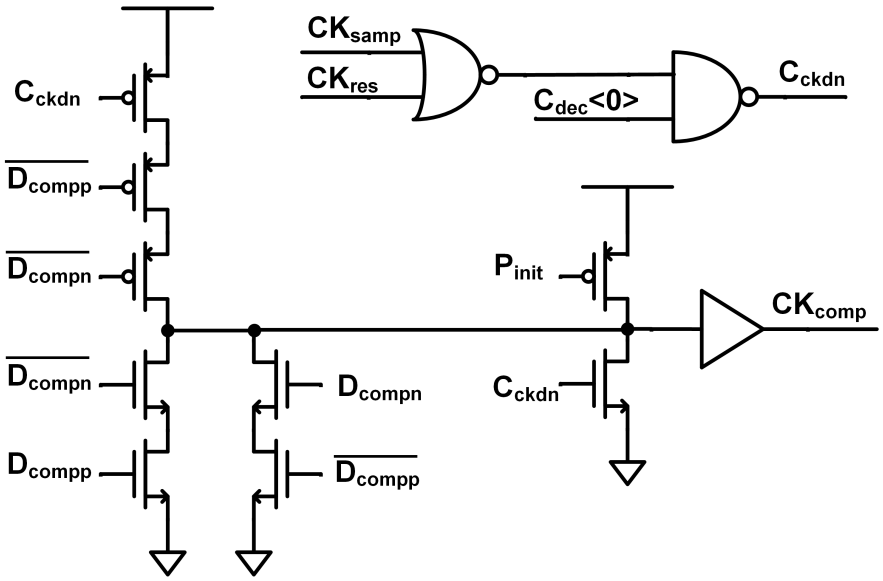


Figure 3.9: Asychronous comparator clock generation circuitry.

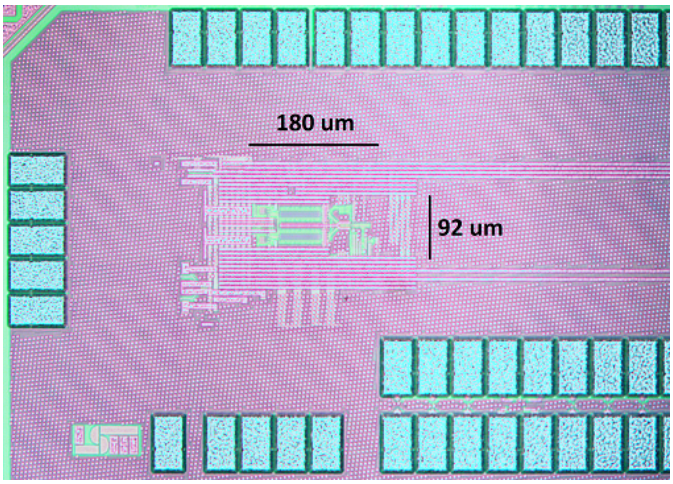


Figure 3.10: Chip micrograph.

Figure 3.11, Figure 3.12, and Figure 3.13 show the measured SNDR, power consumption, and FoM values, respectively, for varying sampling rates while the input frequency is around 10 MHz. SNDR plot is almost flat, the power consumption scales linearly with the sampling rate until 222 MS/s, and the FoM is almost constant up to that sampling rate since the ADC does not consume static power. SNDR decreases after 222 MS/s because the least significant bit decision is incomplete. Between 270 MS/s and 320 MS/s, the SNDR is still over 40 dB even though the two least significant bit decisions are not complete and the sampling cannot be performed with sufficient linearity due to the shortened sampling duration.

In Figure 3.14, the measured ADC output spectrums at 222 MS/s with low frequency and near Nyquist rate input signal are given. The SNDR is measured as 48.59 dB with low frequency input and 47.58 dB with near Nyquist frequency input and the corresponding FoMs are 26.3 fJ/conversion-step and 29.6 fJ/conversion-step, respectively. Measured DNL and INL plots of the ADC are shown in Figure 3.15. Peak DNL values are 0.61/-1, while the peak INL values are 1.29/-1.33. The peak values occur at the MSB and (MSB-1) transitions due to missing codes. Capacitor mismatch in the capacitive DAC is the main factor that limits the linearity.

3.3 Conclusion

The SAR ADC architecture proposed in this chapter combines power efficiency and high-speed design techniques to achieve the optimal FoM. The presented low power 9-bit asynchronous SAR ADC in 65 nm CMOS operates over a wide range of sampling rates with almost constant FoM up to 222 MS/s. Measurement results show that it achieves 47.58 dB SNDR and 29.6 fJ/conversion-step FoM with near Nyquist frequency input at 222 MS/s, consumes 1.07 mA from 1.2 V supply and occupies an active area of only 0.0017 mm^2. FoM of the presented design is better than or comparable with the state-of-the-art single-channel high-speed ADCs in 65 nm CMOS with SNDR>40 dB as summarized in Table 3.1.

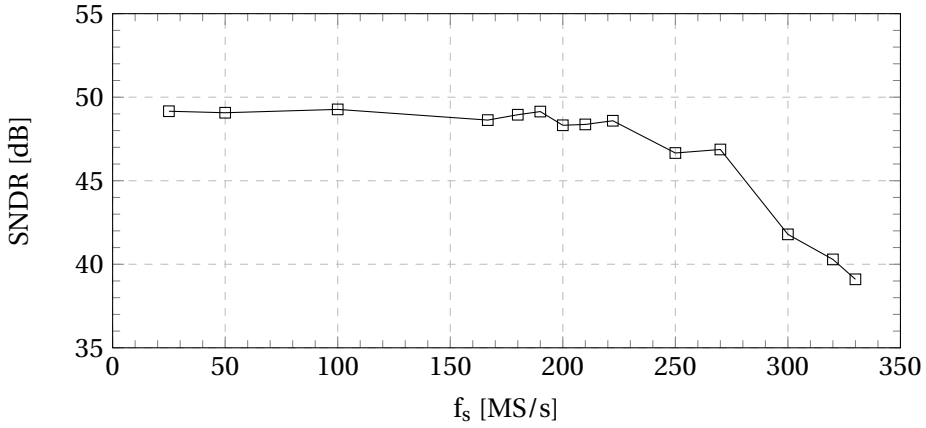


Figure 3.11: SNDR vs. sampling frequency (f_s), $f_{in} \approx 10$ MHz.

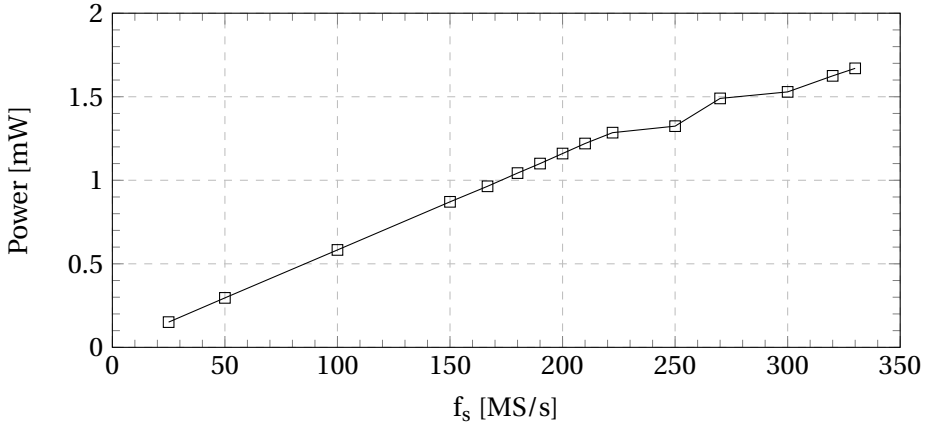


Figure 3.12: Power vs. sampling frequency (f_s), $f_{in} \approx 10$ MHz.

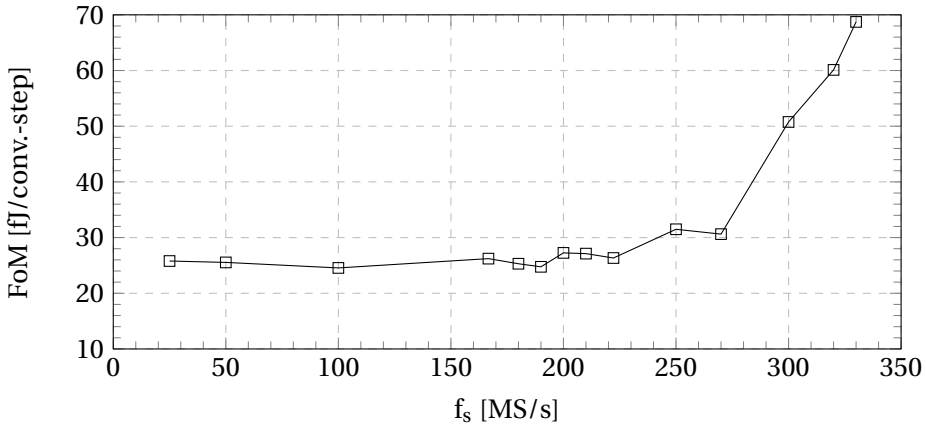


Figure 3.13: FoM vs. sampling frequency (f_s), $f_{in} \approx 10$ MHz.

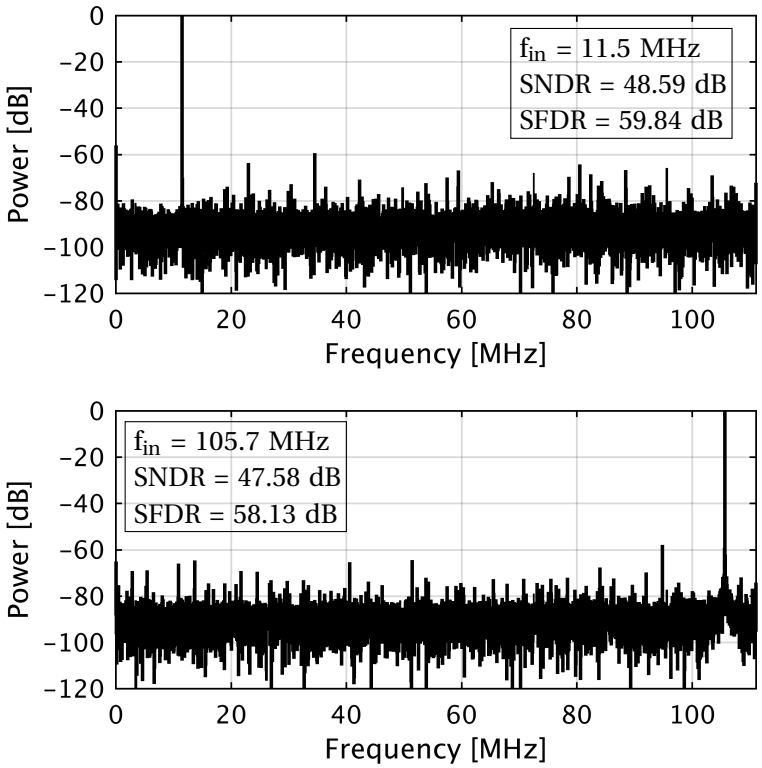


Figure 3.14: Measured output spectrums at $f_s = 222$ MS/s with low frequency and near Nyquist rate input signal.

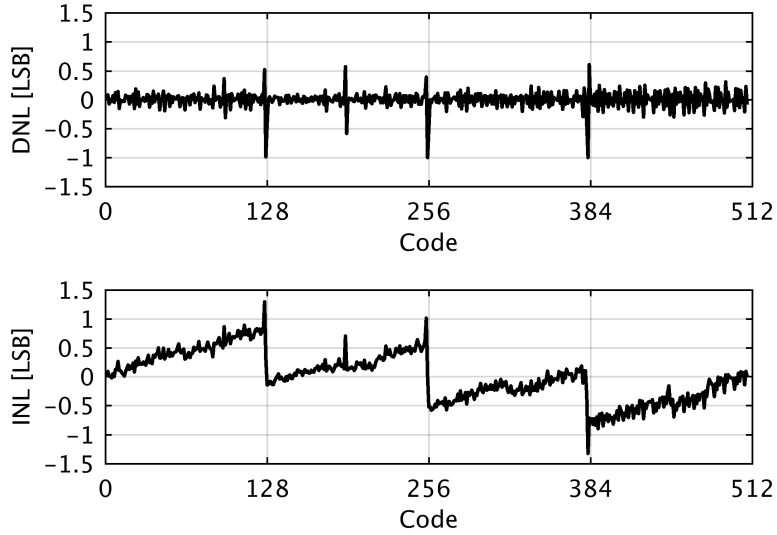


Figure 3.15: Measured DNL and INL plots.

Table 3.1: Performance comparison of the asynchronous SAR ADC.

	[45]	[35]	[28]	[37]	**This work**
Technology [nm]	65	65	65	65	**65**
Resolution [bits]	9	10	8	8	**9**
Supply Volt. [V]	1.2	1.2	1.2	1.2	**1.2**
f_s [MS/s]	100	100	450	400	**222**
Power [mW]	1.26	1.13	6.48	4	**1.28**
$SNDR_{@Nyq}$ [dB]	50.06	56	47.3	40.1	**47.58**
$SNDR_{@DC}$ [dB]	-	59	-	44.4	**48.59**
$FoM_{@Nyq}$ [fJ/conv.-step]	45	21.9	76.1	117	**29.6**
$FoM_{@DC}$ [fJ/conv.-step]	-	15.5	-	73	**26.3**
Area [mm^2]	0.013	0.026	0.035	0.028	**0.017**
Architecture	SAR 1b/c.	SAR 1b/c.	SAR 1b/c.	SAR 2b/c.	**SAR 1b/c.**

4 Delay-Based LSB Extraction[1]

The main speed limitation in charge-redistribution SAR ADCs is usually the settling time of the capacitive digital-to-analog converter (DAC). Therefore, it is desirable to minimize the unit capacitor size. Also, power efficiency and area are the two other parameters that make having a small unit capacitor desirable. The fundamental limitation on the unit capacitor size is the kT/C sampling noise. Generally, the minimum sampling capacitor size is calculated considering the kT/C noise. However, choosing the minimum unit capacitor size that meets the kT/C noise requirement is not always feasible in terms of implementation. For example, the unit capacitor size required for the kT/C noise to be equal to the quantization noise in a 10-bit SAR ADC with a full-scale input voltage of 1 V is around 125 aF. Such a small unit capacitor is hard to implement with sufficient matching. Therefore, the unit capacitor size is chosen larger than the required value, and this results in increased power consumption, area, and settling time.

Contribution

Comparators are used only for deciding the polarity of the applied differential input in standard SAR ADC designs. However, the delay information of the comparator can be used for quantizing the input as well [47, 48, 49]. This chapter proposes a resolution improvement circuitry that uses the previously reported comparator decision delay information utilization technique to extract one more bit from the SAR ADC [48]. Obtaining the extra bit does not require the resolution of the capacitive DAC or the number of comparisons in the SAR cycle to be increased. Therefore, the number of unit capacitors in the capacitive DAC is half of that of a standard SAR ADC's with the same resolution while the unit capacitor size required to meet kT/C noise requirement is double. The previously reported design uses stochastic foreground calibration to tune the digitally controlled delay element [48], while this chapter proposes a low-power stochastic background calibration circuitry to adjust the control voltage of the

[1] This chapter is based on: A. Akkaya, F. Celik, and Y. Leblebici, "Self-Calibrated Delay-Based LSB Extraction for Resolution Improvement in SAR ADCs," *2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC),* Helsinki, Finland, 2019, pp. 1-7, (©IEEE) [46].

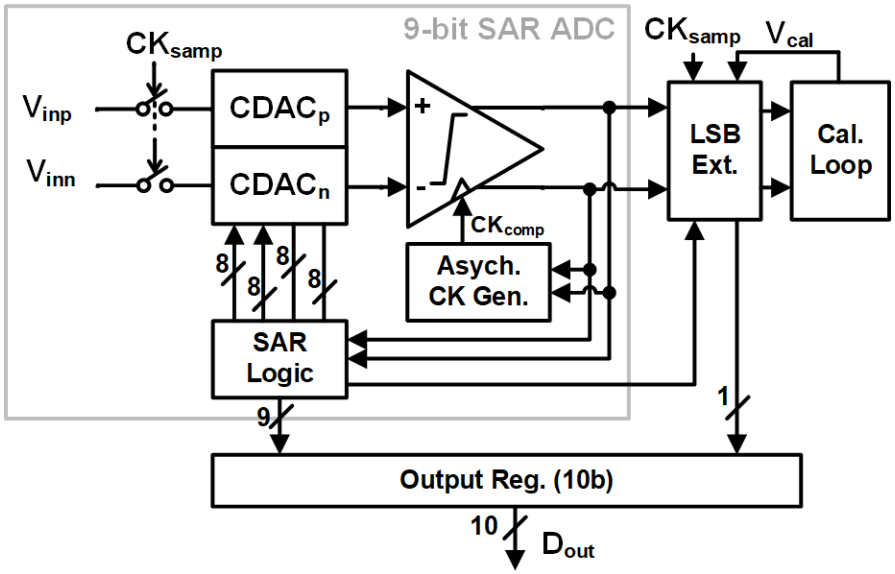


Figure 4.1: Block diagram of the SAR ADC with LSB extraction circuitry and background calibration loop.

reference delay automatically. In this way, the reference delay does not need to be tuned externally, and it is more robust against temperature, supply voltage, and input common-mode variations over time.

Outline

This chapter is organized as follows: Section 4.1 describes how the comparator delay information is used for improving the resolution of a SAR ADC and gives the circuit level implementation details. Section 4.2 analyzes the effect of jitter and variations on the performance and provides the post-layout simulation results of the SAR ADC with the implemented self-calibrated least significant bit (LSB) extraction circuitry. Finally, Section 4.3 concludes the chapter.

4.1 Delay-Based LSB Extraction

4.1.1 Overview of the Method

Figure 4.1 shows the implementation of the proposed self-calibrated delay-based LSB extraction circuitry with a 9-bit differential charge-redistribution asynchronous SAR ADC. The LSB extraction circuitry generates the new LSB (10th bit) using only the comparator delay information. Background delay calibration loop adjusts the reference delay that will be compared with the comparator delay to decide the new LSB.

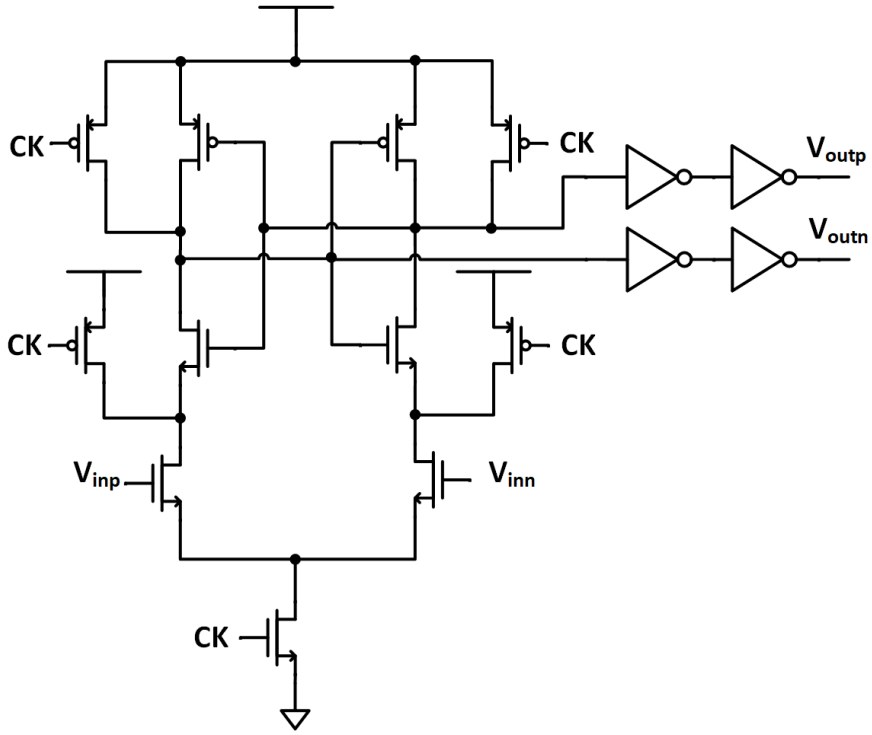


Figure 4.2: Schematic of the comparator based on StrongArm latch.

A StrongArm latch, which is shown in Figure 4.2 is used as a comparator in this SAR ADC design [43]. The delay of the comparator decision is dependent on the applied input voltage. The relationship between the comparator decision delay and the applied differential input voltage is given in Figure 4.3. According to the plot, if the delay information of the comparator is known, then the applied input voltage information can be obtained as well. Therefore, this input voltage information can be used in analog-to-digital conversion to determine the input level. Since the delay values for larger input voltages are very close to each other, it is harder to detect the input voltage precisely. However, the delay difference is larger for smaller input voltages because the delay increases exponentially as the input voltage decreases.

The differential capacitive DAC output voltages of a 3-bit ADC during the successive approximation cycle are depicted in Figure 4.4 as an example. Considering an ideal SAR operation, if the residue voltage after all the successive approximation (SA) switching is known, then the exact value of the input voltage can be derived. Therefore, the delay of the last comparison holds important information about the input voltage.

In Figure 4.5, the resolution improvement method using the delay of the last comparison is summarized, and the implementation on a 3-bit SAR ADC is shown for simplicity. In this diagram, the x-axis represents the analog input voltage of the ADC. First, the 3-bit SAR ADC quantization levels corresponding to the analog input voltage are shown. Above the 3-bit quantization levels, the residue voltage after the SA cycle is plotted for the whole input range.

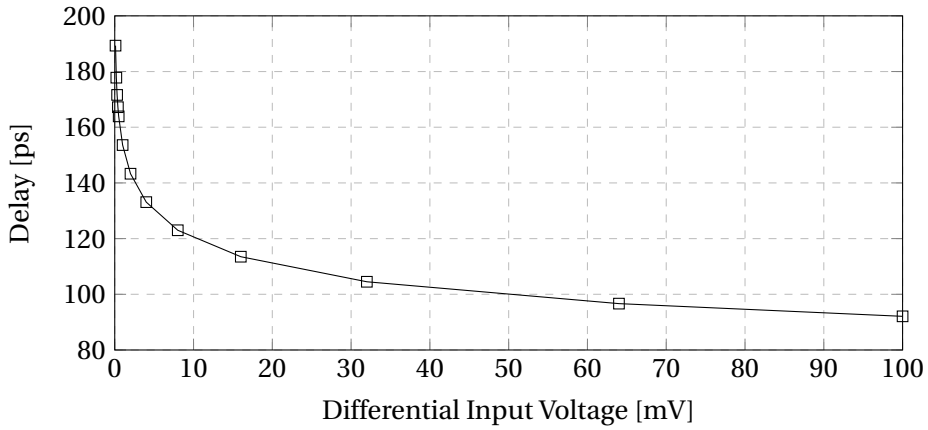


Figure 4.3: Decision delay vs. differential input voltage plot of the comparator.

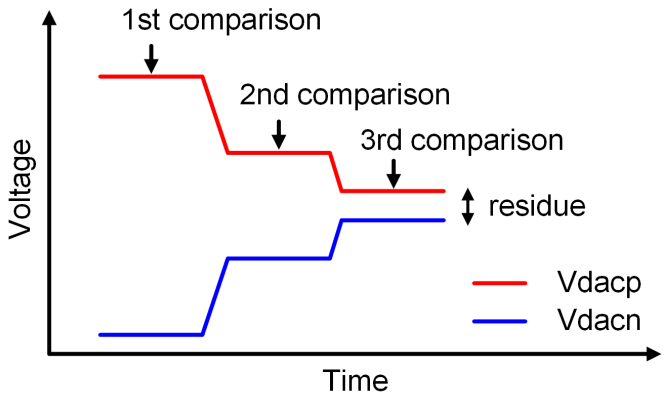


Figure 4.4: Differential DAC output voltages of a 3-bit SAR ADC during the SA cycle.

Regarding the standard SAR operation shown in Figure 4.4, this residue voltage is the input of the last comparison. The LSB of the 3-bit SAR ADC output is decided depending on the polarity of the residue voltage. However, the information that the residue voltage carries can be used further to extract more information about the input, as mentioned previously. When the residue voltage plot is linearly divided into four regions, each region corresponds to the last two bits of the 4-bit ADC output. Since the residue voltage for the whole range is known, the delay values that correspond to the residue voltages can also be plotted for the whole input range. By mapping these four regions to the comparator delay plot, we can see that the delay value shown with the red dashed line assists us in obtaining the 4th bit. The proposed method is based on comparing the delay of the last comparison with a reference delay (t_d), represented by the red dashed line in Figure 4.5, to generate the new LSB. The reference delay should be equal to the comparator decision delay when $\pm V_{DAC\_LSB}/2$, which is equal to the half of the LSB voltage of the capacitive DAC, is applied as the input voltage. Therefore, the middle steps

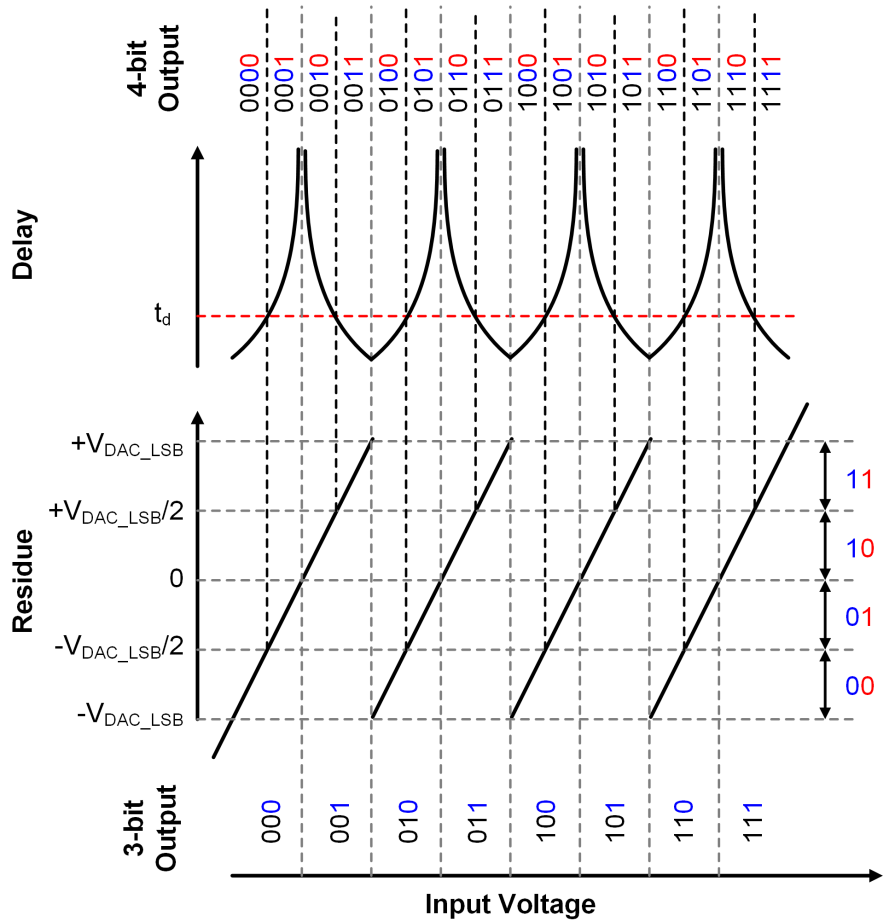


Figure 4.5: The diagram showing the relationship between the ADC decision levels, SA residue voltage and the comparator decision delay for a 3-bit SAR ADC with LSB extraction from comparator decision delay.

in the input/output characteristic of the ADC, as shown in Figure 4.6 with the dashed lines are generated. As a result, the number of ADC quantization levels are doubled, and the resolution of the ADC is increased by one bit. This technique can be applied to a standard N-bit SAR ADC to turn it into an (N+1)-bit ADC without requiring any modifications on the SAR ADC operation.

4.1.2 Circuit-Level Implementation

In this subsection, the circuit level implementation of the novel LSB extraction circuit with the background calibration loop will be explained. The implementation is made with an asynchronous 9-bit differential charge redistribution SAR ADC. Since the proposed method can be applied to any SAR ADC topology, the details of the SAR ADC part will not be given, and only the implementation of the resolution improvement method with the self-calibration

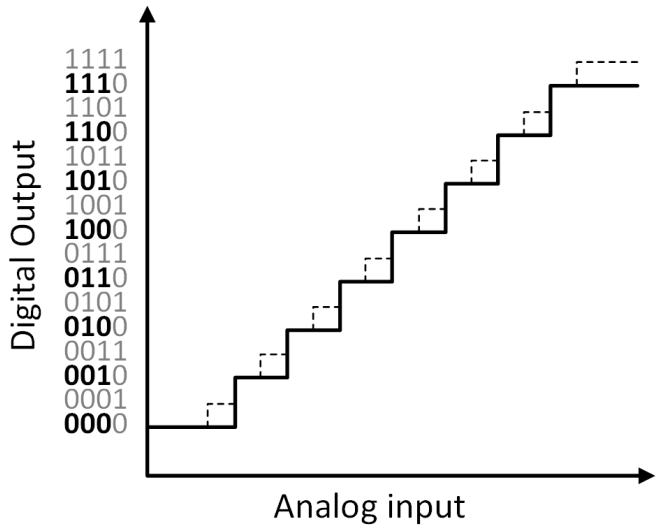


Figure 4.6: Ideal input-output characteristic of a 3-bit SAR ADC without LSB extraction circuit (in solid line) and with LSB extraction circuit (in dashed line).

loop will be described.

The proposed method is based on comparing the last comparator decision delay with a certain reference delay to decide whether comparator input voltage, which is the residue of the SA operation, is higher or lower than $\pm V_{DAC\_LSB}/2$. Outputs of the comparator (StrongArm latch) are set to logic-1 when the clock signal is low. With the rising edge of the clock, the comparator starts to make a decision. When one of its outputs goes to logic-0, the decision is made, and the ready signal rises. Comparator decision time is defined as the delay between the rising edges of the comparator clock and the ready signal. Therefore, the reference delay, which will be used in the time-domain comparison of the ready signal, is generated by delaying the rising edge of the clock.

The schematic and the timing diagram of the proposed LSB extraction circuitry is given in Figure 4.7, where CK_{samp} is the sampling clock of the SAR ADC, $\overline{D_{compp}}$ and $\overline{D_{compn}}$ are the inverted comparator outputs, and CK_{comp} is the comparator clock. First, the comparator clock and the inverse comparator outputs corresponding to the last decision of the SAR cycle are obtained by using the appropriate select signals C_{CK_sel} and C_{Dcomp_sel}. These select signals are derived from the SAR logic block. The selected rising edge of the clock is delayed by the voltage-controlled delay line to generate the C_{ref} signal while the C_{ready} signal is generated by the OR operation of the last inverse comparator outputs. Then, the rising edge of the C_{ref} signal is compared with the rising edge of the C_{ready} signal by the set-reset (SR) latch. The latch output that generates the new LSB (D_{lsb}), goes to logic-0 if the rising edge of the C_{ref} is earlier, otherwise stays at logic-1. The SR latch output passes through a dynamic logic gate to keep the decision on the dynamic node until the ADC outputs are sampled by the output

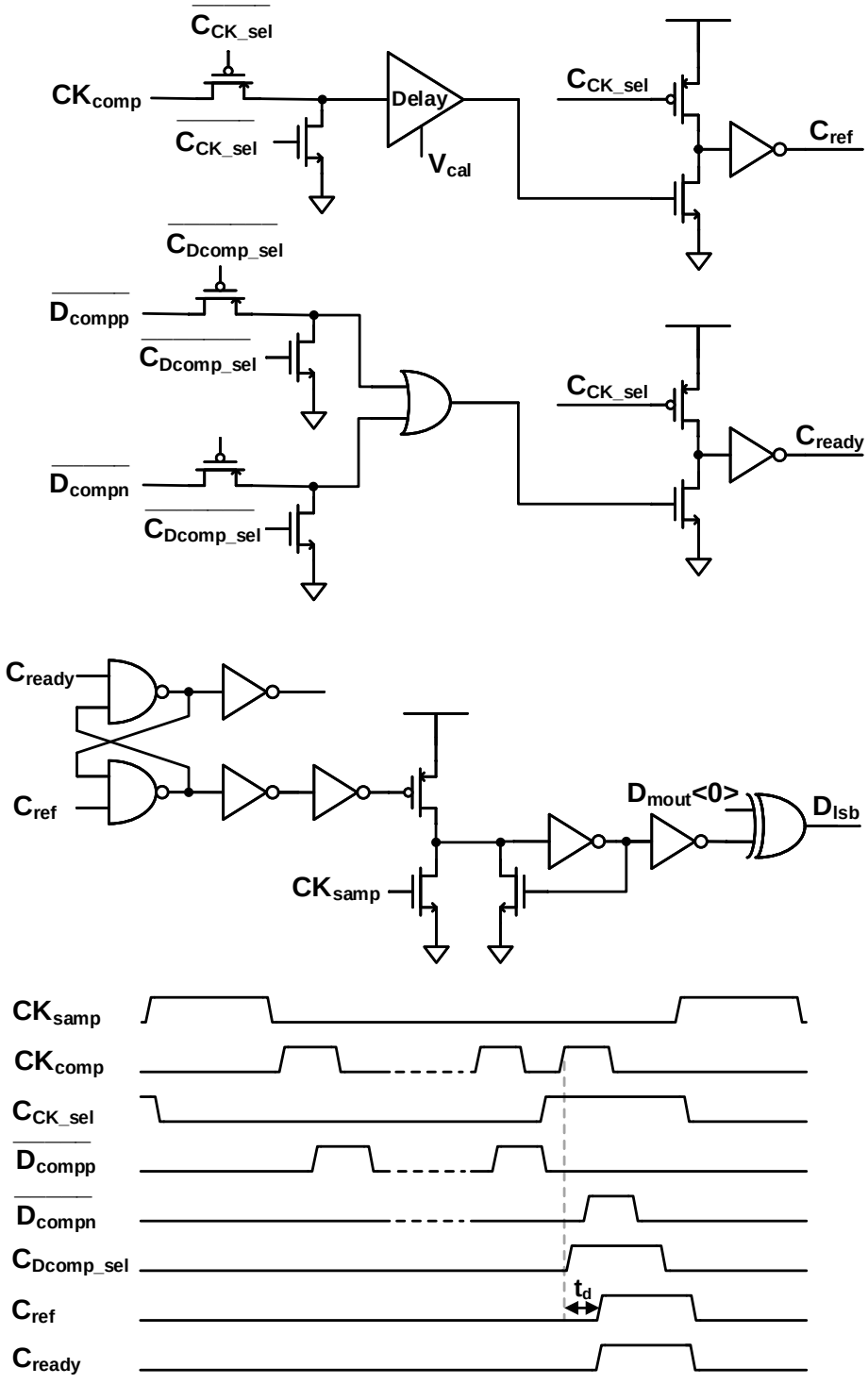


Figure 4.7: LSB extraction circuitry and the timing scheme of the signals.

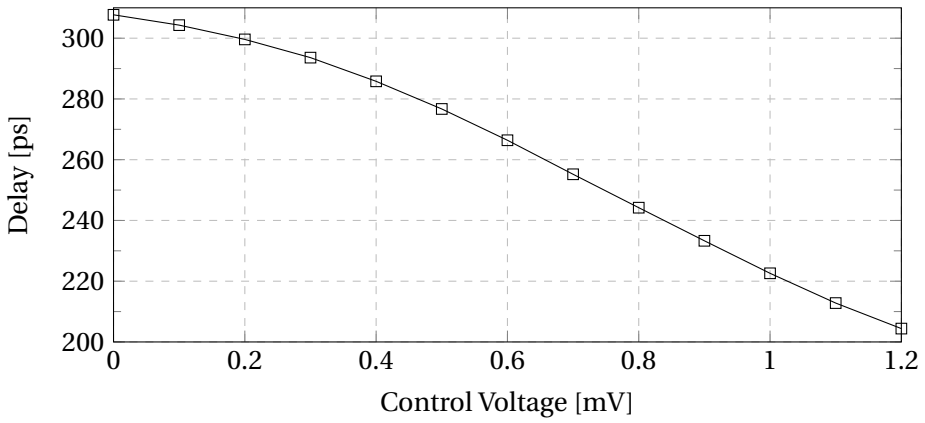


Figure 4.8: Delay of the reference signal vs. control voltage.

registers. Finally, using an XOR gate, D_{lsb} is obtained.

The delay element used in the reference delay generation consists of an inverter and a varactor as the load of the inverter. The delay value is controlled by the voltage applied to the varactors, which varies the values of the capacitive loads. In Figure 4.8, the rising edge delay plot of the C_{ref} signal with respect to the rising edge of the clock is given for varying control voltages.

In the previously reported work [48], the reference delay is generated by a digitally tunable delay element, and the foreground stochastic calibration is used for tuning the delay. In this chapter, a similar stochastic approach is used but with background calibration. Background calibration loop can track the variations over time, such as temperature, power supply, and input common-mode variations, and adjust the control voltage accordingly. The control voltage of the delay line is adjusted by the background calibration loop, which is shown in Figure 4.9. Charge based dynamic calibration circuit which is previously used for comparator offset calibration [27, 50] is adapted for the background calibration loop of the control voltage. This calibration circuit adjusts the calibration voltage on the capacitor by adding or subtracting a small amount of charge at each LSB extraction step. Whether the charge is added or subtracted is decided by the SR latch output. Therefore, the loop adjusts the control voltage so that the probability of the comparator delay being higher or lower than the reference delay is 50% considering the distribution of the residue voltage is uniform.

Since the size of the calibration capacitor is large enough, the effect of each SR decision on the control voltage is very small. As a result, the number of samples in the stochastic calibration is large enough, and the voltage can be calibrated finely. Moreover, the calibration loop is fully dynamic; therefore, its power consumption is very low.

In the presented SAR ADC design, a single comparator is used for all the comparisons. Thus, its offset does not degrade the linearity of the SAR ADC. Comparator offset, which translates into the offset of the SAR ADC for this single-comparator SAR ADC design, does not affect the

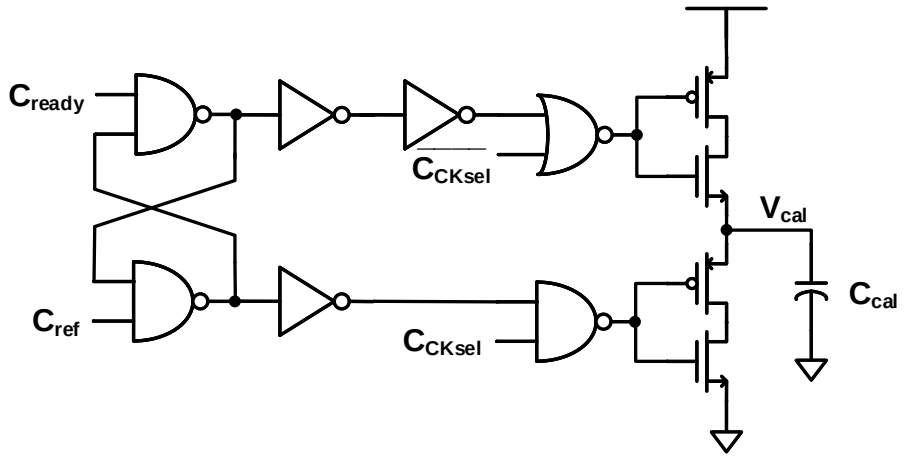


Figure 4.9: Self-calibration loop to generate the control voltage for the reference delay.

delay-based LSB extraction since it means just a DC offset in the successive approximation.

It should be noted that, regarding kT/C noise, the total sampling capacitor should be large enough to perform the sampling with (N+1)-bit resolution when using this technique. However, it is not the primary restriction on the sampling capacitance in this design since the primary limitation on the minimum unit capacitor is the matching for this resolution. Therefore, this does not create a problem.

4.2 Simulation Results

The proposed ADC is designed in 65 nm CMOS, and it occupies an area of 93 μm × 203 μm (0.019 mm^2) as shown in Figure 4.18. The LSB extraction circuitry and the reference delay calibration loop occupies only 23 μm × 48 μm (0.001 mm^2), which corresponds to 5.8% of the total area. The simulation results given in this section are derived from the post-layout simulations.

Since the applied method is based on time-domain information, jitter is an important factor that limits its efficiency. The objective of this design is maximizing the sampling frequency, so the comparator is designed to be fast. Previously reported work that uses the comparator delay information [48] was a low-voltage SAR ADC; therefore, the comparator decisions were slower. Since the noise of the StrongArm latch increases with speed, the jitter of the comparator delay is one of the main factors limiting the efficacy of the LSB extraction method in SAR ADCs with faster comparators.

Jitter will be examined in three main parts: jitter of the comparator delay, jitter of the reference

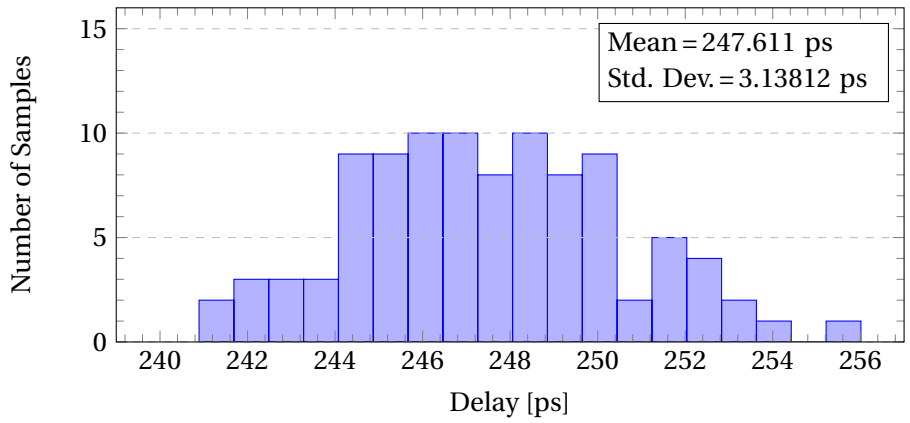


Figure 4.10: Histogram showing the effect of noise on the delay of the ready signal.

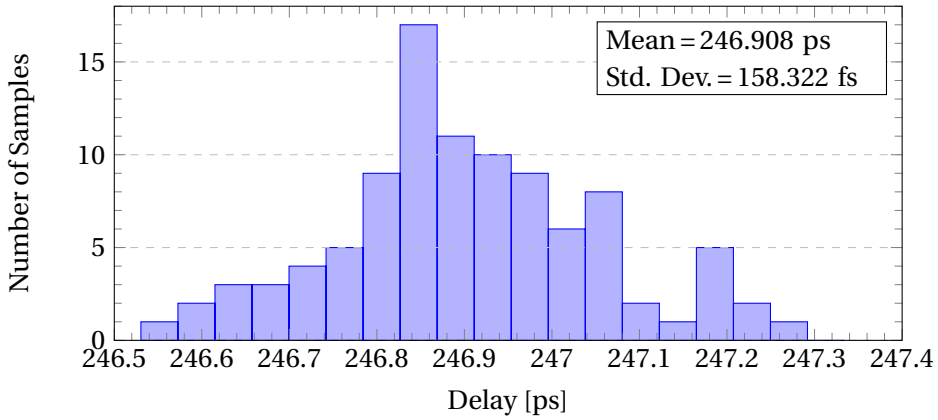


Figure 4.11: Histogram showing the effect of noise on the delay of the reference signal.

delay, and jitter of the SR latch. The comparator input that we would like to detect in this SAR ADC design to extract the new LSB is $V_{DAC\_LSB}/2 = 2.07$ mV. The variation of the comparator delay when $V_{DAC\_LSB}/2 = 2.07$ mV is applied as the input voltage is simulated with transient noise and the histogram of the comparator delay is given in Figure 4.10. Similarly, the variation of the reference delay is simulated with transient noise when the control voltage is adjusted to the value decided by the calibration loop, and the histogram of the reference delay is given in Figure 4.11. The root-mean-square (RMS) jitter of the ready signal is obtained as 3.138 ps while the RMS jitter of the reference signal is only 158 fs.

The SR latch should detect whether the rising edge of the ready signal or the reference signal arrives earlier. Due to noise, the SR latch might not decide correctly depending on how small the time difference between the rising edges of its two inputs (Δt_{SR}). In Figure 4.12, bit-error-rate (BER) values of the SR latch is plotted by sweeping the Δt_{SR}. Using the error function and the BER values obtained, the input-referred RMS jitter of the SR latch is calculated as 180 fs.

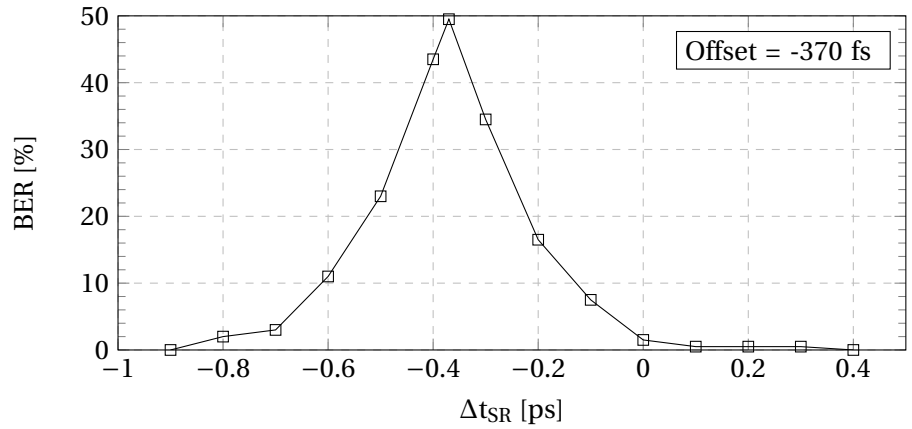


Figure 4.12: BER vs. time difference between the rising edges of the SR latch inputs.

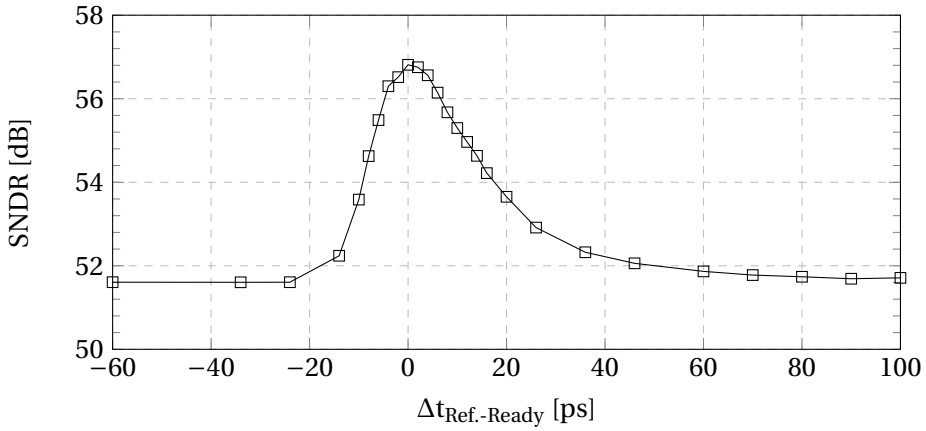


Figure 4.13: SNDR vs. the time difference between the rising edges of the reference and ready signals.

SR latch has 370 fs offset; however, it does not affect the resolution improvement since the calibration loop compensates it. The jitter contribution of the reference delay generator and the SR latch is very small compared to the jitter of the comparator. The total jitter is calculated as 3.147 ps by taking the root-sum-of-squares of all the jitter values obtained.

In Figure 4.13, the signal-to-noise-and-distortion ratio (SNDR) variation of the designed (9+1)-bit ADC against the time difference between the rising edges of the reference and ready signals ($\Delta t_{Ref.\text{-}Ready}$) is plotted. Considering that the SNDR of the 9-bit SAR ADC output is 52.9 dB, the LSB extraction circuit still provides improvement even for $\Delta t_{Ref.\text{-}Ready}$ values between -12 ps and 26 ps. Therefore, SNDR is improved even in the $\pm 3\sigma$ range of the calculated total jitter.

Comparator delay and the reference delay are also sensitive to temperature, supply voltage, and input common-mode variations. To observe the effect of these variations, the reference

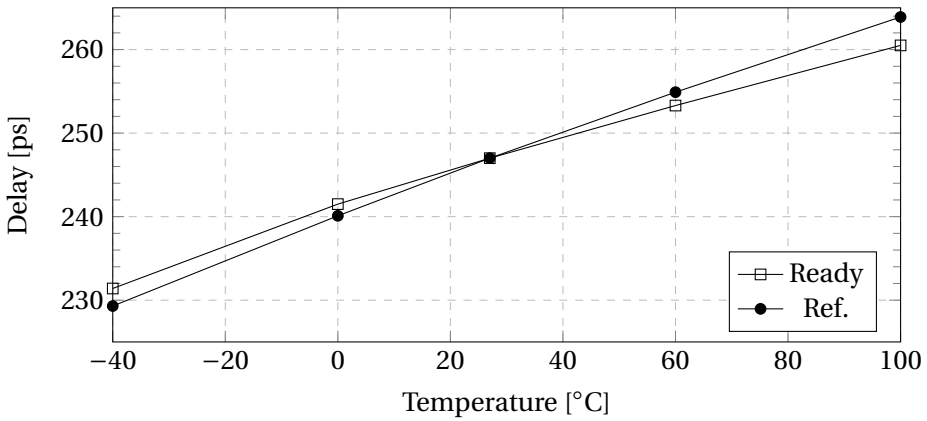


Figure 4.14: Effect of temperature variation on the delays of the ready and reference signals.

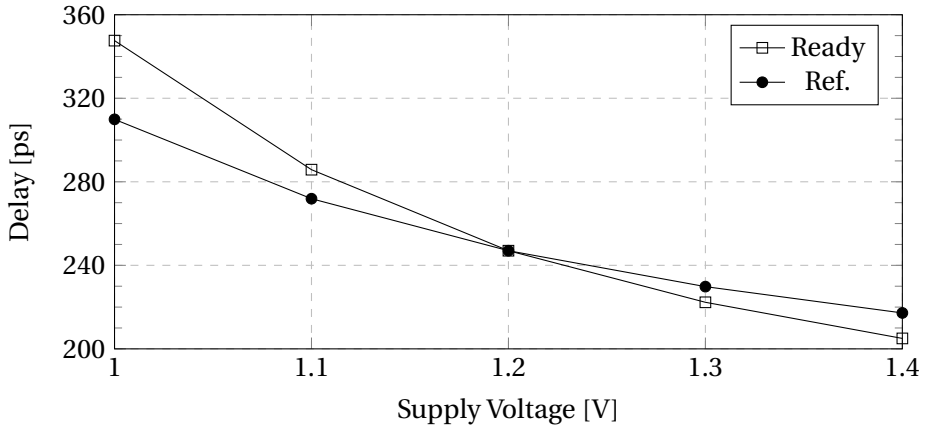


Figure 4.15: Effect of power supply variation on the delays of the ready and reference signals.

delay is foreground calibrated in nominal conditions, then the temperature, supply voltage, and the input common-mode are swept. The effect of these variations on the delay values is given in Figure 4.14, 4.15, and 4.16, respectively. As can be seen in these plots, the ready delay and the reference delay values do not change at the same rate while the conditions change over time. However, background calibration can compensate for the difference between the two delays and provides a robust solution by helping the reference delay to track the ready delay, while the foreground calibration is sensitive to the variations.

The frequency-domain characteristics of the designed (9+1)-bit ADC near Nyquist-rate at sampling rate (f_s) of 200 MS/s, including the LSB extraction circuitry and the background calibration loop acquired from the post-layout simulation is shown in Figure 4.17. Transient noise is included in this simulation to be able to observe the effect of jitter on the resolution improvement. The SNDR value obtained from the 10-bit ADC is 55.76 dB while the SNDR of the 9-bit SAR ADC only is 52.41 dB. Therefore, the LSB extraction from comparator decision

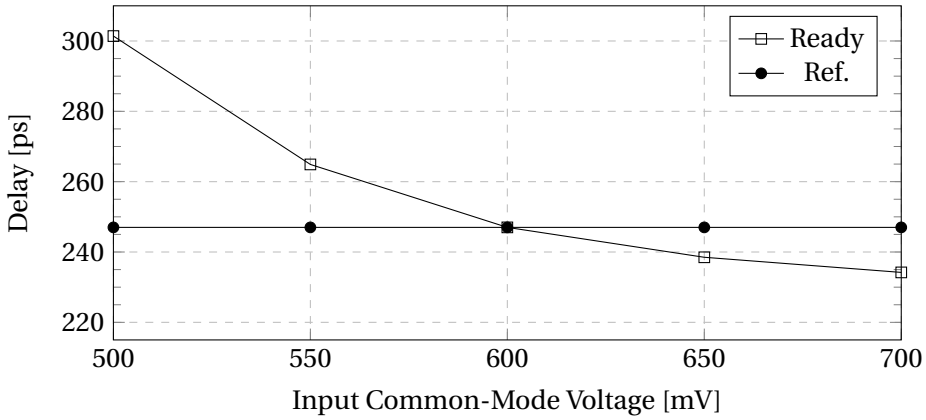


Figure 4.16: Effect of input common-mode variation on the delays of ready and reference signals.

Table 4.1: Performance comparison of the 9-bit SAR ADC and the (9+1)-bit ADC (with LSB extraction and self-calibration circuity).

	9-bit SAR ADC	(9+1)-bit ADC
Technology	65 nm	
Supply Voltage	1.2 V	
f_s	200 MS/s	
$SNDR_{max}$	52.41 dB	55.76 dB
$SFDR_{max}$	63.35 dB	64.81 dB
SNR_{max}	52.91 dB	56.49 dB
$ENOB_{max}$	8.41 bits	8.97 bits
Active Area	0.018 mm^2	0.019 mm^2
Power	1.049 uW	1.084 uW
FoM	15.4 fJ/conv.-step	10.8 fJ/conv.-step

delay increases the SNDR by 3.35 dB. In Table 4.1, the performance comparison of the 9-bit SAR ADC and (9+1)-bit ADC with self-calibrated LSB extraction is given. The typical figure-of-merit (FoM) of ADCs is defined as FoM = Power/($2^{ENOB} f_s$), where ENOB is the effective number of bits. Since the sampling rate is not affected by the implementation of the resolution improvement circuitry, and the increase in the power consumption is very small compared to the ENOB improvement, FoM is also improved.

4.3 Conclusion

In this chapter, a low-power self-calibrated LSB extraction circuitry to be used with SAR ADCs for resolution improvement is proposed, and its implementation on a 9-bit 200 MS/s SAR ADC is presented. The LSB extraction circuit uses comparator decision delay information to double the number of quantization levels without increasing the resolution of the capacitive DAC

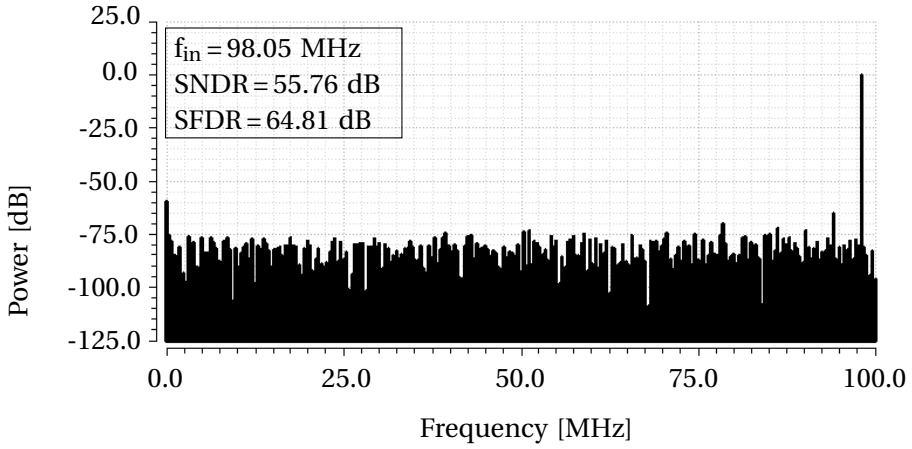


Figure 4.17: FFT plot of the (9+1)-bit ADC with self-calibrated LSB extraction ($f_s = 200$ MS/s).

in the SAR ADC or increasing the number of comparisons in the SAR operation. Since a fast comparator is used in the SAR ADC to increase the speed and the method is based on the comparator decision delay, the effect of comparator noise/jitter on the resolution improvement is analyzed. Implementing this technique does not bring any penalty on the sampling rate of the SAR ADC. The background calibration loop automatically adjusts the reference delay and provides robustness against the temperature, power supply, and input common-mode variations over time. The LSB extraction circuitry and the background calibration loop occupies a small area compared to the overall area of the ADC and cause a small increase in the total power consumption. As a result, post-layout simulations with transient noise show that the proposed self-calibrated resolution improvement circuitry implementation increases the SNDR of the 9-bit 200 MS/s SAR ADC from 52.41 dB to 55.76 dB while the FoM is improved from 15.4 fJ/conversion-step to 10.8 fJ/conversion-step.

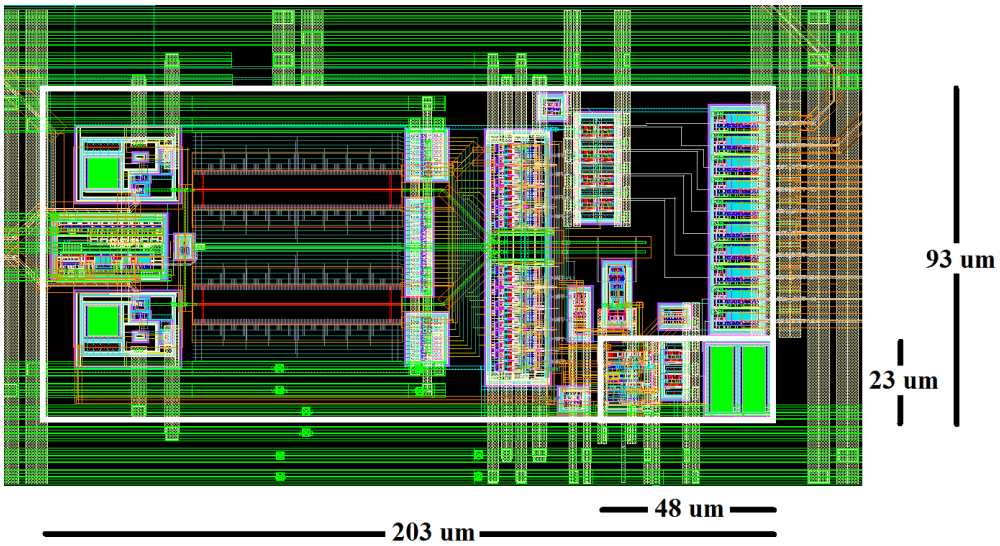


Figure 4.18: Layout of the ADC.

5 Loop-Unrolled SAR ADC

This chapter presents a low-power single-channel 8-bit loop-unrolled (LU) successive approximation register (SAR) analog-to-digital-converter (ADC) with a novel common-mode adaptive background comparator offset calibration scheme. LU-SAR ADCs use multiple comparators to reduce the SAR loop delay. Offset mismatch between the comparators severely degrades the effective resolution. This chapter addresses the common-mode voltage variation in the LU-SAR architecture due to comparator kickback and the problems related to the common-mode dependency of the comparator offset. The proposed offset calibration scheme ensures that the comparators are calibrated at the same input common-mode voltage at which they each operate during the SAR conversion to prevent the common-mode dependent offset mismatch between them. Moreover, the proposed ADC design exploits the common-mode variation immunity of the proposed calibration scheme to optimize the figure-of-merit (FoM). The prototype ADC manufactured in 28 nm FDSOI CMOS achieves 42.57 dB signal-to-noise-and-distortion ratio and 22.8 fJ/conv.-step FoM at 800 MS/s with near Nyquist frequency input, and occupies an area of 0.0037 mm^2.

Outline

This chapter is organized as follows. Section 5.1 provides an overview of the previously published LU-SAR ADC calibration techniques and explains the contribution of proposed calibration scheme. Section 5.2 describes the proposed LU-SAR ADC architecture with common-mode adaptive offset calibration, analyzes the effect of common-mode on the precision of the offset calibration, and explains the design choices to achieve lower FoM. Section 5.3 summarizes the measurement results of the prototype ADC and Section 5.4 concludes the chapter.

5.1 Overview of the LU-SAR ADC Calibration Techniques

The loop-unrolled (LU) SAR architecture uses N comparators for N-bit conversion and the outputs of the comparators control the capacitive digital-to-analog converter (DAC) directly without any additional logic operation. The main challenge of using multiple comparators in an LU-SAR ADC is the offset matching of the comparators. The LU-SAR ADC designs in [30] and [51] use foreground calibration and calibrate the offsets of the comparators by observing the comparator outputs to trim the calibration bits/voltages externally. However, foreground calibration cannot track time-varying process, voltage, and temperature (PVT) variations and each recalibration requires to interrupt the SAR operation. The effect of variations over time might be tolerable in these foreground-calibrated 6-bit ADCs, but it becomes more severe as the resolution increases. Considering the analysis in [52], to target 0.5-bit effective number of bits (ENOB) loss and 99% yield in an 8-bit LU-SAR ADC, the standard deviation of the comparator offset should be lower than 0.15 least significant bits (LSBs).

In an LU-SAR ADC, comparators are triggered one by one without resetting them until the end of the SAR conversion. Every time a comparator is triggered, the common-mode of the capacitive DAC, hence the comparator input common-mode, decreases due to comparator kickback. Due to the accumulation of voltage drops from comparator kickback, the input common-mode varies as the comparators are triggered one after each other. Since the offset of a comparator is dependent on the input common-mode voltage, the common-mode voltage during the calibration and SAR operation should be the same for conversion precision. [52] proposes an LU-SAR ADC with background offset calibration that uses a capacitive DAC with constant common-mode. The comparator kickback in this design does not decrease the common-mode severely since the capacitive load imposed by the DAC is large (512 fF). However, generally a smaller capacitance is preferred in SAR ADCs for speed and power consumption considerations, which renders the common-mode variation due to kickback more severe. In [14] and [39], the cumulative reduction in common-mode is prevented by resetting each comparator right after the decision is complete and before triggering the next comparator. This way, the voltage drop due to kickback is removed before the next comparison starts and the common-mode is kept constant. However, resetting the comparators after the completion of the decision and triggering the next comparator in a way that the comparator clocks do not overlap adds additional delay to the critical path.

In [53], a hybrid calibration scheme for offset calibration in an LU-SAR ADC is proposed. It solves the comparator offset mismatch problem by using coarse foreground calibration for the most significant bit (MSB) comparators and fine background calibration for the LSB comparators with redundancy. That design uses an auxiliary reference comparator whose offset is coarsely foreground calibrated. The offsets of all the fine comparators are calibrated to the offset of the coarsely foreground calibrated reference comparator. Therefore, the offset mismatch between the fine comparators in a single-channel LU-SAR ADC is eliminated. However, the residual offset of the coarsely calibrated reference comparator creates a systematic offset. Although this systematic offset does not degrade the signal-to-noise-and-distortion ratio

(SNDR) for a single-channel ADC, it potentially causes offset mismatch between the channels when used in a time-interleaved architecture. The calibration is performed by triggering the reference comparator at the same time with the comparator which is being calibrated, comparing the comparator output with the reference comparator, and adjusting the calibration voltage accordingly. Additional calibration time is not required for this design, but it tends to lose track when there is a DC or a very low-frequency input because the offset mismatch can be detected only if the reference comparator and the comparator being calibrated give different outputs. The residual offset of the coarsely calibrated reference comparator depends on the time-varying PVT variations because it is foreground calibrated. Moreover, this method requires additional effort to design more than one comparator.

Contribution

In this chapter, we analyze the effect of common-mode voltage variation on the comparator offset and we propose a common-mode adaptive background offset calibration scheme for auto-zeroing the offsets of the comparators in the LU-SAR ADC architecture. The proposed calibration scheme ensures that each comparator is calibrated at the same input common-mode voltage at which they are triggered during the SAR conversion. Therefore, the offset of each comparator is properly calibrated even though the common-mode varies during the SAR conversion. Since the common-mode variation does not affect the precision of the offset-calibration, the common-mode of the capacitive DAC can be manipulated to decrease the noise in LSB decisions in combination with redundancy in the proposed 8-bit LU-SAR ADC design. Hence, lower noise operation for the LSB decisions does not require an additional low-noise comparator design, and identical comparators can be used for all the decisions to minimize the design and layout effort. The common-mode immunity of the proposed calibration scheme provides flexibility for the design of the capacitive DAC as well. The proposed capacitive DAC design uses a combination of capacitor splitting and single-sided switching to reduce both settling time and routing to optimize the FoM. The prototype 8-bit LU-SAR ADC with a novel common-mode adaptive background offset calibration, manufactured in 28 nm FDSOI achieves 42.57 dB SNDR and 22.8 fJ/conv.-step FoM at 800 MS/s with near Nyquist frequency input.

5.2 ADC Architecture

The block diagram of the proposed 8-bit LU-SAR ADC architecture is provided in Figure 5.1 and the corresponding timing diagram for 800 MS/s sampling rate is given in Figure 5.2. The proposed ADC consists of a sampling clock generator block, a capacitive DAC, nine identical comparator stages, a reset signal generation block, and a calibration control logic. The sampling clock generator generates the sampling pulse CK_{SAMP} from the external clock signal CK_{EXT} with 50% duty cycle and then buffers it. The differential analog inputs are sampled into the capacitive DAC with top-plate sampling via sampling switches controlled

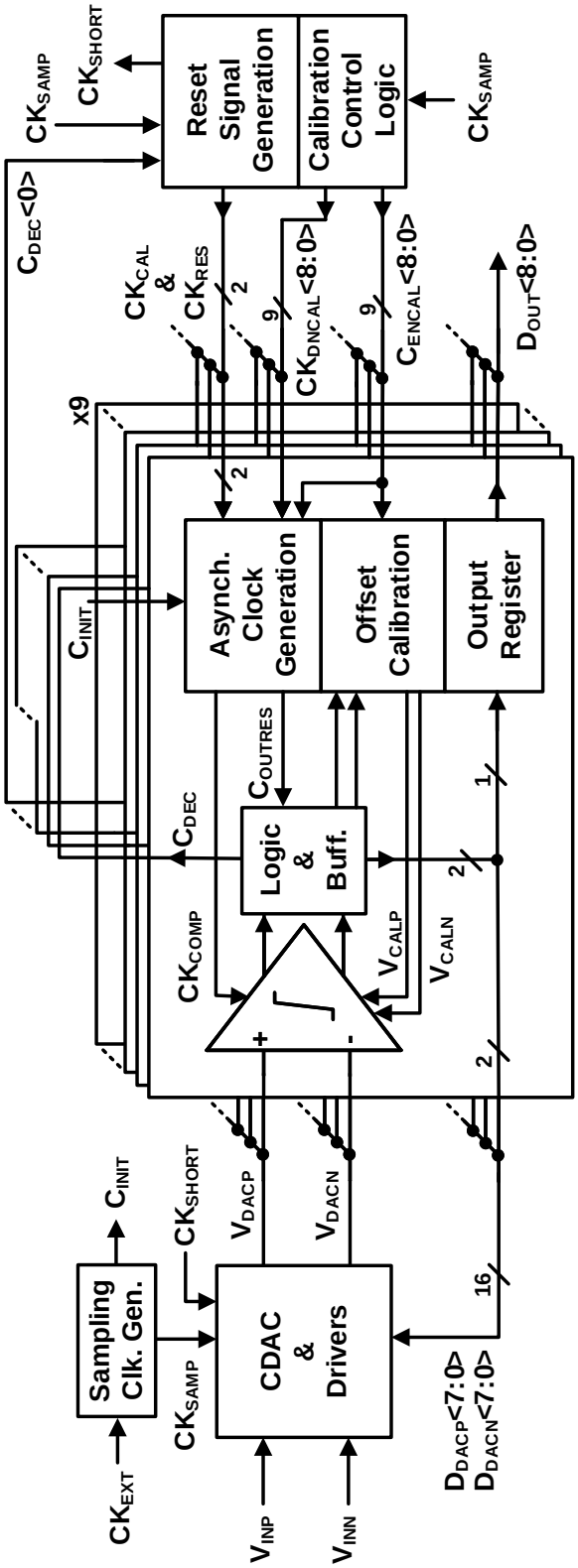


Figure 5.1: Block diagram of the proposed LU-SAR ADC with common-mode adaptive background offset calibration.

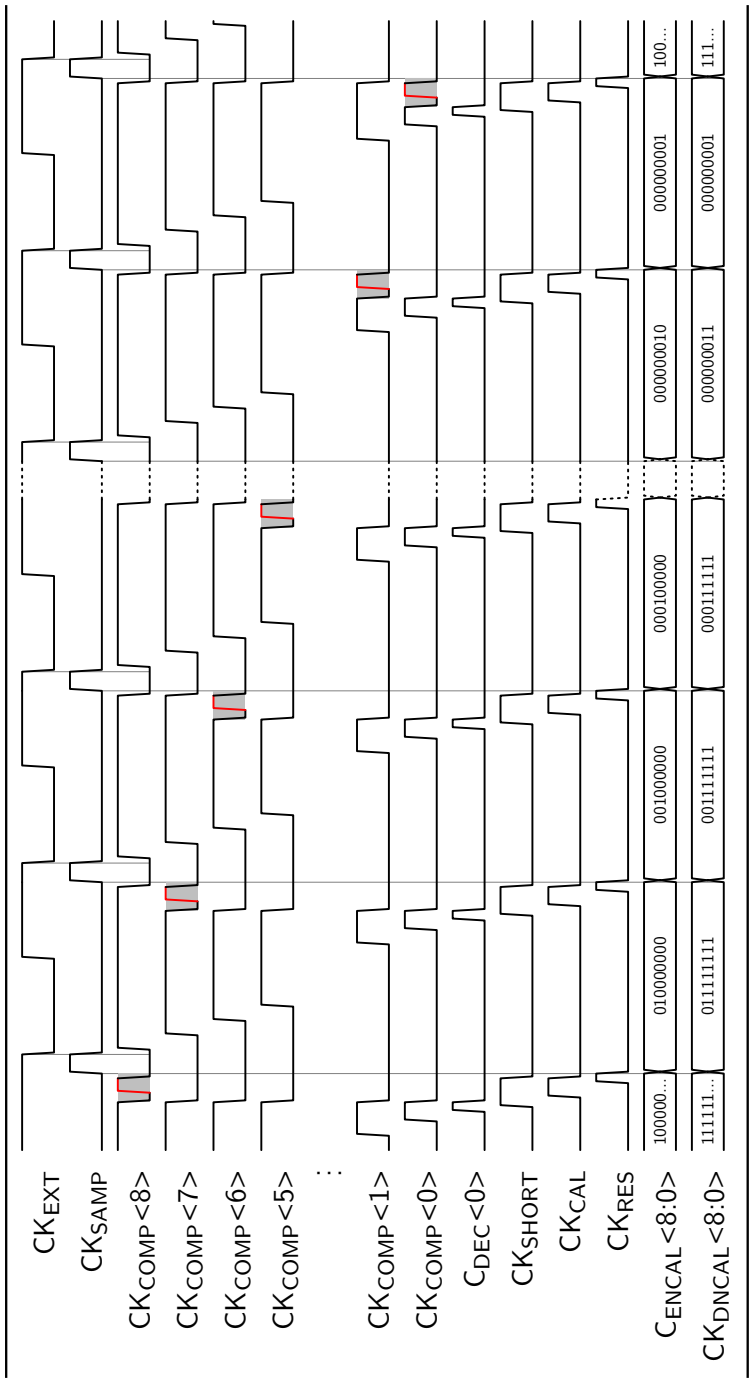


Figure 5.2: Timing scheme of the proposed LU-SAR ADC with common-mode adaptive background offset calibration.

by the CK_{SAMP}. The proposed capacitive DAC has redundancy to provide an error budget for capacitive DAC settling errors and noise. Because of the redundancy, nine decisions are made during the SAR cycle. Each of the nine identical comparator stages consists of a dynamic comparator, logic and buffering at the output of the comparator, an asynchronous clock generation block that generates $CK_{COMP}<N>$, an offset calibration circuit, and an output register.

5.2.1 Timing and the Calibration Scheme

The first comparison starts with the rising edge of $CK_{COMP}<8>$ signal, generated by C_{INIT}, immediately after the sampling phase ends as shown in Figure 5.2. After the completion of the decision in Comparator-*N*, the next comparator is triggered with the rising edge of $CK_{COMP}<N\text{-}1>$, generated by $C_{DEC}<N>$ that indicates the completion of decision-*N*. All the comparators are triggered one by one by their own clock signals generated asynchronously in a ripple fashion until the last comparator. When the last comparator decision, triggered by the rising edge of the $CK_{COMP}<0>$, is complete, $C_{DEC}<0>$ signal becomes logic-1, which indicates the end of the SAR cycle.

After the SAR cycle, the calibration procedure starts by shorting the differential capacitive DAC outputs by CK_{SHORT} signal to provide zero differential input voltage to the comparators during the self-calibration. Comparators are calibrated in rotation; one of the comparators is calibrated in each calibration phase. Which comparator is to be calibrated at the end of a particular conversion cycle is decided by $C_{ENCAL}<8:0>$. The rising edges of the comparator clocks that trigger them for calibration are highlighted in red with gray background in Figure 5.2.

The offset of a comparator is auto-zeroed in the calibration phase. For the same comparator to make a decision with zero-offset at the SAR conversion as well, the common-mode voltage of the comparator during the SAR conversion and the calibration should be the same. To achieve the same common-mode, the corresponding state in the SAR conversion should be provided during the calibration phase for each comparator. Where comparators are numbered from 8 to 0 starting from the one that makes the first decision, the following calibration procedure sets the correct state which provides the desired common-mode voltage for each comparator in the calibration phase. Before the Comparator-*N* is triggered for calibration, all the comparators numbered $\leq N$ and the capacitive DAC bottom plates controlled by these comparators should be reset; all the comparators numbered $> N$ and the corresponding capacitive DAC bottom plates should not be reset. For example, before the Comparator-6 is triggered, Comparators 6-0 and the capacitive DAC bottom plates controlled by these comparators are reset; Comparators 8 and 7 and the corresponding bottom plates are kept as they are. Whether a comparator will be reset or not before the calibration is controlled by 9-bit C_{DNCAL} signal generated by the Calibration Control Logic. If the $C_{DNCAL}<N>$ signal that is sent to Asynchronous Clock Generation Block is logic-1 then $CK_{COMP}<N>$ is pulled-down after the SAR conversion. The capacitive DAC bottom plate controlled by the comparator under calibration is forced to reset

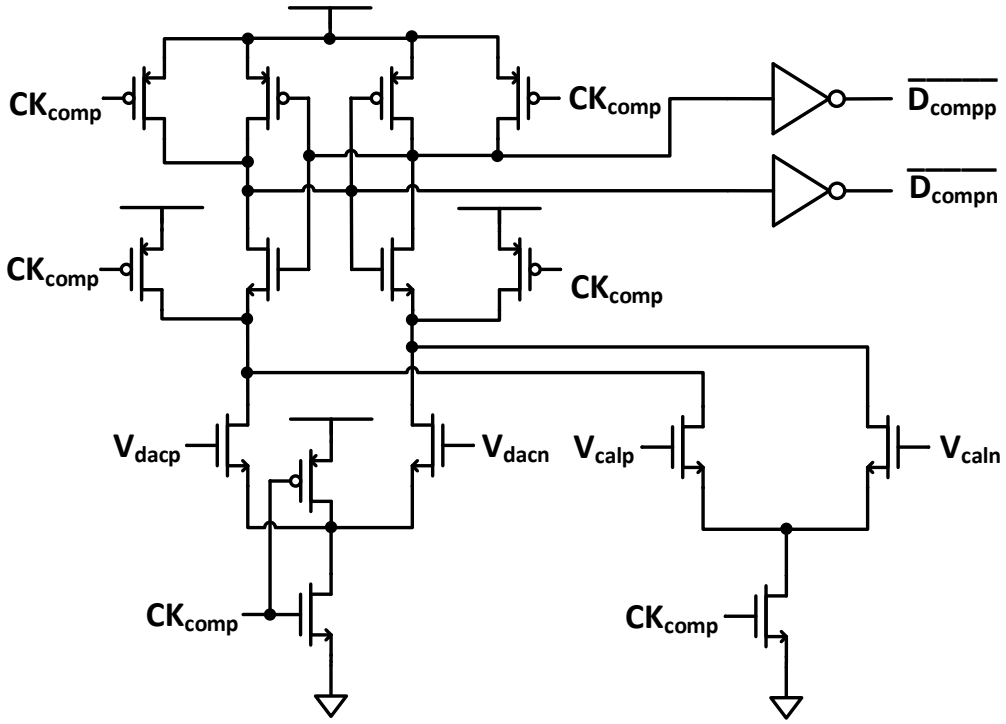


Figure 5.3: Schematic of the comparator.

by the C_{OUTRES} signal to prevent unnecessary capacitive DAC switching during the calibration. Before the new sampling starts, the capacitive DAC and all the comparators are reset by the reset signal CK_{RES}.

Each conversion cycle takes 1.25 ns, which corresponds to 800 MS/s sampling rate. Sampling, conversion, calibration, and reset phases that make up a conversion cycle take approximately 250 ps, 750 ps, 200 ps, and 50 ps, respectively. In the case of a SAR cycle with a longer decision time, the calibration phase can be skipped. Skipping the calibration of a comparator occasionally does not affect the calibration precision. Therefore, the calibration phase provides a margin for the samples with longer decision time.

5.2.2 Comparator

The schematic of the StrongArm latch which is used as a comparator in the proposed LU-SAR ADC is given in Figure 5.3 [27]. It includes an additional smaller differential pair for offset calibration. The internal nodes of the comparator are reset to the supply voltage including the tail of the main differential pair before each comparison, to avoid any memory effect and to ensure that the kickback of the comparator is constant for all the decisions. Monte Carlo simulation results of the comparator offset are given in Figure 5.4. The standard deviation (σ)

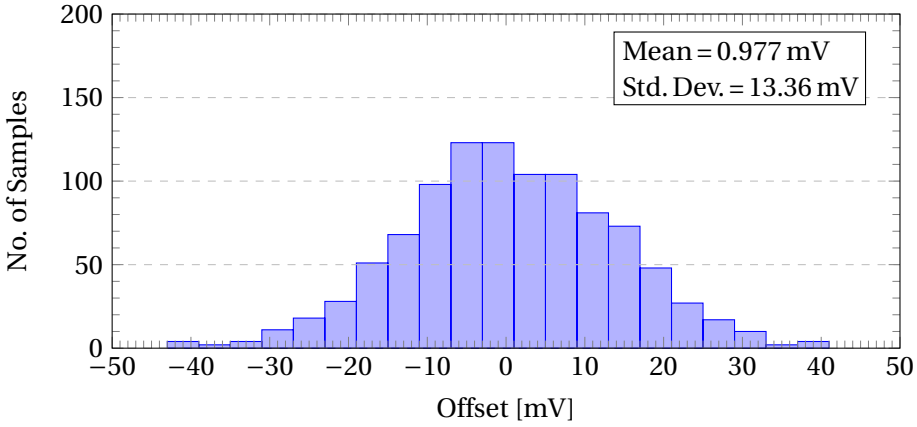


Figure 5.4: Monte Carlo simulation result of the comparator offset at 500 mV input common-mode.

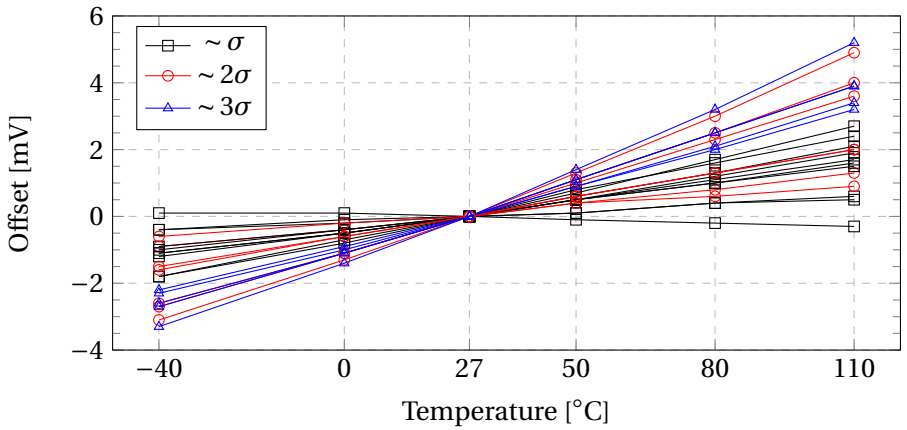


Figure 5.5: Comparator offset vs. temperature (calibrated to zero-offset at 27 °C).

of the input-referred offset voltage is found to be 13.36 mV at 500 mV input common-mode.

The following simulation setup has been created to observe the effect of temperature and input common-mode variation on the comparator offset. The samples from the Monte Carlo simulations have been grouped into those which show $\sim\sigma$, $\sim 2\sigma$, and $\sim 3\sigma$ offsets. Each group has more than one sample because how much the offset changes with variations depends on the source of the mismatch. For example, even if two samples have the same offset value at a certain common-mode voltage, their offsets can be different at another common-mode voltage. To simulate the effect of temperature variation on the comparator offset, first, each sample is foreground calibrated to zero-offset by adjusting the calibration voltage of the comparator at 27 °C. Then, their offsets are simulated by changing the temperature. The corresponding comparator offset versus temperature plot is given in Figure 5.5. Considering the large range of offset values in the plot, background calibration is preferred in the proposed 8-bit LU-ADC to maintain the zero-offset at all operating temperatures by tracking the temperature variations

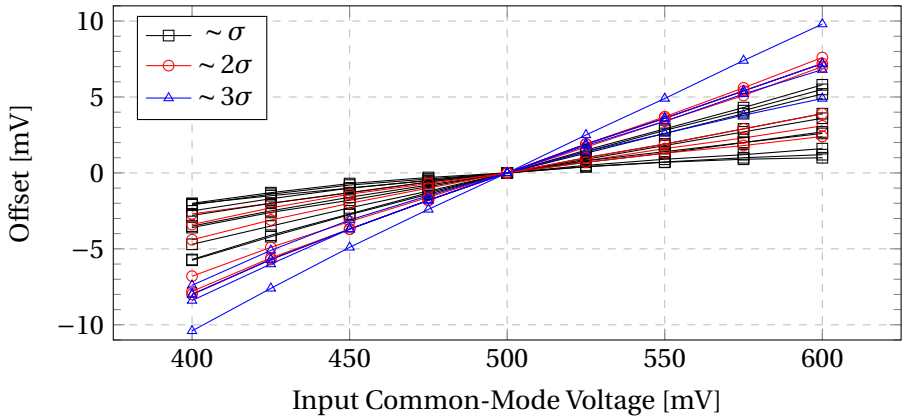


Figure 5.6: Comparator offset vs. comparator input common-mode (calibrated to zero-offset at 500 mV common-mode).

over time.

To observe the effect of common-mode voltage variation on the comparator offset, using the same samples selected from the Monte Carlo simulation, we now consider the case after offset-calibration at 500 mV input common-mode. This time, the comparator offset is simulated by changing the comparator input common-mode between 400 mV and 600 mV. The corresponding comparator offset versus input common-mode is provided in Figure 5.6. This plot shows that ±100 mV change in the common-mode potentially can cause a change in the offset by more than ±10 mV. Hence, the proposed calibration scheme calibrates each comparator at the correct common-mode to avoid potential offset mismatches between the comparators in the considered LU-SAR.

Each comparison causes a common-mode voltage drop of 9.5 mV at the capacitive DAC output. The mismatch between the input differential pair of the comparator might cause a kickback mismatch and create an offset. To simulate the kickback mismatch of a comparator in the ADC, a simulation setup with the same total sampling capacitance as the ADC (100 fF) connected to the input of the comparator is created. Monte Carlo simulations are run and the voltage drop mismatch between the two sampling capacitors, each connected to one of the comparator inputs, is checked. The histogram of the kickback voltage mismatch of a comparator is given in Figure 5.8 and the standard deviation of the mismatch is obtained as 37.86 μV. Since the accumulation of the mismatch voltage drop occurs over time, the kickback creates a dynamic offset. However, the redundancy implemented in the capacitive DAC, which will be explained in detail in the following subsection, can correct decision errors occurring due to kickback mismatch during the SAR conversion up to the last redundant step. In the proposed SAR ADC, there are only three comparisons that take place after the redundant step and one of them is the LSB comparison, that does not cause dynamic offset. Therefore, there are only two comparisons with kickback mismatch that can cause a dynamic offset and the standard deviation of the error due to dynamic mismatch is only $\sqrt{2\sigma^2} = 53.54\,\mu$V,

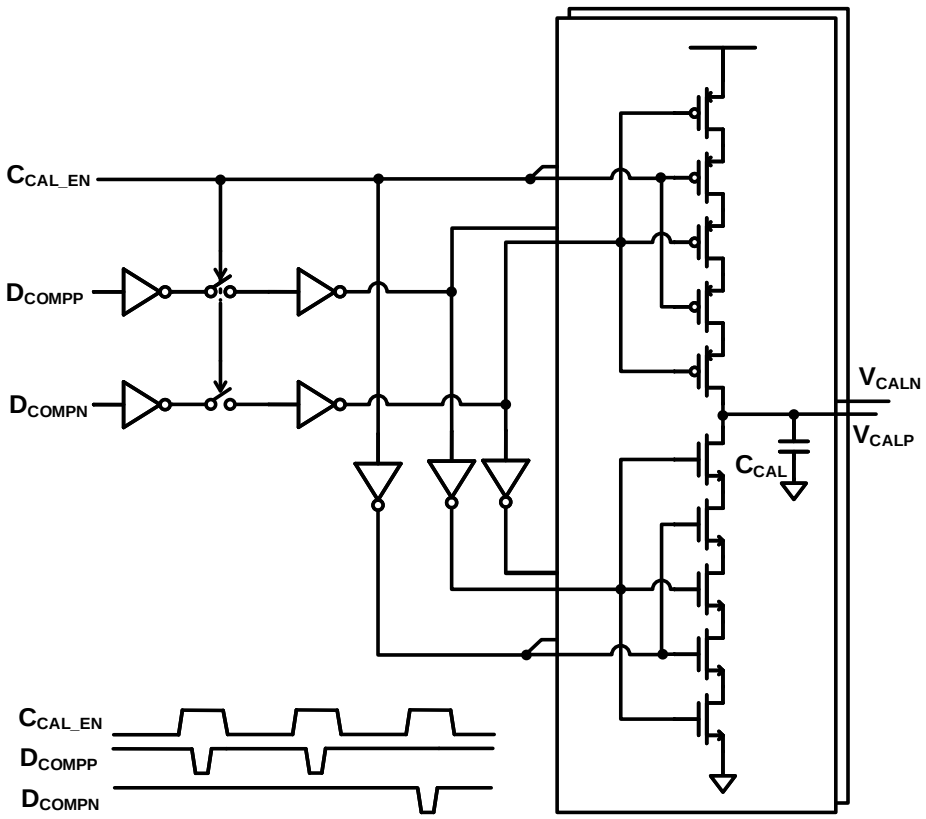


Figure 5.7: Schematic of the comparator offset calibration circuit.

which is very small. Even though the redundancy corrects the dynamic errors and prevents SNDR degradation for a single-channel ADC, the accumulated kickback mismatch might still create a systematic offset that can cause an offset mismatch between the channels in a time-interleaved architecture. Using the standard deviation value obtained from the Monte Carlo simulation, we can calculate the standard deviation of the potential systematic offset due to kickback mismatch. Including the kickback of the eight comparators until the LSB comparison, the standard deviation of the systematic offset is calculated as $\sqrt{8\sigma^2} = 107.08\,\mu$V which is tolerable, considering that the LSB voltage is 4.5 mV.

The background offset calibration of the comparators is performed by the auxiliary differential pair added to the comparator and the low-power charge-based calibration circuit shown in Figure 5.7 [39]. Providing a calibration voltage with small calibration steps is crucial to reduce the residual offset. Moreover, having smaller calibration steps prevents large jumps in the calibration voltage due to comparator noise. To achieve smaller calibration steps, either the calibration capacitor C_{CAL} should be large or the charge switched into C_{CAL} should be small. Since nine separate calibration circuits are used in the design, choosing a large C_{CAL} value increases the area significantly. To avoid using a large C_{CAL}, the calibration circuit

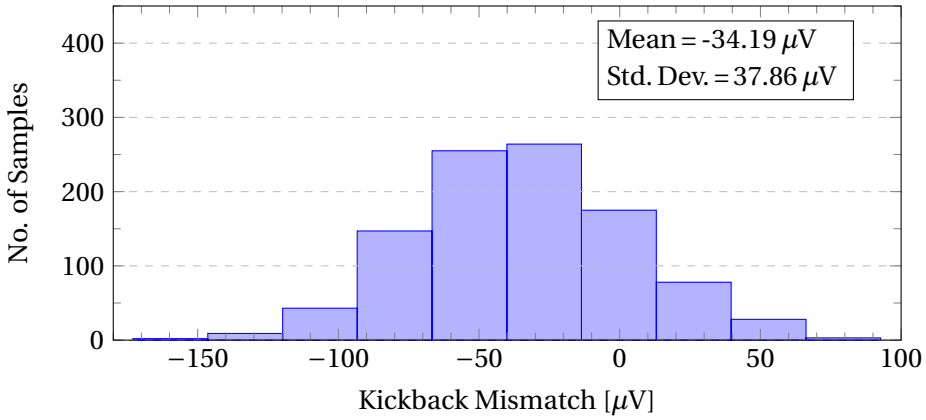


Figure 5.8: Monte Carlo simulation result of the comparator kickback mismatch.

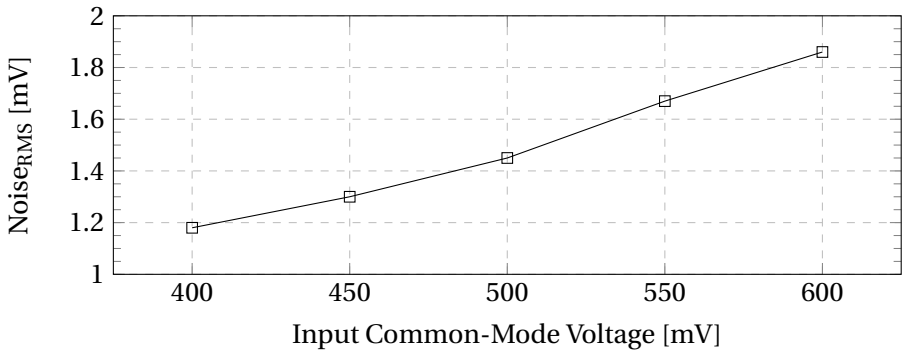


Figure 5.9: Input referred RMS noise vs. input common-mode voltage of the comparator (at 80 °C).

performs charge division by using multiple charge-sharing nodes to reduce the amount of charge switched into C_{CAL}.

5.2.3 Capacitive DAC

The schematic of the capacitive DAC with redundancy is given in Figure 5.10. The differential analog inputs are top-plate sampled into the capacitive DAC via bootstrapped switches [44] for improved linearity. Cross-coupled and constantly turned-off transistors which have the same size as the sampling switches are added to compensate for signal feed-through for high-frequency input. The topology of the capacitive DAC is based on the set-and-down capacitor switching method [24, 25]. Thanks to the top-plate sampling, the first comparison starts immediately after the sampling without any switching before the first comparison. The bottom plates of the capacitive DAC are directly controlled by the comparator outputs without additional logic. During the sampling phase, all the comparators are reset; hence, the corresponding capacitive DAC control bits ($D_{DACP/N}$) are all set to logic-1. Then, during the SAR conversion, either $D_{DACP}<N>$ or $D_{DACN}<N>$, goes to logic-0 depending on the com-

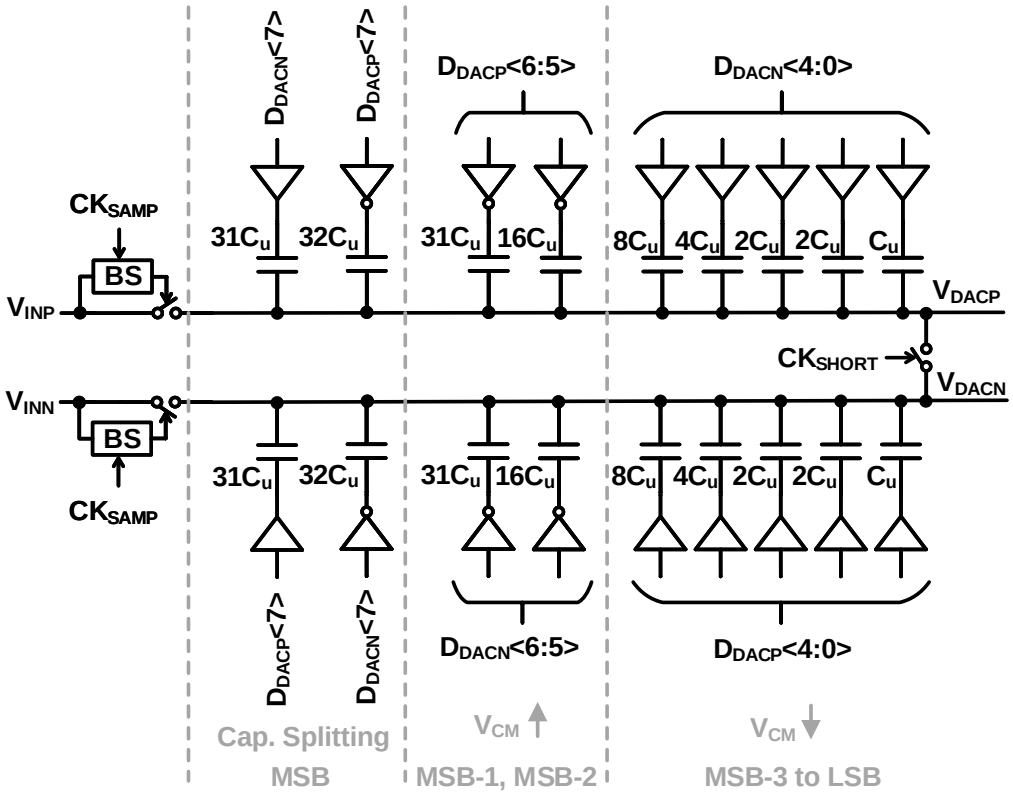


Figure 5.10: Schematic of the capacitive DAC.

parator decision. Redundancy is applied in the capacitive DAC to provide an error budget for dynamic decision errors due to incomplete capacitive DAC settling and comparator noise. The redundancy is applied by decreasing the weights of the MSB and MSB-1 capacitors by 1 unit capacitor (C_u) and adding the $2C_u$ reduced from MSB and MSB-1 capacitors as a redundant step at LSB+2. Thanks to the redundancy, dynamic errors during the SAR conversion can be recovered until the last redundant step (LSB+2).

A further concern is the comparator noise. RMS input-referred noise of the comparator versus the input common-mode voltage is plotted in Figure 5.9. Noise decreases as the common-mode decreases; therefore, lower common-mode is desired for better noise performance. However, decreasing the common-mode slows down the comparator [27]. Since the proposed ADC employs redundancy, only the noise of the comparisons after the last redundant step is critical. Because the proposed calibration scheme provides flexibility in terms of common-mode variation during the SAR operation, the SNDR of the ADC can be improved by using lower common-mode only for those last decisions.

To achieve the same differential DAC voltage step during the SAR conversion, there are two single-sided switching direction options: whether the bottom plate control bit of the Nth

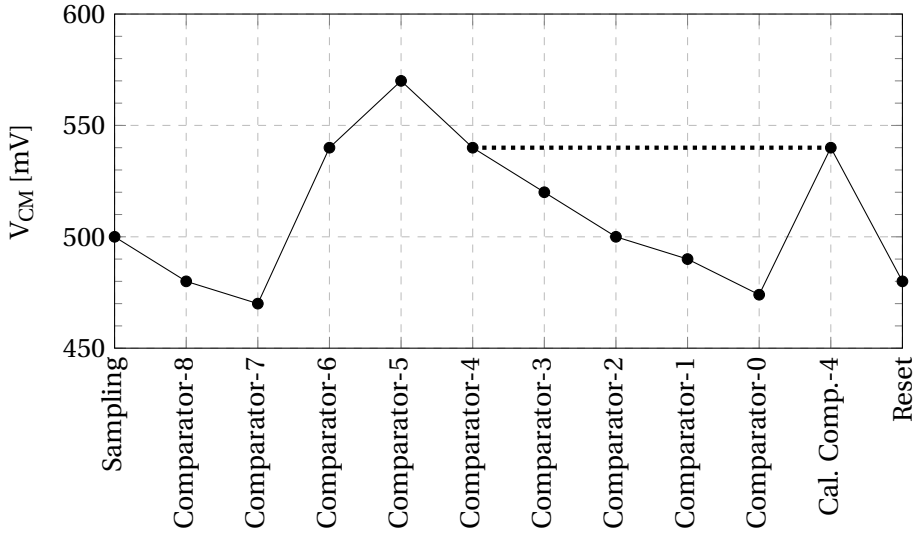


Figure 5.11: Common-mode voltage during SAR conversion.

capacitor in the capacitive DAC transitions 1) from logic-1/0 to logic-0/1 in the top row (P-side), or 2) from logic-0/1 to logic-1/0 in the bottom row (N-side). The output common-mode voltage of the capacitive DAC is dependent on the direction of the switching. Therefore, the common-mode can be adjusted by controlling the switching direction. Capacitor splitting [26] is applied to only the MSB capacitors. Splitting the MSB capacitors helps to avoid a large change in the common-mode. Moreover, the settling is faster when the capacitor is split, which is especially desirable for the MSB switching since it has the longest settling time. On the other hand, single-sided switching requires less routing from comparator output to the capacitive DAC. Therefore, the rest of the switching is single-sided. The noise of the last three decisions affects the SNDR performance directly because their decision errors due to noise cannot be recovered with redundancy. Consequently, lower common-mode voltage is desirable for the last three decisions. MSB-1 and MSB-2 switchings are arranged in the direction that increases the common-mode for faster comparator decisions. Then, to provide lower common-mode to the last decisions, the common-mode is gradually decreased by arranging the directions of all the remaining switchings in the direction that decreases the common-mode. The common-mode voltage at which each comparator is triggered is shown in Figure 5.11.

Finally, the power efficiency of the capacitive DAC is an important factor to achieve a low FoM value. The size of the unit capacitors should be small, but have sufficient matching. Besides, the layout of the capacitive DAC should be as compact as possible to minimize the routing. Therefore, the capacitive DAC is custom-designed as an array of 0.5 fF metal-metal unit capacitors [54].

Table 5.1: Performance comparison of the LU-SAR ADC.

	[27]	[55]	[56]	[30]	[51]	[52]	[53]	**This work**
CMOS Technology	32 nm SOI	28 nm	28 nm	40 nm	40 nm	130 nm	40 nm	**28 nm FDSOI**
Power Supply [V]	1	0.9	1	1	1.2	1.2	1.1	**1**
Resolution [bits]	8	8	7	6	6	8	8	**8**
Sampling Rate [GS/s]	1.2	1	1.25	1.25	0.7	0.15	0.35	**0.8**
$SNDR_{Nyq.}$ [dB]	39.3	43.6	40.1	26.8	34.8	42.9	43.7	**42.57**
Power [mW]	3.06	3.2	3.6	6.08	0.95	0.64	1.37	**2**
$FoM_{Nyq.}$ [fJ/conv.-step]	34	25.3	43.4	272	30	37.5	31.3	**22.8**
Area [mm^2]	0.0015	0.00675	0.0071	0.014	0.0043	0.048	0.0161	**0.0037**
Architecture	SAR Alternating 2-Comp.	SAR Coarse & Fine Comp.	SAR Single Comp.	LU-SAR	LU-SAR	LU-SAR	LU-SAR	**LU-SAR**
Offset Calibration	Background	Background	-	Foreground	Foreground	Background	Hybrid	**Background**

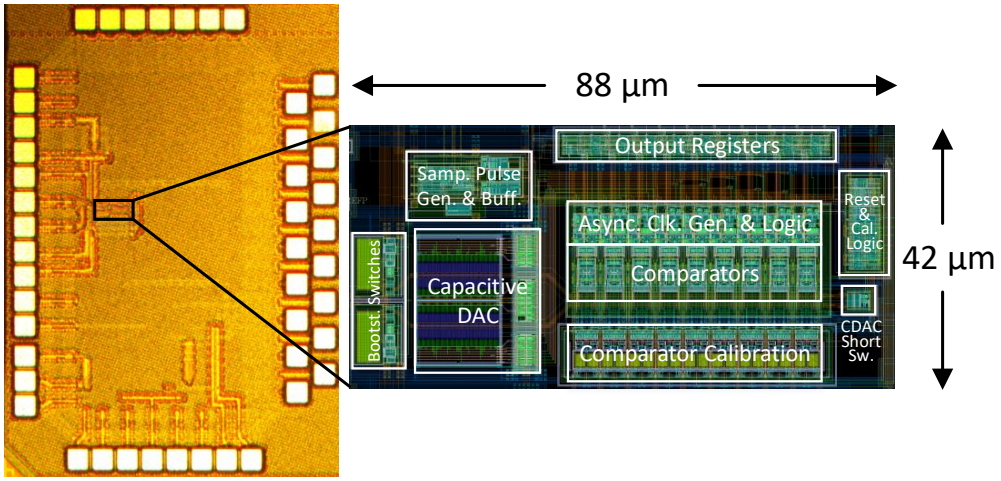


Figure 5.12: Chip micrograph.

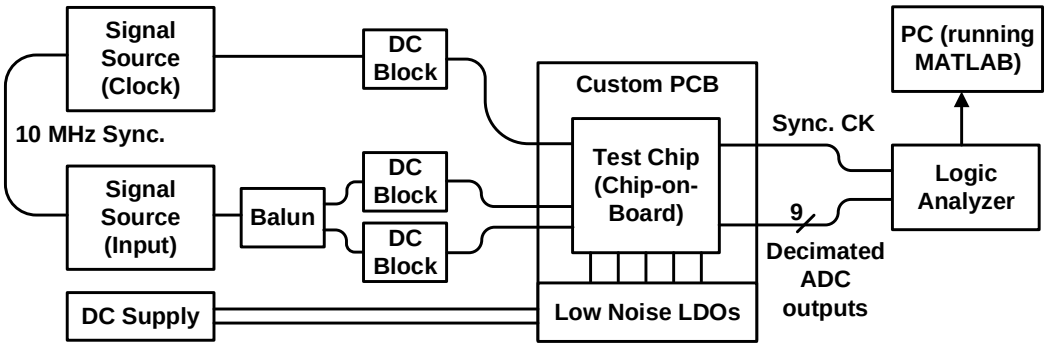


Figure 5.13: Measurement setup.

5.3 Measurement Results

The ADC is manufactured in 28 nm FDSOI CMOS process and it occupies an active area of 88 μm × 42 μm (0.0037 mm^2) as shown in the chip micrograph in Figure 5.12. The measurement setup is given in Figure 5.13. The chip is wire-bonded on a custom printed circuit board (PCB). The required supply voltages for the different domains in the chip is generated by low-noise low-dropout (LDO) regulators on the measurement PCB. The analog input and clock signals are provided by two synchronized signal sources. The single-ended analog input signal is converted into a differential signal using a broadband balun. The digital ADC outputs are decimated by 13 on-chip, then sampled by a logic analyzer using a sampling clock generated on-chip and synchronized to the ADC outputs, and finally processed with MATLAB.

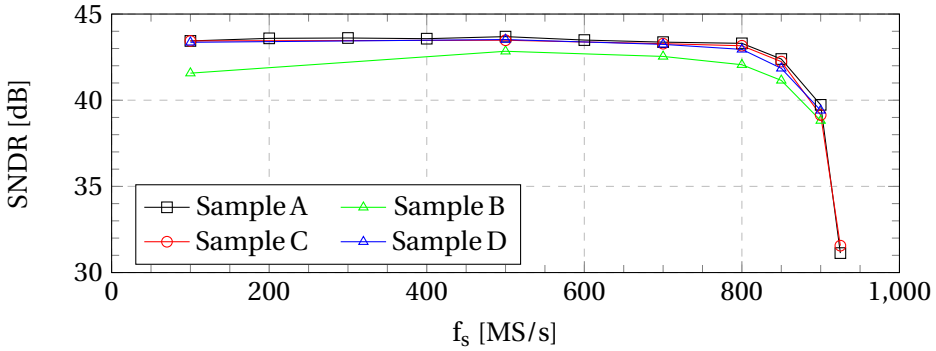


Figure 5.14: SNDR vs. sampling frequency plots for different chip samples ($f_{in} \approx 18$ MHz).

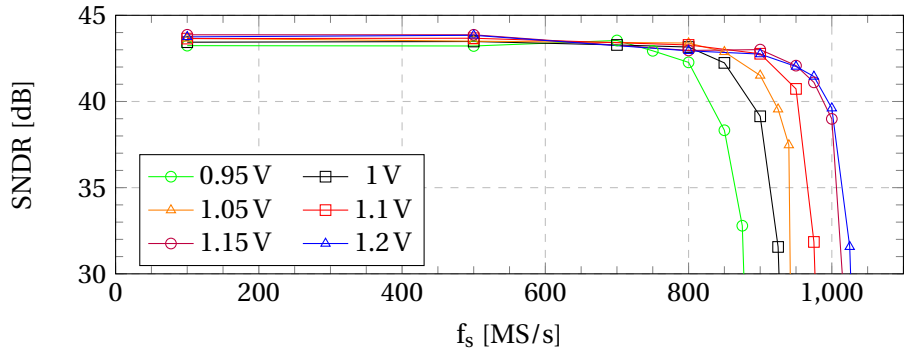


Figure 5.15: SNDR vs. sampling frequency plots for different supply voltages ($f_{in} \approx 18$ MHz).

The SNDR versus sampling rate (f_s) plot for four different chip samples with low-frequency input and nominal 1 V supply voltage is given in Figure 5.14. The three of the four chip samples have almost the same characteristics while the SNDR of one is slightly lower than the rest. The SNDR starts to degrade after 800 MS/s because the offset calibration of the comparators which takes place after each SAR conversion cannot be completed anymore. All the remaining results in this section are measured using Sample A. Figure 5.15 shows the SNDR versus sampling rate plot for various supply voltage values. Up to 1.15 V supply voltage, the sampling rate at which the SNDR starts to roll off increases as the supply voltage increases.

Figure 5.16 shows the measured spectra with low-frequency input and near Nyquist rate input. The measured SNDR and SFDR values are 43.30 dB and 54.90 dB with low-frequency input while they are 42.57 dB and 50.70 dB with near Nyquist rate input at 800 MS/s, respectively.

The measured differential non-linearity (DNL) and integral non-linearity (INL) plots are given in Figure 5.17. With 18 MHz sinusoidal input at 500 MS/s, the max./min. DNL is measured as 0.74/-0.53 LSB and INL as 0.59/-0.65 LSB. The systematic jump at 1/2 full-scale input occurs due to the mismatch of the MSB capacitor in the capacitive DAC layout [57].

Figure 5.21 shows the SNDR and SFDR values measured by sweeping the input frequency (f_{in}) in the first Nyquist zone at 800 MS/s sampling rate. SNDR, power consumption, and

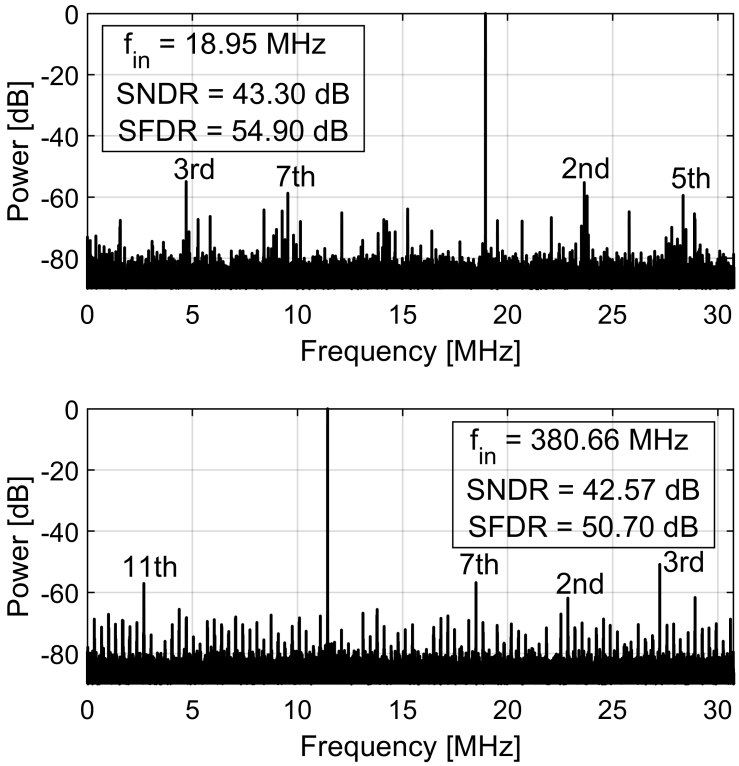


Figure 5.16: Measured power spectral density, f_{samp} = 800 MS/s (ADC outputs are decimated by 13).

the corresponding FoM versus sampling rate plots with near Nyquist rate input are given in Figure 5.18. Power consumption scales with the sampling rate because all the blocks in the ADC are fully dynamic. Therefore, the corresponding FoM plot is nearly flat from 300 MS/s to 800 MS/s. FoM increases slightly at lower sampling rates since the power consumption does not exactly scale down with the sampling rate due to leakage. At sampling rates higher than 800 MS/s, the reason for the FoM degradation is the degradation in SNDR. The ADC achieves 22.8 fJ/conv.-step and consumes only 2 mA from 1 V supply at 800 MS/s. The corresponding power breakdown based on simulations is provided in Figure 5.22.

The performance of the ADC is summarized and compared with the other single-channel high-speed state-of-the-art SAR ADCs and other LU-SAR ADCs in TABLE 5.1. The prototype ADC with the proposed calibration scheme achieves the lowest FoM among the designs listed in the table.

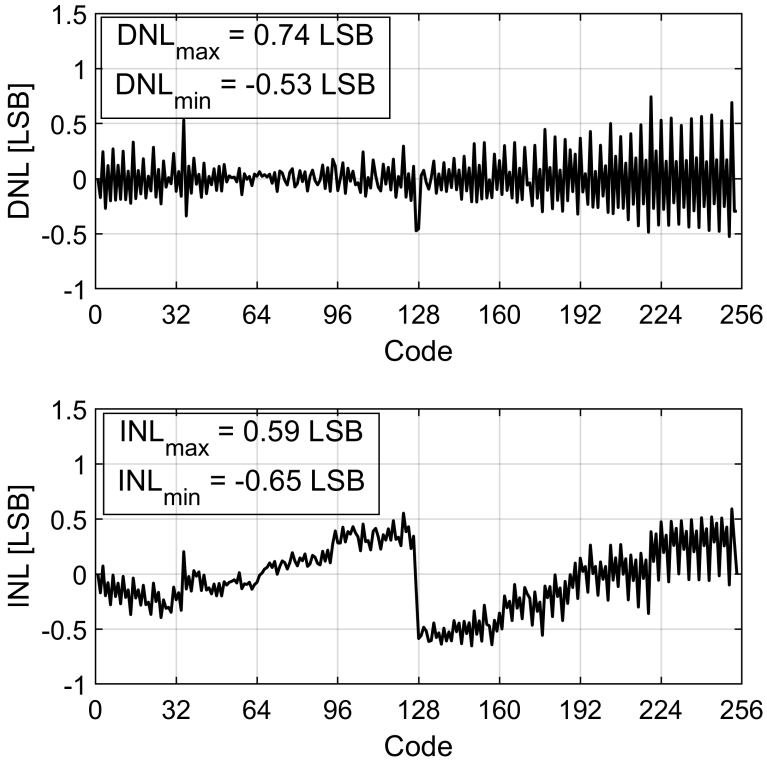


Figure 5.17: Measured DNL and INL.

5.4 Conclusion

This chapter has presented a low-power single-channel 8-bit 800 MS/s LU-SAR ADC with a novel common-mode adaptive background comparator offset calibration scheme. The common-mode adaptive background offset calibration scheme ensures that the offset of each comparator is calibrated to zero at the input common-mode at which they each operate during the SAR conversion. Moreover, the noise of the ADC is decreased by lowering the common-mode towards the LSB decisions without increasing the power consumption or designing an additional lower-noise comparator, thanks to the common-mode variation immunity of the proposed offset calibration scheme combined with the redundancy. The effectiveness of the proposed calibration scheme and the power efficiency of the proposed ADC design have been verified by the measurement results of the prototype ADC manufactured in 28 nm FDSOI CMOS. The prototype achieves a Nyquist Walden FoM of 22.8 fJ/conv.-step and 42.57 dB SNDR at 800 MS/s and occupies an area of 0.0037 mm^2.

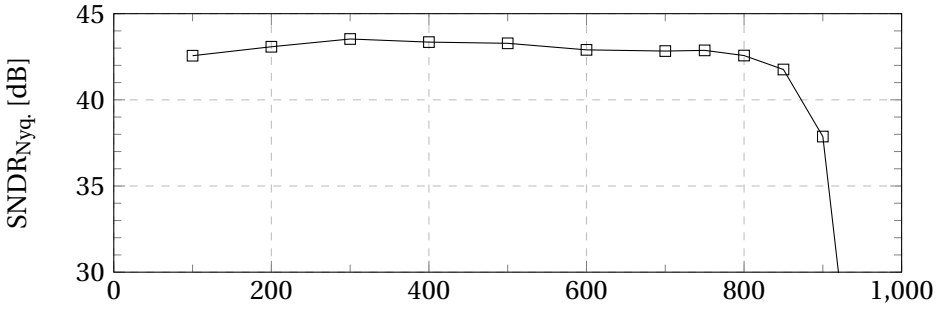


Figure 5.18: SNDR vs. sampling rate (with near Nyquist rate input).

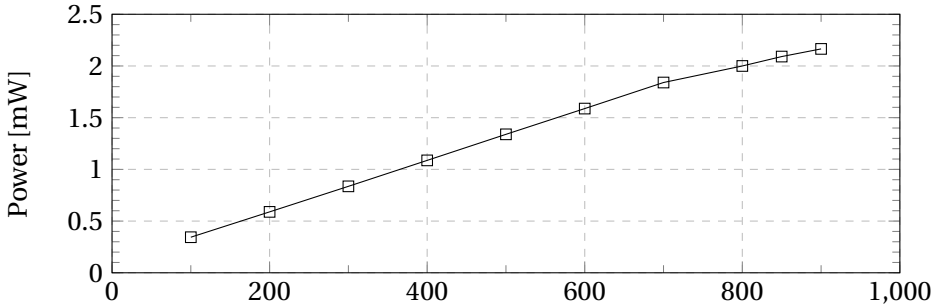


Figure 5.19: Power consumption vs. sampling rate (with near Nyquist rate input).

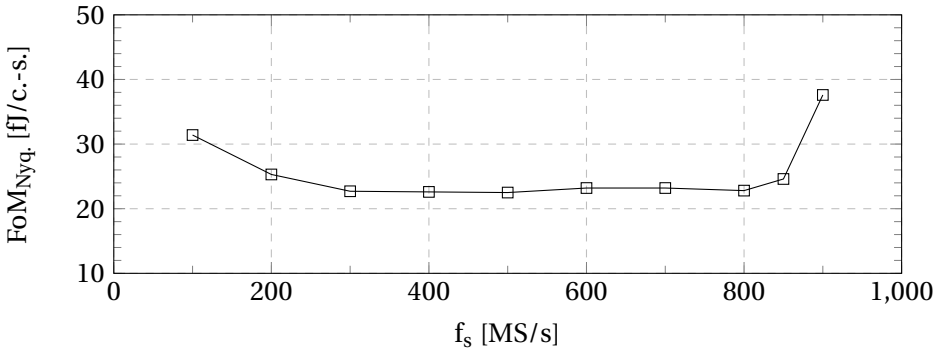


Figure 5.20: FoM vs. sampling rate (with near Nyquist rate input).

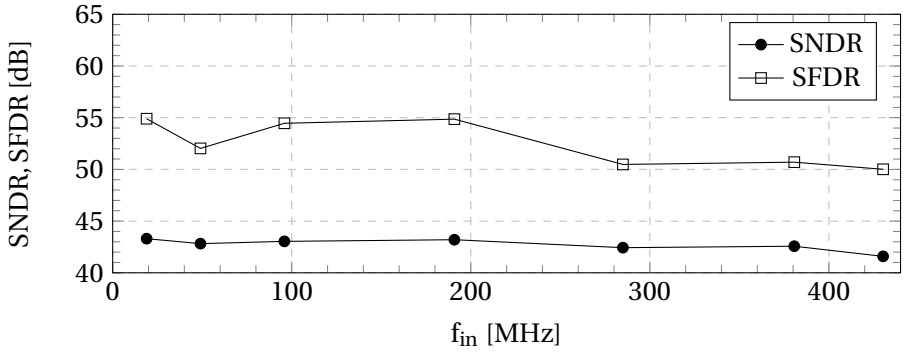


Figure 5.21: SNDR vs. input frequency, $f_{samp} = 800$ MS/s.

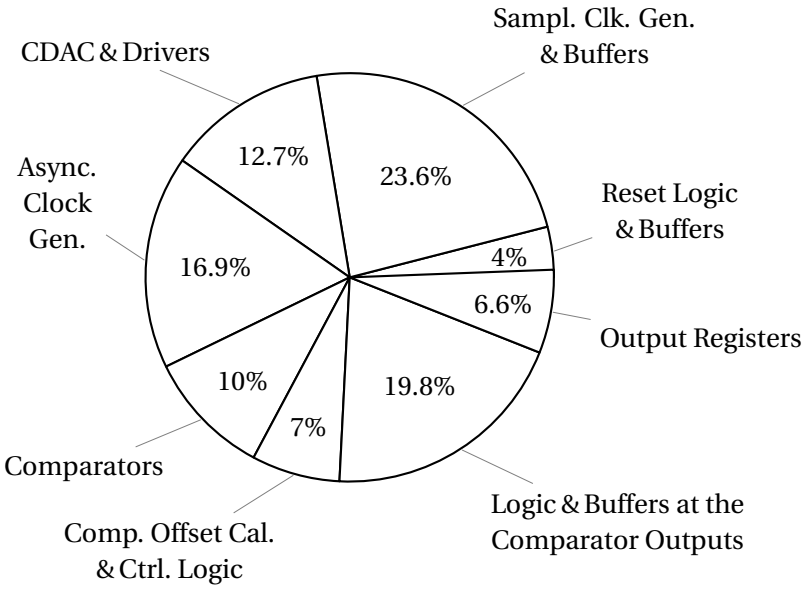


Figure 5.22: Power breakdown.

6 ADC-Based Receiver[1]

This chapter presents an ADC-based receiver analog front-end compatible with high order pulse amplitude modulation (PAM). The ADC-based RX AFE employs a CTLE and an 8 GS/s 8×TI SAR ADC with embedded 2-tap analog FFE and provides 32 Gb/s data rate for PAM-16.

Outline

This chapter is organized as follows. In Section 6.1, the pulse amplitude modulation is reviewed and the results of a modeling study are summarized to decide the optimum modulation order for the target moderate-loss channel at the target data rate of 32 Gb/s. The ADC-based RX AFE architecture is described in Section 6.3. The circuit details of the 8 GS/s 8×TI SAR ADC with embedded 2-tap analog FFE is explained in Section 6.4. The simulation results of the system consisting of an SST transmitter and the ADC-based RX AFE are given in Section 6.5. The chapter is concluded in Section 6.6.

6.1 Pulse Amplitude Modulation

6.1.1 Overview

As the bandwidth of the wireline links increases to reach higher data rates, the channel losses that the circuit designers have to deal with increased as well. To compensate for the high channel loss, more extensive equalization techniques are introduced at the expense of increased power consumption. For the data rates over 40 Gb/s, designs moved from PAM-2 to PAM-4 to halve the bandwidth and decrease the amount of channel loss that needs to be equalized [10].

PAM-2, also known as non-return-to-zero (NRZ), transmits only one bit per symbol. It has two voltage levels representing logic-1 and logic-0. PAM-4 transmits 2-bits per symbol using

[1] This chapter is based on: F. Celik, A. Akkaya, and Y. Leblebici, "A 32 Gb/s PAM-16 TX and ADC-Based RX AFE with 2-Tap Embedded Analog FFE in 28 nm FDSOI," *Microelectronics Journal,* vol. 108, 2021, 104967, [58].

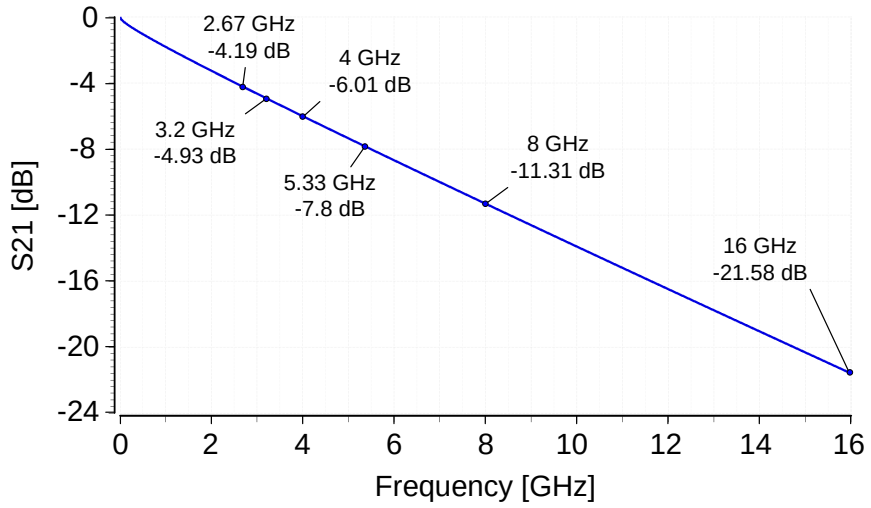


Figure 6.1: Loss characteristic of the channel.

four voltage levels. Because each symbol represents the information of two bits, PAM-4 has half the Nyquist frequency of PAM-2 and doubles the throughput for the same Baud rate. At 32 GS/s data rate, the Nyquist frequency for PAM-4 is 8 GHz while it is 16 GHz for PAM-2. The advantage of having half the Nyquist rate is that the channel loss at the Nyquist frequency lower for PAM-4 compared to PAM-2. On the other hand, PAM-4 has one-third of the vertical opening that PAM-2 has, assuming that the total swing is the same for both. Therefore, the SNR of PAM-4 is worse than the PAM-4 and PAM-4 is more sensitive to noise and residual ISI [59].

Similarly, PAM-8 transmits 3-bits per symbol using eight voltage levels and PAM-16 transmits 4-bits using sixteen voltage levels. Therefore, for the same target data rate, the Nyquist frequency is one-third and one-fourth, respectively, compared to PAM-2. For a moderate-loss channel, the channel losses at Nyquist frequency are shown for PAM-64,32,16,8,4,2 in Figure 6.1 at the target data rate of 32 Gb/s.

6.1.2 Modulation Order

As the PAM order increases, the channel loss that needs to be compensated for decreases. Since the complexity and power consumption of the equalizer can potentially be decreased by decreasing the Nyquist frequency, using higher order PAM can potentially offer better energy efficiency. On the other hand, the multi-bit per symbol operation in high order PAM could make the digital equalization circuits more challenging, complex, and power-hungry. However, using analog equalization only instead of digital equalization can provide equalization capability independent from the PAM order and help to avoid the complexity of the digital equalization circuits with high order PAM.

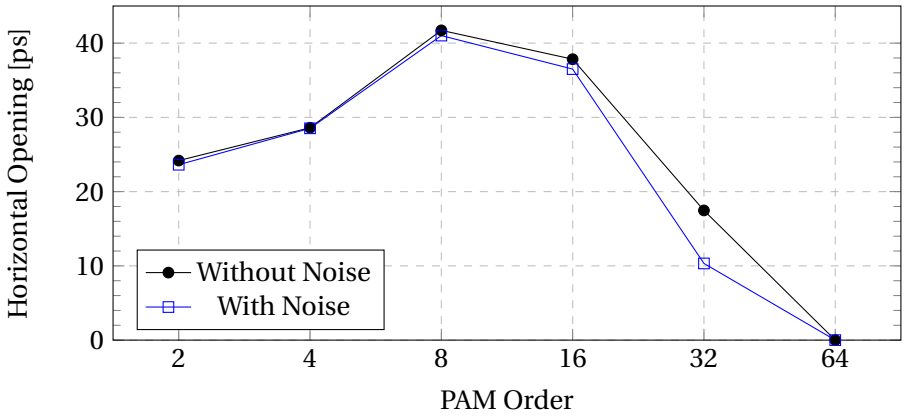


Figure 6.2: Horizontal eye-opening values of different PAM orders.

To decide the optimum PAM order for the target channel shown in Figure 6.1 at the target data rate of 32 Gb/s, a simulation setup is built using behavioral models. The setup consists of a PAM-N transmitter driving the target channel and a receiver with a CTLE and 2-tap analog FFE block. Since the circuit level system is planned to have analog-only equalization, the simulation setup is built accordingly. The setup is simulated for different PAM orders at 32 Gb/s and the CTLE and 2-tap analog FFE parameters are optimized for each PAM order. The simulated horizontal eye-opening for each modulation order is plotted in Figure 6.2 without noise and with injecting 1 mV_{RMS} noise at the input of the CTLE. As can be seen in the plot, the noise does not change the comparative performance. The reason is that the effect of ISI is the main limiting factor. PAM-8 and PAM-16 gives the largest eye openings. Since PAM-16 requires a lower operating frequency for the TI ADC, PAM-16 is chosen as the target modulation order.

6.2 Transceiver System

The transceiver system consists of a transmitter and an ADC-based receiver analog front-end. The SST transmitter is compatible with PAM-2, PAM-4, PAM-8, and PAM-16; one of these modulation orders can be selected by changing the modulation order selection bits.

The transmitter does not have any equalization capability to avoid the complexity. The swing at the receiver input is 1 V_{ppd}. All the equalization is performed by the receiver side in the analog domain. The details of the receiver side will be explained in the following section.

6.3 ADC-Based RX AFE

6.3.1 Overview

The block diagram of the ADC-based RX AFE consisting of a CTLE and 8×TI SAR ADC with 2-tap embedded analog FFE is shown in Figure 6.3. To avoid the complexity, hardware cost,

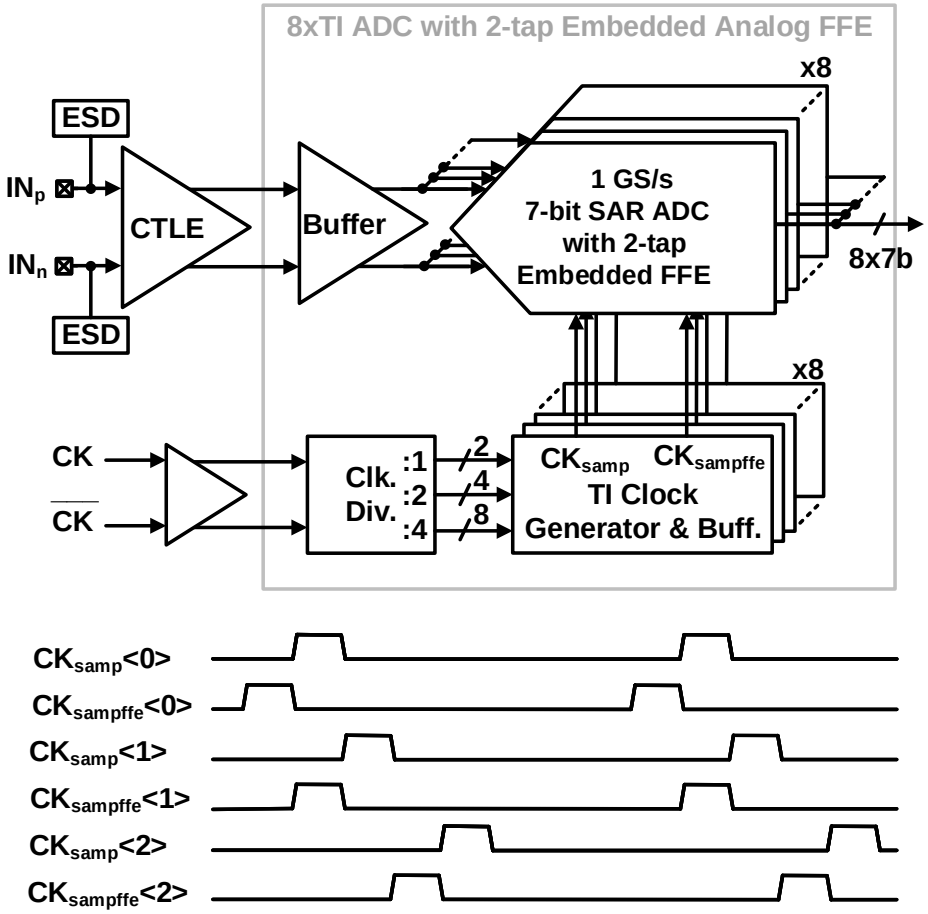


Figure 6.3: Block diagram and the timing scheme of the ADC-based RX AFE.

and high power consumption of the digital equalization with PAM-16, all the equalization is performed in the analog domain in the RX side. The data input is partially equalized by the CTLE first, then the remaining ISI is equalized by the 8×TI SAR ADC with 2-tap embedded analog FFE after the sampling and finally, the quantization is performed by the ADC.

This chapter examines the feasibility and power efficiency of high order modulation. Based on the simulation results of Section 6.1, the horizontal opening of the eye diagram is very high and this results in a relaxed timing specification. Therefore, the performance of the clock data recovery circuit is not critical and this circuit is not included in this work.

6.3.2 CTLE

The schematics of the CTLE with the ADC input buffer is shown in Figure 6.4. The degeneration resistor and the capacitor of the CTLE each consist of independently programmable 4-bit DACs to optimize the equalization parameters. Figure 6.5 shows the frequency response of the

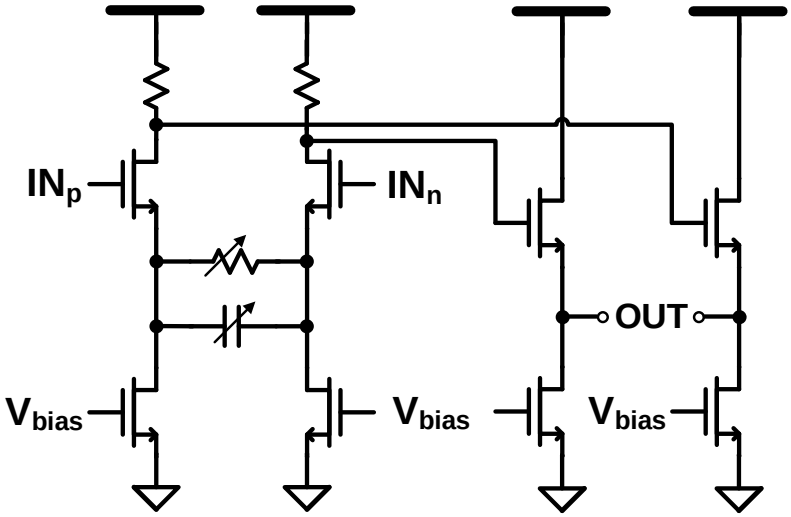
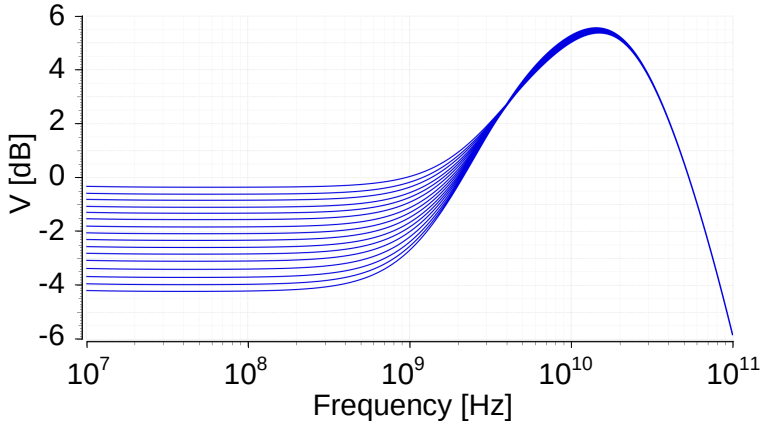


Figure 6.4: Schematic of the CTLE and the ADC input buffer.

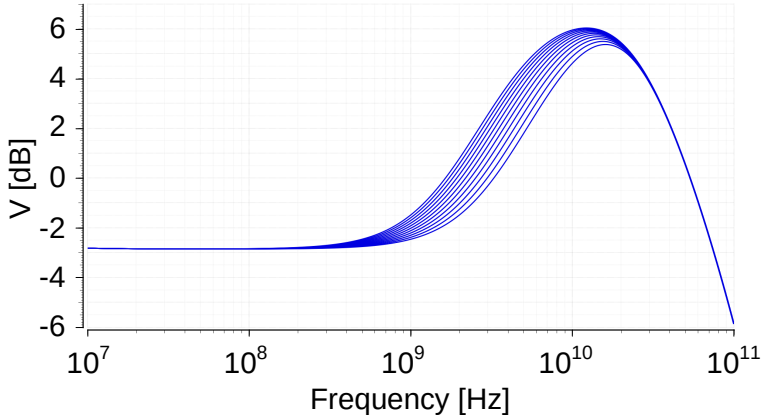
CTLE is for different trim settings. Trimming the resistor changes the DC gain and the amount of effective peaking, whereas changing the capacitive trim changes the frequency at which the gain boosting starts. The variable gain of the CTLE is adjusted so that the full-scale input swing is applied to the ADC.

A high modulation order such as PAM-16 is more sensitive to the residual ISI compared to lower modulation orders. In this RX AFE system, the CTLE and the 2-tap analog FFE function embedded in the ADC should equalize all the channel loss. Since the optimum CTLE parameters depend on the equalization capability of the 2-tap FFE as well, the 2-tap behavioral analog FFE model is used in the simulations to decide the trim settings of the CTLE.

Figure 6.6 shows the pulse responses at the output of the channel, the output of the CTLE, and the output of the behavioral 2-tap FFE model after the equalization parameters are adjusted for the target channel given in Figure 6.1. CTLE parameters are adjusted to equalize almost all the loss at the Nyquist frequency. The load of the CTLE is the input buffer of the ADC. Since the ADC consist of 8-channels, the input buffer is not large. Therefore, the bandwidth of the CTLE is high enough and inductive peaking is not needed. The best eye-opening at the output of the 2-tap FFE block has been observed when the CTLE has a peak frequency of $\sim 3\times$Nyquist frequency. The following two factors are considered to decide the peaking of the CTLE. First, the pulse response at the Nyquist frequency should be able to reach the high-logic level. Second, the second post-cursor should be equalized properly. 2-tap FFE applied after the CTLE can correct the first post-cursor. Therefore, undershoot in the first post-cursor at the output of the CTLE can be corrected by the 2-tap FFE but the undershoot at the second post-cursor cannot be corrected.



(a) Resistance trim.



(b) Capacitance trim.

Figure 6.5: Trim settings of the CTLE.

The linearity of the CTLE is an important parameter, especially in a transceiver system with high order modulation. To minimize the non-linearity of the CTLE, the input common-mode is chosen as 1 V. For the CTLE to be able to operate with 1 V input common-mode, the data sent by the TX is AC coupled to the RX input and the input common-mode voltage is set through the 50 Ω input termination resistors at the CTLE input. Also due to the linearity considerations, the supply voltage of the CTLE is increased to 1.25 from the nominal supply voltage of 1 V to keep the current sources at the saturation region. The ADC input buffer should provide 500 mV common-mode to the ADC. The output common-mode voltage of the CTLE is set to 1 V to have 500 mV common-mode at the output of the buffer.

6.4 Time-Interleaved ADC

The 8 GS/s 8×TI ADC consists of an input buffer, a clock divider, 8 identical TI clock generation circuits with output buffers, and 8 SAR ADC channels as shown in Figure 6.3. The output of the

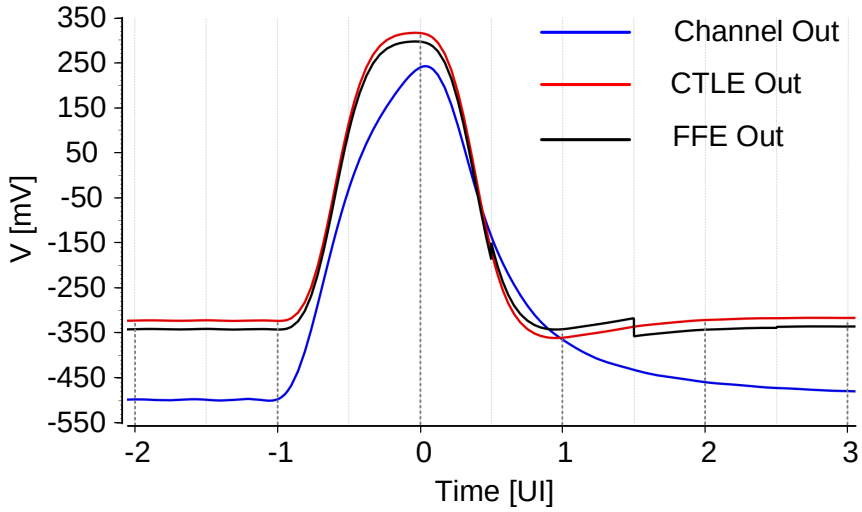


Figure 6.6: Pulse response at the output of the channel, CTLE, and FFE block.

source-follower input buffer is connected to the sampling switches inside the 8-parallel 7-bit 1 GS/s SAR ADCs. Each TI clock generator provides two sampling pulses, namely CK_{samp} and $CK_{sampffe}$, to a SAR ADC channel. The 7-bit 1 GS/s SAR ADCs have a 2-tap analog FFE function integrated into them; hence, each ADC channel requires two consecutive sampling pulses for sampling the current input voltage for the main-cursor and for acquiring the previous sample to cancel out the post-cursor. TI clock generator block uses differential 4 GHz clocks (CK_2), 4-phase 2 GHz clocks (CK_4), and 8-phase 1 GHz clocks (CK_8) provided by the clock divider. The generation of the CK_{samp} and $CK_{sampffe}$ is based on pass-gate selection clocking as shown in Figure 6.7 [60]. The pass-gate, controlled by the enable signal generated from CK_4 and CK_8, passes only one of the four CK_2 pulses. Since there is enough time margin between the enable signal and the rising/falling edges of the CK_2, the timing requirements of the CK_4 and CK_8 signals are relaxed. However, the timing of the 4 GHz clocks (CK_2) is critical. The layouts of the differential 4 GHz clocks (CK_2) and the differential ADC inputs driven by the input buffer should be symmetrical for the matching between ADC channels. Moreover, the timing skew of each sampling signal can be fine-tuned by tunable capacitance at the output of the pass-gate. This tunable capacitance is provided by a set of binary-weighted NMOS transistors connected to grounded capacitors [14].

6.4.1 7-bit SAR ADC with 2-Tap Embedded FFE

Block diagram of the single-channel 7-bit 1 GS/s SAR ADC with 2-tap embedded FFE is shown in Figure 6.8. This SAR ADC architecture uses multiple comparators for enhanced speed [14, 30]. Thanks to using one comparator per decision, the reset time of the comparator is removed from the critical path and the multiplexing of the comparator decisions is avoided. Comparator decisions stored in a memory directly controls the corresponding bottom plate switch of the

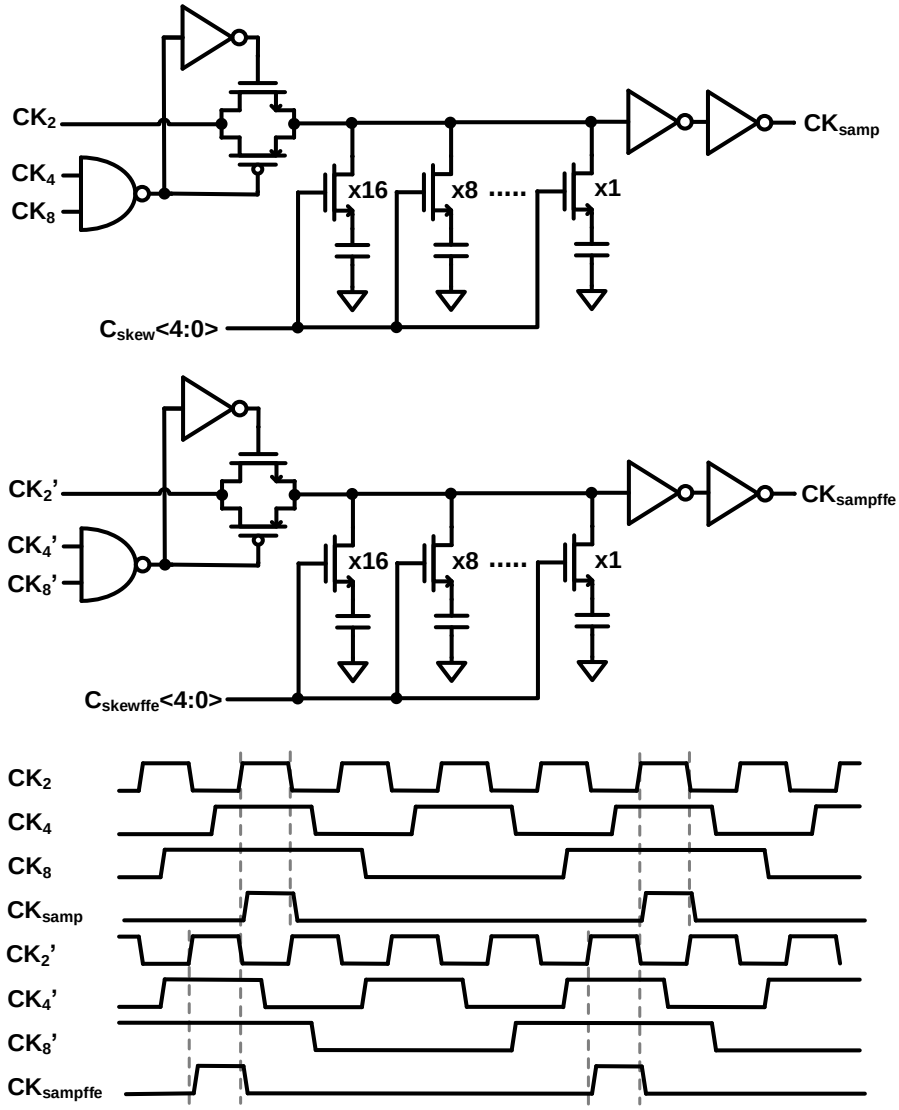


Figure 6.7: Schematic of the sampling clock generator block.

capacitive DAC, $CDAC_{SAR}$ without additional logic. Moreover, using one comparator per decision helps with electromigration issues because each comparator is triggered once in each SAR conversion, instead of triggering the same comparator over and over again in the same conversion cycle.

There are two differential capacitive DACs, named as $CDAC_{SAR}$ and $CDAC_{FFE}$ in this ADC architecture. $CDAC_{SAR}$ performs the SAR conversion and $CDAC_{FFE}$ is dedicated for the implementation of the FFE function. The input voltage corresponding to the previous sample is sampled into the $CDAC_{FFE}$, shown in Figure 6.10, by $CK_{sampffe}$. The input voltage corre-

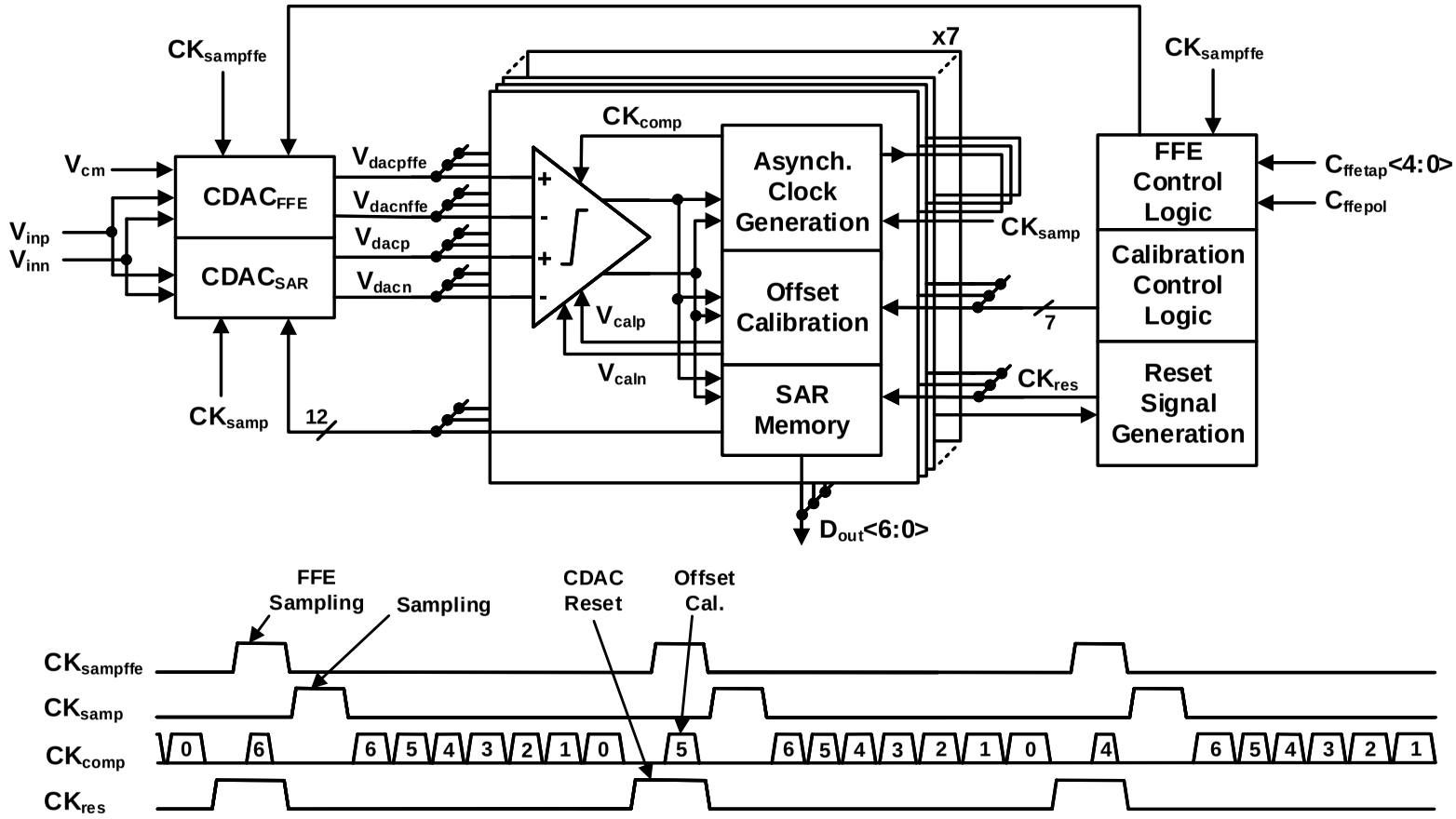


Figure 6.8: Block diagram and the timing scheme of the single-channel 7-bit SAR ADC with 2-tap embedded FFE.

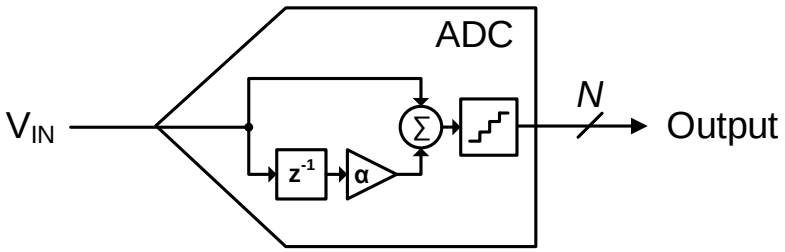


Figure 6.9: Block diagram of the 2-tap embedded FFE.

sponding to the main-cursor is sampled into the $CDAC_{SAR}$, shown in Figure 6.11, via the bootstrapped switches clocked by CK_{samp}. The embedded FFE implementation is based on subtracting/adding the previous sample scaled by the FFE tap coefficients from/to the current sample before the quantization as shown in Figure 6.9. Since the FFE operation is implemented in the analog domain before the quantization, the quantization noise is reduced compared to the digital FFE option. The proposed SAR ADC design uses an idea similar to [61] for the implementation of the embedded analog FFE. However, the proposed FFE implementation is adapted for the direct interleaving technique and the SAR ADC architecture with multiple comparators without compromising from the conversion rate.

Each bit of the 5-bit tap coefficient, C_{ffetap}<4:0> is used in the generation of the enable signal that controls the bottom plate switches of a capacitor in the 5-bit capacitive DAC in $CDAC_{FFE}$ shown in Figure 6.10. The voltage sampled by $CK_{sampffe}$ is scaled according to the 5-bit FFE tap coefficient. In the FFE sampling phase, if the corresponding digit of the tap coefficient is logic-1, then the bottom-plate switch connected to the ADC input is turned on for that capacitor, sampling the input signal into the capacitor; otherwise, the bottom-plate switch connected to the common-mode voltage turns on, sampling zero voltage in between the capacitor terminals. In this way, the number of unit capacitors in which the input voltage is sampled is adjusted. In the meantime, V_{ffep} and V_{ffen} are pre-charged to the common-mode voltage. Then, either switches controlled by C_{ffetrd} or C_{ffetrx} turned on, depending on the polarity of the FFE tap coefficients defined by C_{ffepol}, and all the bottom-plates are shorted to the common-mode voltage; therefore, the sampled input voltage is inverted to the top plate, scaled by charge sharing and transferred into the capacitances at the V_{ffep} and V_{ffen} nodes. The scaling range of the previous sample is between 0 and ±0.16, divided into 5-bit steps. Although, it is not necessary to use bootstrapped switches to connect the top-plates to the common-mode voltage in the $CDAC_{FFE}$, bootstrapped switches identical to the ones used in the $CDAC_{SAR}$ are employed to match the timing skew of CK_{samp} and $CK_{sampffe}$ by matching the loads of these signals. The power consumption of the $CDAC_{FFE}$ and the FFE control logic is dependent on the value of the FFE tap coefficient. As the value of the tap coefficient increases, the power consumption of these blocks increases as well.

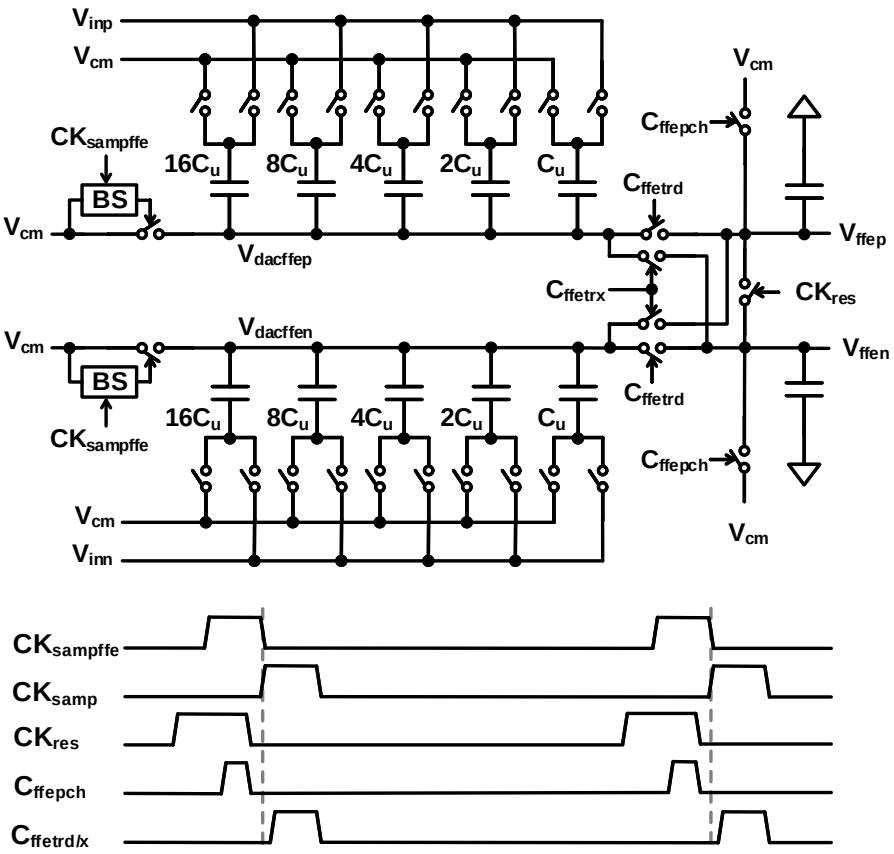


Figure 6.10: Schematic of the $CDAC_{FFE}$ and the timing of the control signals.

$CDAC_{SAR}$ shown in Figure 6.11 is a 6-bit binary-weighted capacitive DAC and uses splitting monotonic switching [26]. The switching is fully differential except for the last switching. Therefore, the common-mode is kept constant during the SAR switching except for the last one. Thanks to using single-sided switching instead of fully differential switching for the last capacitor, the number of unit capacitors in the $CDAC_{SAR}$ is halved, yielding a smaller and more compact capacitive DAC. Since single-sided switching of the last capacitor causes a very small change in the common-mode, its effect in comparator precision is tolerable.

After the input is sampled into the $CDAC_{SAR}$ by CK_{samp}, the first comparison starts immediately, as shown in the timing scheme in Figure 6.8, thanks to using top plate sampling. Clock signals triggering the comparators are generated asynchronously. Asynchronous clocking of the comparators alleviates the metastability issues in addition to enhancing the conversion rate. After a comparison is completed, the comparator clock is pulled down immediately and the next comparator clock is pulled up. The comparator clocks are disabled right after the completion of the decision, as in [14], instead of staying enabled until the end of the conversion cycle, as in [30]. The common-mode voltage of the capacitive DACs decreases due to the

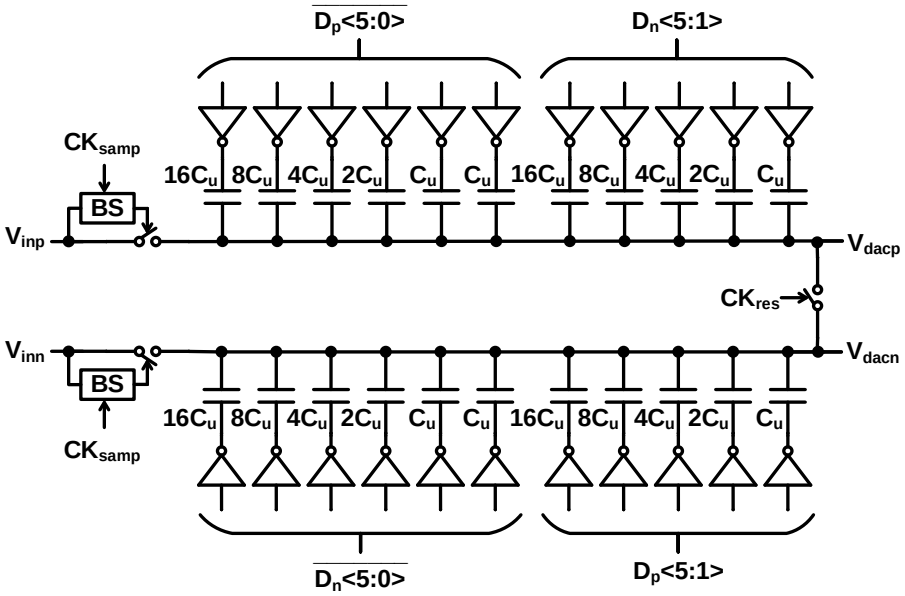


Figure 6.11: Schematic of the $CDAC_{SAR}$.

comparator kickback on the capacitive DACs when the comparator is enabled. Disabling the comparator takes back the charge kickback and provides constant common-mode for the following comparisons. The disabling of the comparators after the completion of the decision is preferred in this design because constant common-mode is required for the precision of the comparator with double differential inputs shown in Figure 6.12. Moreover, also to achieve better comparator precision, the capacitances at the comparator inputs are matched to have the same amount of common-mode drop due to comparator kickback.

After the completion of the last comparison, the bottom plates of the $CDAC_{SAR}$ are reset and the differential comparator inputs are shorted by CK_{res} signal. Then, the background calibration starts. One of the seven comparators is calibrated alternately at the end of each SAR conversion. Schematic of the StrongArm based dynamic comparator with two identical differential inputs and a smaller additional differential input for offset calibration is given in Figure 6.12. This design is very sensitive to the input common-mode mismatch between the two differential inputs. Therefore, CDACs are carefully designed to provide matched common-mode voltage. The offset of each comparator is calibrated to zero by a differential calibration voltage generated by the low-power switched capacitor background offset calibration circuit [39].

Since the vertical opening is very small in PAM-16, the precision of the ADC is important. The unit capacitor size in the capacitive DACs should be large enough to provide sufficient matching for good DNL and INL. Moreover, the thermal noise of the comparator should be

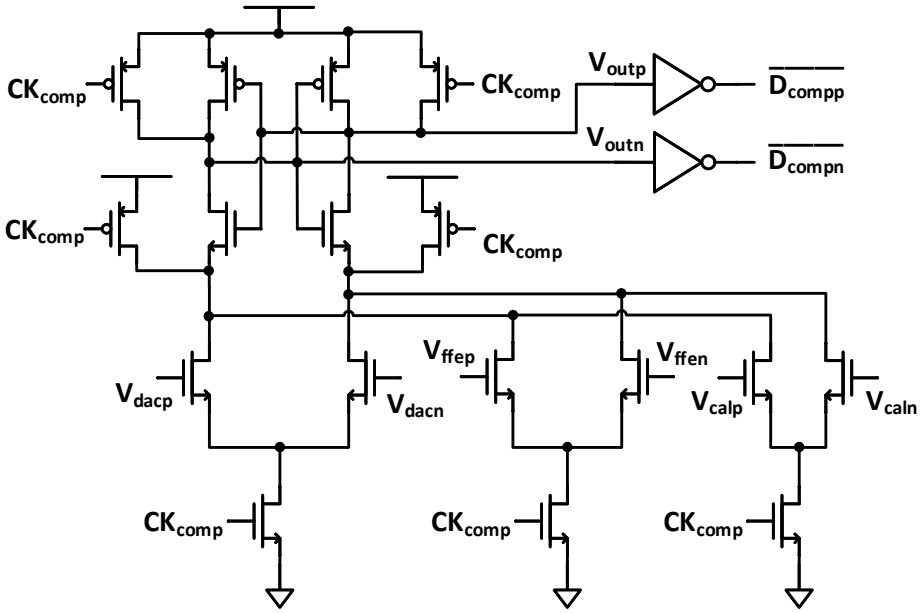


Figure 6.12: Schematic of the dynamic comparator.

smaller than half LSB. The offset of each ADC channel is background calibrated to zero. Since all the ADC channels are driven by the same input buffer, additional offset calibration for the offset mismatch between the channels is not required. The effect of bandwidth mismatch between the ADC channels is negligible considering the bandwidth is larger than the 4 GHz Nyquist frequency. Regarding the horizontal eye opening values in Figure 6.2 for PAM-16, the precision of the sampling time is relaxed compared to the lower order modulations such as PAM-2 and PAM-4. Therefore, the jitter, timing skew matching, and clock data recovery circuit requirements are relatively relaxed as well. Another important point is the gain matching of the TI channels. The reference buffer and R-3R ladder gain control circuit in [60] can be used for adjusting the capacitive DAC reference voltages individually for each TI channel and calibrating the gain.

6.5 Simulation Results

Figure 6.13 shows the layouts of the TX and the ADC-based RX AFE including the 8×TI SAR ADC with 2-tap embedded analog FFE. This section presents the results of post-layout simulations. To include the effect of the thermal noise into the presented simulation results, first, the noise of each block has been simulated at 80 °C. The input-referred noise of the CTLE is 303 μV_{RMS}. The noise of the CTLE and the following ADC input buffer together referred to the CTLE input is 338 μV_{RMS}. The input-referred noise of the ADC is 1.46 mV_{RMS}. The total noise of all these blocks combined results in 749 μV_{RMS} referred to the input of the CTLE. If we assume that the system also has supply noise approximately equal to the thermal noise, 1 mV white

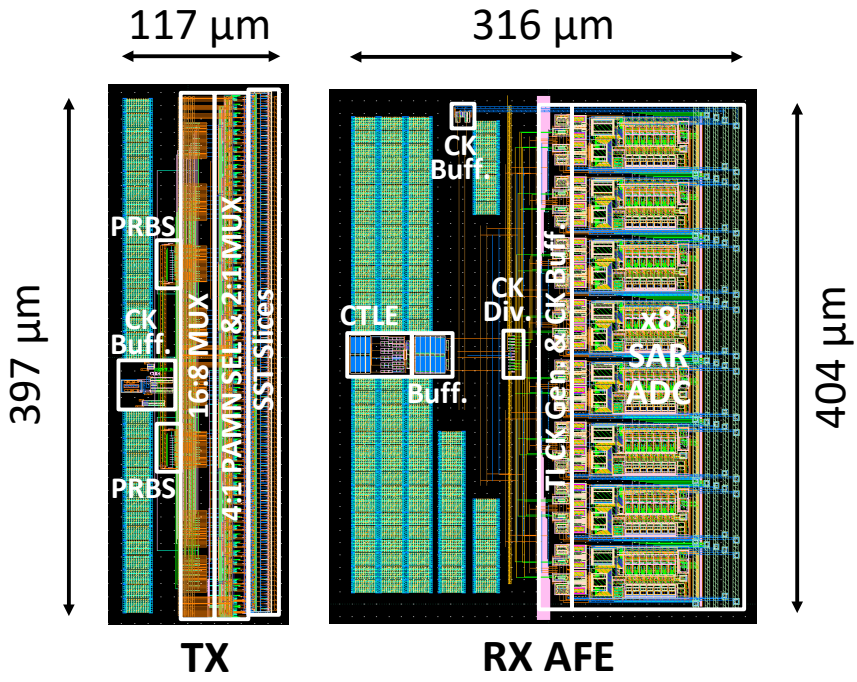
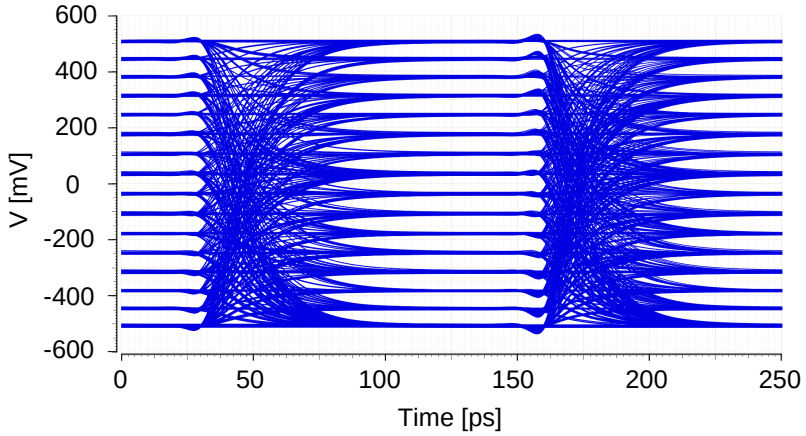


Figure 6.13: Layout of TX and ADC-based RX AFE.

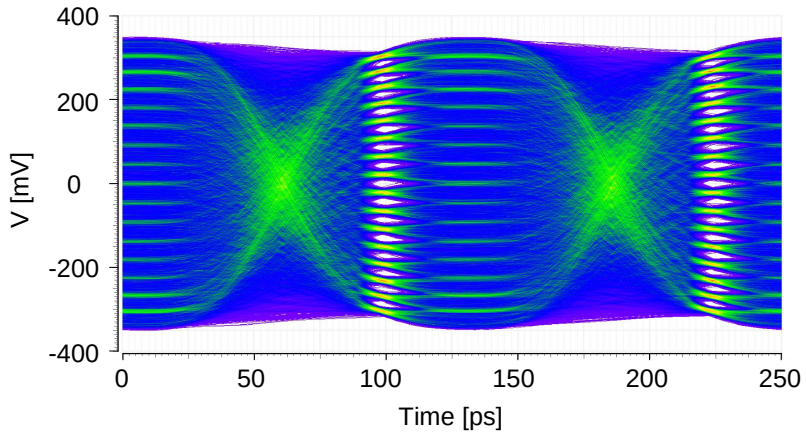
noise has been injected at the CTLE input for the simulations presented in this section. Also, capacitances whose value is equal to the sum of capacitances coming from the I/O pads and ESD diodes added to the TX output and the RX input are added to the simulation setup. The channel whose characteristic is shown in Figure 6.1 is used in the simulations.

Figure 6.14 shows the eye-diagrams at the output of the TX, at the output of the ADC input buffer following the CTLE, and after 2-tap analog FFE algorithm applied the signal at the buffer output. The TX block in this system does not provide any equalization. The eye diagram at the RX input is not given since it is closed due to ISI. The eye-diagram at the output of the CTLE has a significant overshoot/undershoot due to intentional high peaking. This overshoot/undershoot in the first cursor will be corrected later by the analog FFE embedded in the SAR ADC. Since the FFE embedded in the ADC applied after the signal is sampled by the ADC, the continuous FFE eye-diagram cannot be observed. Therefore, a behavioral 2-tap analog FFE block is used only in this simulation to obtain the eye diagram at the FFE output. The timing bathtub curve of the mid-eye in the FFE eye diagram is plotted in Figure 6.15. The timing histogram of the FFE eye-diagram is given in Figure 6.16. The horizontal eye-opening values for each eye in the FFE eye-diagram are plotted in Figure 6.17.

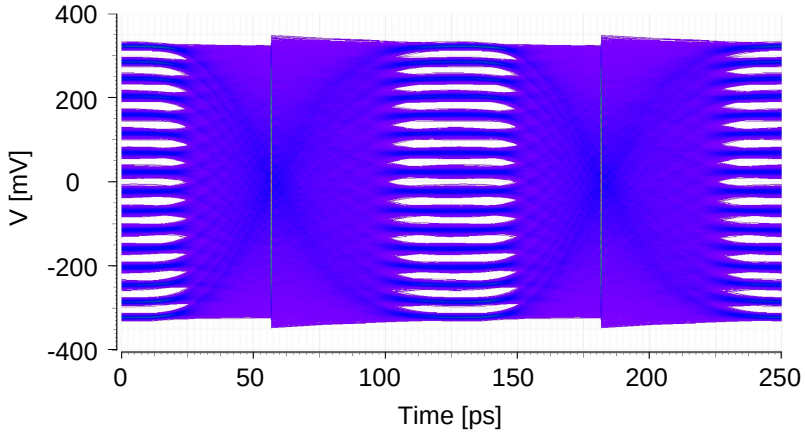
The power spectral density of the TI ADC is provided in Figure 6.18. The post-layout simulation of the TI ADC shows that it achieves 43.37 dB SNDR at 8 GS/s with near Nyquist rate input. The histograms are shown in Figure 6.19 are derived from the post-layout simulations of the whole transceiver system including TX, CTLE, ADC input buffer, and the 8×TI SAR ADC with 2-tap



(a) Eye-diagram at the output of the TX.



(b) Eye-diagram at the output of the ADC input buffer following the CTLE.



(c) Eye-diagram after 2-tap analog FFE function applied to the signal at the output of the ADC input buffer.

Figure 6.14: Simulated eye-diagrams.

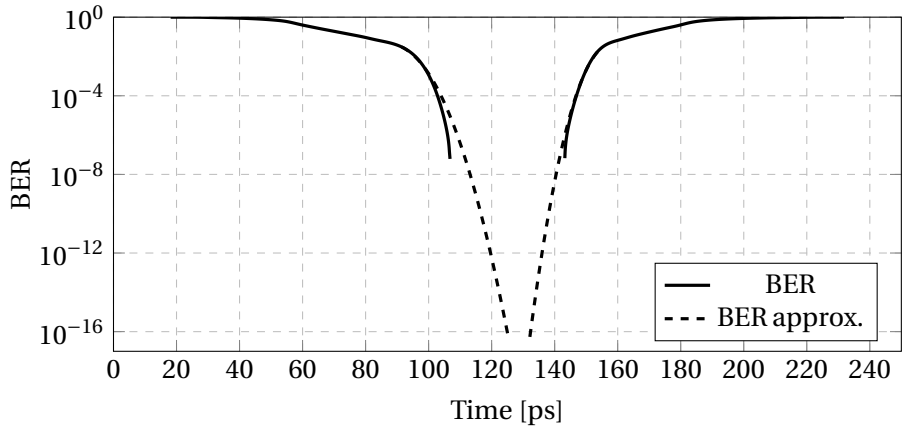


Figure 6.15: Timing bathtub curve of the eye-diagram at the output of the FFE block.

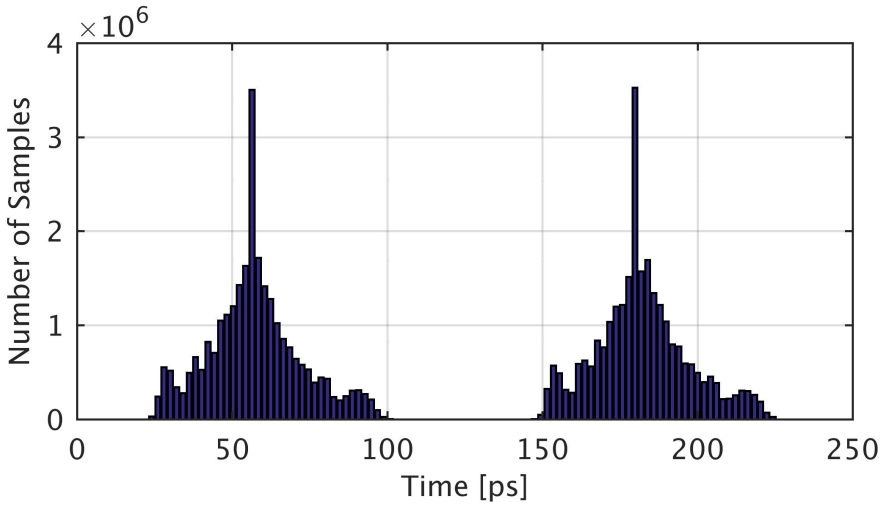


Figure 6.16: Horizontal histogram of the eye-diagram at the output of the FFE block.

embedded FFE. For PAM-16 at 32 Gb/s, the worst eye openings of 2-codes are observed at the top and bottom eyes. For PAM-8 at 24 Gb/s, the worst eye openings of 11-codes are observed at the top and bottom eyes as well. The histograms shown in Figure 6.19 are extrapolated and the number of samples is plotted in logarithmic-scale as shown in Figure 6.20 for the bit error rate (BER) estimation. The crossing point of the extrapolated lines for PAM-16 is below 10^{-6}, while it is well below 10^{-12} for PAM-8. The bit error rate can be derived from the sum of the areas which are extending beyond the crossing points for each PAM level. For PAM-16 at 32 Gb/s, the BER is obtained as $<10^{-5}$ while for PAM-8 at 24 Gb/s, BER$<10^{-12}$.

The total power consumption of the ADC-based RX AFE is 49.36 mW for PAM-16 at 32 Gb/s, including the CTLE and the TI ADC. The corresponding power breakdown is given in Figure 6.21. The total power consumption of the TX is 26.85 mW. Therefore, the whole system consisting of the TX and ADC-based RX AFE consumes 76.21 mW for PAM-16 at 32 Gb/s, which corresponds

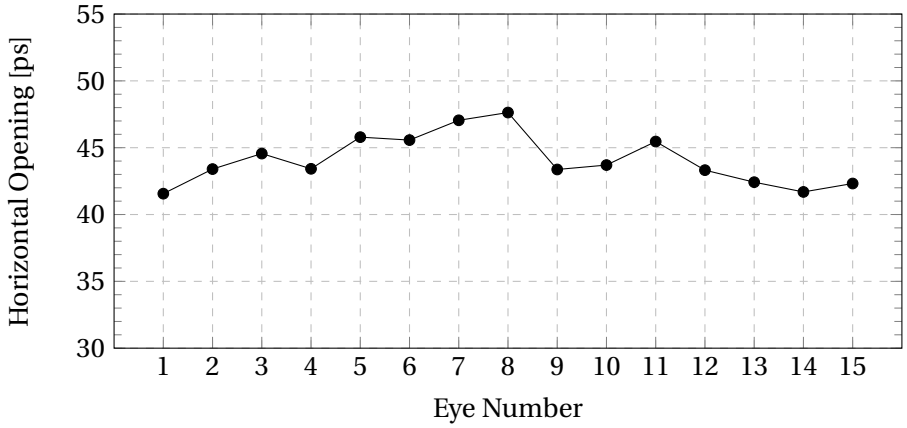


Figure 6.17: Horizontal eye-openings of each PAM-16 eye at the output of the FFE block.

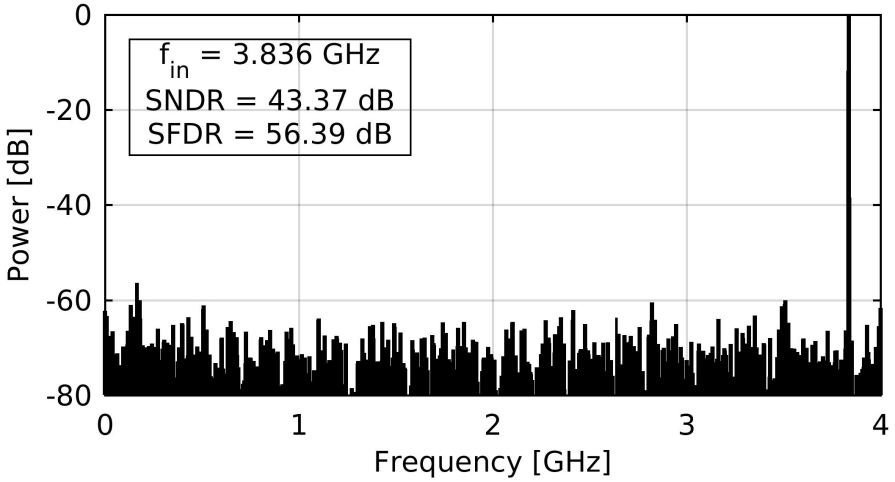
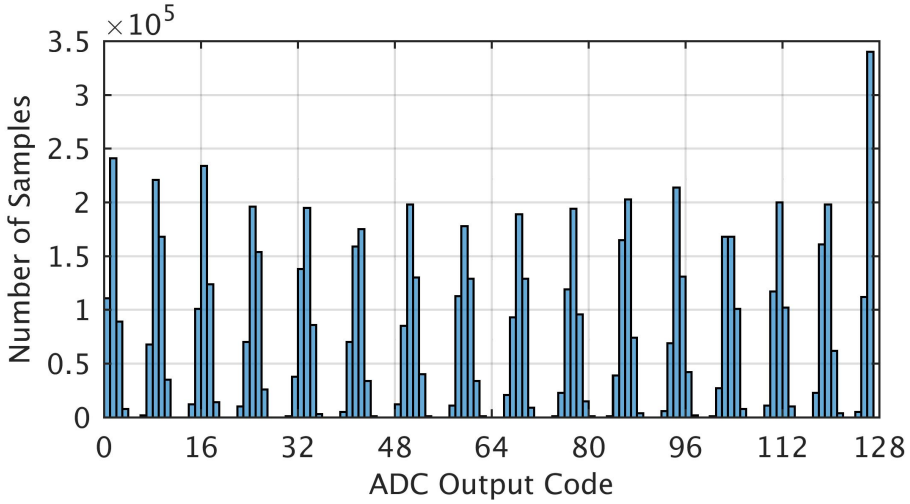


Figure 6.18: Power spectral density of the TI ADC.

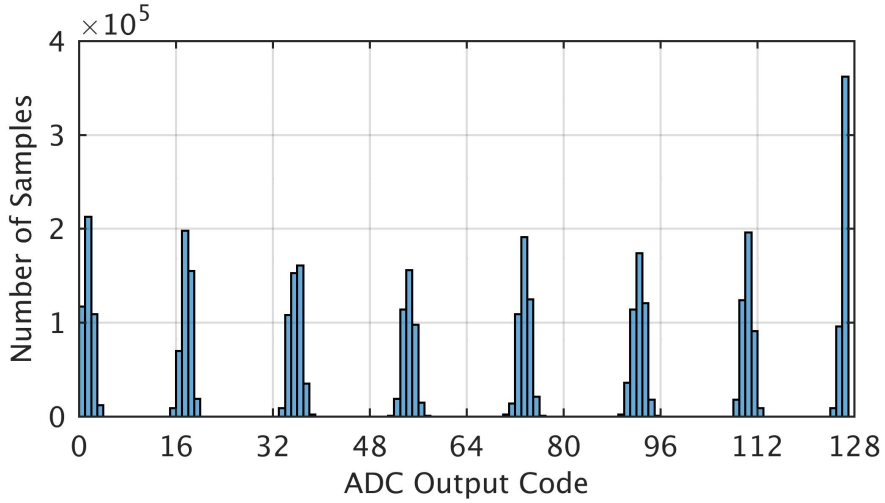
to 2.28 pJ/bit energy-efficiency.

6.6 Conclusion

This chapter presents an ADC-based receiver analog front-end design compatible with various PAM orders thanks to employing only analog equalization. The receiver front end performs the equalization using CTLE and 2-tap analog FFE embedded in the 8×TI SAR ADC. The behavioral level simulations of the system show that using PAM-8 and PAM-16 better horizontal eye-opening can be obtained. Since by using higher order PAM, the Nyquist frequency and the corresponding channel loss is lowered, the required equalization capability and the power consumed for the equalization is lower. At 32 Gb/s, using only CTLE and 2-tap analog FFE embedded the ADC and PAM-16, 6.01 dB channel-loss can be compensated. If PAM-4 was used for the same target data rate and the same moderate loss channel, the channel loss

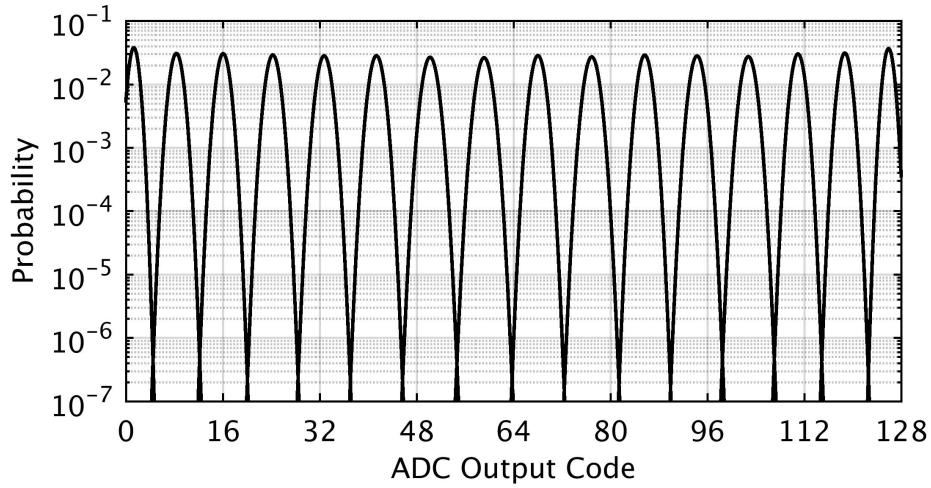


(a) PAM-8 at 24 Gb/s.

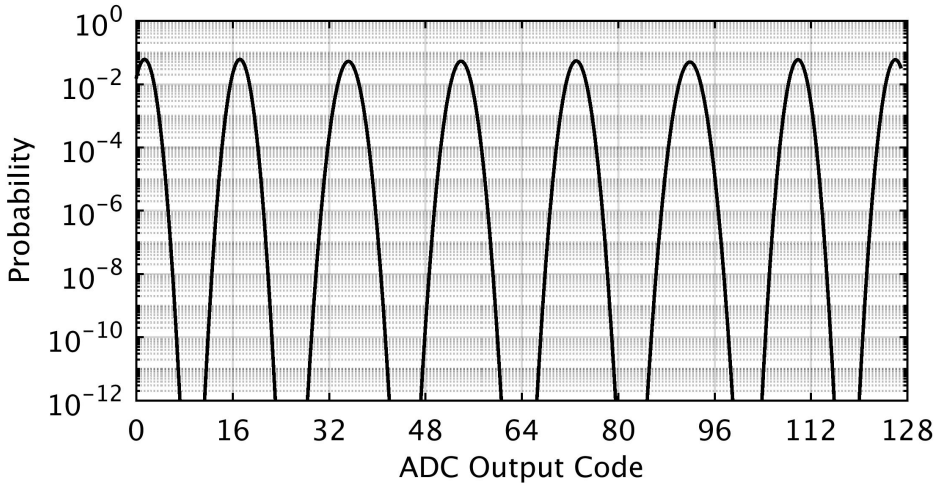


(b) PAM-8 at 24 Gb/s.

Figure 6.19: Histogram of the ADC output codes.



(a) PAM-16 at 32 Gb/s.



(b) PAM-8 at 24 Gb/s.

Figure 6.20: Extrapolated probability distribution of the ADC output codes.

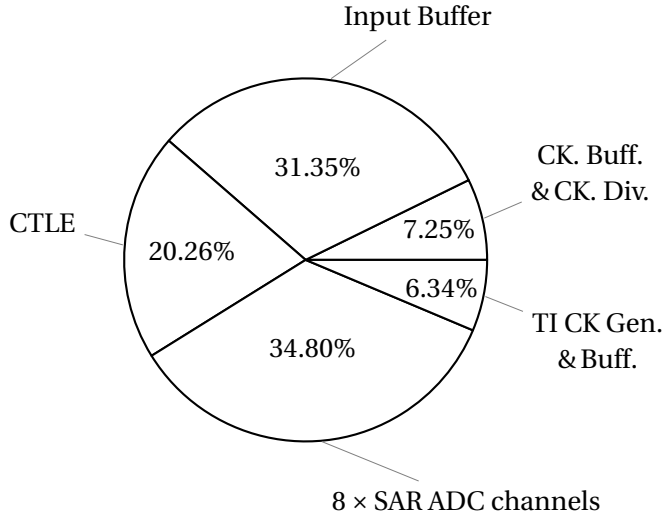


Figure 6.21: Power breakdown of the ADC-based RX AFE.

that needs to be compensated for would be 11.31 dB. Post-layout simulations of the system consisting of an SST transmitter and the presented ADC-based receiver analog front-end show that the estimated BER<10^{-5} for PAM-16 at 32 Gb/s and <10^{-12} for PAM-8 at 24 Gb/s without any additional digital equalization following the presented analog front-end. The comparison of the presented ADC-based receiver analog front-end design with the other ADC-based receiver publications is summarized in Table 6.1. The power consumed by the CTLE and the TI-ADC is 49.36 mW for 8 Gbaud. For PAM-16 at 32 Gb/s, the corresponding energy efficiency is 1.54 pJ/bit while it is 2.06 pJ/bit for PAM-8 at 24 Gb/s.

Table 6.1: Performance comparison of the ADC-based RX AFE.

	[11]	[62]	[61]	[8]	**This work**
Technology	28 nm	65 nm	65 nm	16 nm FinFET	**28 nm FDSOI**
Power Supply	-	1 & 1.2 V	1 & 1.2 V	0.9, 1.2 & 1.8 V	**1 & 1.25 V**
Max. Data Rate	32 Gb/s	25.6 Gb/s	52 Gb/s	56 Gb/s	**32 Gb/s**
Modulation	PAM-4	PAM-4	PAM-4	PAM-4	**PAM-16**
TX Eq.	-	4-tap	-	3-tap	**-**
RX Equalization	CTLE	Emb. IIR Filter	CTLE 3-tap emb. FFE & DSP	CTLE DSP	**CTLE 2-tap emb. FFE**
Channel Loss	31 dB @8 GHz	9.6 dB @6.4 GHz	31 dB @13 GHz	31 dB @14 GHz	**6 dB @4 GHz**
Power ADC+AFE: DSP:	320 mW	62 mW	236 mW 183 mW	370 mW	**49 mW**
Energy Eff. AFE+ADC:	10 pJ/bit	2.43 pJ/bit	4.54 pJ/bit	6.61 pJ/bit	**1.54 pJ/bit**

7 Conclusion

This thesis investigated the high-speed design techniques for the optimization of ADCs for wireline applications. The work aimed to design high-speed energy-efficient ADCs suitable for wireline applications. This is mainly motivated by the key role of high-speed ADCs in ADC-based receivers to enable the implementation of complex digital equalization algorithms. ADCs used in ADC-based receivers should be compatible with technology scaling because the ADC and DSP are realized on the same chip. SAR ADCs offer suitability to advanced technology nodes because they consist of mostly digital blocks. As a result, this thesis focused on high-speed and energy-efficient design techniques in SAR ADCs. After reviewing the high-speed design techniques, numerous SAR ADC designs were proposed. Since the multi-GS/s ADCs are required for wireline links and such speed cannot be met using only a single-channel SAR ADC, time-interleaving has become a common design approach. Although the main design objective for all the proposed designs was improving the speed, power consumption, and consequently the figure-of-merit, occupying a smaller area is also aimed for single-channel ADC designs for the suitability to time-interleaving.

The first design presented in Chapter 3 aims is to explore the limits of speed and figure-of-merit for a relatively simple SAR ADC architecture that uses a single comparator. Many different design techniques are combined to minimize the SAR loop delay, capacitive DAC settling time, and power consumption. The single-channel 9-bit asynchronous SAR ADC prototype, designed and fabricated in 65 nm CMOS, achieves 47.6 dB SNDR and 29.6 fJ/conversion-step figure-of-merit near Nyquist frequency at 222 MS/s, consuming 1.07 mA from a 1.2 V supply, and occupies an active area of 0.017 mm^2. The figure-of-merit of the prototype was better than or comparable with the other state-of-the-art high-speed single-channel SAR ADCs in 65 nm CMOS with SNDR>40 dB.

To further improve the resolution of the 9-bit asynchronous SAR ADC presented in Chapter 4, a delay-based quantization method which uses the comparator delay for the extraction of an additional 1-bit is examined. Even though SAR ADCs with delay-based LSB extraction exist in the literature, they require foreground calibration to adjust the reference delay. However, the reference delay is sensitive to variations over time. Also, the implementation of such a

circuit into a high-speed SAR ADC and the noise related aspects were not examined previously. The work explained in Chapter 4 fills that gap and proposes a low-power self-calibration circuit operating on the background to track the variations. The proposed self-calibrated delay-based LSB extraction circuit improves the SNDR of a 9-bit 200 MS/s SAR ADC by 3.35 dB with insignificant degradation in power consumption, speed, and area.

Since the sampling rate is limited using only one comparator, the next SAR ADC design, presented in Chapter 5, focused on loop-unrolled SAR architecture to remove the reset time of the comparator from the critical path to improve the sampling rate. The comparator kickback, common-mode voltage variation issue and its effect on the comparator offset are examined. To solve the offset mismatch problem due to common-mode voltage variation a novel common-mode adaptive background offset calibration scheme is proposed. Immunity against common-mode variation provides flexibility in terms of design choices; therefore, this flexibility is exploited to improve the figure-of-merit of the design. A prototype 8-bit loop-unrolled SAR ADC was designed and fabricated in 28 nm FDSOI CMOS. The prototype achieves 42.57 dB SNDR and 22.8 fJ/conv.-step at 800 MS/s with near Nyquist frequency and occupies an active area of only 0.0037 mm^2. The measured SNDR proves the effectiveness of the proposed calibration method.

Chapter 6 examined the use of high order PAM for improving energy efficiency in an ADC-based transceiver system. In the proposed ADC-based receiver analog front-end, all the equalization is implemented in the analog domain by the CTLE and the ADC for the compatibility with various modulation orders and to avoid the high complexity of digital equalization implementation for high order PAM. The proposed 8 GS/s 7-bit 8×TI SAR ADC design combines the embedded analog FFE implementation with the SAR ADC architecture with multiple comparators to minimize the SAR loop delay. The ADC-based RX that includes the CTLE and 8×TI SAR ADC with 2-tap embedded analog FFE consumes 49.36 mW at 8 Gbaud, which corresponds to 1.54 pJ/bit for PAM-16 at 32 Gb/s and 2.06 pJ/bit for PAM-8 at 24 Gb/s. Even though the design objective was mainly the compatibility with high order PAM, the embedded analog FFE implementation provides advantages for lower order modulation as well by relaxing the requirements on the ADC resolution and the equalization capability of the DSP.

7.1 Future Work

The asynchronous SAR ADC design presented in Chapter 3 can be improved by using a larger unit capacitor size in the custom-designed capacitive DAC because measured SNDR is limited by the capacitor mismatch. Using a slightly larger unit capacitor size does require only a small change in the capacitive DAC layout. The capacitive DAC settling would take more time and consequently, the sampling rate would decrease slightly. Also, the power consumption of the capacitive DAC bottom plate drivers would increase slightly as well. However, the figure-of-merit is expected to improve because the increase in the measured SNDR is expected to be more dominant compared to the degradation in the other parameters mentioned.

The noise analysis of the self-calibrated delay-based LSB extraction circuit proposed in Chapter 4 is presented with post-layout simulations. This design can be taped-out and silicon measurements can be done. The proposed LSB extraction circuit can also be implemented to the faster SAR ADC designs using multiple comparators presented in Chapter 5 and Chapter 6 easily. Potential resolution improvement that can be gained with such implementation can be investigated by conducting an analysis similar to the one in Chapter 4.

The time-interleaved SAR ADC design with 2-tap embedded FFE proposed in Chapter 6 can be improved by adding programmable voltage references for each ADC channel to calibrate the gain mismatch between the channels. The layout of the ADC-based receiver analog front-end is complete but it is not taped-out. Therefore, the silicon measurement of this design can be conducted to prove the performance of the high order pulse amplitude modulation.

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List of Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
BER	Bit Error Rate
CDAC	Capacitive Digital-to-Analog Converter
CDR	Clock and Data Recovery
CMOS	Complementary Metal-Oxide Semiconductor
CTLE	Continuous-Time Linear Equalizer
DAC	Digital-to-Analog Converter
DC	Direct Current
DNL	Differential Non-Linearity
DSP	Digital Signal Processor
ENOB	Effective Number of Bits
ESD	Electro-Static Discharge
f_{in}	Input Frequency
f_s	Sampling Frequency
FDSOI	Fully-Depleted Silicon-on-Insulator
FFE	Feed-Forward Equalizer
FFT	Fast Fourier Transform
FoM	Figure-of-Merit
FS	Full-Scale
INL	Integral Non-Linearity
I/O	Input/Output
IP	Internet Protocol
ISI	Inter-Symbol Interference
LSB	Least Significant Bit
LU	Loop-Unrolled
LU-SAR	Loop-Unrolled Successive-Approximation Register
MSB	Most Significant Bit
MUX	Multiplexer

N	Resolution
NMOS	N-Type Metal-Oxide Semiconductor
NRZ	Non-Return-to-Zero
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PMOS	P-Type Metal-Oxide Semiconductor
PVT	Process, Voltage, and Temperature
RX	Receiver
SAR	Successive-Approximation Register
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SR	Set-Reset
SST	Source-Series Terminated
TI	Time-Interleaved
TX	Transmitter
V_{DD}	Supply Voltage
V_{IN}	Input Voltage
VGA	Variable Gain Amplifier
XOR	Exclusive OR

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List of Publications

- A. Akkaya, F. Celik, and Y. Leblebici, "A Low-Power 9-Bit 222 MS/s Asynchronous SAR ADC in 65 nm CMOS," *2020 IEEE International Symposium on Circuits and Systems (ISCAS),* Sevilla, 2020, pp. 1-5.

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- F. Celik, A. Akkaya, A. Tajalli, and Y. Leblebici, "A 32 Gb/s PAM-4 SST Transmitter with 4-Tap FFE Using High-Impedance Driver in 28 nm FDSOI," (2021, under review, journal paper).