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Enhancement Mode Tri-gate GaN Power Devices and Logic Circuits

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par

Minghua ZHU

Acceptée sur proposition du jury

Prof. D. Dujic, président du jury
Prof. E. D. N. Matioli, directeur de thèse
Dr T. Detzel, rapporteur
Prof. B. Bakeroot, rapporteur
Prof. A. Rufer , rapporteur

École polytechnique fédérale de Lausanne

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Lausanne, 16 December 2020 Minghua ZHU

Abstract

Gallium Nitride (GaN) is one of the most promising materials for high frequency power switching due to its exceptional properties such as large saturation velocity, high carrier mobility, and high breakdown field strength. The high switching frequency of GaN-based power converters can lead to a significant reduction of the size of passive components, such as capacitors and inductors, and thus, increasing the power density of the overall system .

Due to the polarization effect induced high density and high mobility 2DEG in AlGaN/GaN heterostructure, GaN HEMT is an intrinsic normally-on (D-mode) transistor. However, normally-off transistors are required in most power eletronics system for safe operation and easier driver design. Despite the presence of several commercial GaN HEMT based devices, current GaN device performance is far from the fundamental material capabilities, as relatively large on-resistance (R_{ON}), smaller threshold voltage (V_{TH}) and insufficient breakdown voltage (V_{BR}) .

Recently, tri-gate structures are attracting considerable attention due to their better gate control and enhanced V_{BR} compared to planar devices, without degrading the R_{ON}. In addition, tri-gates allow a controllable positive shift of V_{TH} by changing the fin width, due to the partial relaxation of the AlGaN barrier and the enhanced electrostatic control from the tri-gate sidewalls. This would offer the possibility to maintain high V_{TH} and low R_{ON} at the same time.

In this thesis, we propose a few technologies combined with tri-gate structure to overcome these challenges. Firstly, we demonstrate normally-off GaN metal-oxide-semiconductor field-effect transistors (MOSFETsbased on the combination of tri-gate with barrier recess in the gate region to yield a more positive V_{TH}, while maintaining a low R_{ON} and high current density (I_D). The tri-gate structure offer excellent channel control, enhancing the V_{TH} up to +1.4 V at 1μA/mm for the recessed tri-gate, along with a much reduced hysteresis in V_{TH}, and a significantly increased transconductance (g_m). Additional conduction channels at the sidewalls of the tri-gate trenches compensated the degradation in R_{ON} from the gate recess, resulting in a small R_{ON} of 7.32 ± 0.26 Ω·mm for gate to drain length L_{GD} of 15 μm, and an increase in the maximum output current (I_D^{max}).

Secondly, we propose a novel concept for normally-off GaN MOS-HEMTs based on the combination of tri-gate, p-GaN, and MOS structures to achieve low R_{ON} and high V_{TH}. The p-GaN is used to change the band structure and reduce the carrier density (N_s) combined with the tri-gate structure for a high V_{TH}. The gate control is mainly achieved from field-effect through the tri-gate sidewalls, and does not rely on injection of gate current. The MOS structure enables much

larger gate voltages (V_G) and the effective sidewall modulation results in excellent switching performance at high switching frequencies. In addition, this concept eliminates the need for thin barriers (typical in p-GaN devices), which combined to the conduction channels formed at the tri-gate sidewalls, resulted in a smaller R_{ON} compared with planar p-GaN structures.

Finally, we investigated NMOS GaN-based logic gates including NOT, NAND, and NOR by integration of E/D-mode GaN MOSHEMTs. The GaN NMOS inverter was achieved with logic swing voltage of 4.93 V at a supply voltage of 5 V, low-input noise margin of 2.13 V and high-input noise margin of 2.2 V at room temperature. However, these logic gates suffer from unstable transient voltage, low noise margin, and high logic leakage current. Additionally, the large size mismatch between the E-mode and D-mode transistors hinders their compact integration. Thus, high-performance logic gates with monolithic integration of tri-gate E/D-mode tri-gate MOSHEMTs were fabricated. The tri-gate structure in the logic gate offers unique advantages compared with conventional planar E/D-mode design with much compact size match and more stable V_{TH}.

The results in this thesis reveal the great potential of GaN transistors and GaN based logic gate for high switching frequency, which would pave the path for future GaN power IC.

Key words: HEMT, GaN transistors, power device, III-Nitride,tri-gate, trench conduction, breakdown voltage, on resistance

Résumé

Le nitrure de gallium (GaN) est l'un des matériaux les plus prometteurs pour la commutation de puissance à haute fréquence en raison de ses propriétés exceptionnelles telles que la grande vitesse de saturation, la haute mobilité et la tension de claquage élevée. La fréquence de commutation élevée des convertisseurs de puissance à base de GaN peut conduire à une réduction significative de la taille des composants passifs, tels que les condensateurs et les inductances, et donc à augmenter la densité de puissance de l'ensemble du système.

En raison de la haute densité du gaz électronique à deux dimensions (2DEG) induit par la polarisation, transistor AlGaN/GaN à electrons à haute mobilité (AlGaN/GaN HEMT) est normalement à l'état passant. Cependant, la plupart des systèmes électroniques de puissance necessitent des tarnsistors normalement bloqués pour la sécurité de fonctionnement. Malgré la présence de plusieurs appareils commerciaux basés sur GaN HEMT, les performances actuelles des appareils GaN sont loin des capacités des matériaux fondamentaux à cause de la résistance à l'état passant relativement élévée (R_{ON}), tension de seuil trop petite (V_{TH}) et la tension de claquage insuffisante (V_{BR}).

Récemment, les structures à trois grilles ont attiré l'attention considérable en raison de leur meilleur contrôle de grille et de l'amélioration de V_{BR} par rapport aux dispositifs planaires, sans dégrader le R_{ON}. De plus, les tri-grilles permettent un décalage positif contrôlable de V_{TH} en modifiant la largeur des tranchées, en raison de la relaxation partielle de la barrière AlGaN et du contrôle électrostatique amélioré des parois latérales des tri-grilles. Cela offrirait la possibilité de maintenir un V_{TH} élevé et un R_{ON} réduit en même temps.

Dans cette thèse, nous proposons plusieurs technologies basées sur la structure trois grilles pour surmonter ces défis. Premièrement, nous présentons des MOSFET GaN-on-Si normalement bloqués basés sur la combinaison de tri-grille avec une barrière légèrement enfoncée pour produire un grand V_{TH} positif, tout en maintenant un R_{ON} et une densité de courant élevée (I_{D}). La structure à trois grilles offre l'un excellent contrôle de canal, améliorant le V_{TH} jusqu'à +1.4 V à 1 μ A / mm , avec hystérésis de V_{TH} très réduite , et la transconductance significativement accrue (g_{m}). Des canaux de conduction supplémentaires sur les parois latérales compensent la dégradation de R_{ON} en plus du renfoncement de la grille, résultant en un petit R_{ON} de 7.32 ± 0.26 $\Omega \cdot$ mm pour la longueur de la grille au drain (L_{GD} de 15 μ m, et en une augmentation du courant de sortie maximum ($I_{\mathrm{D}}^{\mathrm{max}}$).

Deuxièmement, nous proposons un nouveau concept pour les MOS-HEMT AlGaN / GaN-on-Si normalement bloqué sur la combinaison de structures p-GaN, tri-grille et MOS pour atteindre un

V_{TH} élevé et un faible R_{ON}. Le p-GaN est utilisé pour concevoir la structure des bandes et réduire la densité de grilleuse (N_s) dans la structure à trois grilles pour un V_{TH} élevé. La commande de grille est principalement réalisée par l'effet de champ à travers les parois latérales à trois grilles et ne repose pas sur l'injection de courant de grille. La structure MOS permet des tensions de grille beaucoup plus importantes (V_G) et la modulation efficace de la paroi latérale se traduit par d'excellentes performances de commutation à des fréquences de commutation élevées. De plus, ce concept élimine le besoin de barrières minces (typiques des dispositifs p-GaN), qui, combinées aux canaux de conduction formés au niveau des parois latérales à trois grilles, ont abouti à un R_{ON} plus petit par rapport au structures planaired dopées p GaN.

Enfin, nous avons étudié les grilles logiques NMOS basées sur GaN, y compris NOT, NAND et NOR par intégration de MOSHEMT GaN en mode E / D. L'onduleur GaN NMOS a été réalisé avec une tension de basculement logique de 4.93 V à une tension de 5 V, une marge de bruit d'entrée faible de 2.13 V et une marge de bruit d'entrée élevée de 2.2 V à température ambiante. Cependant, ces grilles logiques souffrent d'une tension transitoire instable, d'une faible marge de bruit et d'un courant de fuite logique élevé. De plus, le décalage de grande taille entre les transistors en mode E et en mode D empêche leur intégration compacte. Ainsi, les grilles logiques à haute performance avec intégration monolithique de MOSHEMT à trois grilles à trois modes E / D ont été fabriquées. La structure à trois grilles de la grille logique offre des avantages uniques par rapport à la conception en mode E / D planaire conventionnelle avec une correspondance de taille beaucoup plus compacte et plus stable V_{TH}.

Les résultats de cette thèse révèlent le grand potentiel des transistors GaN et de la grille logique basée sur GaN pour une fréquence de commutation élevée, ce qui ouvrirait la voie à un futur circuit intégré de puissance GaN.

Mots clefs : HEMT, transistors GaN, dispositif de puissance, nitrure III, tri-gate, conduction de tranchée, tension de claquage, résistance

Symbols and Acronyms

Symbols

Symbol	Quantity	Measurement unit or value
ϵ	Relative dielectric constant	
ϵ_0	Vacuum dielectric constant	8.85×10^{-12} F/m
g_m	Transconductance	S
μ	Mobility	cm^2/Vs
N_s	Sheet carrier concentration	cm^{-2}
$DIBL$	Drain induced barrier lowering	mV/V
SS	Subthrehsold slope	mV/dec
V_BR	Breakdown voltage	V
V_on	Turn-on voltage	V
v_sat	Saturation velocity	cm/s
w_sd	Sidewall depletion width	nm
R_ON	On-resistance	$\Omega\cdot mm$
V_TH	Threshold voltage at 1μA/mm	V
V_G	Gate voltage	V
I_D	Output current density	A/mm
$I_\mathrm{D}^\mathrm{max}$	Maximum output current	A/mm
I_OFF	OFF-state leakage current	A/mm
I_ON	On-state current	A/mm
$V_\mathrm{G}^\mathrm{max}$	Maximum gate voltage	V
L_G	Gate length	μm
L_GD	Gate to source length	μm
L_GS	Gate to drain length	μm
w_fin	fin width	μm
FF	Filling factor	%
l_fin	Length of the fins	nm
V_OL	Low-level output voltages	V
V_OH	High-level output voltages	V
NM_L	Low noise margin	V
NM_H	High noise margin	V
α	Driver to load resistance ratio	%
C_top	Top capacitor of tri-gate fin	F

C_{side}	Sidewall capacitor of tri-gate fin	F

Acronyms

Abbreviation	Full name
GaN	Gallium Nitride
Si	Silicon
SiC	Silicon carbide
2DEG	2-Dimensional Electron Gas
PV	photovoltaic
D-mode	Depletion-mode
E-mode	Enhancement-mode
BFM	Baliga's Figure of Merit
JFoM	Johnson figure of merit
BHFFM	Baliga's High Frequency Figure of Merit
P_{pz}	piezoelectro polarization
P_{sp}	spontaneous polarization
DUT	Device under test
HEMT	High Electron Mobility Transistor
MESFET	Metal-Semiconductor Field-Effect Transistor
MOSFET	Metal-Oxide Field-Effect Transistor
MISFET	Metal-insulator-Semiconductor Field-Effect Transistor
FP	Field plate
LV	Low voltage
HV	High voltage
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N-type Metal-Oxide-Semiconductor
DCFL	Direct-coupled FET logic
IC	Integrated Circuits
MMIC	Monolithic Microwave Integrated Circuits
RF	Radio Frequency
UVLO	Under voltage-lockout
GIT	Gate injection transistor
EBL	Electron-Beam Lithography
MSBA	Multi-stage boost architecture
CSI	Common source inductance
FinFET	Fin field-effect transistor
VTC	voltage transfer characteristic
VSD	Voltage Source Driver
CSD	Current Source Driver
RGD	Resonant Gate Driver
HCl	Cloridric acid
Cl_2	Chlorine
BCl_3	Boron trichloride
SiO_2	Silicon dioxide
BOE	Buffered Oxide Etch
SEM	Scanning electron microscopy
FIB	Focused Ion Beam
ALD	Atomic layer deposition
RTA	rapid thermal annealing
AFM	Atomic force microscopy
RT	Room Temperature
XHSQ	Hydrogen Silsesquioxane
ICP RIE	Inductive coupled plasma reactive-ion
KOH	Potassium hydroxide
TMAH	Tetramethylammonium hydroxide

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1 Introduction

Distributed energy resources, including photovoltaic (PV) cells, wind turbines, micro-turbines, and energy storage, are playing an increasingly important role in the electric power distribution markets, especially in Europe where renewable energy is highly demanded [1]. Generally, a renewable energy generation system is shown in Fig. 1.1 [2], which consists of primary energy, prime mover, energy conversion and power grid. In order to realize more cost-effective and eco-friendly power conversion compared to conventional techniques, power converters with high efficiency, low cost, and compact size is of great significance for the distributed energy systems [3].

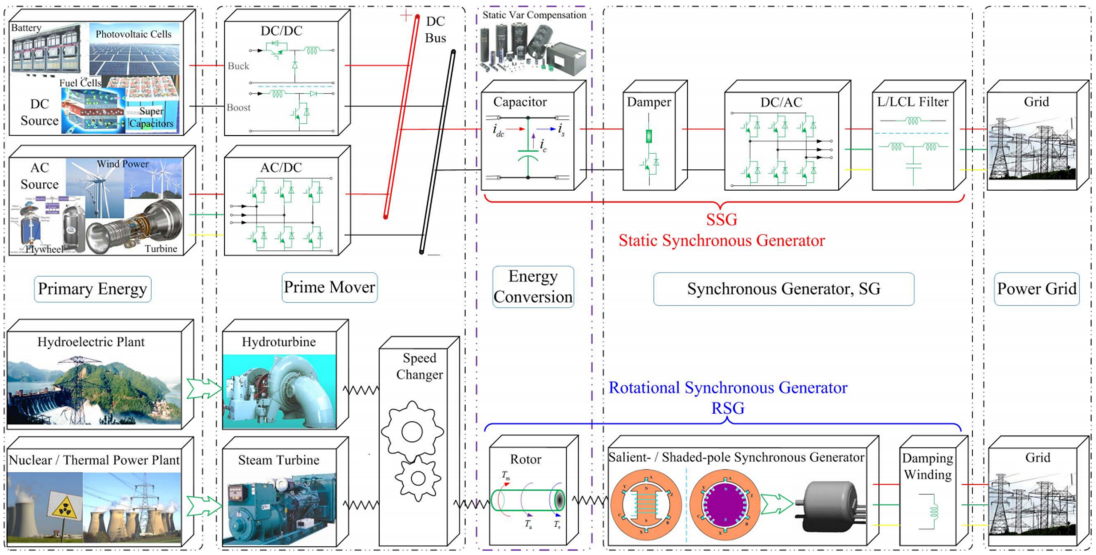


Figure 1.1 – Generalized structure of renewable/conventional energy generation system [2]

The size of bulky passive components, which takes up the largest portion of the overall size, is inversely proportional to the switching speed for power converters [4, 5]. Thus, high frequency switching is extremely essential to achieve compact converters. However, Si-based devices suffer from severe switching losses and thermal issues under high switching frequency [6, 7]. With

much lower switching losses, conduction losses and negligible reverse-recovery losses, GaN transistors show a huge potential for future high-frequency power switching applications.

In the following sections, we first compare GaN with other materials to find out why GaN transistors is favorable for future power semiconductors. Next, we present a comprehensive review of the state-of-the-art of normally-off power transistors for power applications. Later on, the state-of-the-art of GaN based logic gate and monolithically integration will be discussed. Finally, we will talk about the current challenges and the outline of the thesis.

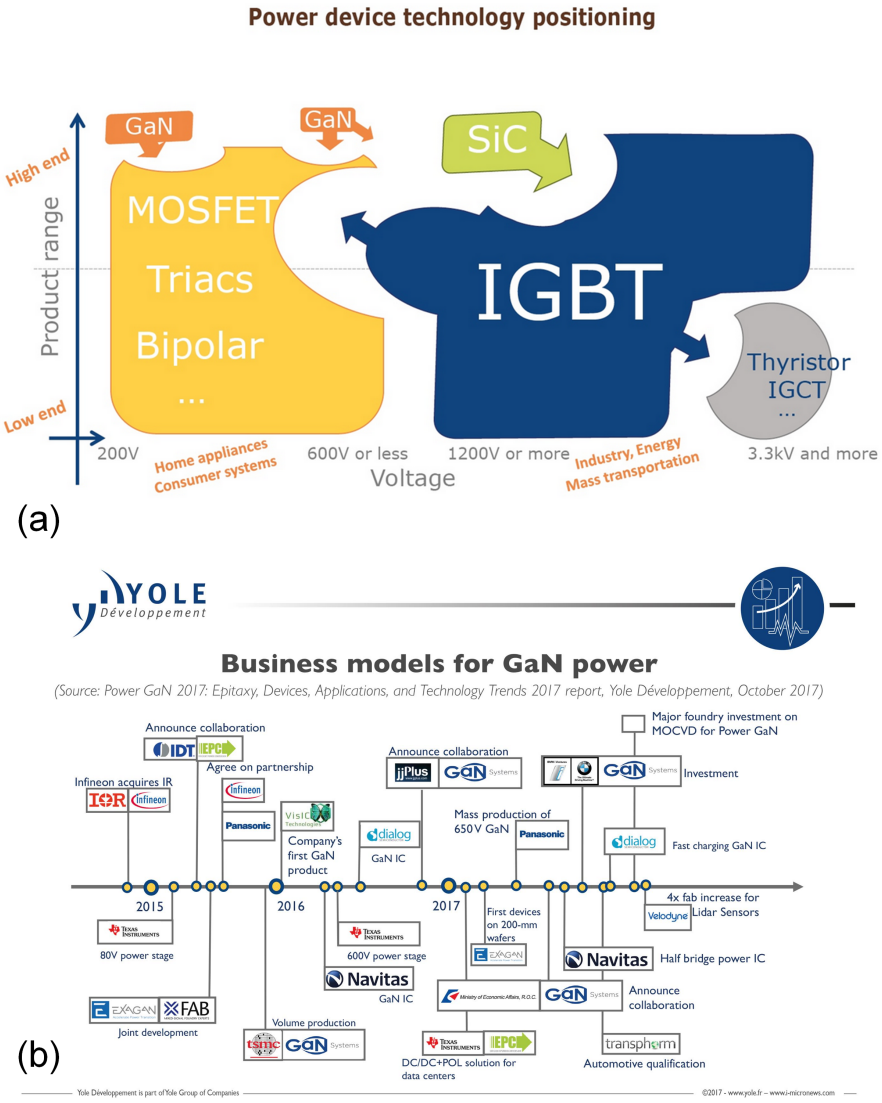
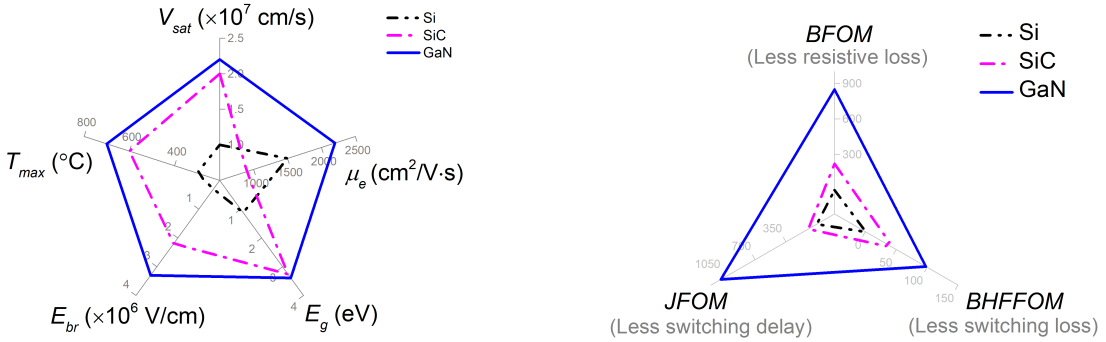


Figure 1.2 – (a) The current position of power device, showing the GaN and SiC existing market and potential market, obtained from https://www.slideshare.net/Yole_Developpement / status-of-power_electronicsindustry2015sample [8].(b) Business models for GaN power device, indicating the massive growth of GaN power device industry, obtained from https://www.systemplus.fr/gan-power-device-industry-the-supply-chain-is-acting-to-support-market-growth/#_ftnref1 [8]

1.1 Advantages of GaN power devices

The key components of a power eletronics system are power semiconductor devices. Traditional power conversion system typically includes MOSFET, Bipolar transistors, IGBT, thyristors, and/or diodes depends on the topologies and applications as shown in Fig. 1.2 (a) [8]. Majority of these power devices are still based on silicon as a direct consequence of the easy availability of low cost and high quality bulk silicon wafers [9]. Though the efficiency and cost have been constantly improved for the conventional Si-based power devices, the improvement rate is approaching a certain limit due to the material limits of Si [10]. It is challenging to make a further improvement in terms of energy efficiency and power density to suit the high demand of industry development nowadays.

On the contrast, wide band-gap semiconductors like Gallium nitride (GaN) and Silicon carbide (SiC) have emerged as the front-running solution to these issues [11–13]. There is an explosive increase in the development of GaN power transistor industry in recent years (Fig. 1.2) and attracted a huge attention from new companies like GaN system, EPC, and Navitas, as well as traditional Si-based companies like Infineon, Panasonic, and Texas Instruments. This can be attributed to the superior property of AlGaN/GaN heterostructures with two-dimensional-electron-gas (2DEG) that offers high electron mobility and saturation velocity, and large bandgap that provides high breakdown field strength and high temperature operation capability as shown in Fig. 1.3 (a) [14, 15]. Moreover, GaN has much better Baliga's Figure of Merit (BFM) [11], Baliga's High Frequency Figure of Merit (BHFFM) [16] and Johnson's Figure of Merit (JFM) [17] than SiC and Si devices as illustrated in Fig. 1.3 (b). However, current GaN device performances are far from their fundamental materials capabilities, which is hindered by a number of factors such as thermal management [14, 18], current collapse [19–21], self-heating [22] and reliability [23, 24].



(a) (b)

Figure 1.3 – Comparison of Si, SiC, and GaN in terms of (a) normalized fundamental material properties as well as (b) three kinds of normalized Figure of Merits (FOM)

Table 1.1 – Comaprison of Si, SiC and GaN power devices in terms of their physical properties together with the BFM, BHFFM and JFM .

Material	E_g [eV]	E_{BR} [MV/cm]	μ [cm^2/Vs]	v_{sat} [cm/s]	BFM	BHFFM	JFoM
Si	1.1	0.3	1350	1.0×10^7	1	1	1
SiC	3.26	3.0	700	2.0×10^7	280	45	180
GaN	3.39	3.3	2200	2.5×10^7	850	98	1090

1.2 The GaN-on-Si Normally-on/off power device technology

Currently, the majority of commercial GaN devices are based on lateral $Al_xGa_{1-x}N$/GaN HEMT on Si structure (Fig. 1.4 (a)) despite the difficult challenges in managing the large lattice and thermal mismatch between GaN and Si as most power applications are cost-sensitive [13]. There was also enormous market potential and the possibility to integrate GaN power switches with the Si-based CMOS circuit technology [25]. In the passed decade, massive efforts have been made to optimize the GaN devices to have low on-resistance (R_{ON}) [26–29], high breakdown voltage (V_{BR}) [29–32], low OFF-state leakage current (I_{OFF}) [33–35], low subthreshold (SS) [36, 37] and large transconductance (g_m) [25]. Especially after the tremendous progress has been made on the epitaxial growth on Si substrates, which can grow 6- and 8-in crack free GaN-on-Si substrate [12, 38].

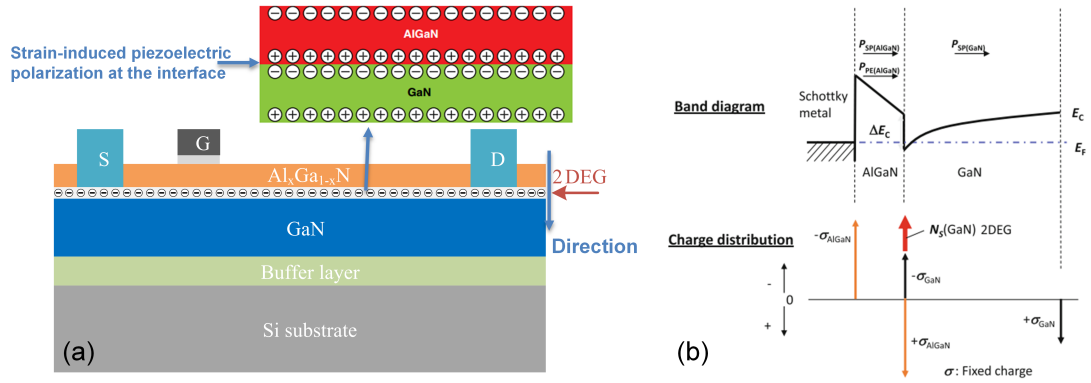


Figure 1.4 – (a) Cross-sectional schematic of an AlGaN/GaN HEMT. (b) Band diagram of the AlGaN/GaN heterostructure and the 2DEG at the interface [15].

The thin layer of $Al_xGa_{1-x}N$ (typically around 20 nm) grown on GaN will form 2DEG at the AlGaN/GaN interface by spontaneous polarization (P_{sp}) and piezoelectro polarization (P_{pz}) effects of the AlGaN barrier layer as shown in Fig. 1.4 (a-b) [15]. The 2DEG channel exhibits excellent electric conductivity due to the high eletron mobility up to 2200 cm^2/V·s and its high electron concentration (N_s), which is essential for the high performance of GaN HEMT devices. However, this structure (Fig. 1.4 (a)) would result in normally-on behavior, which is not ideal and unsafe for power electronics system operation.

Thus, a lot of efforts are carried out by various ways for making normally-off operation in GaN

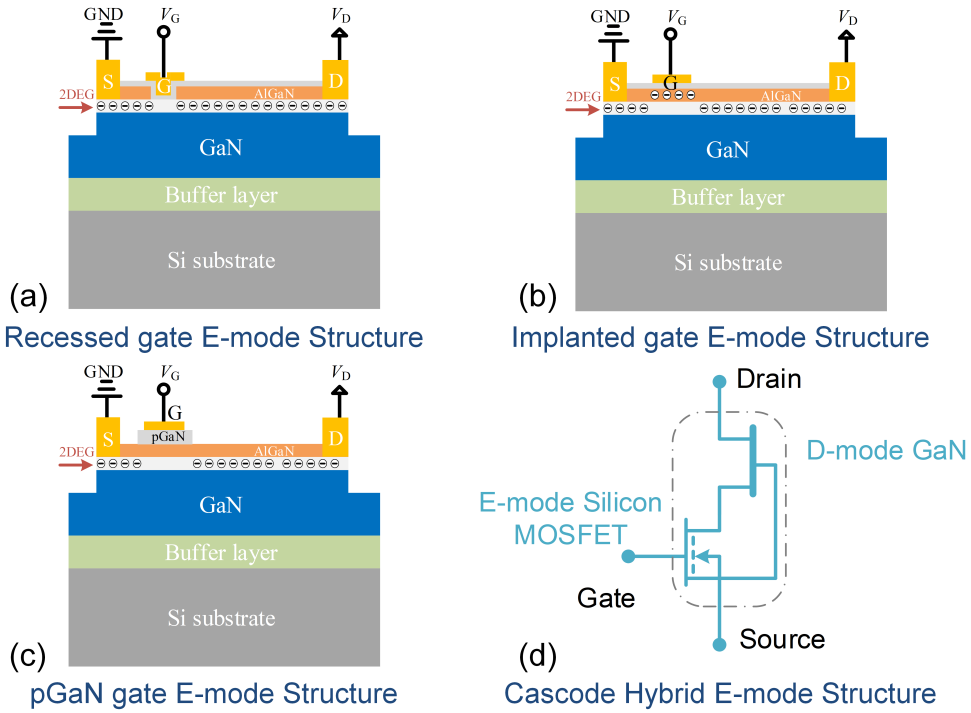


Figure 1.5 – Cross-sectional schematic of a (a) recessed gate, (b) implated gate, and (c) p-GaN gate E-mode structure. (d) Schematic of a typical cascode hybrid E-mode structure.

transistors for the safe operation and for the simplicity of GaN driving circuits [13, 25]. The are typically classified into four categories of normally-off approaches:

1. **Gate recess:** By partially or fully recessing the AlGaN barrier under the gate region (Fig. 1.5 (a)) [39–43].

2. **Implanted gate:** By implanting fluorine atoms into the AlGaN barrier (Fig. 1.5 (b)), these fluorine atoms create a "trapped" negative charge in the AlGaN layer that depletes the 2DEG [44–48].

3. **p-GaN gate:** By growing a p-GaN layer on top of the AlGaN barrier (Fig. 1.5 (c)) [36, 49–55]. If the positive charges in the p-GaN layer have a built-in positive voltage larger than P_{sp}+P_{pz}, the p-GaN gate would deplete the electrons and create an E-mode structure [15].

4. **Cascode hybrid:** By integration a low voltage(LV) E-mode Si-based MOSFET with a high voltage power normally-on GaN transistor (Fig. 1.5 (d)) [56–61].

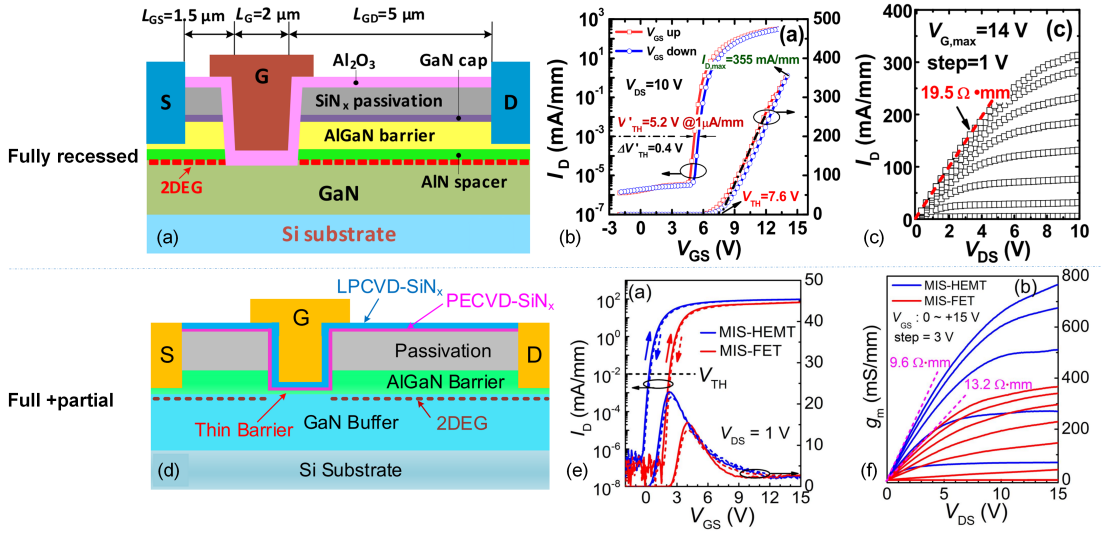


Figure 1.6 – Fully recessed GaN devices: (a) Schematic of recessed devices. (b) Transfer and (c) output characteristics of fully recessed GaN transistors [62]. Fully+partially recessed GaN transistors: (d) Schematic of partially etched MESHEMT.(e) Transfer and (f) output characteristics of MIS-HEMT and MISFET [63].

1.2.1 Recessed gate normally-off transistors

The first practical solution proposed for normally-off GaN HEMT was by fully [62] or partially [63] recessing the AlGaN barrier layer in the gate region (Fig. 1.5 (a)), which has the easiest process compared with other approaches [40]. In order to suppress the gate leakage after recessing, an insulating dielectric was deposited, which formed GaN metal-insulator-semiconductor field-effect transistor (MISFET). The recessed MISFETs were very attractive from the gate driving point of view due to the high V_{TH} and high V_G^{max} compared with other technologies. For example, the high speed switching of 10 MHz has been demonstrated by using recessed structure of E-mode GaN MISFET [64]. It is extremely important in high frequency switching applications, the V_G might exceed the critical safety margin (such as p-GaN gate technology has a limited V_G^{max} around 6-7 V).

However, there were a few drawbacks in this approach. First, due to the lack of high quality dielectric on GaN, the recessed GaN MISFET experienced low V_{TH} stability. Moreover, the addition gate dielectric typically had high density of traps at the interface [13]. Second, as we can see from Fig. 1.6 (a-c), the fully recessed GaN transistor can reach a very high V_{TH} of 5.2 V at 1 μA/mm. However, the R_{ON} was as high as 19.5 $\Omega \cdot$mm and the the I_D^{max} is as low as ~300 mA/mm. There is an important benchmarking between I_D^{max} and R_{ON} versus V_{TH} (Fig. 1.7), which indicates the trade-off between high V_{TH} and low R_{ON}. There were studies showed the partially recessed approaches [13, 63] which left a thin barrier layer under the gate channel to maintain a high electron mobility, leading towards a low R_{ON} (Fig. 1.6 (d-f)). However, this approach requires a highly accurate control of the AlGaN etching technology [25]. The V_{TH}

uniformity was very challenging due to potential uneven etching depth. Moreover, the damage induced by the plasma etching process could lead to an increase in the gate leakage current. Thus, partially recess is not practical for mass production.

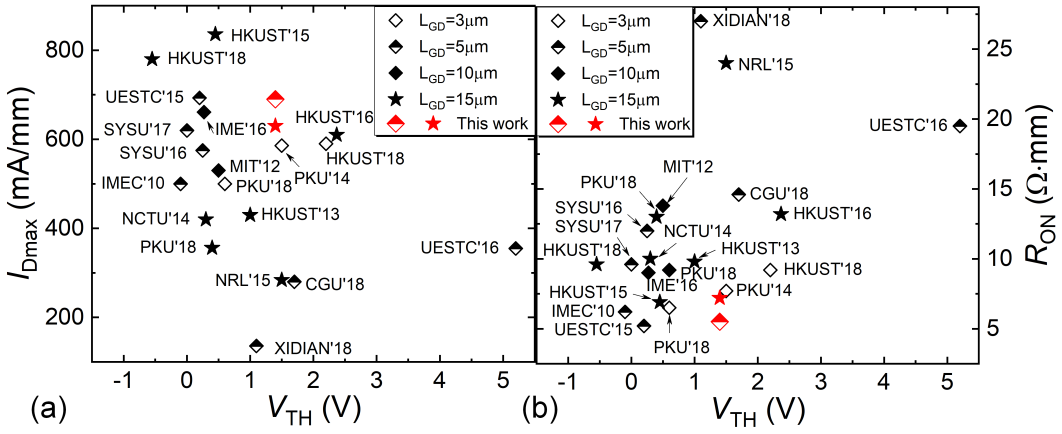


Figure 1.7 – Benchmarking of (a) I_D^{max} and (b) R_{ON} versus V_{TH} (defined at 1 μA/mm) of the recessed tri-gate against E-mode GaN-on-Si transistors. [65]

In general, gate recess is a easy adopted approach to realize GaN normaly-off operation. However, there were challenges regarding to precise gate recess control and high quality gate dielectric might hinder the development of this technology. However, this is a good showcase of how to achieve GaN normally-off operation.

1.2.2 Implanted gate transistors

The introduction of fluorine below the gate electrode has been also used to obtain normally-off operation (Fig. 1.5 (b) and Fig. 1.8). In this case, the negative charge of the F^- ions, introduced either by plasma etch [44, 66] or ion-implantation [67], promotes the depletion of the 2DEG channel, thus leading to a positive shift of threshold voltage V_{TH} (Fig. 1.8 [46]).

This process seems promising because it does not require such processes as the precise etching [68]. The first non-recessed E-mode GaN transistors was reported by Endoh *et al* [69] with V_{TH}=0 V, I_D^{max}=550 mA/mm for V_{GS} =2 V. Palacios *et al* reported the first time positve V_{TH}=0.1 V with fluorine-based gate [70] combined with partial gate recess. The high performance fluorine gate with TiN based source contact exibits high g_m of 412 mS/mm, V_{TH} = 0.6 V and I_D^{max}=845 mA/mm [48].

However, E-mode HEMT can be achieved with fluorine plasma treatment, large fluorine ions can be introduced in AlGaN barrier layer with long treatment time and large bias voltage, which makes the channel electrons density and mobility decrease [68]. Therefore, it is necessary to

optimize the fluorine ions deposition method. As shown in Fig. 1.8 (a), there will be partially etching of GaN/AlGaN during the process of fluorine ionization [46]. The typical structure of the implanted gate transistor is shown in [46]. The fluorine plasma treatment induces a small degradation in the on-resistance and maximum current Fig. 1.8 (c). However, the main draw back regarding to this method is the instability of V_{TH} after a long period or high temperature operation [45].

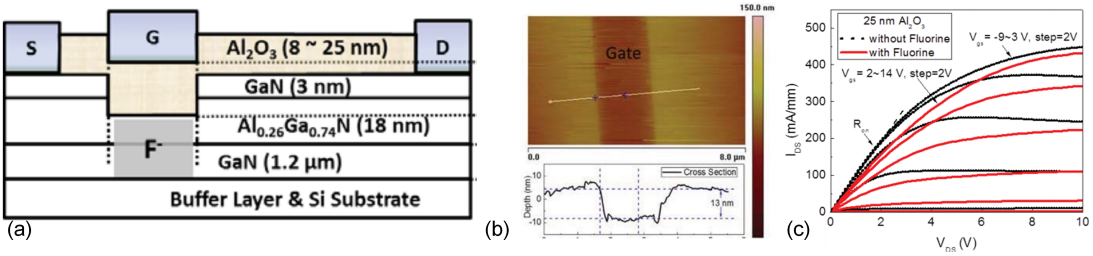


Figure 1.8 – (a) Schematic of the E-mode MOS-HEMT by fluorine plasma treatment. (b) Atomic force microscope picture of the HEMT structure after 150 s CF_4 plasma treatment in the gate region. (c) Output characteristics of standard and fluorinated MOS-HEMTs with 25 nm Al_2O_3 as gate oxide. [46]

1.2.3 p-GaN gate structure

One of the mainstream approach is the use of a p-GaN layer on top of AlGaN/GaN heterostructure [51,71] and the working principle was shown in Fig. 1.9. The p-GaN gate lifted up the conduction band and deplete the 2DEG underneath [72]. One of the first pioneering works in p-GaN gate device was carried out by Uemoto *et al.* [71], who observed the interesting phenomenon in the transfer characteristics of p-GaN gate devices. The conduction of the devices was through the injection of holes towards the interface(Named gate injection transistor (GIT) by panasonic), and this type of device was first commercialized by Efficient Power Conversion(EPC) corporation [13].

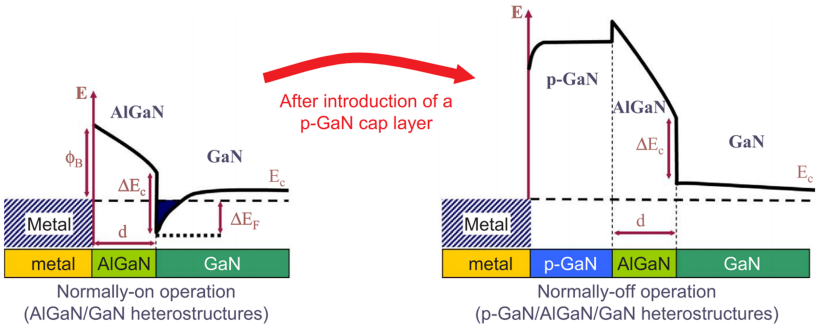


Figure 1.9 – Schematic of the operation principle of the normally-off HEMT with a p-GaN gate.The introduction of the p-GaN layer lifts up the conduction band of the AlGaN, leading to the depletion of the 2DEG. [25]

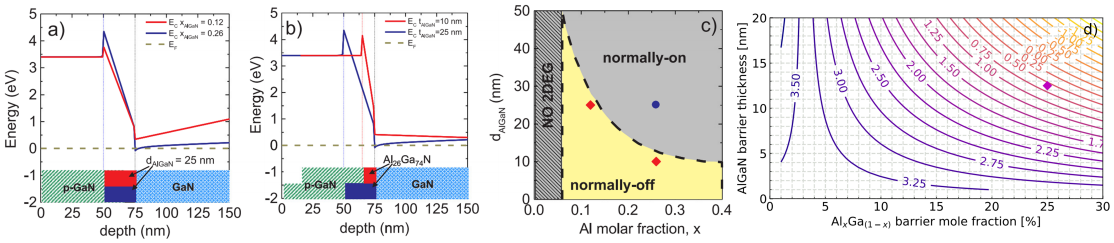


Figure 1.10 – Simulated conduction band diagrams of a p-GaN/AlGaN/GaN heterostructure, for two different values of Al molar fraction (a), or two different values of the AlGaN thickness (b). The borderline between normally-on and normally-off operation mode as function of the Al molar fraction and AlGaN thickness in p-GaN/AlGaN/GaN heterostructures (c) based on the simulations performed in Ref. [25]. (d) Calculated [36, 55] V_{TH} (in Volt) of the p-GaN gate AlGaN/GaN HEMT as a function of mole fraction and thickness of the AlGaN barrier. The diamond symbol represents our AlGaN barrier reference.

However, the p-GaN on top the GaN cannot by itself gurantee the normally-off operation of p-GaN devices. The most important parameters are the thickness of AlGaN layer and the Al concentration to enable normally-off behavior in equilibrium (Fig. 1.10 (a-c)). This is the fundamental in order to efficiently deplete the 2DEG channel and achieve a reasonable V_{TH} [25]. The V_{TH} versus Al concentration and AlGaN barrier thickness is plotted in Fig. 1.10 (d) [36]. Thus, typically low Al concentration and thin AlGaN barrier thickness are required for a typical p-GaN transistors, however, this would lead to higher R_{ON} and low I_D^{max}.

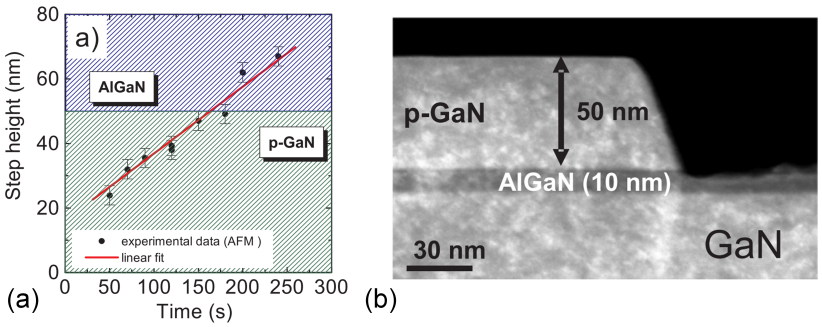


Figure 1.11 – (a) AFM measurement of the step height as a function of the etching time; (b) Cross sectional TEM image of the p-GaN/AlGaN/GaN heterostructure after p-GaN removal from access regions. [25]

One of the big challenges in p-GaN fabrication process is the precise control of etching between p-GaN and AlGaN layer [73, 74] as the majority approach is to remove the overgrown p-GaN in the access region [75, 76]. Typically, the critical etching step is carried out with Cl_2 / BCl_3 low slew-rate ICP etching by controlling the etching time (Fig. 1.11). In practice, the etching rate is difficult to control precisely due to the inconsistent chamber condition for each process. Consequently, a stable and reproducible etching process is difficult to be achieved, which lead to narrow etching time window [77]. Thus, high selectivity between p-GaN and AlGaN is desired for reproducible fabrication process [50, 76]. The etching process has been performed using a

Cl_2/O_2/Ar mixture with a low chamber pressure and low ICP power.

High voltage p-GaN gate FETs face the same dynamic R_{ON} issue as in the normally ON GaN HEMTs, which is also named current collapse. Recently, to solve this current-collapse problem, a hybrid-drain-embedded GIT (HD-GIT) was proposed [13], where an additional p-GaN layer is grown besides the drain electrode and is connected to the drain electrode (hole injection gate), as shown in Fig. 1.12 (a). The hole injection from the additional drain-side p-GaN gate at the OFF state compensates the electron trapping in the epilayer [78]. It has been suppressed current collapse up to 850 V , as shown in Fig. 1.12 (b).

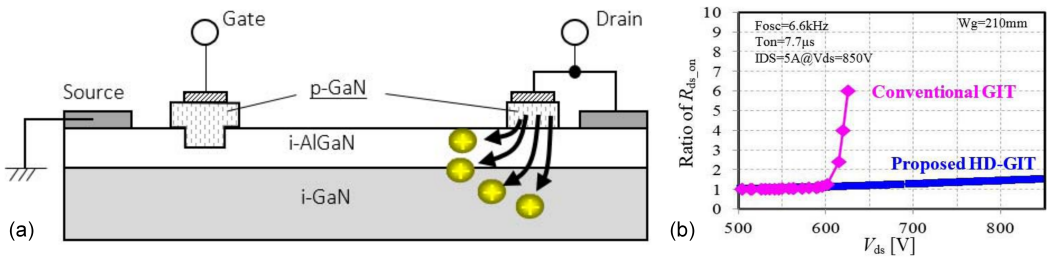


Figure 1.12 – (a) Schematic cross view of the operation of the a hybrid-drain-embedded-GIT. (b) Comparison of dynamic R_{ON} of HD-GIT with conventional GIT. [13]

In summary, p-GaN gate technology is a very promising approach to achieve GaN normally-off operation and it is widely adopted in industry. The main problem is how to further improve the R_{ON} while maintain the postive V_{TH}.

1.2.4 Cascode structure

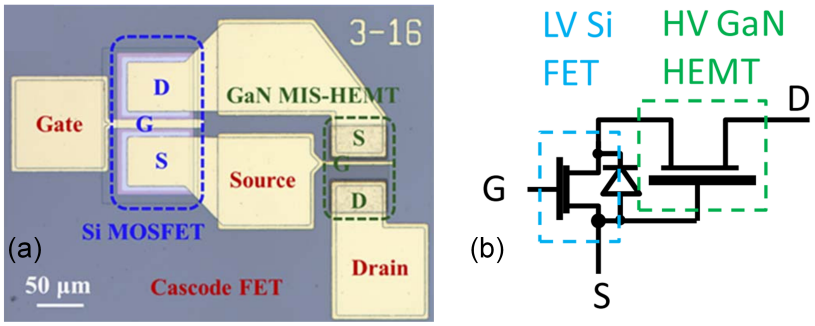


Figure 1.13 – (a) Optical photograph of fabricated device [79]. (b) Schematic of a typical GaN cascode device [13].

Cascode hybrid structure is an alternative way of realizing normally-off operation of GaN by having a LV e-mode silicon MOSFET in series with a HV depletion-mode HEMTs devices to form a cascode structure (Fig. 1.5 (d) and Fig. 1.13) [56–61, 80]. There were a few companies that have adopted this concept due to its gate reliability and high V_G^{max} (15 - 25 V) compared with other GaN technology [57]. The gate control can easily be adopted with the traditional Si

based driving circuit. Fig. 1.13 (a) is the schematic of the typical top view of a fabricated cascode device, which indicates the LV Si MOSFET has larger size compared with HV GaN HEMT [79]. The source and drain ohmic contacts were made with gold-free metal layers for compatibility to a Si foundry [13].

The output characteristics of D-mode HV GaN HEMT, LV Si MOSFET, and the cascode HEMT device were shown in Fig. 1.14 (a-c), respectively [13]. Both transistors were turned on when the V_G of Si MOSFET is on. The R_{ON} of cascode would add up the R_{ON} of Si MOSFET and R_{ON} of GaN HEMT. The percentage of added R_{ON} by rated voltage was shown in Fig. 1.14 (e). The R_{ON} of Si MOSFET would increase dramatically due to the lower voltage rating, which would not be practical for low voltage utilization. The higher induced R_{ON} also affect the gate turn-on/off speed. Moreover, the extraordinary feature of GaN device operates in high temperature will be lost due the usage of Si MOSFET.

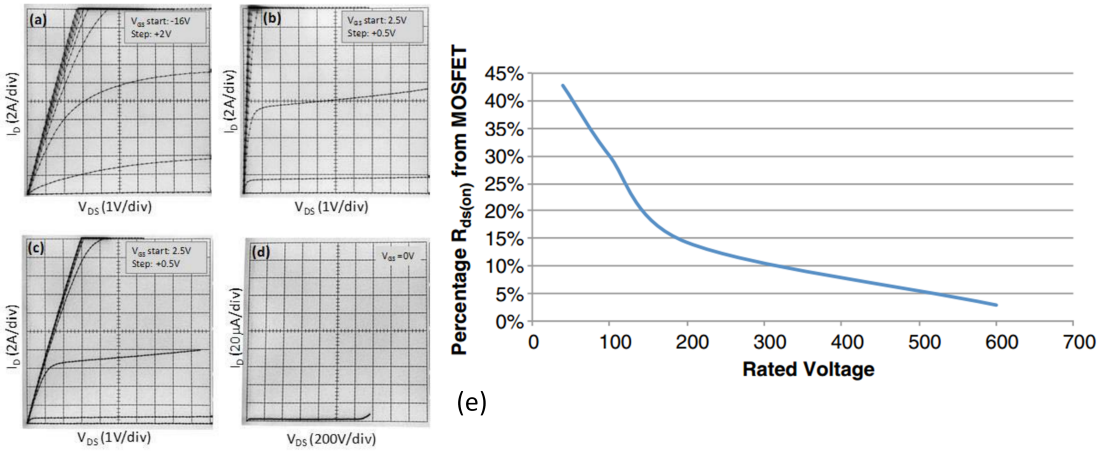


Figure 1.14 – The output I_D–V_G characteristics of (a) D-mode HV GaN HEMT, (b) E-mode LV Si MOSFET, (c) cascode device, and (d) OFF-state blocking curve of the cascode device [13].(e)The percentage of $R_{on,ds}$ from MOSFET compared with GaN devices [15]

In summary, these are very promising approaches to achieve the normally-off operation. However, those techniques have sacrificed the R_{ON} in order to reach positive V_{TH}. In this thesis, we will explore the combination of tri-gate structure to maintain high R_{ON} with normally-on operation. The detailed work will be presented in chapter 3 and 4.

1.3 GaN based logic gates

GaN is one of the most promising materials for high frequency power switching due to its exceptional properties such as large saturation velocity, high carrier mobility, and high breakdown field strength. Despite the advantages of GaN power devices, discrete Si-based logic control and gate drivers still have to be used to control the GaN power devices [82]. Thus, the switching frequency is limited by parasitic inductances from external connections of GaN power devices

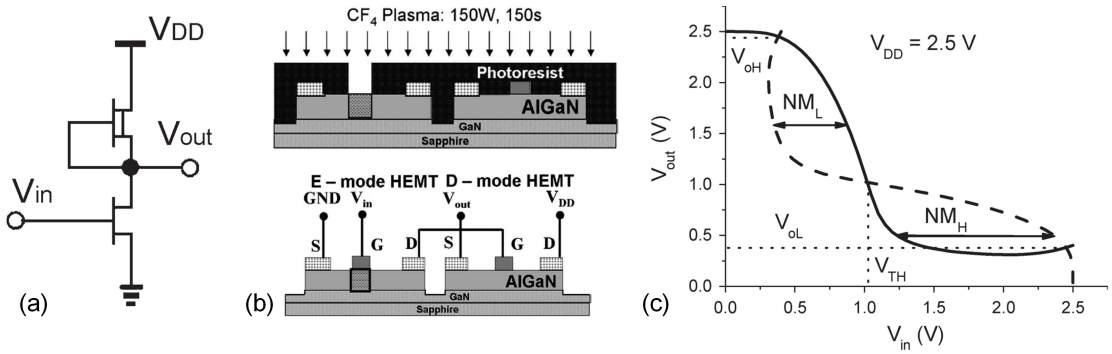


Figure 1.15 – (a) Schematic of the DCFL circuit (b) Cross sectional of E-mode HEMT gate definition and plasma treatment and gate pad metallization. (c)Static voltage transfer characteristics for a typical E/D HEMT inverter. The output levels (V_{OH} and V_{OL}), inverter threshold voltage (V_{TH}), and static noise margins (NM_L and NM_H) are defined. [81]

and gate drivers. A monolithic integration of GaN power devices with GaN-based gate drivers would minimize parasitic components and unveil the full potential of GaN transistors for high frequency power conversion with high efficiency. Such monolithic integration requires GaN-based logic circuits, since they are essential components to realize level shift, driver control, dead time control and under voltage-lockout (UVLO) for driver circuits. However, CMOS logic in GaN is not feasible today due to the poor performance of p-type GaN devices [83, 84].

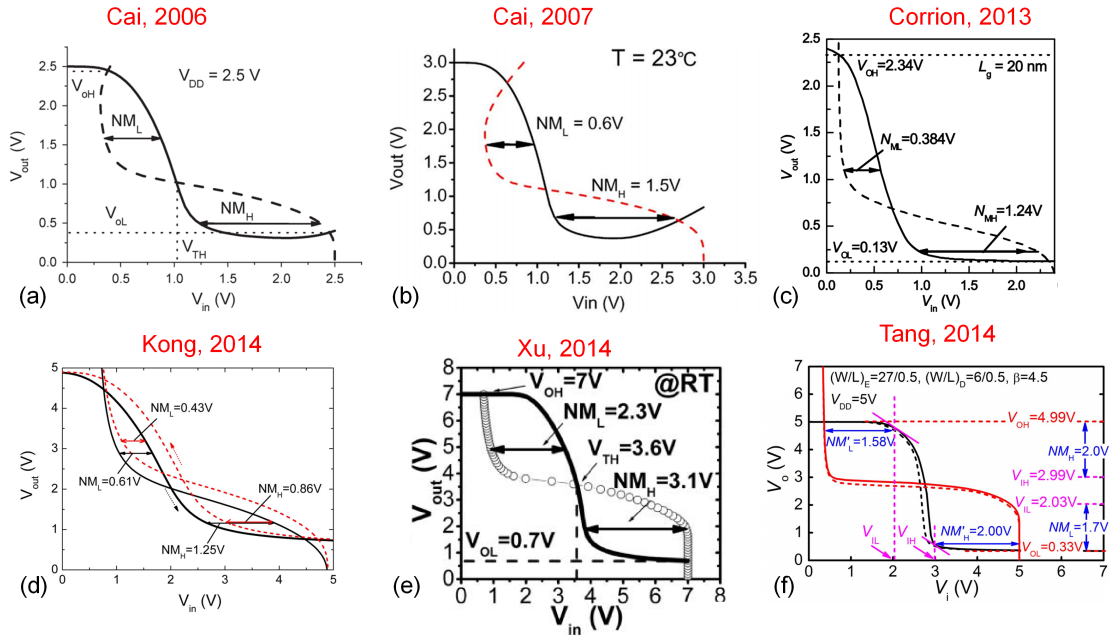


Figure 1.16 – Static voltage transfer characteristics for a typical E/D HEMT inverter of (a)[81] (b) [85] (c) [86] (d) [87] (e) [88] (f) [89] .

The first GaN direct-coupled FET logic (DCFL) is shown in Fig. 1.15 (a). The E-mode and D-mode transistors were fabricated at the same time for the whole process except for the E-mode

GaN definition [81]. The voltage transfer characteristics for the logic is shown in Fig. 1.15, the devices has a relatively poor performance with static low output level (V_{OL}) of 0.3 V. The low noise margin (NM_L) and high noise margin(NM_H) are 0.5 V and 1.12 V, respectively. The performance of the device is insufficient to secure the logic safe operation.

GaN DCFLs have also been demonstrated in [44, 82, 85–87], however their performances are also not sufficient to satisfy the logic requirements, due to their small noise margins, large logic transition voltages, small logic swing and large low-level output voltages (V_{OL}). Recent research show steady improvements on GaN DCFL [89, 90], however the V_{OL} is still quite high, up to 0.3 V and the maximum voltage swing is 4.66 V, which would lead to high logic losses and safety problems. A very distinct property of GaN compared to Silicon is its capability for high temperature operation, which led to the demonstration of GaN DCFLs operating at high temperatures, up to 375 °C [85, 90]. Thus, AlGaN/GaN HEMTs have the potential to be used to construct ICs to perform reliable operations at high temperature that have not be possible for silicon- or GaAs-based technologies.

1.4 Monolithic integration of GaN power IC

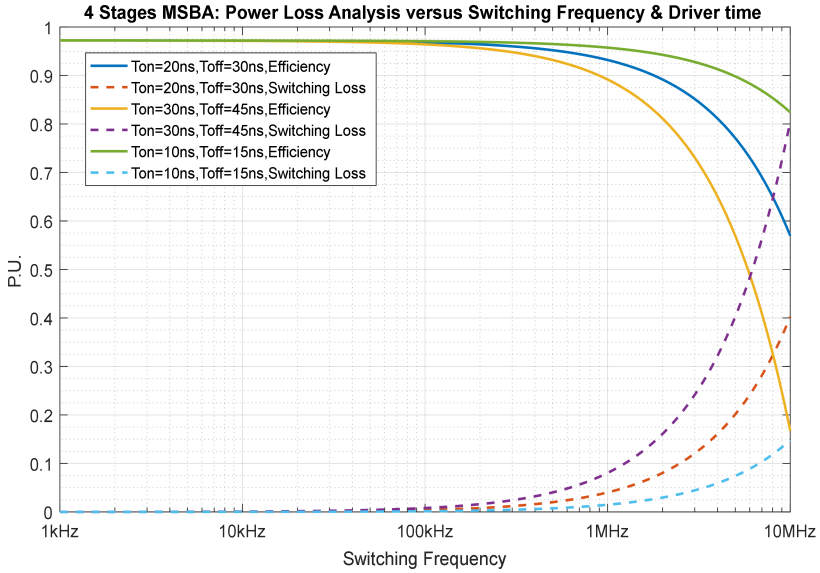


Figure 1.17 – Power Loss analysis versus switching frequency in a multi-stage boost architecture (MSBA)

Increasing the switching frequency of the GaN transistors is an important strategy to reduce the size and volume of passive components in power converters [1] and increase the power density of switching power supplies. However, as the switching frequency increases, both switching losses and gate driver losses increase proportionally, which limits the converter efficiency.

Fig. 1.17 shows the loss calculation of a multi-stage boost architecture (MSBA) based on the

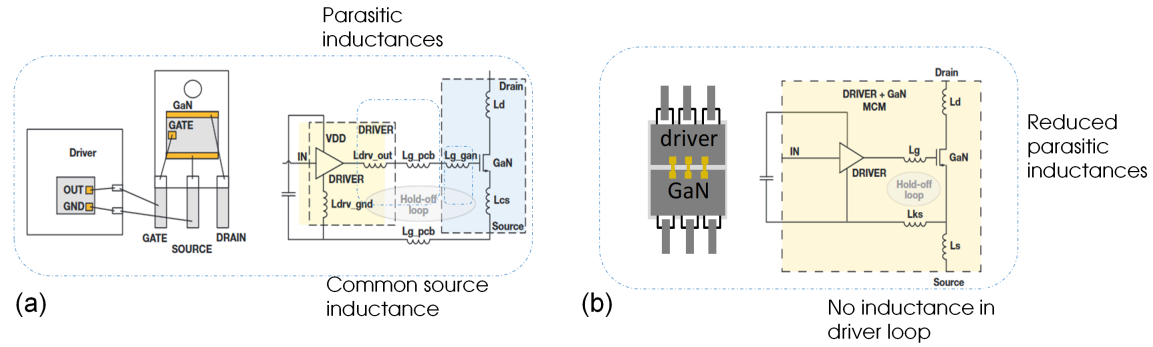


Figure 1.18 – GaN device-driver connection in (a) a separate package [91] and (b) an integrated GaN/driver package.

characteristics of commercial GaN transistors (GS66502B from GaN Systems), which shows the overall system efficiency versus switching frequency. An increase in switching frequency causes a large increase in switching losses, which depend on turn-on/turn-off times of the transistor. The overall efficiency of GaN-based high-frequency power converters can be significantly improved through a judicious design of the switching times of the gate driver.

Traditionally, a discrete gate driver chip is used for controlling GaN power devices as shown in Fig. 1.18 (a) [91], since GaN transistors and drivers are based on different fabrication processes and even come from different suppliers. Thus, bond wires and/or lead connections introduce parasitic inductances and capacitances as illustrated in Fig. 1.18 (a). Fast switching of GaN enables high slew-rate up to 177 V/ns [92] during turn-off transitions, when these parasitic inductances can potentially cause switching loss, ringing and even reliability issues [91].

A monolithic integration of gate drivers with GaN power transistors might solve these issues as illustrated in Fig. 1.18 (b), which will significantly reduce parasitic inductances and eliminate common source inductances (CSI) simultaneously. To maintain very high efficiency, the gate driver will be based on a unipolar topology using GaN HEMTs, since the poor behavior of p-type GaN transistors prevents the use of CMOS-based topologies.

One of the first GaN monolithically integrated circuits can date back to the early 2000s [94, 95], which focused on Monolithic Microwave Integrated Circuits (MMICs) for low power Radio Frequency (RF) applications. The research and development of GaN MMICs gained considerable momentum when it became possible to reproducibly grow high-quality GaN on 4H-SiC substrates [96] for better thermal management. However, few studies have been carried out on the development of monolithic integration of GaN power transistors and drivers for high frequency power conversion. Most of the existing gate drivers designed for GaN transistors are commercial discrete chips such as LTC 3891 for EPC2011 and IXD609 for GS6650X, which are connected externally with GaN power transistors. The typical working frequency of most commercial power devices with discrete drivers are around 100kHz ~ 1MHz in 1kW applications, which is far from the theoretical operation frequency of GaN transistors as illustrated in Fig. 1.19.

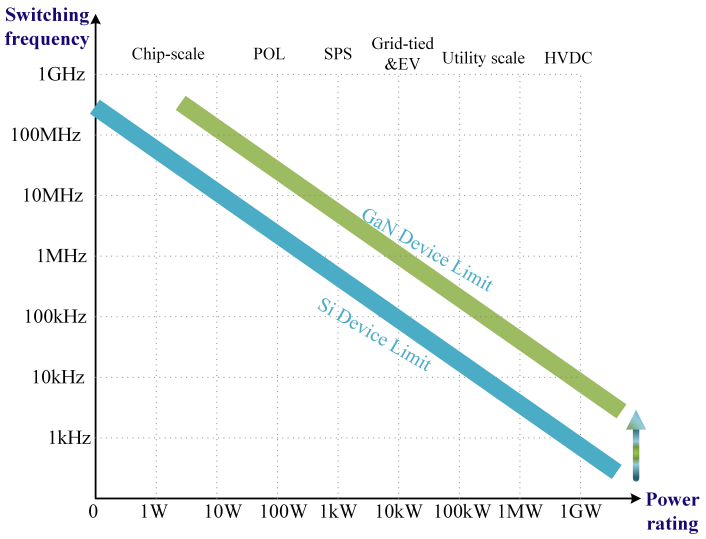


Figure 1.19 – Comparison of Si devices and GaN devices in terms of power rating versus switching frequency [93]

The Fig. 1.19 shows the large potential of GaN devices in high-frequency switches for different power ratings compared to Si devices [93]. It can also be concluded from Fig. 1.19 that the general switching frequency goes down as the system power rating goes up due to the thermal limitation, while with the superior property of GaN the theoretical switching limit of GaN would be much higher compared with Si devices.

1.5 Major challenges

GaN power devices have been explored widely in both industry and academia. A monolithic integration of GaN power devices with GaN-based gate drivers would minimize parasitic components and unveil the full potential of GaN transistors for high frequency power conversion with high efficiency. To achieve this goal, there are a few major challenges:

- **Lack of high performance normally-off GaN transistors:** Due to the polarization effect induced high density and high mobility 2DEG in AlGaN/GaN heterostructure, GaN HEMT is an intrinsic normally-on (D-mode) transistor. However, normally-off transistors are required in most power eletronics systam for safe operation and easier driver design. Although GaN e-mode HEMTs have already been recently commercialized by EPC, GaN System, Transphorm, etc. The normally-off operation is still very challenging due to unsatisfied performance of recessed gate [39–43], implanted gate [44–48], cascode hybrid [56–61] and , p-GaN gate [36, 49–55] compared with D-mode GaN. There is a trade-off of achieving high enough V_{TH} and small R_{ON}.

- **Lack of GaN based logic gates:** Logic devices are essential in driver circuits for control

and protection implementation, which are the basis of smart GaN power IC. Moreover, there have been increasing number of applications that require electronic devices and circuits to operate at higher temperatures, such as automotive and aerospace engine control, and well logging in petroleum exploration [85]. Conventional Si based ICs could not fulfill the high temperature requirement, while GaN has fundamental advantages for higher temperature operation up to 750 °C [97]. However, the poor behavior of P-channel GaN HEMT prevents the development of CMOS based topologies in GaN logic circuit [84]. The only GaN-based CMOS demonstrated in Ref. [84] shows very poor voltage transfer curve of the inverter due to the poor mobility of P-GaN (20 cm^2/V·sec) compared with N-GaN (2200 cm^2/V·sec). Another type of GaN-based logic named direct-coupled FET logic (DCFL) [85, 88] draws focus of researchers, which is based on the idea of NMOS logic with depletion load [98]. However, their performances are not sufficient to satisfy the logic requirements, due to their small noise margins, large logic transition voltages, small logic swing and large low-level output voltages.

1.6 Thesis outline

The thesis aims to overcome the challenges above by developing novel structure for GaN normally-off transistors and logic gate circuits.

Chapter 2 elucidates the impact of tri-gates on the characteristics of GaN transistors, including V_{TH}, R_{ON}, trench conduction, etc. In particular, we have compared the difference of tri-gate in normally-on and normally-off operation.

Chapter 3 presents E-mode GaN MOSFETs based on the combination of tri-gate with barrier recess to yield a large V_{TH}, while maintaining a low specific on resistance ($R_{ON,SP}$) and I_D^{max}. This method overcomes the drawback of high $R_{ON,SP}$ presented in other recessed gate technology and higher V_{TH} stability due to tri-gate technology. The main contents are published in [65, 99].

Chapter 4 reveals a novel concept for GaN normally-off MOS-HEMTs based on the combination of tri-gate, p-GaN, and MOS structures to realize low R_{ON} and high threshold voltage (V_{TH}). In this structure, the p-GaN layer is used to engineer the band structure to reduce the carrier density in the tri-gate region for a high V_{TH} , and the efficient field-effect gate control is mainly from the sidewall gates from the tri-gate. Thus the device operation does not rely on injection of gate current. The MOS structure enabled much larger gate voltages and the effective sidewall modulation resulted in excellent switching performance at high switching frequencies. In addition, this concept eliminates the need for thin barriers (typical in p-GaN devices), which combined to the conduction channels formed at the tri-gate sidewalls, resulted in a smaller R_{ON} compared with planar p-GaN structures. The main contents are published in [100, 101].

Chapter 5 discloses high-performance NOT, NAND and NOR logic gate units with a monolithic integration of E/D-mode MOSHEMTs with planar structure and tri-gate structure. These logic

units were optimized for larger voltage swing, wider noise margin, and smaller transition periods. Such high performance was observed even up to 300°C , which could be applied for high temperature applications. These logic gate are applied to gate driver structure, which would be a huge potential for monolithic integration of GaN power device with gate driver. The main content has been published in [102].

Chapter 6 concludes the thesis and ends with some future perspectives.

2 Tri-gate technologies for normally-off MOSHEMT

2.1 Introduction

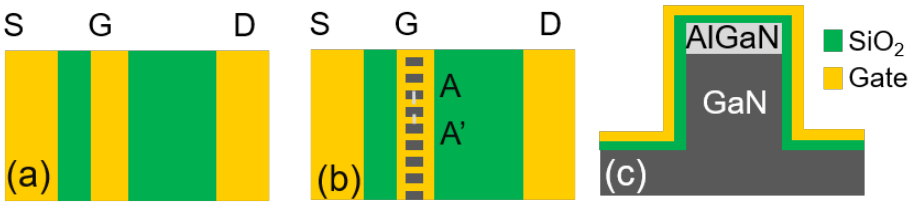


Figure 2.1 – Top view schematics of (a) planar and (b) tri-gate MOSHEMTs. (c) Cross-sectional schematic of the tri-gate region along the AA' line.

The fin field-effect transistor (FinFET) is a multi-gate device, which is traditonally built on a substrate where the gate is placed on two, three, or four sides of the channel [103]. The FinFET devices have significantly faster switching time and higher current density than planar CMOS (complementary metal-oxide-semiconductor) technology [103, 104]. The most widely used FinFET has three gate electrodes warped around the fins, which is also called tri-gate structure. Compared to conventional planar MOSFETs, tri-gate devices experience reduced I_{OFF}, reduced short channel effect, higher on-state current (I_{ON}) [105–107].

Tri-gate technologies have attracted considerable attention for lateral GaN power eletronices devices due to the advantages over conventional planar gates [108–111]. The top view schematics of typical planar and tri-gate MOSHEMTs are shown in Fig. 2.1 (a-b), the main difference between these two devices is the etched nanowire under the gate. Unlike the traditional FinFET technology that grown fin on the substrate, the GaN was partially etched underneath the gate before gate dielectric deposition and metalization. As seen from the cross-sectional view of the tri-gate structure, there were top gate control and two sidewall control in tri-gate structure (Fig. 2.1 (c)). The advantage of sidewall control will be discussed later on in this chapter.

The earlier tri-gate HEMTs were demonstrated using a AlGaN/GaN-on-sapphire heterostructure

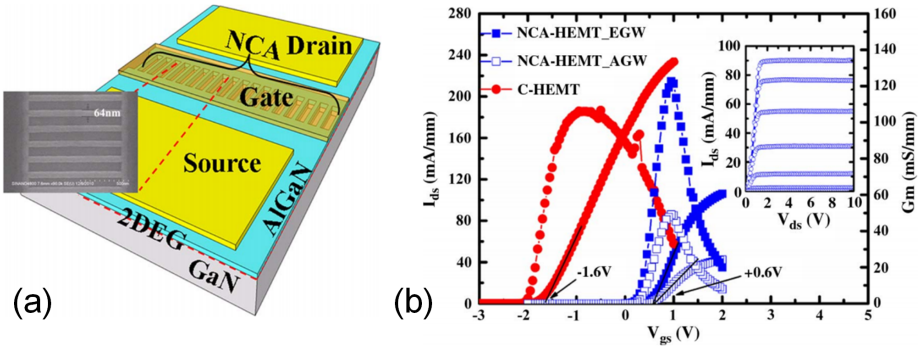


Figure 2.2 – (a) Schematic illustration of nanochannel array (NCA)-HEMT with L_g, L_{gs}, and L_{gd} of 2, 2, and 3 μm, respectively. Inset shows a top view SEM image of the NCA structure before gate metalization. (b) Transfer characteristics of conventional HEMT (C-HEMT) and NCA-HEMT at V_{ds} = 8 V, in which W_{ch} of 64 nm. [111]

, revealing the excellent current stabilities, tunable V_{TH}, reduced I_{OFF} and SS [37, 112]. The dependence of V_{TH} on tri-gate fin width (w_{fin}) has obtained the researchers' attention towards normally-off operation for security operation. The first quasi normally-off tri-gate HEMT was achieved by narrowing down the w_{fin} down to 64 nm [111], which has V_{TH} of 0.64 V (V_{TH} was determined by extrapolation of the transfer curve in linear scale) (Fig. 2.2). The further narrowing down the w_{fin} to 20 nm was demonstrated [113], which exibited V_{TH} over 0 V at 1μA/mm. Improvements have been made combined with partially recess [114] and large work function gate metal [113].

In the following sections, we will discuss the unique features of tri-gate structure in normally-on/off transistors. The detailed investigation has been carried out for better understanding of these features. Especially, the superior advantage of tri-gate structure in normally-off transistor are investigated, revealing the potential of tri-gate technology in future power electronics applications.

2.2 Impact of tri-gate structure on normally-on transistors

In this chapter, we mainly focus on the discussion of how tri-gate structure impact on GaN normally-off operation. We will firstly overview a few key features that tri-gate on normally-on transistors.

In summary, the tri-gate structures offer the following unique features:

- **Improved gate control:** Due to combined effect of top gate control and side wall gate control. The device exibits lower SS and higher g_m, which greatly improved the device performance.
- **Tunable V_{TH}:** Due to the increased capacitors, strain relaxation and sidewall depletion,

the V_{TH} is changed accordingly due to the change of w_{fin}. This feature is one of the main feature of tri-gate structure and can be used to realize excellent normally-off GaN transistors.

- **Enhanced V_{BR}:** The tri-gate structure acts as an integrated field plate compared with planar device, which can better distribute the electric field and then enhance the V_{BR}.

2.2.1 Improved gate control

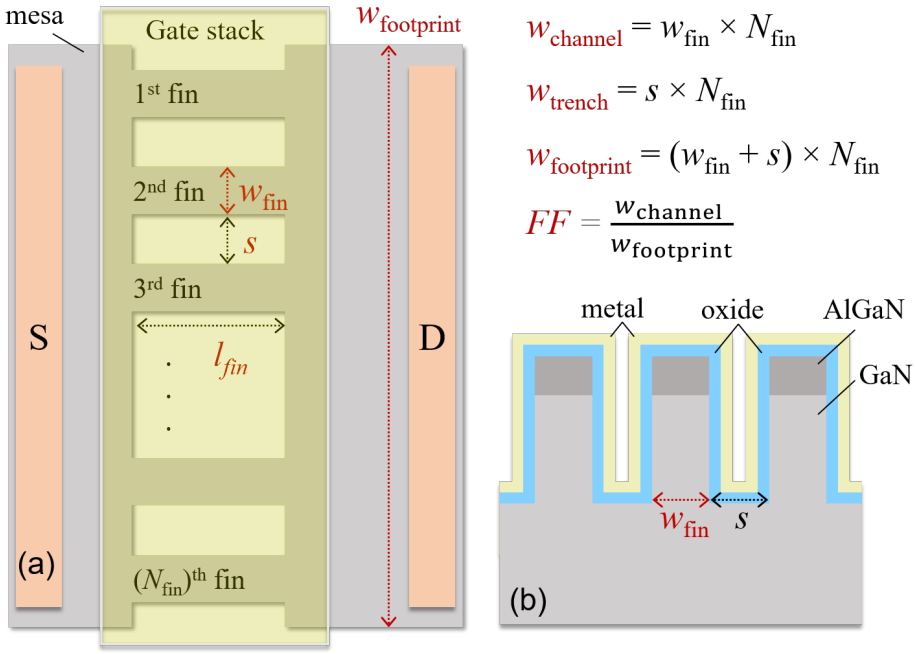


Figure 2.3 – (a) Top schematic view of tri-gate GaN MOSFET. (b) Cross-sectional schematic of the tri-gate region and important parameters definition [115].

In order to define the tri-gate structure, some important parameters regarding to tri-gate are shown in Fig. 2.3 [115]. The detailed definitions were in Ref. [115]. The researchers have demonstrated the effective control of tri-gate compared with planar devices [114–116]. The transfer characteristics of g_m–V_G and I_D–V_G characteristics in tri-gate AlGaN/GaN MOSHEMTs with different w_{fin} was shown in Fig. 2.4 [115]. As shown in Fig. 2.4(a-b), V_{TH} increased and SS decreased with narrower w_{fin}. In planar MOSHEMTs, V_{TH} was - 7.43 V and SS was 98 mV/dec, which were improved by the tri-gate with w_{fin} of 123 nm to -1.68 V and 83 mV/dec, respectively [115].

2.2.2 Tunable threshold voltage

One of the key feature of tri-gate GaN device is the dependence of V_{TH} on w_{fin} (Fig. 2.5), which has been used to control the breakdown voltage, leakage current, as well as logic gate. This

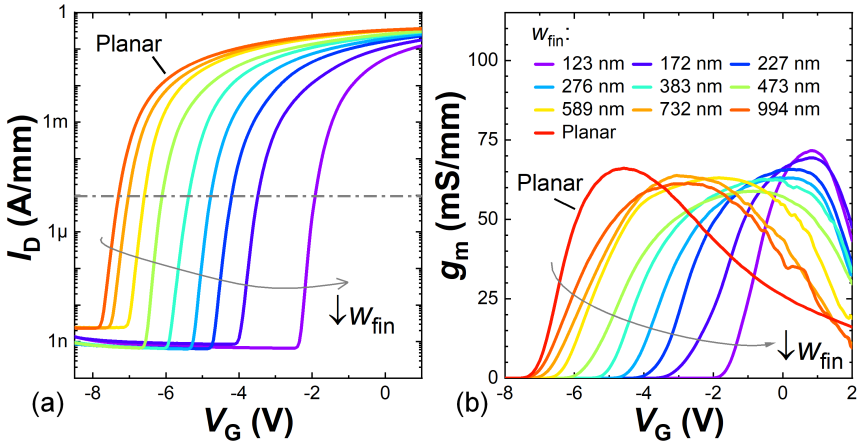


Figure 2.4 – Average (a) I_D–V_G and (b) g_m–V_G transfer characteristics in tri-gate GaN transistors, measured at V_D = 5 V. The w_{fin} was measured by SEM [115].

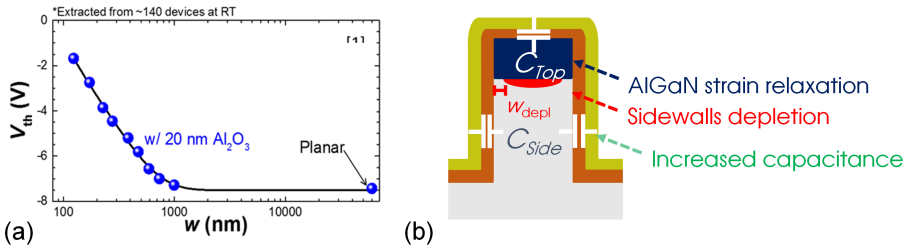


Figure 2.5 – (a) Dependence of V_{TH} on w_{fin}. (b) The effect of sidwall depletion in distributing the 2DEG across a fin. [14]

dependence of V_{TH} on w_{fin} is determined by several reasons, including the increased C_{fin} and the reduced N_s in narrower fins caused by strain relaxation and sidewall depletion, which can be described in more details as follows:

1. **Increased capacitance:** The simplified tri-gate fin model includes three capacitors (Fig. 2.5(b)). The top capacitor (C_{top}) is formed by the gate dielectric and the barrier layer, and the two sidewall capacitors ($2{\cdot}C_{side}$) are formed by the oxide and parts of the fin sidewall body. C_{side} is a varied value that depends on both w_{fin} and V_G, and increases as w_{fin} reduces, similarly to double gate junctionless transistors. It should be noted that the C_{top} can also increase as w_{fin} decreases due to the fringing electric field, especially when w_{fin} approaches the thickness of the barrier and the dielectric layers.

2. **Strain relaxation:** The strain of AlGaN/GaN heterostructure starts to relax after the fin etching by elastic deformation, which partially relieves the strain and reduces the N_s. Such relaxation highly depends on the dimension of the fins [117, 118], and can diminish the charges from both piezoelectric and spontaneous polarization effects.

3. **Sidewall depletion:** Carriers within the fins are depleted within a certain width (w_{dep}) from the sidewalls towards the fin center (Fig. 2.5 (b)). Thus N_s, even at the center of the fin, can be affected by sidewall depletion. This is a crucial factor that allows to achieve normally-off tri-gate GaN transistors. In addition, w_{dep} is also important to determine the equivalent width of the 2DEG (w_{2DEG}) within each fin and extract an equivalent N_s.

2.2.3 Enhanced breakdown voltage

The limited V_{BR} is still far from the GaN materials capabilities. One of the important reason for such early breakdown is the inhomogeneous distribution of the electric field [119, 120]. When a high voltage is blocked in OFF state, the electric field is concentrated at the edge of the gate electrode, leading to the early breakdown of the device [121]. Various designs of field plates (FPs) have been developed to spread more homogeneously the eletric field for the gate edge [31, 122, 123]. Typically, such FPs were achieved by a precise control over oxide thick ness by modulate the gate capacitance, which is not very practical for fabrication. J. Ma *etal*. has presented the novel concept of slanted tri-gate architecture to effectively spread the electrical field by using the tunable V_{TH} of tri-gate structure [124] (Fig. 2.6). With tri-gate structure, an improvement in V_{BR} from 877 V to 1100 V was achieved. And the V_{BR} can be further improved up to 1350 V with barely 10 μm L_{GD}.

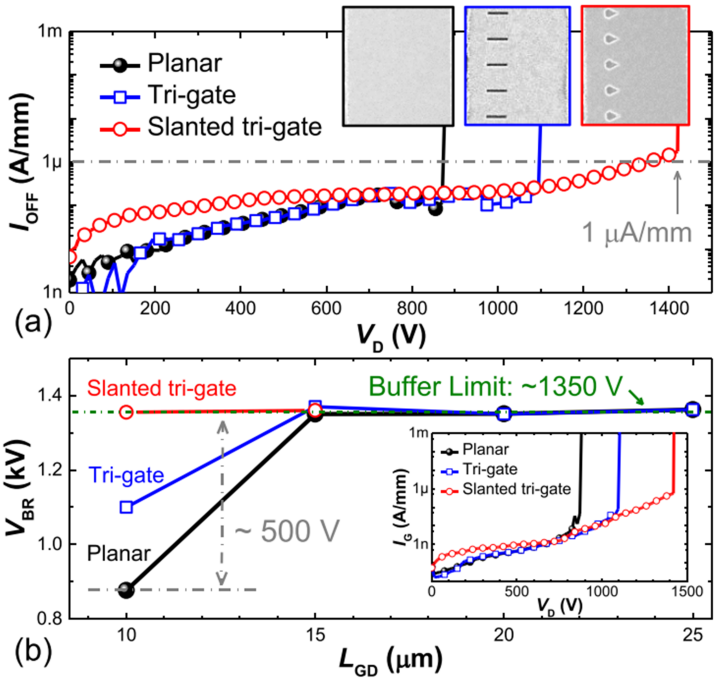


Figure 2.6 – (a) Breakdown characteristics of GaN transistors with planar gates, tri-gates and slanted tri-gates and (b) their L_{GD}-dependent V_{BR} (at 1 μA/mm, V_G= 10 V) with a floating substrate. [124].

2.3 Impact of tri-gate structure on normally-off transistors

The unique tri-gate feature of improved gate control, tunable V_{TH} and enhanced V_{BR} can be further extended towards GaN normally-off operations. Better understanding of the impact on normally-off operation can beneficial to explore the full potential of tri-gate structure. In this section, we will investigate the effect of tri-gate structure on the performance of normally-off devices.

2.3.1 Trench conduction

Trench conduction is one of the most important features of tri-gate GaN devices, which indicates an additional conductive channels formed oxide/GaN interface at the sidewall and bottom in the trench region (Fig. 2.7 (a-b)). The trench conduction acted as a MOSFET transistor, which is in parallel with 2DEG transistor (Fig. 2.7 (a)).

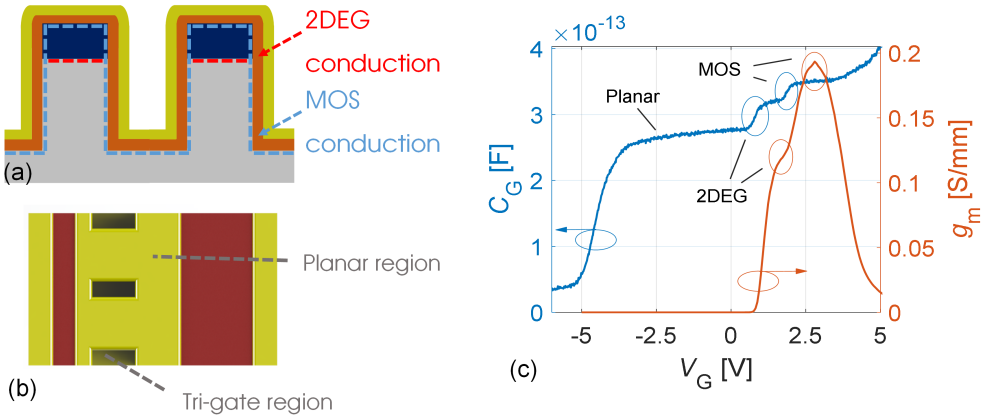


Figure 2.7 – (a) Cross-sectional view of tri-gate sidewall. (b) Top view of a typical GaN tri-gate transistor. (c) Gate capacitors (C_G) and g_m dependence on V_G [113].

This phenomenon has also been reported by many studies [125–129]. As shown in Fig. 2.7 (c), the g_m curve has two peaks corresponding to the conduction contribution from the 2DEG in the fin top layer and the MOS channel at the fin sidewalls [113]. This phenomenon can be also seen from CV measurement (Fig. 2.7), there were 3 capacitors plateau which indicates the turn on of planar region, top fins conduction region, and trench conduction regions. The periodically gate-recessed MOS transistors were fabricated (Fig. 2.8 (a-b)) with SiO_2 as the gate dielectric to observe this phenomenon [125]. L_{GS} and L_{GD} were 4 μm, while L_G was 132 μm. The gate region was etched periodically with long fins with length of 165 nm (period of 300 nm) and depth of 114 nm (Fig. 2.8). The transfer and output characteristics of this devices was shown in Fig. 2.8 (c-d). This device has normally-off behavior with $V_{TH} \sim 2$ V in linear scale. This work clearly showed that the trench conduction is presented and it is working like a normally-off transistor.

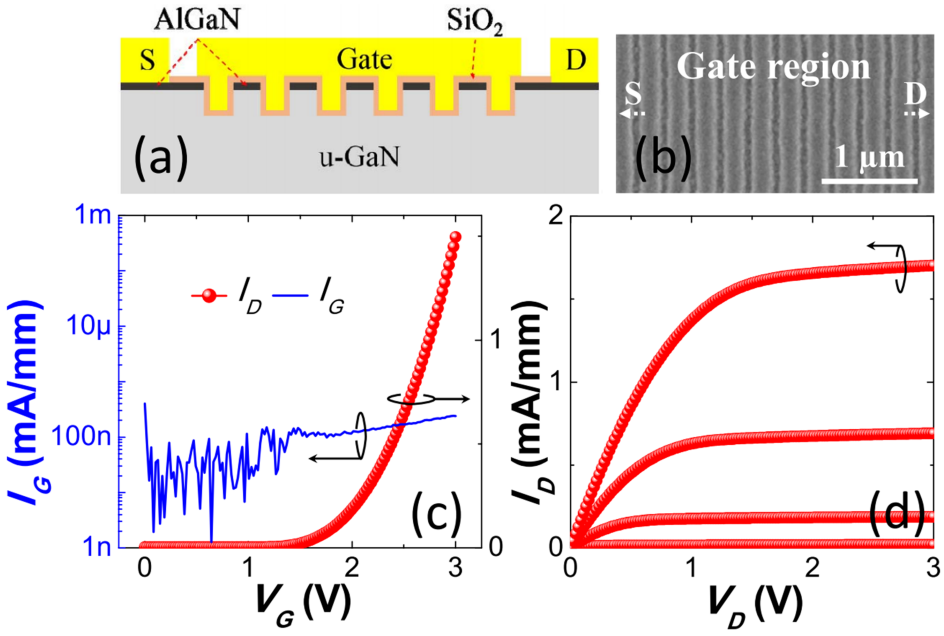


Figure 2.8 – (a) Cross-sectional view of the periodically gate-recessed MOS transistors. (b) Top view of gate region of the transistors. (c) The transfer and (d) output characteristics of this devices [14]. This work shows the existence of tri-gate trench conduction by J. Ma and E. Matioli.

Trench conduction is presented in normally-on transistors, however, the contribution of trench conduction compared with 2DEG conduction is minor. Firstly, the trench conduction is normally-off behavior (V_{TH} ~ 2 V), while 2DEG conduction is normally-on behavior. Another reason is due to the mobility difference between trench conduction and 2DEG or planar MOS conduction [130–133]. According to the study done by Ma *et al.* [125], the N_s contribution from the trench conduction is about 1/4 of N_s from the planar at V_G = 2 V. The I_D trench contribution is only around 6.5% of that from planar region at V_G = 2 V. Moreover, the normally-on transistor typically did not work at high V_G. Thus, the trench contribution is negligible for normally-on transistors.

However, the trench conduction is very important in tri-gate normally-off operation. One of the reason is the V_{TH} of tri-gate MOSFET region matches with trench MOSHEMT. Thus, the trench conduction might have much more significant contribution.

This phenomenon was investigated by fabricating devices as shown in Fig. 2.9 (a-c). These devices were fabricated in same batch and the fabrication started with Cl_2-based ICP etching for device isolation, followed by metal deposition of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/Ni (60nm)/Au (50nm) and RTA in N_2 atmosphere at 780 ºC to form ohmic contacts. The 200 nm-deep AlGaN/GaN fins were fabricated with electron beam lithography and ICP etching. The w_{fin} was about 200 nm and the FF was ~0.63. Then gate recess region was defined by e-beam lithography with a length of about 150 nm and recessed using ICP etching with a depth of about 30 nm (Fig. 2.9 (c)). The ethcing surface was treated by cycled 37% HCL + O_2 based plasma

to ensure the V_{TH} stability. Then 25 nm SiO_2 was deposited by ALD as the gate dielectric and selectively removed in ohmic contact regions. The comparison of the DC transfer and output

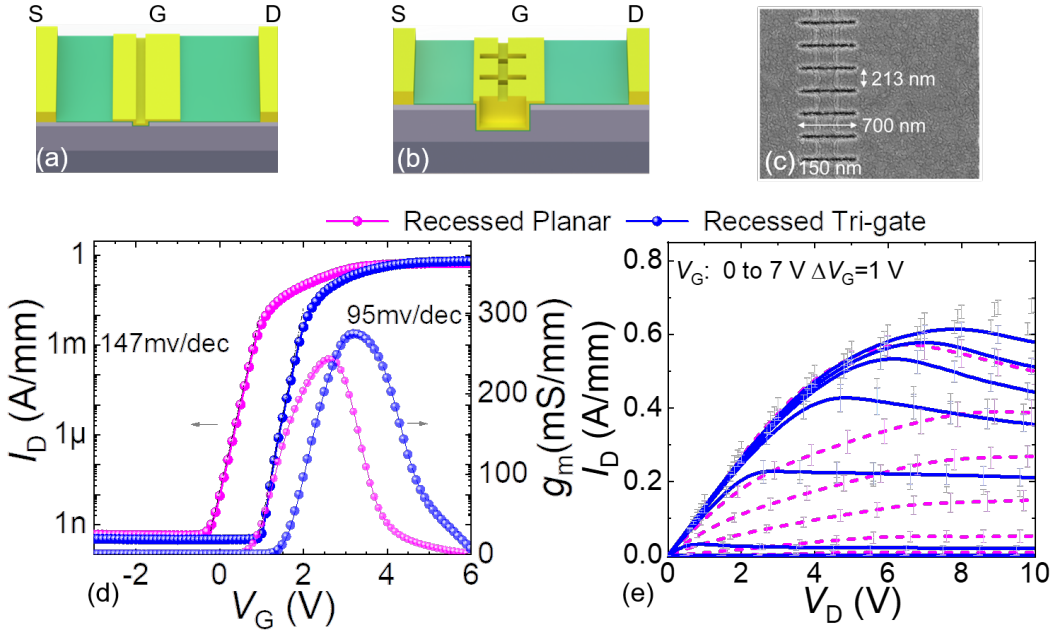


Figure 2.9 – The schematics of (a) recessed GaN MOSFET and (b) recessed tri-gate GaN MOSFET. (c) Top-view of the observed recessed tri-gate region. Comparison of the (d) transfer and (e) output characteristics of recessed GaN MOSFET and recessed tri-gate GaN MOSFET.

characteristics of recessed planar and recessed tri-gate devices is shown in Fig. 2.9 (d) and (e). There is a noteworthy V_{TH} shift of ~1 V from recessed planar to recessed tri-gate MOSFET (Fig. 2.9 (d)). The normally-off tri-gate MOSFET presented a steeper SS and a lower I_{OFF} compared with recessed planar devices, revealing a better gate control by the tri-gate structre. The recessed tri-gate exhibited an ON/OFF ratio beyond 10^9, an enhanced SS of 95.5 ± 3.1 mV/dec comapred to 147.3 ± 4.2 mV in recessed planar device. Moreover, the g_m was increased from 210 mS/mm to 260 mS/mm with tri-gate structure, indicating a combined trench conduction from the sidewall. Furthermore, these devices presented high I_D^{max} (at V_G = 7V) of 622 ± 16 mA/mm compared with 581 ± 34.05 mA/mm for recessed planar (Fig. 2.9 (e)).

Trench conduction is a very important property for tri-gate normally-off operation. In order to better understand the trench conduction mechanism, the simplified conduction model has been built and presented in chapter 3.

2.3.2 Novel p-GaN MOS conduction mechanism

In the last section, we have investigated the important feature of tri-gate for the trench conduction. The trench conduction can reduce the R_{ON}, reduce SS, increase V_{TH}, and g_m. One of the new feature that we have discovered during the thesis is the unique MOS conduction mechanism for

p-GaN MOSFET.

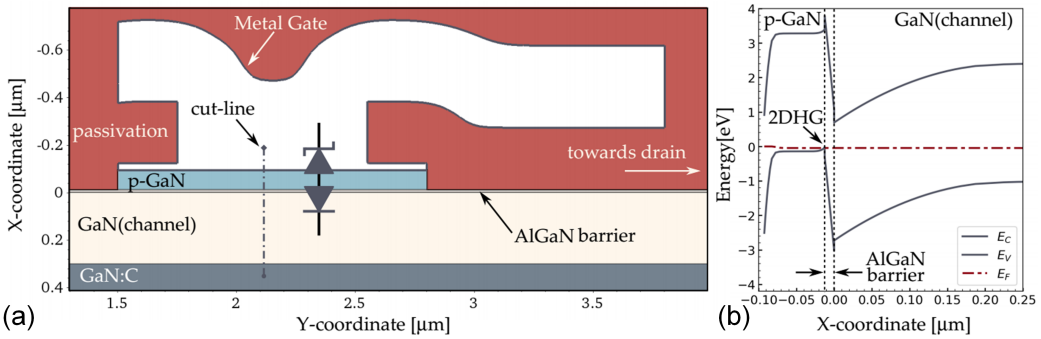


Figure 2.10 – (a) Detailed cross-section showing the p-GaN gate of an AlGaN/GaN HEMT: the metal itself is left blank and contacts the p-GaN layer. (b) Band diagram at equilibrium along the cut-line as indicated in the left figure [36]

.

The mechanism of p-GaN tri-gate MOS conduction is different from traditional p-GaN HEMT. Bakeroot *et al.* has built up the p-GaN conduction model and the V_{TH} changing mechanism for p-GaN HEMT [36, 55]. The cross-sectional schematic of a typical p-GaN HEMT is shown as in Fig. 2.10 (a). As for the traditional p-GaN HEMT, a 2DEG can only form at the AlGaN/GaN interface if at the same time a 2DHG builds up at the p-GaN/AlGaN interface (Fig. 2.11) [36, 55]. The necessary holes for this 2DHG come from the gate metal (Scottky or Ohmic contact) and the fast switching of the device relies on the gate leakage current. If there is a dielectric barrier between the gate metal and the p-GaN layer, the 2DHG cannot build up, and as a result the 2DEG will not form and the transistor remains as the off-state. The gate leakage is necessary for the fast device operation, however, this would lead to a large gate loss and low V_G^{max} (the gate might be broken with high voltage spike). If there was oxide layer in between p-GaN and gate metal, this would lead to low charging and discharging speed of p-GaN MOSHEMT.

In order to investigate how tri-gate structure might help the p-GaN conduction, we have fabricated the device as shown in Fig. 2.11 (a). The detailed fabrication process of this device will be discussed in chapter 4. The cross-sectional view of p-GaN tri-gate and p-GaN planar devices are shown in Fig. 2.11 (b-c). As for the p-GaN tri-gate devices (Fig. 2.11 (a)), the sidewall control is more dominant than the top gate control. Thus, the device can be turned on/off by the side gate. For the p-GaN planar devices, the gate length is small (200 nm) and the gate can be modulated slowly. If we take a cross section along with source and drain of p-GaN planar device (Fig. 2.11. (b)), the gate control from the fringing capacitor is more dominant compared with the top gate. The gate control of p-GaN planar device will be weaker compared with tri-gate devices. We have implemented the pulsed gate setup (inset of Fig. 2.11 (a)) and we observed the switching waveform of drain output voltage. The V_G of p-GaN tri-gate is from 0 V to 8 V and the planar is -1 V to 8 V. When the switching frequency is 500 kHz, the p-GaN tri-gate device can be switched on and off instantly, however, the planar p-GaN MOS could not turn-off at that frequency (Fig. 2.11 (d-e)). The p-GaN planar MOS can be turned off at frequency of 100 Hz

and it took around 4 ms to turn off the device (Fig. 2.11 (g)).

This indicate the superior of using tri-gate structure to enhance the gate control and form the new mechanism of p-GaN MOS conduction. In this way, the V_G^{max} can go up to 10 V and gate leakage will be less than 1 nA/mm up to 8 V (the detailed figure and analysis will be further discussed in Chapter 4).

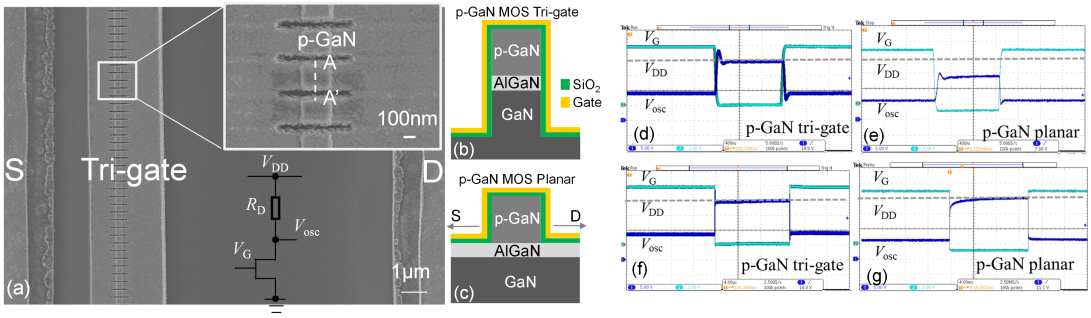


Figure 2.11 – (a) Top-view and zoomed SEM images of the p-GaN MOS tri-gate. Inset: Schematic of experimental setup of p-GaN test. (b) Cross-sectional schematic of the p-GaN MOS Tri-gate region along the AA' line, and of the (c) p-GaN MOS Planar gate along the source-drain direction. Switching waveform of (d) p-GaN tri-gate MOSHEMT and (e) planar p-GaN MOSHEMT devices at 500 kHz. Switching waveform of (f) p-GaN tri-gate MOSHEMT at 1 kHz and (g) planar p-GaN MOS HEMT devices at 100 Hz

2.3.3 Enhanced V_{BR}

The schematic of planar and tri-gate transistors with FPs are shown in Fig. 2.12 (a-b). The gate region in the recessed tri-gate device contains two FPs: tri-gate FP (FP_1) from the recess edge to tri-gate drain-side edge, and planar FP (FP_2) from the tri-gate drain-side edge to gate drain-side edge (Fig.2.12 (c-d)). These regions function as two gate-connected FPs, due to their more negative pinch-off voltages compared to the recessed region, of - 2 V in the tri-gate FP and - 4 V in the planar FP [108, 124, 134, 135]. With increasing V_D, the 2DEG under FP_1 and FP_2 are sequentially depleted, reducing the electric field in the recessed gate region and leading to a much enhanced V_{BR} [31, 120]. In addition, despite the lack of passivation in both devices, this additional FP also improved the dynamic R_{ON} of the recessed tri-gate devices by better distributing the electric field under the gate, as supported by [136, 137] . Moreover, the place where breakdown occurs depends significantly on the difference between V_{TH} of the interfacing regions. We carried out TCAD simulations according to the specifications, which are shown in Fig. 2.12 (c-d). We adjusted the layer thicknesses to represent the relative V_{TH} in our devices. The dielectric thickness of FP_1 in the 1-FP structure is exactly same as the dielectric thickness of FP_2 in the 2-FPs structure. The same gate and drain voltages are fixed at -11 V and 100 V, respectively, for both 1 FP and 2 FPs structure. As we can see from the simulation results, the peak electric field occurs at the gate edge, not at the field plate edge. The electric field under the recessed regions is reduced with 2 FPs, thus enhancing the breakdown voltage.

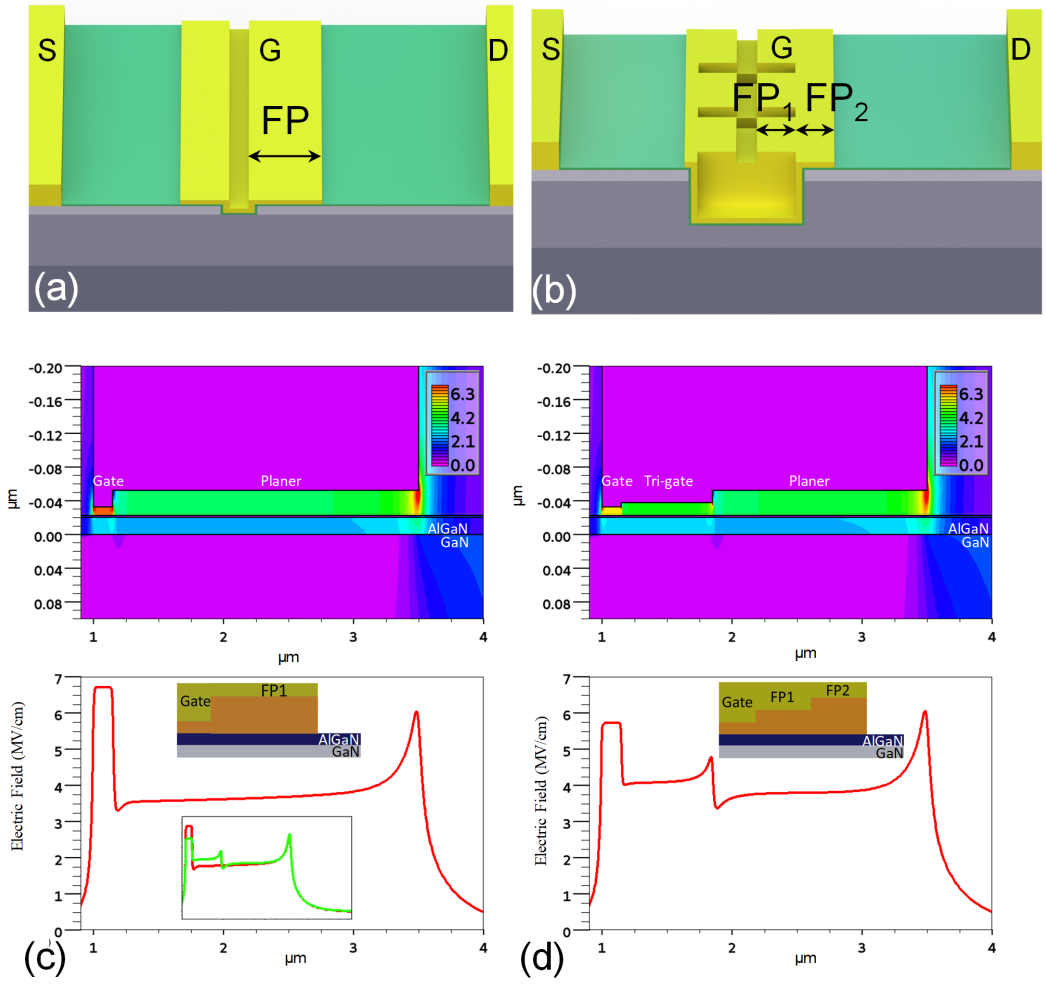


Figure 2.12 – Schematic of (a) planar transistor with one equivalent field plate and (b) recessed tr-gate transistor with 2 equivalent field plate. Schematic and simulated electric field distribution of (d) 1 *FP* and (e) 2 *FP*s, which are representing the recessed planar and recessed tri-gate transistors, respectively under V_G=-11V and V_D=100V. The electric field profiles correspond to the electric filed in the dielectric layer. (Inset) Comparison between the electric field profiles.

2.3.4 Reduced short channel effect

The improved channel confinement of the tri-gate structure is effective in reducing the short-channel effects of the submicrometer recessed-gate GaN MOSFET. The shallow etching of less than 30 nm in depth and 100 nm width in the recessed gate did not create enough barrier in the conduction band to block the electrons and make a completely normally-off devcies. While the recessed planar and tri-gate devices shared the same short recessed regions (150 nm), the tri-gate presented much better performance (Fig. 2.13 (a-b)), which has also been shown in [114], revealing an advantage of the tri-gate in widening the process flow by alleviating the requirement of damage-free gate recess.

The V_D-dependent V_{TH} in the recessed planar devices is likely due to the drain-induced barrier lowering (DIBL). The short recess in the recess planar device could not create enough barrier to avoid DIBL. The recess planar devices with longer recessed region (500 nm) were free of problem (Fig. 2.13 (a)), which indicated the insufficient barrier might be the cause of DIBL. The recessed tri-gate can improve the channel confinement effectively to reduce short-channel effects without R_{ON} degradation compared to wider recess approach.This also affected the output performance of recessed planar device with short gate recess (Fig. 2.13 (b)).

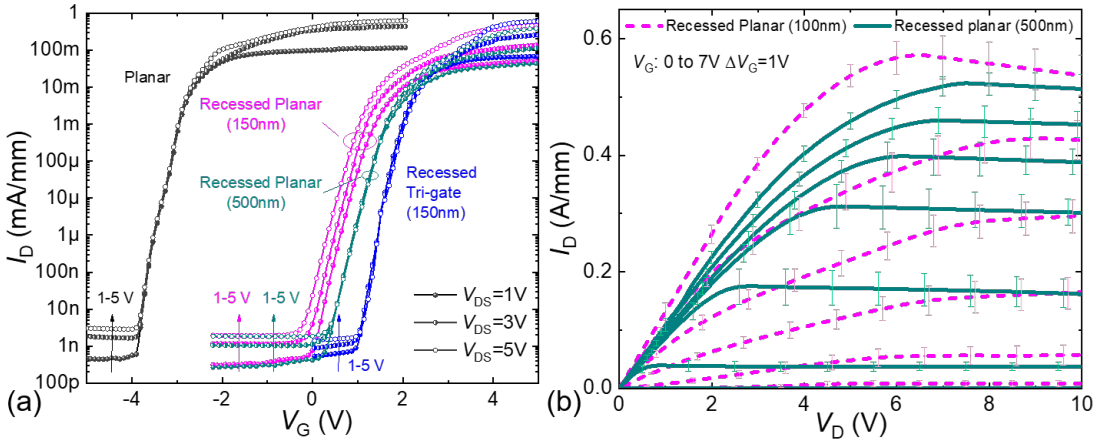


Figure 2.13 – (a) Transfer characteristics of fabricated devices with different drain-source bias (1V to 5V). (b) Output characteristics of recessed planar device with different recess width.

2.4 Conclusion

In this chapter, we investigated the impact of tri-gate on normally-on/off transistors. The V_{TH} can be tuned by adjusting the w_{fin}. The tunable V_{TH} can be used for improving the V_{BR} by designing the tri-gate structure. One of the most important feature is the trench conduction, which can enhance V_{TH}, improve g_m, reduce SS, and reduce the impact of reduce R_{ON} by etching. Though the contribution of channel conduction from the trench is weak in normally-on tri-gate transistors, it has a very strong impact in normally-off transistors. This trench conduction also formed a unique conduction mechanism for p-GaN + MOS structure. The tri-gate sturcture is beneficial for the future power electronics applications.

3 Normally-off transistors with recessed tri-gate technologies

3.1 Introduction

In this chapter, we will discuss one of the techniques that we are using for the Normally-off transistors, which is recessed tri-gate technologies. We present normally-off GaN-on-Si MOSFETs based on the combination of tri-gate with a short barrier recess to yield a large positive threshold voltage (V_{TH}), while maintaining a low specific on resistance ($R_{ON,SP}$) and high current density (I_D). These main results are from Ref.[99] and [65].

As mentioned in previous chapter, a lot of techniques were reported in the literature to achieve normally-off operations, such as p-type gate [77], fluorine based plasma treatment [46, 48], and recessing the barrier [39, 63, 138, 139], under the gate region either fully or partially could contribute to large V_{TH} [63], however these methods typically degrade R_{ON} and lower the I_D^{max}. Tri-gate structure can offer a controllable V_{TH}, enhanced gate control [108, 111, 114] and larger V_{BR} [124, 134, 135].

However, reaching positive V_{TH} relying only on tri-gates, requires very small fin widths [113] in our previous cooperated work, which demands high resolution lithography as shown in Fig. 3.1. A scanning electron microscopy (SEM) image of the device channel is shown in Fig. 3.1(a). The width of the 700 nm-long nanowires in the gate was varied from 15 nm to 40 nm to investigate the effect of sidewall depletion (Fig. 3.1(b)) and A Focused Ion Beam (FIB) cross-section of the nanostructured gate region is shown in Fig. 3.1(c). The transfer characteristics for the transistors with standard Ni-Au gate metal stack are presented in Fig. 3.1(d). Reference devices with planar gates, which is fabricated in the same batch, presented normally-on behavior with V_{TH} = -4.8 V. A significant shift in V_{TH} of about 4 V was achieved by patterning 700 nm-long nanowireds in the gate region with w of 40 nm. As the fin width was reduced, V_{TH} futher approached to 0 V.

This requirement can be significantly relieved by combining tri-gates with gate recess, as demonstrated in this chapter. Additional conduction channels at the sidewalls of the tri-gate trenches compensate the degradation in R_{ON} from the gate recess, resulting in a small R_{ON} of

7.32 ± 0.26 Ω·mm for L_{GD} of 15 m, and an increase in the maximum output current (I_D^{max}).

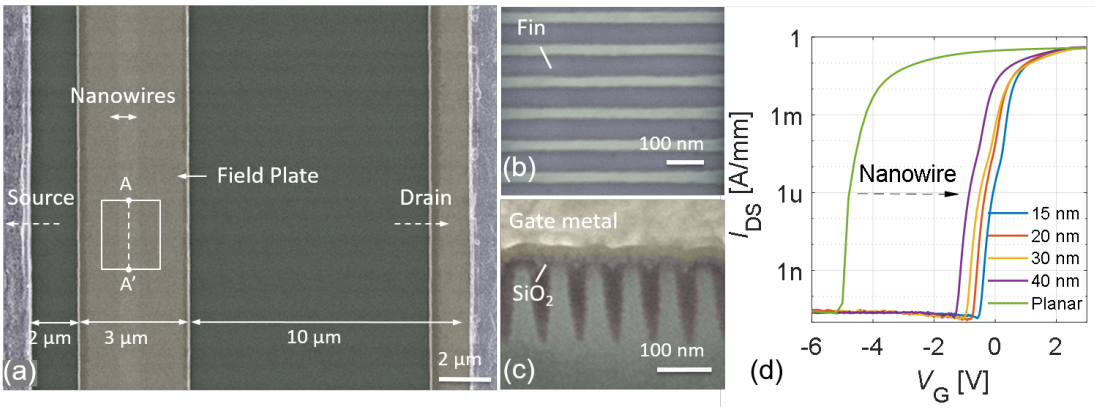


Figure 3.1 – (a) Top-view image of device access region and the gate region is highlighted. (b) Zoomed SEM image of the nanowire region before gate oxide deposition. (c) Cross-section FIB of the gate nanowires along the AA' line. The fins are covered only by 20 nm ALD SiO_2, on top of which the Ni-Au or Pt-Au gate stacks were deposited. (d) Transfer curve for different fin width for Ni-Au gate stack at V_{DS}=5 V. As the nanowire width decreases, V_{TH} further approaches 0 V. [113]

3.2 Device design and fabrication

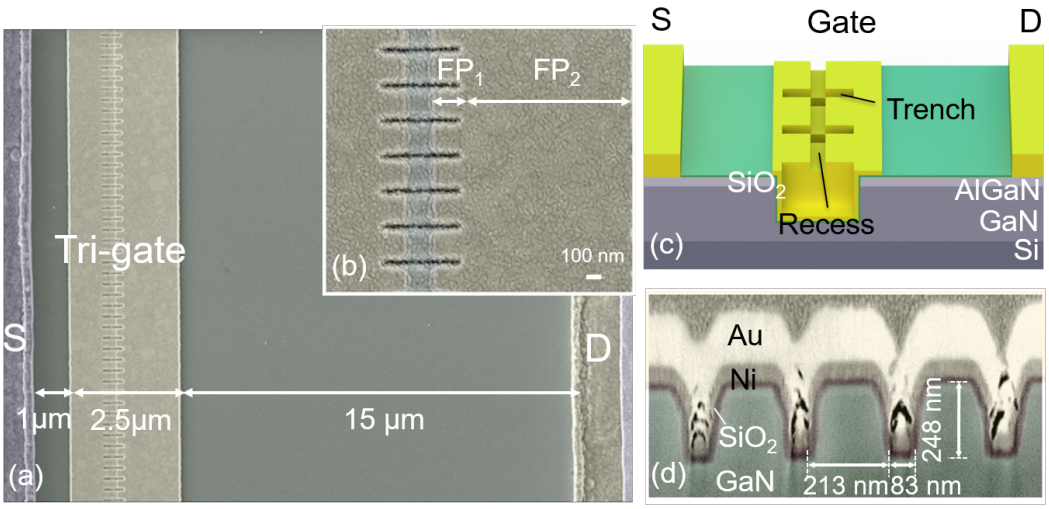


Figure 3.2 – (a) Top-view and (b) zoomed SEM images of the recessed tri-gate MOSFET. (c) 3D schematic of recessed tri-gate MOSFET. (d) Cross-sectional views of recessed tri-gate MOSFET.

The AlGaN/GaN epitaxial structure in this work consisted of 4.2 μm buffer, 420 nm undoped GaN channel, 20 nm $Al_{0.5}Ga_{0.75}N$ barrier and 2.5 nm GaN cap layers. The schematics and scanning electR_{ON} microscopy (SEM) images of the device are shown in Fig. 3.2.

The device fabrication started with the definition of the mesa and tri-gate regions by e-beam lithography, and followed by Cl_2-based ICP etching. The tri-gate width (w) was varied from 200 nm to 600 nm, and the spacing (s) was fixed at 100 nm. This corresponds to filling factors ($FF = w/(w+s)$) varying from 0.66 to 0.87. The tri-gate length (l) was fixed at 700 nm and the height of tri-gate trench (h) was 250 nm.

A 150 nm-long gate recess (l_r) was defined by e-beam lithography, followed by a 20 nm-deep slow-etch-rate Cl_2-based ICP etch. A metal stack composed of Ti/Al/Ti/ Ni/Au was deposited in source and drain regions, followed by rapid thermal annealing. The gate dielectric was 25 nm-thick SiO2, deposited by atomic layer deposition (ALD), without any further passivation layers. Finally, gate and contact pads were formed by Ni/Au. Devices with planar gates (planar) and recessed planar gates (recessed) were fabricated on the same batch with same process conditions for comparison.

3.3 Device optimization and characterization

3.3.1 Device optimization

The main factors that affect device performance were tri-gate fin width and gate recessed length. Thus in this section, tri-gate fin width and gate recess length were varied in order to find the optimum combination to achieve low R_{ON} and high V_{TH} simultaneously.

Fig. 3.3 (a) shows transfer characteristics of recessed tri-gate devices with different recess length (100 nm to 600 nm). We observed that the recessed planar device with 100 nm showed quasi-normally off behavior, however the tri-gate devices with 100 nm recess already exhibited much higher V_{TH} compared to planar devices. There was roughly around 1 V V_{TH} shift from recessed tri-gate to recessed planar devices. Moreover, the V_{TH} of recessed tri-gate devices remained unchanged with the variation of recess length up to 600 nm. Nevertheless, the maximum saturation current decreased with increasing recess length. This proved that the enhanced gate control of recessed tri-gate could minimize the gate recess length and then lower the current degradation.

To optimize the tri-gate geometry, we fabricated devices with w of 200, 400, 500, and 600 nm and fixed s of 100 nm, corresponding to a number of tri-gate wires per mm N_{NW} of 3333, 2000, 1666, and 1333, respectively. We have measured the transfer characteristics of recessed tri-gate transistors with the variation of w (Fig. 3.3 (b)). We have measured the transfer characteristics of recessed tri-gate transistors with the variation of fin width (w) (Fig. 3.3 (b)). The extracted V_{TH} in Fig. 3.3 (c) has revealed that V_{TH} is not strongly dependent on the tri-gate width, which indicates the absence of 2DEG in the recessed region. The recess is a more dominant factor of the V_{TH} compared with w changes, which is different compared with normally-on tri-gate devices. The Fig. 3.3 (d) shows the narrow V_{TH} distribution among measured 56 recessed tri-gate devices, with a V_{TH} of $+1.41 \pm 0.12$ V, confirming the excellent process uniformity of the fabrication and

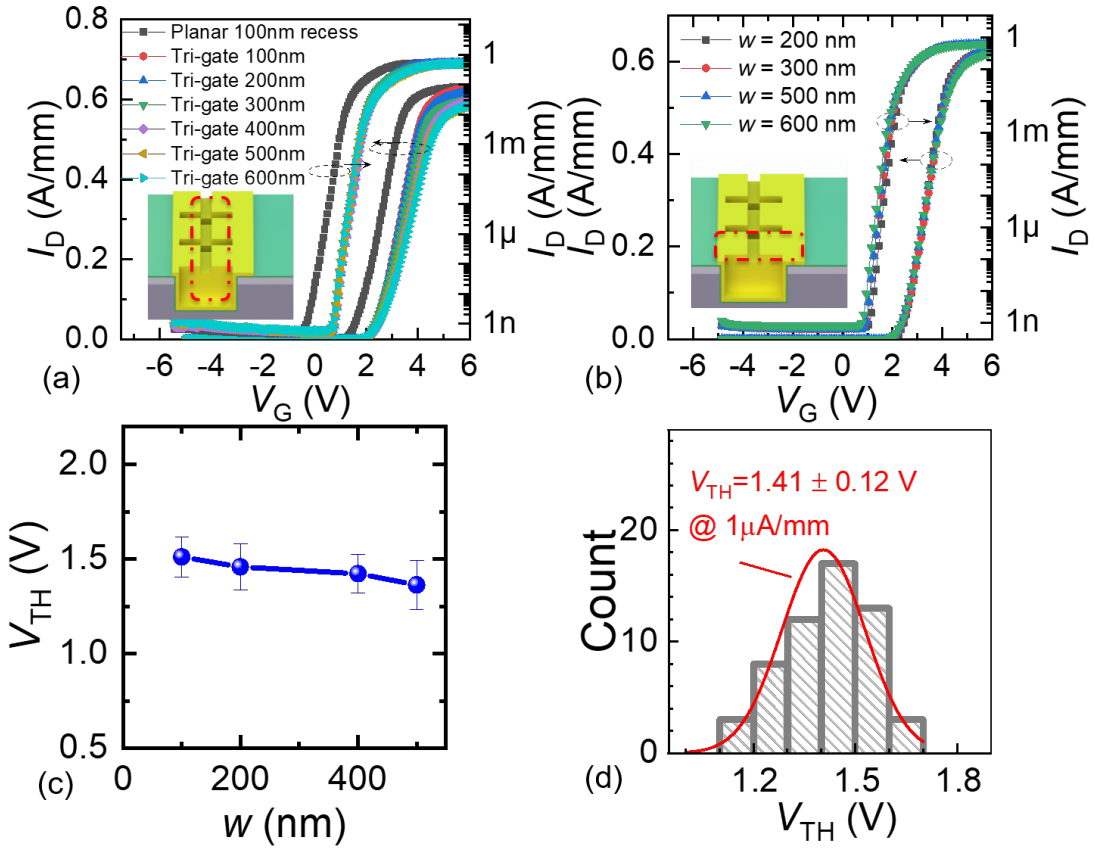


Figure 3.3 – (a) Comparison of planar recessed transistors with recessed tri-gate under different recess length (100nm to 600 nm). (b) Transfer characteristics of recessed tri-gate with different nanowire width. Inset: Schematic of recessed tri-gate regions.(c) The extracted V_{TH} dependence with tri-gate fin width (d) Distribution of V_{TH} of 56 recessed tri-gate devices.

stability of the devices.

3.3.2 Device performance

The transfer characteristics of the Planar, Recessed Planar and Recessed tri-gate devices are shown in Fig. 3.4 (a). A significant positive shift of V_{TH} was observed from - 3.6 V (at 1 μA/mm) for the planar, to + 0.3 V for the recessed and + 1.4 V for the recessed tri-gate (Fig. 3.4 (a)). The large V_{TH} in the recessed tri-gate is mainly due to the strain relaxation of the AlGaN barrier and the sidewall gate modulation [108, 111, 117, 140]. The recessed tri-gate exhibited a larger gm of 275 ± 12 mS/mm, with an ON/OFF ratio beyond 10^9, an improved SS of 95 ± 3 mV/dec and I_{OFF} at V_G = 0 V as small as 300 pA/mm, as compared with planar and recessed devices, revealing an improved tri-gate control over electrons in the channel. The small hysteresis below 0.5 V for all devices, under different V_G up to 8 V (Fig. 3.4 (b)) indicates a good oxide quality. The recessed tri-gate devices showed the smallest hysteresis of 0.18 ± 0.05 V (at V_G^{max} of 8 V)

compared to 0.47 ± 0.09 V of recessed planar and 0.53 ± 0.06 V. Moreover, the recessed tri-gate presented a much narrower V_{TH} distribution among all measured devices, with an average V_{TH} of + 1.41 ± 0.12 V, confirming the excellent gate uniformity of our process.

The output characteristics of these devices are shown in Fig. 3.4 (c). The recessed tri-gate presented a larger I_D^{max} of 622 ± 16 mA/mm at V_G = 7 V compared to 581 ± 34 mA/mm for the recessed planar, which was only slightly smaller than that of the planar D-mode device (672 ± 19 mA/mm) (Fig. 3.4 (c)). The degraded output characteristic of recessed planar devices shown in Fig. 3.4 (c) is likely due to the short recess length of 150 nm, since the recessed planar with 500 nm-long recessed region presented good output characteristics. The recessed tri-gate presented much better performance with the same recess length of 150 nm, revealing a better channel control of the tri-gate combined with a narrow gate recess. The negative output resistance of these devices is mostly due to the self-heating. The R_{ON} of planar, recessed and recessed tri-gate, extracted from I_D - V_D sweeps in linear region, were 6.82 ± 0.29 Ω·mm, 7.37 ± 0.45 Ω·mm, and 7.32 ± 0.26 Ω·mm at V_G = 7 V, respectively (Fig. 3.4 (d)). The recessed tri-gate required a much smaller gate driving voltage to reach low R_{ON} (Fig. 3.4 (d)), as compared to the recessed planar devices, which is due to the superior control of the tri-gate recessed over electrons in the channel that results in a larger gm compared to the planar recessed device.

3.3.3 Equivalent model of recessed tri-gate devices

The low R_{ON} and large I_D^{max} of the recessed tri-gate are a consequence of the trench conduction in the tri-gate geometry. To illustrate this, we fabricated recessed tri-gate devices with w of 200, 400, 500, and 600 nm and fixed s of 100 nm, corresponding to a number of tri-gate wires per mm (N_{NW}) of 3333, 2000, 1666, and 1333, respectively. The R_{ON} was extracted at V_G = 7 V for all recessed tri-gate device, since the small difference in V_{TH} is negligible compared to the driving voltage, and the R_{ON} is already saturated at this V_G. An increase in I_D^{max} and a reduction of R_{ON} were observed when increasing N_{NW} (Fig.3.5 (a)). This can be understood with an equivalent model of the recessed tri-gate MOSFET (inset of Fig.3.5(a)) consisting of 2 parallel parts of the top (recessed + planar) and trench portions of the tri-gate (sidewall and bottom portions), plus the source (R_S) and drain (R_D) contact and access resistances (inset of Fig.3.5 (b)). Thus the total R_{ON} can be written as:

$$R_{ON} = \left\{ \left[\left(\frac{R_{sh}^{r} \cdot l_r + R_{sh}^{p} \cdot (l - l_r)}{w} \right)^{-1} + \left(\frac{R_{sh}^{trench} \cdot l}{2h} \right)^{-1} \right] N_{NW} \right\}^{-1} + R_S + R_D \tag{3.1}$$

Where, R_{sh}^{r} and R_{sh}^{p} are the equivalent sheet resistances of the recessed and top planar regions, respectively. We assumed an equivalent sheet resistance for the sidewall and bottom parts (R_{sh}^{trench}) to simplify the model [126, 129, 141]. The R_{sh}^{r} and R_{sh}^{p} were obtained by averaging 7

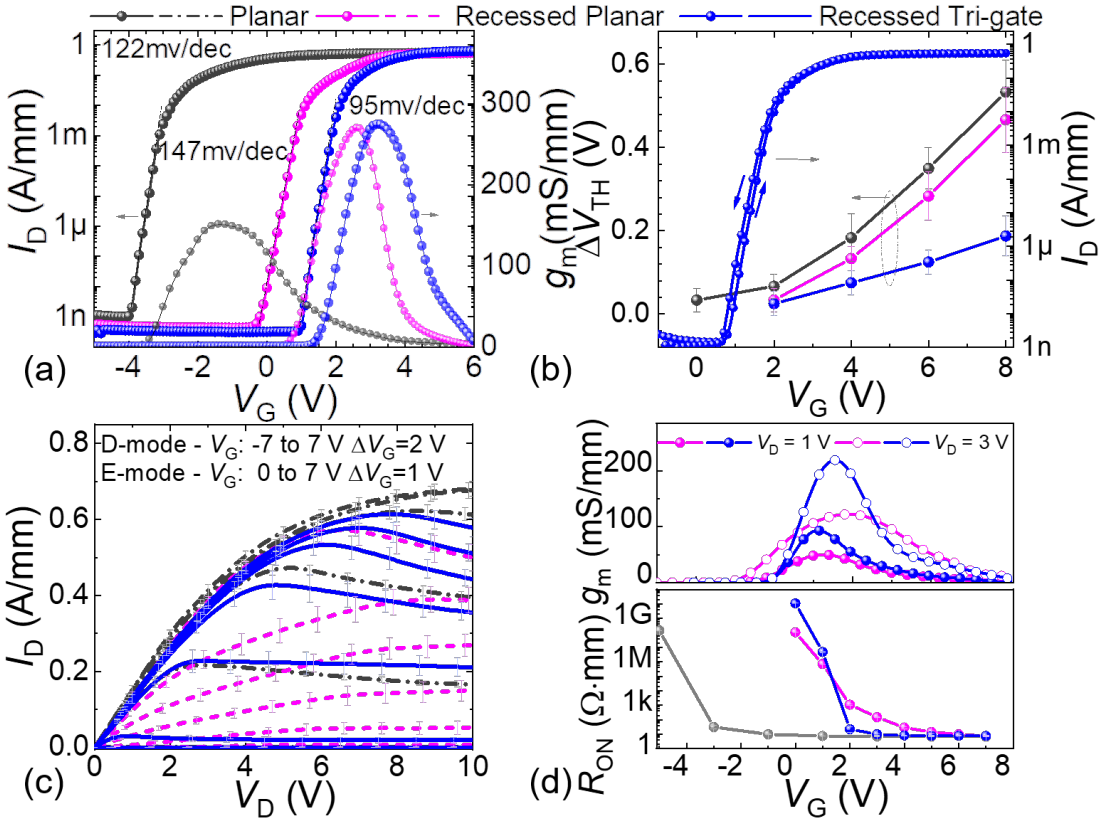


Figure 3.4 – Comparison of the normally-off recessed tri-gate with planar and recessed devices. (a) Transfer at V_D = 5 V and (b) Measured V_G^{max} - ΔV_{TH} dependence of planar, recessed and recessed tri-gate devices and gate hysteresis up to 8 V of recessed tri-gate transistor. (c) Output characteristics of the three devices with V_G up to 7 V. (d) g_m of recessed planar and recessed tri-gate MOSFET under V_D of 1 V and 3 V and extracted $V_G - R_{ON}$ dependence of planar, recessed and recessed tri-gate transistors. The L_{GS}, L_G and L_{GD} were 1, 2.5 and 15 μm, respectively, and FF was 0.66. Standard deviation bars were determined from the measurement of 8 devices of each type, revealing their consistent performance.

separate planar and recessed gated Halls, respectively, resulting in R_{sh}^{p} and R_{sh}^{r} of 269 ± 7 Ω/sq and 1713 ± 92 Ω/sq (at V_G = 7 V). The R_S and R_D were calculated based on the planar sheet resistance and contact resistance from separate TLM on the same wafer. To determine the missing variable R_{sh}^{trench} , the measured R_{ON} versus N_{NW} was fitted using this model (black curve in Fig.3.5 (a)), resulting in R_{sh}^{trench} of 3355 ± 138 Ω/sq. Based on these values, we calculated the share of current flowing at the top and sidewall regions (Fig.3.5 (b)). For large FF, the main contribution to conduction is from the top region, whereas by reducing FF, N_{NW} is increased and the contribution from the sidewalls becomes dominant.

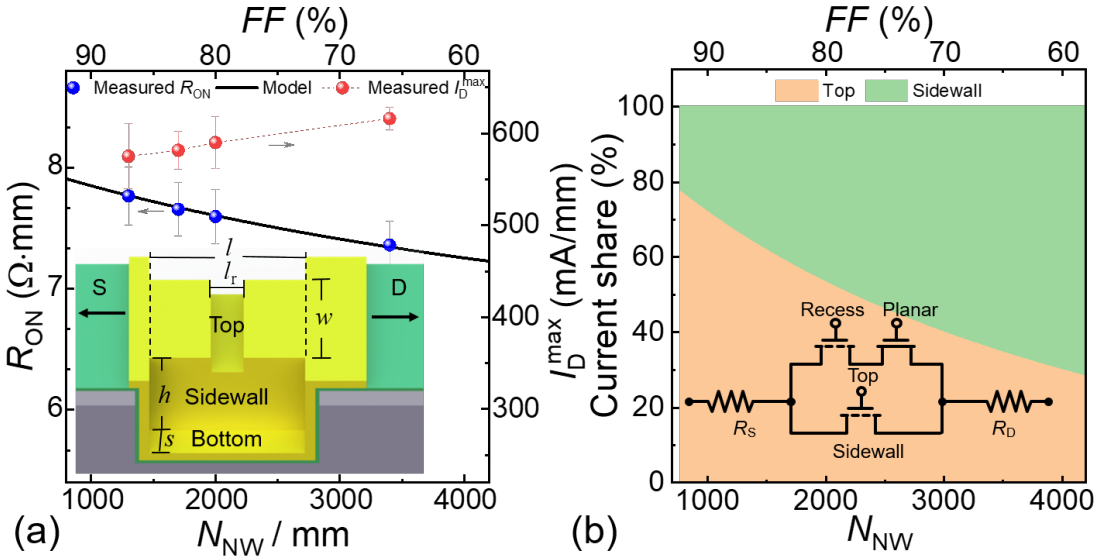


Figure 3.5 – R_{ON} and I_D^{max} of the recessed tri-gate versus the number of nanowires (N_{NW}) and fill factor (FF) in the tri-gate region. (b) Current share in the recessed tri-gate region. Insets: Schematic and equivalent circuit of the recessed tri-gate

3.3.4 Breakdown Characterization of Recessed Tri-gate and Benchmark

The breakdown voltage of the devices was measured with floating (Fig.3.6 (a)) and grounded substrates (Fig.3.6 (b)), with $V_G = 0$ V. The observed breakdown mainly happened at the edge of gate. With floating substrate, the soft V_{BR} at I_{OFF} of 1 A/mm of the recessed tri-gate with L_{GD} of 15 and 20 m were 1650 and 1800 V, respectively. A large hard V_{BR} of 2050 V was measured for the recessed tri-gate with L_{GD} of 20 m (at $I_{OFF} = 9$ A/mm). The gate leakage was 1 nA/mm until 1400 V. A V_{BR} of 960 V at 1 A/mm was observed with grounded substrate, for both recessed and recessed tri-gate, with a high hard breakdown of 1100 V, which was mainly limited by the buffer thickness and quality.

The observed improvement in V_{BR} compared with the recessed devices is mainly due to the integrated FP in the recessed tri-gate. The gate region in the recessed tri-gate device contains two FPs: tri-gate FP (FP_1) from the recess edge to tri-gate drain-side edge, and planar FP (FP_2) from the tri-gate drain-side edge to gate drain-side edge (Fig.3.6 (c-d)). These regions function as two gate-connected FPs, due to their more negative pinch-off voltages compared to the recessed region, of - 2 V in the tri-gate FP and - 4 V in the planar FP [108, 124, 134, 135]. With increasing V_D, the 2DEG under FP_1 and FP_2 are sequentially depleted, reducing the electric field in the recessed gate region and leading to a much enhanced V_{BR} [31, 120]. In addition, despite the lack of passivation in both devices, this additional FP also improved the dynamic R_{ON} of the recessed tri-gate devices by better distributing the electric field under the gate, as supported by [136, 137] (inset of Fig.3.6 (b)). The measured floating breakdown voltage could be affected by virtual gating, which can be resolved by a proper passivation process without sacrificing the breakdown

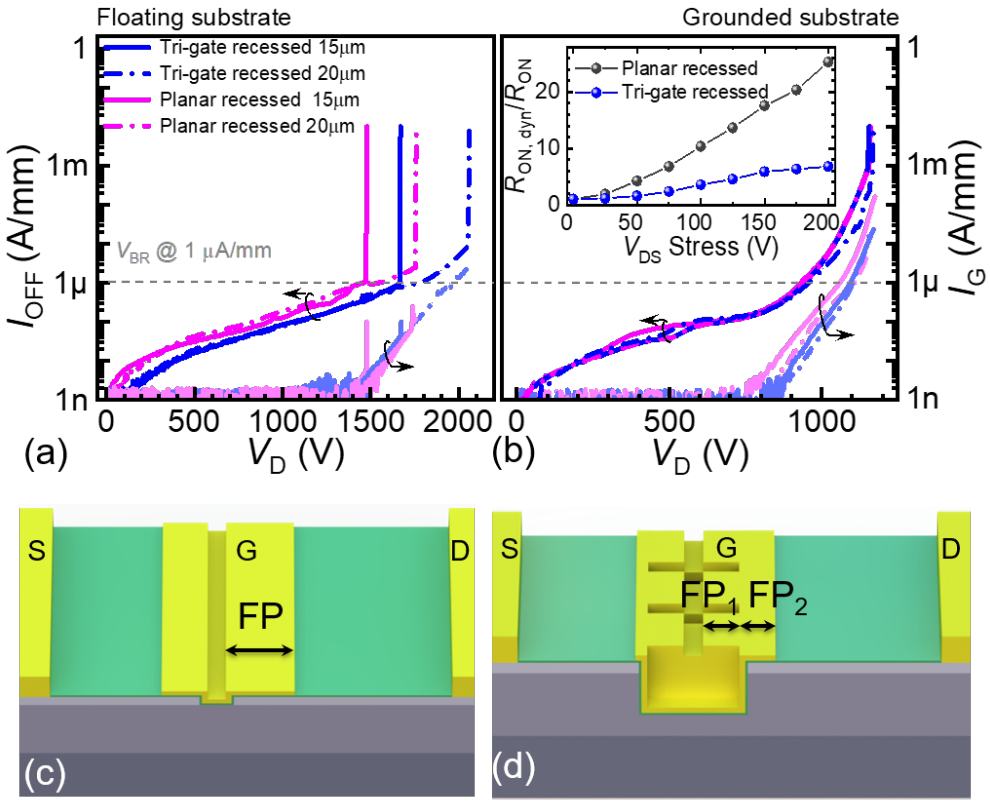


Figure 3.6 – Breakdown characteristics of the recessed (V_G = -1 V) and recessed tri-gate (V_G = 0 V) MOSFETs with L_{GD} = 15 m and 20 m, for (a) grounded and (b) floating substrate. Inset: Dynamic R_{ON} of unpassivated recessed planar and recessed tri-gate transistors measured up to a quiescent bias stress of 200V with a pulse width of 50 s and a period of 5ms. Schematic of (c) planar *FP* and (d) Tri-gate *FP*s.

voltage [32, 142, 143].

The I_D^{max} and R_{ON} versus V_{TH} of the recessed tri-gate devices in this work were benchmarked against E-mode GaN transistors in the literature, demonstrating concurrently high I_D^{max} , low R_{ON} and large V_{TH} of 1.4 V at 1 μA/mm and 1.85 V with linear exploitation (Fig.3.7 (a-b)), with $R_{ON,SP}$ of 1.76 and 2.42 mΩ·cm^2 for L_{GD} of 15 and 20 m, respectively (Fig.3.7 (c)). These results highlight the benefits of combining tri-gate structures and narrow gate recess for high-performance normally-off devices.

3.4 Conclusion

In this Chapter, we have demonstrated state-of-the-art normally-off recessed tri-gate GaN-on-Si MOSFETs by combining tri-gates with a short barrier recess. We have optimized the recess and tri-gate geometry to take full advantage of tri-gate structure. We have also built the mathematical model of trench and tri-gate MOS conduction model to understand the current share of fin

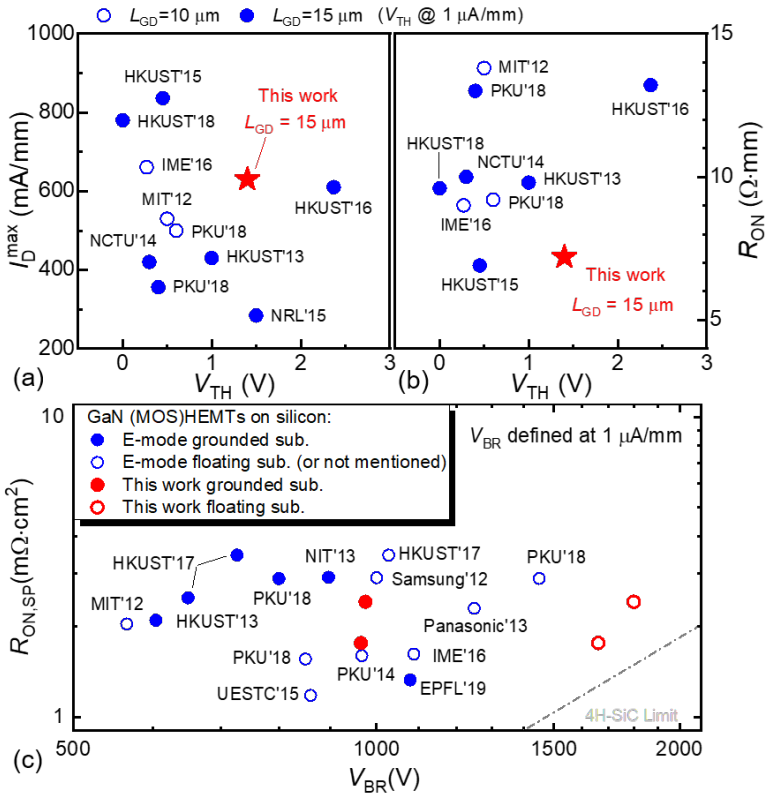


Figure 3.7 – Benchmarking of (a) I_D^{max} and (b) R_{ON} versus V_{TH} (defined at 1 A/mm) of the recessed tri-gate against E-mode GaN-on-Si transistors. For fair comparison, L_{GD} smaller than 10 m were not included (c) $R_{ON,SP}$ versus VBR of the recessed tri-gate against E-mode GaN-on-Si transistors, by defining VBR at IOFF < 1A/mm with floating and grounded substrates. For fair comparison, L_{GD} smaller than 10 m, and literature results with unspecified $R_{ON,SP}$ or IOFF were not included. To calculate $R_{ON,SP}$, a 1.5 m transfer length for each ohmic contact was taken into account.

and trench conduction. Due to trench conduction in the tri-gate region, the devices presented concurrently large positive V_{TH} of 1.9 V (from linear extrapolation), along with high I_D^{max} of 622 ± 16 mA/mm at V_G = 7 V and low R_{ON} of 7.32 ± 0.26 Ω· mm. The excellent channel control from the tri-gate structure enhanced the V_{TH} stability, reduced gate driving voltage and increased the transconductance. These results unveil the excellent prospect of recessed tri-gate for power applications.

4 Normally-off p-GaN MOSHEMTs with tri-gate technology

4.1 Introduction

The most promising approach so far in achieving normally-off operation is the use of p-GaN on the AlGaN barrier [51,71]. This process is receiving a lot of attention in the industry and scientific community, and is also the only "real" normally-off GaN power device currently commercially available. That being said, the p-GaN technology is highly complex and to this day still suffers from several issues such as V_{TH} instability [144, 145] , charge trapping [146] and degradation induced by the positive gate bias and high drain biases in the off-state [147,148]. In this approach, the p-GaN on the AlGaN gives rise to conduction band-bending, which depopulates the 2DEG under the gate[25], and the fast control of the channel conductivity relies on current injected from the p-GaN ohmic or Schottky gate contacts [36]. However, there is a trade-off between positive V_{TH} and low sheet resistance (R_S). On one hand, this is due to the combined effect of the thinner barrier needed for the p-GaN to deplete the channel [3] which increases R_S on the access regions. On the other hand, as shown in this Chapter, it is not possible to fully restore the conductivity of the channel under the p-GaN gate by applying a positive gate bias, which indicates that the p-GaN region is still less conductive than the typical access region, even at high gate bias. Thus, to reduce the on-resistance (R_{ON}) degradation, a shorter p-GaN region and/or a thicker barrier would be desired, which however, makes it difficult to reach normally-off behavior.

Tri-gate structures offer an excellent approach to locally adjust the electron concentration (N_s) by etching fins under the gate. This method enables to reach a positive V_{TH} [12]–[14] while still using thick barriers (20-25 nm) in the access regions, thus conserving a low access resistance in the un-patterned region. Etch-induced damages can still be present, however, they are less sensed due to the thicker barrier that yields a larger N_s. In addition, a significant positive V_{TH} shift can be achieved by adjusting the tri-gate filling factor (FF) and by reducing the tri-gate fin width combined with high work-function gate metals [113].

In this Chapter, we studied two promising novel approaches for achieving high performance normally-off devices to combine p-GaN and tri-gate structures. Firstly, we present a new concept

for normally-off AlGaN/GaN-on-Si MOS-HEMTs based on the combination of p-GaN, tri-gate and MOS structures to achieve high threshold voltage (V_{TH}) and low R_{ON}. In this structure, the p-GaN is used to engineer the band structure to reduce the carrier density in the tri-gate structure for a high V_{TH} , and the efficient field-effect gate control is mainly from the sidewall gates from the tri-gate. Thus the device operation does not rely on injection of gate current. The MOS structure enabled much larger gate voltages and the effective sidewall modulation resulted in excellent switching performance at high switching frequencies. In addition, this concept eliminates the need for thin barriers (typical in p-GaN devices), which combined to the conduction channels formed at the tri-gate sidewalls, resulted in a smaller R_{ON} compared with planar p-GaN structures [100, 101]. Furthermore, we have investigated the p-GaN tri-gate devices by regrowth approaches, which has not been finished in this work. This might be an interesting approach to achieve normally-off behaviors on multichannel devices. These results are from Ref.[100, 101].

4.2 Motivation and Approaches

In this chapter, we will discuss a series of p-GaN devices. In order to avoid confusing, here we will define mainly three type of devices might be discussed in the thesis: p-GaN planar HEMT (p-GaN planar), p-GaN planar MOS-HEMTs (p-GaN MOS Planar), p-GaN tri-gate MOS-HEMTs (p-GaN MOS Tri-gate).

The thickness and Al molar fraction of the Al_xGaN_{1-x} barrier are two important parameters influencing the band diagram of the p-GaN/AlGaN/GaN, and the whole device performance. Traditionally, thin barriers or low Al concentration are used in planar p-GaN transistors to enable normally-off behavior in equilibrium, as the conduction band edge at the AlGaN/GaN interface should lie above the Fermi level. However, it affects the access regions in the same way, increasing the R_S. Moreover, etch-induced damages are much more significant on thin barriers, degrading even further the R_{ON}.

In this section, we focus on the use of p-GaN (75 nm-thick) grown on an $Al_{0.25}GaN$ (20 nm-thick)/GaN epi-structure. Numerical simulations show that the N_S of p-GaN planar device starts rising at -0.5 V (Fig. 4.1 (a)), indicating that the p-GaN on such thick barrier is not enough to result in normally-off behavior. Here, this was addressed by adding a tri-gate structure underneath the gate (Fig. 4.1 (a)), which allows to locally adjust N_S by the tri-gate fin width (Fig. 4.1 (b)), while still using a thick barrier for small access resistance. The combined effect of p-GaN and tri-gate lowers the Fermi level farther from the conduction band, as shown in the simulated band diagram of p-GaN planar and p-GaN tri-gate devices (Fig. 4.1 (c)).

Moreover, we compared the gated-Hall measurements of R_S between p-GaN and planar HEMT structures, which revealed that the channel conductivity under the p-GaN gate is not fully restored even at high V_G (Fig. 4.1 (d)), whereas tri-gate structures cause negligible degradation in R_{ON} [108]. This shows the importance of reducing the p-GaN length to decrease the overall R_{ON}. As

shown in the following section, a reduction of the p-GaN length without affecting V_{TH} is possible in tri-gate structures, but not in planar p-GaN MOS-HEMTs. We also elucidate the mechanism behind the operation of p-GaN MOS Tri-gate for the first time.

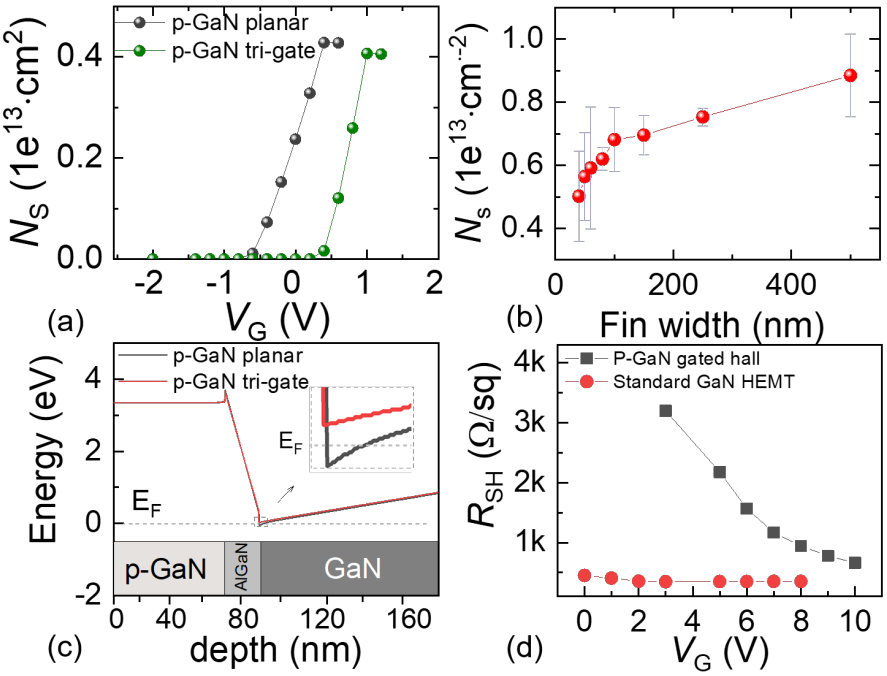


Figure 4.1 – (a) Simulated electron concentration of p-GaN planar and p-GaN tri-gate devices on p-GaN (75 nm)/$Al_{0.25}$GaN (20 nm)/GaN epi-structure, under V_G from -2 to 2 V. (b) Measured electron concentration with different tri-gate fin widths (w) on an AlGaN (20 nm)/GaN structure. (c) Simulated band diagram of p-GaN planar and p-GaN tri-gate devices. (d) Measured sheet resistance by gated hall of a p-GaN and a GaN HEMT structures.

4.3 Top-down approach: Tri-gates on p-GaN/AlGaN/GaN wafer

4.3.1 Device structure

Our top-down approach consists of combining short p-GaN gates with tri-gate structures (Fig. 4.2), based on a pre-grown wafer consisting of p-GaN/AlGaN/GaN layers, which resulted in high V_{TH} and low R_{ON} simultaneously, and presented excellent normally-off performance.

The structure is based on a tiny portion of p-GaN layer (150 nm-long) on top of the tri-gate fins to locally lift the conduction band together with the tri-gate sidewalls, to yield a positive V_{TH}. Fig. 4.2 illustrates the top-view (Fig. 4.2 (a)), 3D (Fig. 4.2 (b)) and, cross-sectional schematics (Fig. 4.2 (c)) of the fabricated p-GaN MOS Tri-gate GaN MOSFETs based on commercial p-GaN/AlGaN/GaN-on-Si wafers.

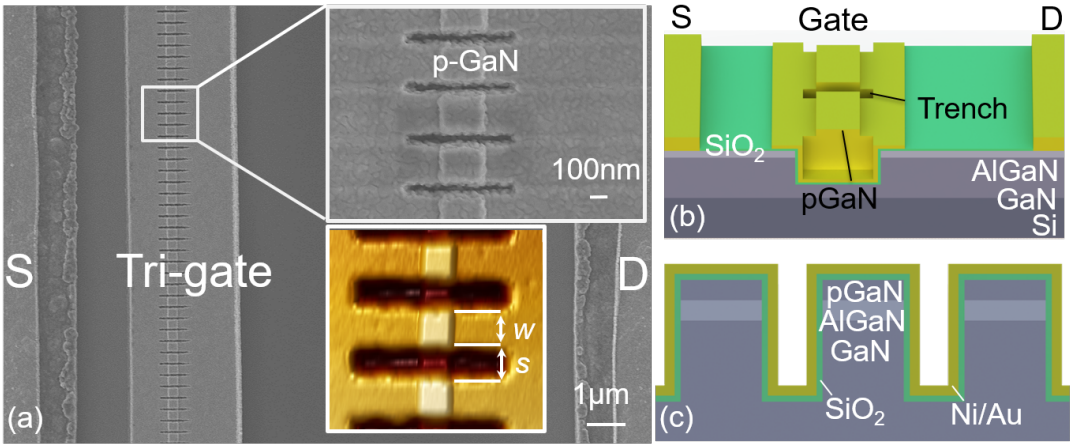


Figure 4.2 – (a) Top-view SEM image of the p-GaN MOS Tri-gate . Inset: Zoomed-in SEM image of p-GaN MOS Tri-gate region and AFM image of p-GaN on top of tri-gate nanowire. (b) Schematic of fabricated p-GaN MOS Tri-gate MOSHEMTs and (c) cross-sectional views of p-GaN MOS Tri-gate region.

4.3.2 Selective p-GaN/AlGaN etching and fabrication

The device fabrication process started with mesa and tri-gate regions defined by e-beam lithography, and followed by Cl_2-based ICP etch. The major challenge for p-GaN gated HEMTs is to obtain uniform p-GaN etching of non-gated active regions and to minimize etching plasma damage [25, 75, 77]. A 200 nm-wide p-GaN (Fig. 4.2 (a)) was protected with e-beam lithography resist, followed by a 75 nm-deep low-damage slow-etch-rate Cl_2/O_2/Ar-based selective ICP etch.

The slow-rate selective etching combined with O_2 plasma/ HCl treatment is a critical process for smothering the etched surface, which minimizes the surface damage and results in low R_{ON}. As we can see from Fig. 4.3 (a), the etching of 75 nm p-GaN took around 58 s while the etching of 20 nm $Al_{0.25}Ga_{0.75}N$ took 542 s, which resulted in a very high selectivity of about 35:1 between p-GaN and $Al_{0.25}Ga_{0.75}N$.The etched surface was then treated with O_2 plasma/HCl, followed by surface annealing at 500 °C to further smoothen the surface and recover the dry etching damages. The surface morphology comparison of etched surface by traditional and selective recipe is shown in Fig. 4.3 (b-c). The traditional ICP ethching poses higher surface roughness and will be potentially caused more problems. However, the seletive recipe will oxidize the Al components in AlGaN and dramatically slow down the etching speed. Thus, the surface of etching is much clearner and smoother (Fig. 4.3 (c)). This is one of the critical step to lower the R_{ON} degradation. As seen from the Tab. 4.1, the traditional recipe had much higher R_C and R_S with big error bar. The selective recipe had much consistent results with R_C and R_S, though there is still partially damage and degradation compared to the reference GaN HEMT without p-GaN growth. As we can see from the Fig. 4.1, they p-GaN covered region could not fully recovered even without etching.

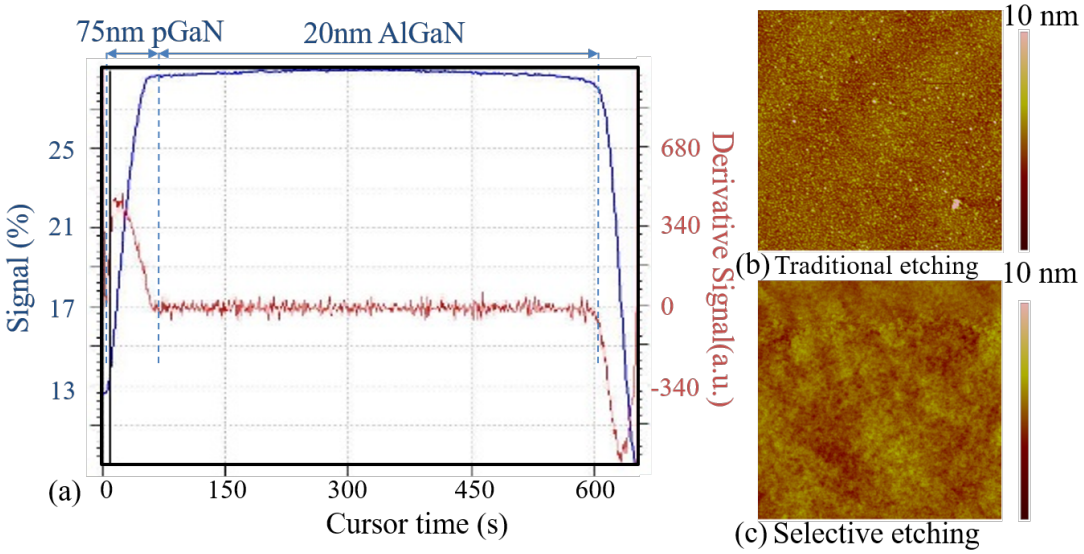


Figure 4.3 – (a) Laser detector of ICP etching. The surface morphology after (b) traditional ICP etching and (c) the selective ICP etching.

Table 4.1 – Comparison of different tranditional etching recipe with selective etching recipe

Recipe	R_C [Ω·mm]	R_S [Ω/sq]	Electron Mobility [cm^2/V·s]
Traditional Recipe	3 ± 1.2	3000 ± 1000	200
Selective Recipe	0.8 ± 0.15	500 ± 40	1200
Ref:GaN HEMT	0.5 ± 0.06	280 ± 15	1500

A metal stack composed of Ti/Al/Ti/Ni/Au was deposited in both source and drain regions, followed by rapid thermal annealing (RTA) at 780 °C under N_2 atmosphere. The 25 nm-thick SiO_2 gate dielectric was deposited by atomic layer deposition (ALD) at 300 °C, immediately after a surface treatment in 37 % HCl for 1 min and 500 °C bake for 5 min. Finally, gate metal was formed by Ni/Au (50 nm / 150 nm).

4.3.3 Device Characterization of p-GaN MOS Planar

In order to understand the effect of p-GaN on GaN transistor, we have firstly fabricated planar p-GaN MOSHEMT transistor. The SEM picture of fabricated p-GaN-gated transistor is shown in Fig. 4.4 (a) and the comparison of the DC transfer characteristics of planar and p-GaN-gated planar devices is shown in Fig. 4.4 (b) and (c). A shift of V_{TH} was observed from - 2.6 V for the planar devices, to - 0.1 V for the 150 nm-long p-GaN-gated planar devices and + 1.3 V for the 1.5 μm-long p-GaN MOS Planar device (V_{TH} was defined at 1 μA/mm) (Fig. 4.4 (b-c)). As the V_{TH} shifted more positively with the increase of the p-GaN length, the current density was reduced dramatically from ~ 400 mA/mm (planar MOSHEMT), ~ 300 mA/mm (150 nm-long p-GaN gate) to ~ 150 mA/mm (1.5 μm-long p-GaN gate). However, while reducing the p-GaN length

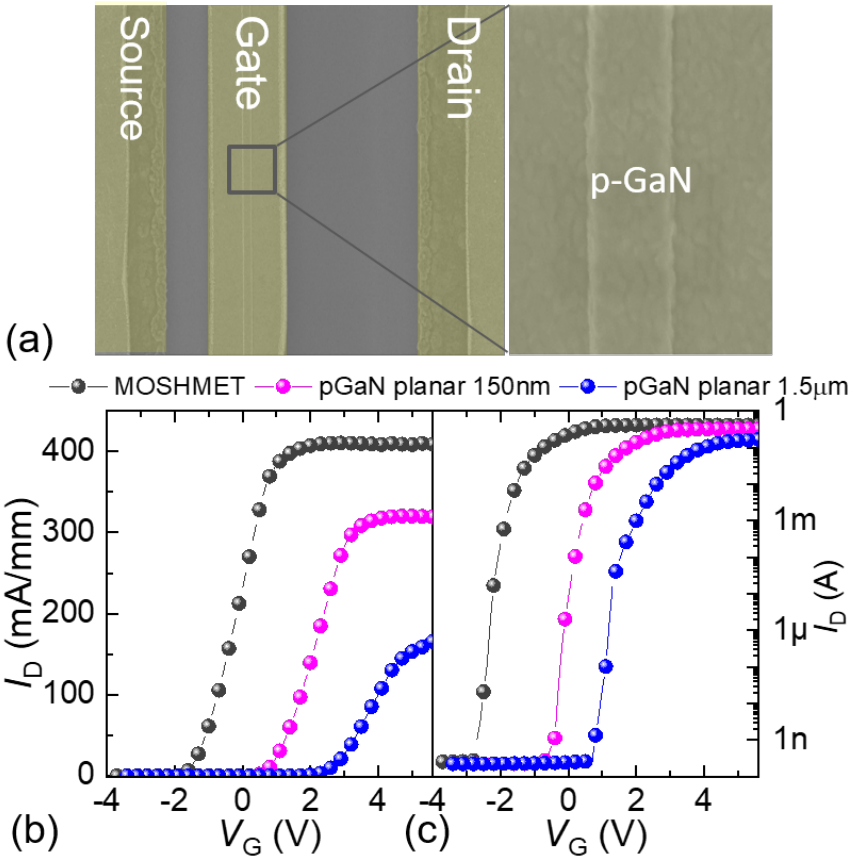


Figure 4.4 – (a) Top view of planar p-GaN transistors. Transfer characteristics of MOSHEMT and p-GaN MOS Planar in (b) Linear and (c) logarithmic scale for V_{DS} = 5 V.

diminishes the current degradation, the V_{TH} is not positive enough to ensure the safe operation of GaN transistor.

4.3.4 p-GaN MOS Tri-gate DC characterization

In this section, we compare the performance of p-GaN MOS Planar MOS-HEMTs and p-GaN MOS Tri-gate MOS-HEMTs to reveal their operation mechanism. A significant positive shift of 1.5 V in V_{TH} (at 1 μA/mm) was observed from the p-GaN MOS Planar to the p-GaN MOS Tri-gate (Fig. 3(a)), with p-GaN length of 200 nm. The larger V_{TH} in the p-GaN MOS Tri-gate is mainly due to the additional strain relaxation of the AlGaN barrier and the sidewall gate modulation [108, 111, 117, 140]. The p-GaN MOS Tri-gate exhibited a larger g_m of 124 ± 18 mS/mm, with an ON/OFF ratio beyond 10^9, an improved sub-threshold slope (SS) of 98 ± 5 mV/dec and lower I_{OFF} at V_G = 0 V, as compared with the p-GaN MOS Planar, revealing an improved tri-gate control over electrons in the channel. The small hysteresis, below 0.1 V and low gate leakage, below 7×10^{-8} A/mm, observed for p-GaN MOS tri-gate device under V_G up to

8 V (Fig. 3 (b)) indicates a good gate-oxide quality. The p-GaN MOS Tri-gate showed a much smaller hysteresis of ~0.17 V (at V_G^{max} of 8 V), which is also smaller than in the p-GaN MOS Planar (0.45 V). This is likely due to the better gate control in the Tri-gate, since both devices had the same gate oxide. Moreover, the V_{TH} histogram from 40 different Tri-gate devices shows a relatively consistent V_{TH} of around 0.89 V at 1 μA/mm. The output characteristics of these devices are shown in Fig. 3 (d). The p-GaN MOS Tri-gate presented a good I_D^{max} of 522 ± 16 mA/mm at V_G = 7 V comparable to the p-GaN MOS Planar (508 ± 18 mA/mm). The high I_D^{max} was due to the combined effect of the short p-GaN and the tri-gate structure. The R_{ON} of the p-GaN MOS Tri-gate and p-GaN MOS Planar, extracted from I_D - V_D sweeps in linear region, were 9.2 ± 0.26 Ω·mm and 9.82 ± 0.29 Ω·mm at V_G = 7 V, respectively.

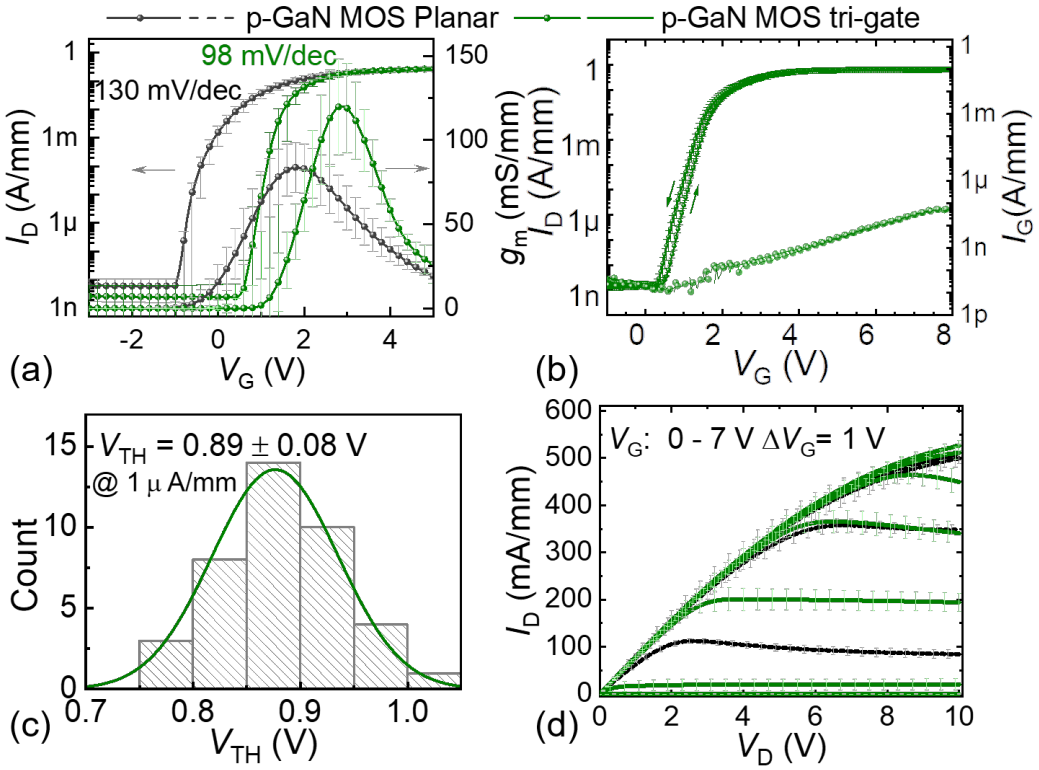


Figure 4.5 – (a) Comparison of transfer characteristics of the p-GaN MOS Tri-gate and the p-GaN MOS Planar device at V_{DS} = 5 V. The p-GaN length was 200 nm. (b) Double-sweep I_D and IG versus V_G for the p-GaN MOS Tri-gate. (c) Histogram of V_{TH} measured from 40 p-GaN MOS Tri-gate devices. (d) Output characteristics of the two types of devices with V_G up to 7 V. The L_{GS}, L_G and L_{GD} were 1, 2.5 and 10 μm, respectively, width was 80 μm and FF was 0.66. Standard deviation bars were determined from the measurement of 10 devices of each type, revealing their consistent performance.

4.3.5 p-GaN MOS tri-gate optimization

We have optimized the tri-gate geometry (Fig. 4.6) in the gate region (p-GaN gate length and FF of tri-gate) to obtain the optimum R_{ON} and V_{TH} simultaneously. As we can see from Fig. 4.6 (a),

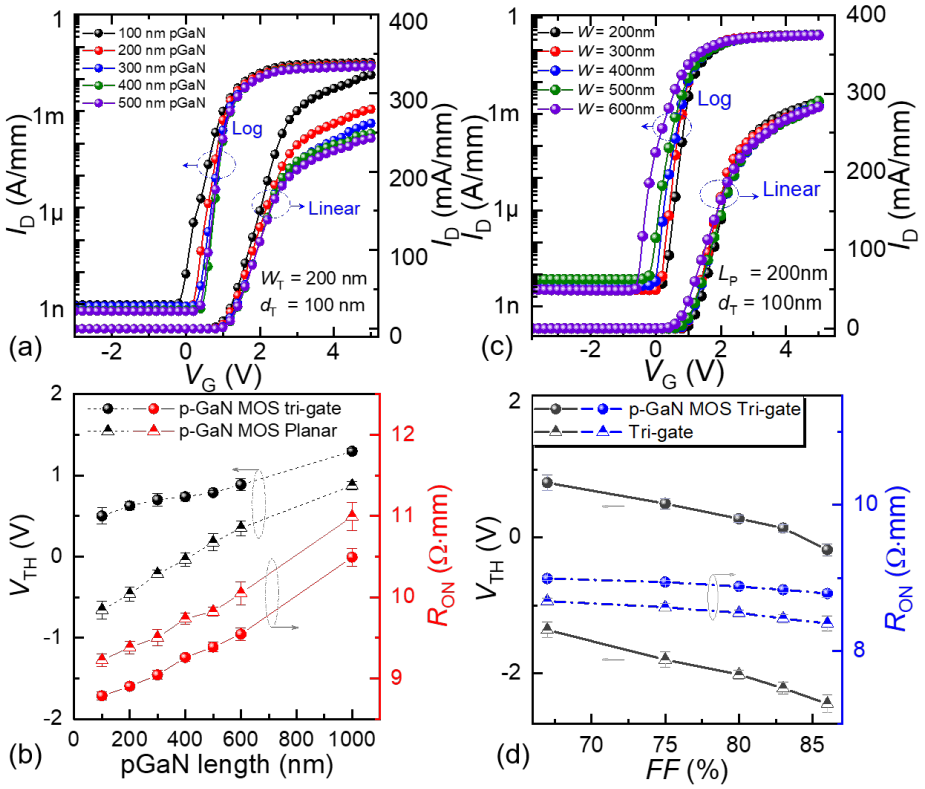


Figure 4.6 – The Log and linear transfer characteristics at V_{DS} = 5 V of normally-off p-GaN MOS Tri-gate with different (a) p-GaN length and (b) Filling factor (FF) of Tri-gate ($w/w+d$). The L_{GS}, L_G and L_{GD} were 1.5, 2 and 15 μm, respectively. Standard deviation bars were determined from the measurement of 6 devices of each type, revealing their consistent performance. (c) The p-GaN length – V_{TH} and R_{ON} dependence of p-GaN MOS Planar and p-GaN MOS Tri-gate devices. (d) FF – V_{TH} and R_{ON} dependence of Tri-gate (Normally-on) and p-GaN MOS Tri-gate (Normally-off) transistors (The p-GaN length is fixed at 200nm).

the p-GaN length did not have a strong effect on V_{TH} for p-GaN lengths over 200 nm. However, the current density dropped significantly with the increase of the p-GaN length. Thus, reducing the p-GaN length is favorable, with length larger than 100 nm (since this device exhibited a low V_{TH} of 0.3 V). Moreover, the tri-gate FF (defined as $w/(w+s)$, as shown in Fig. 4.2, in which the w is the width of nanowires and s is the trench spacing) had a relatively strong effect on V_{TH} and barely degraded the current density (Fig. 4.6 (b)). We have compared the dependence of V_{TH} and R_{ON} on the p-GaN gate length for p-GaN MOS Planar and p-GaN MOS Tri-gate devices (Fig. 4.6 (c)). For p-GaN MOS Planar devices, the V_{TH} shifted from - 0.3 V to 0.4 V with a p-GaN length varying from 100 to 600 nm. On the other hand, for the p-GaN MOS Tri-gate devices the voltage increased from 0.3 to 0.9 V. The slope of V_{TH} versus p-GaN length is much smaller for p-GaN MOS Tri-gate devices compared with p-GaN MOS Planar devices, since the tri-gate structure also contributes to the V_{TH} shift.

However, the V_{TH} difference between these two kinds of devices becomes very small with large

p-GaN length (above 1 μm). The R_{ON} of these two devices is almost linearly dependent on the p-GaN length. We have also compared the V_{TH} and R_{ON} dependence on the tri-gate FF for tri-gate (normally-on) and p-GaN MOS Tri-gate (normally-off) transistors (Fig. 4.6 (d)). The s is fixed at 100 nm and the w was varied from 200 nm to 600 nm, which corresponded to FF varying from 0.66 to 0.87. The p-GaN length is fixed at 200 nm. As the FF increase, the V_{TH} dropped from 0.9 V to -0.2 V for the p-GaN MOS Tri-gate devices, in contrast, the V_{TH} of tri-gate-only devices shifted from -1.3 V to -2.8 V (Fig. 4.6 (d)). When FF is varied from 0.66 to 0.87, the R_{ON} of p-GaN MOS Tri-gate remains almost constant with a reduction of 0.2 Ω·mm, while the reduction of tri-gate R_{ON} was slightly higher up to 0.4 Ω·mm. In summary, the p-GaN length and the tri-gate FF can be tuned to obtain an optimum balance between V_{TH} and R_{ON}.

4.3.6 Tri-gate MOS conduction mechanism

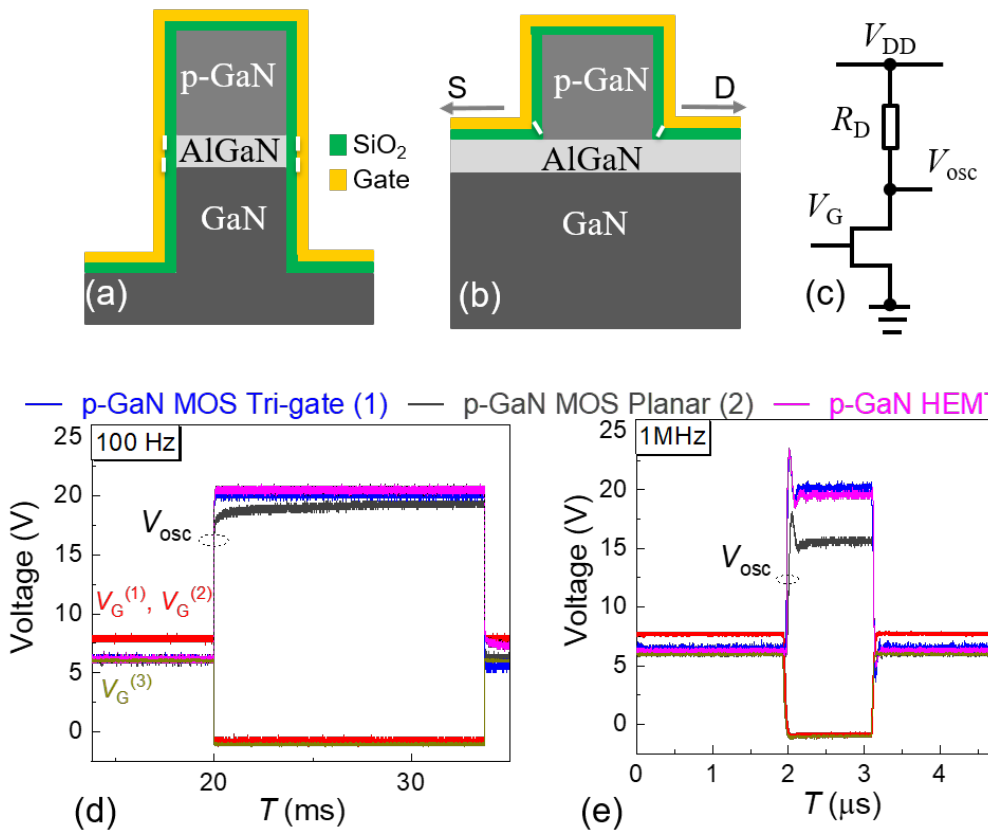


Figure 4.7 – Cross-sectional schematic of (a) p-GaN MOS tri-gate along with tri-gate region and (b) p-GaN MOS planar gate along with Source and Drain. (c) Schematic of experimental setup of p-GaN devices test. Switching waveform of Switching waveforms of the p-GaN MOS Tri-gate, p-GaN MOS Planar, and p-GaN HEMT at (d) 100 Hz and (e) 1 MHz with V_{DD} = 20 V and V_G from -1 V to 8 V for p-GaN MOS Tri-gate and p-GaN MOS Planar, while V_G from -1 V to 6 V for p-GaN HEMT, due to its lower gate voltage capability.

The mechanism of p-GaN conduction is different from traditional p-GaN HEMT. As for the p-GaN HEMT, a 2DEG can only form at the AlGaN/GaN interface if at the same time a 2DHG builds up at the p-GaN/AlGaN interface [36, 55]. The necessary holes for this 2DHG come from the gate metal (Scottky or Ohmic contact) and the fast switching of the device relies on the gate leakage current.If there is a dielectric barrier between the gate metal and the p-GaN layer, the 2DHG cannot build up, and as a result the 2DEG will not form and the transistor remains in the off-state. However, this would lead to large gate loss and low V_G^{max}. In this section, we can demonstrate that the p-GaN MOS Planar could not switching properly, while p-GaN MOS Tri-gate can get rid of this restriction.

The Cross-sectional schematic of p-GaN MOS tri-gate along with tri-gate region was shown in Fig. 4.7 (a) and cross-sectional schematic of p-GaN MOS Planar along with S-D direction was shown in Fig. 4.7 (b). The dynamic performance of p-GaN MOS Planar, p-GaN MOS Tri-gate, and p-GaN HEMT was investigated using the device test setup shown in Fig. 4.7 (c). The V_{DD} is fixed at 20 V for all these devices. V_G was from -1 V to 8 V for p-GaN MOS Tri-gate and p-GaN MOS Planar, while V_G from -1 V to 6 V for p-GaN HEMT due to its lower gate voltage capability. This is already a main novelty of this p-GaN tri-gate MOS structure, since the gate bias can be much larger than in typical p-GaN structures.

At a low frequency of 100 Hz (Fig. 4.7 (d)), it took a few miliseconds for the p-GaN MOS Planar to be completely turned off, while the p-GaN MOS Tri-gate and p-GaN HEMT turned-off instantaneously. This phenomenon can be seen more clearly at higher frequency of 1 MHz (Fig. 4.7 (e)). The p-GaN MOS Tri-gate and p-GaN HEMTs can be turned on/off within a few nanoseconds, while the p-GaN MOS Planar could not fully turn off at such frequencies. This shows the effective and fast sidewall gate control of p-GaN MOS Tri-gate, which is more dominant than the top gate control compared with traditional GaN HEMTs. For the p-GaN MOS planar device, the gate control is mainly through fringing capacitances from the surface to the 2DEG, which is less effective compared with tri-gate sidewall control. This indicates the superior side gate control of using tri-gate structures which forms a new mechanism of p-GaN MOS conduction.

4.3.7 Improved breakdown voltage

The comparison of breakdown characteristics between the p-GaN MOS Planar and p-GaN MOS Tri-gate is shown in Fig. 4.8. The V_{BR} of p-GaN MOS Tri-gate was extracted for V_G of 0 V with grounded substrate at 1 μA/mm (Fig. 4.8 (a)), resulting in 520 V and 980 V for L_{GD} of 5 μm and 10 μm, respectively, compared to 380 V and 750V, for p-GaN MOS planar devices (at V_G = -1 V). The observed improvement in V_{BR} compared with the p-GaN MOS Planar is due to the effective integrated field plates (FP) in the p-GaN tri-gate region [26, 108]. The p-GaN MOS Tri-gate presented lower R_{ON} for the same L_{GD} compared with p-GaN MOS Planar devices (Fig. 4.8 (b)). The low R_{ON}, larger V_{TH} and V_{BR}, together with the effective gate control reveal the significant potential of the p-GaN tri-gate MOS technology for high-performance E-mode GaN devices.

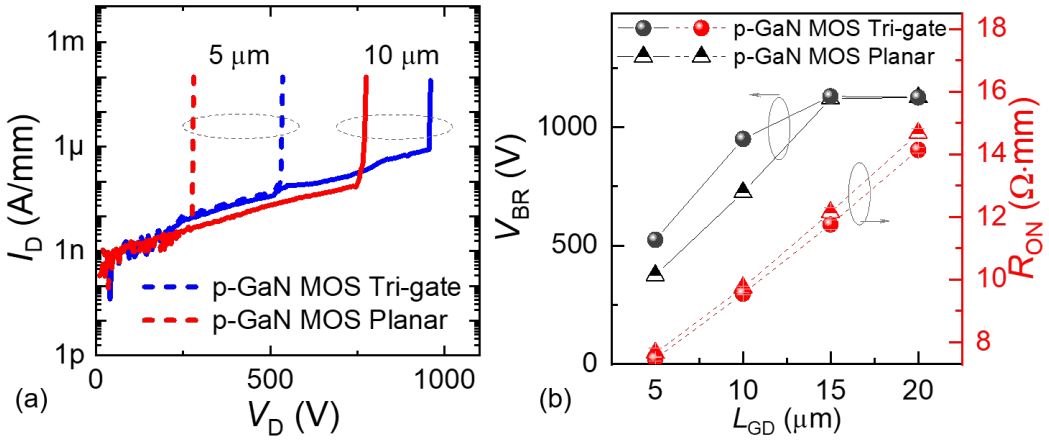


Figure 4.8 – (a) Breakdown Characteristics of the p-GaN MOS Tri-gate (at V_G = 0 V) and p-GaN MOS Planar (at V_G = -1 V) with different L_{GD} with grounded substrate. (b) Extracted V_{BR} and R_{ON} dependence on L_{GD} of p-GaN MOS Planar and p-GaN MOS Tri-gate. The V_{BR} was defined at IOFF 1 μA/mm.

4.4 Bottom-up approach: growth of p-GaN layers over tri-gates

4.4.1 Introduction

In this approach, normally-off operation is attempted by fabricating tri-gate structures in AlGaN/GaN heterostructures (Fig. 4.9 (a)) with subsequent growth of p-type GaN (red regions in Fig. 4.9 (b-c) on top and the sidewalls of the trenches (Bottom-up approach). In contrast to the Top-down approach described in the previous section, the p-GaN covers in this case not only the surface of the AlGaN/GaN but also the sidewalls allowing for even better charge control and larger V_{TH} shift for normally-off operation. The device fabrication process is similar to the devices described in the previous section. The main difference lies in the hard mask design for the regrowth of the p-GaN over the full tri-gate device width filling all the trenches (Fig. 4.9 (b)). The process could be potentially used for multi-channel normally-off GaN devices gate control.

For a selective regrowth, the device surface is covered with a hard mask, with only small controlled openings allowing the growth of p-GaN in the trenches of the tri-gates (Fig. 4.9(c)). The main challenges to this approach are selective growth under appropriate growth conditions and good electrical contact of the p-GaN layers to the tri-gate structure.

4.4.2 Regrowth Process

The p-GaN layer is deposited over the tri-gate structures in an additional epitaxial step performed by metalorganic vapor-phase epitaxy (MOVPE). In the following study, a horizontal Aixtron 200/4 RF-S reactor was used with NH_3 and TMGa (Trimethylgallium) as precursors for the growth of GaN. The p-type doping was done by incorporation of Mg using Cp_2Mg as the

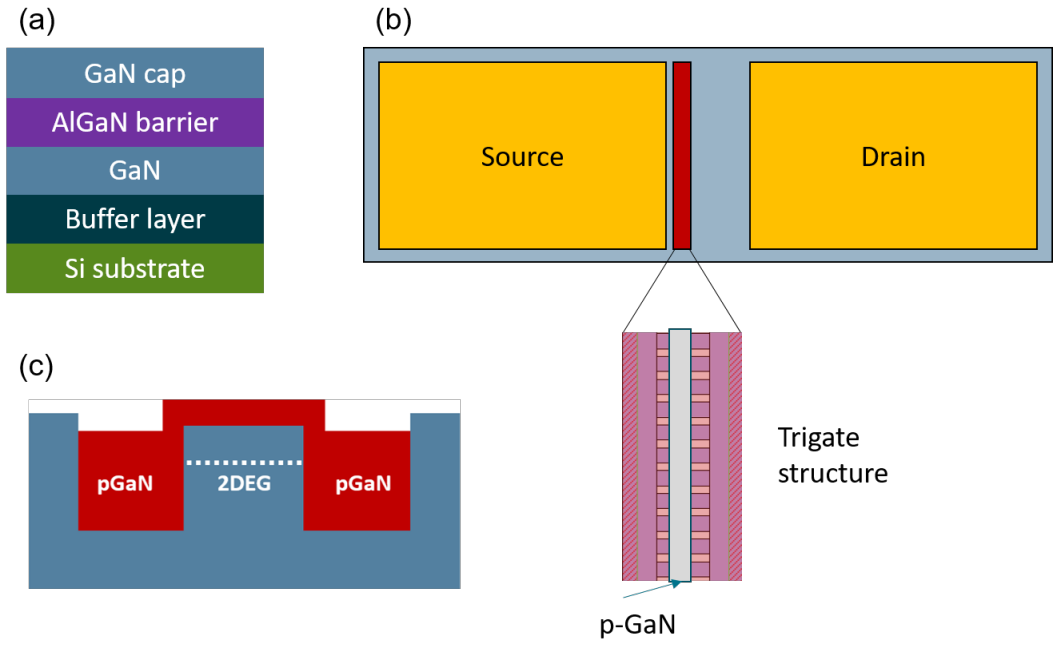


Figure 4.9 – Illustration of (a) epitaxial heterostructure (b) Top view device geometry and (c) Cross-section of tri-gate trench regrowth with p-GaN.

precursor. Prior to the regrowth a surface treatment was performed by cleaning the samples with a hot Piranha solution (3:1, H_2SO_4:H_2O_2) for 15 minutes. This initial cleaning process has been shown to be crucial in achieving a regrowth surface free of organic contamination.

After the sample is loaded into the reactor a second cleaning procedure is performed at high temperature (> 1000 °C) under H_2 for several minutes (1 - 3 min) in order to remove any remaining residues from the growth surface. The p-GaN layer is grown at a surface temperature of 1000 to 1050 °C. The thickness is generally chosen to be between 70 and 200 nm with a growth rate of approximately 500 nm/h. Prior to the actual growth a Mg pre-flow is introduced in order to have sufficient p-type doping at the crucial lower interface. Furthermore, the final several 10 nm of the growth are performed under over-doping conditions in order to insure an unhindered Mg activation process. After regrowth the hard mask is removed by HF. The p-GaN is activated by a rapid thermal annealing step at 850 °C under O_2 for 20 minutes. Finally, the surface morphology and the electronic properties are investigated by scanning electron microscopy (SEM) and standard metal deposition techniques, respectively. In the following two sections the main challenges of the regrowth process are discussed in more detail.

4.4.3 Challenges: Growth issues due to hard-mask residues

One of the initial issues faced during the regrowth process was the discontinuous growth along the device width which can be seen in Fig. 4.10 (a) Bottom. Furthermore, small pits were visible

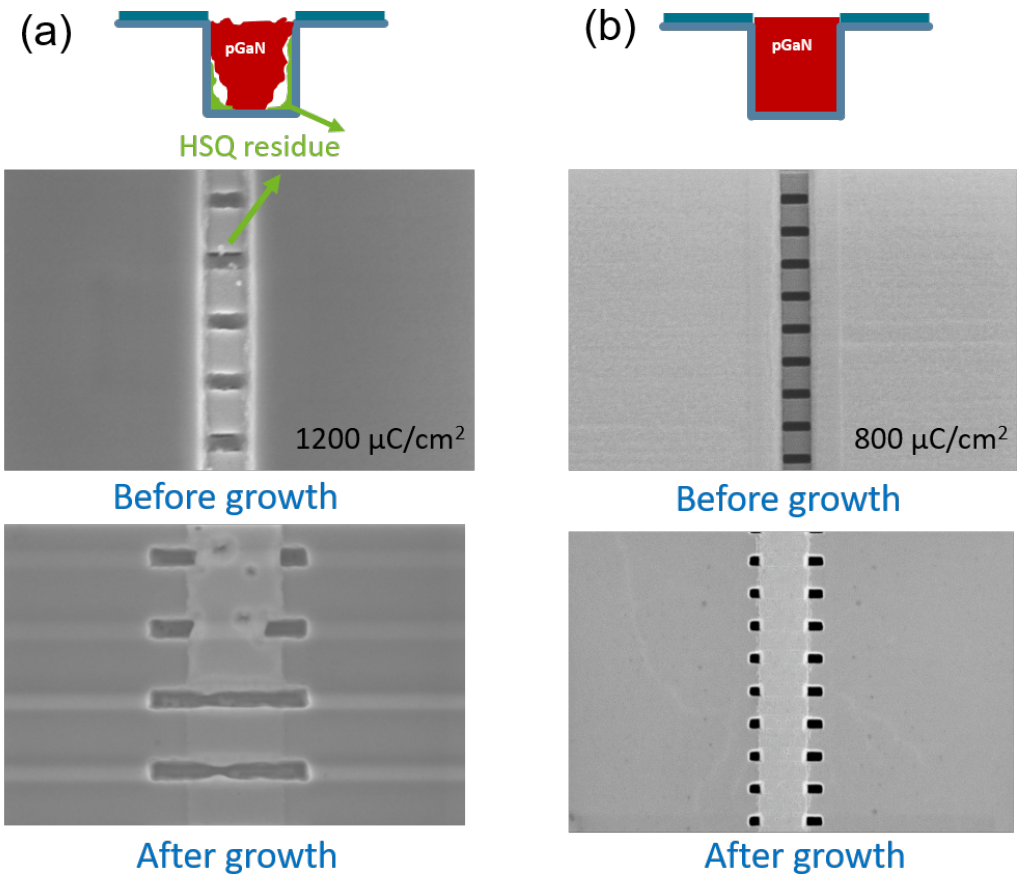


Figure 4.10 – Illustration and SEM images of tri-gate trenches before and after regrowth of p-type GaN for an e-beam exposure dose of (a) 1200 and (b) 800 μC/cm^2 (p-GaN length: 400 nm).

on the regrown surface indicating a possible issue at the growth interface. As can be seen in the SEM image in Fig. 4.10 (a) Top, hard mask residues remain on the surface and within the trenches after development. This is most likely due to strong electron scattering during the exposure of the mask. It has been demonstrated in the past, that even a single monolayer of a hard mask such as SiO_2 or metals can prevent high quality epitaxial regrowth of III-V semiconductors.

Several cleaning treatments were applied to the samples prior to the regrowth in order to remove the hard mask residues. In particular, cleaning by HF, BHF (5 s to 15 s treatment) and inductively coupled plasma (ICP) etching showed promising results in reducing the residues and avoiding discontinuities and pits of the regrown p-GaN layers. However, these surface treatments have several side effects. Chemical cleaning with HF and BHF can potentially damage the hard mask. Furthermore, ICP etching is known to damage the semiconductor surface and thus lead to poor transport properties of the device. Hence, avoiding these residues in the first place seems to be the most efficient option.

In order to eliminate the hard mask residues, the dose of the exposure was lowered from 1200 to

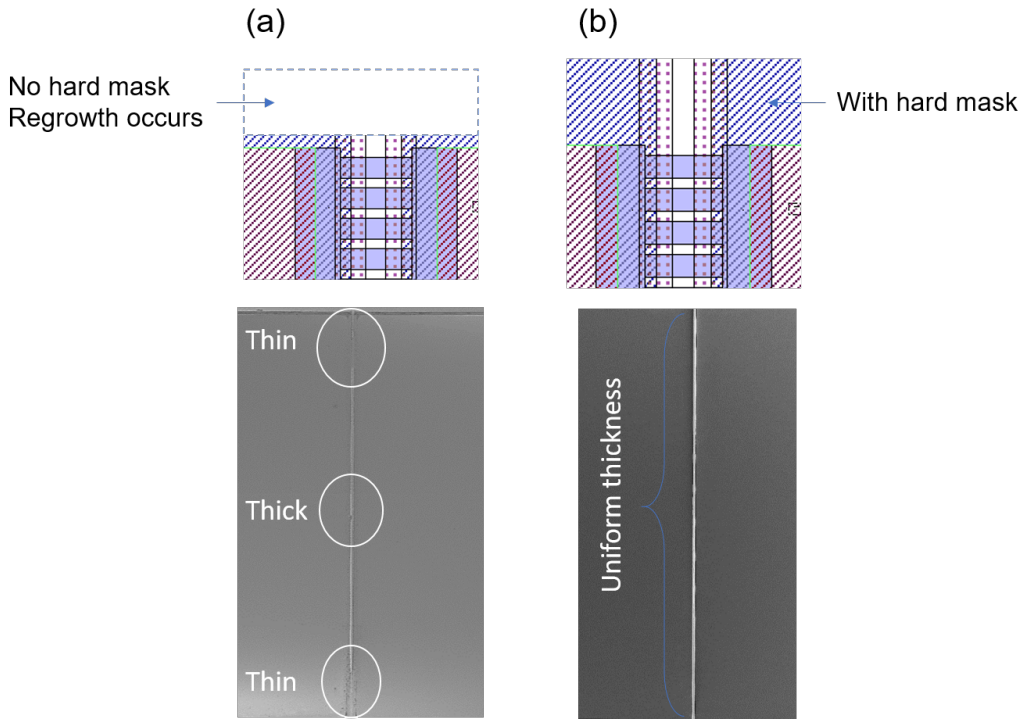


Figure 4.11 – Illustration of hard mask layout and SEM images for (a) narrow and (b) wide mask widths at the tri-gate edges.

800 μC/cm^2. The resulting hard mask and regrowth surface are shown in Fig. 4.10 (b). The lower dose clearly reduces the electron scattering, giving rise to sufficiently less hard mask residues and sharper edges. Furthermore, the regrowth was continuous along the full device width with no visible pits on the surface.

4.4.4 Challenges: Thickness inhomogeneity

The hard mask layout is defined in such a way that selective regrowth occurs within the trenches, while preventing deposition on the remaining parts of the device. However, areas between devices allow for growth since there is no hard mask present. In this case the growth rate strongly depends on the distance between the adatoms coming from the precursors and the trenches. For adatoms close to the edges of the device, there is sufficient area for epitaxial growth outside the trenches. In the center of the devices on the other hand the only area for the deposition of the adatoms is in the tri-gate trenches. Therefore, the effective growth rate at the edges of the device is lower than within the device. This can be clearly seen in Fig. 4.11 (a) where for the initial hard mask the deposited p-GaN layer is thicker in the center of the device than at the edges .

From a device perspective this thickness inhomogeneity can prevent fully turning off the device, due to leakage current in the thin regions. In order to have a homogeneous growth rate and thus thickness of p-GaN across the device, the hard mask was extended at the edges, which

prevents the reduction of the growth rate. The resulting regrowth shown in Fig. 4.11 (b) shows a homogeneous and continuous regrowth across the full device width.

4.5 Conclusion

In this chapter, we propose a new concept for normally-off AlGaN/GaN-on-Si MOS-HEMTs based on the combination of p-GaN, tri-gate and MOS structures to achieve high V_{TH} and low R_{ON}. The p-GaN is used to engineer the band structure and reduce the carrier density (N_s) in the tri-gate structure for a high V_{TH}. The gate control is mainly achieved from field-effect though the tri-gate sidewalls, and does not rely on injection of gate current. The MOS structure enables much larger gate voltages (V_G) and the effective sidewall modulation results in excellent switching performance at high switching frequencies. In addition, this concept eliminates the need for thin barriers (typical in p-GaN devices), which combined to the conduction channels formed at the tri-gate sidewalls, resulted in a smaller R_{ON} compared with planar p-GaN structures. We have also investigate the regrowth tri-gate process, which would be promising for the future development of this technology.

5 GaN-based logics and driving circuits

5.1 Introduction

Increasing the switching frequency of power converters will lead to a significant reduction of the size of passive components, such as capacitors and inductors, and thus of the overall system, enhancing its power density [3,6]. GaN is one of the most promising materials for high frequency power switching due to its exceptional properties such as large saturation velocity, high carrier mobility, and high breakdown field strength. Despite the advantages of GaN power devices, discrete Si-based logic control and gate drivers still have to be used to control the GaN power devices [82]. The external connections introduce parasitic inductances and capacitances, which hinders their high-frequency switching capability.

A monolithic integration of GaN power devices with GaN-based gate drivers would minimize parasitic components and unveil the full potential of GaN transistors for high frequency power conversion with high efficiency. Such monolithic integration requires GaN-based logic circuits, since they are essential components to realize level shift, driver control, dead time control and under voltage-lockout (UVLO) for driver circuits. However, CMOS logic in GaN is not feasible today due to the poor performance of p-type GaN devices [83, 84] . Ideas to demonstrate purely n-type logic circuits date back of more than 30 years with NMOS logics [149–151], also named direct-coupled FET logic (DCFL). GaN DCFLs have been demonstrated [82, 85, 88, 89], however their performances are not sufficient to satisfy the logic requirements, due to their small noise margins, large logic transition voltages, small logic swing and large low-level output voltages (V_{OL}). Recent research show steady improvements on GaN DCFL, however the V_{OL} is still quite high, up to 0.3 V and the maximum voltage swing is 4.66 V, which would lead to high logic losses and safety problems.

A very distinct property of GaN compared to Silicon is its high temperature operation, which led to the demonstration of GaN DCFLs operating at high temperatures, up to 375 °C, however, it resulted in a much degraded operation compared to room temperature (RT). Moreover, most of the research in the literature today is focused on inverters and no papers mention other logic

gates such as NAND or NOR, which are essential for realizing gate drive control.

In this Chapter, we demonstrates high-performance NOT, NAND and NOR logic gate units with a monolithic integration of E/D-mode MOSHEMTs with planar structure and tri-gate structure. These logic units were optimized for larger voltage swing, wider noise margin, and smaller transition periods. Such high performance was observed even up to 300°C [85, 88], which could be applied for high temperature applications. Finally, we demonstrate of the usage of logic gate in the integrated circuits, which could be potentially for the future fully monolithically integration of GaN transistors.

5.2 CMOS or NMOS GaN logic circuits

5.2.1 Ideal logic switch and typical logic switch

The voltage transfer characteristic(VTC) provides the relationship between the input voltage (V_{IN}) and the output voltage (V_{IN}). Fig. 5.1 (a) is the voltage transfer characteristics of the ideal logic inverter circuit. The high-level output voltage (V_{OH}) is equal to DC power supply voltage (V_{DD}). The low-level input voltage (V_{IL}) and high-level input voltage (V_{IH}) are equal to half of V_{DD} in ideal case. The transition from low to high and vice versa is very sharp at V_{IN}=V_{DD}/2. In

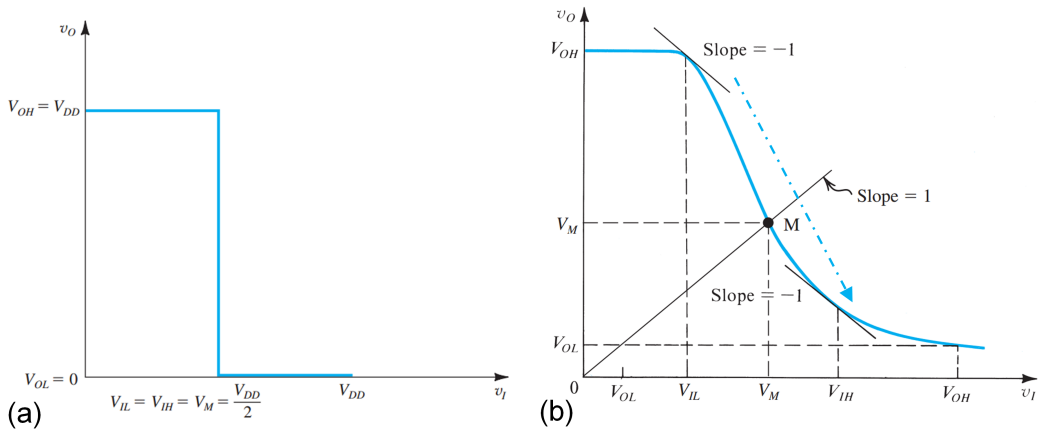


Figure 5.1 – Voltage transfer characteristics of logic gate of (a) ideal inverter logic circuit and (b) practical inverter logic gate circuits [152]

reality, the logic gate would not be turned-on/off instantaneously (Fig. 5.1 (b)). Typically, it goes through a transition region from the high state to the low state. The VTC of a typical inverter Fig. 5.1 (b) has three distinct regions: the low-input region, where $V_{IN} < V_{IL}$; the transition regions, where $V_{IL} \leq V_{IN} \leq V_{IH}$; and the high input regions, where $V_{IN} > V_{IH}$. The V_{IL} and V_{IH} are defined as the points at which the slope of the VTC is -1 (dV_{out}/dV_{in}=-1). The width of the transition voltage region (V_{TR}= V_{IH} - V_{IL}) is a way of measure the ambiguity of the logic inverter [153], which must be as low as possible. Noise generally is present in logic circuits, superimposed on input signals. Noise simply refers to extraneous signals, which may arise from

inadequate regulation or decoupling of the power supply, electromagnetic radiation, inductive or capacitive coupling from other parts of the system, or line drops [153]. One of the advantages of logic circuits is their tolerance for variations in the input signal, which results from the fact that the input signal is interpreted simply as high or low. Noise immunity is a measure of the tolerance for variations in the signal level, and it is that voltage that, applied to the input, will cause the output to change its state. Thus, noise immunity is an important device characteristic. The low-input-logic noise margin N_{ML} is defined as NM_L=V_{IL} - V_{IL} and high-input-logic noise margin (NM_H) is defined as NM_H=V_{IH} - V_{OH}, which would be preferred as high as possible.

5.2.2 CMOS GaN logic gates

There were some studies regarding to GaN CMOS [83, 84]. Fig. 5.2 (a) is a typical schematic of CMOS circuit, which includes a PMOS and NMOS GaN. The typical NMOS GaN exhibited a channel electron mobility of 1300 - 2000 cm^2/V·s Fig. 5.2 (b), however, the PMOS exhibited a channel hole mobility of up to 20 cm^2/V·s [83, 84], which is similar to the reported value of typical bulk mobility of 10 cm^2/V·s in P-type GaN [154]. This would lead to high size mismatch of PMOS and NMOS devices Fig. 5.2 (c) [84]. The noise margin of the device is very low, the V_{OH} is small, as well as the V_{OL} is very high, which is impossible to be used as logic gate.

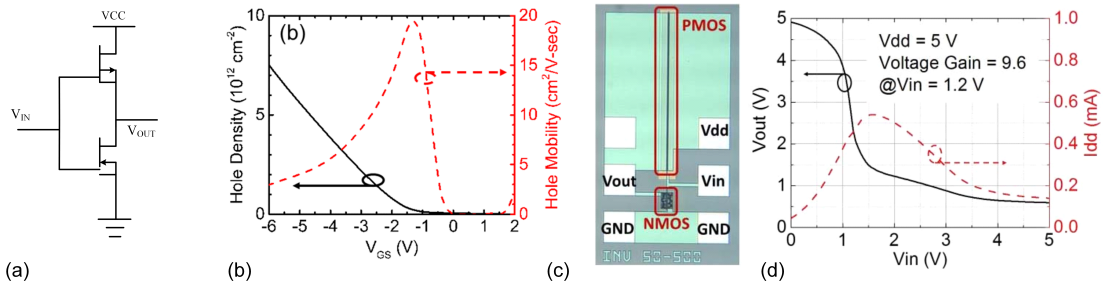


Figure 5.2 – (a) Schematic of CMOS logics circuit. (b) Channel carrier density and mobility of a PMOS extracted from DC-IV and VC meansurement of FAT-FET structures.(c) Microscopy top view photograph and (d) measured voltage transfer curve of a fabricated GaN CMOS inverter IC. The NMOS and PMOS have a gate width of 50 μm and 500 μm, respectively. [84]

5.2.3 GaN based NMOS logic

There were a few typical GaN based NMOS logic circuits, which are NMOS logic ciruits with resister load, enhancement transistor load and depletion transistor load (Fig. 5.3 (a-c)). They had same lower side E-mode transistors, and the only difference is the upside load. The Fig. 5.3 (a) showed the basic working principle of load logic gate. If $V_{IN} > V_{TH}^E$ (Threshold voltage of lower E-mode transistors), the transistor is on and the V_{OUT} will be low logic signal close to 0 V. If $V_{IN} < V_{TH}^E$, the lower E-mode transistor is off and the V_{OUT} will be close to V_{CC}. The simulation of the VTC of these devices were shown in Fig. 5.3 (d) with comparative design. The E-mode load and resistive load had a very slow trasition and also the V_{OL} is relatively high. The E-mode load

would not have the same high level of V_{OH} due to the turn on of the upside transistors. Thus, the most suitable NMOS logic gate is the transistors with depletion load, also named the DCFL.

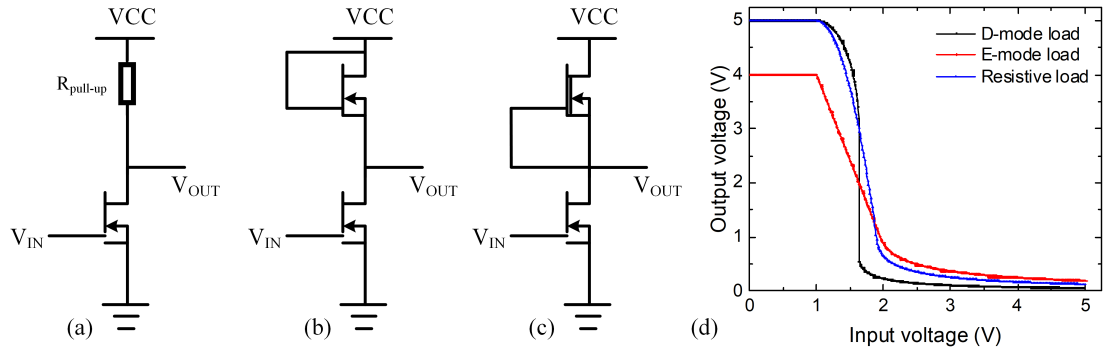


Figure 5.3 – GaN NMOS inverter with (a) resister load (b) enhancement load (c) depletion load. (d) Simulated VTC of GaN NMOS inverters.

5.3 E-/D-Mode MOSHEMTs based GaN NMOS digital logic gate circuit

5.3.1 Integrated logic design and fabrication

The NMOS logic gate circuits, shown in Fig. 5.4 (a), were fabricated on AlGaN/GaN epitaxial layer on silicon substrate (Fig. 5.4 (b)) consisting of 3.75 μm buffer, 322 nm of un-doped GaN channel, 23.7 nm of AlGaN barrier and 2.4 nm of GaN cap layer. D-mode and E-mode MOSHEMTs were fabricated at the same time, with the sole difference of one additional gate recess process to achieve E-mode operation. The Fig. 5.4 (c) is the top views of the fabricated monolithic integration of E/D-mode MOSHEMTs. To optimize the design of the logics, we simulated the driver-to-load resistance ratio $\alpha = \frac{(W/L)_E}{(W/L)_D}$, as shown in Fig. 5.4 (d), where W and L are the width and length of the E- and D-mode transistors respectively. Larger values of α result in sharper transitions, higher logic voltage swings and higher noise margins, since the equivalent resistance of E-mode transistor is much smaller than the overall resistance of the circuit. To achieve large values of α, we designed a multi-finger structure for the E-mode MOSHEMT that results in a much smaller resistance of the E-mode compared to the D-mode device without oversizing too much the E-mode transistor (Fig. 5.4 (c)).

The chip fabrication started with the definition of the mesa regions by Cl_2-based inductively coupled plasma (ICP) etching. For the E-mode devices, a 1.5 μm-long gate recess (the gate length was limited by optical lithography) was defined by optical lithography and followed by a Cl_2-based slow-rate dry etching, which leads to a precise control of the etching depth. To improve the surface morphology after gate recess, therefore the electron transport of the e-mode devices, we have combined a slow, low-damage ICP etch with a 5%-TMAH wet treatment performed at 80 °C for 30 minutes (Fig. 5.5). This step is very critical to obtain a good V_{TH}

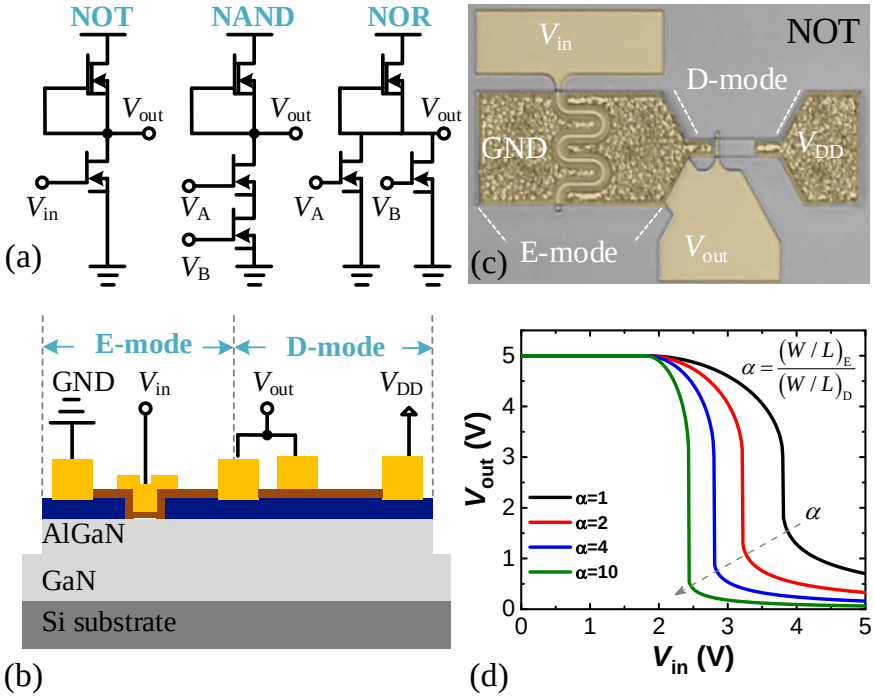


Figure 5.4 – (a) Equivalent circuits of inverter, NAND and NOR logic gates. (b) Cross-sectional schematic and (c) top view of monolithic integration of E/D-mode MOSHEMTs. (d) Simulated transfer characteristics versus different α ratios.

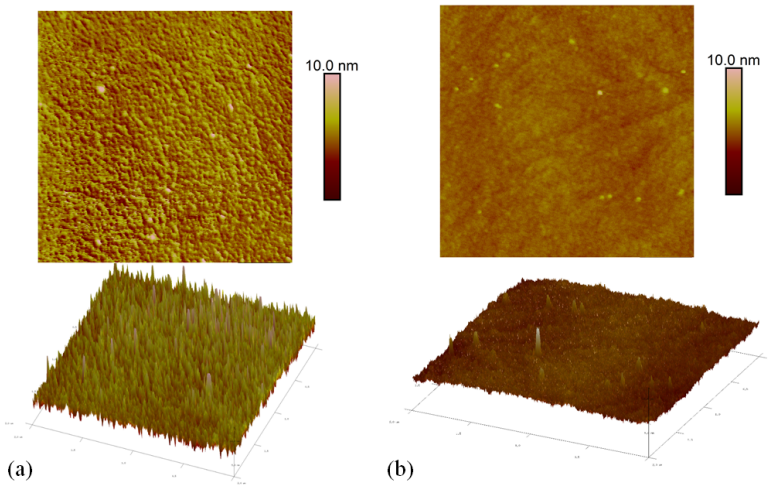


Figure 5.5 – Surface morphology (a) before and (b) after TMAH treatment.

control and reasonable R_{ON} of E-mode transistor. A metal stack of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/ Ni (60 nm)/ Au (50 nm) was deposited in the source and drain contact regions by electron-beam evaporation, followed by rapid thermal annealing at 830 °C under N_2 atmosphere. The gate dielectric was 25 nm-thick SiO_2 deposited by atomic layer deposition (ALD) at 300 °C, immediately after a surface treatment in 37% HCl for 1 min. Finally, gate and contact pads were

formed by depositing Ni/Au for both E-mode and D-mode devices.

5.3.2 DCFL inverter

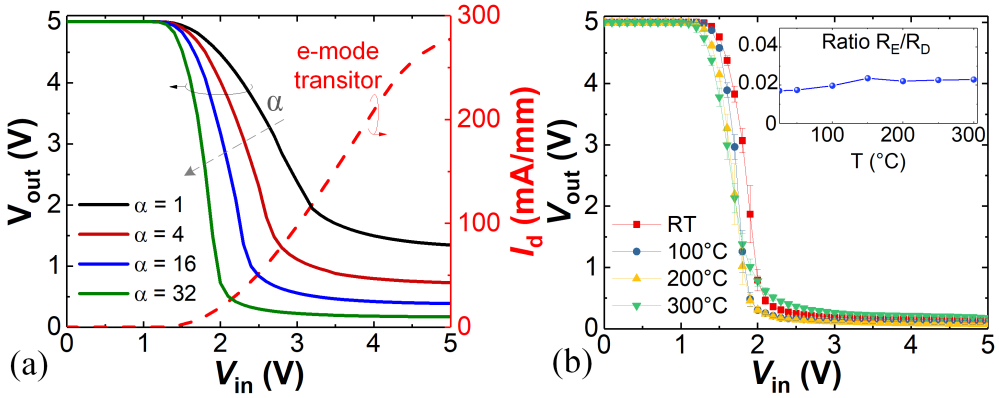


Figure 5.6 – (a) DCFL VTC versus different α ratio and the transfer characteristics of E-mode transistors (b) DCFL VTC under different temperature varied from RT to 300 °C. Inset: resistance ratio of E/D-mode logic versus temperature for output logic equal to 0.

Fig. 5.6 (a) shows the measured VTC for DCFL inverters with different α, which is consistent with the simulations shown in Fig. 5.4 (c). The performance of the DCFL inverters was characterized with a V_{DD} of 5 V from RT to 300 °C revealing a proper operation with very little variations for this entire temperature range (Fig. 5.6 (b)). The transition voltage was slightly decreased as the temperature went higher, presenting a much sharper behavior at higher temperature. The V_{OL} was nearly unchanged, since the resistance of the E- and D-mode transistors increases at the same rate with temperature (inset of Fig. 5.6 (b)), which results in a nearly constant E/D-mode resistance ratio and thus in a similar V_{OL} since:

$$V_{OL} = \frac{R_E}{R_E + R_D} V_{DD} \tag{5.1}$$

As shown in Fig. 5.6 (a), the transition voltage of the DCFL inverter is affected by two main factors: the V_{TH} of the E-mode transistor and the ratio α. For high performance logics, the ratio α must be as large as possible and the V_{TH} of E-mode transistor must be close to $V_{DD}/2$ = 2.5 V in linear scale, which can be controlled by adjusting the gate recess depth.

We optimized the design of the DCFL inverter by integrating a D-mode MOSHEMT with $(W/L)_E$ = 160 μm / 8 μm acting as the active load and an E-mode MOSHEMT with a $(W/L)_E$ = 10 μm / 32μm acting as the driver source, which corresponds to a ratio α of 64. By adjusting the gate recess from 25 nm to 27 nm, the V_{TH} of the E-mode transistor was increased from 1.8 V (Fig. 5.6 (a)) to 2.5 V in linear scale. The VTCs of the optimized DCFL inverter are shown in Fig. 5.7.

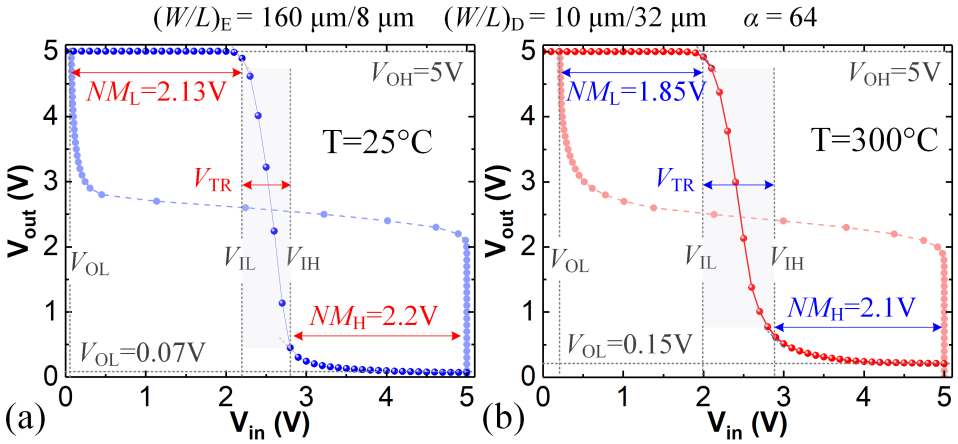


Figure 5.7 – The VTC of the optimized DCFL inverter with α = 64 at (a) 25°C and (b) 300°C with supply voltage V_{DD}=5V.

The high-level output voltage (V_{OH}) and V_{OL} were 5 V and 0.07 V, respectively, yielding a much larger voltage swing of 4.93 V/5 V (98.6%) compared to the best values in the literature of 4.66 V / 5 V (93.2%) [89] and 6.3 V / 7 V (90%) [88]. The low-level input voltage (V_{IL}) and high-level input voltage (V_{IH}), defined at dV_{out}/dV_{in} = -1, were 2.2 V and 2.8 V respectively. The VTC consist of three main regions: the low-input region at v_{in}<V_{IL}, the transition region at $V_{IL} \leq v_{in} \leq V_{IH}$, and the high-input region at v_{in}>V_{IH}. The width of the transition voltage region (V_{TR}= V_{IH} - V_{IL}) is a way of measure the ambiguity of the logic inverter [153], which must be as low as possible. The transition voltage width was 0.6 V / 5 V (12%) in our case, which is smaller than the lowest values in the literature 1 V / 5 V (20%) [89] and 1.6 V / 7 V (22%) [88]. The low-input-logic noise margin (NM_L=V_{IL} - V_{OL}) and high-input-logic noise margin (NM_H=V_{IH} - V_{OH}) are 2.13 V / 2.5V (85.2%) and 2.2 V / 2.5 V (88%) respectively, which outperforms the best values of 1.7 V / 2.5 V (68%) and 2 V / 2.5 V (80%) in [89].

High temperature performance of this inverter is shown in Fig. 5.7 (b), revealing a very good behavior at 300 °C with V_{OH}, V_{OL}, V_{IL}, V_{IH} equal to 5 V, 0.15 V, 2 V, 2.9 V, respectively. The voltage swing at 300 °C was 4.85 V / 5 V (97%), with 1.6% degradation compared with the value at RT. This value is much larger than the best values in the literatures 4.5 V / 5 V (90%) in [89] at 200 °C and 6.5 V / 7 V (93%) in [88] at 300 °C. NM_L and NM_H at 300°C were 1.85 V / 2.5 V (74%) and 2.1 V / 2.5V (84%), respectively, which shows an excellent operation even at 300 °C.

To investigate the operating speed of the GaN digital ICs based on the E/D-mode HEMTs, a 59-stage ring oscillator (*RO*) with one buffer stage was fabricated using 118 integrated transistors. The inverter at each stage features the same transistor size as the inverter circuit discussed above. The microphotograph, schematic circuit, and frequency domain characteristics are shown in Fig. 5.8. The oscillation frequency fosc is 3.27 MHz, corresponding to a propagation delay τ_{pd} of 2.59 ns by formula $\tau_{pd} = (2nf_{osc})^{-1}$, where the number of stages n is 59 in this work. The propagation delay is not as low as we have expected, due to the size of our devices and gate

recess. This can be improved in the future work to result in much lower propagation delay.

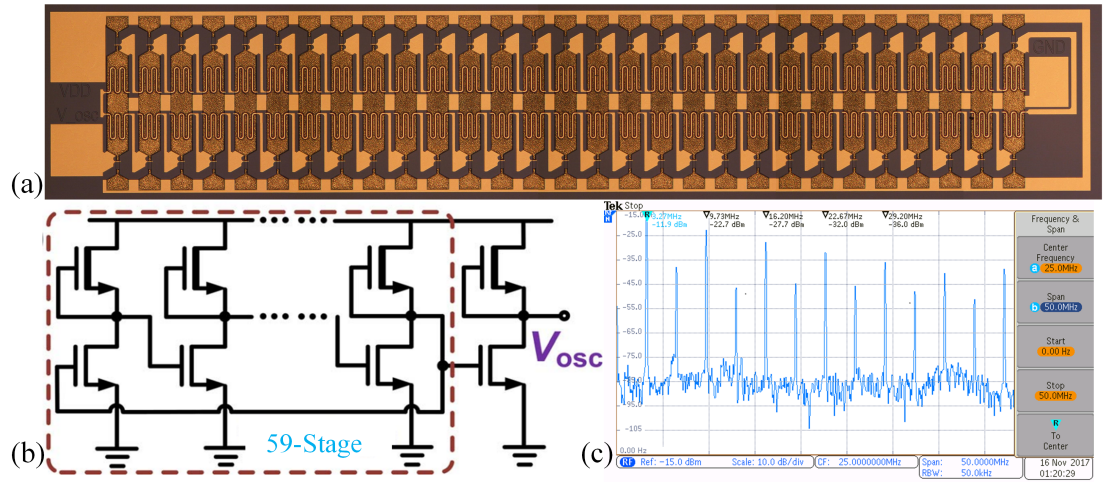


Figure 5.8 – (a) Top view micrograph and (b) schematic equivalent circuit of the fabricated 59-stage ring oscillator. (c) The measured frequency characteristics of ring oscillator at room temperature when the supply voltage V_{DD} is 5V.

5.3.3 NAND and NOR logic gate

NAND and NOR logic gate are widely used in digital logic and driving circuits as basic components. The NAND and NOR circuits were fabricated and characterized along with NOT inverter circuits. Fig. 5.9 shows the VTC of the fabricated NAND logic gates (equivalent circuit in Fig. 5.4 (a)), for which V_{DD} was 5 V, V_B was swept from 0 to 5V and V_A was set at 4 different cases:

Case 1:

$V_A = 0$, thus $V_{out} = \overline{V}_A + \overline{V}_B = 1$ (Fig. 5.9 (a));

Case 2:

$V_A = 1$, thus $V_{out} = \overline{V}_A + \overline{V}_B = \overline{V}_B$ (Fig. 5.9 (b)). The $V_{OL} = 2R_E/(R_D + 2R_E) \cdot V_{DD}$ is larger than that of the inverter since the equivalent resistance of E-mode transistor is $2R_E$ instead of R_E.

Case 3:

$V_A = V_B$, thus $V_{out} = \overline{V}_A + \overline{V}_B = 2\overline{V}_B$. In this case, V_A and V_B are changing simultaneously, which is quite similar to the case 2 (Fig. 5.9 (c)), except that the transition region is relatively longer, since the equivalent resistance in the lower side is larger.

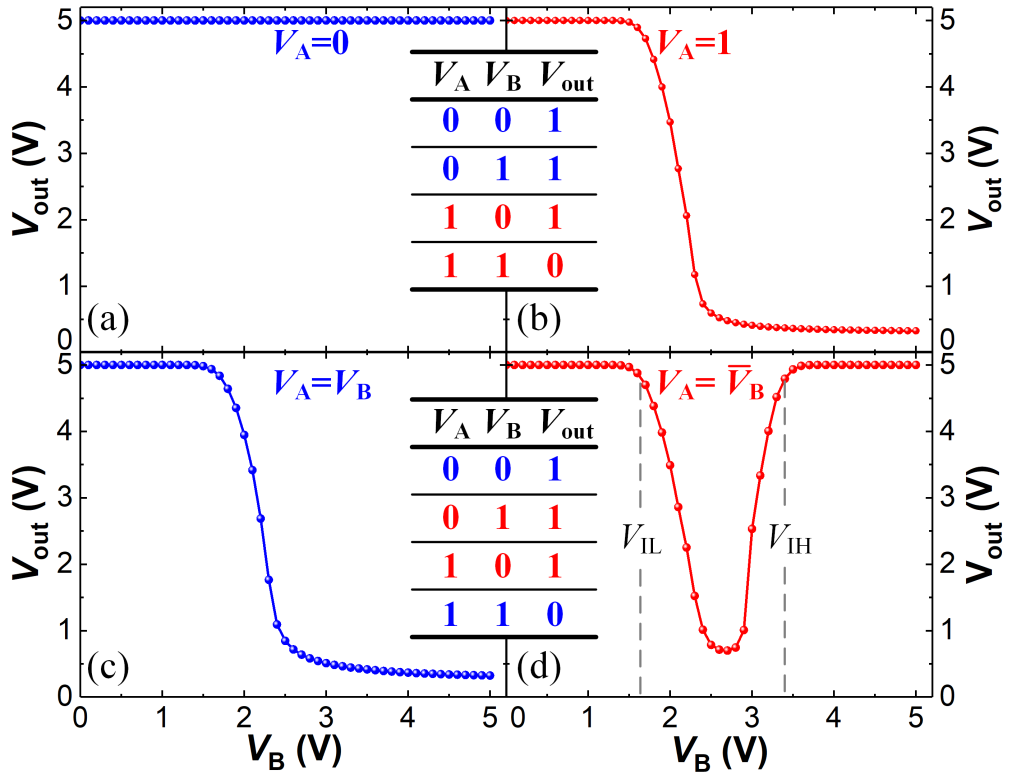


Figure 5.9 – The VTC of NAND gate logics under different input voltages, where (a) V_A = 0, (b) V_A = 1, (c) V_A =V_B, and (d) V_A= $\overline{V}_B$, V_B is sweeping from 0 to 5 V. Insets: corresponding truth table for NAND logic.

Case 4:

$V_A = \overline{V}_B$, thus $V_{out} = \overline{V}_A + \overline{V}_B = V_B + \overline{V}_B$ (Fig. 5.9 (d)). When $V_B < V_{IL}$ and $V_B > V_{IH}$, V_B=0 and V_B=1, thus V_{out}=1, and $V_{IL} \leq V_B \leq V_{IH}$, the logic output is ambiguous.

Fig. 5.10 shows the VTC of the fabricated NOR logic gates (equivalent circuit in Fig. 5.4 (a)), for which V_A was set at 4 different cases:

Case 1:

$V_A = 0$, thus $V_{out} = \overline{V}_A \cdot \overline{V}_B = \overline{V}_B$ (Fig. 5.10 (a));

Case 2:

$V_A = 1$, thus $V_{out} = \overline{V}_A \cdot \overline{V}_B = 0$ (Fig. 5.10 (b));.

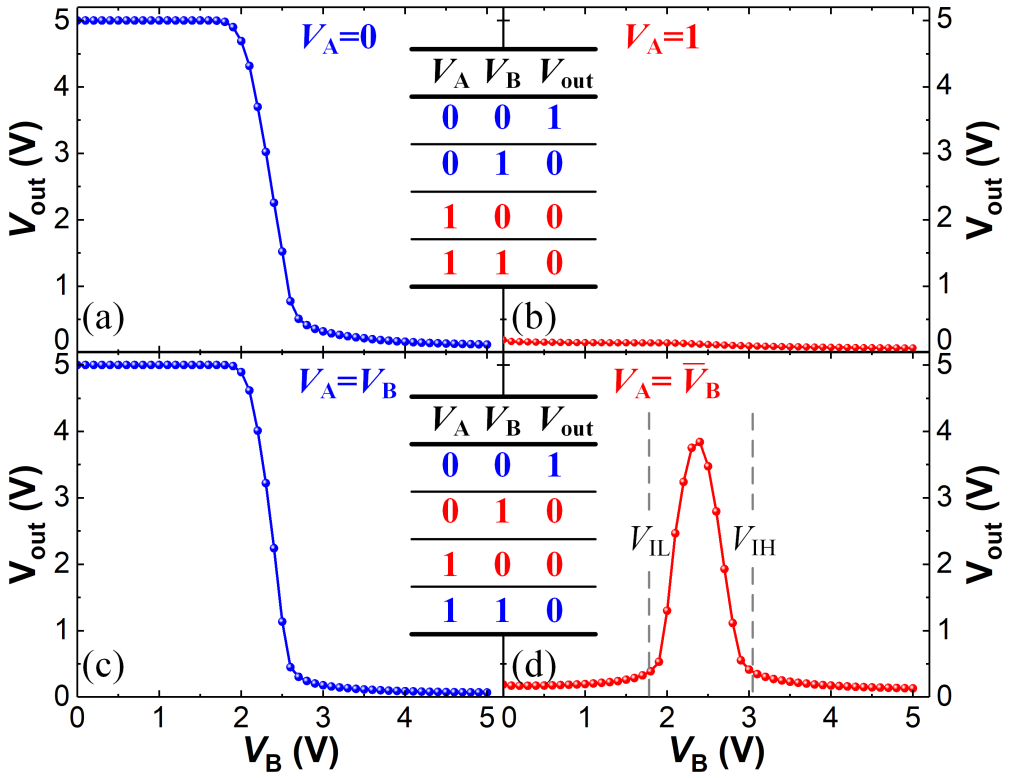


Figure 5.10 – The VTC of NOR gate logics under different input voltages, where (a) $V_A = 0$, (b) $V_A = 1$, (c) $V_A = V_B$, and (d) $V_A = \overline{V}_B$, V_B is sweeping from 0 to 5 V. Insets: corresponding truth table for NOR logic.

Case 3:

$V_A = V_B$, thus $V_{out} = \overline{V}_A + \overline{V}_B = \overline{V}_B \cdot \overline{V}_B$. In this case, V_A and V_B are changing simultaneously, which is quite similar to the case 1 (Fig. 5.10 (c)), except that the equivalent resistance is $R_E/2$ instead of R_E, which led to a lower V_{OL} and sharper transition.

Case 4:

$V_A = \overline{V}_B$, thus $V_{out} = \overline{V}_A \cdot \overline{V}_B = V_B \cdot \overline{V}_B$ (Fig. 5.10 (d)). When $V_B < V_{IL}$ and $V_B > V_{IH}$, V_B=0 and V_B=1, thus V_{out}=0, and $V_{IL} \leq V_B \leq V_{IH}$, the logic output is ambiguous.

In this section, we have demonstrated high performance NOT logic with high logic swing voltage, high noise margin, and low transition period both at RT and at 300°C. NAND and NOR GaN logic gates were demonstrated for the first time with very good performance. These results show the enormous potential of GaN-based logic gates for future monolithic integration in gate drivers as well as for high temperature applications.

5.4 E-/D-mode tri-gate MOSHEMTs based GaN NMOS logic gate circuits

5.4.1 Introduction and motivation

In last section, we have demonstrated logic NOT, NAND, and NOR circuits with monolithic integration of E/D-mode GaN transistors by optimizing the load-to-driver resistance ratio in NMOS logic gates through the use of a multi-finger gate design of E-mode GaN MOSHEMTs to improve the logic performance (high noise margins, low logic transition voltages, large logic swing, and small V_{OL}). The gate recess of E-mode device was optimized to reduce the R_{ON} of E-mode GaN MOSHEMT and to minimize the overall size of NOT logic gate. We developed a novel treatment for the dielectric deposition to achieve high temperature performance up to 300°C. High voltage E-mode power MOSHEMTs were monolithically fabricated together with logic gates, which reveals the possibility of monolithic integration of gate drivers with power devices.

However, these logic gates suffer from unstable transient voltage, low noise margin, and high logic leakage current. Additionally, the large size mismatch between the E-mode and D-mode transistors hinders their compact integration [85]. The more positive threshold voltage, lower gate leakage, and smaller threshold-voltage (V_{TH}) variation of tri-gate HEMTs [99] can lead to higher noise margin, lower leakage current, and more stable transient voltage of logic gates. Moreover, the tunable V_{TH} of tri-gate transistors offer much more design flexibility for the size of the load transistor (D-mode transistor in this case), which lead to the size matching of E/D-mode transistors.

Thus, in this section, we demonstrated logic gates with monolithic integration of tri-gate E/D-mode tri-gate MOSHEMTs. The tri-gate structure in the logic gate offers unique advantages compared with conventional planar E/D-mode design. Firstly, the logic gate can be designed with much more compact integration with same E/D-mode transistor size thanks to the additional tunable V_{TH} of tri-gate structure. Moreover, the stable and consistent V_{TH} of E-mode tri-gate devices leads to better logic performance. The tri-gate structure enables larger logic transition V_{TH}, lower V_{OL} without oversizing the E-mode transistor, and smaller logic gate leakage simultaneously.

5.4.2 Device structure and logic design

The structure of fabricated E/D-mode tri-gate MOSHEMTs is shown in Fig. 5.11. As we can see from Fig. 5.11 (b-c), the device consists of E-mode recessed tri-gate transistors and D-mode tri-gate transistors. The E-mode transistors used the technology developed in chapter 3. The V_{TH} of planar, tri-gate, recessed planar and recessed tri-gate is different as shown in Fig. 5.12. One of the main feature of tri-gate structure is the tunable V_{TH}, this can help to design a much compact integration of E/D-mode transitors pair. In order to have a lower V_{OL}, we have to make a smaller R_E and a larger R_D according to equation 5.1. This would lead to a size mismatch between the

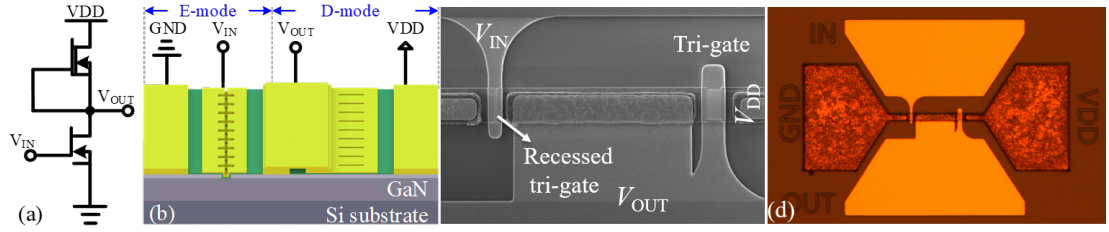


Figure 5.11 – (a) Equivalent circuits of a typical NOT logic. (b) 3D structure of monolithic integration of E/D-mode tri-gate MOSHEMTs. (c) SEM and (d) top microscopy view of E/D-mode tri-gate logics.

E-mode and D-mode transistors in previous design (Fig.5.4 (c)). The V_{TH} of D-mode tri-gate transistors is -2 V compared with -4 V for D-mode planar transistors Fig. 5.12 (a). Since the V_{TH} of tri-gate transistors is much closer to 0 V, the tri-gate D-mode transistor would have much larger resistance compared with D-mode planar transistor (at V_G= 0 V, since the gate and source were interconnected for D-mode load transistors). In this way, there is not necessary to make the D-mode device a much smaller size compared with E-Mode device. Furthermore, the E-mode recessed tri-gates present small ON resistance (V_G = 5) of about 7 Ω·mm (Fig. 5.12 (b)), which lead to small low-level output voltage (V_{OL}).

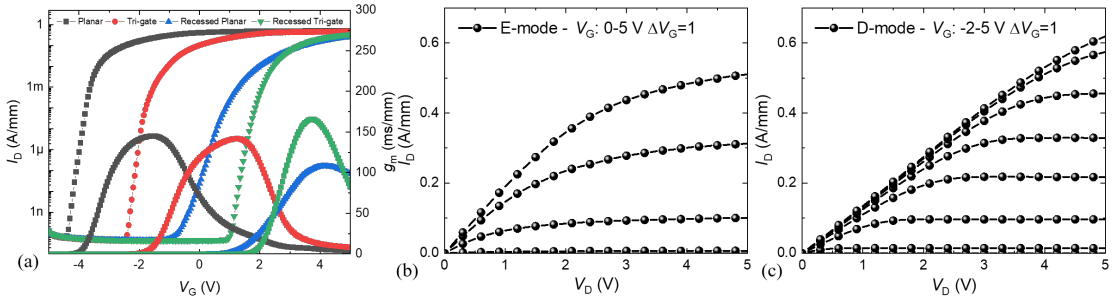


Figure 5.12 – (a) Transfer characteristics comparison of planar, tri-gate, recessed planar and recessed tri-gate devices. Output characteristics of (b) E-mode recessed tri-gate transistors and (c) D-mode standard tri-gate transistors.

5.4.3 Device optimization and characterization

The optimized design of the planar DCFL inverter discussed previously by integrating a D-mode MOSHEMT with $(W/L)_D$ = 160 μm / 8 μm acting as the active load and an E-mode MOSHEMT with a $(W/L)_E$ = 10 μm / 32μm acting as the driver source, which corresponds to a ratio α of 64. There is a size mismatch between D-mode and E-mode devices of 16 for the device width and 4 for the device length hinders their compact integration. However, the tri-gate DCFL inverter will be monolithically integrated a D-mode tri-gate MOSHEMT with $(W/L)_D$ =5 μm / 5 μm acting as the active load and an E-mode tri-gate MOSHEMT with a $(W/L)_E$ = 5 μm / 5μm acting as the driver source, which corresponds to a ratio α of 1. This mainly due to the tunable V_{TH} of

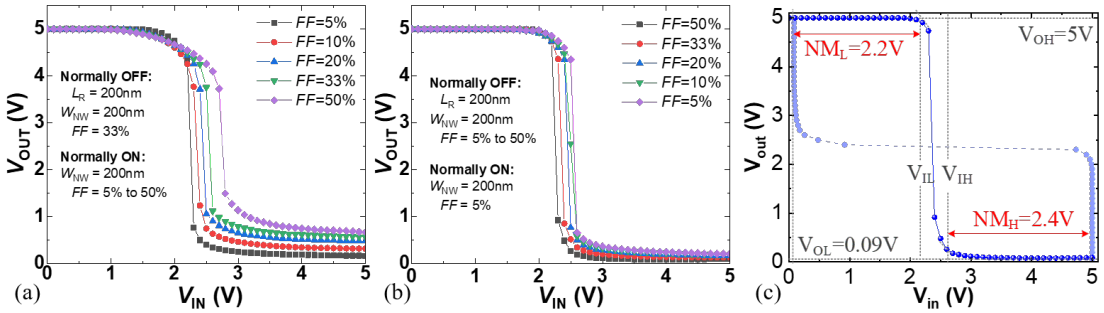


Figure 5.13 – (a) The VTCs of the tri-gate NMOS inverters with different FF of D-mode tri-gate structure with the fixed nanowire width of w = 200 nm. The E-Mode tri-gate structure is fixed with FF=0.33. (b) The VTCs of the tri-gate NMOS inverters with different FF of E-mode tri-gate structure with the fixed nanowire width of w = 200 nm. The D-Mode tri-gate structure is fixed with FF=0.05. (c) The VTC of the optimized tri-gate logic inverter.

E/D-mode tri-gate transistors.

Fig. 5.13 (a) shows the optimization of tri-gate DCFL inverter circuit by changing the fin width (w) from 200 to 100 nm at the same time to maintain the variation of FF from 5% to 50% for the D-Mode tri-gate devices, however the E-mode recessed tri-gate transistors remained unchanged. The lower FF would lead to higher equivalent R_D and according to $V_{OL} = \frac{R_E}{R_E+R_D} V_{DD}$, thus could contribute to lower V_{OL} and sharper transition. Thus, the D-mode load resistance could be tuned by simply change the FF of D-mode tri-gate structure. Similarly, the FF of E-mode tri-gate device was varied to observe the variation of logic VTC. The FF of E-mode tri-gate driving transistors would affect the V_{TH} of logic gate as well as the equivalent R_E. The smaller FF had higher V_{TH}, as well as higher resistance, which was contradictory for a high performance logic gate circuit. Thus, there was a trade-off to reach high performance logic gate circuit.

The optimum VTC of tri-gate DCFL inverter was shown in Fig. 5.13 (c). The V_{TH} of the DCFL was close to 23 V, which made the logic VTC is very close to the ideal switch. The V_{OH} and V_{OL} were 5 V and 0.09 V, respectively, yielding a large voltage swing of 4.91 V/5 V (98.2%) compared to the best values in the literature of 4.66 V / 5 V (93.2%) [89] and 6.3 V / 7 V (90%) [88]. The V_{IL} and V_{IH}, defined at dV_{out}/dV_{in} = -1, were 2.25 V and 2.6 V, respectively. The width of the transition voltage region (V_{TR}= V_{IH} - V_{IL}) is a way of measure the ambiguity of the logic inverter [153], which must be as low as possible. The transition voltage width was 0.35 V / 5 V (12%) in our case, which is outperform the state of the art [88, 89]. The NM_L and NM_H are 2.2 V / 2.5V and 2.4 V / 2.5 V, respectively, which outperforms the best values of 1.7 V / 2.5 V (68%) and 2 V / 2.5 V (80%) in [89, 102]. The excellent performance of tri-gate DCFL is achieved without oversizing the E/D-mode transistors, with very sharp transition with less than 0.5V, high NM_L of 2.2V, high NM_H of 2.4V, high V_{OH} of 5V and low V_{OL} of 0.09 V.

To investigate the operating speed of the GaN digital ICs based on the E/D-mode tri-gate MOSHEMTs, a 101-stage ring oscillator (RO) with one buffer stage was fabricated using 202

integrated transistors (Fig. 5.14 (a)). The inverter at each stage features the same transistor size as the inverter circuit discussed after optimization. The microphotographs of fabricated logic gates are shown in Fig. 5.8 (a-b). The measurement was carried out with precise RF probe station to lower the noise and unnecessary long wire. The oscillation frequency f_{osc} is 10.17 MHz, corresponding to a propagation delay τ_{pd} of 489 ps by formula $\tau_{\mathrm{pd}} = (2nf_{\mathrm{osc}})^{-1}$, where the number of stages n is 101 in this work. The propagation delay is much lower than previous version with planar E/D-mode MOSFETs (2.59 s).

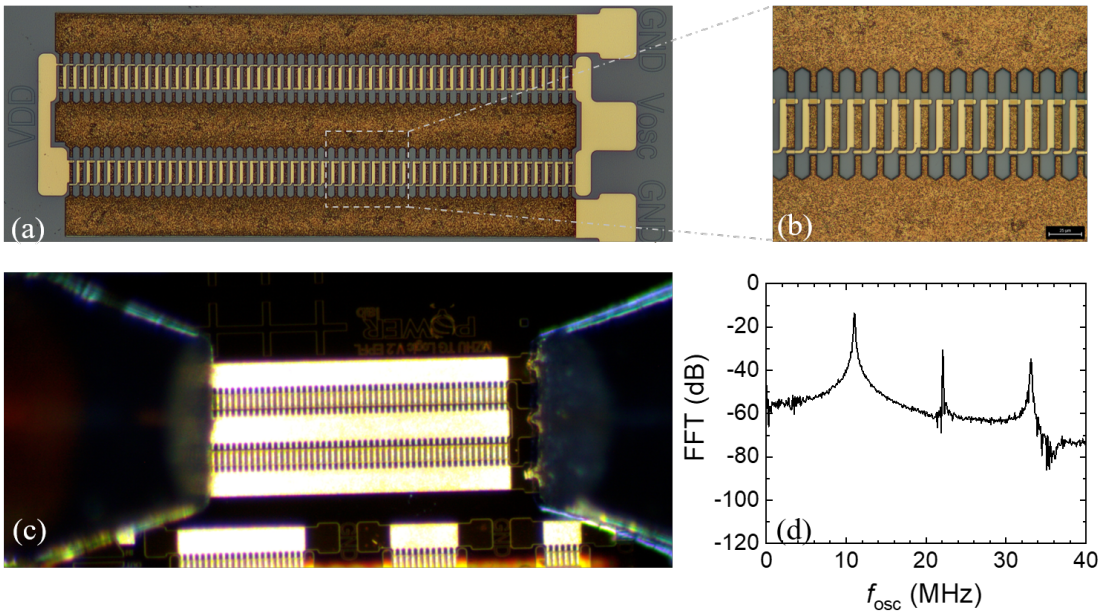


Figure 5.14 – (a) Top view micrograph and (b) zoomed top view of the fabricated 101-stage ROs. (c) Experimental setup of RF probe station for measuring *RO* oscillation frequency. (d)The measured frequency characteristics of ring oscillator at room temperature when the supply voltage V_{DD} is 5 V.

5.5 GaN-based voltage source driver (VSD)

5.5.1 Introduction

Increasing the switching frequency of the GaN transistors is an important strategy to reduce the size and volume of passive components in power converters [15] and increase the power density of switching power supplies. However, as the switching frequency increases, both switching losses and gate driver losses increase proportionally, which limits the converter efficiency.

The typical GaN HEMT structure and the simplified model are shown as Fig.5.15 (a) and (b), the

turn-on and turn-off time constant is determined by:

$$\tau = (R_{DRV} + R_G)(C_{GS} + C_{GD}) \tag{5.2}$$

where R_{DRV}, R_G, C_{GS}, C_{GD} are shown as Fig.5.15 (c). Thus the final challenge is to reduce R_{DRV}, R_G, C_{GS}, C_{GD} simultaneously. While most of the efforts of the scientific community have been on improving the device performance. The gate driver must be designed and optimized together with the GaN power device. The ultimate aim is to monolithically integrate the driver and device in the same GaN chip. In this way, we can truly take advantage of the high-frequency switching properties of GaN semiconductors.

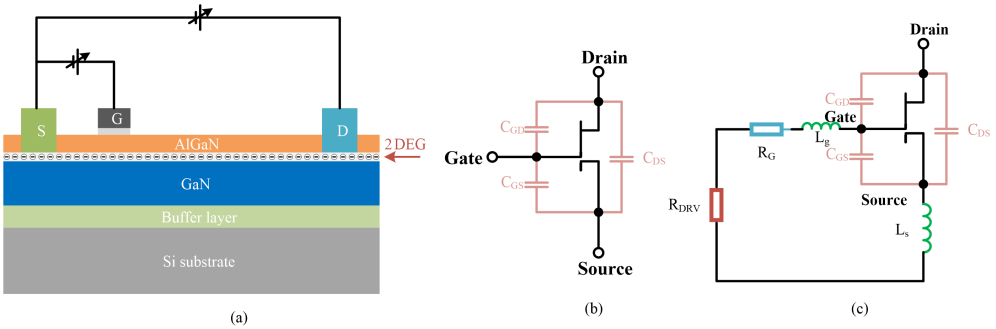


Figure 5.15 – (a) Schematic of a GaN HEMT cross-section structure. (b) Circuit Model and (c) Driver circuit.

The technical challenges for GaN gate drivers operating at high frequencies are the following:

a) **Small Gate Voltage:** GaN transistors have relatively low gate breakdown voltage compared with silicon devices, as illustrated by the devices from EPC and GaN Systems. As a result this offers very low safe margins for operation as the fast switch of GaN transistors lead to large dv/dt and di/dt and the voltage drop at parasitic inductances and capacitances could break the gate oxide of the device, which consequently limits their switching speed.

b) **dv/dt and di/dt immunity:** GaN transistors can switch at speeds as high as 177 V/ns [92]. The dv/dt going through C_{GD} and C_{GS} during a switching period of the device can lead to V_{GS} larger than the threshold voltage of transistor to falsely turn-on the devices. Similarly, the high di/dt of GaN transistors can induce large voltages on L_g and L_s to false turn-on or even breakdown the devices.

There are three common types of driver topologies, Voltage Source Driver (VSD), Resonant Gate Driver (RGD) and Current Source Driver (CSD). VSD is very easy to implement, however all gate charges are dissipated through gate resistors and the charging speed is limited by the gate driver loop resistors, causing large gate charging and switching losses in high switching frequency applications. RGD requires a resonant tank, which will feedback part of the gate charge to the

Table 5.1 – Comparison of gate driver voltage of GaN transistor, Silicon and SiC transistors

Gate voltage	GaN system	EPC GaN	Si MOSFET	IGBT	SIC MOSFET
Maximum rating	-10/+7 V	-5/6 V	+/-20 V	+/-20 V	18/18 V
Operation	0/6 V	0/5 V	0/10 V	0/15 V	-4/15 V

power supply, however the resonant tank needs fixed frequency for a given configuration, which limits the flexibility of circuit operation frequency. In addition, the parasitic components of the LC tank could lead to stability issues at high frequency switching.

CSD offers the possibility to combine the advantages of both of these configurations. This circuit is able to feedback gate charges to the power supply through a judicious control strategy. Its current source can reduce switching losses by reducing the overlap between drain-source voltage and current in the transistor. More importantly, the presence of a current source in the CSD topology offers the ability to charge the gate capacitance very quickly, increasing the switching frequency of the circuit. The drawbacks of CSD are the need of more transistors and the more complex logic signal control. CSD has similar complexity as RGD, however it offers the benefit of reducing switching loss (which is considerably larger than gate charge losses). Thus, in this proposal we choose to investigate and compare the performance of VSD and CSD focusing on the trade-off between complexity and efficiency.

Ideal gate driver: The ideal gate driver (Fig.5.16) operates as voltage source during the static state (on or off) and current source during transient state (turn-on or turn-off). The higher static state voltage will reduce R_{ON} and then reduce conduction losses, while the higher current during transient will shorten switch period and then reduce switching losses. This is the ultimate goal of our driver circuit design: minimizing gate charge, switching loss and conduction loss simultaneously.

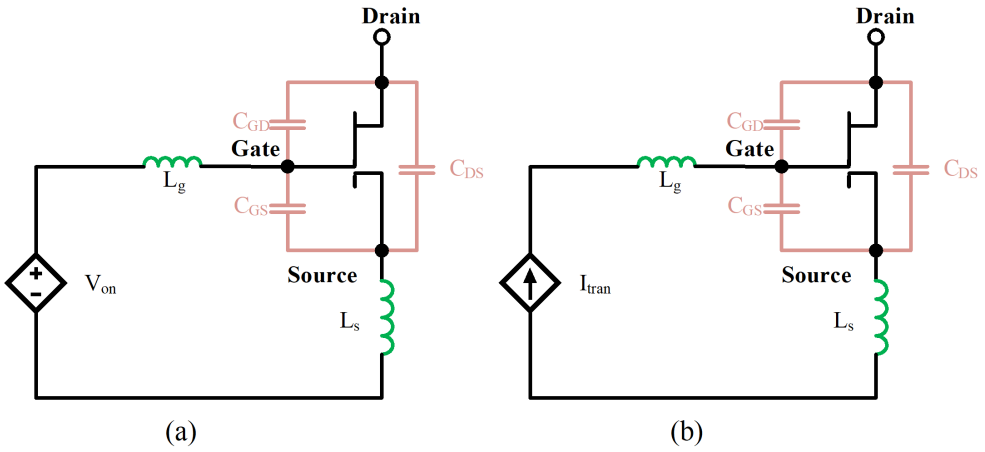


Figure 5.16 – Ideal gate driver (a) steady state of transistor (b) transient of transistor

Voltage Source Drivers: Typically, CMOS transistors are used for gate drivers, however its

monolithic implementation on GaN chips is limited by the poor quality of p-type GaN transistors. In this thesis, we will focus solely on n-channel GaN HEMTs which can be achieved by introducing a NOT logic in our topologies as shown in Fig.5.17 (a) and (b). In addition, R_{Gon} and R_{Goff} will be separately designed to yield higher switching speed at turn-on period and higher dv/dt immunity at turn-off period. We highlight that these resistances, and consequently t_{on} and t_{off} do not need to be equal since they affect differently the circuit response. The equivalent piecewise waveform of voltage source gate driver is shown as Fig.5.17 (c), where the switching losses happen on t_{on} (t_3-t_1) and t_{off} (t_8-t_6).

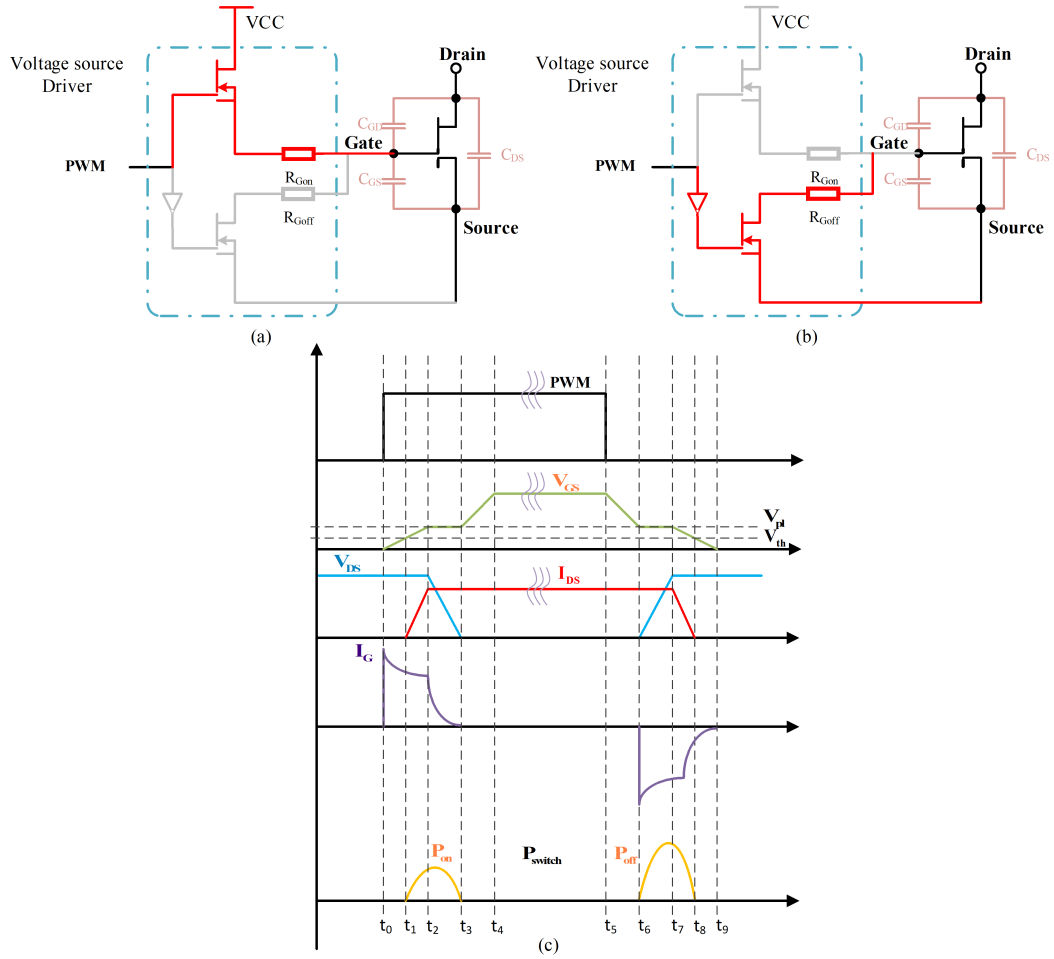


Figure 5.17 – Conventional voltage source driver (a) turn on transition, (b) turn off transition and (c) Switching waveforms

$$P_{\text{sw}} = \frac{1}{2} V_{\text{DS}} \cdot I_{\text{D}} \cdot (t_{\text{on}} + t_{\text{off}}) \cdot f_{\text{sw}} \tag{5.3}$$

From equation 5.3, the switching losses are proportional to turn-on and turn-off times. The main drawback of the VSD is that the RC charging and discharging limits the switching speed

(time constant is determined by equation 5.2). In such topology, simply reducing R is not a solution to decrease charging/discharging times since this would increase ringing through the parasitic components from both the driver and transistor, hence reduce di/dt and dv/dt immunity. A monolithically integration of the driver and transistors would address this issue by reducing R but also all the other parasitic components, hence maintaining good di/dt and dv/dt immunity.

In addition, losses related to the gate charging become important when switching at very high frequencies. The dependence of gate losses on frequency is given by equation 5.4:

$$P_{\mathrm{g}} = Q_{\mathrm{g}} V_{\mathrm{cc}} f_{\mathrm{s}} \tag{5.4}$$

P_{g} dissipates through the R_{driver}, R_{Gon}, R_{Goff} which heats up the driver. This heating at high switching frequencies can be a challenge for CMOS drivers due to the low operation temperature of silicon circuits, however it is not a problem for GaN drivers due to its higher operation temperature. In addition, our laboratory is developing technologies for optimized heat transfer in GaN devices that will also be applied to gate drivers.

In summary, the biggest advantage of VSD is the easy implementation compared with the other gate driver topologies. The monolithic integration proposed all-in-GaN solution will minimize the parasitic inductance and enable smaller R_{driver}, R_{Gon}, R_{Goff} to reduce the switching losses.

5.5.2 Development of the GaN HEMT gate charging model

Hard-switching and soft-switching topologies are most commonly used in power electronis converters, while only drivers for hard switching topologies will be investigated in this thesis due to their simplicity.

The total hard switching losses in GaN HEMTs include switching losses (P_{sw}), gate charge loss (P_{G}), output capacitance charging losses (P_{oss}) and reverse conduction losses (P_{RC}), while the reverse recovery losses (P_{RR}) are zero due to the majority carrier conduction in GaN HEMTs. Understanding the loss mechanism is essential for minimizing overall power losses and improving the efficiency.

The turn-on and turn-off transitions of GaN power transistors are shown on Fig. 5.18 (a), which indicates that the overlap of drain voltage and current is inevitable during these transitions. Thus, our main target is to minimize this overlap in order to reduce switching losses. However, GaN HEMTs have their own intrinsic inductances and capacitances, which impose limitation in reducing the gate and driving resistance.

In order to easily understand the GaN HEMT charging process, a model of the gate charging is built considering the ideal case with inductive current source input. The diagram of the charging model and the charging process are illustrated as Fig. 5.18 (b)-(e).When the gate voltage begins

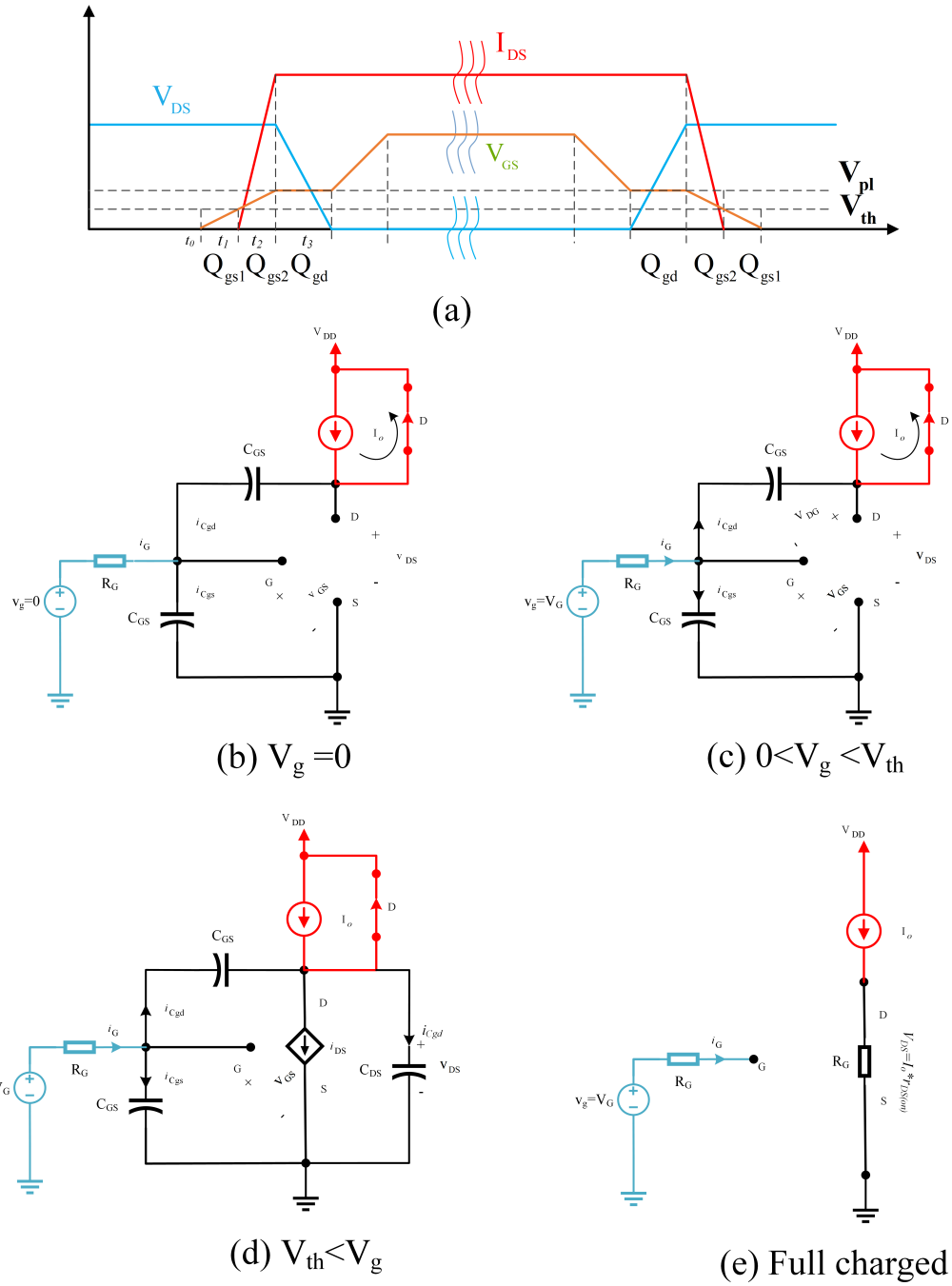


Figure 5.18 – (a) Ideal switching waveform of GaN HEMT in terms of V_{ds}, V_{gs} and I_{ds} versus time during turn-on and turn-off period. Simplified turn-on model of GaN HEMT with a current source input: (b) GaN HEMT is off when gate voltage is low, (c) GaN HEMT is off before gate voltage reaches V_{th}, (d) gate keeping charging until input capacitance is full, while C_{DS} is discharging, (e) gate is fully charged.

to rise with gate charging, the model can be written as:

$$\begin{cases} v_{\mathrm{GS}}(t) = V_{\mathrm{G}}\left(1 - e^{-(t-t_0)/\tau}\right) \\ i_{\mathrm{G}}(t) = \frac{V_{\mathrm{G}}}{R_{\mathrm{G}}} e^{-(t-t_0)/\tau} \\ \Delta t_{1-0} = -\tau \ln\left(1 - \frac{V_{\mathrm{th}}}{V_{\mathrm{G}}}\right) \end{cases} \tag{5.5}$$

Where τ is equal to 5.2, V_{th} is the threshold voltage, the time range Δt_{1-0} is shown in Fig. 5.18 (a). The charging process is shown in Fig. 5.18 (c), the gate voltage begins to rise until it reaches the threshold voltage and the V_{DS} is kept constant and I_{DS} is zero. When the voltage reaches the threshold voltage, the drain voltage will decrease and the drain current will begin to rise. In the simplified model, the drain voltage remains constant since the current is clamped by the input current source until the GaN HEMT current catches up as shown in Fig. 5.18 (d). The model during this process is:

$$\begin{cases} i_{\mathrm{DS}}(t) = g_{\mathrm{m}}(v_{\mathrm{GS}} - v_{\mathrm{th}}) - g_{\mathrm{m}} V_{\mathrm{G}} e^{-(t-t_1)/\tau} \\ \Delta t_{2-1} = \tau \ln \frac{g_{\mathrm{m}} V_{\mathrm{G}}}{g_{\mathrm{m}}(V_{\mathrm{G}} - V_{\mathrm{th}}) - I_o} \end{cases} \tag{5.6}$$

Where transconductance ($g_{\mathrm{m}} = dI_{\mathrm{DS}}/dV_{\mathrm{GS}}$) is the change in I_{DS} caused by the variation of V_{GS}. Equation 5.6 shows that the device current I_{DS} is determined by channel modulation and better transconductance. After the drain current I_{DS} reaches the input current, the driver voltage begins to drop until the gate capacitance is fully charged. Then, the entire gate current flows through C_{GD},

$$\begin{cases} V_{\mathrm{DS}}(t) = -\frac{V_{\mathrm{G}} - V_{\mathrm{th}}}{R_{\mathrm{G}} C_{\mathrm{GD}}}(t - t_2) + V_{\mathrm{DD}} \\ \Delta t_{3-2} = R_{\mathrm{G}} C_{\mathrm{GD}} \frac{V_{\mathrm{DD}} - I_{\mathrm{D}} r_{\mathrm{DS(on)}}}{V_{\mathrm{G}} - V_{\mathrm{th}}} \end{cases} \tag{5.7}$$

Thus, the overall turn-on time ($t_{on} = \Delta t_{1-0} + \Delta t_{2-1} + \Delta t_{3-2}$) is needed to take into account in gate driver design. The final state as illustrated in Fig. 5.18 (e) shows the gate charging dynamic is over and transistor is fully on. The similar model can be derived for the turn-off transition.

According to equations 5.5 - 5.7, all variables that can be controlled can be divided into two groups:

- **Intrinsic parameters:** The intrinsic parameters of the HEMTs will be determined by device optimization. The C_{GS} and C_{GD} will be the premier target for minimization. This gate capacitance can be optimized by changing the gate dielectric and dielectric thickness. The thicker gate dielectric can have higher threshold voltage, which is also good for the

reliability of normally-off transistors. Moreover, reducing the gate length can minimize gate resistance and capacitance.

- **External parameters:** As we can see from equations equations 5.5 - 5.7, the gate driver resistance affects all the process of gate charging. The high di/dt, dv/t with the parasitic inductance/capacitance would cause gate ringing, false turn-on or oxide break down, which prevents the design of the gate driver.

5.5.3 Simulation of VSD versus different driver resistance and driver loop inductance

As concluded from the simplified transistor turn-on model, the gate charging periods are strongly related to the equivalent series resistance of the gate driver. However, the approach will not solely rely on reducing the driver resistance with the presence of LCR-series resonant tank formed by equivalent resistance (R_{drive}+R_{G}), interconnection inductors (L_{g}+L_{s}) and input capacitance (C_{GS}+C_{GD}) during the turn-on process as shown in Fig. 5.19 (a) and turn-off process as shown in Fig. 5.19 (b). The gate driving voltage of most existing commercial E-mode devices is around 4.5~5V to achieve optimal performance with minimum R_{ON}, while most of the commercial GaN devices' gate oxide breakdown voltage is around 6 V. This leaves a very small margin for driver overshoot to ensure safety operation of GaN devices. This phenomenon can be observed by simulations (Fig. 5.19 (c) and (d)). If the gate resistance is too small, the gate driver loop inductance will resonate with the input capacitance during turn-on/turn-off transition. The gate overvoltage during the turn on transition may exceed gate oxide breakdown, resulting in failure of power transistor. Moreover, the gate ringing voltage during turn-off transition may exceed the threshold voltage, leading to false turn-on of the devices. This would cause circuit shot-through leading to higher power losses. This gate overvoltage and ringing can be reduced with higher gate resistances as shown in Fig. 5.19 (c), nevertheless, this would result in higher switching loss due to the lower charging speed.

In order to improve the frequency performance of GaN devices, a proper gate driver circuit has to be designed. The overshoot for this network can be described by:

$$V_{\text{overshoot}} = \frac{V_{\text{peak}} - V_{\text{final}}}{V_{\text{peak}}} = e^{\frac{-\zeta \cdot \pi}{\sqrt{1-\zeta^2}}} \tag{5.8}$$

where $\zeta = \frac{R_{EQ}}{2}\sqrt{\frac{C_{iss}}{L_{EQ}}}$ is the damping factor of the LCR gate tank. C_{iss} is the input capacitance of GaN devices, which is equal to the sum of C_{GS} and C_{GD}. To ensure the safety of GaN transistor, the R_{EQ} should be larger than the following limit:

$$R_{\text{EQ}} \geq \sqrt{\frac{4L_{\text{EQ}}}{C_{\text{iss}}}} \tag{5.9}$$

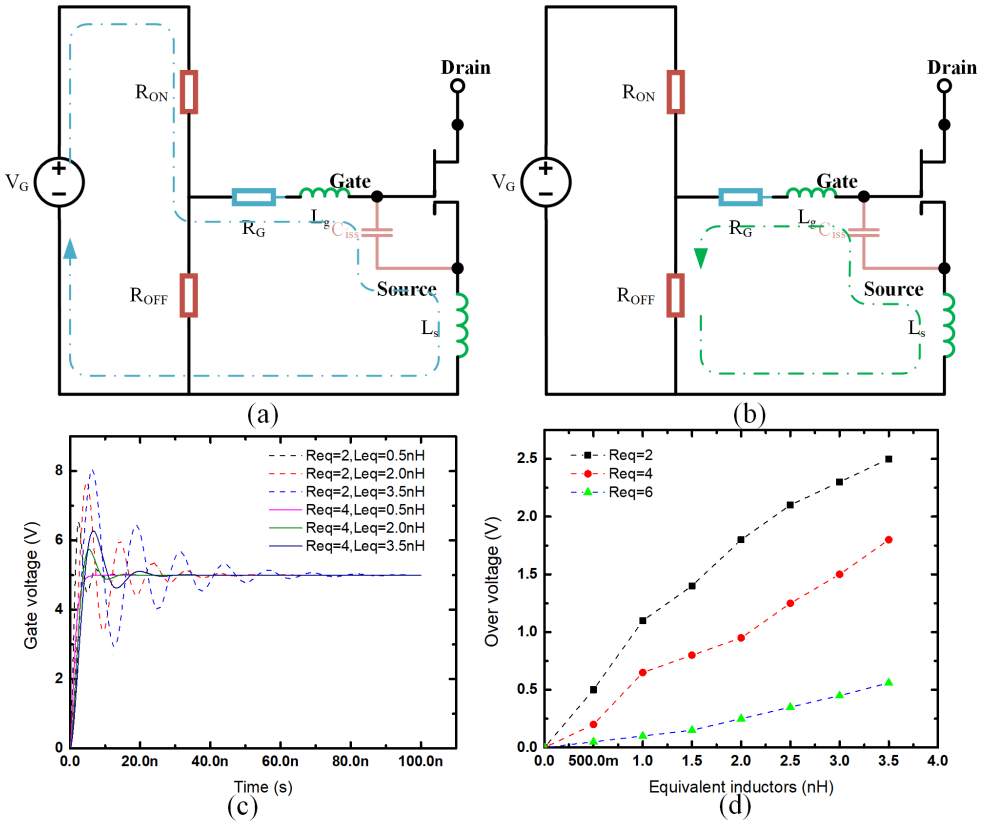


Figure 5.19 – The relationship between gate driver equivalent resistance (R_{EQ}) and the gate loop equivalent inductance (L_{EQ}) with the gate overvoltage: (a) turn-on LCR tank, (b) turn-off LCR tank ,(c) gate voltage versus R_{EQ} and L_{EQ} and (d) gate peak overvoltage versus R_{EQ} and L_{EQ}.

Thus, in order to reduce the gate loop resistance, the best option is to minimize the gate loop inductance according to the equations 5.8 - 5.9. This will help to damp the gate overvoltage and ringing without increasing switching losses.

The simplified equivalent circuit of VSD is shown in Fig. 5.17(a). Due to the absence of CMOS, GaN-based logic would be implemented as shown in Fig.5.20 (a). The VSD circuit contain three logic inverters, driving circuit and bootstrap circuits. Driving circuit is formed by two E-mode transistor instead of typical n- and p-MOS combination, thus a bootstrap circuit is needed for driving purpose. Typical bootstrap circuit is shown in Fig.5.20 (a), which includes a diode and a capacitor. When low side transistor is on, capacitor is charged by V_{DD}. And when the low side transistor is off, the capacitor will maintain the voltage difference of V_{DD}-V_{Forwad} of V_{gs} of upside transistor (V_{D1}). The simulation results of VSD driving signals (Fig.5.20(b)) indicate the bootstrap circuit function well to maintain V_{D1} to be around 4 V. Fig.5.20 (c) shows the simulation results without bootstrap circuits, which could not have a sufficient turn on voltage for the upside transistor. Thus, this would introduce a relative high Rdson for the gate driver.

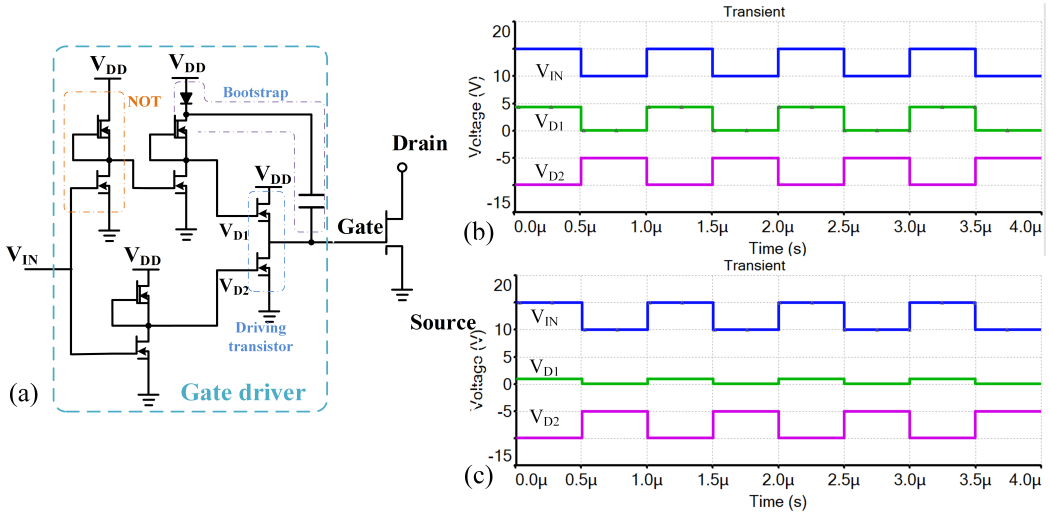


Figure 5.20 – - (a) Equivalent circuit of VSD for implementation (b) simulated gate signal for the VSD with bootstrap circuits (c) simulated gate signal for the VSD without bootstrap circuits

5.5.4 Design and fabrication of VSD

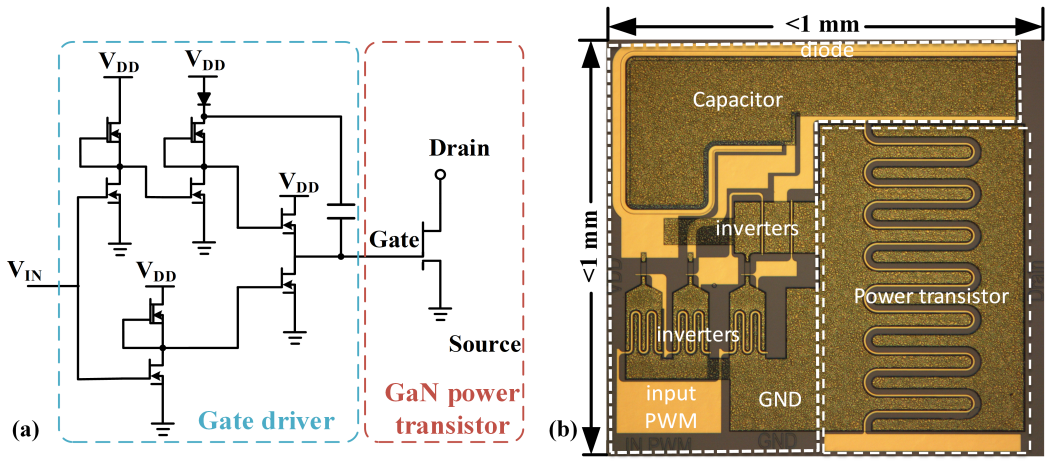


Figure 5.21 – - (a) Equivalent circuit of VSD for implementation (b) simulated gate signal for the VSD with bootstrap circuits (c) simulated gate signal for the VSD without bootstrap circuits

In order to monolithically integrate the GaN driver and power devices on the same chip, we have to ensure every component works seamlessly with each other. We have included the design of integrated diodes and capacitors. A challenging part of the project is the integration of the passive components with the rest of the circuit, which also takes a lot of space of the overall chip size. However, the on-chip diode and capacitor would shorten the circuit connection pass and reduce the wiring parasitic capacitors and inductors. In addition, the on-chip capacitor is built based on standard metal – oxide – metal configuration. The capacitor need to provide fast charge during the turn-on period of lower side transistors and provide stable voltage bias between gate and source pad of up-side transistors. We should have a small capacitance or large diode size

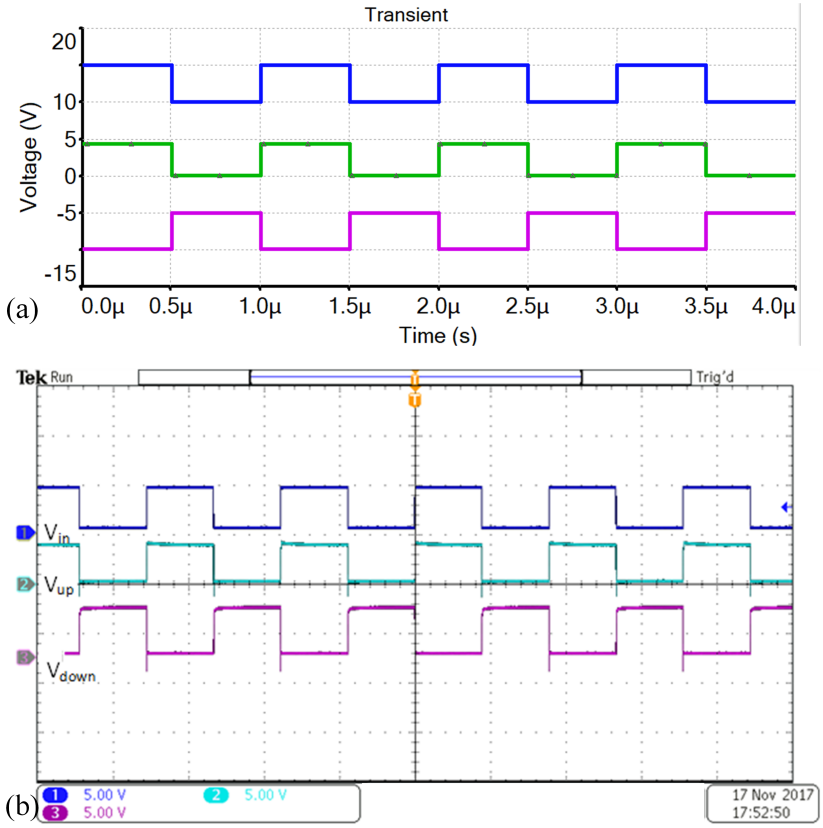


Figure 5.22 – - (a) Equivalent circuit of VSD for implementation (b) simulated gate signal for the VSD with bootstrap circuits (c) simulated gate signal for the VSD without bootstrap circuits

to enable faster charging, while providing constant voltage bias required large capacitance and small diode leakage current. These two requirements are contradictory to each other, thus there is a trade-off between fast charging and stable bias.

The GaN-on-Si epi in this work consisted of 2 nm of GaN cap, 24 nm of $Al_{0.25}Ga_{0.75}N$ barrier, 300 nm of un-doped GaN channel and 5 μm of buffer layers. The concentration and mobility of the 2DEG were about 1×10^{13} cm^2 and 2000 cm^2/V·s, respectively. The device fabrication started with optical lithography to define the mesa, which were etched by inductively coupled plasma with a depth of 450 nm. The ohmic contact was formed by Ti/Al/Ti/Ni/Au (20/120/40/60/50 nm), annealed at 800 °C under forming gas for 30 sec. Then 25 nm SiO2 were deposited by atomic layer deposition and with three dummy pre-run of 10nm deposition. And then, we did the contact opening for source and drain parts as well as the diode pad. We need to notice that there were cross line such as the input PWM signal, which are separated by ALD SiO_2 oxide. The gate, drain contacts and wiring connections were formed using Ni/Au (30nm/170nm).

The equivalent circuit of fabricated VSD is shown in Fig. 5.21 (a). The VSD chip is fabricated successfully as shown in Fig. 5.21 (b). The chip size is within 1mm^2, which includes a capacitor, a diode, three inverters and two driving transistor and a power transistor.

The experimental results of VSD is shown in Fig. 5.22 (b), the driving signal matchs very good compared with the simulation results (Fig. 5.22). The driving voltage of upside transistor is 4V, which has exact same driving voltage as simulated. This indicates the bootstrap circuit works fine in our VSD design.

However, the driving circuit is not working properly due to the bad dynamic performance of GaN power transistor. This big transistor need further optimization for the full monolithic integration.

5.6 Conclusion

In this chapter, we investigated NMOS GaN-based logic gates including NOT, NAND, and NOR by integration of E/D-mode GaN MOSHEMTs. The GaN NMOS inverter was achieved with logic swing voltage of 4.93 V at a supply voltage of 5 V, low-input noise margin of 2.13 V and high-input noise margin of 2.2 V at room temperature. However, these logic gates suffer from unstable transient voltage, low noise margin, and high logic leakage current. Additionally, the large size mismatch between the E-mode and D-mode transistors hinders their compact integration. Thus, the high-performance logic gates with monolithic integration of tri-gate E/D-mode tri-gate MOSHEMTs were fabricated. The tri-gate structure in the logic gate offers unique advantages compared with conventional planar E/D-mode design with much compact size match and more stable V_{TH}. The VSD driver circuit is designed and analyzed and the driving logic signal is tested and working. However, the whole driving circuit is not working properly due to the bad dynamic performance of big power device.

6 Conclusion and future directions

6.1 Conclusions

In this thesis, we investigated the E-mode tri-gate power transistors and logic circuits. We investigated the impact of tri-gate on normally-on/off transistors. This unique structure provided tunable V_{TH}, enhanced V_{BR}, reduced R_{ON}, improved g_m, unique trench conduction and enhanced gate contol. These properties were the fundamental components of this thesis.

We presented normally-off GaN-on-Si MOSFETs based on the combination of tri-gate with a short barrier recess to yield a large positive V_{TH}, while maintaining a low R_{ON} and high I_D^{max}. The tri-gate structure offered excellent channel control, enhancing the V_{TH} up to +1.4 V at 1μA/mm for the recessed tri-gate, along with a much reduced hysteresis in V_{TH}, and a significantly increased g_m. The model of trench conduction is built to understand the additional conduction channels at the sidewalls of the tri-gate trenches compensated the degradation in R_{ON} from the gate recess, resulting in a small R_{ON} of 7.32 ± 0.26 Ω·mm for L_{GD} of 15 μm.

We proposed a new concept for normally-off AlGaN/GaN-on-Si MOS-HEMTs based on the combination of p-GaN, tri-gate and MOS structures to achieve high V_{TH} and low R_{ON}. The p-GaN is used to engineer the band structure and reduce the N_s in the tri-gate structure for a high V_{TH}. This concept eliminates the need for thin barriers (typical in p-GaN devices), which combined to the conduction channels formed at the tri-gate sidewalls, resulted in a smaller R_{ON} compared with planar p-GaN structures. The gate control is mainly achieved from field-effect through the tri-gate sidewalls, and does not rely on injection of gate current, which is different from the conventional p-GaN conduction mechanism. The MOS structure enables much larger gate voltages (V_G) and the effective sidewall modulation results in excellent switching performance at high switching frequencies. .

We investigated GaN based logic circuits and driver circuits. The NMOS GaN-based logic gates including NOT, NAND, and NOR by integration of E/D-mode GaN MOSHEMTs. The GaN NMOS inverter was achieved with logic swing voltage of 4.93 V at a supply voltage of 5 V,

low-input noise margin of 2.13 V and high-input noise margin of 2.2 V at room temperature as well at 300 °C. However, these planar transistors based logic gates suffer from unstable transient voltage, low noise margin, and high logic leakage current. Additionally, the large size mismatch between the E-mode and D-mode transistors hinders their compact integration. Thus, the high-performance logic gates with monolithic integration of tri-gate E/D-mode tri-gate MOSHEMTs were fabricated. The tri-gate structure in the logic gate offers unique advantages compared with conventional planar E/D-mode design with much compact size match and more stable V_{TH}. Addtionally, the possibility of monolithic integration of VSD is investigated and the driving siganal is demonstrated sucessfully.

The results in this thesis reveal the great potential of tri-gate technologies for high voltage normally-off transistor operation, as well as the application in logic circuit filed with fast transient. This work indicates the bright future for the GaN power IC.

6.2 Future development

Due to the time limitation and I found out a lot interesting topic are worthwhile to continue my research.

Normally-off tri-gate devices with good dynamic R_{ON} performance. Although tri-gate structure is interesting and beneficial for the device performance, most of the devices are suffering from the unsatisfying dynamic performance. Especially, the tri-gate normally-off devices (combined with gate recess or p-GaN gate) require gate dielectrics. The gate dielectrics maintain lower gate leakage, however, it causes the problems of V_{TH} instability, hysteresis, and long-term reliability under electrical stress. The dielectrics deposited in this thesis were using plasma enhanced chemical vapor deposition or atomic layer deposition, which is hardly pass those stress test. Depositing high temperature (e.g. 780 °C) using low-pressure chemical vapor deposition (LPCVD) has shown the supior performance in terms of low leakage, high breakdown and long TDDB life time. However, combining LPCVD-SiN_x with tri-gate structure is very challenging due to the severely degraded interface between SiN_x and etched sidewall. Sometime, it might even etch away the tri-gate fins totally. Thus, it would be an important subject to explore the normally-off tri-gate structure with good dynamic performance.

P-GaN regrowth on tri-gate structure and for multi-channel devices. In chapter 4, we have demonstrated p-GaN tri-gate structure with top-down approach. Although the etching process is optimized with low-damage and selective etching, the access region still suffers sheet resistance degradation. Thus, selective regrowth on a specific region is highly desired for continuing the work. The growth process is optimized and the main hinder is the unknown surface Si-based contamination, which could not shift the V_{TH} to positive zone. However, this is an interesting direction to continue. Especially, this might be a very good solution for achieving normally-off operation for a multi-channel GaN transistors.

Full monolithic integration GaN power IC based on tri-gate technology. In order to achieve high frequency, high power density operation of GaN devices, the monolithic integration GaN power IC is highly needed. The tri-gate technology in this work has already demonstrated high performance power transistors and faster logic circuits. Further improvement on power transistors with decent passivation and scaled up power tri-gate devices is required. Moreover, there are missing high quality on chip inductor and capacitors, which is inevitable for the future GaN power IC.

Bibliography

[1] J. A. Carr, D. Hotz, J. C. Balda, H. A. Mantooth, A. Ong, and A. Agarwal, "Assessing the Impact of SiC MOSFETs on Converter Interfaces for Distributed Energy Resources," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 260–270, Jan. 2009.

[2] L. Xiong, F. Zhuo, F. Wang, X. Liu, Y. Chen, M. Zhu, and H. Yi, "Static Synchronous Generator Model: A New Perspective to Investigate Dynamic Characteristics and Stability Issues of Grid-Tied PWM Inverter," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6264–6280, Sep. 2016.

[3] S. Ujita, Y. Kinoshita, H. Umeda, T. Morita, K. Kaibara, S. Tamura, M. Ishida, and T. Ueda, "A fully integrated GaN-based power IC including gate drivers for high-efficiency DC-DC Converters," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 1–2.

[4] T. Kim, M. Jang, and V. G. Agelidis, "1-MHz isolated bipolar half-bridge GaN gate driver for SiC MOSFETs," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Jun. 2015, pp. 575–580.

[5] D. Maksimović, Y. Zhang, and M. Rodríguez, "Monolithic very high frequency GaN switched-mode power converters," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2015, pp. 1–4.

[6] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[7] P. Czyz, A. Reinke, A. Cichowski, and W. Sleszynski, "Performance comparison of a 650 V GaN SSFET and CoolMOS," in *2016 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, Jun. 2016, pp. 438–443.

[8] Y. Developpement, "Status of Power Electronics Industry 2015 Report by Yole Developpement." [Online]. Available: https://www.slideshare.net/Yole_Developpement/status-of-powerelectronicsindustry2015sample

[9] N. Machida, "Si wafer technology for power devices: A review and future directions," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2018, pp. 12–14, iSSN: 1946-0201.

[10] D. Disney and Z. J. Shen, "Review of Silicon Power Semiconductor Technologies for Power Supply on Chip and Power Supply in Package Applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4168–4181, Sep. 2013, conference Name: IEEE Transactions on Power Electronics.

[11] B. J. Baliga, "Gallium nitride devices for power electronic applications," *Semiconductor Science and Technology*, vol. 28, no. 7, p. 074011, 2013. [Online]. Available: http://stacks.iop.org/0268-1242/28/i=7/a=074011

[12] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si Technologies for Power Switching Devices," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013, conference Name: IEEE Transactions on Electron Devices.

[13] K. J. Chen, O. Häberlen, A. Lidow, C. l. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, conference Name: IEEE Transactions on Electron Devices.

[14] J. Ma and E. Matioli, "Improved electrical and thermal performances in nanostructured GaN devices," in *2016 International Conference on IC Design and Technology (ICICDT)*, Ho Chi Minh City, Vietnam, Jun. 2016, pp. 1–4.

[15] A. Lidow, *GaN transistors for efficient power conversion*, second edition ed. Chichester, West Sussex: John Wiley & Sons Ltd, 2014.

[16] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455–457, Oct. 1989.

[17] F. A. Marino, N. Faralli, D. K. Ferry, S. M. Goodnick, and M. Saraniti, "Figures of merit in high-frequency and high-power GaN HEMTs," *Journal of Physics: Conference Series*, vol. 193, no. 1, p. 012040, 2009. [Online]. Available: http://stacks.iop.org/1742-6596/193/i=1/a=012040

[18] M. Faqir, T. Batten, T. Mrotzek, S. Knippscheer, M. Massiot, M. Buchta, H. Blanck, S. Rochette, O. Vendier, and M. Kuball, "Improved thermal management for GaN power electronics: Silver diamond composite packages," *Microelectronics Reliability*, vol. 52, no. 12, pp. 3022–3025, Dec. 2012. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271412003162

[19] T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress," *IEEE Transactions on Electron Devices*, vol. 50, no. 10, pp. 2015–2020, Oct. 2003.

[20] M. Faqir, M. Bouya, N. Malbert, N. Labat, D. Carisetti, B. Lambert, G. Verzellesi, and F. Fantini, "Analysis of current collapse effect in AlGaN/GaN HEMT: Experiments and numerical simulations," *Microelectronics Reliability*, vol. 50, no. 9–11, pp. 1520–1522, Sep. 2010. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271410002933

[21] J. Joh, J. A. d. Alamo, and J. Jimenez, "A Simple Current Collapse Measurement Technique for GaN High-Electron Mobility Transistors," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 665–667, Jul. 2008.

[22] J. Kuzmík, M. Ťapajna, L. Válik, M. Molnár, D. Donoval, C. Fleury, D. Pogany, G. Strasser, O. Hilt, F. Brunner, and J. Würfl, "Self-Heating in GaN Transistors Designed for High-Power Operation," *IEEE Transactions on Electron Devices*, vol. 61, no. 10, pp. 3429–3434, Oct. 2014.

[23] S. G. Khalil, S. Hardikar, S. Sack, E. Persson, M. Imam, and T. McDonald, "HV GaN reliability and status," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov. 2015, pp. 21–23.

[24] S. R. Bahl, D. Ruiz, and D. S. Lee, "Product-level reliability of GaN devices," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2016, pp. 4A–3–1–4A–3–6.

[25] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate," *Materials Science in Semiconductor Processing*, Oct. 2017.

[26] J. Wei, S. Liu, B. Li, X. Tang, Y. Lu, C. Liu, M. Hua, Z. Zhang, G. Tang, and K. J. Chen, "Low On-Resistance Normally-Off GaN Double-Channel Metal–Oxide–Semiconductor High-Electron-Mobility Transistor," *IEEE Electron Device Letters*, vol. 36, no. 12, pp. 1287–1290, Dec. 2015.

[27] A. Suzuki, S. Choe, Y. Yamada, S. Nagai, M. Hiraiwa, N. Otsuka, and D. Ueda, "Extremely low on-resistance enhancement-mode GaN-based HFET using Ge-doped regrowth technique," in *2014 IEEE International Electron Devices Meeting*, Dec. 2014, pp. 11.1.1–11.1.4.

[28] Z. Li, R. Chu, D. Zehnder, S. Khalil, M. Chen, X. Chen, and K. Boutros, "Improvement of the dynamic on-resistance characteristics of GaN-on-Si power transistors with a sloped field-plate," in *72nd Device Research Conference*, Jun. 2014, pp. 257–258.

[29] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. V. Hove, M. Germain, and G. Borghs, "Low On-Resistance High-Breakdown Normally Off AlN/GaN/AlGaN DHFET on Si Substrate," *IEEE Electron Device Letters*, vol. 31, no. 2, pp. 111–113, Feb. 2010.

[30] Huili Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates," *IEEE Electron Device*

Letters, vol. 25, no. 4, pp. 161–163, Apr. 2004, conference Name: IEEE Electron Device Letters.

[31] Y. Dora, A. Chakraborty, L. Mccarthy, S. Keller, S. P. Denbaars, and U. K. Mishra, "High Breakdown Voltage Achieved on AlGaN/GaN HEMTs With Integrated Slant Field Plates," *IEEE Electron Device Letters*, vol. 27, no. 9, pp. 713–715, Sep. 2006.

[32] T. Kabemura, S. Ueda, Y. Kawada, and K. Horio, "Enhancement of Breakdown Voltage in AlGaN/GaN HEMTs: Field Plate Plus High-k Passivation Layer and High Acceptor Density in Buffer Layer," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3848–3854, Sep. 2018.

[33] D. Kikuta, J. P. Ao, and Y. Ohno, "Gate leakage and electrical performance of AlGaN/GaN MIS-type HFET with evaporated silicon oxide layer," *Solid-State Electronics*, vol. 50, no. 3, pp. 316–321, Mar. 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110105003588

[34] E. Matioli and C. Weisbuch, "Active Region Part A. Internal Quantum Efficiency in LEDs," in *III-Nitride Based Light Emitting Diodes and Applications*, ser. Topics in Applied Physics, T.-Y. Seong, J. Han, H. Amano, and H. Morkoc, Eds. Springer Netherlands, 2013, no. 126, pp. 121–152. [Online]. Available: http://link.springer.com/chapter/10.1007/978-94-007-5863-6_6

[35] M. V. Hove, S. Boulay, S. R. Bahl, S. Stoffels, X. Kang, D. Wellekens, K. Geens, A. Delabie, and S. Decoutere, "CMOS Process-Compatible High-Power Low-Leakage AlGaN/GaN MISHEMT on Silicon," *IEEE Electron Device Letters*, vol. 33, no. 5, pp. 667–669, May 2012.

[36] B. Bakeroot, S. Stoffels, N. Posthuma, D. Wellekens, and S. Decoutere, "Trading Off between Threshold Voltage and Subthreshold Slope in AlGaN/GaN HEMTs with a p-GaN Gate," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2019, pp. 419–422, iSSN: 1946-0201.

[37] K. Ohi and T. Hashizume, "Drain Current Stability and Controllability of Threshold Voltage and Subthreshold Current in a Multi-Mesa-Channel AlGaN/GaN High Electron Mobility Transistor," *Japanese Journal of Applied Physics*, vol. 48, no. 8R, p. 081002, Aug. 2009, publisher: IOP Publishing. [Online]. Available: https://iopscience.iop.org/article/10.1143/JJAP.48.081002/meta

[38] D. Marcon, Y. N. Saripalli, and S. Decoutere, "200mm GaN-on-Si epitaxy and e-mode device technology," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2015, pp. 16.2.1–16.2.4, iSSN: 2156-017X.

[39] W. B. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," *Electronics Letters*, vol. 41, no. 7, pp. 449–450, Mar. 2005, conference Name: Electronics Letters.

[40] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-gate structure approach toward normally off high-Voltage AlGaN/GaN HEMT for power electronics applications," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 356–362, Feb. 2006, conference Name: IEEE Transactions on Electron Devices.

[41] T. Oka and T. Nozawa, "AlGaN/GaN Recessed MIS-Gate HFET With High-Threshold-Voltage Normally-Off Operation for Power Electronics Applications," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 668–670, Jul. 2008.

[42] S. Maroldt, C. Haupt, W. Pletschen, S. Müller, R. Quay, O. Ambacher, C. Schippel, and F. Schwierz, "Gate-Recessed AlGaN/GaN Based Enhancement-Mode High Electron Mobility Transistors for High Frequency Operation," *Japanese Journal of Applied Physics*, vol. 48, no. 4S, p. 04C083, Apr. 2009. [Online]. Available: http://iopscience.iop.org/article/10.1143/JJAP.48.04C083/meta

[43] Y. Wang, M. Wang, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, K. J. Chen, and B. Shen, "High-Performance Normally-Off Al2O3/GaN MOSFET Using a Wet Etching-Based Gate Recess Technique," *IEEE Electron Device Letters*, vol. 34, no. 11, pp. 1370–1372, Nov. 2013.

[44] Y. Cai, Y. Zhou, K. Lau, and K. Chen, "Control of Threshold Voltage of AlGaN/GaN HEMTs by Fluoride-Based Plasma Treatment: From Depletion Mode to Enhancement Mode," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2207–2215, Sep. 2006, conference Name: IEEE Transactions on Electron Devices.

[45] A. Lorenz, J. Derluyn, J. Das, K. Cheng, S. Degroote, F. Medjdoub, M. Germain, and G. Borghs, "Influence of thermal anneal steps on the current collapse of fluorine treated enhancement mode SiN/AlGaN/GaN HEMTs," *physica status solidi c*, vol. 6, no. S2, pp. S996–S998, 2009, _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/pssc.200880838. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssc.200880838

[46] Y. Zhang, M. Sun, S. J. Joglekar, and T. Palacios, "High threshold voltage in GaN MOS-HEMTs modulated by fluorine plasma and gate oxide," in *71st Device Research Conference*, Jun. 2013, pp. 141–142.

[47] Y. He, M. Mi, C. Wang, X. Zheng, M. Zhang, H. Zhang, J. Wu, L. Yang, P. Zhang, X. Ma, and Y. Hao, "Enhancement-mode AlGaN/GaN nanowire channel high electron mobility transistor with fluorine plasma treatment by ICP," *IEEE Electron Device Letters*, vol. PP, no. 99, pp. 1–1, 2017.

[48] L. Yang, B. Hou, M. Mi, Q. Zhu, M. Wu, J. Zhu, Y. Lu, M. Zhang, L. Chen, X. Zhou, L. Lv, X. Ma, and Y. Hao, "High-Performance Enhancement-Mode AlGaN/GaN High Electron Mobility Transistors Combined With TiN-Based Source Contact Ledge and Two-Step Fluorine Treatment," *IEEE Electron Device Letters*, vol. 39, no. 10, pp. 1544–1547, Oct. 2018.

[49] R. Wenzel, G. G. Fischer, and R. Schmid-Fetzer, "Ohmic contacts on p-GaN (Part I):: investigation of different contact metals and their thermal treatment," *Materials Science in Semiconductor Processing*, vol. 4, no. 4, pp. 357–365, Aug. 2001. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1369800100001773

[50] S.-I. Na, G.-Y. Ha, D.-S. Han, S.-S. Kim, J.-Y. Kim, J.-H. Lim, D.-J. Kim, K.-I. Min, and S.-J. Park, "Selective wet etching of p-GaN for efficient GaN-based light-emitting diodes," *IEEE Photonics Technology Letters*, vol. 18, no. 14, pp. 1512–1514, Jul. 2006.

[51] I. Hwang, J. Kim, H. S. Choi, H. Choi, J. Lee, K. Y. Kim, J.-B. Park, J. C. Lee, J. Ha, J. Oh, J. Shin, and U.-I. Chung, "p-GaN Gate HEMTs With Tungsten Gate Metal for High Threshold Voltage and Low Gate Current," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 202–204, Feb. 2013, conference Name: IEEE Electron Device Letters.

[52] F. Lee, L. Y. Su, C. H. Wang, Y. R. Wu, and J. Huang, "Impact of Gate Metal on the Performance of p-GaN/AlGaN/GaN High Electron Mobility Transistors," *IEEE Electron Device Letters*, vol. 36, no. 3, pp. 232–234, Mar. 2015.

[53] I. Rossetto, M. Meneghini, O. Hilt, E. Bahat-Treidel, C. D. Santi, S. Dalcanale, J. Wuerfl, E. Zanoni, and G. Meneghesso, "Time-Dependent Failure of GaN-on-Si Power HEMTs With p-GaN Gate," *IEEE Transactions on Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016.

[54] H. Jiang, R. Zhu, Q. Lyu, and K. M. Lau, "High-Voltage p-GaN HEMTs With OFF-State Blocking Capability After Gate Breakdown," *IEEE Electron Device Letters*, vol. 40, no. 4, pp. 530–533, Apr. 2019.

[55] B. Bakeroot, A. Stockman, N. Posthuma, S. Stoffels, and S. Decoutere, "Analytical Model for the Threshold Voltage of p -(Al)GaN High-Electron-Mobility Transistors," *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 79–86, Jan. 2018, conference Name: IEEE Transactions on Electron Devices.

[56] W. Zhang, X. Huang, F. C. Lee, and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Mar. 2014, pp. 1484–1489.

[57] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.

[58] W. Zhang, X. Huang, Z. Liu, F. C. Lee, S. She, W. Du, and Q. Li, "A New Package of High-Voltage Cascode Gallium Nitride Device for Megahertz Operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1344–1353, Feb. 2016.

[59] W. Du, X. Huang, F. C. Lee, Q. Li, and W. Zhang, "Avoiding divergent oscillation of cascode GaN device under high current turn-off condition," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 1002–1009.

[60] L. Katzir and D. Shmilovitz, "A 1-MHz 5-kV Power Supply Applying SiC Diodes and GaN HEMT Cascode MOSFETs in Soft Switching," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 4, pp. 1474–1482, Dec. 2016.

[61] J. Ren, C. Liu, C. W. Tang, K. M. Lau, and J. K. O. Sin, "A Novel Si #x2013;GaN Monolithic Integration Technology for a High-Voltage Cascoded Diode," *IEEE Electron Device Letters*, vol. 38, no. 4, pp. 501–504, Apr. 2017.

[62] Q. Zhou, L. Liu, A. Zhang, B. Chen, Y. Jin, Y. Shi, Z. Wang, W. Chen, and B. Zhang, "7.6 V Threshold Voltage High-Performance Normally-Off Al2O3/GaN MOSFET Achieved by Interface Charge Engineering," *IEEE Electron Device Letters*, vol. 37, no. 2, pp. 165–168, Feb. 2016.

[63] J. He, M. Hua, Z. Zhang, and K. J. Chen, "Performance andVTHStability in E-Mode GaN Fully Recessed MIS-FETs and Partially Recessed MIS-HEMTs With LPCVD-SiNx/PECVD-SiNxGate Dielectric Stack," *IEEE Transactions on Electron Devices*, vol. 65, no. 8, pp. 3185–3191, Aug. 2018.

[64] J. Kashiwagi, T. Fujiwara, M. Akutsu, N. Ito, K. Chikamatsu, and K. Nakahara, "Recessed-Gate Enhancement-Mode GaN MOSFETs With a Double-Insulator Gate Providing 10-MHz Switching Operation," *IEEE Electron Device Letters*, vol. 34, no. 9, pp. 1109–1111, Sep. 2013, conference Name: IEEE Electron Device Letters.

[65] M. Zhu, J. Ma, L. Nela, and E. Matioli, "High-performance normally-off tri-gate GaN power MOSFETs," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2019, pp. 71–74, iSSN: 1063-6854.

[66] G. Greco, F. Giannazzo, A. Frazzetto, V. Raineri, and F. Roccaforte, "Near-surface processing on AlGaN/GaN heterostructures: A nanoscale electrical and structural characterization," *Nanoscale research letters*, vol. 6, p. 132, Feb. 2011.

[67] K. J. Chen and C. Zhou, "Enhancement-mode AlGaN/GaN HEMT and MIS-HEMT technology," *physica status solidi (a)*, vol. 208, no. 2, pp. 434–438, 2011, _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/pssa.201000631. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssa.201000631

[68] H. Mizuno, S. Kishimoto, K. Maezawa, and T. Mizutani, "Quasi-normally-off AlGaN/GaN HEMTs fabricated by fluoride-based plasma treatment," *physica status solidi c*, vol. 4, no. 7, pp. 2732–2735, 2007, _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/pssc.200674859. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssc.200674859

[69] A. Endoh, Y. Yamashita, K. Ikeda, M. Higashiwaki, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, "Non-Recessed-Gate Enhancement-Mode AlGaN/GaN High Electron Mobility Transistors with High RF Performance," *Japanese Journal of Applied Physics*, vol. 43, no. 4S, p. 2255, Apr. 2004, publisher: IOP Publishing. [Online]. Available: https://iopscience.iop.org/article/10.1143/JJAP.43.2255/meta

[70] T. Palacios, C. Suh, A. Chakraborty, S. Keller, S. P. DenBaars, and U. K. Mishra, "High-performance E-mode AlGaN/GaN HEMTs," *IEEE Electron Device Letters*, vol. 27, no. 6, pp. 428–430, Jun. 2006, conference Name: IEEE Electron Device Letters.

[71] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3393–3399, Dec. 2007, conference Name: IEEE Transactions on Electron Devices.

[72] Y. Shi, Q. Zhou, Q. Cheng, P. Wei, L. Zhu, D. Wei, A. Zhang, W. Chen, and B. Zhang, "Carrier Transport Mechanisms Underlying the Bidirectional VTH Shift in p-GaN Gate HEMTs Under Forward Gate Stress," *IEEE Transactions on Electron Devices*, pp. 1–7, 2018.

[73] S. A. Smith, W. V. Lampert, P. Rajagopal, A. D. Banks, D. Thomson, and R. F. Davis, "Selective etching of GaN over AlN using an inductively coupled plasma and an O2/Cl2/Ar chemistry," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 18, no. 3, pp. 879–881, May 2000. [Online]. Available: http://avs.scitation.org/doi/abs/10.1116/1.582270

[74] Y. Han, S. Xue, W. Guo, Y. Luo, Z. Hao, and C. Sun, "Highly Selective Dry Etching of GaN over AlGaN Using Inductively Coupled Cl2/N2/O2 Plasmas," *Japanese Journal of Applied Physics*, vol. 42, no. 10A, p. L1139, Sep. 2003. [Online]. Available: http://iopscience.iop.org/article/10.1143/JJAP.42.L1139/meta

[75] Y. Zhong, Y. Zhou, H. Gao, S. Dai, J. He, M. Feng, Q. Sun, J. Zhang, Y. Zhao, A. DingSun, and H. Yang, "Self-terminated etching of GaN with a high selectivity over AlGaN under inductively coupled Cl2/N2/O2 plasma with a low-energy ion bombardment," *Applied Surface Science*, vol. 420, pp. 817–824, Oct. 2017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0169433217315416

[76] G. Lükens, H. Hahn, H. Kalisch, and A. Vescan, "Self-Aligned Process for Selectively Etched p-GaN-Gated AlGaN/GaN-on-Si HFETs," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3732–3738, Sep. 2018.

[77] Y. Zhou, Y. Zhong, H. Gao, S. Dai, J. He, M. Feng, Y. Zhao, Q. Sun, A. Dingsun, and H. Yang, "p-GaN Gate Enhancement-Mode HEMT Through a High Tolerance Self-Terminated Etching Process," *IEEE Journal of the Electron Devices Society*, vol. 5, no. 5, pp. 340–346, Sep. 2017.

[78] S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, H. Okita, T. Morita, K. Tanaka, M. Hikita, Y. Uemoto, S. Takahashi, and T. Ueda, "Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 41–44, iSSN: 1946-0201.

[79] "Transfer printing and self-aligned etching for E-mode GaN transistors," Aug. 2020. [Online]. Available: http://www.ivwkr.com/transfer-printing-and-self-aligned-etching-for-e-mode-gan-transistors/

[80] M. Murphy, "Cascode circuit employing a depletion-mode, GaN-based FET," US Patent US7 501 670B2, Mar., 2009. [Online]. Available: https://patents.google.com/patent/US7501670B2/en

[81] Y. Cai, Z. Cheng, W. C. W. Tang, K. M. Lau, and K. J. Chen, "Monolithically Integrated Enhancement/Depletion-Mode AlGaN/GaN HEMT Inverters and Ring Oscillators Using$hboxCF_4$Plasma Treatment," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2223–2230, Sep. 2006.

[82] B. Wang, M. Riva, J. D. Bakos, and A. Monti, "Integrated Circuit Implementation for a GaN HFET Driver Circuit," *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 2056–2067, Sep. 2010.

[83] H. Hahn, B. Reuters, S. Kotzea, G. Lükens, S. Geipel, H. Kalisch, and A. Vescan, "First monolithic integration of GaN-based enhancement mode n-channel and p-channel heterostructure field effect transistors," in *72nd Device Research Conference*, Jun. 2014, pp. 259–260.

[84] R. Chu, Y. Cao, M. Chen, R. Li, and D. Zehnder, "An Experimental Demonstration of GaN CMOS Technology," *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 269–271, Mar. 2016.

[85] Y. Cai, Z. Cheng, Z. Yang, C. W. Tang, K. M. Lau, and K. J. Chen, "High-Temperature Operation of AlGaN/GaN HEMTs Direct-Coupled FET Logic (DCFL) Integrated Circuits," *IEEE Electron Device Letters*, vol. 28, no. 5, pp. 328–331, May 2007.

[86] A. L. Corrion, K. Shinohara, D. Regan, Y. Tang, D. Brown, J. F. Robinson, H. H. Fung, A. Schmitz, D. Le, S. J. Kim, T. C. Oh, and M. Micovic, "High-Speed 501-Stage DCFL GaN Ring Oscillator Circuits," *IEEE Electron Device Letters*, vol. 34, no. 7, pp. 846–848, Jul. 2013.

[87] Y. Kong, J. Zhou, C. Kong, Y. Zhang, X. Dong, H. Lu, T. Chen, and N. Yang, "Monolithic Integration of E/D-Mode AlGaN/GaN MIS-HEMTs," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 336–338, Mar. 2014.

[88] Z. Xu, J. Wang, Y. Cai, J. Liu, Z. Yang, X. Li, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, J. Zhang, and Y. Hao, "High Temperature Characteristics of GaN-Based Inverter Integrated With Enhancement-Mode (E-Mode) MOSFET and Depletion-Mode (D-Mode) HEMT," *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 33–35, Jan. 2014.

[89] G. Tang, A. M. H. Kwan, R. K. Y. Wong, J. Lei, R. Y. Su, F. W. Yao, Y. M. Lin, J. L. Yu, T. Tsai, H. C. Tuan, A. Kalnitsky, and K. J. Chen, "Digital Integrated Circuits on an

E-Mode GaN Power HEMT Platform," *IEEE Electron Device Letters*, vol. 38, no. 9, pp. 1282–1285, Sep. 2017.

[90] Z. Xu, J. Wang, J. Liu, C. Jin, Y. Cai, Z. Yang, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, J. Zhang, and Y. Hao, "Demonstration of Normally-Off Recess-Gated AlGaN/GaN MOSFET Using GaN Cap Layer as Recess Mask," *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1197–1199, Dec. 2014.

[91] X. Yong and B. Paul, "Optimizing GaN performance with an integrated driver," Texas Instruments, High-voltage power solution slyy085, Mar. 2016.

[92] S. Mönch, M. Costa, A. Barner, I. Kallfass, R. Reiner, B. Weiss, P. Waltereit, R. Quay, and O. Ambacher, "Quasi-normally-off GaN gate driver for high slew-rate d-mode GaN-on-Si HEMTs," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 373–376.

[93] D. Maksimovic, "Monolithic High Frequency GaN Switched-Mode Power Converters," UC Berkeley, Feb. 2016. [Online]. Available: http://power.eecs.berkeley.edu/pels/seminars/GaNswitchers_DMaksimovic_UCB_Feb2016

[94] B. M. Green, V. Tilak, S. Lee, H. Kim, J. A. Smart, K. J. Webb, J. R. Shealy, and L. F. Eastman, "High-power broad-band AlGaN/GaN HEMT MMICs on SiC substrates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 12, pp. 2486–2493, Dec. 2001.

[95] M. Garven and J. P. Calame, "Simulation and Optimization of Gate Temperatures in GaN-on-SiC Monolithic Microwave Integrated Circuits," *IEEE Transactions on Components and Packaging Technologies*, vol. 32, no. 1, pp. 63–72, Mar. 2009.

[96] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1764–1783, Jun. 2012.

[97] R. Perrin, B. Allard, C. Buttay, N. Quentin, W. Zhang, R. Burgos, D. Boroyevic, P. Preciat, and D. Martineau, "2 MHz high-density integrated power supply for gate driver in high-temperature applications," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 524–528.

[98] R. J. Bayruns, R. L. Johnston, D. L. Fraser, and S. C. Fang, "Delay analysis of Si NMOS Gbit/s logic circuits," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 5, pp. 755–754, Oct. 1984.

[99] M. Zhu, J. Ma, L. Nela, C. Erine, and E. Matioli, "High-voltage normally-off recessed tri-gate GaN power MOSFETs with low on-resistance," *IEEE Electron Device Letters*, pp. 1–1, 2019.

[100] M. Zhu, J. Ma, and E. Matioli, "Investigation of p-GaN tri-Gate normally-Off GaN Power MOSHEMTs," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Sep. 2020, pp. 345–348, iSSN: 1946-0201.

[101] M. Zhu, C. Erine, J. Ma, M. S. Nikoo, L. Nela, P. Sohi, and E. Matioli, "P-GaN Tri-Gate MOS structure for Normally-Off GaN Power Transistors," *IEEE Electron Device Letters*, pp. 1–1, 2020, conference Name: IEEE Electron Device Letters.

[102] M. Zhu and E. Matioli, "Monolithic integration of GaN-based NMOS digital logic gate circuits with E-mode power GaN MOSHEMTs," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2018, pp. 236–239.

[103] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *2012 Symposium on VLSI Technology (VLSIT)*, Jun. 2012, pp. 131–132, iSSN: 2158-9682.

[104] Y. Ma, M. Xiao, Z. Du, X. Yan, K. Cheng, M. Clavel, M. K. Hudait, I. Kravchenko, H. Wang, and Y. Zhang, "Tri-gate GaN junction HEMT," *Applied Physics Letters*, vol. 117, no. 14, p. 143506, Oct. 2020, publisher: American Institute of Physics. [Online]. Available: https://aip.scitation.org/doi/full/10.1063/5.0025351

[105] J. Singh, A. Bousquet, J. Ciavatti, K. Sundaram, J. S. Wong, K. W. Chew, A. Bandyopadhyay, S. Li, A. Bellaouar, S. M. Pandey, B. Zhu, A. Martin, C. Kyono, J. Goo, H. S. Yang, A. Mehta, X. Zhang, O. Hu, S. Mahajan, E. Geiss, S. Yamaguchi, S. Mittal, R. Asra, P. Balasubramaniam, J. Watts, D. Harame, R. M. Todi, S. B. Samavedam, and D. K. Sohn, "14nm FinFET technology for analog and RF applications," in *2017 Symposium on VLSI Technology*, Jun. 2017, pp. T140–T141, iSSN: 2158-9682.

[106] P. Zheng, D. Connelly, F. Ding, and T. K. Liu, "FinFET Evolution Toward Stacked-Nanowire FET for CMOS Technology Scaling," *IEEE Transactions on Electron Devices*, vol. 62, no. 12, pp. 3945–3950, Dec. 2015, conference Name: IEEE Transactions on Electron Devices.

[107] H. C. Lo, D. Choi, Y. Hu, Y. Shen, Y. Qi, J. Peng, D. Zhou, M. Mohan, C. Yong, H. Zhan, H. Wei, X. He, D. Kang, A. Sirman, Y. Wang, H. Zang, S. Y. Mun, A. Vinslava, W. H. Chen, C. Gaire, J. Liu, X. Dou, Y. Shi, P. Zhao, B. Zhu, A. Jha, X. Zhang, X. Wan, E. Lavigne, C. Kyono, M. Togo, J. Versaggi, H. Yu, O. Hu, J. G. Lee, S. B. Samavedam, and D. K. Sohn, "A 12nm FinFET Technology Featuring 2nd Generation FinFET for Low Power and High Performance Applications," in *2018 IEEE Symposium on VLSI Technology*, Jun. 2018, pp. 215–216, iSSN: 2158-9682.

[108] J. Ma and E. Matioli, "High Performance Tri-Gate GaN Power MOSHEMTs on Silicon Substrate," *IEEE Electron Device Letters*, vol. 38, no. 3, pp. 367–370, Mar. 2017.

[109] ——, "High-Voltage and Low-Leakage AlGaN/GaN Tri-Anode Schottky Diodes With Integrated Tri-Gate Transistors," *IEEE Electron Device Letters*, vol. 38, no. 1, pp. 83–86, Jan. 2017.

[110] D. F. Brown, Y. Tang, D. Regan, J. Wong, and M. Micovic, "Self-Aligned AlGaN/GaN FinFETs," *IEEE Electron Device Letters*, vol. 38, no. 10, pp. 1445–1448, Oct. 2017.

[111] S. Liu, Y. Cai, G. Gu, J. Wang, C. Zeng, W. Shi, Z. Feng, H. Qin, Z. Cheng, K. J. Chen, and B. Zhang, "Enhancement-Mode Operation of Nanochannel Array (NCA) AlGaN/GaN HEMTs," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 354–356, Mar. 2012, conference Name: IEEE Electron Device Letters.

[112] T. Tamura, J. Kotani, S. Kasai, and T. Hashizume, "Nearly Temperature-Independent Saturation Drain Current in a Multi-Mesa-Channel AlGaN/GaN High Electron Mobility Transistor," *Applied Physics Express*, vol. 1, no. 2, p. 023001, Feb. 2008, publisher: IOP Publishing. [Online]. Available: https://iopscience.iop.org/article/10.1143/APEX.1.023001/meta

[113] L. Nela, M. Zhu, J. Ma, and E. Matioli, "High-Performance Nanowire-Based E-Mode Power GaN MOSHEMTs With Large Work-Function Gate Metal," *IEEE Electron Device Letters*, vol. 40, no. 3, pp. 439–442, Mar. 2019.

[114] B. Lu, E. Matioli, and T. Palacios, "Tri-Gate Normally-Off GaN Power MISFET," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 360–362, Mar. 2012.

[115] J. Ma, G. Santoruvo, L. Nela, T. Wang, and E. Matioli, "Impact of Fin Width on Tri-Gate GaN MOSHEMTs," *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 4068–4074, Sep. 2019, conference Name: IEEE Transactions on Electron Devices.

[116] K. Ohi, J. T. Asubar, K. Nishiguchi, and T. Hashizume, "Current Stability in Multi-Mesa-Channel AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 2997–3004, Oct. 2013.

[117] M. Azize and T. Palacios, "Top-down fabrication of AlGaN/GaN nanoribbons," *Applied Physics Letters*, vol. 98, no. 4, p. 042103, Jan. 2011. [Online]. Available: https://aip.scitation.org/doi/10.1063/1.3544048

[118] E. Ertekin, P. A. Greaney, D. C. Chrzan, and T. D. Sands, "Equilibrium limits of coherency in strained nanowire heterostructures," *Journal of Applied Physics*, vol. 97, no. 11, p. 114325, Jun. 2005, publisher: American Institute of Physics. [Online]. Available: https://aip.scitation.org/doi/full/10.1063/1.1903106

[119] R. Coffie, "Analytical Field Plate Model for Field Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 3, pp. 878–883, Mar. 2014.

[120] ——, "Slant Field Plate Model for Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2867–2872, Aug. 2014.

[121] S. Karmalkar, M. S. Shur, G. Simin, and M. A. Khan, "Field-plate engineering for HFETs," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2534–2540, Dec. 2005.

[122] H. Onodera and K. Horio, "Physics-based simulation of field-plate effects on breakdown characteristics in AlGaN/GaN HEMTs," in *2012 7th European Microwave Integrated Circuit Conference*, Oct. 2012, pp. 401–404.

[123] H.-T. Kwak, S.-B. Chang, H.-J. Kim, K.-W. Jang, H. S. Yoon, S.-H. Lee, J.-W. Lim, and H.-S. Kim, "Operational Improvement of AlGaN/GaN High Electron Mobility Transistor by an Inner Field-Plate Structure," *Applied Sciences*, vol. 8, no. 6, p. 974, Jun. 2018. [Online]. Available: https://www.mdpi.com/2076-3417/8/6/974

[124] J. Ma and E. Matioli, "Slanted Tri-Gates for High-Voltage GaN Power Devices," *IEEE Electron Device Letters*, vol. 38, no. 9, pp. 1305–1308, Sep. 2017.

[125] J. Ma, G. Santoruvo, P. Tandon, and E. Matioli, "Enhanced Electrical Performance and Heat Dissipation in AlGaN/GaN Schottky Barrier Diodes Using Hybrid Tri-anode Structure," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3614–3619, Sep. 2016.

[126] S. Takashima, Z. Li, and T. P. Chow, "Sidewall Dominated Characteristics on Fin-Gate AlGaN/GaN MOS-Channel-HEMTs," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3025–3031, Oct. 2013, conference Name: IEEE Transactions on Electron Devices.

[127] D.-H. Son, Y.-W. Jo, V. Sindhuri, K.-S. Im, J. H. Seo, Y. T. Kim, I. M. Kang, S. Cristoloveanu, M. Bawedin, and J.-H. Lee, "Effects of sidewall MOS channel on performance of AlGaN/GaN FinFET," *Microelectronic Engineering*, vol. 147, pp. 155–158, Nov. 2015. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931715003457

[128] Y. Xu, S. Cristoloveanu, M. Bawedin, K. Im, and J. Lee, "Performance Improvement and Sub-60 mV/Decade Swing in AlGaN/GaN FinFETs by Simultaneous Activation of 2DEG and Sidewall MOS Channels," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 915–920, Mar. 2018, conference Name: IEEE Transactions on Electron Devices.

[129] C. Yadav, P. Kushwaha, S. Khandelwal, J. P. Duarte, Y. S. Chauhan, and C. Hu, "Modeling of GaN-Based Normally-Off FinFET," *IEEE Electron Device Letters*, vol. 35, no. 6, pp. 612–614, Jun. 2014, conference Name: IEEE Electron Device Letters.

[130] B. Lu, O. I. Saadat, and T. Palacios, "High-Performance Integrated Dual-Gate AlGaN/GaN Enhancement-Mode Transistor," *IEEE Electron Device Letters*, vol. 31, no. 9, pp. 990–992, Sep. 2010.

[131] Z. Li, H. Naik, and T. P. Chow, "Modeling and experimental study of MOS channel mobility of etched GaN on silicon substrate," *physica status solidi c*, vol. 8, no. 7-8, pp. 2433–2435, 2011, _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/pssc.201001172. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssc.201001172

[132] K. Tang, W. Huang, and T. P. Chow, "GaN MOS Capacitors and FETs on Plasma-Etched GaN Surfaces," *Journal of Electronic Materials*, vol. 38, no. 4, pp. 523–528, Apr. 2009. [Online]. Available: https://doi.org/10.1007/s11664-008-0617-y

[133] G. Zhu, Y. Wang, Q. Xin, M. Xu, X. Chen, X. Xu, X. Feng, and A. Song, "GaN metal-oxide-semiconductor high-electron-mobility transistors using thermally evaporated SiO as the gate dielectric," *Semiconductor Science and Technology*, vol. 33, no. 9, p. 095023, Aug. 2018, publisher: IOP Publishing. [Online]. Available: https://doi.org/10.1088%2F1361-6641%2Faad8d7

[134] J. Ma, M. Zhu, and E. Matioli, "900 V Reverse-Blocking GaN-on-Si MOSHEMTs With a Hybrid Tri-Anode Schottky Drain," *IEEE Electron Device Letters*, vol. 38, no. 12, pp. 1704–1707, Dec. 2017.

[135] J. Ma and E. Matioli, "2kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current," *Applied Physics Letters*, vol. 112, no. 5, p. 052101, Jan. 2018. [Online]. Available: http://aip.scitation.org/doi/abs/10.1063/1.5012866

[136] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of Dynamic On-Resistance Increase and Gate Charge Measurements in High-Voltage GaN-HEMTs With Optimized Field-Plate Structure," *IEEE Transactions on Electron Devices*, vol. 54, no. 8, pp. 1825–1830, Aug. 2007.

[137] M. T. Hasan, T. Asano, H. Tokuda, and M. Kuzuhara, "Current Collapse Suppression by Gate Field-Plate in AlGaN/GaN HEMTs," *IEEE Electron Device Letters*, vol. 34, no. 11, pp. 1379–1381, Nov. 2013.

[138] Z. Xu, J. Wang, Y. Liu, J. Cai, J. Liu, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, and J. Zhang, "Fabrication of Normally Off AlGaN/GaN MOSFET Using a Self-Terminating Gate Recess Etching Technique," *IEEE Electron Device Letters*, vol. 34, no. 7, pp. 855–857, Jul. 2013.

[139] M. Hua, Z. Zhang, J. Wei, J. Lei, G. Tang, K. Fu, Y. Cai, B. Zhang, and K. J. Chen, "Integration of LPCVD-SiNxgate dielectric with recessed-gate E-mode GaN MIS-FETs: Toward high performance, high stability and long TDDB lifetime," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, pp. 10.4.1–10.4.4.

[140] O. Landré, D. Camacho, C. Bougerol, Y. M. Niquet, V. Favre-Nicolin, G. Renaud, H. Renevier, and B. Daudin, "Elastic strain relaxation in GaN/AlN nanowire superlattice," *Physical Review B*, vol. 81, no. 15, p. 153306, Apr. 2010. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.81.153306

[141] K. Im, C. Won, Y. Jo, J. Lee, M. Bawedin, S. Cristoloveanu, and J. Lee, "High-Performance GaN-Based Nanochannel FinFETs With/Without AlGaN/GaN Heterostructure," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3012–3018, Oct. 2013.

[142] C. Tang and J. Shi, "Effects of passivation on breakdown voltage and leakage current of normally-off InAlN/GaN MISHFETs—a simulation study," *Semiconductor Science and Technology*, vol. 29, no. 12, p. 125004, Oct. 2014. [Online]. Available: https://doi.org/10.1088%2F0268-1242%2F29%2F12%2F125004

[143] H. Hanawa, H. Onodera, A. Nakajima, and K. Horio, "Numerical Analysis of Breakdown Voltage Enhancement in AlGaN/GaN HEMTs With a High-k Passivation Layer," *IEEE Transactions on Electron Devices*, vol. 61, no. 3, pp. 769–775, Mar. 2014.

[144] M. Meneghini, I. Rossetto, V. Rizzato, S. Stoffels, M. V. Hove, N. Posthuma, T.-L. Wu, D. Marcon, S. Decoutere, G. Meneghesso, and E. Zanoni, "Gate Stability of GaN-Based HEMTs with P-Type Gate," *Electronics*, Mar. 2016. [Online]. Available: https://scinapse.io/papers/2311509203

[145] M. Meneghini, O. Hilt, J. Würfl, and G. Meneghesso, "Technology and Reliability of Normally-Off GaN HEMTs with p-Type Gate," 2017.

[146] K. Tanaka, H. Umeda, H. Ishida, M. Ishida, and T. Ueda, "Effects of hole traps on the temperature dependence of current collapse in a normally-OFF gate-injection transistor," *Japanese Journal of Applied Physics*, vol. 55, no. 5, p. 054101, Apr. 2016, publisher: IOP Publishing. [Online]. Available: https://iopscience.iop.org/article/10.7567/JJAP.55.054101/meta

[147] T.-L. Wu, D. Marcon, S. You, N. Posthuma, B. Bakeroot, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere, "Forward Bias Gate Breakdown Mechanism in Enhancement-Mode p-GaN Gate AlGaN/GaN High-Electron Mobility Transistors," *IEEE Electron Device Letters*, vol. 36, no. 10, pp. 1001–1003, Oct. 2015, conference Name: IEEE Electron Device Letters.

[148] M. Ťapajna, O. Hilt, E. Bahat-Treidel, J. Würfl, and J. Kuzmík, "Gate Reliability Investigation in Normally-Off p-Type-GaN Cap/AlGaN/GaN HEMTs Under Forward Bias Stress," *IEEE Electron Device Letters*, vol. 37, no. 4, pp. 385–388, Apr. 2016, conference Name: IEEE Electron Device Letters.

[149] M. I. Elmasry, "Multidrain NMOS for VLSI logic design," *IEEE Transactions on Electron Devices*, vol. 29, no. 4, pp. 779–781, Apr. 1982.

[150] ——, "Nanosecond NMOS VLSI current mode logic," *IEEE Transactions on Electron Devices*, vol. 29, no. 4, pp. 781–784, Apr. 1982.

[151] T. Mimura, S. Hiyamizu, K. Joshin, and K. Hikosaka, "Enhancement-Mode High Electron Mobility Transistors for Logic Applications," *Japanese Journal*

of Applied Physics, vol. 20, no. 5, p. L317, May 1981. [Online]. Available: http://iopscience.iop.org/article/10.1143/JJAP.20.L317/meta

[152] A. S. Sedra and K. C. Smith, *Microelectronic Circuits (The Oxford Series in Electrical and Computer Engineering) 7th edition*, 7th ed. New York ; Oxford: Oxford University Press, Nov. 2014.

[153] M. H. Rashid, *Microelectronic Circuits: Analysis & Design*, 2nd ed. Stamford, CT: CL Engineering, Apr. 2010.

[154] S. Nakamura, T. Mukai, M. Senoh, and N. Iwasa, "Thermal Annealing Effects on P-Type Mg-Doped GaN Films," *Japanese Journal of Applied Physics*, vol. 31, no. 2B, p. L139, Feb. 1992, publisher: IOP Publishing. [Online]. Available: https://iopscience.iop.org/article/10.1143/JJAP.31.L139/meta

MINGHUA ZHU

School of Electrical Engineering
École Polytechnique Fédérale de Lausanne
Lausanne,1015, Switzerland

☞ Gender: Male
✉ E-mail: minghua.zhu@epfl.ch
☎ Mobile: +41789206005

EDUCATION

School of Electrical Engineering, École Polytechnique Fédérale de Lausanne, Switzerland Jan. 2016 - Now
- PhD Candidate in Electrical Engineering

School of Electrical Engineering, Xi'an Jiaotong University, China Sep. 2012 - June. 2015
- M.Eng., in Electrical Engineering

School of Electrical Engineering, Xi'an Jiaotong University, China Sep. 2008 - Jul. 2012
- B.Eng., Electrical Engineering & Automation

RESEARCH EXPERIENCES

Research Areas of Interest: Power Semiconductor Devices, GaN Power Devices Fabrication and Characterization, Power Electronics, Renewable Energy Systems

PhD Candidate, Power and Wideband-gap Electronics Research Laboratory (POWERLAB), École Polytechnique Fédérale de Lausanne, Switzerland Jan. 2017 - Present
Project title: Growth and Optimization of pGaN or alternative layers over tri-gate structures for high performance Normally-off GaN transistors
Supervisor: Prof. Elison Matioli
- Supported by **ECSEL Joint Undertaking (JU) under grant agreement NO.826392. The JU receives support from the European Union's Horizon 2020 research and innovation programme.**.
- Demonstrated excellent results with gate recess combined with tri-gate: 2kV normally-off tri-gate devices
- Demonstrated p-GaN tri-gate MOSHEMT for normally-off operation
- Demonstrated normally-off nanostructured transistors with large work-function gate metal (cooperated with another PhD)
- Investigation of alternative deposition methods and new materials (sputtering, PLD, ALD)
- Epitaxial growth of pGaN by MOCVD or MBE over tri-gates (cooperated with another Posdoc for regrowth)

PhD Candidate, Power and Wideband-gap Electronics Research Laboratory (POWERLAB), École Polytechnique Fédérale de Lausanne, Switzerland Jan. 2016 - Dec. 2017
Project title: Monolithic Integration of Gate Driver and GaN Power Devices for High-frequency Power Switches
Supervisor: Prof. Elison Matioli
- Supported by **European Space Agency and Swiss Space Center**.
- Designed and fabricated the monolithic integration of gate driver and GaN power devices for high-frequency power switches.
- Investigated the development of GaN gate logic circuits in the driving circuits.
- Tested and characterized the GaN based logic circuits and voltage source driver circuits.

Graduate student, Power Electronics and Renewable Energy Research Center (PEREC), Xi'an Jiaotong University, China Oct. 2012 - July. 2015
Project title: Research on Key Technologies of Coordinated Control for Large-scale Intermittent Generation Integrated to Power System

Supervisor: Prof. Fang Zhuo

- Supported by **National High-tech R&D Program of China (863 Program)**.
- Established the mathematical model of a single-machine infinite-bus power system integrated with a PV generation plant.
- Investigated the control strategy of high penetration PV system on suppressing low-frequency oscillations in power system.
- Conducted the simulation and Hardware-in-the-Loop (HiL) experiment based on MATLAB/Simulink and RTLAB/DSP28335 respectively.

Graduate student, Fujian Cee Installations Co., Ltd, Fu Jian, China Dec. 2012 - May. 2013
Project title: Power Factor Correction and Harmonic Elimination Based on 450kVA STATCOM
Supervisor: Prof. Fang Zhuo

- Established the MATLAB/Simulink simulation model and figured out the control strategy.
- Designed the DSP control board with Altium Designer and debugged it with Code Composer Studio (CCS).
- Designed and debugged a prototype.

Undergraduate Researcher, Solar Electric Vehicle Team, Xi'an Jiaotong University, China Sept. 2010 - May. 2012
Supervisor: Prof. Jing Wang

- **Group leader** of Energy and Control group.
- Participated in designing the first hybrid solar electric vehicle of XJTU.
- Focused on design and control method of hybrid energy-storage system of solar vehicle.
- Had a deep understanding of bi-directional DC/DC circuit, storage battery and super-capacitor.

Undergraduate Researcher, The National Undergraduate Innovative Experiment Program, Xi'an Jiaotong University, China Otc. 2010 - Jul. 2012
Project title: Research on Management Strategy for Hybrid Energy System in Solar Car
Supervisor: Prof. Yi Wu

- **Team leader** of the project.
- Proposed the energy management control algorithm of hybrid energy storage system.
- Proposed a novel control method for bi-directional DC/DC circuit to keep the battery discharging current within a certain limit and make full use of super-capacitor.
- Rated **excellent** during the project evaluation (3/63).

Contemporary Undergraduate Mathematical Contest in Modeling (CUMCM) Mar. 2009 - Sept. 2009
Supervisor: Associate Prof. Wei Wang

- **Team leader** among three students.
- Studied linear and nonlinear programming, regression analysis and variance analysis, ordinary differential equations and stability theory, optimization theory, multi-objective decision, queuing theory, neural network theory etc.

PUBLICATIONS & PATENTS

- **M. Zhu**, J. Ma, and E. Matioli,"High performance tri-gate GaN logic gates," ***IEEE Electron Device Letters*** (under review).
- **M. Zhu**, C, Erine, J. Ma, M.S. Nikoo, L. Nela, P. Sohi and E. Matioli,"P-GaN Tri-Gate MOS structure for Normally-Off GaN Power Transistors," ***IEEE Electron Device Letters***, Vol. 1, No.1,pp 1-1,2020.
- J. Ma, C. Erine, **M. Zhu**, N. Luca, P. Xiang, K. Cheng, and E. Matioli, 1200 V Multi-Channel Power Devices with 2.8 mm ON-Resistance, in 2019 IEEE International Electron Devices Meeting (***IEDM***), Dec. 2019, p. 4.1.1-4.1.4.
- M. Samizadeh, A. Jafari, N. Perera, **M. Zhu**, G. Santoruvo, E. Matioli, "Nanoplasma-Enabled Picosecond Switches for Ultra-Fast Electronics", ***Nature***, vol. 579, no. 7800, pp. 534539, Mar. 2020, doi: 10.1038/s41586-020-2118-y.
- **M. Zhu**, J. Ma, and E. Matioli,"P-GaN tri-Gate normally-Off GaN Power MOSHEMTs," in 2020

32st International Symposium on Power Semiconductor Devices and ICs (***ISPSD 2020***), May 2020, Vienna .

- **M. Zhu**, J. Ma, L. Nela, C. Erine, and E. Matioli, High-voltage normally-off recessed tri-gate GaN power MOSFETs with low on-resistance, ***IEEE Electron Device Letters***, pp. 11, 2019.
- L. Nela, **M. Zhu**, J. Ma, and E. Matioli, High-performance nanowire-based E-mode Power GaN MOSHEMTs, in 2019 Compound Semiconductor Week (***CSW 2019***), May 2019, Japan.
- **M. Zhu**, J. Ma, L. Nela, and E. Matioli, High-performance normally-off tri-gate GaN power MOSFETs, in 2019 31st International Symposium on Power Semiconductor Devices and ICs (***ISPSD 2019***), May 2019, pp. 7174, Shanghai.
- L. Nela, **M. Zhu**, J. Ma, and E. Matioli, High-Performance Nanowire-Based E-Mode Power GaN MOSHEMTs With Large Work-Function Gate Metal, ***IEEE Electron Device Letters***, vol. 40, no. 3, pp. 439442, Mar. 2019.
- **M. Zhu** and E. Matioli, Monolithic integration of GaN-based NMOS digital logic gate circuits with E-mode power GaN MOSHEMTs, in 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (***ISPSD 2018***), May 2018, pp. 236239.
- J. Ma, **M. Zhu**, and E. Matioli, 900 V Reverse-Blocking GaN-on-Si MOSHEMTs With a Hybrid Tri-Anode Schottky Drain, ***IEEE Electron Device Letters***, vol. 38, no. 12, pp. 17041707, Dec. 2017.
- L. Xiong, F. Zhuo, F. Wang, X. Liu, **M. Zhu**, and H. Yi, A Novel Fast Open-loop Phase Locking Scheme Based on Synchronous Reference Frame for Three-phase Non-ideal Power Grids, ***Journal of Power Electronics***, vol. 16, no. 4, pp. 15131525, 2016.
- L. Xiong, F. Zhuo, F. Wang, X. Liu, **M. Zhu**, and H. Yi, A Quantitative Evaluation and Comparison of Harmonic Elimination Algorithms Based on Moving Average Filter and Delayed Signal Cancellation in Phase Synchronization Applications, ***Journal of Power Electronics***, vol. 16, no. 2, pp. 717730, 2016.
- L. Xiong, F. Zhuo, F. Wang, X. Liu, Y. Chen, **M. Zhu**, and H. Yi, Static Synchronous Generator Model: A New Perspective to Investigate Dynamic Characteristics and Stability Issues of Grid-Tied PWM Inverter, ***IEEE Transactions on Power Electronics***, vol. 31, no. 9, pp. 62646280, Sep. 2016.
- L. Xiong, F. Zhuo, F. Wang, X. Liu, and **M. Zhu**, A Fast Orthogonal Signal-Generation Algorithm Characterized by Noise Immunity and High Accuracy for Single-Phase Grid, ***IEEE Transactions on Power Electronics***, vol. 31, no. 3, pp. 18471851, Mar. 2016.
- L. Xiong, F. Zhuo, X. Liu, **M. Zhu**, Y. Chen, and F. Wang, Research on fast open-loop phase locking scheme for three-phase unbalanced grid, in 2015 IEEE Applied Power Electronics Conference and Exposition (***APEC 2015***), Mar. 2015, pp. 16721676.
- **M. Zhu**, C. Li, J. Huang, F. Zhuo*, L. Xiong, B. Liu, H. Zhang. "A Novel Method for Modeling of DC Micro-grid Based on Characteristic Parameter," ***APEC 2014***, Fort Worth, USA.
- **M. Zhu***, F. Zhuo. "Research on the Control Strategy of PV System on Suppressing Low-frequency Oscillation in Power System", ***PEAC 2014***, Shanghai, China.
- **M. Zhu***, F. Zhuo. "A Novel Method for Low-frequency Oscillation Suppression Based on PV System", ***PEAC 2014***, Shanghai, China.
- L. Xiong, C. Li, F. Zhuo*, **M. Zhu**, B. Liu, H. Zhang, "A Novel Real-time and On-line Computation Algorithm for Characteristic Parameters of Micro-grids", ***APEC 2014***, Fort Worth, USA.
- **M. Zhu***, H. Li, X. Li. "Improved State-space Model and Analysis of Islanding Inverter-based Microgrid", ***ISIE 2013***, Taipei, Taiwan.
- L. Xiong, F. Zhuo*, **M. Zhu** ,"Study on the Compound Cascaded STATCOM and Compensating for 3-phase Unbalancd Loads", ***APEC 2013***, Long Beach, USA.
- F. Zhuo*, L. Xiong, C. Li, Y. Xie, **M. Zhu**. "A Novel Real-time Computation Algorithm for Characteristic Parameters of DC Micro-grids", Authorized by State Intellectual Property Office. **Patent No**. 201310680852.5

INTERNSHIPS

STATE GRID Shaanxi Electric Power Company, Xi'an Shaanxi Jun. 2013 - Jan. 2014

- Studied typical topology of High-voltage Direct Current (HVDC) transmission, especially for Modular Multilevel Converter (MMC).

- Investigated the topology, modeling and control theory of MMC.

Emerson Network Power Co., Ltd, Shenzhen, China Jul. 2011 - Sept. 2011
"From Stranger to Emerson" Summer camp
- Became familiar with the main products of EMERSON, such as AC Power Supply/UPS, DC Power Supply, Industrial Power Supply etc.
- Studied the design and manufacture process of Low Power UPS.
- Took part in the Quality Expanding & Training.

Xi'an Action Electric Co., Ltd., Xi'an, China May. 2011 - Jul. 2011
- Learned to make inductors and electric lines.
- Designed a switching power supply from 380V AC to 5V DC.

SKILLS

Cleanroom fabrication:
- 4 years'experience of cleanroom fabrication

Programming & Circuits Design:
- Skilled in C/C++, DSP (TMS320), Altium Designer, LaTeX , Python

Simulation & Experiment:
- Skilled in MATLAB/Simulink, PSPICE, Origin
- Engineering design ability, testing experience, and advanced problem solving capability

Languages:
- Native CHINESE, Fluent ENGLISH, Intermediate FRENCH, Basic GERMAN

HONORS AND AWARDS

- NARI-RELAYS Scholarship, XJTU (Rated 17/300) 2014
- National Scholarship for Graduate Students (Rated 10/300) 2013
- First prize of 10×50 Freestyle Relay of Swimming Championship in XJTU. 2013
- Outstanding Graduates Awards of XJTU 2012
- Rated excellent of the National Undergraduate Innovative Experiment Program(3/63) 2012
- Siyuan Scholarship, XJTU 2011
- Excellent Student Cadre, XJTU 2009 & 2010
- National Encouragement Scholarship (Top 3% in 399 students) 2009

Fabrication process flow

The fabrication of the devices presented in this thesis is entirely performed in the clean room facilities of the EPFL, namely the *Center of Micronanotechnology* (CMi) and the *IPHYS* of the Physics department. In this appendix, the fabrication process flow is described.

Step	Process description	Tool
1	Wafer cleaning 1.1 Wash with SVC 14 from squirt bottle Sonicate 4’ 1.2 Wash with Isopropanol from squirt bottle,2’ 1.3 Wash with DI water 1.4 Dehydrate: Bake hotplate 5 min at 135°C 1.5 Cool down 3’	solvent-bench, HDMS,Hot plate
2	Mesa etch 2.1 Dehydrate, Clean the pipet with N_2 gun and fully cover the sample with resist. 2.2 AZ 1512 6000rpm, 30" 2.3 Bake at hotplate 1’30" at 95°C, 1’ cooling 2.4 MLA writing: 42 mJcm^2, Defocus 0 2.5 Development: AZ MIF 726, around 25’ with agitation, 3’ rinsing in DI water 2.6 Sample preparation: wafer warm up to 135°C and use quick stick to stick it on Si wafer 2.7 Descum: O_2 plasma strip low 1min 2.8 ICP:GaN standard 3min (RF200w, bias 100w, Ar:10, Cl_2:20, BCl_3:10), around 450nm 2.9 Sample unload: warm up to 135°C and unload it 2.10 Sample cleaning: SVC 14(60°C, 7w sonication) 5’,Acetone 3’, IPA 1’, N_2 gun dry off, HDMS hotplate dehydrate 1’ 2.11 Descum: O_2 plasma, strip high 3’(To clean the remaining glue on the surface)	SSE manual coater, Hotplate, MLA 150, Tepla, STS ICP

Step	Process description	Tool
3	Gate recess 3.1 SiO_2 hard mask: SiO_2 standard 32s 30nm (deposition rate is 55nmmin for small chips) 3.2 HDMS: HDMS standard 3.3 Resist coating (AZ 1512), clean the pipet with N_2 gun and fully cover the sample with resist. Coating with recipe 6000rpm, 30" (layer thickness 1.1-1.2 μm) 3.4 Bake at hotplate 1'30" at 95°C, 1' cooling 3.5 MLA writing: Dose 42 mJcm_2, Defocus 0 3.6 Development: AZ MIF 726, around 25' with agitation, 3' rinsing in DI water 3.7 Descum: O_2 plasma strip low 1min 3.8 SiO_2 etching: SiO_2 standard 1'30"(etching rate is 35nmmin) 3.9 Recess: gan vvs(RF 50w,bias 50w,Ar:17 Cl_2:50) 33s 3.10 Sample cleaning: SVC 14(60°C, 7w sonication) 5' , IPA 1', N_2 gun dry off, HDMS hotplate dehydrate 1' 3.11 TMAH treatment: TMAH 5%, 85°C, 20 min, 3 min rinse+3min rinse in two big glass bottles 3.12 Oxide removal: BOE 1min(etching rate is 350 nmmin for PEVCD SiO_2)	PEVCD, HDMS, SSE manual coater, Hot plate, MLA 150, Tepla, RIE, STS ICP, Base bench, Acid bench

Step	Process description	Tool
4	Ohmic contact 4.1 Resist coating (LOR 5A), clean the pipet with N_2 gun and fully cover the sample with resist. Coating with recipe, 2000rpm, 1' (layer thickness 700nm) 4.2 Bake at hotplate 4'10" at 175°C, 1' cooling 4.3 Resist coating (AZ 1512), clean the pipet with N_2 gun and fully cover the sample with resist. Coating with recipe POWERLAB6000, 6000rpm, 30" (layer thickness 1.1-1.2μm) 4.4 Bake at hotplate 1'30" at 95°C, 1' cooling 4.5 MLA writing: Dose 42 mJcm_2, Defocus 0 4.6 Development: AZ MIF 726, around 50' with agitation, 3' rinsing in DI water 4.7 Descum: O_2 plasma strip low 1min 4.8 Oxide strip: 1. DI water dip 1'. 2. 37% acid 1' 3. DI water 1' 4.9 Metal evaporation: HRN- recipe No.626: TiAl TiNiAu 2001200400600500 Å 4.10 Lift off: 1. Place in SVC 14 (60°C) for more than 6h. 2. use a injector in order to squirt away as much of the metal as possible. Then, place the sample in a new beaker with fresh SVC 14 and agitate for 1-2' at power level 1(pulse) in the ultrasonic bath 3. 2' in IPA 4. 2' rinse in DI water 4.11 RTA: 780°C 30"	SSE manual coater, Ceram Hotplate, MLA 150, Tepla, Acid bench, LAB 600, Solvent-bench, RTA
5	Gate oxide 5.1 Sample cleaning: as described above 5.2 ALD: 300°C 20nm Al_2O_3 or 300°C 25nm SiO_2	Solvent bench and Beneq-ALD
6	Contact opening 6.1 Resist coating (AZ 1512), clean the pipet with N_2 gun and fully cover the sample with resist. Coating with recipe 6000rpm, 30" 6.2 Bake at hotplate 1'30" at 95°C, 1' cooling 6.3 MLA writing: Dose 42 mJcm_2, Defocus 0 6.4 Development: AZ MIF 726, around 25' with agitation, 3' rinsing in DI water 6.5 Oxide removal: BOE 20-30s	SSE manual coater, Hot plate, MLA 150, and Acid bench

Step	Process description	Tool
7	Gate metal and pad 7.1 Resist coating (LOR 5A), clean the pipet with N_2 gun and fully cover the sample with resist. Coating with recipe 3000rpm, 1' (layer thickness 400nm) 7.2 Bake at hotplate 4'10" at 175°C, 1' cooling 7.3 Resist coating (AZ 1512), clean the pipet with N_2 gun and fully cover the sample with resist. Coating with recipe, 3000rpm, 30" 7.4 Bake at hotplate 1'30" at 95°C, 1' cooling 7.5 MLA writing: Dose 42 mJcm2, Defocus 0 7.6 Development: AZ MIF 726, around 40' with agitation, 3' rinsing in DI water 7.7 Descum: O_2 plasma strip low 1min 7.8 Metal evaporation: HRN- recipe No.626: NiAu 2001500 Å 7.9 Lift off: 1. Place in SVC 14 (60°C) for more than 6h. 2. use a injector in order to squirt away as much of the metal as possible. Then, place the sample in a new beaker with fresh SVC 14 and agitate for 1-2' at power level 1(pulse) in the ultrasonic bath 3. 2' in IPA 4. 2' rinse in DI water	SSE manual coater, Hot plate, MLA 150, Tepla, Lab 600, Solvent bench
8	Metal removal, in case of bad lift-off 8.1 Au etching: KI+I2 2' etching, twice 3' rinsing in DI water in two different glasses 8.2 Piranha for metal etching: Preparation: 1 heater, 1 magnet, 4 glasses cup,1 chip holder, 1 graduated cylinder, 96% sulfuric acid, 30% hydrogen peroxide Steps: 1)Set up the heater and put one glass cup on the heater. 2)Measure 300 ml H_2SO_4 96% in the glasses 3)Set magnet to 300rpm, put the thermal meter higher enough for not breaking it 4) Measure 100 ml H_2O_2, pull H_2O_2 very gently to H_2SO_4(never set it too fast, otherwise it may cause explosion) 5) Set the temperature to 75°C if needed 6) 4-5' for etching	Acid bench

Recessed tri-gate R_ON model

This section is the code for the simplified model of the recessed tri-gate structure.

```
clc;

clear;

R_meas=[7.36167,7.59667,7.65667,7.76667];

w_meas=[200,400,500,600];

w_n=100:2:1200 %varied width

w_T=100; %etched trench 100nm

h=240; %nanowire depth 240nm

R_sh1=1713;

R_sh2=3520;

R_sh3=269;

FF=w_n.(w_n+w_T)%filling factor

L=700;%etched length 700nm

l_rec=550;

N_nw=1000000.(w_n+w_T)

S_nw=1.(R_sh1*(l_rec+480).w_n+R_sh3*(L-l_rec).w_n)

S_on=w_nR_sh3L

S_side=2*hR_sh2L

S_Bot=0;w_TR_sh2L
```

```
S_total=(S_nw+S_side+S_Bot).*N_nw

S_total_on=(S_on+S_side+S_Bot).*N_nw

R_total=1.S_total+5.8

R_total_on=1.S_total_on+5.8

Inw=S_nw.(S_nw+S_side+S_Bot)

Iside=S_side.(S_nw+S_side+S_Bot)

Ibot=S_Bot.(S_nw+S_side+S_Bot)

figure

plot(w_n,R_total)

hold on

xlabel('Width(nm)')

ylabel('Resistance (Ohmmm)')

plot(w_meas,R_meas,'or')

figure

hold on

plot(N_nw,R_total)

plot(N_nw,R_total_on)

xlabel('N_NW')

ylabel('Resistance (Ohmmm)')

figure

plot(FF,R_total)

xlabel('FF (%)')

ylabel('Resistance (Ohmmm)')

plot(N_nw,R_total_on)
```

figure

plot(FF,Inw,FF,Iside,FF,Ibot)

legend('nanowire contribution','sidwall contribution','bottomcontribution')

TCAD simulation of field plate

This part is the TCAD simulation of the electric field on the edge of recessed tri-gate structure compared with recessed planar structure.

##################WAFER SETTINGS######################### #set cap thickness

set ct=0.0025

#barrier thickness

set bth=0.02

set bth_nm=floor($bth*1000)

#barrier composition

set bcomp=0.23

#i-GaN channel thockness

set chth=0.42

#buffer thickness

set buf=4.5

##################DEVICE SETTINGS######################### #oxide thickness

set ox_th=0

set ox_th_nm=floor($ox*1000)

#recess length

set recess_l=0.4

#recess depth

```
set bleft=0.003

set recess_d=0

#$ct+$bth-$bleft

set recess_d_nm=floor($recess_d*1000)

#gate thickness from AlGaN barrier

set gate_th=0.2

#gate length

set gate_l=2.5

#gate to drain distance

set Lgd=5

#source to gate distance

set Lsg=1

#right edge of the structure

set xmax=$Lsg+$gate_l+$Lgd

###################DOPINGINTERFACE#######################

# density of background donors in GaN

set d_gan=1e15

# density of background donors in AlGaN

set d_algan=1e17

# location of surface donor trap level relative to valence band

set Ed=3.43-1.2

# density of surface donor traps

set Dens=3e13

# location of surface acceptor trap level relative to conduction band
```

set Ea=3.43-0.9

density of acceptor

set Buf_dens=1e20

set ox1=0.01

set ox2=0.03

set ox3=0.03

go atlas simflags="-P 12"

##################X.MESH#######################

#gives the out of plane width if width=1000=1mm all the results are normalized to 1mm in Z(Amm, etc.)

mesh width=1000

#left edge of structure

x.m l=0 s=0.1

#left edge of gate

x.m l=$Lsg s=0.025

x.m l=$Lsg s=0.001

x.m l=$Lsg+0.45 s=0.05

x.m l=$Lsg+0.9 s=0.001

x.m l=$Lsg+0.9+0.15 s=0.025

x.m l=$Lsg+0.9+0.275 s=0.001

x.m l=$Lsg+0.9+0.275+0.075 s=0.015

x.m l=$Lsg+0.9+0.275+0.15 s=0.001

x.m l=$Lsg+0.9+0.275+0.15+0.15 s=0.025

x.m l=$Lsg+0.9+0.275+0.15+0.275 s=0.001

x.m l=$Lsg+0.9+0.275+0.15+0.275+0.45 s=0.05

x.m l=$Lsg+0.9+0.275+0.15+0.275+0.9 s=0.001

x.m l=$Lsg+0.9+0.275+0.15+0.275+0.9+2.5 s=0.25

#right edge of structure

x.m l=$xmax s=0.1

##################Y.MESH#######################

#top of structure

y.m l=-$gate_th-$bth-ox_th-ct s=0.1

#top of oxide

#y.m l=-$bth-$ox_th-$ct s=0.01

#top of cap

y.m l=-$bth-$ct s=0.001

y.m l=-$bth-$ct-$ox3 s=0.001

y.m l=-$bth-$ct-$ox2 s=0.001

y.m l=-$bth-$ct-$ox1 s=0.001

#top of barrier

y.m l=-$bth s=0.001

#middle of barrier

y.m l=-$bth2 s=0.001

#top of oxide in recess region

#y.m l=-$bth-$ct+$recess_d-$ox s=0.0005

#top of recess

#y.m l=-$bth-$ct+$recess_d s=0.0005

#2deg

y.m l=0 s=0.0005

```
#end of sorce and drain contats
y.m l=0.04 s=0.005
#bottom of channel
y.m l=$chth s=0.05
#bottom of structure
y.m l=$chth+$buf s=1
##################STRUCTURE#######################
#SiN on top
region num=1 mat=SiO2 y.min=-$gate_th-$bth-$ox-$ct
y.max=-$bth-$ct insulator
#cap
region num=5 mat=GaN y.min=-$bth-$ct y.max=-$bth donors=$d_gan #barrier
region num=2 mat=AlGaN y.min=-$bth y.max=0 x.comp=$bcomp
donors=$d_algan
#GaN channel
region num=3 mat=GaN y.min=0 y.max=$chth donors=$d_gan
#GaN buffer
region num=4 mat=GaN y.min=$chth y.max=$chth+$buf substrate
#oxide in recess
region num=1 mat=SiO2 x.min=$Lsg+($gate_l-$recess_l)2
x.max=$Lsg+($gate_l-$recess_l)2+$recess_l
y.min=-$bth-$ct y.max=-$bth-$ct+$recess_d insulator
##################ELECTRODES#######################
elect num=1 name=source x.max=0 y.min=-$bth2 y.max=0.04
```

elect num=2 name=drain x.min=$xmax y.min=-$bth2 y.max=0.04

#elect num=3 name=gate x.min=$Lsg x.max=$Lsg+$gate_l

y.min=-$bth-$gate_th-$ox-$ct y.max=-$bth-$ox

elect num=3 name=gate x.min=$Lsg x.max=$Lsg+0.9

y.min=-$bth-$gate_th-$ox-$ct y.max=-$bth-$ox3-$ct

elect num=3 name=gate x.min=$Lsg+0.9 x.max=$Lsg+0.9+0.275

y.min=-$bth-$gate_th-$ox-$ct y.max=-$bth-$ox2-$ct

elect num=3 name=gate x.min=$Lsg+0.9+0.275

x.max=$Lsg+0.9+0.275+0.15 y.min=-$bth-$gate_th-$ox-$ct

y.max=-$bth-$ox1-$ct

elect num=3 name=gate x.min=$Lsg+0.9+0.275+0.15

x.max=$Lsg+0.9+0.275+0.15+0.275 y.min=-$bth-$gate_th-$ox-$ct

y.max=-$bth-$ox2-$ct

elect num=3 name=gate x.min=$Lsg+0.9+0.275+0.15+0.275

x.max=$Lsg+0.9+0.275+0.15+0.275+0.9

y.min=-$bth-$gate_th-$ox-$ct y.max=-$bth-$ox3-$ct

##################TRAPS#####################

doping region=4 uniform trap acceptor conc=$buf_dens degen=4

e.level=$Ea taun=1e-12 taup=1e-12

inttrap donor density=$Dens degen=2 e.level=$Ed taun=1e-12

taup=1e-12 y.min=-$bth-$ct y.max=-$bth-$ct s.i

#COMMENT IF NO RECESSS!!!!

#inttrap donor density=$Dens degen=2 e.level=$Ed+3.87-3.43

taun=1e-12 taup=1e-12 y.min=-$bth-$ct+$recess_d

```
y.max=-$bth-$ct+$recess_d s.i
##################CONTACTS#######################
contact name=gate work=5.23
contact name=source work=3.43
contact name=drain work=3.43
##################MODELS#######################
models region=2 print POLAR CALC.STRAIN polar.scale=1 fermi
ni.fermi pch.ins
models region=3 print POLAR polar.scale=1 fermi ni.fermi
models region=5 print POLAR polar.scale=1 fermi ni.fermi pch.ins
mobility albrct.n
##################METHOD#######################
method autonr gumits=300 carriers=2
##################OUTPUT#######################
output con.band val.band polar.charge
################################################################################
# idvg curve
################################################################################
#initial solution
solve init
save outf=zero.str
#drain ramp from 0 to 5
#log outf="Id_Vd_Vg0V.log"
# solve vdrain=0
```

```
# solve name=drain vfinal=5 vstep=0.5

#log off

#transfer at Vd=5V

log outf="Id_Vg_Vd5V.log" no.trap

solve name=gate vfinal=-8 vstep=-0.5

solve name=gate vfinal=-11 vstep=-0.1

save outf=test.str

log off

save outf="Vd5V_Vgm14V.str"

#drain ramp to high voltage

log outf=drain_ramp.dat

solve name=drain vfinal=1 vstep=0.05

solve name=drain vfinal=5 vstep=0.1

solve name=drain vfinal=10 vstep=0.5

solve name=drain vfinal=20 vstep=1

save outf=20v.str

solve name=drain vfinal=100 vstep=5

save outf=100v.str

log off

quit
```