P-GaN Tri-Gate MOS structure for Normally-Off GaN Power Transistors

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***Abstract*— In this letter, we present a new concept for normally-off AlGaN/GaN-on-Si MOS-HEMTs based on the combination of p-GaN, tri-gate and MOS structures to achieve high threshold voltage (V_{TH}) and low on-resistance (R_{ON}). The p-GaN is used to engineer the band structure and reduce the carrier density (N_s) in the tri-gate structure for a high V_{TH}. The gate control is mainly achieved from field-effect though the tri-gate sidewalls, and does not rely on injection of gate current. The MOS structure enables much larger gate voltages (V_G) and the effective sidewall modulation results in excellent switching performance at high switching frequencies. In addition, this concept eliminates the need for thin barriers (typical in p-GaN devices), which combined to the conduction channels formed at the tri-gate sidewalls, resulted in a smaller R_{ON} compared with planar p-GaN structures. The p-GaN length and tri-gate filling factor (*FF*) were optimized to achieve a good trade-off between high V_{TH} and low R_{ON}. The excellent channel control capability offered by the tri-gate structure led to a higher ON/OFF ratio and smaller sub-threshold slope (*SS*) compared to similar planar p-GaN devices. These results unveil the excellent prospects of p-GaN tri-gate MOS technology for future power electronics applications.**

Index Terms— **E-mode, p-GaN, MOS HEMT, tri-gate, trench**

I. Introduction

GaN (MOS)HEMTs offer a huge potential for high-frequency power electronics applications due to their excellent materials' properties, enabling low R_{ON} and high breakdown voltages (V_{BR}) [1], [2]. Normally-off operation in power devices is highly desired to guarantee a safe operation and to be widely adopted by the power electronics industry [3]. Among several techniques reported to achieve normally-off operation, such as barrier-recess [4]–[7] and fluorine-based plasma treatment under the gate [8], [9], one of the most promising and widely adopted methods is based on p-GaN gates [10]. In this method, the conduction band of the AlGaN/AlN/GaN at the channel under the gate is lifted up by the p-doped GaN at the surface, depleting the 2DEG under the gate [3]. The control of the channel conductivity relies on current injected from the p-GaN ohmic or Schottky gate contacts [11]. However, there is a trade-off between positive V_{TH} and low sheet resistance (R_S). On one hand, this is due to the combined effect of the thinner barrier needed for the p-GaN to deplete the channel [3], which increases R_S on the access regions. On the other hand, as shown in this work, it is not possible to fully restore the conductivity of the channel under the p-GaN gate by applying a positive V_G. This indicates that the p-GaN region is still less conductive than the typical access region, even at high V_G. Thus, to reduce the R_{ON}, a shorter p-GaN and/or a thicker barrier is desired, which however, makes it difficult to reach normally-off behavior.

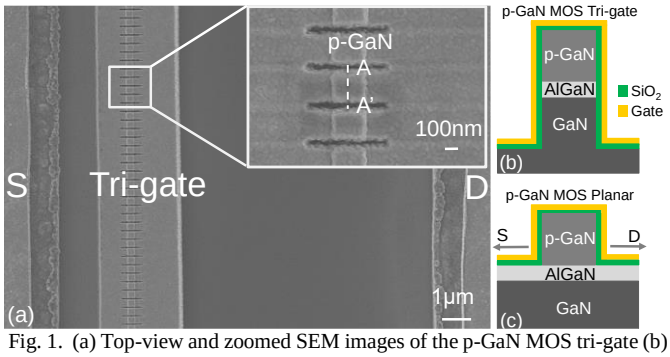

Fig. 1. (a) Top-view and zoomed SEM images of the p-GaN MOS tri-gate (b) Cross-sectional schematic of the p-GaN MOS Tri-gate region along the AA' line, and of the (c) p-GaN MOS Planar gate along the source-drain direction.

Tri-gate structures offer an excellent approach to locally adjust the N_s by etching fins under the gate. This method enables to reach a positive V_{TH} [12]–[14] while still using thick barriers (~20-25 nm) in the access regions, thus conserving a low access resistance in the un-patterned regions. Etch-induced damages can still be present, however, they are less sensed due to the thicker barrier that yields a larger N_s. In addition, a significant positive V_{TH} shift can be achieved by adjusting the tri-gate *FF* and fin width combined with high work-function gate metals [15].

In this work, we demonstrate the combination of p-GaN, tri-gate and MOS to form a new device structure that enables to reach positive $V_{TH,}$ relying on much shorter p-GaN regions with wider tri-gate fins and thicker AlGaN barriers (compared to planar p-GaN gated devices). This yields a significantly smaller R_{ON} for the same V_{TH}. In addition, the MOS gate enables a fast control over the channel and much larger V_G, without relying on gate current injection. This also makes them compatible with common gate driver circuits.

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II. Device Design and Fabrication

Fig.1 illustrates the top-view SEM picture and cross-sectional schematics of the p-GaN tri-gate MOS-HEMTs (p-GaN MOS Tri-gate) (Fig.1 a,b) and p-GaN Planar MOS-HEMTs (p-GaN MOS Planar) (Fig.1c) regions of the fabricated GaN MOS-HEMTs presented in this work. The device fabrication, based on a p-GaN (75 nm)/$Al_{0.25}Ga_{0.75}N$ (20 nm)/GaN-on-Si wafer, started with the definition of mesa and tri-gate regions by e-beam lithography, followed by Cl_2-based Inductively Coupled Plasma etch. A major challenge for p-GaN-gated HEMTs is to obtain uniform and low-damage p-GaN etching over the non-gated active regions [3], [10], [16]. To this end, the 200 nm-wide p-GaN gate region was protected with e-beam lithography resist, followed by a 75 nm-deep low-damage slow-etch-rate Cl_2/O_2/Ar-based selective ICP etching recipe [16]–[18]. The high selectivity of 35:1 for p-GaN:AlGaN, combined with O_2 plasma/ HCl treatment is a critical process to minimize surface damages. A surface annealing at 500 °C was performed to further smoothen the surface and recover the dry-etching damages, followed by ohmic contact formation. A 25 nm-thick SiO_2 gate dielectric was deposited by atomic layer deposition (ALD), after surface treatment in 37% HCl for 1 min and 500°C bake for 5 min. Finally, the gate metal was formed by Ni/ Au.

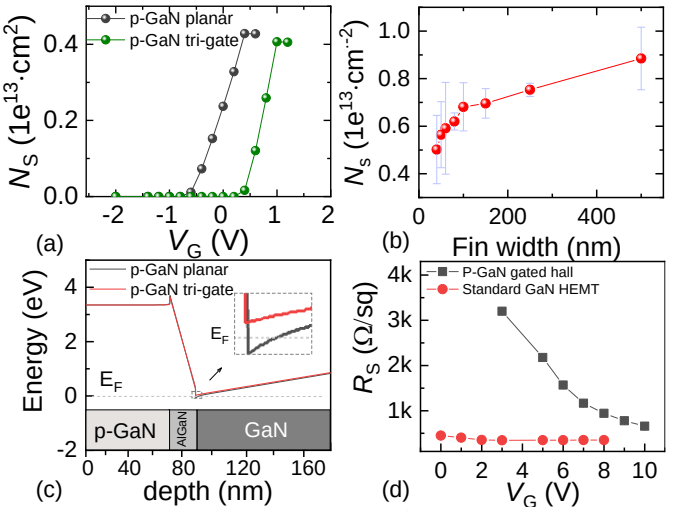

Fig. 2. (a) Simulated electron concentration of p-GaN planar and p-GaN tri-gate devices on p-GaN (75 nm)/$Al_{0.25}$GaN (20 nm)/GaN epi-structure, under V_G from -2 to 2 V. (b) Measured electron concentration with different tri-gate fin widths on an AlGaN (20 nm)/GaN structure. (c) Simulated band diagram of p-GaN planar and p-GaN tri-gate devices. (d) Measured sheet resistance by gated hall of a p-GaN and a GaN HEMT structures.

III. Motivation and Approaches

The thickness and Al molar fraction of the Al_xGaN_{1-x} barrier are two important parameters influencing the band diagram of the p-GaN/AlGaN/GaN, and the device performance. Traditionally, thin barriers or low Al concentration are used in p-GaN transistors to enable normally-off behavior in equilibrium, as the conduction band edge at the AlGaN/GaN interface should lie above the Fermi level. However, it affects the access regions in the same way, increasing the R_S. Moreover, etch-induced damages are much more significant on thin barriers, degrading even further the R_{ON}.

In this work, we focus on the use of p-GaN (75 nm-thick) grown on an $Al_{0.25}$GaN (20 nm-thick)/GaN epi-structure.

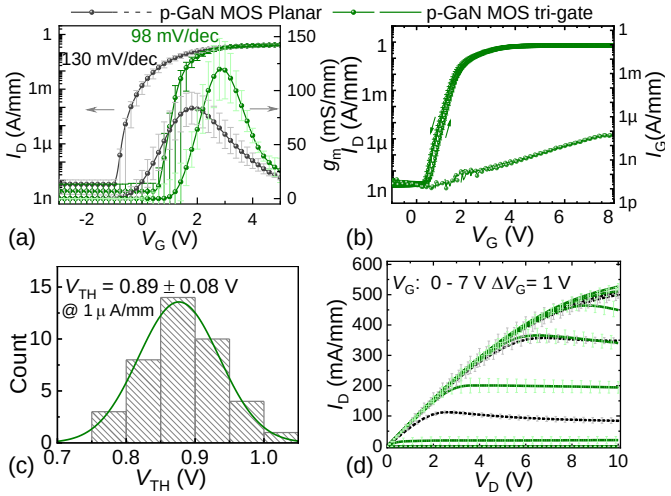

Fig. 3. (a) Comparison of transfer characteristics of the p-GaN MOS Tri-gate and the p-GaN MOS Planar device at V_{DS} = 5 V. The p-GaN length was 200 nm. (b) Double-sweep I_D and I_G versus V_G for the p-GaN MOS Tri-gate. (c) Histogram of V_{TH} measured from 40 p-GaN MOS Tri-gate devices. (d) Output characteristics of the two types of devices with V_G up to 7 V. The L_{GS}, L_G and L_{GD} were 1, 2.5 and 10 μm, respectively, width was 80 μm and *FF* was 0.66. Standard deviation bars were determined from the measurement of 10 devices of each type, revealing their consistent performance.

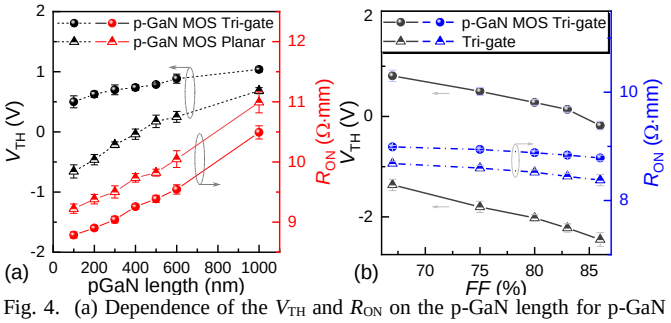

Fig. 4. (a) Dependence of the V_{TH} and R_{ON} on the p-GaN length for p-GaN MOS Planar and p-GaN MOS Tri-gate devices. (b) V_{TH} and R_{ON} dependence on filling factor (*FF*) of Tri-gate (Normally-on) and p-GaN MOS Tri-gate (Normally-off) transistors (p-GaN length was fixed at 200nm).

Numerical simulations show that the N_s of p-GaN planar device starts rising at -0.5 V (Fig. 2 (a)), indicating that the p-GaN on such thick barriers is not enough to result in normally-off behavior. Here, this was addressed by adding a tri-gate structure underneath the gate (Fig. 2 (a)). This allows to locally adjust N_S by the tri-gate fin width (Fig. 2 (b)), while still using a thick barrier for small access resistance. The combined effect of p-GaN and tri-gate lowers the Fermi level farther from the conduction band, as shown in the simulated band diagram of p-GaN planar and p-GaN tri-gate devices (Fig. 2(c)).

Moreover, we compared gated-Hall measurements of R_S between p-GaN and planar HEMTs. This revealed that the channel conductivity under the p-GaN gate is not fully restored even at high V_G (Fig. 2(d)), whereas tri-gate structures cause negligible degradation in R_{ON} [14]. This shows the importance of reducing the p-GaN length to decrease the overall R_{ON}. As shown later, a reduction of the p-GaN length without affecting V_{TH} is possible in tri-gate structures, but not in planar p-GaN MOS-HEMTs.

IV. Results and Discussion

In this section, we compare the performance of p-GaN MOS Planar and p-GaN MOS Tri-gate to reveal their operation mechanism. A significant positive shift of 1.5 V in V_{TH} (at 1

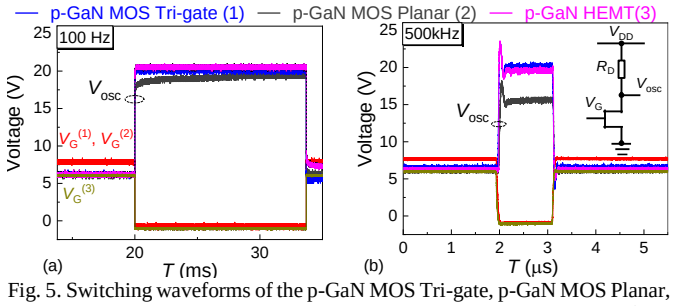

Fig. 5. Switching waveforms of the p-GaN MOS Tri-gate, p-GaN MOS Planar, and p-GaN HEMT at (a) 100 Hz and (b) 500 kHz with V_{DD} = 20 V and V_G from -1 V to 8 V for p-GaN MOS Tri-gate and p-GaN MOS Planar, while V_G from -1 V to 6 V for p-GaN HEMT, due to its lower gate voltage capability. (Inset) Schematic of experimental setup used to measure the experiment.

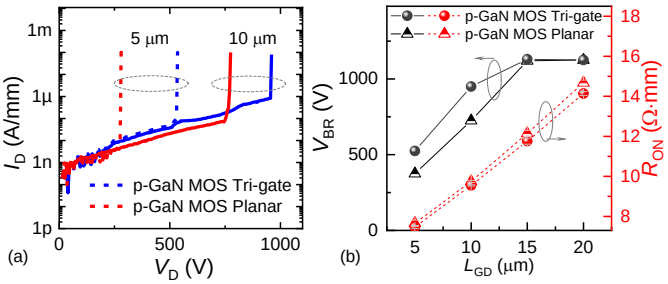

Fig. 6. (a) Breakdown characteristics of the p-GaN MOS Tri-gate (at V_G = 0 V) and p-GaN MOS Planar (at V_G = -1 V) with different L_{GD} with grounded substrate. (b) Extracted V_{BR} and R_{ON} dependence on L_{GD} of p-GaN MOS Planar and p-GaN MOS Tri-gate. The V_{BR} was defined at $I_{OFF} \leq 1$ μA/mm.

μA/mm) was observed from the p-GaN MOS Planar to the p-GaN MOS Tri-gate (Fig. 3(a)), with p-GaN length of 200 nm. The larger V_{TH} in the p-GaN MOS Tri-gate is mainly due to the additional strain relaxation of the AlGaN barrier and the sidewall gate modulation [13], [14], [19], [20]. The p-GaN MOS Tri-gate exhibited a larger g_m of 124 ± 18 mS/mm, with an ON/OFF ratio beyond 10^9, an improved *SS* of 98 ± 5 mV/dec and lower I_{OFF} at V_G = 0 V, as compared with the p-GaN MOS Planar, revealing an improved tri-gate control over electrons in the channel. The small hysteresis, below 0.1 V and low gate leakage, below 7×10^{-8} A/mm, observed for p-GaN MOS tri-gate device under V_G up to 8 V (Fig. 3(b)) indicates a good gate-oxide quality. The p-GaN MOS Tri-gate showed a much smaller hysteresis of ~0.17 V (at V_G^{max} of 8 V), which is also smaller than in the p-GaN Planar (~0.45 V). This is likely due to the better gate control in the Tri-gate, since both devices had the same gate oxide. Moreover, the V_{TH} histogram from 40 different Tri-gate devices shows a relatively consistent V_{TH} of around 0.89 V at 1 μA/mm.

The output characteristics of these devices are shown in Fig. 3 (d). The p-GaN MOS Tri-gate presented a good I_D^{max} of 522 ± 16 mA/mm at V_G = 7 V comparable to the p-GaN MOS Planar (508 ± 18 mA/mm). The high I_D^{max} was due to the combined effect of the short p-GaN and the tri-gate structure. The R_{ON} of the p-GaN MOS Tri-gate and p-GaN MOS Planar, extracted from I_D - V_D sweeps in linear region, were 9.2 ± 0.26 Ω·mm and 9.82 ± 0.29 Ω·mm at V_G = 7 V, respectively. The dependence of V_{TH} and R_{ON} on p-GaN gate length was investigated for both devices (Fig. 4(a)). The p-GaN MOS Tri-gate achieved a V_{TH} of ~0.5 V with a p-GaN length of 100 nm, resulting in a R_{ON} of 8.78 ± 0.05 Ω·mm. On the other hand, the p-GaN MOS Planar devices could only reach a similar V_{TH} with p-GaN length of ~1000 nm, thus resulting in an R_{ON} of 10.99 ± 0.17 Ω·mm. For the same p-GaN length, the p-GaN MOS Tri-gate showed a much reduced R_{ON} compared to the p-GaN MOS Planar.

To reveal the effect of the p-GaN layer, Fig. 4 (b) shows the dependence of V_{TH} and R_{ON} on the tri-gate *FF* for MOS Tri-gate (D-mode) and p-GaN MOS Tri-gate (E-mode) transistors. The trench spacing (d_T) was fixed at 100 nm and the fin width (w_T) was varied from 200 nm to 600 nm, which corresponded to *FF* varying from 0.66 to 0.87. The p-GaN length was fixed at 200 nm. As the *FF* increased, the V_{TH} dropped from 0.9 V to -0.2 V for the p-GaN MOS Tri-gate, and from -1.3 V to -2.8 V for the Tri-gate. While the *FF* had a significant effect on the V_{TH}, it did not affect much the R_{ON}, presenting only a reduction of 0.2 Ω·mm for the p-GaN MOS Tri-gate, and of 0.4 Ω·mm for the Tri-gate. Thus a small R_{ON} and positive V_{TH} can be designed with a short p-GaN combined with tri-gates with small *FF*.

The dynamic performance of p-GaN MOS Planar, p-GaN MOS Tri-gate, and p-GaN HEMT was investigated using the device test setup shown in the inset of Fig. 5. At a low frequency of 100 Hz (Fig. 5 (a)), it took a few miliseconds for the p-GaN MOS Planar to be completely turned off, while the p-GaN MOS Tri-gate and p-GaN HEMT turned-off instantaneously. This phenomenon can be seen more clearly at 500 kHz (Fig. 5 (b)). The p-GaN MOS Tri-gate and p-GaN HEMTs can be turned on/off within a few nanoseconds, while the p-GaN MOS Planar could not fully turn off at such frequencies. This shows the effective and fast sidewall gate control of p-GaN MOS Tri-gate, which is more dominant than the top gate control in traditional GaN HEMTs. For the p-GaN MOS planar device, the gate control is mainly through fringing capacitances from the surface to the 2DEG, which is less effective compared with the tri-gate sidewall control.

The comparison of breakdown characteristics between the p-GaN MOS Planar and p-GaN MOS Tri-gate is shown in Fig. 6. The V_{BR} of p-GaN MOS Tri-gate was extracted for V_G of 0 V with grounded substrate at 1 μA/mm (Fig. 6 (a)), resulting in 520 V and 980 V for L_{GD} of 5 μm and 10 μm, respectively, compared to 380 V and 750V, for p-GaN MOS planar devices (at V_G = -1 V). The observed improvement in V_{BR} compared with the p-GaN MOS Planar is due to the effective integrated field plates (FP) in the p-GaN tri-gate region [16, 21]. The p-GaN MOS Tri-gate presented lower R_{ON} for the same L_{GD} compared with p-GaN MOS Planar devices (Fig. 6 (b)). The low R_{ON}, larger V_{TH} and V_{BR}, together with the effective gate control reveal the significant potential of the p-GaN tri-gate MOS technology for high-performance E-mode GaN devices.

V. Conclusions

In this work we have demonstrated normally-off p-GaN tri-gate GaN-on-Si MOSHEMTs with a combination of tri-gate, p-GaN and MOS structures on the gate. The introduction of the tri-gate enables a reduction of the necessary p-GaN length to reach E-mode operation, resulting in a smaller R_{ON}. With a selective p-GaN recess, an integrated field plate and an optimized p-GaN structure, p-GaN MOS Tri-gate devices presented V_{TH} of 0.9 V at 1μA/mm, low R_{ON} of 9.2 Ω·mm and high V_{BR} of 960 V for L_{GD} of 10 μm, with grounded substrate.

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