

# Investigation on Output Capacitance Losses in Superjunction and GaN-on-Si Power Transistors

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**Abstract**—Low ON-resistance of advanced superjunction (SJ) and GaN-on-Si transistors is of great importance in power converters, however, the anomalous loss in their output capacitance ( $C_{oss}$ ) severely limits their performance. In this work, we use an energy-oriented measurement technique providing high voltage swings, high frequencies, and high values of  $dv/dt$ , which unlike Sawyer Tower, works without any pre-assumptions about circuit model of the transistor under test. This measurement method just relies on a low-voltage dc supply without the need of a high-power RF amplifier. In contrast with previous studies, the method shows that the small-signal  $E_{oss}$  of SJ devices is not necessarily different from the one measured at large-signal domain. However, the reported  $E_{oss}$  in datasheets might correspond to the discharging cycle, which is considerably lower than the actual  $E_{oss}$  needed to charge  $C_{oss}$ . Measurements on enhancement-mode GaN-on-Si power transistors give insights on the possible relation between  $C_{oss}$ -losses and dynamic  $R_{on}$  degradation, as the two main phenomena hindering the performance of GaN transistors at high switching frequencies. These results give useful guidelines in utilizing and optimizing power transistors, especially at high-frequency operation.

**Keywords**— $C_{oss}$  losses, soft-switching losses, GaN, Si, Superjunction.

## I. INTRODUCTION

The non-recoverable energy loss associated with charging and discharging the output capacitance ( $C_{oss}$ ) of some of the advanced transistors and diodes considerably limit their performance in power converters, especially those operating at high frequencies [1]-[10]. An unexpected power loss in soft-switched power converters based on Si superjunction (SJ) MOSFETs with low specific  $R_{on}$ , initiated studies on their large-signal  $C_{oss}$ , where a non-symmetric charging and discharging processes were obtained [5]-[7]. Recently,

investigations on GaN-on-Si high-electron-mobility transistors (HEMTs) revealed a new type of  $C_{oss}$ -losses in these devices [2], [4].

Nonlinear resonance is an innovative approach to characterize  $C_{oss}$ -losses at very high frequencies (exceeding 40 MHz) and extremely high values of  $dv/dt$  (exceeding 100 V/ns) [8]. The method works based on a resonance between  $C_{oss}$  and a pre-calibrated inductor, where the initially stored energy of inductor  $L$  (Fig. 1a) is fully transfers to the  $C_{oss}$  and comes back again to the inductor (Fig. 1b). By a single voltage measurement ( $v_{ds}$ ) the energy dissipated in  $C_{oss}$  can be extracted [8]. In this work we extract the energies

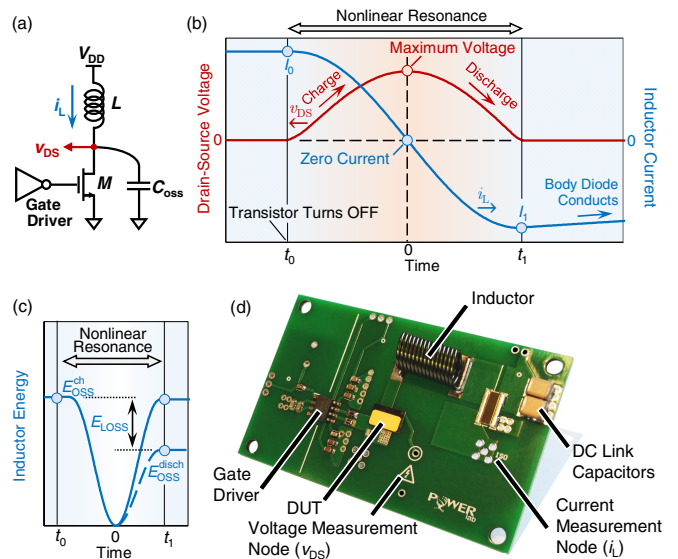


Fig. 1. (a) Schematics of the proposed circuit. (b) Illustrations of  $v_{ds}$  and  $i_L$  waveforms showing a resonance between  $L$  and  $C_{oss}$ . (c) Inductor energy for devices with (solid line) and without (dashed line)  $C_{oss}$ -loss. (d) Realization of the proposed circuit.

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corresponding to charging and discharging of  $C_{OSS}$  as well as  $E_{DISS}$ , based on the inductor current  $i_L$ . This is a unique feature of this method and makes it an ‘energy-oriented’ technique. Even by looking at  $C_{OSS}$  as a black-box with an unknown circuit model, the method gives a valid value of dissipated energy. This is of extreme importance especially for devices with complex charging and discharging processes. For instance in SJ transistors, stranded charges left within the p-columns discharging as minority carriers in a high resistive path, reflect as an infinite capacitance in ST method, and the reason for this non-physical result is that the device cannot be modeled by a single capacitance in this regime.

## II. METHODOLOGY

As shown in Fig. 1b both charging and discharging processes occurs in this resonance ( $t_0 < t < t_1$ ), so the initial energy of inductor ( $E_0 = 1/2 LI_0^2$ ) equals the charging energy of  $C_{OSS}$  when it charges up to  $V_{max}$ , and the final energy of inductor ( $E_1 = 1/2 LI_1^2$ ) equals the discharging energy of  $C_{OSS}$ . Fig. 1c shows inductor energy over time for devices with and without  $C_{OSS}$ -losses. Although losses due to the high- $Q$  inductor  $L$  is very small during the single-cycle resonance, this loss can be easily de-embedded, resulting in a very high-precision measurement. In this regard,  $2\pi/Q$ , where  $Q$  is the inductor quality factor, is the portion of energy dissipated in  $L$ , so the  $C_{OSS}$ -loss can be calculated as

$$E_{DISS} = (1 - 2\pi/Q)E_0 - E_1 \quad (1)$$

The  $C_{OSS}$  charging and discharging can also be extracted from

$$E_{OSS}^{ch} = (1 - \pi/Q)E_0 \quad (2)$$

and

$$E_{OSS}^{disch} = E_1 + (\pi/Q)E_0 \quad (3)$$

respectively. A typical  $Q$ -factor larger than 100 leads to 2% or less change in  $E_{OSS}$ . A realization of the proposed circuit has been illustrated in Fig. 1d. A high precision series resistor is used to measure  $i_L$ .

## III. EXPERIMENT

We conducted experiments on transistors with different technologies to show the applicability of the proposed method. The measurements were carried out with a 1-GHz 5-GS/s digital oscilloscope. Voltage measurement with a 1-GHz differential-probe across a 200 m $\Omega$  series resistor was used to extract current of the inductor. The small energy loss in this small resistor is included into the inductor quality factor. The high bandwidth provided in these measurement enables capturing  $C_{OSS}$ -losses at very high frequencies.

Measured results for a 650-V 60-A Si SJ MOSFET at  $V_{max} = 250$  V are shown in Fig. 2. From the initial inductor energy of 17.3  $\mu$ J, only 7.7  $\mu$ J has been recovered, showing a lossy charging/discharging process. This method, not only extracts the  $C_{OSS}$ -losses, but also gives insights to device behavior and

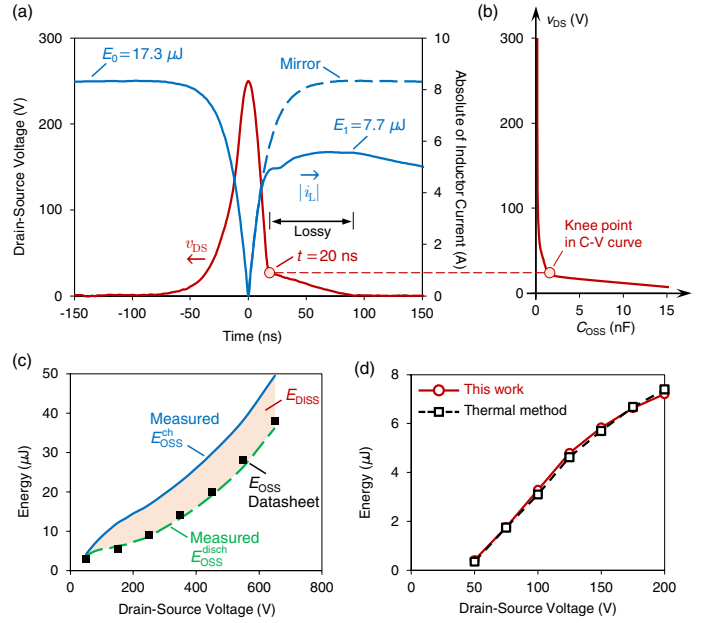


Fig. 2. (a) Measurement results for a 650-V 60-A Si SJ MOSFET using  $L = 500$  nH at maximum voltages 250 V. Lossy behavior of this device starts when it is getting out from full depletion regime. (b)  $C_{OSS}$ - $V_{DS}$  curve reported in datasheet verifies the jump in  $C_{OSS}$  happens exactly at the voltage that the lossy behavior is started. (c) Extracted  $C_{OSS}$  charging/discharging energies and data reported in datasheet as well as the extracted  $C_{OSS}$  loss ( $E_{DISS}$ ). (d) The estimated  $C_{OSS}$  loss from thermal measurement (dashed line) verifies the extracted  $E_{DISS}$  by the proposed method (solid line).

shows indications about origin of these losses. The mirror of current with respect to  $t = 0$ , shows a symmetry until  $t = 20$  ns, where the inductor current is almost equal to that at  $t = -20$  ns.

At  $t = 20$  ns the slope of  $v_{DS}$  significantly changes, which corresponds to the jump in  $C_{OSS}$  (knee point in Fig. 2b), typical for SJ devices, showing that the depletion process is fully completed around this voltage [2]. The lossy behavior starts immediately after  $t = 20$  ns, when the device is getting out from depletion regime, showing that the energy corresponds to stranded charges has not been fully recovered. Fig. 2c shows extracted  $E_{OSS}^{ch}$  and  $E_{OSS}^{disch}$ , as well as the  $E_{OSS}$  reported in datasheet (corresponding to small-signal measurement). It appears that the smaller energy corresponds to the discharge of  $C_{OSS}$  has been reported in datasheet. The extracted  $C_{OSS}$  energy loss from this method were verified with a thermal measurement, where sinusoidal signals with different amplitudes from 25 V to 200 V was applied to the device in a ST circuit. The temperature rise was captured with a thermal camera. The measurements were calibrated with a DC test. Fig. 2d shows a good agreement between extracted energy loss with this method and the estimated energy loss with thermal measurement.

Zulauf *et al.* reported a difference between the large-signal  $E_{OSS}^{ch}$  and the values reported in datasheet based on small-signal measurements [5]. Figs. 2c suggests that the origin of the observed difference could be due to the fact that the  $E_{OSS}^{disch}$  is reported in the datasheet, while there is no difference in the results obtained by small-signal and large-

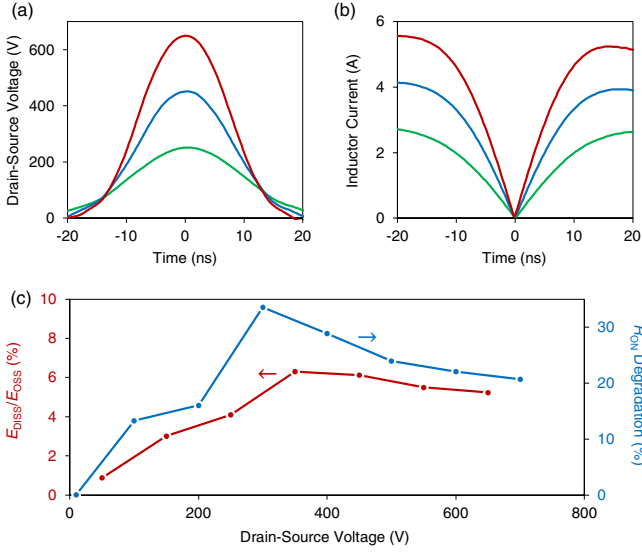


Fig. 3. (a) Measured  $v_{DS}$  at three different voltage levels for an enhancement-mode GaN HEMT together with (b) current waveforms. (c) Extracted  $E_{DISS}$  and measured ON resistance degradation.

signal measurements (small-signal  $E_{OSS}$  matches with large-signal  $E_{OSS}^{disch}$  in Fig. 2c).

Figs. 3a and b, respectively show measured  $v_{DS}$  and  $i_L$  waveforms for a 650-V 30-A GaN HEMT. The extracted  $C_{OSS}$  energy dissipation, as well as  $R_{ON}$  degradation (measured with AMCAD pulsed IV system) are shown in Fig. 3c. The  $R_{ON}$  degradation rises until 300-V and then it becomes smaller. Such effect has been previously observed [11]. Interestingly, the percentage of  $C_{OSS}$ -losses also decreases at almost the same voltage, suggesting a possible relationship between these two effects [2].

Recent measurements have shown considerable frequency independent  $C_{OSS}$ -losses in cascode transistors [8]. Figs. 4a and 4b, respectively show the measured  $v_{DS}$  and  $i_L$  of a Si/GaN cascode transistor. As shown in Fig. 4c, the device exhibits relatively low  $C_{OSS}$ -losses at low voltages ( $V_{DS} < 200$  V), however,  $E_{DISS}$  becomes considerable at higher drain-source voltages. Fig. 4c shows that by changing  $L$ , it is possible to cover a wide variety of different frequencies and  $dv/dt$  values. For instance, an inductance of 500-nH results in a very high frequency and  $dv/dt$  of 33 MHz and 87 V/ns, respectively. To obtain the same frequency with the ST method, a power amplifier with a high power delivery of  $\sim 4$  kW at the same frequency is needed, while the proposed method just relies on an ordinary dc power supply.

#### IV. CONCLUSION

In this work we used an energy-oriented measurement method to quantify  $C_{OSS}$ -losses in SJ and GaN transistors. Measurements on SJ devices showed identical small-signal and large-signal (in discharge cycle)  $E_{OSS}$ , although the  $E_{OSS}$  in the discharging cycle is considerably lower than those measured in charging cycle. Measurements on a GaN HEMTs indicated that

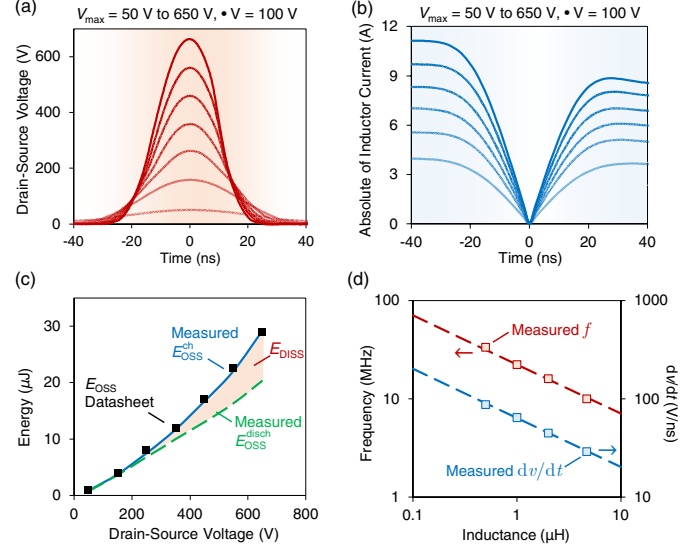


Fig. 4. (a) Measured  $v_{DS}$  at different voltage levels  $V_{max} = 50$  V, 150 V, 250 V, 350 V, 450 V, 550 V, and 650 V for a cascode GaN transistor together with (b) current waveforms. (c) Extracted  $C_{OSS}$  charging/discharging energies and data reported in datasheet as well as the extracted  $C_{OSS}$  loss ( $E_{DISS}$ ). (d) Measured (discrete points) and modeled (dashed lines) frequency and  $dv/dt$  versus inductance  $L$ .

both the  $R_{ON}$  degradation and the relative  $C_{OSS}$ -losses ( $E_{DISS}/E_{OSS}$ ) increased up to  $\sim 300$  V, and then decreased up to the device voltage rating. These results provide new insights on  $C_{OSS}$ -losses in SJ and GaN-on-Si power transistors, which is essential in designing high-frequency power converters.

#### REFERENCES

- [1] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active power device selection in high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6818–6833, Jul. 2019.
- [2] M. Guacci, et al. "On the origin of the  $C_{OSS}$ -losses in soft switching GaN-on-Si power HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 679–694, Jun. 2019.
- [3] Z. Tong, G. Zulauf, J. Xu, J. D. Plummer, and J. Rivas-Davila, "Output capacitance loss characterization of silicon carbide schottky diodes," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 856–878, Jun. 2019.
- [4] G. Zulauf, S. Park, W. Liang, K. Surakitbovorn, and J. Rivas-Davila, " $C_{OSS}$  losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10748–10763, Dec. 2018.
- [5] G. D. Zulauf, J. Roig-Guitart, J. D. Plummer, and J. M. Rivas-Davila, " $C_{OSS}$  measurements for superjunction MOSFETs: Limitations and opportunities," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 578–584, Jan. 2019.
- [6] J. Fedison, M. Fornage, M. Harrison, and D. Zimmanck, " $C_{OSS}$  related energy loss in power MOSFETs used in zero-voltage-switched applications," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 150–156.
- [7] J. Roig and F. Bauwens, "Origin of anomalous  $C_{OSS}$  hysteresis in resonant converters with superjunction FETs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3092–3094, Sep. 2015.
- [8] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of large-signal  $C_{OSS}$  and  $C_{OSS}$  losses of transistors based on nonlinear resonance," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2242–2246, Mar. 2020.

- [9] K. Surakitbovorn and J. Rivas-Davila, "Evaluation of GaN transistor losses at MHz frequencies in soft switching converters," in Proc. IEEE 18th Workshop Control Modelling Power Electron. (COMPEL), Stanford, CA, USA, Jul. 2017.
- [10] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "New insights on output capacitance losses in wide-band-gap transistors," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6663-6667, Mar. 2020.
- [11] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic on-state resistance test and evaluation of GaN power devices under hard-and soft-switching conditions by double and multiple pulses," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1044-1053, Feb. 2019.