Resonances on GaN-on-Si Epitaxies: A Source of Output Capacitance Losses in Power HEMTs

Mohammad Samizadeh Nikoo, Riyaz Abdul Khadar, Armin Jafari, Minghua Zhu, *Student Member*, *IEEE*,
and Elison Matioli, *Member*, *IEEE*

Abstract—GaN-on-Si high-electron-mobility transistors (HEMTs) exhibit excellent properties for efficient power conversion. Nevertheless, a considerable energy loss associated with the charging and discharging of the output capacitance (C_{OSS}) in these transistors severely limits their application at high switching frequencies. In this work we report the observation of unexpected resonances in GaN-on-Si HEMTs. These high-frequency resonances lead to considerable energy losses in fast charging and discharging of the C_{OSS} during switching transients. We propose a simple wafer-level measurement technique to evaluate such losses at the epitaxy level, prior to the transistor fabrication. Experimental results from this technique revealed that the Silicon substrate is the main origin of these losses. Such wafer-level evaluation of C_{OSS} losses opens opportunities to characterize and optimize epitaxies for future power devices, especially those operating at high switching frequencies.

Index Terms—Output capacitance, C_{OSS}, C_{OSS} losses, E_{DISS}, GaN, HEMT, AlGaN/GaN, Si substrate.

I. INTRODUCTION

THE-LOWER-THAN-EXPECTED efficiency of high-frequency soft-switching power converters based on GaN high-electron-mobility transistors (HEMTs) highlighted the energy dissipation (E_{DISS}) in charging and discharging of their output capacitance (C_{OSS}) [1]-[10]. The initial studies using the Sawyer–Tower (ST) technique revealed a lossy behavior in the C_{OSS}-charging/discharging process, however, the magnitude of the measured losses by sinusoidal excitation was smaller than the amount of losses in real switching transients [2]. Further investigations showed that the origin of the C_{OSS} losses was in the epitaxial structure of power HEMTs [3]-[5], which was completely different from the previously-observed C_{OSS} losses in super-junction (SJ) transistors [11], [12]. A precise characterization, and ultimately reduction, of E_{DISS} in power epitaxies is of great importance, especially for power devices operating at high switching-frequencies, where C_{OSS} losses can be even larger than conduction losses [13].

Low parasitic-capacitances of GaN power transistors enable ultra-fast nanosecond switching times [14], [15], resulting in extremely high-frequency harmonics, well-beyond 100 MHz. Nevertheless, practical considerations limit the frequency characterization of C_{OSS} losses to typically less than 40 MHz [2], [7]. Packaging and external-connection parasitics are other limitations hindering the accurate measurement of C_{OSS} losses at very high frequencies. In this work we present a precise on-wafer measurement technique to evaluate C_{OSS} losses due to the epitaxial structure. This method uses a small-signal

modeling approach to evaluate large-signal C_{OSS} losses [8], [9], which quantifies frequency-dependent energy dissipation in the C_{OSS} [10]. The extremely low parasitics provided by this method enables the measurement of C_{OSS}-related losses at very high frequencies >100 MHz. This provides a general characterization method of epitaxial structures, enabling their optimization prior to the transistor fabrication. This new technique revealed unexpected resonant lossy-peaks in GaN-on-Si epitaxies, which were identified to be mainly due to the Silicon substrate.

II. METHODOLOGY

The output capacitance of a power HEMT mainly consists of three parts: gate-drain capacitance (C_{GD}), drain-substrate capacitance through the vertical epitaxial structure (C_{epi}), and drain-source capacitance through the two-dimensional electron gas (2DEG) (C_{lat}). In power (MOS)HEMTs, C_{GD} is significantly smaller than the two other terms, so that one can consider $C_{OSS} = C_{epi} + C_{lat}$ (Fig. 1a). By applying drain-source voltage in the OFF-state, the 2DEG under the gate is depleted, resulting in a considerable reduction in C_{lat} and C_{OSS}. At high enough drain-source voltages, C_{OSS} becomes constant, approximately equal to C_{epi} (Fig. 1b) [5]. C_{epi} has been presented as the significant part of C_{OSS} and also the main source of C_{OSS} losses in power HEMTs [5]. This is a vertical capacitance sandwiched between drain pad and silicon substrate, so the capacitance mainly depends on the area of the drain pad, independent from the device layout. Although the characterization of high-frequency losses of RF epitaxies has been proposed in the literature [6], there is little knowledge on high-frequency losses of power epitaxies.

Here we present a wafer-level measurement method based on a simple proposed test structure (Fig. 2a) including a signal and ground pads to extract losses due to the epitaxial structure, which is the main source of C_{OSS} losses. The signal pad dimensions should be considerably larger than thickness of the insulating epitaxy so that the effect of fringing fields can be neglected. The RF signal pad is surrounded by a considerably larger ground pad. The ground pad forms a giant capacitance (C_∞) with the substrate, which grounds the doped silicon
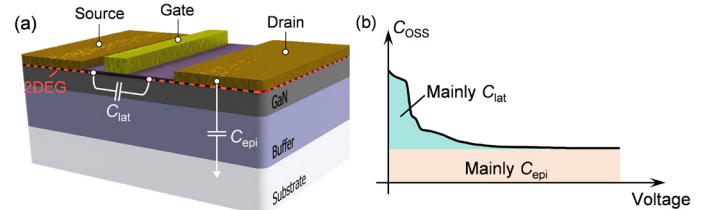

Fig. 1. (a) Simplified structure of an AlGaN/GaN HEMT showing its output capacitance $C_{OSS} = C_{GD} + C_{epi} + C_{lat}$. In practice the effect of $C_{GD} \ll C_{OSS}$ is negligible. (b) C_{OSS} versus V_{DS} curve for a commercial device showing that C_{epi} dominates at high drain-source voltages.
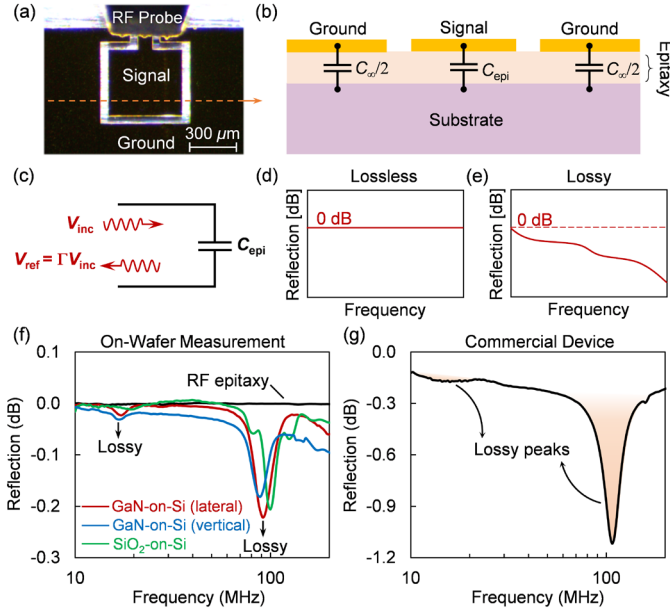
Fig. 2. (a) Optical image of the test structure measured with an RF probe. (b) Cross-section illustration of the proposed test structure. (c) Measurement method to extract losses from output capacitance to characterize epitaxial structures. Illustration of reflection coefficient for (d) lossless, and (e) lossy epitaxies. (f) Measurement results for an RF epitaxy (GaN-on-SiC), together with two GaN-on-Si power epitaxies (corresponding to a lateral HEMT and a vertical MOSFET), as well as a SiO₂-on-Si test structure. (g) Measurement results for a 600-V-rated commercial device showing similar lossy peaks.

substrate at radio frequencies (Fig. 2b). The test structure shown is examined with an incident wave with amplitude V_{inc}, and the reflection coefficient $\Gamma = V_{ref}/V_{inc}$, in which V_{ref} is the reflected wave amplitude, is measured by a network analyzer (Fig. 2c). A frequency sweep of V_{inc} gives full information on the behavior of the device under test (DUT), including its circuit model and losses. A lossless C_{epi} results in the total reflection of the incident wave, thus Γ is equal to 0 dB (Fig. 2d). Whereas a lossy C_{epi} results in a partial reflection of the incident wave, thus in negative values of Γ (Fig. 2e).

One can extract the impedance of the DUT using

$$Z = Z_0 (1+\Gamma)/(1-\Gamma). \quad (1)$$

where $Z_0 = 50\ \Omega$ is the measurement port characteristic impedance. The quality factor Q of the capacitor is obtained as

$$Q = \text{Im}(Z)/\text{Re}(Z) \quad (2)$$

where $\text{Im}(Z)$ and $\text{Re}(Z)$ represent the imaginary and real parts of Z, respectively. For a capacitive element, the amount of charging/discharging losses (between 0 to V) is inversely proportional to its Q, as

$$E_{diss} = \frac{\pi}{2Q} E_{tot} \quad (3)$$

where $E_{tot} = \frac{1}{2}CV^2$ is the total energy stored in the capacitor when charged to the voltage V. Thus $\pi/(2Q)$ represents the percentage of energy losses.

Fig. 2a shows the fabricated experimental structure. The size of the signal and ground pads are 0.24 mm² and 3.7 mm², respectively, and the thickness of the pads is 300-nm (270-nm gold with 30-nm titanium adhesion layer). A ground-signal-ground (GSG) RF probe connected to a network analyzer (Keysight N5225A) was used to measure the reflection coefficient at different frequencies, with the lowest possible parasitics and an extremely high bandwidth of 50 GHz. Fig. 2f shows the measured reflection coefficient from test structures fabricated on four different epitaxies: GaN-on-SiC RF epitaxy,

GaN-on-Si power epitaxies for lateral HEMTs and vertical MOSFETs, and a test SiO₂-on-Si wafer. In all cases, we fabricated devices on 2 cm × 1.8 cm chips diced from 6-inch wafers. All samples on Si substrates (p-type with a resistivity of ~ 0.02 Ω·cm) exhibited considerably higher losses with respect to the reference RF epitaxy, with two pronounced peaks at ~17 MHz and ~90 MHz. The presence of lossy peaks (especially the larger one at higher frequency) for the SiO₂-on-Si sample (with no GaN layer) suggests that that the Si substrate is a potential origin of C_{OSS} losses in GaN-on-Si HEMTs. We also observed very similar lossy peaks in some commercial GaN-on-Si power HEMTs (Fig. 2g). In this case – in an off-chip measurement – we measured the reflection coefficient from drain-source of the commercial transistor, while the gate was shorted to the source. The vertical GaN-on-Si epitaxy also presented similar lossy peaks. In this case, the drift layer is lightly doped which results in a leakage current between the signal and the ground pads. This causes a lossy behavior over all frequencies and so a lower Q factor. This effect can be seen in Fig. 2(f), where the vertical epitaxy (blue) shows higher background losses. Therefore, the proposed method reveals all sorts of power dissipations including resonant and leakage losses.

III. RESULTS

We used the proposed method to quantify the amount of output capacitance losses due to these resonances for epitaxies with different buffer thicknesses. Using (1) and (3), we extracted the capacitance as well as the losses related to C_{epi}, for two GaN-on-Si power epitaxies 4-μm (Fig. 3a) and 5-μm (Fig. 3b) buffer thicknesses (similar to the lateral GaN-on-Si epitaxy shown in Fig. 2(f)). There are two distinct peaks corresponding to losses for both epitaxies. Exactly at these peaks, abrupt changes in capacitance are observed, which shows a resonance happening in the epitaxial structure. Although the second epitaxy is 25% thicker than the first one, the resonance frequencies are very close, showing a material dependency of such resonances. As expected, the thicker buffer has a lower capacitance and so a lower stored energy while the dominant part of losses due to the substrate is about the same. This results in a higher relative losses for the thicker epitaxy.

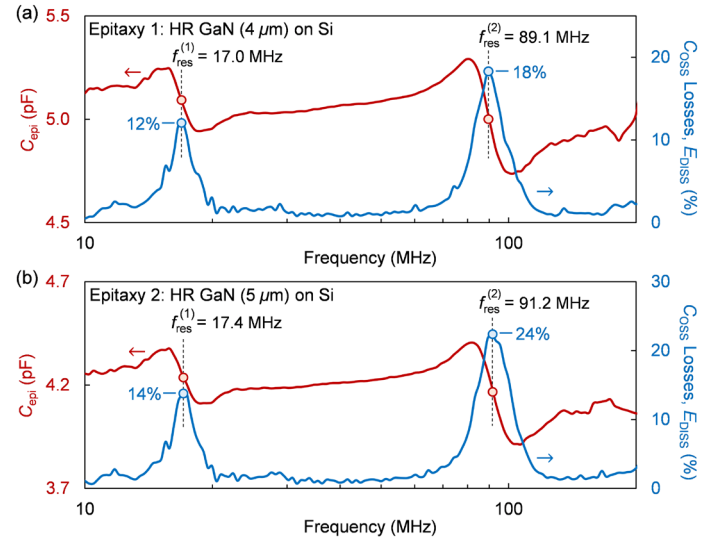Fig. 3 shows the importance of characterizing C_{OSS} losses at

Fig. 3. Extracted capacitance and losses of the test capacitor on (a) 4-μm-thick, and (b) 5-μm-thick carbon-doped high-resistive (HR) GaN buffers. In both cases, there are lossy resonances at ~17 MHz, and ~90 MHz.
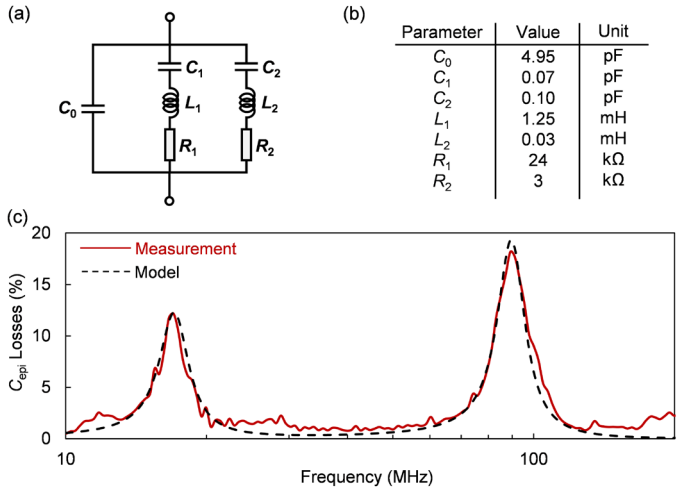
Fig. 4. (a) Proposed circuit model for output capacitance losses, together with (b) circuit parameters of the 4-μm-thick buffer sample. (c) Measured (solid line) and modeled (dashed line) C_{epi} losses.

high frequencies, since a low frequency test, for instance up to 10 MHz, would not show such significant frequency-dependent losses happening at high frequencies. This could be a potential reason of higher measured losses with pulse excitation (containing higher harmonics) in comparison to sine-wave in ST method [2]. For instance, at 10-MHz, the employed pulse waveform in [2] had a 5-ns rise-time, and the C_{OSS} losses corresponding to this waveform was not limited to the fundamental frequency of 10-MHz, but it included all the frequency content of the pulse, exceeding 100-MHz. This also shows that single-tone ST measurements, previously performed up to 35 MHz [2], [13], should be performed at much higher frequencies to cover the typical switching harmonics of wide-band-gap transistors. In addition, Fig. 3 shows a 1-2% loss over a wide frequency range, which indicates the ability of the proposed method in capturing background C_{epi} losses, caused by other phenomena such as the resistivity of substrate.

A circuit model of the C_{epi} can be extracted from the results shown in Fig. 3. The model includes a lossless capacitor C_0 in parallel with two lossy RLC resonant branches (Fig. 4a). Fig. 4b shows the extracted circuit parameters for the 4-μm-thick buffer. Fig. 4c presents the measured and modeled C_{epi} power dissipation, showing a good agreement between them. We employed the model presented in Fig. 4a in a circuit-level simulation with LTspice to extract the amount of C_{OSS} losses due to these resonances for different switching times. Fig. 5a shows the power dissipated in R_1 and R_2 (Fig. 4a) representing the low-frequency and high-frequency resonances. The switching time and voltage are 2-ns and 400-V, respectively. The results for 5-ns switching at the same switching voltage level are shown in Fig. 5b. As expected, the high-frequency resonance leads to much higher losses for the faster switching transient. The low-frequency resonance, however, is considerably slower than the typical switching transient of a GaN transistor, so both switching times of 2-ns and 5-ns lead to an almost equal power loss. It should be noted that the power loss continues happening after the switching transient is finished. For example for low-frequency resonance, there is a considerable power loss even 100-ns after the switching transient. This cannot be observed in the previous simplified models of output capacitance losses [4], since they do not show any resonances. Fig. 5c shows the C_{OSS}-related energy
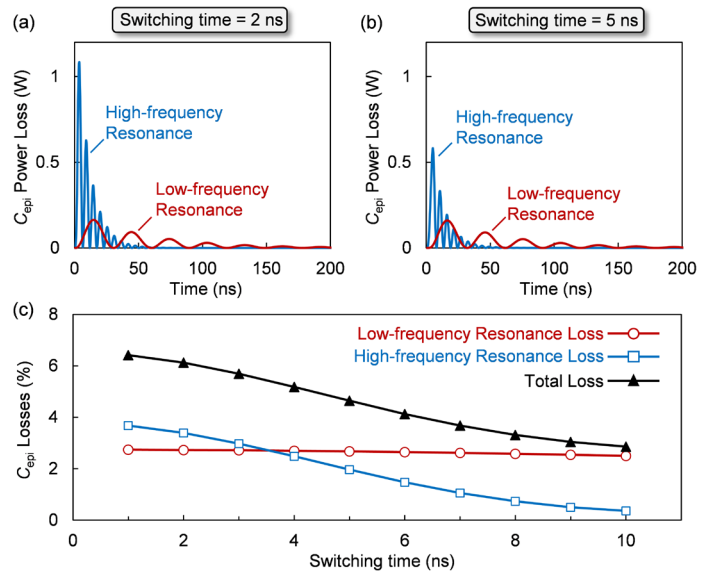

Fig. 5. Simulated C_{OSS} power losses of the 4-μm-thick buffer sample for 400-V (a) 2-ns, and (b) 5-ns switching transients. The plots show separately the power loss representative for the low- and high-frequencies resonates. (c) Extracted C_{OSS} energy dissipation corresponding to the low- and high-frequencies resonates, as well as the total loss.

dissipation versus switching time for 400-V switching, from 1 to 10 ns, as well as the share of each resonance in the total loss. For fast switching transients, about 6% of the stored energy is dissipated during charging and discharging. This number is higher for the 5-μm-thick buffer and can reach to about 8% of the stored energy, showing that C_{OSS} losses can be potentially more severe for devices with a higher blocking voltage capability.

IV. CONCLUSION

We proposed a new on-wafer test method to characterize C_{OSS}-related losses in a power epitaxy. Measurements on different power epitaxies revealed new insights on C_{OSS}-related losses. Two lossy resonances at 17 MHz and 90 MHz were observed, which are of very different nature from previously proposed models and opens opportunities for further investigations. The proposed method can be used to evaluate and optimized power wafers at the epitaxial level for future power electronic devices operating at high switching frequencies.

REFERENCES

[1] K. Surakitbovorn and J. Rivas-Davila, "Evaluation of GaN transistor losses at MHz frequencies in soft switching converters," in *Proc. IEEE 18th Workshop Control Modelling Power Electron. (COMPEL)*, Jul. 2017. doi: 10.1109/COMPEL.2017.8013330.

[2] G. Zulauf, S. Park, W. Liang, K. Surakitbovorn, and J. Rivas-Davila, "C_{OSS} losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10748–10763, Dec. 2018. doi: 10.1109/TPEL.2018.2800533.

[3] M. Guacci, M. Heller, D. Neumayr, D. Bortis, J. W. Kolar , G. Deboy, C. Ostermaier, and O. Häberlen, "On the origin of the C_{OSS}-losses in soft switching GaN-on-Si power HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 679-694, Jun. 2019. doi: 10.1109/JESTPE.2018.2885442.

[4] J. Zhuang, G. Zulauf, J. Roig, J. D. Plummer, and J. Rivas-Davila, "An Investigation into the Causes of C_{OSS} Losses in GaN-on-Si HEMTs," in *Proc. IEEE 20th Workshop Control Modelling Power Electron. (COMPEL)*, Jun. 2019. doi: 10.1109/COMPEL.2019.8769661.

[5] J. Zhuang, G. Zulauf, and Juan Rivas-Davila, "Substrate bias effect on e-mode GaN-on-Si HEMT C_{OSS} losses," in *Proc. IEEE 19th Workshop*

Control Modelling Power Electron. (COMPEL), Jun. 2018. doi: 10.1109/WiPDA.2018.8569205.

[6]   H. Chandrasekar, M. J. Uren, M. A. Casbon, H. Hirshy, A. Eblabla, K. Elgaid, J. W. Pomeroy, P. J. Tasker, and M. Kuball, "Quantifying Temperature-Dependent Substrate Loss in GaN-on-Si RF Technology," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1681-1687, April 2019. doi: 10.1109/TED.2019.2896156.

[7]   M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of large-signal output capacitance of transistors based on nonlinear resonance," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2242-2246, Mar. 2020. doi: 10.1109/TPEL.2019.2938922.

[8]   M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "New insights on output capacitance losses in wide-band-gap transistors," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6663-6667, Jul. 2020. doi: 10.1109/TPEL.2019.2958000.

[9]   M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Output capacitance losses in wide-band-gap transistors: a small-signal modeling approach," *2020 Int. Symp. On Power Semiconductor Devices and ICs*, Sep. 2020, pp. 190-193. doi: 10.1109/ISPSD46842.2020.9170093.

[10] N. Perera, A. Jafari, L. Nela, G. Kampitsis, M. Samizadeh Nikoo, and E. Matioli, "Output-capacitance hysteresis losses of field-effect transistors," in *Proc. IEEE 21th Workshop Control Modelling Power Electron. (COMPEL)*, Nov. 2020. doi: 10.1109/COMPEL49091.2020.9265823.

[11] J. Roig and F. Bauwens, "Origin of anomalous C_{OSS} hysteresis in resonant converters with superjunction FETs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3092–3094, Sep. 2015. doi: 10.1109/TED.2015.2455072.

[12] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016. doi: 10.1109/TPEL.2016.2574998.

[13] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active power device selection in high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6818–6833, Jul. 2019. doi: 10.1109/TPEL.2018.2874420.

[14] S. Moench, P. Hillenbrand, P. Hengel, and I. Kallfass, "Pulsed measurement of sub-nanosecond 1000 V/ns switching 600 V GaN HEMTs using 1.5 GHz low-impedance voltage probe and 50 Ohm scope," in *Proc. IEEE 5th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct./Nov. 2017, pp. 132–137. doi: 10.1109/WiPDA.2017.8170535.

[15] J. W. Simonaitis, B. Slayton, Y. Yang-Keathley, P. D. Keathley, and K. K. Berggren, "Precise, sub-nanosecond, and high-voltage switching of complex loads enabled by gallium nitride electronics," arXiv:2102.03271, 2021.