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Cryogenic CMOS Integrated Circuits for Scalable Readout of Silicon Quantum Computers

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“Un paese ci vuole, non fosse che per il gusto di andarsene via. Un paese vuol dire non essere soli, sapere che nella gente, nelle piante, nella terra, c’è qualcosa di tuo, che anche quando non ci sei resta ad aspettarti. Ma non è facile starci tranquillo.”
— Cesare Pavese, *La luna e i falò*

A mamma, papà e Marco,
per essermi sempre vicini anche da lontano…

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Abstract

Quantum computing promises to revolutionize our lives, achieving unprecedented computational powers and unlocking new possibilities in drug discovery, chemical simulations and cryptography. The fundamental unit of computation of a quantum computer is the quantum bit (qubit). It can be implemented in a number of technologies, such as superconducting qubits, spin qubits, photonic systems, trapped ions and NV-centers. Solid-state superconducting qubits and spin qubits seem to be the most promising ones, as shown by the recent demonstration of quantum supremacy with a superconducting qubit processor. Such quantum processors, to operate in the quantum regime, require very low temperatures around 10 mK, and they are hence kept inside dilution fridges. The electronics required to read out and control such processors is typically realized by discrete components or bulky scientific instruments at room temperature wired into the dilution fridge. Such approach is only feasible until few (< 100) qubits are handled, but it is not scalable for million-qubit processors required for fault-tolerant operation.

In this thesis, readout and control electronics is proposed to be integrated and operated directly at cryogenic temperatures, in close proximity with the qubits and potentially even co-integrated. CMOS technology is advocated for its scalability, compactness and low prototyping cost, to create a comprehensive cryo-CMOS class of fully-integrated transceivers to read out and control solid-state qubits. In particular, the thesis focuses on cryo-CMOS radio-frequency integrated circuits for the readout of silicon quantum computers, looking to integrate the whole readout system, from the quantum layer to the room temperature user interface.

Cryogenic CMOS devices are explored first, to lay the foundations of integrated circuit design. The realization of quantum dots in standard CMOS technology is explored as a platform to realize solid-state qubit arrays, demonstrating functionality at 50 mK and good reproducibility. Moreover, the operation of integrated transistors at 50 mK and 4.2 K is explored to understand their basic cryogenic functionality, through characterization and modeling. Then also integrated passives, such as capacitors, inductors and transformers, are studied and modeled at cryogenic temperatures.

Then, a fully-integrated readout platform spanning across all the blocks needed for dispersive readout is proposed. A fully-integrated matrix of quantum dots with radio-frequency gate-based readout capabilities is demonstrated along with time- and frequency-multiplexing. This quantum-classical circuit shows all the features for a scalable approach and is the core of the platform following it. A cryogenic CMOS circulator based on a new all-pass filter architecture is demonstrated, to be used as integrated replacement for current bulky counterparts; it allows power reduction, insertion loss and bandwidth enhancement with respect to state-of-the-art integrated circulators. The rest of the front-end is also

explored with dedicated test multiplexers, a low noise-amplifier and an oscillator, that are finally merged in a single fully-integrated low-noise receiver with frequency synthesizer operating at 3.5 K for scalable multiplexed readout of silicon qubits.
The platform presented in this thesis, across temperature boundaries, carries all the features required for future scalable silicon quantum computing platforms and could therefore form their core.

Keywords: Quantum computer, quantum processor, spin qubit, quantum dot, scalability, cryogenic characterization, modeling, cryo-CMOS, quantum integrated circuit, radio-frequency integrated circuit, gate-based reflectometry, multiplexing, circulator, low-noise amplifier, low-noise receiver.

Sommario

Il calcolo quantistico promette di rivoluzionare le nostre vite, raggiungendo potenze di calcolo mai ottenute finora e aprendo nuove possibilità nella scoperta di medicinali, simulazioni chimiche e crittografia. L'unità di calcolo fondamentale di un calcolatore quantistico è il quantum bit (qubit). Esso può essere realizzato in diverse tecnologie, come i qubit superconduttivi, i qubit di spin, sistemi fotonici, trappole ioniche, o centri azoto-vacanza. I qubit a stato solido superconduttivi o di spin sembrano essere i più promettenti, come indicato dalla recente dimostrazione di supremazia quantistica con un processore quantistico superconduttivo.
Tali calcolatori quantistici, per operare nel regime quantistico, richiedono temperature molto basse, intorno a 10 mK, e pertanto sono tenuti dentro a dei refrigeratori a diluizione. L'elettronica richiesta per leggere e controllare tali processori è di norma realizzata da componenti discreti o voluminosi strumenti scientifici a temperatura ambiente collegati da cavi dentro al refrigeratore a diluizione. Tale approccio è possibile soltanto finchè pochi (< 100) qubit sono trattati, ma non è scalabile a processori da milioni di qubit, come richiesto da un'operazione tollerante agli errori quantistici.
In questa tesi, si propone di integrare l'elettronica di lettura e controllo e di operarla direttamente a temperature criogeniche, a stretto contatto con i qubit e potenzialmente perfino cointegrata. La tecnologia CMOS è raccomandata per la sua scalabilità, compattezza e basso costo di prototipazione, per creare una classe comprensiva di ricetrasmettitori criogenici CMOS completamente integrati per leggere e controllare qubit a stato solido. In particolare, questa tesi si concentra su circuiti criogenici CMOS integrati a radiofrequenza per la lettura di calcolatori quantistici in silicio, nella prospettiva di integrare l'intero sistema di lettura, dal livello quantistico all'interfaccia con l'utente a temperatura ambiente.
I dispositivi criogenici CMOS sono esplorati per primi, per porre le basi della progettazione di circuiti integrati criogenici. La realizzazione di punti quantistici in tecnologia standard CMOS è esplorata come piattaforma per realizzare matrici di qubit a stato solido, dimostrandone la funzionalità a 50 mK e buona riproducibilità. Inoltre, l'operazione di transistor integrati a 50 mK e 4.2 K è studiata per caprine la funzionalità criogenica di base, per mezzo di caratterizzazione e modellizzazione. Poi anche i componenti passivi integrati, come condensatori, induttori e trasformatori, sono studiati e modellizzati a temperature criogeniche.
In seguito, viene proposta una piattaforma di lettura completamente integrata che percorre i vari blocchi richiesti dalla tecnica di lettura dispersiva sul gate dei transistor. Una matrice completamente integrata di punti quantistici con capacità di lettura a radiofrequenza sul gate dei transistor è dimostrata insieme alla multiplazione nel dominio del tempo e della frequenza. Questo circuito quantistico-classico mostra tutte le caratteristi-

che richieste per un approccio scalabile ed è il cuore della piattaforma che lo segue. Un circolatore criogenico in CMOS basato su una nuova architettura di filtri passa-tutto è dimostrato, per essere usato come sostituto integrato delle corrispettive parti discrete; permette riduzione di potenza consumata e di perdita d'inserzione e un aumento di banda rispetto a circolatori integrati allo stato dell'arte. Anche il resto dell'interfaccia frontale è esplorato con dei multiplatori, un amplificatore a basso rumore e un oscillatore, che alla fine sono uniti in un singolo ricevitore a basso rumore completamente integrato con sintetizzatore di frequenza che opera a 3.5 K per la lettura scalabile e multipla di qubit al silicio.
La piattaforma presentata in quesa tesi, attraverso diverse regioni di temperatura, possiede tutte le caratteristiche richieste dalle piattaforme di calcolo quantistico scalabili al silicio e potrebbe pertanto formarne la base in futuro.

Parole chiave: Calcolatore quantistico, processore quantistico, qubit di spin, punto quantistico, scalabilità, caratterizzazione criogenica, modellizzazione, CMOS criogenico, circuito integrato quantistico, circuito integrato a radiofrequenza, riflettometria sul gate, multiplazione, circolatore, amplificatore a basso rumore, ricevitore a basso rumore.

Résumé

L'informatique quantique promet de révolutionner nos vies, en atteignant des puissances de calcul sans précédent et en ouvrant des nouvelles possibilités dans la découverte de médicaments, les simulations chimiques et la cryptographie. L'unité fondamentale de calcul d'un ordinateur quantique est le bit quantique (qubit). Il peut être réalisé avec plusieurs technologies, telles que les qubits supraconducteurs, les qubits de spin, les systèmes photoniques, les ions piégés et les centres azote-lacune. Les qubits à l'état solide supraconducteurs et de spin semblent être les plus prometteurs, comme le montre la récente démonstration de la suprématie quantique avec un processeur de qubits supraconducteurs.

Ces processeurs quantiques, pour fonctionner dans le régime quantique, nécessitent des températures très basses, autour de 10 mK, et ils sont donc conservés dans des réfrigérateurs à dilution. L'électronique nécessaire pour lire et contrôler ces processeurs est généralement réalisée par des composants discrets ou des instruments scientifiques volumineux à température ambiante câblés dans le réfrigérateur à dilution. Une telle approche n'est possible que jusqu'à ce que quelques qubits (< 100) soient traités, mais elle n'est pas extensible pour les processeurs de millions de qubits nécessaires à un fonctionnement tolérant aux erreurs quantiques.

Dans cette thèse, il est proposé d'intégrer et de faire fonctionner l'électronique de lecture et de contrôle directement à des températures cryogéniques, à proximité immédiate des qubits et potentiellement même co-intégrée avec. La technologie CMOS est préconisée pour son extensibilité, sa compacité et son faible coût de prototypage, afin de créer une classe complète d'émetteurs-récepteurs CMOS cryogéniques entièrement intégrés pour lire et contrôler les qubits à l'état solide. La thèse se concentre en particulier sur les circuits intégrés CMOS cryogéniques à radiofréquence pour la lecture des ordinateurs quantiques en silicium, en cherchant à intégrer l'ensemble du système de lecture, de la couche quantique à l'interface utilisateur à température ambiante.

Les dispositifs CMOS cryogéniques sont explorés d'abord, pour jeter les bases de la conception des circuits intégrés. La réalisation de points quantiques dans la technologie CMOS standard est explorée comme une plate-forme pour réaliser des matrices de qubits à l'état solide, démontrant la fonctionnalité à 50 mK et une bonne reproductibilité. En outre, le fonctionnement des transistors intégrés à 50 mK et 4.2 K est exploré pour comprendre leur fonctionnalité cryogénique de base, au moyen de la caractérisation et de la modélisation. Puis, les passifs intégrés, tels que les condensateurs, les inductances et les transformateurs, sont également étudiés et modélisés à des températures cryogéniques.

Ensuite, une plate-forme de lecture entièrement intégrée couvrant tous les blocs nécessaires à la lecture dispersive sur la grille des transistors est proposée. Une matrice

entièrement intégrée de points quantiques avec des capacités de lecture dispersive à radiofréquence sur la grille des transistors est démontrée avec le multiplexage en temps et en fréquence. Ce circuit quantique-classique présente toutes les caractéristiques requises pour une approche extensible et constitue le cœur de la plate-forme qui le suit. Un circulateur CMOS cryogénique basé sur une nouvelle architecture de filtres passe-tout est démontré, pour être utilisé comme remplacement intégré des circulateurs encombrants actuels ; il permet une réduction de la puissance, de la perte d'insertion et une amélioration de la bande passante par rapport aux circulateurs intégrés de pointe. Le reste du circuit frontal est également exploré avec des multiplexeurs de test dédiés, un amplificateur à faible bruit et un oscillateur, qui sont finalement combinés en un seul récepteur à faible bruit entièrement intégré avec un synthétiseur de fréquence fonctionnant à 3.5 K pour une lecture multiplexée extensible des qubits de silicium.
La plate-forme présentée dans cette thèse, à travers différentes régions de température, comporte toutes les caractéristiques requises pour les futures plates-formes de calcul quantique en silicium extensibles et pourrait donc en constituer le cœur.

Mots-clés : Ordinateur quantique, processeur quantique, qubit de spin, point quantique, extensibilité, caractérisation cryogénique, modélisation, CMOS cryogénique, circuit intégré quantique, circuit intégré à radiofréquence, réflectométrie sur la grille, multiplexage, circulateur, amplificateur à faible bruit, récepteur à faible bruit.

Zusammenfassung

Quantencomputer versprechen, unser Leben zu revolutionieren, indem sie eine noch nie dagewesene Rechenleistung erreichen und neue Möglichkeiten in der Medikamentenentwicklung, chemischen Simulationen und Kryptographie erschließen. Die fundamentale Berechnungseinheit eines Quantencomputers ist das Quantenbit (Qubit). Es kann in einer Reihe von Technologien implementiert werden, sowie supraleitenden Qubits, Spin-Qubits, photonischen Systemen, gefangenen Ionen und Stickstoff-Fehlstellen-Zentren. Festkörper supraleitende Qubits und Spin-Qubits scheinen die vielversprechendsten zu sein, wie die jüngste Demonstration der Quantenüberlegenheit mit einem supraleitenden Qubit-Prozessor zeigt.
Solche Quantenprozessoren benötigen, um im Quantenregime zu arbeiten, sehr niedrige Temperaturen, etwa 10 mK, und werden daher in Verdünnungskühlschränken gehalten. Die Elektronik, die zum Auslesen und Steuern solcher Prozessoren benötigt wird, wird typischerweise durch diskrete Komponenten oder sperrige wissenschaftliche Instrumente bei Raumtemperatur realisiert, die mit dem Verdünnungskühlschrank verkabelt sind. Ein solcher Ansatz ist nur bis zu wenigen (< 100) Qubits praktikabel, aber für Millionen-Qubit-Prozessoren, die für einen quantenfehlertoleranten Betrieb benötigt werden, nicht skalierbar.
In dieser Arbeit wird vorgeschlagen, die Auslese- und Steuerelektronik direkt bei kryogenen Temperaturen zu integrieren und zu betreiben, in unmittelbarer Nähe zu den Qubits und möglicherweise sogar ko-integriert. Die CMOS-Technologie wird wegen ihrer Skalierbarkeit, Kompaktheit und niedrigen Prototyping-Kosten befürwortet, um eine umfassende kryo-CMOS Klasse voll integrierter Transceiver zum Auslesen und Steuern von Festkörper-Qubits zu schaffen. Insbesondere konzentriert sich die Arbeit auf kryo-CMOS-Hochfrequenz-integrierte Schaltungen für das Auslesen von Silizium-Quantencomputern, um das gesamte Auslesesystem, von der Quantenschicht bis zur Benutzerschnittstelle bei Raumtemperatur, zu integrieren.
Zunächst werden kryogene CMOS-Bauelemente untersucht, um die Grundlagen für das Design der integrierten Schaltungen zu schaffen. Die Realisierung von Quantenpunkten in Standard-CMOS-Technologie wird als Plattform für die Realisierung von Festkörper-Qubit-Matrizen erforscht, wobei Funktionalität bei 50 mK und gute Reproduzierbarkeit demonstriert werden. Darüber hinaus wird der Betrieb von integrierten Transistoren bei 50 mK und 4.2 K erforscht, um deren grundlegende kryogene Funktionalität durch Charakterisierung und Modellierung zu verstehen. Dann werden auch integrierte passive Bauelemente, wie Kondensatoren, Induktivitäten und Transformatoren, bei kryogenen Temperaturen untersucht und modelliert.
Danach wird eine vollintegrierte Ausleseplattform vorgeschlagen, die alle Blöcke umfasst,

die für eine dispersive Gate-basierte Auslese benötigt werden. Eine vollintegrierte Matrix von Quantenpunkten mit hochfrequenten Gate-basierten Auslesemöglichkeiten wird zusammen mit Zeit- und Frequenz-Multiplexing demonstriert. Diese quantenklassische Schaltung zeigt alle Eigenschaften, die für einen skalierbaren Ansatz erforderlich sind, und ist das Herzstück der folgenden Plattform. Ein kryogener CMOS-Zirkulator, der auf einer neuen Allpass-Filter-Architektur basiert, wird demonstriert, um als integrierter Ersatz für die derzeitigen sperrigen Gegenstücke verwendet zu werden; er ermöglicht eine Leistungsreduzierung, Einfügungsdämpfungsreduzierung und Bandbreitenverbesserung im Vergleich zu den modernen integrierten Zirkulatoren. Der Rest des Front-Ends wird ebenfalls mit dedizierten Testmultiplexern, einem rauscharmen Verstärker und einem Oszillator erforscht, die schließlich in einem einzigen vollintegrierten rauscharmen Empfänger mit Frequenzsynthesizer zusammengeführt werden, der bei 3.5 K für das skalierbare gemultiplexte Auslesen von Silizium-Qubits arbeitet.
Die in dieser Arbeit vorgestellte Plattform trägt, über verschiedene Temperaturbereiche, alle Eigenschaften, die für zukünftige skalierbare Silizium-Quantencomputerplattformen erforderlich sind und könnte daher deren Kern bilden.

Schlüsselwörter: Quantencomputer, Quantenprozessor, Spin-Qubit, Quantenpunkt, Skalierbarkeit, kryogene Charakterisierung, Modellierung, Kryo-CMOS, integrierte Quantenschaltung, Hochfrequenz integrierte Schaltung, Gate-basierte Reflektometrie, Multiplexing, Zirkulator, rauscharmer Verstärker, rauscharmer Empfänger.

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List of Acronyms

2DEG	2-Dimensional Electron Gas
5G	5^{th} Generation
AC	Alternating Current
ADC	Analog-to-Digital Converter
AM	Amplitude Modulated
AP	AlCu Pad
ASIC	Application-Specific Integrated Circuit
AWG	Arbitrary Waveform Generator
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BSIM	Berkeley Short-channel Insulated-gate field-effect transistor Model
BW	Band-Width
CAD	Computer-Aided Design
CG	Common Gate
CML	Current-Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CP	Charge Pump
CPU	Central Processing Unit
CS	Common Source
DAC	Digital-to-Analog Converter
DC	Direct Current
DCO	Digitally-Controlled Oscillator
DGS	Dispersive Gate Sensing
DIBL	Drain-Induced Barrier Lowering
DRAM	Dynamic Random-Access Memory
DSP	Digital Signal Processor
DUT	Device Under Test
EBL	Electron-Beam Lithography
EKV	Enz-Krummenacher-Vittoz
EM	Electro-Magnetic
EOT	Effective Oxide Thickness
ESD	Electro-Static Discharge
FDMA	Frequency-Division Multiple Access
FDSOI	Fully-Depleted Silicon-On-Insulator
FET	Field-Effect Transistor

FOM	Figure Of Merit
FPGA	Field-Programmable Gate Array
FTR	Frequency Tuning Range
GSG	Ground Signal Ground
GSM	Global System for Mobile communications
HBT	Heterojunction Bipolar Transistor
HEMT	High-Electron-Mobility Transistor
I/O	Input/Output
I/Q	In-phase/Quadrature
IC	Inversion Coefficient
ID	Inductive Degeneration
IF	Intermediate Frequency
IIP3	3^{rd} order Input Intercept Point
IL	Insertion Loss
IM3	3^{rd} order Inter-Modulation
IR	Image Rejection
IRR	Image Rejection Ratio
ISF	Impulse Sensitivity Function
ITRS	International Technology Roadmap for Semiconductors
JPA	Josephson Parametric Amplifier
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
LPTV	Linear Periodic Time-Variant
MoM	Metal oxide Metal
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NC	Noise Cancelling
NF	Noise Figure
NISQ	Noisy Intermediate-Scale Quantum
NV	Nitrogen Vacancy
OIP3	3^{rd} order Output Intercept Point
OOK	ON-OFF Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Phase Detector
PDK	Process Design Kit
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PM	Phase Modulated
PN	Phase Noise
PPF	Poly-Phase Filter
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QD	Quantum Dot
QEC	Quantum Error Correction

QIP	Quantum Information Processing
QPC	Quantum Point Contact
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RSFQ	Rapid Single-Flux Quantum
SAW	Surface Acoustic Wave
SET	Single-Electron Transistor
SNR	Signal-to-Noise Ratio
SoC	System on Chip
SOI	Silicon-On-Insulator
SOLT	Short Open Load Through
SPI	Serial-to-Parallel Interface
SQUID	Superconducting QUantum Interference Device
SRF	Self-Resonance Frequency
SS	Subthreshold Swing
SSB	Single Side-Band
TDC	Time-to-Digital Converter
TDMA	Time-Division Multiple Access
TIA	Trans-Impedance Amplifier
VCO	Voltage-Controlled Oscillator
VLSI	Very Large-Scale Integration
VNA	Vector Network Analyzer
VSA	Vector Signal Analyzer
VSG	Vector Signal Generator

List of Symbols

α	Gate lever arm
A	Amplitude
ΔA	Amplitude change
β_φ	Phase error
B	Magnetic field
C	Capacitance
C_{ox}	Oxide capacitance
C_{q}	Quantum capacitance
δ_{cu}	Copper skin depth
e	Electron charge
ε_{r}	Relative dielectric permittivity
ε_{v}	Dielectric permittivity of vacuum
E	Energy
E_{c}	Charging energy
E_{J}	Josephson energy
E_{sat}	Saturation electric field
E_{Z}	Zeeman energy
f	Frequency
f_{T}	Transit frequency
F	Noise factor
F_{R}	Readout fidelity
g_{ds}	Drain-to-source transconductance
g_{L}	Landé g-factor
g_{m}	Gate transconductance
γ	Thermal noise excess factor
γ_{R}	Gyromagnetic ratio
G	Conductance
G_0	Quantum of conductance
G_{spec}	Specific transconductance
Γ	Reflection coefficient
h	Planck constant
H	Transfer function
I	Current
I_{c}	Josephson junction critical current
I_{ds}	Drain-to-source current
I_{spec}	Specific current

$\mathbf{j}$	Imaginary unit
k_B	Boltzmann constant
k_F	Fermi wavevector
k_m	Transformer coupling coefficient
λ	Wavelength
λ_c	Velocity saturation parameter
λ_F	Fermi wavelength
L	Inductance
L_g	Gate length
L_J	Josephson inductance
L_J0	Zero-flux Josephson inductance
L_sat	Saturation length
$\mathcal{L}$	Phase noise power spectral density
μ	Electrochemical potential
μ_0	Carrier mobility
μ_B	Bohr magneton
μ_r	Relative magnetic permeability
μ_v	Magnetic permeability of vacuum
n	Slope factor
ϕ	Phase
φ	Reflected phase
$\Delta\varphi$	Phase shift
Φ_0	Flux quantum
ψ	Wavefunction
P	Power
P_DC	Power consumption
q	Normalized charge
Q	Quality factor
Q_spec	Specific charge
ρ	Carrier density
R	Resistance
s	Laplace variable
σ	Shot noise excess factor
σ_cu	Copper conductivity
S	Scattering parameter
t	Time
t_d	Unit time delay
τ	Time constant
τ_s	Shot noise suppression factor
T	Absolute temperature
T_d	Time delay
T_eq	Noise-equivalent temperature
T_m	Clock period
U	Potential energy
U_T	Thermal voltage
v	Normalized voltage

v_{sat}	Saturation velocity
V	Voltage
V_{A}	Early voltage
V_{ds}	Drain-to-source voltage
V_{gs}	Gate-to-source voltage
$V_{\mathrm{g,1st}}$	Gate voltage of the first Coulomb oscillation
V_{P}	Pinch-off voltage
V_{th}	Threshold voltage
ω	Angular frequency
ω_0	Resonance frequency
ω_{B}	Bragg frequency
ω_{Larmor}	Larmor frequency
ω_{Rabi}	Rabi frequency
W_{g}	Gate width
Y	Admittance
Z	Impedance
Z_0	Characteristic impedance
Z_{opt}	Optimal noise impedance

1 Introduction

1.1 Quantum computing and quantum bits

Quantum computers are an emerging solution to address the ever-growing quest for computational power in modern classical (super)computers and, in particular, to solve today's intractable problems, such as the simulation of complex molecules, the design of new materials with specific properties, and the prime factorization of large numbers [1, 2].
Among classical computers, digital and analog architectures exist: digital architectures store, process and transmit information by means of bits. A classical bit is the fundamental unit of information in classical computers, and it can have a value which is either 0 or 1. Information is stored inside memory cells, and a memory register with N cells can have 2^N possible states. However, despite having 2^N possible states, at any point in time the N-bit memory register can only assume one instantaneous state determined by one of the possible N-bit strings. In a classical computer, information is moved from the memory to the Central Processing Unit (CPU), to perform operations and computations on the input bits. The processing unit provides one and only one predefined output N-bit string for each input N-bit string, according to a hardware-defined mapping [3].
The quantum counterpart of classical bits are quantum bits (qubits). A qubit is any quantum mechanical two-level system, where information can be encoded in the base states, represented by $|0\rangle$ and $|1\rangle$, according to Dirac's notation. Quantum mechanics allows each qubit to be in a *superposition* of the two base states expressed by the wavefunction:

$$|\psi\rangle = \alpha_\mathrm{p} |0\rangle + \beta_\mathrm{p} |1\rangle , \tag{1.1}$$

with α_p and β_p being the probability amplitudes corresponding to each of the two base state vectors. The graphical representation of this state is shown in Figure 1.1, in the so-called Bloch sphere.
Similarly to classical computers, a quantum register made by N qubits has 2^N possible states. However, since each qubit state can be a superposition of the two base states, then at any point in time the quantum register can be in a superposition of its 2^N base states with certain probability amplitudes or, in classical fashion, bit strings, and quantum operations

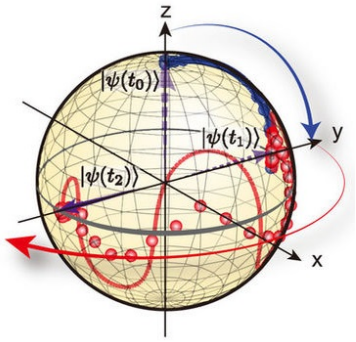

Figure 1.1 – Graphical representation of the wavefunction in the Bloch sphere [4].

will act by creating an input-output mapping between all such 2^N computational states simultaneously [3]. This determines a very important property: the computational power of quantum computers grows exponentially with the number of qubits, since operations can be executed on all the states in parallel.
However, the full set of quantum states can be accessed only if the qubits are allowed to interact with each other; if N qubits are isolated, there are still only $2N$ degrees of freedom available. In particular, some multi-qubit states can be realized by isolated single-qubit quantum states, which means that mathematically the wavefunction $|\psi\rangle$ can be factored in separate functions only involving one qubit at once. However, some states, such as the Bell state $|\psi\rangle = (|00\rangle + |11\rangle)/\sqrt{2}$, cannot be factored into independent single-qubit states, and therefore require interactions between qubits. Such states represent *entanglement* and this phenomenon has no classical counterpart. The state of one qubit in an entangled state is linked to the state of the other, even if the qubits are far away and have no apparent way to interact.
A quantum computer operates by processing the information stored in qubits. Differently from classical computers, qubits act both as the quantum register storing the information and as processing units when quantum operations are performed on them directly.
According to quantum mechanics, a quantum state, which is expressed as a superposition of bases states, cannot be measured in superposition: during the *measurement* phase, such state collapses into one of the two bases states, with a probability given by the relative amplitude coefficient in the superposition. Therefore, the act of measurement is a projective action that maps the quantum superposition state into one base state, in probabilistic fashion.
The quantum state in Equation (1.1) can be expressed as:

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{j\phi}\sin\left(\frac{\theta}{2}\right)|1\rangle\,. \tag{1.2}$$

This indicates that the state of the qubit could be coherent if there were no interactions with its surrounding environment. However, every source of microscopic noise affects the quantum state and induces *decoherence* and dephasing. This means that quantum operations need to be performed on the quantum state before it decoheres in a computationally

unusable state, and measurements need to be fast enough as well, while the qubit state needs to be refreshed in its correct state frequently.
For this reason, typically a logical qubit is realized by multiple physical qubits, that act as ancilla qubits, to allow for correction of errors occurring on individual data qubits. This is required by Quantum Error Correction (QEC) algorithms to allow fault-tolerant quantum computing [5]. Hence, a practical quantum computer will need to handle thousands if not millions of qubits.
In particular, well established criteria exist to determine the necessary conditions to build a quantum computer, the DiVincenzo criteria [6]. These criteria establish that to achieve quantum computation one needs a scalable physical system with well characterized qubit, the ability to initialize the state of the qubits to a simple fiducial state, long qubit decoherence times, a "universal" set of quantum operations or gates, and a qubit-specific measurement capability.
In order to realize quantum computers according to these criteria, several ways exist to implement qubits, among which there are spin qubits, superconducting qubits, single photons in waveguide systems, trapped ions and Nitrogen Vacancy (NV)-centers in diamond [7]. In the following, the focus will be on solid-state qubit implementations, in particular spin and superconducting qubits.

1.2 Spin qubits

In spin qubits, quantum information is stored in the spin of electrons. Different physical implementations are possible for spin qubits [4, 8, 9], such as Quantum Dots (QDs), which are nanostructures capable of confining electrons to allow individual control of their spin. Quantum dots were originally proposed for quantum computation in [10], and have been studied since, in order to achieve this goal.
Usually quantum dots are obtained in semiconductor heterostructures [8], which are capable of confining electrons in a 2-Dimensional Electron Gas (2DEG) due to their band structure, as shown in Figure 1.2, or in transistor-like structures [11], for example in Complementary Metal Oxide Semiconductor (CMOS) technology, trapping electrons in their channel with high electrostatic gate control, as shown in Figure 1.3. In semiconductor heterostructures, thanks to electrode gates, local electrostatic fields can be applied to change the electrochemical potential and create depletion regions and residual electron islands. When the charge islands reach a size comparable with the Fermi wavelength $\lambda_F = 2\pi/k_F = \sqrt{2\pi/\rho}$, where k_F is the Fermi wave-vector and ρ is the carrier density, electrons can be confined in the two remaining directions, thus yielding 0D quantum dots, as shown in Figure 1.2. The island is connected to quasi-metallic charge reservoirs on each side, from which electrons can shuttle on and off.
As a result of the confinement, energy levels in the quantum dot become quantized. The electrostatic confining potential that defines the quantum dot supports indeed several spin-degenerate energy levels. The allowed energy states can be defined from the constant interaction model [8], if a constant capacitance term C is defined for the interaction between electrons in the quantum dot and the surrounding electrostatic environment. If N electrons are confined in the quantum dot in its few-electron regime, the energy of the quantum dot can be expressed as:

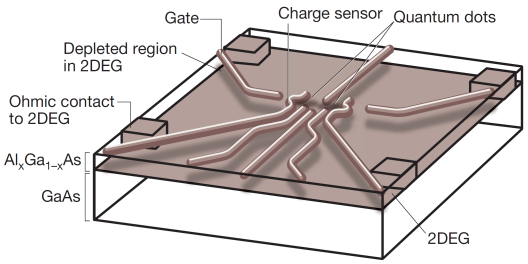

Figure 1.2 – Realization of a quantum dot by means of a 2D electron gas [7].

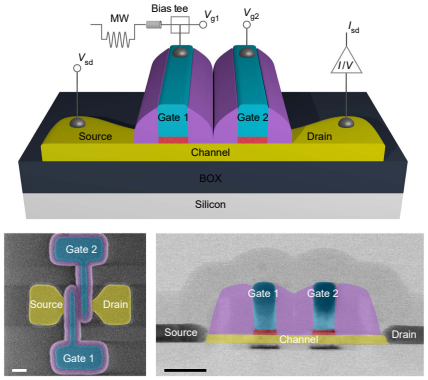

Figure 1.3 – A CMOS compatible qubit [11].

$$U(N) = \frac{(-|e|(N - N_0) + \sum_i C_i V_i)^2}{2C} + \sum_j^N E_j, \tag{1.3}$$

where e is the electron charge, N_0 is the number of electrons in the ground state, C_i and V_i are the capacitance and voltage contributions of the surrounding structures, such as source, drain leads and gate electrodes, and E_j is each single-particle energy level up to N. The electrochemical potential μ of the island is defined as:

$$\mu = U(N) - U(N - 1). \tag{1.4}$$

The energy required to add an extra electron on the island can be expressed as:

$$E_{\text{add}} = \mu(N + 1) - \mu(N) = E_{\text{c}} + \Delta E, \tag{1.5}$$

where $E_{\text{c}} = e^2/C$ is the so-called charging energy and ΔE defines the level spacing.
If the quantum dot is small, the self-capacitance C is small, and so the energy required to add an electron becomes large. If one considers the island and its environment as the plates of a capacitor, the capacitance C also sets the time required to charge the island with an extra electron. The time constant of this process is $\tau = R_{\text{t}}C$, where R_{t} is the tunneling resistance. Heisenberg uncertainty principle must hold for this process, therefore the relationship $\Delta E\ \Delta t = E_{\text{c}}\tau > h$ must apply, where h is Planck's constant. This determines that:

$$R_{\text{t}} > \frac{h}{2e^2}, \tag{1.6}$$

where the factor 2 arises from the degeneracy of spin up and spin down states. The limit found corresponds to the quantum of conductance:

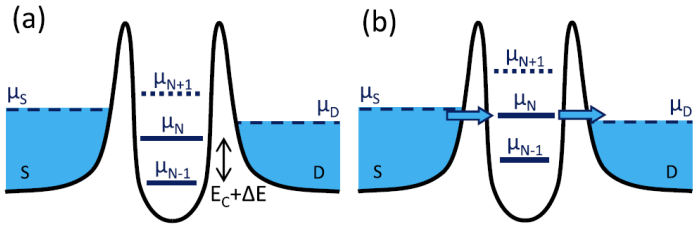

Figure 1.4 – Electrochemical potential levels in a quantum dot (a) when transport is prohibited and (b) when transport is allowed [9].

$$G_0 = \frac{2e^2}{h}, \tag{1.7}$$

and also sets the condition to observe single electron tunneling events through the energy levels of the quantum dot.
Moreover, another requirement is that thermal energy levels of the electrons are sufficiently low not to excite the electrons on or off the dot, namely:

$$k_B T < \frac{e^2}{C}, \tag{1.8}$$

where k_B is the Boltzmann constant and T is the absolute temperature. Therefore, to prevent thermal energy from controlling the system, operation at very low temperature is required. Recently, however, operation of silicon qubits up to 1 K has been demonstrated [12, 13].
When the electrochemical potential of the quantum dot lies within the electrochemical potentials of the source and drain reservoirs, namely $\mu_S < \mu(N) < \mu_D$, a flow of current proportional to the electrochemical potential difference can be observed across the dot, as shown in Figure 1.4. This difference determines the bias window allowing current flow for the energy states in the quantum dot and can be controlled by the source-drain voltage V_{SD}, since $\mu_S - \mu_D = -|e|V_{SD}$. Transport manifests itself as peaks in the conductance of the quantum dot, as shown in Figure 1.5 (a).
Source-drain voltage can be used to control transport across the dot, but also the potential on the island itself can be used to tune transport by means of a gate. Charge tunneling events across the potential barriers can be induced in this scenario, until the energy needed to fill the dot with one extra electron is greater than the chemical potential at the leads. In this case, the energy level of the dot lies outside the bias window, and tunneling is prevented. In this situation, Coulomb blockade manifests itself and current transport is prohibited. This is visible in the charge stability diagram of a quantum dot as Coulomb diamonds, as shown in Figure 1.5 (b).
If the quantum dot is very small, according to Pauli's exclusion principle, up to two electrons with opposite spin can occupy the lowest energy level in the quantum dot. Therefore, in order to create a true two-level system, capable of representing a qubit, a Direct Current

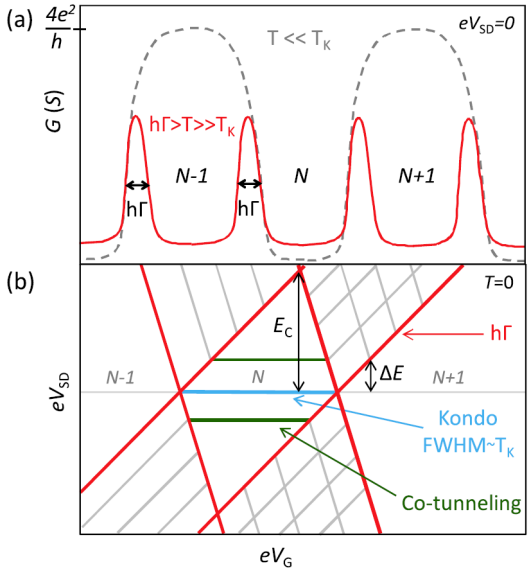

Figure 1.5 – (a) Conductance peaks and (b) Coulomb diamonds in a charge stability diagram for a quantum dot [9].

(DC) magnetic field B_{DC} is applied, to split the energy of electrons in the ground state. Due to the Zeeman effect, an energy $E_{\mathrm{Z}} = \pm\mu_{\mathrm{B}} g_{\mathrm{L}} B_{\mathrm{DC}}$ is added, where μ_{B} is the Bohr magneton, and g_{L} is the Landé g-factor, so that in the system two distinct energy states exist: they can be attributed to the $|0\rangle$ and $|1\rangle$ states.
In order to control the spin of the electron in the quantum dot, microwave signals with accurate amplitude and phase have to be applied [14]. When the electron is located in a static magnetic field B_{DC} in the z direction, it performs a precession around the magnetic field axis at the Larmor frequency $\omega_{\mathrm{Larmor}} = \gamma_{\mathrm{R}} B_{\mathrm{DC}}$, where γ_{R} is the gyromagnetic ratio, due to the interaction of its magnetic dipole with the applied field. However, when a perpendicular Alternating Current (AC) magnetic field, $B(t) = B_{\mathrm{AC}} \cos(\omega_{\mathrm{mw}} t)$, rotating at frequency $\omega_{\mathrm{mw}} = \omega_{\mathrm{Larmor}}$ is applied, it is possible to cancel the effect of the static magnetic field, such that the spin will perform a precession around the rotating magnetic field, at the Rabi frequency $\omega_{\mathrm{Rabi}} = \gamma_{\mathrm{R}} B_{\mathrm{AC}}$. In this way, also x and y rotations in the Bloch sphere are possible, as shown in Figure 1.1.
For qubit state readout, DC techniques are often applied. They are based on direct readout and amplification of the transport current through the quantum dot by means of a Trans-Impedance Amplifier (TIA). This method is simple, but it suffers from $1/f$ noise and the large capacitance of such system typically limits the bandwidth of these measurements, thus making this readout method not very fast.
Alternatively, Radio Frequency (RF) probing techniques have been proposed for semiconductor qubit readout. Two main techniques have been developed: the first one is *radio-frequency reflectometry* [15], the second one is *Dispersive Gate Sensing (DGS)* [16].
In a generic radio-frequency reflectometry, a narrow channel, called Quantum Point Contact (QPC) [15], or a Single-Electron Transistor (SET) [17], as shown in Figure 1.6 (a), is used as an intermediate electrometer to sense the state of the qubit and convert it into an electrical quantity, which is then read out. Typically, spin-to-charge conversion is applied in

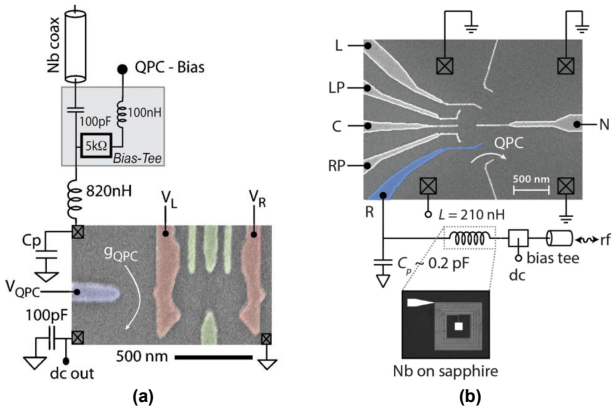

Figure 1.6 – Two techniques for readout of semiconductor quantum dots: (a) RF reflectometry [15], (b) dispersive gate sensing [16].

the case of a QPC. The QPC, due to its small size, has a quantized conductance and exhibits a very steep staircase voltage-to-conductance transfer function. By properly setting the electrical control voltages, the electron is allowed to tunnel out of the quantum dot only in one spin configuration (↑ or ↓) and this results in a spin-dependent charge variation. The potential of the quantum dot is then capacitively coupled to the charge sensor, therefore the voltage variation is sensed and translated into a change in the resistance of the QPC. The high impedance of the QPC is converted to 50 Ω by an impedance matching network, which is tuned to have optimal match at the readout frequency. A radio-frequency carrier is used to probe the QPC, but variations in the resistance of the QPC will lead to a change in the portion of carrier power reflected by it. Therefore, a change in the amplitude of the reflected signal carries information about the state of the quantum device. For this reason, such a readout technique is called radio-frequency reflectometry.
In order to eliminate the need for an external electrometer, direct in-situ connection to the gate of the quantum device, as shown in Figure 1.6 (b), has been proposed [16, 18]. In such a technique, the semiconductor quantum device is addressed at its gate, through an impedance matching network converting the high gate impedance to 50 Ω, with an RF carrier signal and the phase of the reflected signal is read out. According to the state of the quantum device, the capacitance at the gate will be different, due to the presence in the $|1\rangle$ state of an additional quantum capacitance C_q. This contributes to a phase shift $\Delta\varphi$ in the response of the resonant matching network, which carries the quantum information about the state of the quantum device. For this reason, such a technique is called dispersive gate-based sensing.

1.3 Superconducting qubits

Superconducting qubits are monolithically fabricated devices that are based on superconducting materials and structures. Several types of superconducting qubits exist, but the transmon type is recognized as the most established structure. The transmon qubit is a non-linear microwave resonator [19].
If one considers a harmonic LC oscillator, its resonance frequency is defined as $\omega_0 = 1/\sqrt{LC}$,

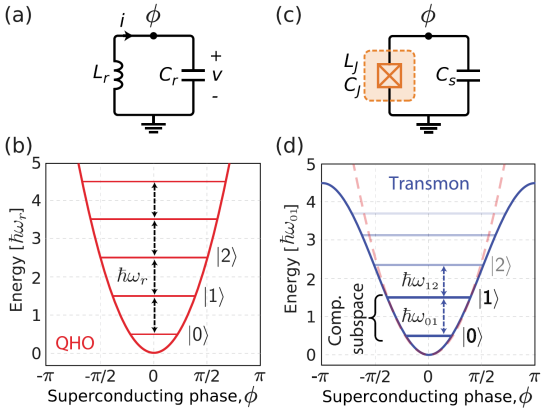

Figure 1.7 – (a) Harmonic LC oscillator and (b) its energy levels. (c) Anharmonic LC oscillator and (d) its respective energy levels [19].

and its quality factor is $Q = R\sqrt{C/L}$, where R is the resistance in parallel. In the quantum mechanical limit, the energy levels of such harmonic oscillator are quantized according to:

$$E_{n,LC} = \hbar\omega_0 \left(n + \frac{1}{2}\right), \tag{1.9}$$

where $\hbar$ is the reduced Planck constant and n is a non-negative integer index. This means that the ground state of a harmonic mechanical oscillator has non-zero energy, and the subsequent energy levels are equally spaced, with an energy step corresponding to $\hbar\omega_0$, as shown in Figure 1.7 (a), (b). The energy separation between two consecutive energy levels corresponds to adding or removing one microwave quantum of energy at the oscillator resonant frequency. The two lowest energy levels could be used to identify the base states of a qubit, namely $|0\rangle$ and $|1\rangle$.
This is however only possible if these discrete energy levels are not excited by thermal energy fluctuations in the system. The energy scale of thermal fluctuations is $k_B T$, while the energy scale of the electromagnetic quantum is $\hbar\omega$, therefore the temperature must be sufficiently low to guarantee the observability of these discrete energy levels. Considering $T < \hbar\omega/k_B = 50\,\mathrm{mK/GHz} \cdot f$, one can conclude that a temperature of about 10 mK is required to observe quantum mechanical behavior for frequencies f above 1 GHz.
Beyond thermal considerations, one should be able to address only the two lowest energy levels to have a pure two-level quantum mechanical system, but a linear energy level spacing does not allow that. Some anharmonicity needs to be added to the system, in such a way that the energy levels become non-uniform and one can address the two lowest energy levels independently. In a transmon qubit this is done by replacing the inductor L with a non-linear inductance created by a Josephson junction, which is a superconducting tunnel junction that exhibits a non-linear inductance:

$$L_J = L_{J0}/\sqrt{1 - I_J^2/I_c^2}, \tag{1.10}$$

where I_J is the current through the Josephson junction, I_c is the critical current of the Josephson junction, $L_{J0} = \Phi_0/2\pi I_c$ is the zero-flux inductance of the Josephson junction, $\Phi_0 = \pi\hbar/e$ is the magnetic flux quantum and e is the elemental electron charge.
If one defines Josephson and capacitive energies $E_J = \Phi_0 I_c/(2\pi)$ and $E_c = e^2/2C$, one can then write the energy levels of the transmon qubit as:

$$E_n \simeq \hbar\omega_0 \left(n + \frac{1}{2}\right) - \frac{E_c}{12}(6n^2 + 6n + 3), \tag{1.11}$$

where $\omega_0 = 1/\sqrt{L_{J0}C}$, under the assumption that $E_J \gg E_c$. In this situation one can see that the energy spacing between subsequent energy levels is different and the transition frequencies as well, so the system can effectively be treated as a two-level quantum mechanical system, as shown in Figure 1.7 (c), (d).
The transmon structure can be further enhanced by replacing the Josephson junction structure with a superconducting loop interrupted by two Josephson junctions, namely a DC Superconducting QUantum Interference Device (SQUID), that behaves similarly to a single Josephson junction, where however L_{J0} depends on the magnetic flux bias through the superconducting loop.
In order to control a transmon qubit, rotations around the z axis are enabled by controlling the qubit frequency through a flux tuning line, while rotations around the x and y axes are obtained by capacitively coupling a microwave signal drive to the qubit [3]. The phase of the carrier determines the angle of the axis in the xy-plane around which the qubit state rotates, while the integrated envelope amplitude determines the amount of the rotation. During control, one should pay attention not to excite the higher energy levels of the qubit, therefore such microwave control signals are typically generated as microwave pulses, employing spectral-shaping techniques to reduce spectral content at higher qubit transition frequencies.
Concerning the transmon qubit readout, this consists in the projective measurement of the quantum superposition state of the qubit into one of the two base states with a certain probability [20]. This is typically performed by measuring the variable admittance of the qubit, which depends on the qubit state, through a linear resonator capacitively coupled to the qubit and slightly detuned with respect to the qubit frequency. The qubit pulls the readout resonator frequency, and it does so by a different amount, called dispersive shift, in the two qubit states. Therefore, the phase of the readout signal (in reflection or transmission) carries the information about the qubit state and it can be read out by using demodulation techniques typical of modern communication systems.
To this date, transmons are the first qubits to have enabled the demonstration of quantum supremacy, with a superconducting quantum processor [21].

1.4 Cryogenic electronics for quantum computers

Solid-state quantum bits, such as spin qubits and superconducting qubits presented previously, are among the most promising implementations to build large-scale quantum computers. However, these qubits must operate at deep-cryogenic temperatures to work

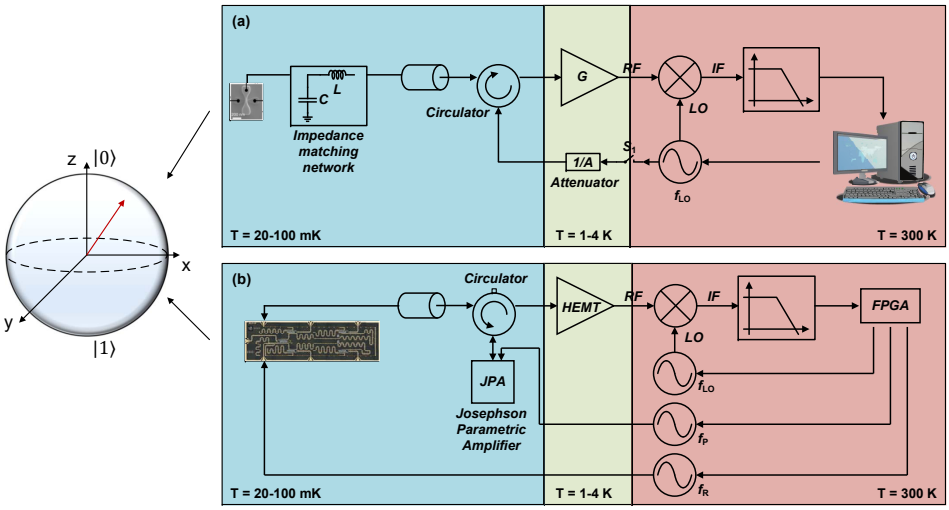

Figure 1.8 – Current implementations of typical qubit readout schemes for (a) spin qubit processors [18] and (b) superconducting qubit processors [20]. The color coding represents temperature variation along the chain, from the base temperature of dilution refrigerators (20-100 mK) in blue, to room temperature (300 K) in red.

in the quantum regime. Therefore, they are kept in dilution fridges, while the electronic setup required for their readout and control is typically realized by discrete commercial components, wired to the qubits through thermalized coaxial cables, and by room temperature scientific instruments.

Typical readout systems for spin and superconducting qubits show close similarities with RF wireless receivers, as shown in Figure 1.8. Qubits are coupled to a resonator, tuned at the readout frequency, and are probed by a readout signal. The signal reflected (or transmitted) by the qubits goes through a directional coupler or circulator, which decouples it from the probing signal, then it goes through one or multiple cryogenic Low-Noise Amplifier (LNA) stages that amplify the weak qubit response. Then, the signal is downconverted by a mixer, typically in a homodyne scheme using as Local Oscillator (LO) the same Voltage-Controlled Oscillator (VCO) used for probing, or in low-Intermediate Frequency (IF) scheme. The signal is then low-pass filtered to remove higher frequency components and digitized by an Analog-to-Digital Converter (ADC) to be processed at room temperature. Current systems employ several discrete components, such as directional couplers, circulators and amplifiers operating at cryogenic temperatures, together with commercial instruments, such as Vector Signal Analyzers (VSAs), operating at 300 K.

Control systems for qubits, on the other hand, remind of RF wireless transmitters and employ benchtop instruments, such as Vector Signal Generators (VSGs) and Arbitrary Waveform Generators (AWGs) at room temperature to generate (pulsed) control radio-frequency waveforms.

This approach is feasible as long as few (< 100) qubits are used, but it is not scalable to large-scale quantum computers that would require thousands if not millions of qubits for error-corrected logical qubit implementations in QEC schemes.

The main limiting factors to scalability in current systems are, at the topological level, the need for an individual control and readout chain for each qubit, and at the circuit level,

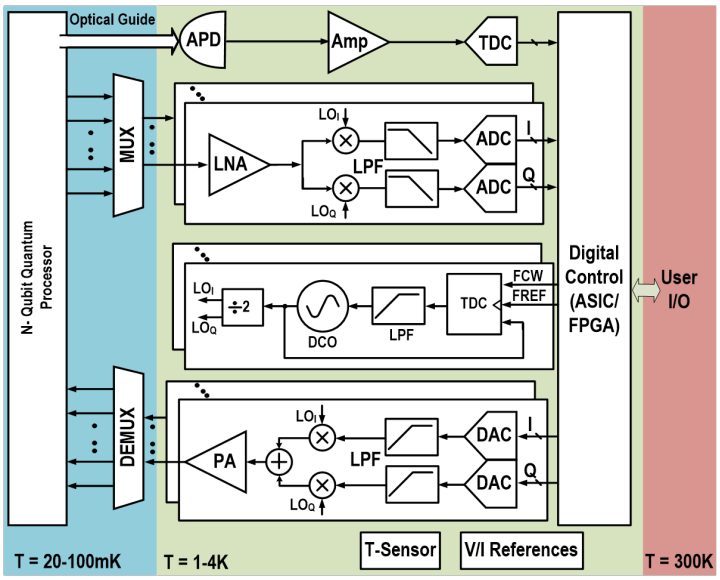

Figure 1.9 – Vision for a fully-integrated cryogenic CMOS RF transceiver, showing the readout and control system architecture for multi-qubit processors [24].

the presence of a discrete matching network and a directional coupler, which are bulky and difficult to integrate.
In order to address the topological drawback, different multiplexing schemes can be applied to reduce the number of connections to and from high temperature instruments. In particular, physical routing of different qubits to the control/readout chain can be performed by means of Time-Division Multiple Access (TDMA) schemes [22], employing multiplexers as controlled switches. For this purpose, accurate and fast RF multiplexers need to be designed to operate at very low temperature. In this case, the bandwidth of the required interconnect is just as large as the maximum frequency of signals that need to be transmitted. Otherwise, also Frequency-Division Multiple Access (FDMA) of different qubits has been proposed as a solution [23]: by means of this, each qubit has its own *LC* matching network tuned at a specific frequency, and the rest of the readout and control chain can be shared. In this case, a high bandwidth interconnect is required and finally the number of used frequencies can be a limiting factor in such an architecture. In any case, both schemes allow to greatly reduce the area and power requirements and largely improve scalability.
For what concerns the scalability of the chain at circuit level, the main improvement can be granted by substituting all the discrete commercial components and instruments in the system by custom integrated circuits eventually reducing to a single chip, capable of granting the same functionality in the area of a small die.
Furthermore, scalability could greatly benefit from the possibility to integrate both qubits and readout/control circuits on the same platform and eventually on the same chip, at low temperature.
For this reason, the need for compact and scalable classical control circuits in physical proximity with the qubits has emerged. Therefore, CMOS integrated circuits operating directly at cryogenic temperatures (cryo-CMOS) have been proposed [22, 24, 25] to read

out and control large numbers of qubits, thus paving the way to future co-integration of qubits and classical control.
The proposed vision to replace current discrete systems consists in moving all the electronics at cryogenic temperature, and implementing it as a fully-integrated cryogenic RF transceiver for qubit readout and control with compact form factor [24], shown in Figure 1.9. Such system, across different temperature boundaries, can connect to the deep-cryogenic temperature qubit processor on one side, thanks to interface multiplexers, and to the user interface at room temperature on the other side.
Moreover, the future vision also includes full integration of the qubits and classical electronics in a single chip, possibly exploiting 3D integration techniques.

1.5 Cryogenic CMOS electronics and its alternatives

In order to realize the proposed fully-integrated electronic readout and control for quantum computers, several technologies have been considered in literature. Semiconductor technologies, in particular silicon, have been dominant in the realization of large-scale integrated circuits and therefore have been considered with primary interest.
CMOS technology has attracted the most attention since very-large scale manufacturing infrastructures exist already and this allows larger scalability, easier integration and much smaller cost. CMOS technology is very mature and has been constantly progressing to push the performance and keep up with the demands of commercial products, therefore a large wealth of design and fabrication expertise is already existing. CMOS technology was proposed for compactness reasons, and for the opportunity of co-integration with silicon qubits, operating directly at low temperature. Operation of integrated CMOS transistors has been shown down to 100 mK [26] and this allows to build integrated circuits for readout and control without major paradigm shifts with respect to existing room temperature integrated circuits. Apart from the mentioned advantages, CMOS technology has some drawbacks, since it does not offer state-of-the-art performance for analog and RF circuit functionality, such as the lowest noise and highest speed among all alternatives. It has however proven to be a good trade-off between performance and flexibility.
Historically, CMOS technology was already explored in terms of its cryogenic operation before the advent of quantum computing. LNAs have been proposed for sensing and astronomy applications [27], and ADCs [28] have been developed for other scenarios where cryogenic operation is an integral part of the system, such as high-energy physics experiments. Despite having been already explored, no systematic approach has been taken in literature to investigate the properties of silicon transistors at cryogenic temperatures down to 4.2 K and to establish CMOS circuit designs and architectures specific to cryogenic operation.
From the earlier exploration of silicon transistors at cryogenic temperatures, some insights about the electronic properties of semiconductors and Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) at cryogenic temperatures were already available and could guide the initial developments [29]. When silicon transistors are cooled down to cryogenic temperature, dopants in the MOSFET body and silicon substrate, which is non-degenerately doped, undergo *freeze-out* or thermal de-ionization [30]. Moreover, there is an *increase in threshold voltage* V_{th} of transistors for decreasing temperature, and this can

be explained by a wider semiconductor bandgap at lower temperatures, and by a more important effect of the Fermi-Dirac statistics at cryogenic temperatures, due to its more step-like shape [31]. Moreover, the role of *interface charge traps* becomes more prominent, since the number of interface traps active at lower temperature can be significantly higher than at room temperature. Low temperature causes a *Subthreshold Swing (SS) decrease*, but with a degradation with respect to the theoretical limit. Moreover, one observes an *increase in mobility* μ_0 at cryogenic temperature, due to the reduced scattering phenomena caused by the lower thermal energy of lattice vibrations.
Alternatively, other semiconductor technologies could be used to address the needs of qubit control and readout, such as **GaAs**, **SiGe** or other semiconductor heterostructures. The advantages of these technologies are the better performance of integrated transistors, especially for analog and RF functionality, thanks to the tailored band structure of the semiconductor heterojunction [32]. This allows typically higher carrier mobility, smaller noise factors, and higher maximum operating frequency of single devices. Moreover, also qubit platforms have been explored in SiGe and GaAs technologies [8], therefore this represents a further advantage. Historically, SiGe Heterojunction Bipolar Transistors (HBTs) resulted in low noise amplifiers and receivers for astronomy applications with excellent performance in terms of noise [33]. However, such technologies have not scaled down as fast as CMOS, and the available technology nodes are not very advanced, therefore the availability of very large scale integration, capable of hosting millions of qubits and transistors, is reduced. Finally, also the cost of such technologies is much higher than standard CMOS, thus limiting the rise as a fast prototyping technology platform for quantum-classical integrated circuits.
Other possible alternatives are represented by **superconducting electronics**, such as **Rapid Single-Flux Quantum (RSFQ) technology**, which is based on Josephson junctions, and offers extremely high-speed electronics supporting THz clock frequencies [34]. This approach would be a more natural fit for the readout and control of superconducting qubits, which are intrinsically based on the same fundamental element, the Josephson superconducting tunnel junction, thus establishing a superconductive platform. However, the size of these circuits is still too large [35] to envision very large scale integration of high-complexity qubit controllers for scalable readout and control.
Consequently, the most attractive solution, in order to lay the foundations of cryogenic integrated circuit design for qubit readout and control was and still is cryogenic CMOS technology, for its compactness, scalability, reliability, low cost, established fabrication infrastructure and for its potential co-integration with silicon qubits at low temperature.

1.6 Research motivation and goals

In order to implement the classical readout and control infrastructure needed to prepare, manipulate and measure the state of qubits, *CMOS technology* and direct *cryogenic operation* are chosen in this thesis for the reasons explained previously, thus targeting cryogenic CMOS circuits and systems.
Moreover, deep-submicron CMOS technologies are proposed to design circuits operating at deep-cryogenic temperatures, in order to meet the strict requirements in terms of scalability and performance of fault-tolerant quantum computers.

Although cryogenic CMOS circuits have already been proposed and were occasionally used in other fields of research, the goal of this thesis is to advocate a **systematic methodology to the study, design and implementation of CMOS circuits and systems specifically at low temperature** and targeting classical readout and control of quantum processors. This consists in the creation of a **comprehensive class of cryogenic analog and RF circuits and systems**, resulting from the use of advanced technological processes and the application of specific constraint-based design strategies targeting low power, low noise and wideband operation.
Such an approach is meant to be applied to a broad range of circuits spanning the spectrum of analog and RF designs, including not only consolidated CMOS circuits, but also new and less known circuit blocks and topologies, in an exploratory fashion.
The chosen cryo-CMOS framework is effective for the proposed goals, as cryogenic operation is favorable for low noise and high speed, as well as for digital-based circuits, therefore the envisioned RF readout and control architecture fits well the context.
Finally, the creation of an integrated platform where qubits and low temperature circuits co-exist is advocated, since it would be a major breakthrough for the creation of a scalable quantum computer.
Such scientific contributions could have an impact not only on the circuit design community, but also on the device modeling and Computer-Aided Design (CAD) communities and could provide a new experimental framework for physicists working in the qubit and quantum computing area.
The broad research goal of the thesis is to explore cryogenic CMOS technology and to lay its foundations, starting from a basic understanding of the operation of cryogenic CMOS quantum devices (such as quantum dots), active devices (MOSFETs) and passives (resistors, capacitors, inductors, transformers), to then develop custom low-temperature integrated circuit designs for each block required in the readout and control of solid-state quantum processors, with the final objective of integrating them in one (or few, based on temperature boundaries) integrated circuits capable of replacing current discrete electronics.
Within this broader research objective, the focus of the thesis is on cryogenic CMOS circuits for readout of silicon quantum bits, with the goal to achieve an integrated circuit realization of the readout, from the quantum layer to the room temperature interface electronics.

1.7 Thesis contributions

Within the goals set and the outline presented previously, this thesis explores two worlds, the **quantum world**, briefly, with the realization of quantum dots in CMOS, and the **classical world**, with the analysis and characterization of active and passive devices and in particular the design of analog and RF front end circuits.
The contributions of this thesis span across different levels of abstraction. At **device level**, this thesis describes the realization of the first quantum dots in a standard bulk CMOS technology, a basic characterization and modeling of integrated active devices, such as MOSFETs, in bulk CMOS technology at low temperatures, accompanied by the first in-depth characterization and modeling of integrated CMOS passive devices, such as

capacitors, inductors and transformers at cryogenic temperatures.
These elements are later combined in the **circuit design** part, whose contributions embrace *new block design*, with the realization of the first fully-integrated time-and frequency multiplexed readout matrix for silicon quantum dots, fundamental *circuit innovation at block level*, with the proposed first fully-integrated cryogenic CMOS circulator based on a new all-pass filter architecture, *system-level design innovation*, with the realization of the first fully-integrated cryogenic CMOS receiver for the readout of spin qubits, and finally also *experimental-level contributions*, with the demonstration of the first fully-integrated readout of silicon quantum dots at 6-8 GHz.
The most important original contributions of this thesis are:

- the first realization of silicon quantum dots in a standard bulk CMOS technology, to allow scalable and reproducible arrays of quantum devices (Chapter 2);
- the realization of the first quantum-classical integrated circuit in bulk CMOS technology, co-integrating quantum dots and simple active and passive circuits operating at 50 mK, with the proposal of a new interface matrix based on a scalable random-access readout architecture, capable of demonstrating, for the first time, fully-integrated gate-based dispersive readout with integrated resonators at 6-8 GHz and time- and frequency-multiplexed readout (Chapter 5);
- the realization of the first fully-integrated cryogenic CMOS circulator and the proposal of a new circulator architecture based on all-pass filters, capable of reducing power consumption, enhancing bandwidth and reducing insertion loss (Chapter 7);
- the realization of the first fully-integrated cryogenic CMOS receiver for spin-qubit readout, exploring a new frequency range (5-6.5 GHz) for improved sensitivity and integration (Chapter 9).

1.8 Thesis organization

This thesis is organized as follows.
An initial introduction in Chapter 1 sets the background of this research, by discussing the basics of quantum computers and qubits, with a focus on solid-state implementations, in particular spin qubits and superconducting qubits, followed by the proposal of integrated electronics for qubit readout and control and a brief summary of the behavior of CMOS electronics at cryogenic temperatures and its alternatives.
The core of the thesis is then divided in two parts: the first part discusses *cryogenic CMOS devices* in terms of characterization and modeling, while the second part deals with custom *cryogenic CMOS integrated circuits* designed by combining the presented devices, and focusing on the readout of spin qubits.
In the first part, Chapter 2 describes the realization of quantum dots in standard bulk CMOS technology by using minimum size transistors. The devices are characterized, the quantum dot properties are modeled, and some insights on variability are provided.
In Chapter 3, a basic characterization and modeling of MOSFETs in deep submicron processes in bulk CMOS technology is presented first at deep-cryogenic temperatures

(50 mK), and then at cryogenic temperatures (4.2 K). Some quantitative estimates on the variations of the most important analog/RF parameters are derived, to provide a first rough understanding for the design of integrated circuits.
In Chapter 4, integrated passive devices in bulk CMOS technology (capacitors, inductors, transformers) are characterized and modeled at 4.2 K, moreover lumped-element and electro-magnetic models are developed to allow predictive circuit design at cryogenic temperatures.
The characterization and models of cryo-CMOS devices presented in the first part are not the main focus of the thesis, but they are instrumental to be used in the second part to design custom integrated circuits for the readout of spin qubits, with increasing complexity, moving from the quantum layer to the room-temperature electronic interface.
In the second part, Chapter 5 presents a fully-integrated readout matrix comprising quantum dots in standard CMOS and a time- and frequency-multiplexed readout random-access architecture for fully-integrated gate-based readout at 6-8 GHz.
Chapter 6 describes the realization of some simple individual low-frequency analog and digital multiplexers that contributed to the design of the fully-integrated matrix in Chapter 5.
Chapter 7 presents a cryo-CMOS fully-integrated circulator with a new architecture based on all-pass filters, that allows to enhance bandwidth, reduce power and insertion loss. It contains a detailed description of the specifications, the fundamental theory behind the proposed architecture, complete measurements, and discussion.
Chapter 8 describes the specifications of the front-end circuits for gate-based dispersive spin qubit readout and then presents a cryo-CMOS low-noise amplifier and a cryo-CMOS voltage-controlled oscillator, which are later combined in a single chip in Chapter 9.
Finally, Chapter 9 presents a fully-integrated receiver for spin qubit readout, containing low-noise amplifier, downconversion mixer, wideband intermediate frequency amplification chain, and a phase-locked loop for frequency generation. It contains a detailed description of the circuit architecture and measurements. This work completes the readout chain, going from the quantum dots (quantum layer), through to the circulator and finally to the receiver (room temperature interface) and closes the work presented in this thesis.
Lastly, Chapter 10 concludes this thesis, summarizing the achievements, discussing the obtained results, across success and failure, and laying the foundations for future improvements of this work into an ever-perfectible perspective.

Cryogenic CMOS devices Part I

2 Quantum devices in standard CMOS

The work presented in this chapter has been published in the paper:

[36] T.-Y. Yang, **A. Ruffino**, J. Michniewicz, Y. Peng, E. Charbon and M. F. Gonzalez-Zalba, "Quantum Transport in 40-nm MOSFETs at Deep-Cryogenic Temperatures," *IEEE Electron Device Letters (EDL)*, vol. 41, no. 7, pp. 981-984, July 2020.

In this work, I designed the test chip, measurements were performed by Tsung-Yeh Yang and John Michniewicz, collaborators at Hitachi Cambridge Laboratory, and then I participated in the data analysis and manuscript writing.

2.1 Introduction

The fundamental element in a silicon-based quantum-classical platform for Quantum Information Processing (QIP) is the realization of reproducible quantum dots that can be used to implement qubits [8, 9].
As explained, from a physics perspective, single-electron spins confined in gate-defined quantum dots can be used to realize qubits [37, 38, 39], which can be operated close to fault-tolerance fidelity levels [40, 41], and elevated temperatures [12, 13]. From a technological perspective, QDs can be manufactured in a similar fashion to Field-Effect Transistors (FETs) [11, 42] with a small footprint ($30\times30\,\mathrm{nm}^2$). This gives the opportunity to leverage Very Large-Scale Integration (VLSI) techniques to scale up the technology beyond state-of-the-art 2-qubit processors [41, 43, 44, 45] to two-dimensional QD arrays [46, 47], a requirement for fault-tolerant quantum computing [5].
However, so far, silicon qubit systems required either (i) high precision Electron-Beam Lithography (EBL) for gate patterning on a planar Si or SiGe substrate [48], or (ii) narrow etching of a thin nanowire in a Fully-Depleted Silicon-On-Insulator (FDSOI) substrate [49, 50, 51], which are not yet industry-ready for massive scale integrated circuit production. Hence, exploring the potential of existing industry-standard CMOS technologies for QIP could be an efficient way to integrate Si quantum electronics into VLSI. Unlike previously reported quantum platforms, focusing on FDSOI custom devices [52, 53], or just

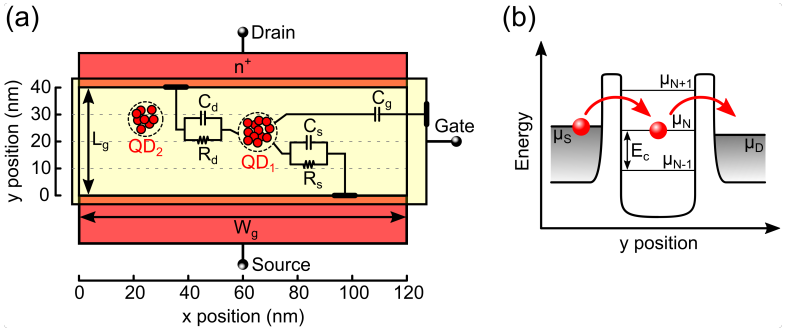

Figure 2.1 – (a) Top view of the MOSFET operated as a quantum device. Red spheres represent charge carriers. (b) Schematic of energy as a function of channel position in the y-axis in (a). μ_s, μ_d and μ_N are the electrochemical potentials of Source, Drain, and QD, respectively. When $V_{ds} = (\mu_s - \mu_d)/e$ is small, I_{ds} only occurs when μ_N is in alignment with the bias window between μ_s and μ_d, meaning that electrons can move from Source to QD to Drain.

CMOS compatible FDSOI nanowire gate-all-around transistors [11], this approach involves fully industry-standard bulk CMOS transistors, with the benefits of the mass-production readiness.
Moreover, scalability of QD array architectures requires compact classical readout and control electronics to be operated in close proximity to the quantum processor. Using standard CMOS technology allows the co-integration of silicon quantum devices with classical analog and digital electronic circuits to reduce the overhead of qubit control and readout [26, 54].
For this reason, in this chapter, commercial bulk 40-nm MOSFETs are explored as a platform for QIP [36]. A statistical characterization of charge transport at deep-cryogenic temperature is performed. At 50 mK, the formation of quantum dots in the channel is observed and a model for how this occurs is proposed. Furthermore, the intra-die variability in parameters important for quantum computing scaling is quantified across different identical devices. In particular, the location of the dots, the voltage to load the first measurable electron, relevant to shared control quantum computing architectures [55], and the gate lever arm, important for dispersive readout schemes [18, 56], are extracted from measurements.

2.2 Devices and experimental setup

Bulk MOSFETs in a commercial 40-nm process are studied. The Devices Under Test (DUTs) are planar low threshold voltage n-type FETs with gate length $L_g = 40$ nm and gate width $W_g = 120$ nm. A drawing of the studied quantum device is shown in Figure 2.1 (a). Charge transport is characterized at 50 mK in an Oxford Instruments Triton dilution refrigerator. The drain voltage V_{ds}, gate voltage V_g, and drain current I_{ds} are applied and measured by a parameter analyzer (HP 4156A). By tuning the devices in the quantum regime, quantum transport is studied. Coulomb blockade parameters such as charging energy E_c, lever arm α and source-drain capacitance ratio C_s/C_d are extracted from a charge stability map (Coulomb diamonds) at low drain bias. Data from 18 DUTs in total, which have nominally identical physical dimensions, are presented and a statistical analysis is performed.

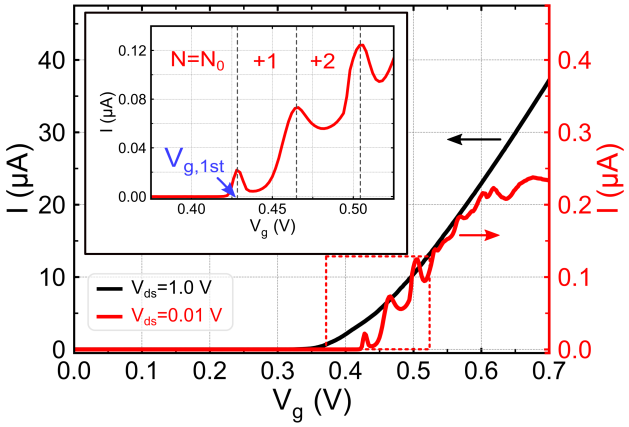

Figure 2.2 – Drain current I_{ds} as a function of gate voltage V_g at 50 mK in the quantum regime. The inset shows a zoom of the red-dotted region, while N indicates the number of electrons.

2.3 Quantum dots in standard bulk MOSFETs

At deep-cryogenic temperatures, MOSFETs with minimum length and width can be operated as quantum devices and show quantum effects. In particular, since the channel size is reduced, at low drain bias, one or more few-electron quantum dots can be created in the channel and Coulomb blockade phenomena can be observed.
When low V_{ds} is applied, Coulomb blockade oscillations are observed near the threshold voltage V_{th} of the transistor, as shown in Figure 2.2. The presence of quasi-periodic Coulomb blockade peaks suggests the existence of a quantum dot in the channel. In low V_{ds} and low V_g regime, the current is dominated by the tunneling current through Source-QD-Drain instead of through the conventional inversion layer. Similar transport behavior was previously observed in a p-type MOSFET platform as well [53].
The number of electrons (N) loaded into the QD can be counted according to the appearance of Coulomb peaks, so that one is able to constrain the QD in the first measurable electron regime, i.e., $N = N_0 + 1$, where N_0 is the offset charge. Coulomb blockade oscillations are observed in all DUTs in the experiment. However, not only devices with quasi-periodic Coulomb diamonds (Figure 2.3 (a)) are observed, but also devices with irregular Coulomb diamonds (Figure 2.3 (b)). Coulomb diamonds that close at $V_{ds} = 0$ mV suggest double or multiple QDs in parallel with Source and Drain.
For the single QD case, the full set of capacitances, namely the gate, source and drain capacitances, can be extracted from a Coulomb diamond diagram as in Figure 2.3 (a).
The charging energy is defined as:

$$E_c = \frac{e^2}{C_\Sigma} = e \cdot \Delta V_{ds}, \tag{2.1}$$

where C_Σ is the total capacitance to the QD, namely $C_\Sigma = C_g + C_s + C_d$. E_c is found to be 18.4 meV, indicating that Coulomb oscillations should still be observable at temperatures as high as 4.2 K, since $E_c \gg k_B T$ at 4.2 K. This was also confirmed by measurement.

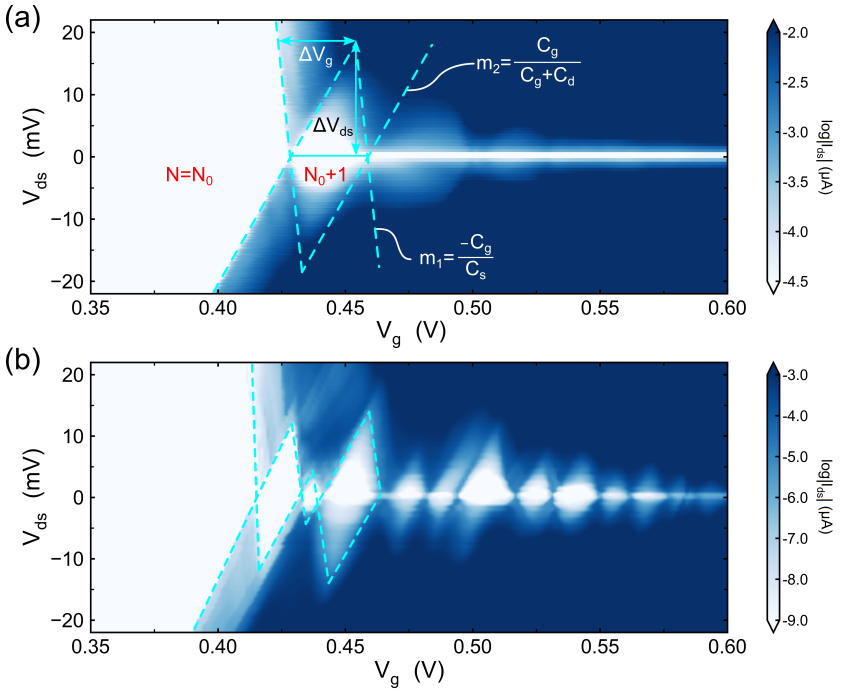

Figure 2.3 – Charge stability diagrams as a function of V_{ds} and V_g of devices **(a)** T01 and **(b)** T07. Measurements are carried out at 50 mK.

The capacitance between the gate and QD can be expressed as:

$$C_g = \frac{e}{\Delta V_g}, \tag{2.2}$$

where ΔV_g is the gate voltage separation between adjacent Coulomb peaks. $C_g = 5.34\,\text{aF}$ is found, corresponding to a QD with an equivalent diameter of $(14.7 \pm 0.7)\,\text{nm}$[1], which suggests that by minimizing channel volume the probability of forming multiple QDs can be lowered. This can be achieved by reducing channel width and length, for instance using a more advanced technology node.
The capacitances between QD/Source (C_s) and QD/Drain (C_d) can be estimated from the slopes of the Coulomb diamond's boundaries as indicated in Figure 2.3 (a):

$$C_s = \frac{-C_g}{m_1}, \tag{2.3}$$

$$C_d = \frac{C_g(1-m_2)}{m_2}. \tag{2.4}$$

[1]The size of the QD is estimated by using a parallel disc model: $C_g = \epsilon_r \epsilon_v \pi r^2/d$, where ϵ_r and ϵ_v are SiO_2 relative permittivity and vacuum permittivity, respectively, r is the radius of the QD disc and for the separation between the gate electrode and the QD disc, the Effective Oxide Thickness (EOT) $d = 1 - 1.2\,\text{nm}$ is used, based on International Technology Roadmap for Semiconductors (ITRS) 2001 and ITRS 2003.

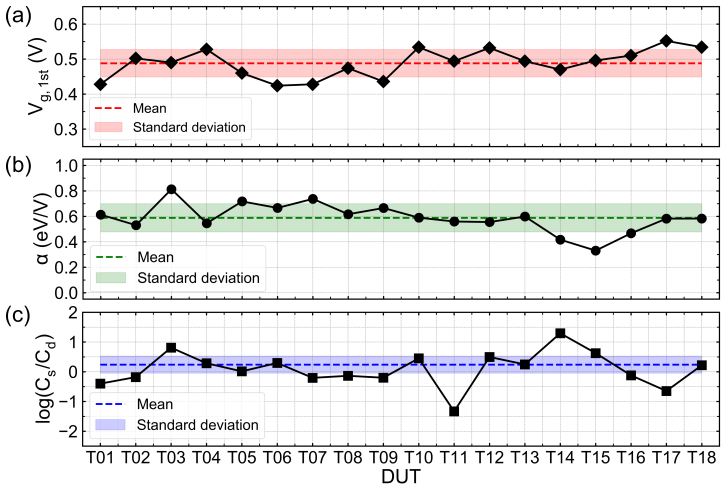

Figure 2.4 – Summary of (a) $V_{g,1st}$, (b) α and (c) C_s/C_d of all measured DUTs. The dashed lines are mean values, and the shaded areas indicate (mean value ± standard deviation).

Thus the capacitance ratio can be expressed as:

$$\frac{C_s}{C_d} = \frac{-m_2}{m_1(1-m_2)}. \tag{2.5}$$

And finally, the gate lever arm is defined as:

$$\alpha = \frac{\Delta V_{ds}}{\Delta V_g} = \frac{C_g}{C_\Sigma}. \tag{2.6}$$

2.4 Quantum dot circuit parameters

For multi-QD systems, as in Figure 2.3 (b), the measured I_{ds} is a result of multiple parallel paths: (i) Source-QD1-Drain; (ii) Source-QD2-Drain; (iii) Source-QD1-QD2-Drain, (iv) Source-QD2-QD1-Drain as in Figure 2.1 (a), and hence it is not possible to extract the full set of capacitances. However, by restricting the analysis to the first Coulomb oscillation, one can obtain a statistical characterization of $V_{g,1st}$, the voltage where the first Coulomb oscillations occur at $V_{ds} = 0\,\text{mV}$, α and the C_s/C_d ratio across the die (Figure 2.4).
The results show a fairly consistent $V_{g,1st} = (0.488 \pm 0.039)\,\text{V}$ (Figure 2.4 (a)), suggesting a small variation from DUT to DUT. A small gate control voltage variation, $\Delta V_g < \Delta V_{g,1st}$, is an essential element for quantum computing, requiring shared control schemes [55]. To allow the use of shared gate voltages V_g in large 2D arrays for VLSI integration, the level of variability of $V_{g,1st}$ should be comparable to the on-chip variability of the gate voltage V_g due to voltage drops or other non-idealities, which is normally in the mV range. The studied DUTs approach this requirement, but further variability reduction will still be necessary.

For the lever arm, $\alpha = (0.6 \pm 0.1)$ eV/V is found (Figure 2.4 (b)). This value is comparably larger than other planar quantum dot devices [57, 58, 59] and just below those reported for 3D geometries [60], such as gate-all-around structures or finFETs, which can achieve higher and more reproducible electrostatic control of the gate on the transistor channel. Large α is essential in dispersive readout schemes [18, 49, 56, 60] and 40-nm bulk MOSFETs should provide a good platform from this point of view.
Finally, the C_s/C_d ratio can be used for estimating the location of the QD in the channel, since in general the capacitance is inversely proportional to the separation between two conductors. C_s/C_d ratio of all DUTs is summarized in Figure 2.4 (c), and the result suggests that the QDs tend to be located in the middle of the channel with good reproducibility and an average deviation of (0.2 ± 6.5) nm from the center. Therefore, one can conclude that the QDs are formed from the charge carrier accumulation due to the applied gate bias rather than from the dopants close to Source and/or Drain diffused regions during the implantation and activation annealing processes. Also, the p-type dopants in the body of the nMOSFET are ruled out as the origin of Coulomb blockade since measurements are performed in the voltage region close to the conduction band edge. Surface roughness and remote charges in the gate stack may as well contribute to the formation of the dots [61, 62]. With all these considerations in mind, a to-scale schematic of how Coulomb blockade transport occurs in the studied 40-nm bulk MOSFETs is shown in Figure 2.1 (a) and the corresponding energy diagram is shown in Figure 2.1 (b).

2.5 Conclusion

In this chapter, a statistical characterization of 18 commercial 40-nm MOSFETs at deep-cryogenic temperatures (50 mK) was presented. At 50 mK under low bias, DUTs behave as quantum devices, and the observation of Coulomb blockade oscillations indicates that quantum dot systems are formed in the channel in the subthreshold region. The properties of the quantum dot systems have been statistically characterized, such as $V_{g,1st}$, gate coupling parameter α, and dot-to-electrode capacitances C_g, C_s and C_d, and it was found that these devices could be a useful resource for large-scale quantum information processing given their low variability, planar geometry and high gate lever arm. The results suggest that 40-nm MOSFETs can be used to build both classical circuits and quantum circuits or to co-integrate the two into quantum-classical hybrids at liquid helium temperatures and below, as will be shown in Chapter 5.

3 CMOS transistors at cryogenic and deep-cryogenic temperatures

The work presented in this chapter has been published in the papers:

[36] T.-Y. Yang, **A. Ruffino**, J. Michniewicz, Y. Peng, E. Charbon and M. F. Gonzalez-Zalba, "Quantum Transport in 40-nm MOSFETs at Deep-Cryogenic Temperatures," *IEEE Electron Device Letters (EDL)*, vol. 41, no. 7, pp. 981-984, July 2020;

[63] A. Beckers, F. Jazaeri, **A. Ruffino**, C. Bruschini, A. Baschirotto, and C. Enz, "Cryogenic Characterization of 28 nm Bulk CMOS Technology for Quantum Computing," *2017 IEEE European Solid-State Device Research Conference (ESSDERC)*, Leuven, September 2017.

In the second work, the test chip was provided, I performed the device measurements together with Arnout Beckers and Farzan Jazaeri, colleagues from ICLAB, then I participated in the data analysis and manuscript writing.

3.1 Introduction

The design of quantum-classical cryo-CMOS integrated circuits and systems requires, together with the development of quantum devices in standard silicon technologies, also the knowledge and understanding of the classical behavior of CMOS transistors at cryogenic and deep-cryogenic temperatures.
CMOS FETs have been demonstrated to be functional and operate down to 4.2 K as well as down to deep-cryogenic temperatures of 100 mK [26]. However, in order to design circuits, a more accurate characterization and modeling of their behavior is needed, with the final objective of developing cryogenic CMOS compact models to be used in simulators and extend the temperature validity range of existing Process Design Kits (PDKs).
To some extent, this has been pursued by the scientific community, which is evident from papers that show DC characterization [26, 63, 64, 65], RF and noise characterization [66], device mismatch [67, 68, 69] of bulk CMOS, as well as DC characterization [52, 70, 71], small-signal and noise characterization [72] of Silicon-On-Insulator (SOI) CMOS devices in different technology nodes. However, the realization of a complete model describing

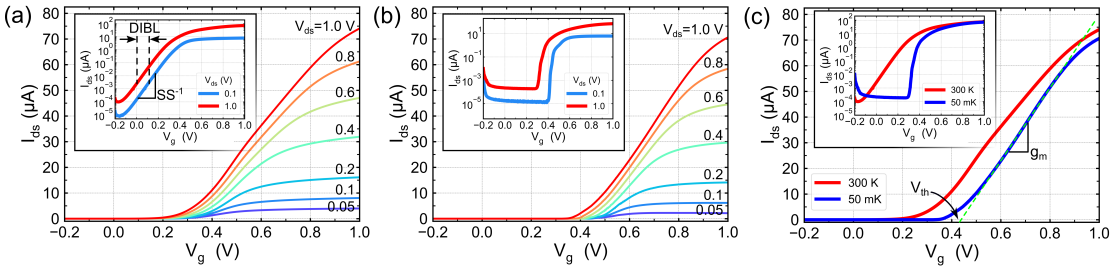

Figure 3.1 – Drain current I_{ds} as a function of V_g at various V_{ds} **(a)** at 300 K and **(b)** at 50 mK. **(c)** I_{ds} as a function of V_g at 300 K and at 50 mK with $V_{ds} = 1.0$ V. The insets report data in logarithmic scale. DIBL represents drain-induced barrier lowering, SS is the subthreshold swing, V_{th} is the threshold voltage, and g_m is the transconductance.

the behavior of transistors at cryogenic temperatures in all its aspects is still not achieved. In this chapter, a first attempt to characterize and model the DC operation of transistors at deep-cryogenic (sub-K) [36] and cryogenic (>4 K) [63] temperatures is presented, to establish some rough understanding of device operation to be used for circuit design in the subsequent chapters.

3.2 MOSFETs at deep-cryogenic temperatures

Previous literature on the cryogenic characterization of CMOS transistors demonstrated the operation of integrated MOSFETs down to 100 mK [26], however, no full extraction of the fundamental device parameters is presented. In this section, bulk CMOS MOSFETs in a commercial 40-nm process are studied in their classical regime at low temperatures. The obtained results show that at 50 mK, these devices can operate as classical transistors or, as shown in Chapter 2, as quantum dot devices when either a high or low drain bias is applied, respectively.

3.2.1 Experimental setup

The tested devices are planar low threshold voltage n-type Metal Oxide Semiconductor (MOS) transistors with gate length $L_g = 40$ nm and gate width $W_g = 120$ nm. Transport is characterized at 300 K and 50 mK in an Oxford Instruments Triton dilution refrigerator. Classical parameters, such as threshold voltage V_{th}, subthreshold swing SS, transconductance g_m, and Drain-Induced Barrier Lowering (DIBL), are extracted from standard $I - V$ measurements.

3.2.2 Deep-cryogenic measurements

The studied DUTs are characterized at room temperature in terms of charge transport by measuring the current I_{ds} as a function of V_g ranging from -0.2 V to 1.0 V with V_{ds} ranging from 0.01 V to 1.0 V, as shown in Figure 3.1.
The classical parameters V_{th}, SS, and g_m can be extracted from the experimental data in

Temperature	300 K		50 mK	
V_{ds} (V)	0.1	1.0	0.1	1.0
V_{th} (V)	0.388 ± 0.030	0.442 ± 0.036	0.514 ± 0.038	0.510 ± 0.037
SS (mV/dec)	86.41 ± 2.43	86.88 ± 1.69	9.93 ± 4.32	15.79 ± 6.27
g_m (µS)	21.48 ± 1.79	118.07 ± 7.48	29.51 ± 6.02	144.53 ± 10.48
ΔV_{th} (V)			0.126 ± 0.017	0.067 ± 0.011
DIBL (mV/V)	162.22 ± 27.85		113.33 ± 24.67	

Table 3.1 – Comparison of classical transistor performance parameters at $V_{ds} = 0.1\,V$ and $V_{ds} = 1.0\,V$ at 300 K and 50 mK.

Figure 3.1 and are collected in Table 3.1.
The ON/OFF ratio of the measured DUTs is approximately 10^6, while the measured subthreshold swing SS is found to be $\sim$ 86 mV/dec, which is slightly higher than the theoretical limit. DIBL is observed in such short channel transistors, as expected, and it has a value of (162 ± 28) mV/V at 300 K.
At 50 mK, with $V_{ds} = 0.1\,V$, an increase in the threshold voltage $\Delta V_{th} = V_{th,50\,mK} - V_{th,300\,K} = 0.126\,V$ is found, which can be understood by the higher Fermi potential at cryogenic temperatures [73]. g_m increases more than 37% and SS decreases to 9.93 mV/dec. Although both results indicate better power efficiency at cryogenic temperatures, SS is still far from the Boltzmann limit. Such data is in line with previous reports, where it saturates to a value proportional to the extent of the conduction band tail [74].

3.2.3 Impact on base temperature circuit design

The obtained results show that bulk CMOS transistors can still be operated as classical transistors down to 50 mK and they exhibit improved performance, in particular better switching behavior. This can be exploited to build simple low-power cryo-CMOS circuits operating at the base temperature of dilution refrigerators (20-100 mK), to be used to directly interface quantum devices. Moreover, these results demonstrate that a different applied bias allows to operate these devices both as classical transistors and as quantum dot devices, thus paving the way for fully-integrated quantum-classical interfaces in standard CMOS silicon chips.
These properties are exploited in Chapter 5 to combine quantum devices and switching transistors to build a quantum-classical interface matrix.

3.3 MOSFETs at cryogenic temperatures

Operation and characterization of CMOS transistors at 50 mK showed interesting results, however, in the perspective of a fully-integrated cryo-CMOS control and readout circuit, it will not be possible to operate the entire architecture directly at base temperature, mainly because the power consumption available at mK temperature would be too small. Therefore, characterization and modeling of MOSFETs at higher cryogenic temperatures, around 1-4 K, is fundamental, in order to design complex integrated circuits for readout and control, capable of implementing the large functionality required by qubits.

Plot symbol	Type	W_g/L_g
●	nMOS	3 µm/1 µm
▲	pMOS	3 µm/1 µm
■	nMOS	1 µm/90 nm
▼	nMOS	3 µm/28 nm
◆	nMOS	300 nm/28 nm

Table 3.2 – 28-nm bulk CMOS measured devices.

Previous research on the cryogenic characterization of advanced CMOS technology nodes exists, as demonstrated by measurements of a 40-nm bulk silicon process at liquid helium temperature (4.2 K) [64] and a 28-nm FDSOI process down to 4.2 K [71].
In this section, the study of a commercial 28-nm bulk silicon process at cryogenic temperatures, namely 77 K and 4.2 K, is reported. Through cryogenic measurement, characterization of the MOSFET behavior is performed, while parameter extraction and modeling are used to quantify the impact of cryogenic temperature on the essential analog/RF design parameters.
In particular, the focus is on: i) the transconductance G_m and transconductance efficiency G_m/I_D used for transistor sizing and biasing; ii) the intrinsic gain G_m/G_{ds} of single transistor amplifiers, which plays an important role in determining the design to achieve the gain needed to amplify the weak signals coming from the qubits, and iii) the transit frequency f_T, which is critical for high frequency qubit readout and control.
This allows to design analog/RF readout and control building blocks that work properly at cryogenic temperature and meet the stringent requirements of classical qubit controllers. Compact models extended to cryogenic temperatures will then be very useful to allow predictive cryogenic circuit design for quantum computing systems. In particular, the simplified charge-based Enz-Krummenacher-Vittoz (EKV) model is used as an interesting first step towards the development of such a cryogenic compact model for advanced technology nodes.

3.3.1 Measurement setup

Measurements were conducted on commercial bulk silicon devices (listed in Table 3.2) fabricated in a 28-nm process. The chip was first wire bonded to standard Printed Circuit Boards (PCBs) using Au wire bonds, as shown in Figure 3.2 (a), and then covered with a glob-top. The PCBs were immersed into liquid nitrogen (77 K) and liquid helium (4.2 K) by means of a dipstick. The results were acquired with a Keysight B1500A semiconductor device parameter analyzer.

3.3.2 DC characterization of transistor parameters

Using this setup, transfer characteristics were measured in linear (V_{DB} = 10 mV) and saturation regions (V_{DB} = 0.9 V), together with output characteristics for different gate voltages.
Figures 3.2 (b)-(f) show the measured transfer characteristics in saturation for the devices

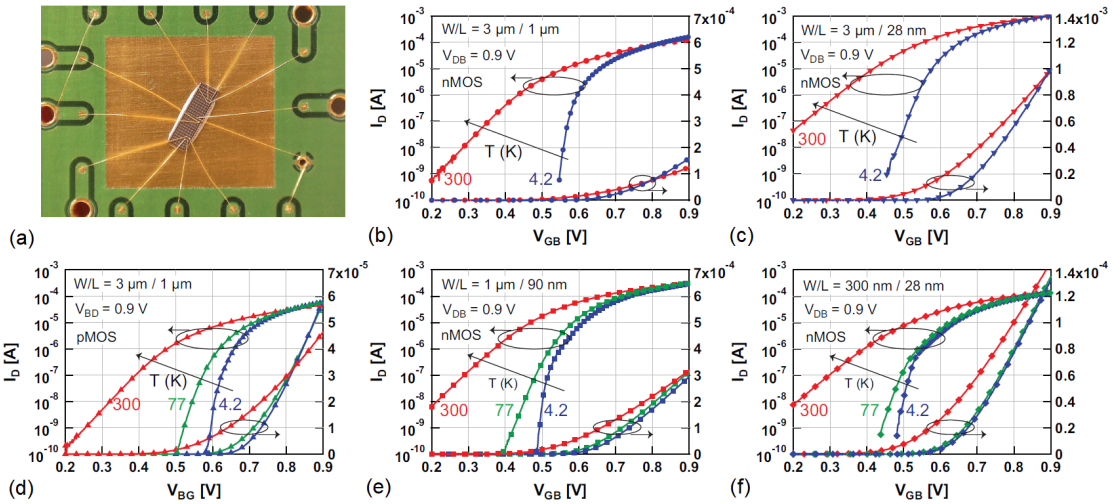

Figure 3.2 – Cryogenic measurements on a 28-nm bulk CMOS technology. (a) Au-wire bonded sample chip glued to a standard PCB, before covering with glob-top. (b)-(f) Measured transfer characteristics at 300 K, 77 K and 4.2 K in saturation (V_{DB} = 0.9 V). In all measurements the gate voltage is referred to the bulk (V_{GB}) and swept from 0.2 V to 0.9 V with a step size of 1 mV. Marker symbols refer to the device type (as shown in Table 3.2). Colors indicate the temperature: red is room temperature (300 K), green is liquid nitrogen temperature (77 K) and blue is liquid helium temperature (4.2 K).

in Table 3.2.
Clearly, SS decreases drastically at 77 K and 4.2 K for all devices. As illustrated in more detail in Figure 3.3 (a), the SS decreases to 11 mV/dec at 4.2 K (-85%) for long channel nMOS (L_g = 1 µm). This decrease is less than the expected value from the theoretical trend ($U_T \ln(10)$ with $U_T = k_B T/e$ thermal voltage), which would result in a SS of 0.8 mV/dec, pointing out that a slope factor n much higher than unity is found at 4.2 K. This can be explained by the presence of an exponential conduction band tail under Fermi-Dirac statistics at low temperature [74]. In short channel nMOS (L_g = 28 nm), the SS reaches 28 mV/dec (-68%). The smaller decrease in SS at cryogenic temperatures in short channel transistors with respect to long channel transistors can be explained by an increased effect of the conduction band tail due to short channel effects, thus causing a highly increased slope factor n at low temperature with respect to the long channel counterpart.
Figure 3.3 (b) emphasizes the strong increase of the slope factor at 4.2 K, which was evident from the extracted values of SS in Figure 3.3 (a). For n = 33 (nMOS, L_g = 28 nm), the modified theoretical trend $nU_T \ln(10)$ indicates a value of 27.5 mV/dec, in accordance with the measured value in Figure 3.3 (a). At 77 K the slope factor remains close to unity (n = 1.6 for nMOS, W_g/L_g = 300 nm/28 nm). Figure 3.4 (a) demonstrates the extraction procedure for the slope factor at 300 K and 4.2 K.
The ON-state current decreases at 77 K and 4.2 K for short devices, while it increases for the long devices (Figure 3.3 (c)).
Additionally, the threshold voltage V_{th} shifts to higher voltages at 77 K and 4.2 K due to the semiconductor bandgap widening and the step-like shape of Fermi-Dirac statistics at low temperatures [31]. The shift in threshold voltage ΔV_{th} with respect to room temperature in Figure 3.3 (d) was extracted from the transconductance in saturation and shows a

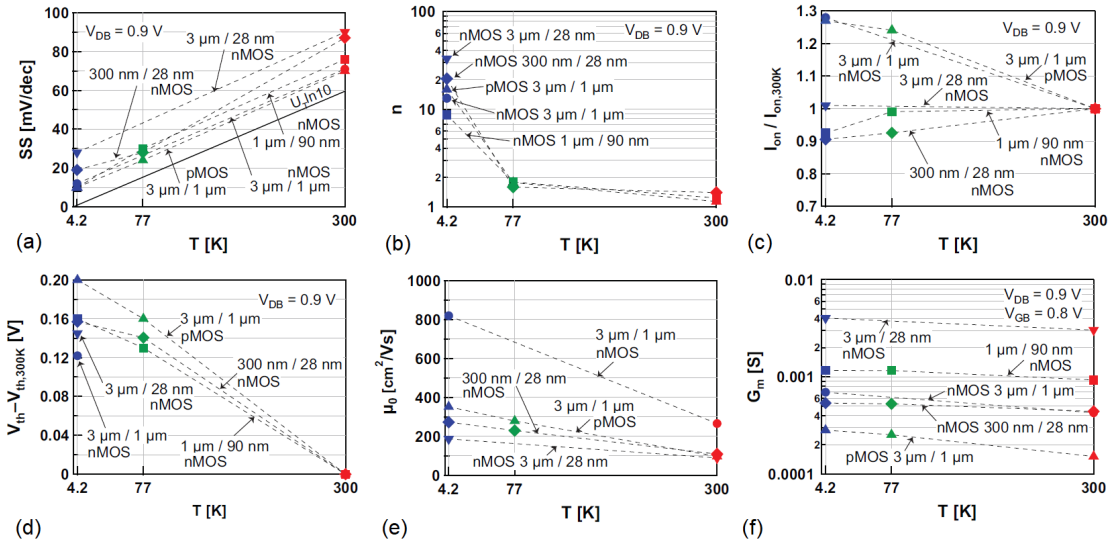

Figure 3.3 – Extraction of the fundamental physical and technological parameters at 300 K, 77 K and 4.2 K. **(a)** Subthreshold swing versus temperature. The results at 4.2 K show a strong deviation from the theoretical trend ($U_T \ln 10$), which is expressed by an increase in the slope factor n. **(b)** Slope factor versus temperature. **(c)** ON-state current normalized to room temperature values. **(d)** Shift in threshold voltage at 77 K and 4.2 K with respect to room temperature, extracted from the transconductance in saturation ($V_{DB} = 0.9$ V) at $V_{GB} = 0.9$ V. **(e)** Low-field mobility versus temperature, extracted using the Y-function method [75]. **(f)** Transconductance in saturation versus temperature.

significant increase, in the order of 0.1 V. It should be noted that the maximum threshold voltage variation is observed in long channel pMOS devices ($\Delta V_{th} = 0.2$ V).
Moreover, relying on the Y-function method [75], the low-field mobility μ_0 was extracted for different gate lengths. Figure 3.3 (e) shows a significant improvement (×3 for nMOS, $L_g = 1\,\mu$m) at 4.2 K due to the phonon scattering reduction, although the Coulomb scattering is becoming dominant at low temperature. As expected, the mobility for nMOS is higher than for pMOS at room temperature. When cooling down to cryogenic temperatures, it can be observed that the increase in mobility is comparable for the two transistor types. This behavior is expected, since the reduced scattering mechanisms have a similar effect to increase the mobility both for electrons in the conduction band and for holes in the valence band.
As shown in Figure 3.3 (f), the transconductance in saturation $G_{m,sat}$ improves at 4.2 K (×1.3 for nMOS, $W_g/L_g = 3\,\mu$m/28 nm).

3.3.3 Analog/RF circuit design parameters

Once the fundamental transistor parameters at cryogenic temperature have been extracted from the measured $I - V$ characteristics, the impact of cryogenic temperatures on the essential analog/RF design parameters can be analyzed, as shown in Figure 3.4.
The transconductance efficiency $G_m n U_T / I_D$ in Figure 3.4 (b) and the normalized transconductance at the source $g_{ms} = nG_m/G_{spec}$ with $G_{spec} = I_{spec}/U_T$ and $I_{spec} = 2(W_g/L_g)n\mu_0 C_{ox} U_T^2$

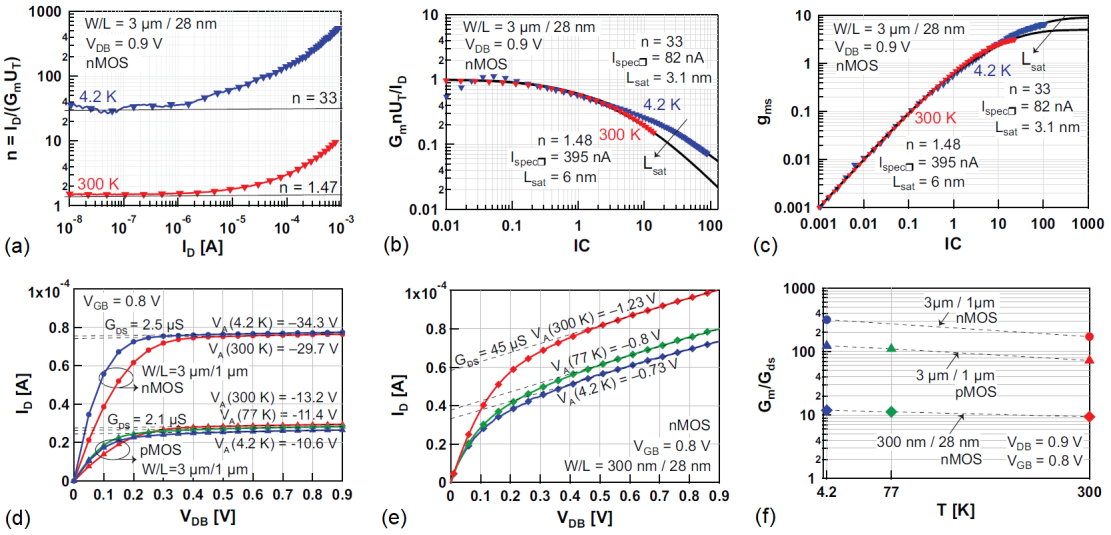

Figure 3.4 – Impact of cryogenic temperatures on analog design parameters. (a) Slope factor versus drain current at 300 K and 4.2 K for nMOS with $W_g/L_g = 3\,\mu m/28\,nm$. (b) Normalized transconductance efficiency versus inversion coefficient for nMOS with $W_g/L_g = 3\,\mu m/28\,nm$, showing a decreased velocity saturation effect at 4.2 K. Solid lines: model. (c) Normalized source transconductance versus inversion coefficient. Solid lines: model. (d) Measured output characteristics for long channel nMOS and pMOS with $W_g/L_g = 3\,\mu m/1\,\mu m$ with extracted values for the output conductance and the Early voltage V_A. (e) Measured output characteristics for short channel nMOS with $W_g/L_g = 300\,nm/28\,nm$ with extracted values for the output conductance and V_A. (f) Intrinsic gain at 300 K, 77 K and 4.2 K.

in Figure 3.4 (c) both show a lower impact of velocity saturation at 4.2 K in strong inversion, when the Inversion Coefficient (IC) ($= I_D/I_{spec}$) is > 10.
The saturation length (L_{sat}) is reduced from 6 nm at 300 K to 3 nm at 4.2 K for $L_g = 28$ nm. This indicates that the portion of channel in saturation decreases at cryogenic temperatures.
As can be seen in the output characteristics plotted in Figure 3.4 (d) for long channel and in Figure 3.4 (e) for short channel, the output conductance G_{ds} remains practically constant with respect to temperature because $G_{ds} \propto \mu_n \rho$, with ρ the charge density and μ_n the electron mobility, and the transistor carries less charges at a higher mobility. This leads to an increased intrinsic gain G_m/G_{ds} at 77 K by a factor of 1.2 and at 4.2 K by a factor of 1.3 for an nMOS with $W_g/L_g = 300\,nm/28\,nm$ (Figure 3.4 (f)), which is promising for cryogenic amplifier design.
Assuming the capacitances do not change significantly going down in temperature [76], the transit frequency (f_T) follows the increase in the transconductance as in Figure 3.3 (f). This increase can be be traded for a lower power consumption, beneficial in terms of heat dissipation from the control system to the qubits. In weak inversion, the current required at cryogenic temperature T to obtain the same f_T as at 300 K, can be evaluated as:

$$\frac{I_D}{I_{D,RT}} = \frac{n}{n_{RT}} \cdot \frac{T}{300\ K}, \tag{3.1}$$

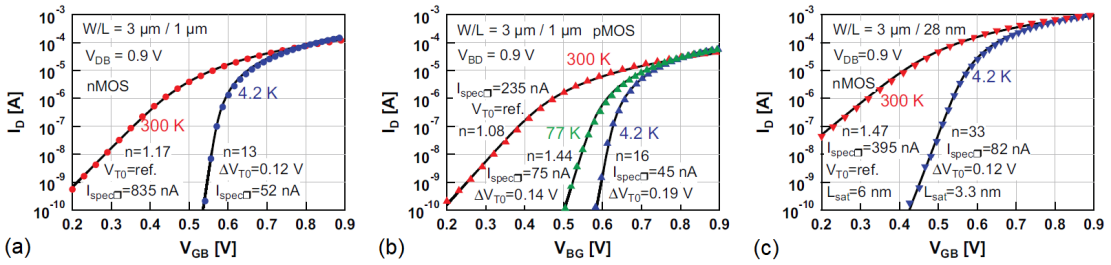

Figure 3.5 – Transfer characteristics: measured (markers) and modeled (solid lines) with the simplified EKV long/short channel model for (a) nMOS with $W_g/L_g = 3\,\mu m/1\,\mu m$ at 300 K and 4.2 K, (b) pMOS with $W_g/L_g = 3\,\mu m/1\,\mu m$ at 300 K, 77 K and 4.2 K and (c) nMOS with $W_g/L_g = 3\,\mu m/28\,nm$ at 300 K and 4.2 K. For each curve, the model parameters are shown.

where n_{RT} and $I_{D,RT}$ are room temperature values. Ideally, if n was the same at 300 K as at 4.2 K, the current reduction factor would be very large and power savings exceptional. However, the current follows the temperature trend only when n is close to n_{RT}, which is the case at 77 K but not at 4.2 K. So, at 77 K, where the change of n is only minor (typically 1.6), the current reduction factor is 3.6. At 4.2 K, where there is a strong increase in the slope factor, the current reduction factor is only 5.2 for $W_g/L_g = 300\,nm/28\,nm$ ($n = 20$) and even 3.2 for $W_g/L_g = 3\,\mu m/28\,nm$ ($n = 33$), due to the lower electrostatic control of wider channels. This means that the n factor increase mitigates the expected current savings moving from 300 K to 4.2 K for reaching the same f_T.

3.3.4 Compact modeling with simplified EKV model

The measured transfer characteristics were modeled using the simplified and normalized charge-based EKV model [77, 78] for long and short channel devices. In the EKV model, all the electrical quantities within the transistor are expressed in terms of inversion charge in the channel, thus making it particularly effective in describing the transistor behavior in all regions of operation with continuous analytical expressions. This allows the realization of compact models using only few parameters, forming the core of Berkeley Short-channel Insulated-gate field-effect transistor Model (BSIM) equations, currently implemented in most circuit simulators.
The long channel model relies on only three model parameters: the slope factor n, the threshold voltage V_{T0} and the specific current $I_{spec} = 2(W_g/L_g)n\mu_0 C_{ox} U_T^2$. The long channel model is expressed by:

$$v_p - v_{sb} = \ln\left(\sqrt{4IC + 1} - 1\right) + \sqrt{4IC + 1} - (1 + \ln 2). \tag{3.2}$$

In this expression, $v_p = V_P/U_T$ is the normalized pinch-off voltage, $v_{sb} = V_{SB}/U_T$ is the normalized source voltage referred to the bulk and $IC = I_D/I_{spec}$ is the inversion coefficient. The measured value for IC is plugged into Equation (3.2) to obtain the normalized pinch-off voltage v_p.
This value is linked to the transistor terminal voltages and to the fundamental model

parameters by the expression:

$$v_p - v_{sb} = \frac{V_P - V_{SB}}{U_T} \simeq \frac{V_{GB} - V_{T0} - nV_{SB}}{nU_T}. \tag{3.3}$$

Initial guesses for the model parameters can be estimated from the extracted values. Using Equation (3.3), modeled V_{GB} values are then obtained and the measured I_D values can be plotted versus such modeled V_{GB} values.
The short channel model also adds the saturation length L_{sat} as a fourth model parameter. The short channel model is expressed by:

$$IC = \frac{4(q_s^2 + q_s)}{2 + \lambda_c + \sqrt{4(1 + \lambda_c) + \lambda_c^2(1 + 2q_s)^2}}, \tag{3.4}$$

where $\lambda_c = L_{sat}/L_g$ is the velocity saturation parameter indicating the fraction of the channel in velocity saturation, and $q_s = Q_s/Q_{spec}$ is the normalized inversion charge at the source with $Q_{spec} = -2nC_{ox}U_T$.
This non-linear equation is solved for q_s for each measured value of IC. q_s is then related to the applied voltages by the relationship:

$$v_p - v_{sb} = \ln(q_s) + 2q_s. \tag{3.5}$$

This gives a modeled V_{GB} value in the same way as in the long channel model.
As shown in Figure 3.5, plotting the measured I_D values versus the modeled V_{GB} values, the cryogenic behavior can be accurately predicted by the proposed model for long devices (Figures 3.5 (a), (b)) and short devices (Figure 3.5 (c)). It is worth mentioning that the model parameters obtained here confirm the extracted results from Figures 3.3 (b), (d) and Figures 3.4 (a)-(c).

3.4 Conclusion

In this chapter, characterization, extraction and modeling of transistors at several cryogenic temperatures, ranging from 50 mK to 4.2 K and 77 K is described. The performed measurements show the operation of MOSFETs down to deep-cryogenic temperatures and indicate that several physical device parameters are improved by cooling, while also favourable trends are found for analog/RF circuit design parameters. This set of measurements allows qualitative circuit design at cryogenic temperatures, for low-to-medium complexity designs and the reported trends are used for all the circuit designs described in the following chapters. Moreover, the measurements could be reproduced thanks to the use of a simplified charge-based EKV model. This represents the first step towards the realization of predictive compact models for cryogenic circuit design directly extending the validity range of existing PDKs.

4 Integrated passives at cryogenic temperatures

The work presented in this chapter has been published in the paper:

[79] B. Patra, M. Mehrpoo*, **A. Ruffino***, F. Sebastiano, E. Charbon and M. Babaie, "Characterization and Analysis of On-Chip Microwave Passive Components at Cryogenic Temperatures," *IEEE Journal of the Electron Devices Society (JEDS)*, vol. 8, pp. 448-456, April 2020.

In this work, I designed the resonator and I performed the respective measurements, then, in collaboration with Bishnu Patra and Milad Mehrpoo, colleagues at TU Delft, who designed and measured capacitor and transformer, I participated in the data analysis and development of the models, in particular the electro-magnetic model, and I wrote the manuscript with them.

4.1 Introduction

The design of solid-state electronics at cryogenic temperatures has triggered the need for characterization of active and passive components, as required to reliably predict the performance of cryogenic Radio Frequency Integrated Circuits (RFICs) [80].
The study of the cryogenic performance of integrated transistors is of cardinal importance and was described in Chapter 3, but also passives play a very important role in the design of RFICs.
In the case of passive devices, cryogenic characterization of *off-chip* discrete commercial off-the-shelf capacitors and resistors [81, 82] proved that the capacitance/resistance can significantly change at low temperatures depending on the material, thus affecting circuit performance. In the case of on-chip passive devices, prior work is limited to the measurement of capacitor and resistor values [83, 84]. Consequently, there is a lack of cryogenic models for on-chip inductive/capacitive components predicting their behavior, variation and quality factor.
In this chapter, the characteristics of *on-chip* passive components in bulk CMOS have been measured and modeled at cryogenic temperatures, to complement active device models for accurate prediction of the behavior of RFICs at cryogenic temperatures [79].

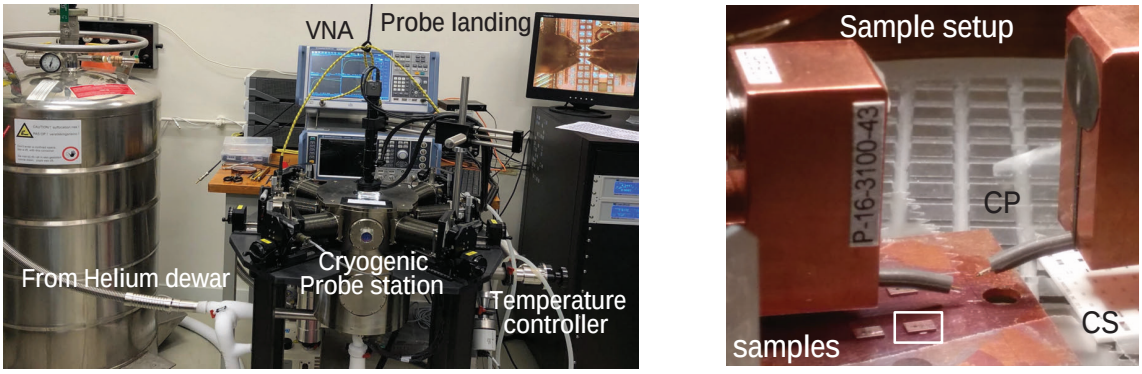

Figure 4.1 – (a) Cryogenic probe station measurement setup. (b) Sample setup inside the 4.2 K chamber.

4.2 Test structures and measurement setup

Several test structures were fabricated in a 40-nm CMOS process with an ultra-thick metal layer to characterize passive components both at 300 K and 4.2 K, comprehensively.
A high-density rotative[1] Metal oxide Metal (MoM) capacitor with a polysilicon shield was chosen from the library provided by the foundry. For the inductance and metal resistance characterization, a transformer with high-inductance *multi-turn* windings was designed to be less sensitive towards calibration errors. Finally, a resonator was also fabricated to validate the cryogenic model of the transformer and capacitor. The substrate was left floating for all test structures.
The measurements were done using Ground Signal Ground (GSG) probes in a 40-GHz Lake Shore CPX cryogenic probe station with Rohde&Schwarz ZNB40 Vector Network Analyzer (VNA). To ensure proper thermalization, the dies were mounted with conductive glue on a copper plate, which was taped to the sample holder (see Figure 4.1).
The thermal conductivity of the chip substrate[2] at temperatures below 20 K is comparable to that at 300 K [85], while the thermal conductivity of copper remains the same or improves at 4.2 K depending on its purity [86], suggesting a good thermal link between the sample holder and DUT. Since all the measured test structures were passive components and the measurements were done by applying small AC signals, self-heating should be negligible. During the measurement the sensor mounted on the sample holder was reading a temperature of 4.2 K. Consequently, although the die temperature was not measured directly, considering the large area under the DUT, no static power dissipation and large copper mass below the dies, it can be concluded that the DUT was at 4.2 K. Moreover, the probes were thermally anchored with thick copper wires to the 4.2 K stage of the probe station.
Due to the variation in the GSG probe electrical characteristics over temperature, Short Open Load Through (SOLT) calibrations were done right before the measurement using a Picoprobe calibration substrate (CS-5) at the measurement temperature. Although the load standards in the CS-5 are accurately trimmed to their 50 Ω stated value at room

[1] with orthogonally interdigitated fingers
[2] boron-doped silicon layers

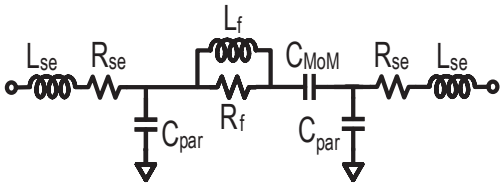

Figure 4.2 – Lumped-element model of MoM capacitor.

Parameter	Unit	300 K	4.2 K
C_{MoM}	fF	191	197
C_{par}	fF	28	26.5
R_{se}	Ω	0.5	0.1
L_{se}	pH	20	20
R_f	Ω	3	3
L_f	pH	17	24

Table 4.1 – Parameters of the MoM capacitor model at 300 K and 4.2 K.

temperature, their absolute value at cryogenic temperature is not specified, and therefore, it was measured by injecting a DC signal. The resistance of the short fixture was measured and it was subtracted from the measurement of the load, so as to remove the effect of cable and GSG probe and to yield the absolute resistance of the load fixture. At 300 K, the measured load was 50.55 Ω, while at 4.2 K its value was 49.91 Ω, showing a negligible (∼ 1 %) change. The measured value of the load was then used as part of the calibration kit file for VNA calibration [87].
For probing, all the components were connected to a 100 µm GSG pad without Electro-Static Discharge (ESD) protection diodes to minimize parasitic capacitance (see chip micrographs in Figure 4.3 (c), Figure 4.4, and Figure 4.8 (b)). The two ground pads in the GSG structure are shorted to each other at metal 1 (M1) level after using vias from AlCu Pad (AP) layer to M1 layer, thus creating a signal-to-ground parasitic capacitance of 60 fF. Finally, the pad parasitics were de-embedded from the measurement results of the test structures by using the open standard, following the method in [88].

4.3 MoM capacitor

A high-density rotative MoM capacitor with a polysilicon shield was taped-out using stacked inter-digitated metal fingers in layers 1 to 5 with a finger width of 100 nm and spacing of 90 nm. To increase the capacitance to a measurable value and in order not to be dominated by the parasitics of pads, 10 such capacitors were connected in parallel, with 6 horizontal and 38 vertical fingers. This provides a capacitance of 202 fF for an area of 150 µm^2 (7.97 µm × 1.89 µm × 10). The distance between the two landing probes is 100 µm and the estimated capacitive coupling between the probe tips based on 3D Electro-Magnetic (EM) simulation is ∼ 0.2 fF.
The MoM capacitor can be modeled by a frequency-independent π-network [89], as shown in Figure 4.2, where C_{MoM} is the actual capacitance due to the interdigitated metal fingers across an extra low-k inter-metal dielectric [90], and C_{par} represents the parasitic capacitance between terminals and ground plane (polysilicon shield). R_{se} and L_{se} represent respectively the access series resistance and inductance of the traces and vias from the pad to the device terminals. Since de-embedding was performed by using an open test fixture, according to the method in [88], R_{se} and L_{se} must be included in the model. The effect of R_{se} is negligible, since the top metal layer was used for interconnection to the pad. However, L_{se} affects the Self-Resonance Frequency (SRF) of the structure. The

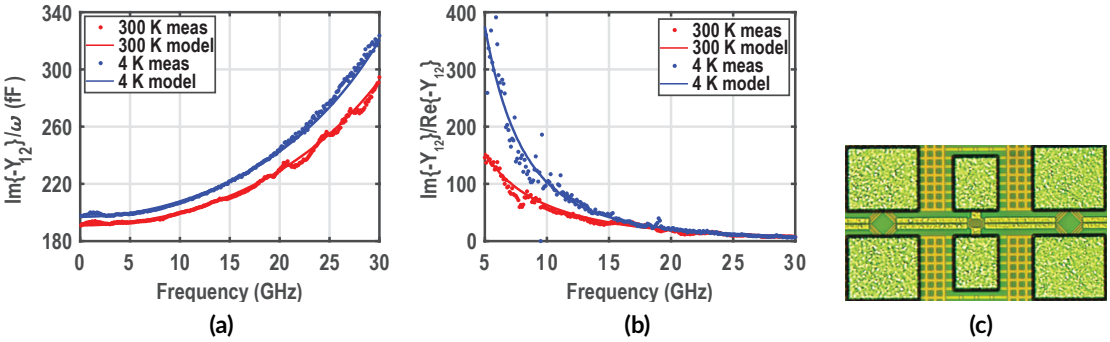

Figure 4.3 – Extraction of MoM (a) capacitance and (b) quality factor. (c) MoM micrograph.

frequency-dependent losses are modeled using R_f and L_f, which represent both metal (skin effect) and dielectric loss. L_f is not a physical parameter, but a fitting parameter, used to model the frequency-dependent loss. The quality factor of the capacitor above 10 MHz is limited by the series resistance [91] and hence, the leakage resistance (modeled as a very high resistance across the capacitor terminals at DC) due to the interface traps [92] is ignored in the model. If inductive and resistive elements in the model are neglected, the capacitive parameters can be extracted using simplified Y-parameters, as shown in the following equations:

$$\begin{aligned} Y_{11} &= Y_{22} = \mathrm{j}\omega(C_{\mathrm{par}} + C_{\mathrm{MoM}}) \\ Y_{12} &= Y_{21} = -\mathrm{j}\omega C_{\mathrm{MoM}} \\ Y_{11} &+ Y_{12} = \mathrm{j}\omega C_{\mathrm{par}}. \end{aligned} \tag{4.1}$$

Figure 4.3 (a) shows the measured $\Im\mathrm{m}\{-Y_{12}\}/\omega$, where ω is the angular frequency, from which the C_{MoM} can be extracted at the lowest measured frequency (i.e., 100 MHz), where the effect of parasitic inductance is negligible [93]. Similarly, C_{par} can be extracted from the measured $Y_{11} + Y_{12}$. The MoM capacitance incurs a slight change at 4.2 K compared to room temperature due to variation in the dielectric constant, as the thermal contraction of metals is negligible [86]. Based on several measurements, the precision error in C_{MoM} value was obtained to be less than 1 % (i.e., $\sim$ 0.5 fF variation in 200 fF).
For the quality factor, expressed as $\Im\mathrm{m}\{-Y_{12}\}/\Re\mathrm{e}\{-Y_{12}\}$, the real part of the transadmittance $\Re\mathrm{e}\{-Y_{12}\}$ represents an equivalent conductance in parallel to the capacitor itself in a parallel G-C model, which corresponds to the equivalent series resistance of the capacitor in the associated series R-C model. The measurement uncertainty increases when the desired real impedance is negligible compared to the VNA reference impedance of 50 Ω [94]. Hence, at frequencies below 5 GHz, where the equivalent series resistance is very small since only the access resistances play a role, the error in the determination of the equivalent series resistance and capacitor's quality factor would be significant and is excluded from Figure 4.3 (b). Due to the reduction of dielectric and metal loss at lower temperatures, there is a boost in the quality factor at frequencies below 10 GHz. However,

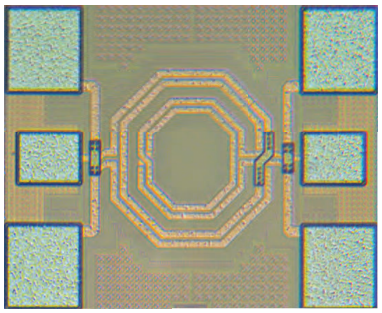

Figure 4.4 – Transformer micrograph.

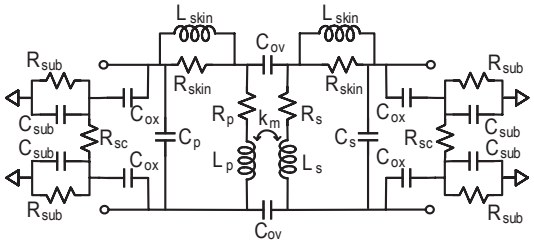

Figure 4.5 – Transformer model.

Parameter	Unit	300 K	4.2 K
L_p	pH	691	650
R_p	Ω	0.95	0.22
R_{skin}	Ω	1.2	0.53
L_{skin}	pH	48	48
C_p	fF	18	19
C_{ox}	fF	50	52
C_{sub}	fF	19	22
R_{sub}	kΩ	1.24	1000
R_{sc}	kΩ	2	2000
C_{ov}	fF	4.5	4
k_m		0.367	0.39

Table 4.2 – Parameters of the transformer lumped-element model at 300 K and 4.2 K.

the dielectric loss does not improve over temperature above a certain frequency. This is also in line with the measurement results of capacitors in the military temperature range in a similar technology, as presented in [91]. Consequently, a negligible quality factor improvement is observed above 15 GHz, as can be gathered from Figure 4.3 (b). Table 4.1 concludes the discussion on MoM capacitors and summarizes the change of the model parameters over temperature.

4.4 Transformer

A multi-turn transformer featuring a two-turn primary winding with 190 µm diameter and 8 µm trace width and a two-turn secondary coil with 130 µm diameter and 7 µm trace width, as illustrated in Figure 4.4, was designed using the ultra-thick metal layer. This structure and sizes were chosen as a good compromise to achieve large inductance with multiple turns, intermediate coupling factor, and measurable series resistance, to minimize the sensitivity towards errors in calibration. Shielding of the transformer was prevented due to a highly resistive substrate at 4.2 K, thereby not having the need to reduce the tangential electric field losses in low-resistive substrates [95]. An open test fixture was used to de-embed the pad parasitics, following the procedure in [88], and this is sufficient for a transformer since the DUT plane is at the GSG pads.
The dotted lines in Figure 4.6 show the extracted parameters of the transformer versus frequency based on the S-parameter measurements at both 300 K and 4.2 K. At first glance, it can be observed that there is a slight reduction in transformer inductance, an increase in the coupling factor k_m and a substantial improvement in the quality factor of the transformer windings at 4.2 K compared to 300 K. To gain more insights and to track the

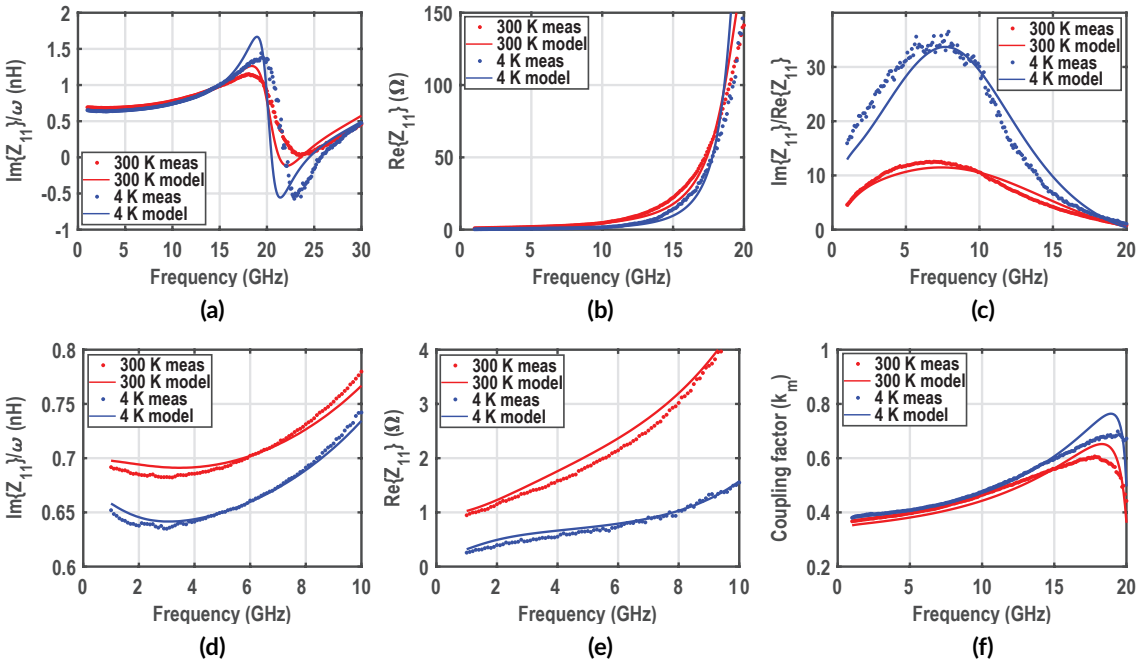

Figure 4.6 – Extraction of (a) inductance, (b) series resistance, (c) quality factor, (d) inductance (zoomed in), (e) series resistance (zoomed in), (f) coupling factor, from measurement and lumped-element model of the transformer[3].

changes in various parameters over temperature, a lumped-element model is presented in Section 4.4.1. Based on the developed model, some modifications to the physical parameters of the metal stack provided by the foundry are suggested in Section 4.4.2. The measurement results are also replicated by using EM simulations.

4.4.1 Lumped-element model

The transformer can be modeled using the well-known frequency-independent lumped model for on-chip spiral inductors [96], as depicted in Figure 4.5, where L_p and L_s represent the inductance, R_p and R_s describe the DC ohmic loss of the primary and secondary windings, respectively. k_m represents the coupling factor of the transformer. C_{ov} models the interwinding capacitance, C_{ox} denotes the oxide capacitance, while C_p and C_s represent the capacitance due to metal lines running in parallel in the multi-turn primary and secondary winding, respectively. R_{skin} and L_{skin} model the frequency-dependent losses (skin effect) in the transformer windings. C_{sub} and R_{sub} model the substrate capacitance and resistance, respectively, while R_{sc} represents an inter-substrate coupling resistance. R_p (extracted from $\Re\mathrm{e}\{Z_{11}\}$ shown in Figure 4.6 (b)) at 1 GHz, where the skin effect is negligible, is $\sim$ 5× lower at 4.2 K compared to 300 K, due to the increase in copper

[3]As can be gathered from Figure 4.6 (a), the transformer SRF is at 21 GHz. Hence, Figures 4.6 (b), (c), (f) have been plotted up to 20 GHz. To keep the visibility, the zoomed in version of $\Im\mathrm{m}\{Z_{11}\}/\omega$ and $\Re\mathrm{e}\{Z_{11}\}$ are shown up to 10 GHz in Figures 4.6 (d), (e).

conductivity σ_{cu} [86]. Note that, the resistivity of copper does not reduce proportionally with temperature until 4.2 K but it saturates at certain temperatures, due to impurities and crystallographic defects in the metal layers [80]. At higher frequencies, the skin effect dominates and the loss becomes proportional to $1/\sigma_{cu}\delta_{cu}$, where the skin depth is $\delta_{cu} = \sqrt{2/\omega\mu_{cu}\sigma_{cu}}$, while $\mu_{cu} = \mu_v\mu_r$ is the magnetic permeability of copper given by the product of the magnetic permeability of vacuum μ_v and the relative magnetic permeability μ_r. Since the copper conductivity σ_{cu} increases by 5×, skin depth and thus the inductor loss at higher frequencies decrease by $\sim \sqrt{5}$ [97], as confirmed by Figure 4.6 (b) for frequencies above 10 GHz.
The inductance associated with a loop has two components: internal (L_{int}) and external (L_{ext}) inductance [98]. L_{ext} dominates the total inductance and it is dictated by the currents that flow on the surface of the conductor. Its value is determined by the phase velocity and characteristic impedance of the inductor trace, and hence, it is a strong function of the coil dimension. L_{int}, the non-dominant component, is associated with the internal current of the inductor and can be calculated as:

$$L_{int} = \frac{R_{AC}}{\omega} = \frac{l}{2d}\sqrt{\frac{\mu_{cu}}{\sigma_{cu}\pi f}}, \tag{4.2}$$

where R_{AC} is the AC resistance, f is the frequency, l and d are the length and width of the trace, respectively [98]. Intuitively, an increase in conductivity would reduce the skin depth and force the current to flow in the boundary of the conductor. Consequently, the current flowing in the conductor interior reduces, decreasing L_{int}, and thus, the total inductance. This phenomenon is also observed in these measurement results: the 5× increase in conductivity leads to a reduction in inductance by $\sim$ 5% (extracted from $\Im\mathfrak{m}\{Z_{11}\}/\omega$ at the lowest measured frequency) as shown in Figures 4.6 (a), (d).
Figure 4.6 (c) reveals that the peak quality factor of the primary winding of the transformer (extracted from $\Im\mathfrak{m}\{Z_{11}\}/\Re\mathfrak{e}\{Z_{11}\}$) increases by 2.7× from 300 K to 4.2 K. The improvement is partially contributed (1.6× as verified from EM simulation in Section 4.4.2) by the increase in conductivity and partly due to the reduction of tangential electric field losses in the silicon substrate, as it becomes highly resistive due to dopant freeze-out.
Figure 4.6 (f) shows the measured k_m, calculated as $k_m = \Im\mathfrak{m}\{Z_{21}\}/\sqrt{\Im\mathfrak{m}\{Z_{11}\}\cdot\Im\mathfrak{m}\{Z_{22}\}}$, at both 300 K and 4.2 K. The coupling factor is mainly set by the physical dimensions of the transformer, which barely change over temperature (i.e., < 1 % as shown in [86]). Since the magnetic coupling is not considered to be temperature dependent, the slight increase in the coupling factor at 4.2 K is attributed to the change in capacitive coupling.
Table 4.2 summarizes the values of model parameters at 300 K and 4.2 K. All the capacitors slightly change over temperature, which is also in line with the extracted MoM model. R_{sub} and substrate coupling resistance R_{sc} increase by 3 orders of magnitude at 4.2 K mainly due to substrate freeze-out [29]. For slightly resistive substrates, the capacitance from the windings to the ground plane is dominated by C_{ox} [99, 100], while for highly resistive substrates, the effective capacitance is lowered by C_{sub} in series with C_{ox}, resulting in a slight increase in the frequency where peak quality factor occurs. The self-resonance frequency of the transformer increases by 5 %, due to the decrease in both inductance and effective parasitic capacitance to ground.

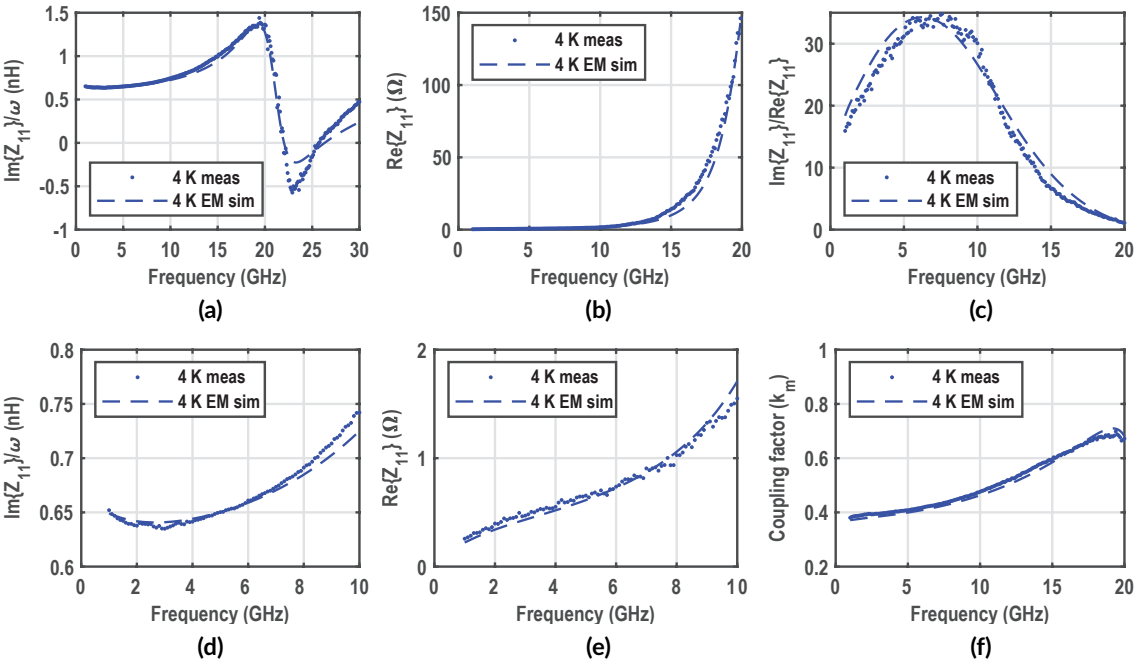

Figure 4.7 – Extraction of (a) inductance, (b) series resistance, (c) quality factor, (d) inductance (zoomed in), (e) series resistance (zoomed in), (f) coupling factor, from measurement and EM simulation of the transformer[3].

4.4.2 EM model

Besides using lumped-element models of integrated passives, it is convenient for circuit designers to perform EM simulations to generate *S*-parameters of inductors/transformers and use them for circuit design. For this reason, and to extend the scope of this work towards the design of cryogenic custom integrated passive networks (e.g., hybrid coupler, power splitter...), the metal stack provided by the foundry was modified to enable EM simulations, predicting cryogenic operation.
Based on the performed measurements, the following material properties have been modified in the foundry metal stack: the conductivity of metal 7 (M7) layer was incremented 5×, to reproduce the copper conductivity increase, while the substrate resistivity was increased 1000×, to reproduce the effect of carrier freeze-out. The obtained modified metal stack was used to perform EM simulations in Keysight ADS Momentum, with an infinite conductive plane underneath the substrate as the current return path, while the simulator temperature was kept at 300 K. The obtained results could accurately predict the performance of the transformer at 4.2 K, as can be gathered from Figures 4.7 (a)-(f). The measured quality factor of the windings was slightly lower than the simulation results at 4.2 K. This is attributed to the exclusion of metal fill in EM simulations, which is required to satisfy the density rules and can slightly degrade the quality factor of an inductor [101].

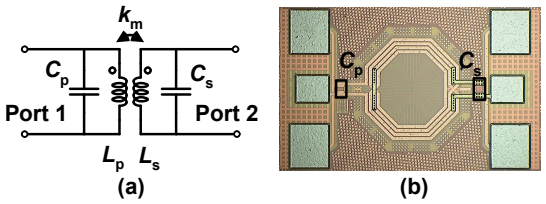

Figure 4.8 – Tank (a) schematic and (b) micrograph.

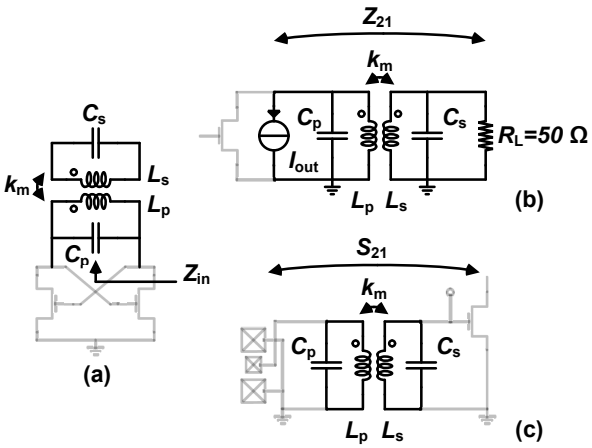

Figure 4.9 – Schematic of transformer-based resonator used in (a) oscillator, (b) power amplifier, and (c) low-noise amplifier.

4.5 Impact on RFICs

To validate the developed models and combine the use of the cryogenic lumped-element modeling for capacitors, with the modified EM simulation for inductors/transformers, a custom transformer-based resonator (matching network), shown in Figure 4.8, was designed. The tank is also used to analyze the impact of cryogenic operation of passive components on the performance of RFIC blocks like oscillators [102], Power Amplifiers (PAs) [103] and wideband LNAs [104]. The application of the transformer-based resonator in such circuits is shown in Figure 4.9.

The custom transformer was realized by an interwinding multi-turn spiral inductor in the ultra-thick metal 7 layer with metal 6 underpass and AP overpass, while capacitors were implemented as design kit rotative MoM capacitors. The resonator parameters are $L_p = 1.25\,\text{nH}$, $L_s = 1.03\,\text{nH}$, $k_m = 0.72$, $C_p = 340\,\text{fF}$ and $C_s = 385\,\text{fF}$.

Its performance at 4.2 K was estimated by combining EM simulation on the developed cryogenic substrate for the spiral transformer and the modified cryogenic model for the capacitors, through layout abutment. The simulation results are compared with the measurement results in Figure 4.10.

Figure 4.10 (a) shows the input impedance of the resonator with Port 2 open ($|Z_{in}|$), which is inversely proportional to the power consumption of a transformer-based oscillator [102] as in Figure 4.9 (a). There is an increase in the impedance peak of the resonator, from 300 K to 4.2 K, due to the overall increase in quality factor, which is well predicted by the cryogenic models. Thanks to this improvement, one can obtain the same output voltage swing for smaller current consumption, thus improving the oscillator's power efficiency. The reduction in inductance and the effective parasitic capacitance causes the first resonance to shift towards higher frequencies by 8 %. The ratio of the resonant frequencies (i.e., the frequency separation between the impedance peaks in $\Re\mathrm{e}\{Z_{in}\}$) merely depends on the coupling factor (k_m), which increases by 4%, as predicted by the model.

Figure 4.10 (b) shows the trans-impedance Z_{21} of a matching network, where the tank in

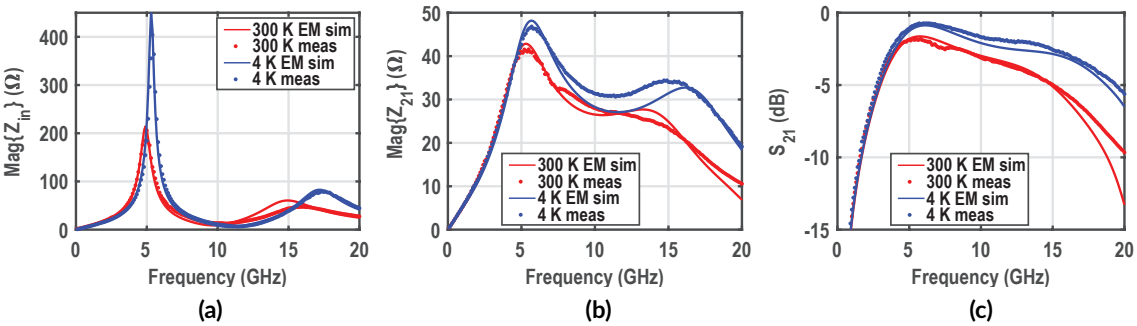

Figure 4.10 – Tank (a) input impedance (Z_{in}), (b) trans-impedance (Z_{21}) and (c) insertion loss (S_{21}).

Figure 4.9 (b) is terminated with a 50 Ω load resistance. This parameter is widely used in calculating the output transfer function when designing wideband PAs [103]. It can be observed that there is a substantial increase in the Z_{21} at 4.2 K compared to 300 K, especially at higher frequencies. Moreover, there is a slight increase in bandwidth due to the increase in k_{m} and an overall shift of the poles of the transfer function towards higher frequencies, due to the decrease in inductance of the windings. Such improvements can be exploited to deliver larger output power for the same current, and over a larger bandwidth at 4.2 K with respect to 300 K, so this is a considerable advantage for PA design at cryogenic temperatures.
Figure 4.10 (c) shows the measured S_{21} of the tank, which is required to predict the Insertion Loss (IL) of input/output or inter-stage matching networks in LNAs/PAs as in Figure 4.9 (c). At cryogenic temperatures, S_{21} improves, consequently reducing the insertion loss. Note that, for an input matching network, the insertion loss directly adds to the overall LNA Noise Figure (NF). Therefore, such an improvement represents a clear advantage in designing multi-stage LNAs with large bandwidth operating at cryogenic temperatures. As can be gathered from Figure 4.10, the developed models can fairly predict the cryogenic performance of the passive network in such circuits.
Such models have also been employed to design more complex circuits, such as a cryogenic CMOS circulator [105] described in Chapter 7, based on *LC* first- and second-order all-pass filters, and a parametric CMOS LNA [106], with transformer-based passive amplification. The developed models were used to predict the performance of such circuits at 4.2 K, leading to more optimized designs and gaining more insights about the cryogenic operation of the circuits.

4.6 Conclusion

In this chapter, integrated passive components have been studied at cryogenic temperatures. They show in general higher quality factor (∼ 2.5×) due to higher metal conductivity and lower loss in the substrate. The value of inductive and capacitive on-chip components slightly changes (∼ 5 %) from 300 K to 4.2 K. These variations are reproduced with both lumped-element models and EM simulations by changing the values of metal conductivity and substrate resistivity. Consequently, during circuit design, one can predictively repro-

duce the performance of passives at cryogenic temperature, both by using EM simulation and by scaling lumped-element model parameters. In combination with the presented active device characterization, this allows the reliable design of cryogenic RF integrated circuits needed for the control and readout of future large-scale quantum computers, as presented in the following chapters.

Cryogenic CMOS circuits Part II

5 A quantum-classical cryo-CMOS readout matrix

The work presented in this chapter has been submitted for publication in the paper:

[107] **A. Ruffino***, T.-Y. Yang*, J. Michniewicz, Y. Peng, E. Charbon^{+} and M. F. Gonzalez-Zalba^{+}, "Integrated multiplexed microwave readout of silicon quantum dots in a cryogenic CMOS chip," submitted to *Nature*, arXiv:2101.08295 [quant-ph], January 2021.

In this work, I conceived the circuit and designed the chip, then most of the measurements were performed by Tsung-Yeh Yang and John Michniewicz, collaborators at Hitachi Cambridge Laboratory, some of which I contributed to, then I analyzed the data with them, and I wrote the manuscript.

5.1 Introduction

The realization of a practical quantum computer will require, on one side, the implementation of qubits in a reproducible standard technology, and, on the other side, the realization of scalable readout and control electronics.
On the quantum side, the implementation of quantum dots in a fully standard CMOS process, as shown in Chapter 2, represents a major step towards the creation of scalable arrays of quantum devices [36].
On the electronics side, the focus of early attempts to implement cryogenic CMOS circuits for qubits has been on control [108, 109, 110, 111] and on complex RF circuits requiring 1-4 K cryogenic operation, for power consumption reasons. Alternatively, the realization of ultra-low power digital-based control electronics directly operating at mK temperatures [112] has been attempted.
However, high-fidelity readout of quantum states is also important in the realization of practical quantum computers. Several architectures have been proposed to minimize the number of wires required to read out each quantum device [113, 114]. Among them, recently, a conditional readout through a MOSFET has been demonstrated in FDSOI technology [115]. This proposal showed new potential to reduce wiring to quantum devices

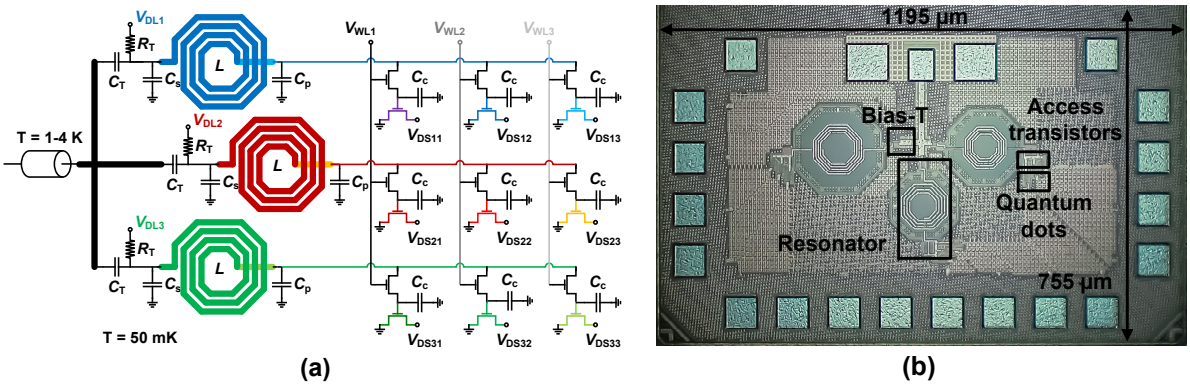

Figure 5.1 – (a) Schematic and (b) chip microphotograph of the quantum-classical readout interface, showing the bias-Ts, integrated *LC* resonators, access transistors and quantum dots.

and improve scalability [116]. The demonstration of such an architecture on a small matrix carrying all the basic features of wiring reduction for larger arrays would represent a milestone in the realization of scalable qubit arrays in fully standard CMOS technologies. Moreover, in order to maximize the flexibility of readout architectures, frequency multiplexing has been proposed for the readout of spin qubits [23], but so far this was always implemented on a separate chip than the actual quantum devices, and never in a standard process.

Finally, recent work has shown trends to increase the frequency of gate-based dispersive readout, whose basics were explained in Chapter 1, towards higher values, close to 6-8 GHz [117], where also new regimes, such as spin-photon coupling, can be explored [118, 119, 120].

In this context, the implementation of CMOS circuits, co-integrated with the qubits and operating at mK temperatures or higher [12, 13], would be the ideal solution to address the needs of scalability and compactness for the realization of practical silicon quantum computers.

In order to address all these challenges, this chapter combines the realization of quantum dots in standard CMOS, shown in Chapter 2, with the knowledge of the cryogenic behavior of transistors and integrated passive components, shown in Chapter 3 and Chapter 4, to demonstrate the suitability of a Dynamic Random-Access Memory (DRAM)-like approach for the realization of a scalable architecture.

A fully integrated 3×3 matrix of quantum dots in standard CMOS technology is implemented, with corresponding classical access transistors arranged in a row-column architecture, and to add frequency selectivity to the matrix, 3 RF resonators are included, one for each row. Both the quantum devices and the classical electronics are co-integrated on the same chip, and are operated at 50 mK. Fully-integrated gate-based readout is performed at frequencies in the 6-8 GHz range, where the gate-based dispersive readout technique has a potential for improved charge sensitivity. Time-multiplexed readout is performed through the access transistors and frequency multiplexing through the resonators. Finally, these two capabilities are combined to realize time- and frequency-multiplexed readout [107].

Row i	C_T (fF)	R_T (kΩ)	C_S (fF)	L (nH)	C_P (fF)	C_C (fF)
1	231	92	231	2.42	540	200
2	81	92	243	1.95	1450	200
3	79	92	210	1.84	1160	200

Table 5.1 – List of values of the circuit components used in the quantum-classical matrix.

5.2 A fully-integrated DRAM-like readout matrix architecture

The proposed quantum-classical readout interface has been designed and fabricated in a fully standard 40-nm bulk CMOS technology. The schematic and layout are presented in Figure 5.1 (a), (b). The matrix consists of 9 silicon quantum dot devices implemented as minimum size MOS transistors (W_g/L_g = 120 nm/40 nm). The gate of each of the quantum devices is connected to the source of an access MOS transistor (W_g/L_g = 15 µm/40 nm) allowing conditional readout, and to a storage capacitor C_C, allowing to store the voltage at the gate of the quantum device. Access transistors on the same column j are controlled by the same word-line signal V_{WLj}. Transistors on the same row i are then connected to an LC resonator, that is used to match the high impedance gate of the quantum devices to the 50 Ω RF input, to perform microwave reflectometry readout of the charge state of the quantum devices. Each of the rows is then biased independently through an on-chip bias-T with a shared data-line signal V_{DLi}, while independent V_{DSij} signals are used to allow tuning of the quantum devices QD_{ij} (with i, j=1,2,3) in the quantum regime. The list of the circuit components in the matrix and their values is reported in Table 5.1.
The quantum dots are arranged in a non-interacting 3×3 matrix structure and the access devices are organized in a row-column random-access arrangement, resembling a DRAM structure. This architecture allows the control of N^2 quantum devices with the use of $2N$ control lines (V_{WLj} and V_{DLi}), which considerably reduces the wiring overhead for large scale-quantum computers and improves the 1-to-1 scaling of current quantum device wiring paradigms.

5.3 A quantum-classical integrated circuit in CMOS

In the proposed architecture, silicon quantum dots are realized as minimum size nMOS transistors in standard bulk CMOS 40-nm technology, as described in Chapter 2. These devices use a low threshold voltage V_{th} mask and are implemented as single finger transistors in a deep n-well, to isolate them from substrate noise. Minimum length and minimum width are chosen to minimize channel volume, where electrons can be electrostatically confined and create few-electron quantum dots at low temperature.
When cooled down to 50 mK, and tuned in the low V_{DS} regime, these devices exhibit quantum behavior, as few-electron silicon quantum dots [36]. The transfer curve $I_{DS} - V_G$ with $V_{DL} \simeq V_G$ is shown in Figure 5.2 (a), and characteristic Coulomb oscillations in current are visible. The corresponding stability diagram shows the characteristic Coulomb diamonds in Figure 5.2 (b). Such behavior is also observed at 4.2 K, which represents the onset of these quantum phenomena at cryogenic temperatures. While at 4.2 K only few

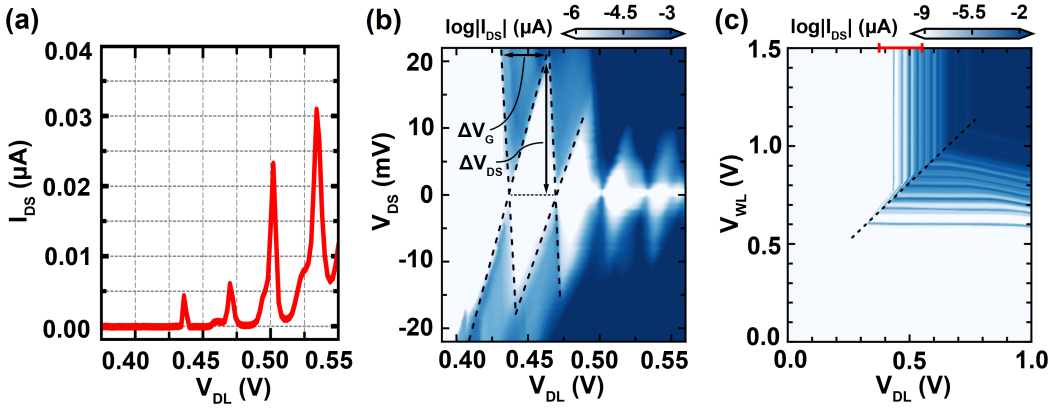

Figure 5.2 – Evidence of quantum phenomena at 50 mK. (a) DC transport current measurement for the individual quantum dot device QD_{33} on chip, acquired through the access transistor in the active state, with $V_{WL} = 1.5\,V$, $V_{DL} \simeq V_G$ and $V_{DS} = 10\,mV$. (b) Coulomb diamonds derived from transport measurements in DC for the quantum dot device QD_{33}. (c) Charge stability diagram V_{WL}-V_{DL} of the quantum dot device-access transistor cell QD_{33}-FET_{33}, with $V_{DS} = 10\,mV$.

devices show Coulomb oscillations, at 50 mK all of the 9 devices in the matrix exhibit quantum behavior. The acquired data is obtained from quantum dot devices with the access transistor in the active state.
In Figure 5.2 (c) the functionality of the access transistor-quantum dot cell is demonstrated and the allowed and forbidden regions for readout are highlighted. When $V_{WL} - V_{DL} < 0.277\,V$ (below the black dashed line), the access transistor channel resistance R_{acc} becomes comparable to the QD transistor gate leakage resistance R_G, therefore the effective gate voltage for the QD transistor $V_G = V_{DL} \cdot \frac{R_G}{R_{acc}+R_G}$ is reduced. So, the QD becomes effectively decoupled from the data-line. However, when $V_{WL} - V_{DL}$ is far higher than this threshold, i.e., above the dashed black line in Figure 5.2 (c), then $V_G \simeq V_{DL}$, and Coulomb blockade oscillations are observed as a function of V_{DL}.
This represents the first quantum-classical integrated circuit in bulk CMOS technology, since all the components in the readout architecture are fully integrated on a single chip, including quantum dots, active and passive classical components forming the readout interface. For the first time, operation of bulk CMOS circuits integrated with silicon quantum devices is demonstrated at the temperature of 50 mK.

5.4 Time-domain measurements

Each quantum dot device can be read individually through a nMOS access transistor, in a row-column architecture, and this allows to perform gated measurements of transport current for each quantum dot. If V_{DLi} and V_{DSij} are set to the appropriate value for the quantum device QD_{ij}, when the V_{WLj} line is activated, the access transistor is activated and transport measurements can be performed on the associated quantum dot device. In fact, the access transistor controlled by the signal V_{WL} behaves like a switch: in the ON-state it gives a low resistance path to the gate of the quantum dot, while in the OFF-state it disconnects the quantum dot, to store its voltage. In order to increase the charge retention

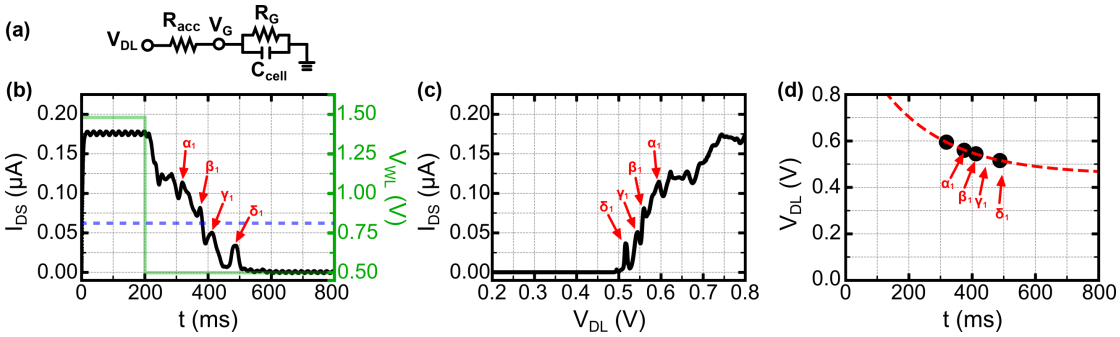

Figure 5.3 – Retention time experiment. (a) Equivalent circuit of a single cell, where V_{DL} is the applied data-line voltage, V_G is the effective gate voltage of the quantum device, R_{acc} is the channel resistance of the access FET, R_G is the gate leakage resistance of the quantum device, and C_{cell} is the equivalent capacitance at the gate of the quantum device. (b) Drain current (I_{DS}) as a function of time (t) (black line) with the application of $V_{WL,High}$=1.49 V for t=0 to 200 ms and $V_{WL,Low}$=0.5 V afterwards (green line), and a constant V_{DL}=0.8 V (blue dashed line). (c) I_{DS} as a function of V_{DL} at V_{WL}=1.49 V. (d) Locations of Coulomb blockade peaks α_1, β_1, γ_1, and δ_1 (see (b)) in time, as a function of the corresponding Coulomb peaks in voltage in (c). The red dashed line is a fit. Measurements are performed at 50 mK on quantum device QD_{23}.

time, an additional capacitor is added at the gate of each quantum device.
The charge retention time for an individual cell is characterized with transport measurements in order to determine the appropriate refresh rate. A simple equivalent circuit model is shown in Figure 5.3 (a) [115]. To extract the retention time, the sequence (i) charging and (ii) discharging is applied. For (i) charging, the cell is firstly charged by applying V_{WL}=1.49 V, as in Figure 5.3 (b), much higher than the threshold voltage of the access FET. This is then followed by (ii) discharging, which consists in reducing V_{WL} to 0.5 V, where the access transistor is highly resistive. The effective voltage on the quantum device gate V_G as a function of time can be expressed as:

$$V_G = V_0 \left[1 + \frac{R_{acc}}{R_G} \exp\left(-\frac{t}{\tau}\right) \right], \tag{5.1}$$

where $V_0 = V_{DL} \frac{R_G}{R_{acc}+R_G}$ is the equilibrium voltage at the quantum device gate at $t \longrightarrow \infty$, and R_G and R_{acc} are the gate leakage resistance of the quantum device and channel resistance of the access FET, respectively. $\tau = C_{cell} \frac{R_G R_{acc}}{R_G+R_{acc}}$ is the circuit time constant, i.e., retention time, where C_{cell} is the parallel sum of the quantum device gate capacitance and storage capacitance C_C in Figure 5.1 (a). By monitoring I_{DS} after V_{WL} is switched from 1.49 V to 0.5 V, Coulomb oscillations are observed as a function of time due to the decay of V_G in time, as shown in Figure 5.3 (b). The observed Coulomb peaks in the time domain, marked as α_1, β_1, γ_1, and δ_1, have their counterparts in the voltage domain as shown in Figure 5.3 (c). Combining the marked Coulomb peaks in time and voltage domains, the data points are fitted to Equation (5.1) and the time constant $\tau \approx 207$ ms is found for this cell, as shown in Figure 5.3 (d).
The time domain measurements for a quantum dot at 50 mK shown in Figure 5.3 highlight an equivalent charge retention time extracted from measurements that is comparable to

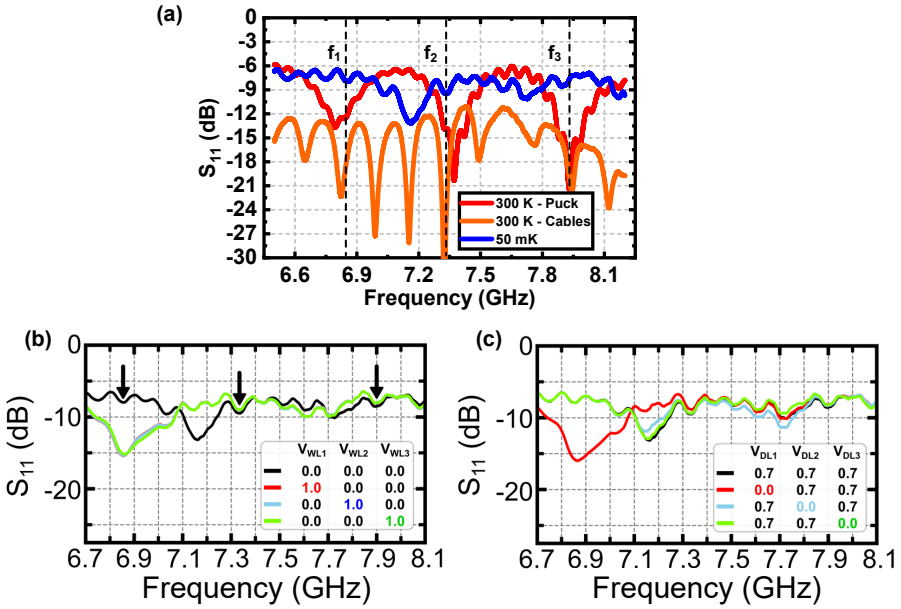

Figure 5.4 – (a) Frequency spectrum at 300 K directly at the sample puck and including all the cables and at 50 mK including all the cables. Spectrum at 50 mK for (b) each word line voltage ON, one after the other, with data line voltage $V_{\mathrm{DLi}} = 0\,\mathrm{V}$, (c) each data line voltage OFF, one after the other, with word line voltage $V_{\mathrm{WLj}} = 1.0\,\mathrm{V}$.

previously reported measurements in FDSOI technology, and is larger than the spin-echo time of typical silicon quantum dots, which demonstrates the viability of this approach for larger scale systems.

5.5 Radio-frequency characterization

The readout matrix includes 3 *LC* resonators (with integrated bias-T to feed DC bias) to perform multi-band impedance matching between the high impedance gate of quantum dots and the 50 Ω impedance of the RF input line. At 300 K, the 3 resonators in Figure 5.1 (a) operate respectively at $f_1 = 6.810\,\mathrm{GHz}$ (Resonator 1, in blue), $f_2 = 7.374\,\mathrm{GHz}$ (Resonator 2, in red) and $f_3 = 7.941\,\mathrm{GHz}$ (Resonator 3, in green), as shown in Figure 5.4 (a), and they introduce frequency selectivity over the different rows. At 50 mK, the corresponding probing frequencies are found to be $(f_1, f_2, f_3) = (6.872, 7.420, 7.951)\,\mathrm{GHz}$. The resonators could be designed to be much closer in frequency, thus enabling a much more dense spectrum utilization, provided limited crosstalk between the channels can be achieved, so as to keep inter-channel interference under a predefined bound, however, to simplify the demonstration, larger spacing was chosen.
At 50 mK, when all V_{WLj} are set to 0 V, the spectrum in Figure 5.4 (b) shows high mismatch, since all quantum devices are deactivated. When each of the 3 word line voltages V_{WLj} is activated, one after the other, one can notice a change of spectrum around the 3 resonances, since all the quantum devices on that column are activated and can be read out at the frequency imposed by the access resonator of their respective row. Moreover, one can see that spectra for different word lines overlap with each other, thus showing that

Temperature	Parameter	Resonator 1	Resonator 2	Resonator 3
300 K	f_{res} (GHz)	6.810	7.374	7.941
	ΔS_{11} (dB)	-6.709	-10.830	-11.169
	Q_{res}	14.478	20.111	14.850
50 mK	f_{probe} (GHz)	6.872	7.420	7.951

Table 5.2 – Benchmark of resonance frequencies, impedance matching and quality factors for the 3 integrated *LC* resonators in the frequency-selective network.

readout at the same frequency is possible for devices on different columns, simply with word line control.
When each of the data line voltages V_{DLi} is (de)activated instead, as shown in Figure 5.4 (c), the corresponding access transistors are turned ON, and one can see that the frequency spectrum changes mostly at the frequency of the corresponding resonator, thus showing the row selectivity of the data line. This demonstrates the functionality of the frequency-selective network, for which a more complete benchmark is shown in Table 5.2.
Similar interfaces were previously reported in literature [23], however typical readout frequencies for RF reflectometry have been mostly limited to < 1 GHz [121]. Recent works have shown trends to perform readout of semiconductor quantum dots at frequencies in the 6-8 GHz range, to explore regimes such as the coupling of spin in the semiconductor quantum dot to microwave photons in the readout resonator [118, 119]. Although these resonators enabled fast state readout [117], hybrid manufacturing was necessary, since they were not integrated on the same chip as the quantum devices. Here, the resonators and the QDs are co-integrated in the same industrial CMOS process.
The choice of a high frequency readout has several advantages. From the design point of view, addressing the 6-8 GHz range, instead of sub-1 GHz readout, makes the design of *LC*-based impedance matching networks on chip much easier, since the size of inductors is more reasonable ($L \sim 1$ nH), and this reduces the footprint of the inductors, the largest elements of the architecture. Furthermore, the resonator quality factor, critical for the sensitivity of the technique [122], is higher for smaller inductors used at higher frequencies. The quality factors in this approach are modest ($Q < 100$) compared to superconductor-based resonators, but show the state-of-the-art of what can be achieved with standard CMOS. Moreover, the gate-based readout technique itself has the potential to improve its charge sensitivity by going to higher frequencies [18]. So, the choice of higher frequency not only enables on-chip integration, but can improve the sensitivity of the readout.

5.6 Gate-based dispersive readout

The resonators are used as sensors to perform integrated gate-based dispersive readout of the charge states of individual silicon quantum dots at 6-8 GHz. The resonators produce an oscillatory voltage on the gate of the QD which can result in cyclic tunneling of electrons back and forth the electronic reservoirs. This results in an equivalent capacitance that modifies the impedance of the resonator producing a change in the reflected voltage.
In this experiment, the RF signal is sent to the common RF input, while an individual

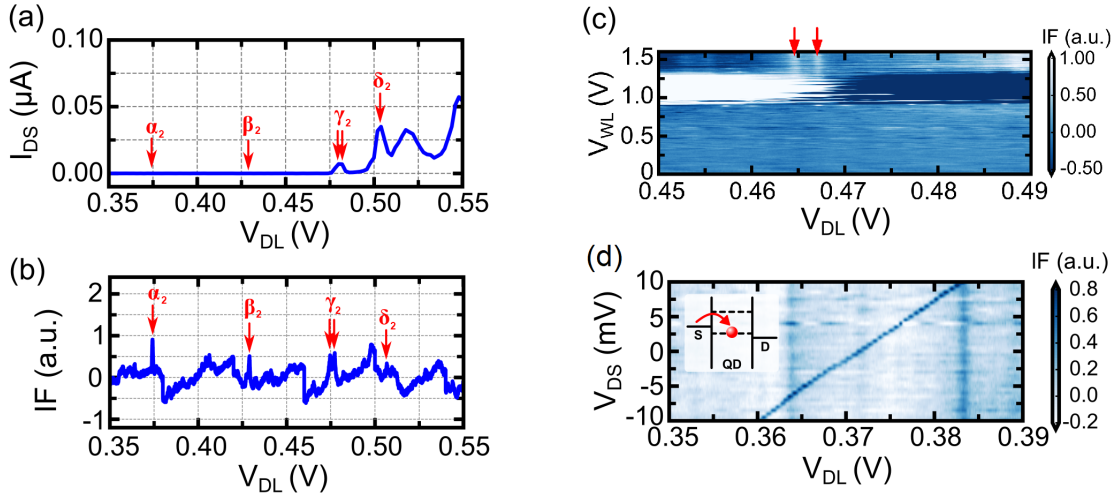

Figure 5.5 – (a) DC transport measurement: I_{DS} as a function of V_{DL}. (b) Gate-based readout: reflectometry signal as a function of V_{DL} at $V_{WL} = 1.5\,V$ and $V_{DS} = 0\,V$. (c) Gate-based readout: reflectometry signal as a function of V_{WL} and V_{DL} at $V_{DS} = 0\,V$. (d) Gate-based readout: reflectometry signal as a function of V_{DS} and V_{DL} at $V_{WL} = 1.5\,V$. Inset: energy diagram of Source-QD-Drain. The measurements are performed at 50 mK on quantum device QD_{13}.

quantum dot is selected by control voltages, then the signal probes the state of the active quantum dot, and reflected waves are separated from incident ones by a cryogenic circulator, the signal is then amplified by a cryogenic LNA and downconverted by a mixer at room temperature, so that finally Coulomb oscillations in reflectometry are read out.
Gate-based reflectometry charge detection is performed on a single quantum dot connected to the lowest frequency Resonator 1 at 6.872 GHz (Figure 5.5 (b)) and results are compared with DC transport measurements (Figure 5.5 (a)) to prove consistency. Peaks γ_2 and δ_2 from the reflectometry detection correspond to DC measurements.
The dependence of this signal on the state of the access transistor is then explored in Figure 5.5 (c), showing allowed and forbidden regions for readout. At low $V_{WL} - V_{DL} < (0.786 - 0.340)$ V, the access transistor is highly resistive and the microwave signal is highly attenuated (OFF region). At intermediate $V_{WL} - V_{DL}$, the access transistor is in the depletion region and the oscillatory voltage at the transistor input produces changes in the capacitance that are picked-up as large changes in the reflected signal (Forbidden region). Finally, at high $V_{WL} - V_{DL} > (1.278 - 0.340)$ V, the access transistor presents a low resistance state and the microwave signal can travel through (ON region), exciting cyclic tunneling in the QD, which manifests as regions of enhanced signal.
Besides the same transitions as in DC measurements, two additional peaks α_2 and β_2 are observed in the reflectometry measurements. In order to understand the origin of these two additional peaks, the signal is measured as a function of V_{DS} and V_{DL} in Figure 5.5 (d). The linearity suggests that this signal comes from the transition between Source and QD. These transitions are results of cyclic tunneling to one of the electron reservoirs only (as opposed to current, that requires sizable tunneling rates to both Source and Drain). The invisibility of peaks α_2 and β_2 in transport measurements can be explained by the fact that at low gate voltages, the volume of the induced quantum dot is small and the location of the quantum dot is much closer to Source than to Drain, so only tunneling from Source

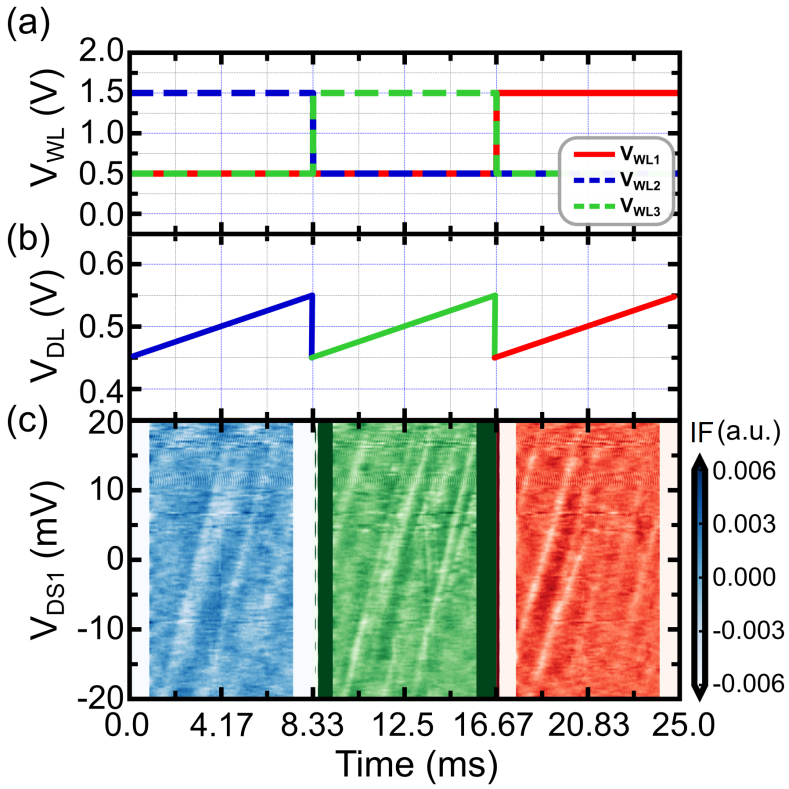

Figure 5.6 – Sequence of signals to perform time-domain multiplexing reflectometry sensing on QD_{12}, QD_{13} and QD_{11}. While (a) V_{WL2} (in blue), V_{WL3} (in green) and V_{WL1} (in red) follow a square wave between 1.5 V and 0.5 V, (b) V_{DL1} follows a synchronized triangular wave and ramps up. (c) Stability diagrams for quantum devices QD_{12} (in blue), QD_{13} (in green) and QD_{11} (in red). The shades indicate the location of Coulomb peaks. Measurements are performed at 50 mK.

to QD is possible, therefore the charge is unable to flow through Source-QD-Drain, thus resulting in no DC current. This highlights the efficiency of gate-based sensing in detecting electronic transitions even if the QDs are offset from the center of the channel and present low tunnel rates to one ohmic contact.
A lineshape analysis from the data in Figure 5.5 (d), reveals a Signal-to-Noise Ratio (SNR) of 28.7 in 400 ms of integration time and a tunnel rate to the Source of 48.3 GHz.
The measurements performed here demonstrate gate-based reflectometry on the lowest frequency resonator at 6.872 GHz and represent the first fully-integrated dispersive readout on a commercial CMOS device and in the 6-8 GHz frequency range. Previous reflectometry experiments have been performed at ~ 6 GHz [117], but resonators were custom fabricated and were not integrated on the same chip with quantum devices in a standard technology.

5.7 Time-multiplexed readout

Once the functionality of the row-column architecture and gate-based reflectometry of integrated quantum dots have been demonstrated, it is possible to perform time-multiplexed reflectometry measurements of quantum dots on the same row, by addressing them at the

frequency of the shared resonator and activating each column one after the other.
In order to perform such experiment, one should make sure that cells (access transistor and quantum device) attached to the same resonator show Coulomb oscillations in the same V_{DL} range. For simplicity, Resonator 1 at the lowest frequency 6.872 GHz is chosen. Quantum devices QD_{11}, QD_{12} and QD_{13} are found to have transitions in the same V_{DL1} voltage range. The dynamic voltage sequence for the time-multiplexing experiment consists of a train of pulsed square waves V_{WLj}, with a digital high voltage ($V_{WLj,High}$=1.5 V) applied to the cell to be read, while the other two cells are set at digital low voltages ($V_{WLj,Low}$=0.5 V). The digital values are selected according to the ON-OFF regions in Figure 5.5 (c). During that period, a voltage ramp is simultaneously applied to the data-line V_{DL1} to acquire the data from the QD_{1j} of the corresponding cell. The V_{WLj} voltage of the next cell is then sequentially raised while keeping the other two low. The full sequence is illustrated in Figure 5.6 (a), (b), where QD_{12} is first measured, followed by QD_{13} and QD_{11}. Finally, the full sequence is repeated as the V_{DS1j} voltages are stepped to acquire the charge stability maps of QD_{12}, QD_{13} and QD_{11}, resulting in a chained series of Coulomb peak transitions in Figure 5.6 (c).
It is important to mention that the Coulomb maps obtained in this time-multiplexed reflectometry experiment are consistent with Coulomb oscillations obtained in DC current transport measurements and in individual gate-based reflectometry experiments on each single cell, they are just a 1×3 time-sequence of them.
It is also worth highlighting that time-domain multiplexing does not necessarily require sequential addressing but can be performed in a random-access manner similar to DRAM architectures.
The results reported here represent the first fully-integrated time-multiplexed measurements of silicon quantum dots in reflectometry in literature. Previous time-multiplexed reflectometry experiments have been performed, but the system was not integrated on a single chip and measurements were not performed in the 6-8 GHz range [115].

5.8 Frequency-multiplexed readout

Once time-multiplexing (exploiting columns) in reflectometry has been demonstrated, the following step consists in using the second degree of freedom in the matrix, frequency-multiplexing (exploiting rows).
For this experiment, Resonator 2 operating at 7.420 GHz can be exploited in combination with Resonator 1 active at 6.872 GHz, to perform parallel readout of two independent quantum dots on different rows (addressable at different frequencies).
To achieve this, quantum dots on different rows showing oscillation in the same range of V_{WL} must be found and quantum devices QD_{12} and QD_{22} fulfill this requirement.
Consequently, two single-tone RF signals at the two chosen resonance frequencies, coming from independent signal generators at room temperature outside the dilution fridge, are combined into the single RF input line. The two sets of waves probe the chip, are reflected, go through a cryogenic circulator and are then amplified by a cryogenic LNA and power split at room temperature to be each separately downconverted by In-phase/Quadrature (I/Q) mixers in a low-IF scheme and acquired. The complete measurement setup used for these measurements is shown in Figure 5.7.

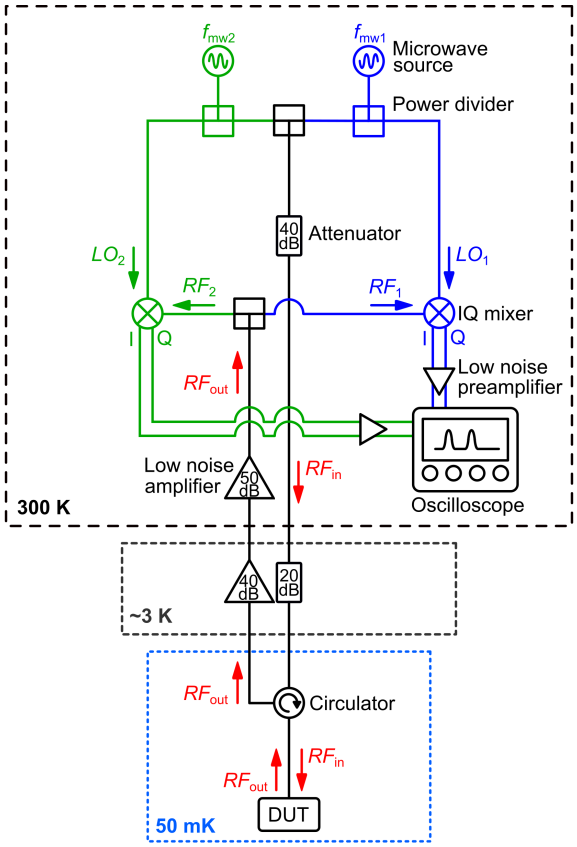

Figure 5.7 – Experimental measurement setup for the (time- and) frequency-multiplexed gate-based readout experiment. The DUT is placed at 50 mK on the sample stage of the dilution fridge. A cryogenic circulator is placed at the mixing chamber plate and a low-noise amplifier and attenuators are placed at intermediate cryogenic temperatures (~ 3 K). At room temperature, two microwave signal sources are power-combined to generate two multiplexed single-tone probing signals f_{mw1} and f_{mw2}, and two I/Q mixers are used to demodulate the reflected signals RF_1 and RF_2 at the two frequencies, by using the microwaves sources as respective local oscillators LO_1 and LO_2. An oscilloscope acquires the I/Q outputs for each of the two tones.

To achieve frequency-multiplexing, as shown in Figure 5.8 (a) (left panels, up to 8.33 ms), the word line voltage V_{WL2} is kept high to activate column 2, while both V_{DL1} and V_{DL2} are ramped up to activate row 1 and 2 (Figure 5.8 (b), left panels, up to 8.33 ms). As a result, a 2×1 parallel set of Coulomb peak transitions from QD_{12} and QD_{22} is obtained, as shown in Figure 5.8 (c), (d) (left panels, up to 8.33 ms).
Also in this case, the Coulomb maps obtained in such frequency-multiplexing experiment are confirmed by DC transport measurements and individual cell gate-based readout. As one can see, the signal coming from the second resonator is weaker. This can be explained by the increasing level of standing waves in the system, as frequency rises, as shown in Figure 5.4.
These results demonstrate, for the first time, fully-integrated frequency-multiplexing gate-based readout of silicon quantum dots on a single chip and in the 6-8 GHz range, unlike in [23].

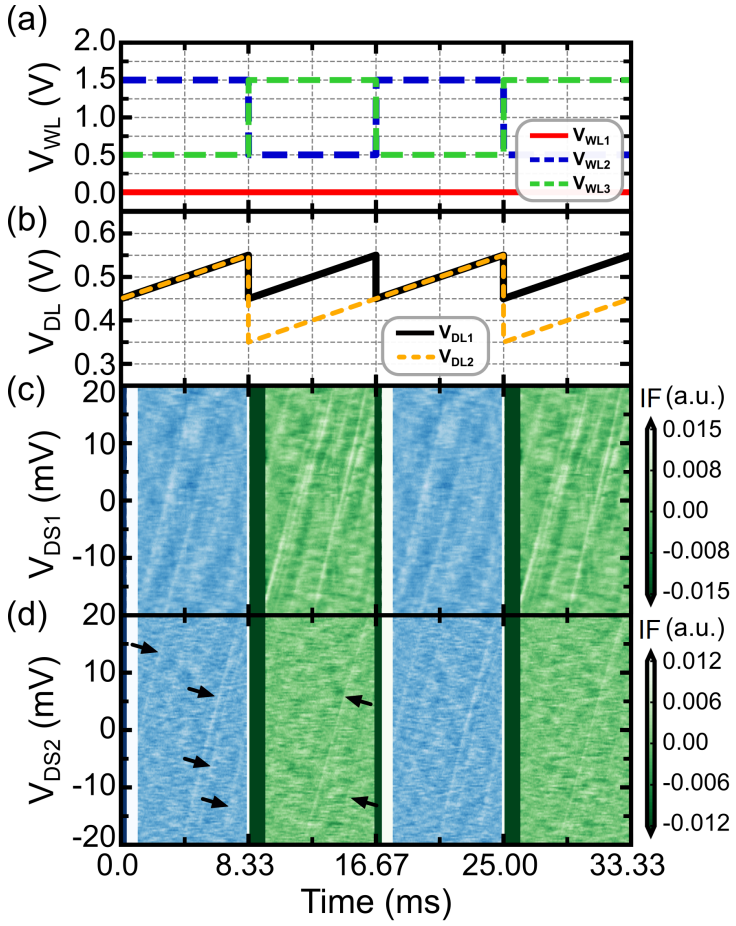

Figure 5.8 – Sequence of signals to perform time- and frequency-multiplexing reflectometry using the 2×2 sub-matrix QD_{12}, QD_{13}, QD_{22} and QD_{23}. While **(a)** V_{WL2} (in blue) and V_{WL3} (in green) follow a square wave between 1.5 V and 0.5 V, V_{WL1} (in red) is disabled and **(b)** V_{DL1} and V_{DL2} follow a synchronized triangular wave and ramp up. **(c)** Stability diagrams for quantum devices QD_{12} (in blue) and QD_{13} (in green) addressed through Resonator 1. **(d)** Stability diagrams for quantum devices QD_{22} (in blue) and QD_{23} (in green) addressed through Resonator 2. The measurements are performed at 50 mK.

5.9 Time- and frequency-multiplexed readout

The last step required to demonstrate the full capability of the designed quantum-classical readout matrix consists in combining time- and frequency-multiplexed gate-based reflectometry, to achieve the maximum degrees of freedom, and consequently scalability, in the structure.

Since time-multiplexing on a 1×3 array including quantum devices QD_{11}, QD_{12} and QD_{13} has been demonstrated, and frequency multiplexing on a 2×1 array including quantum devices QD_{12} and QD_{22}, the 2×2 sub-matrix formed by quantum devices QD_{12}, QD_{13} and QD_{22}, QD_{23} is identified as a good candidate, since Coulomb oscillations in the same range of V_{WL} and V_{DL} have been found.

This experiment consists in using the same setup as for frequency-multiplexing, to address

Resonator 1 and Resonator 2 with two multiplexed single-tone probing signals, while sequencing the word-lines in time to address different columns. As shown in Figure 5.8 (a), the word line voltages V_{WL2} and V_{WL3} follow a train of square wave pulses, to sequentially activate columns 2 and 3, while the data line voltages V_{DL1} and V_{DL2} are ramped up to activate rows 1 and 2 in parallel (Figure 5.8 (b)). The result is a 2×2 matrix of Coulomb maps from the addressed quantum dots (Figure 5.8 (c), (d)). Also for this experiment results are consistent all other DC, individual, time-multiplexed and frequency-multiplexed gate-based readout measurements.
The results presented here demonstrate, for the first time, the combination of time- and frequency-multiplexing gate-based readout for silicon quantum dots, in a fully-integrated platform, with a scalable architecture.

5.10 Conclusion

In this chapter, a fully-integrated quantum-classical cryo-CMOS interface is presented. It consists of a 3×3 matrix of silicon quantum dots with a DRAM-like structure of access transistors and a frequency-selective readout interface with 3 integrated *LC* resonators operating at 50 mK in standard CMOS. Few-electron quantum dots in standard CMOS technology are demonstrated, integrated with classical CMOS readout circuits to realize a quantum-classical integrated circuit at 50 mK. The implementation of a scalable readout architecture that allows to reduce the number of wires for the readout of semiconductor quantum dots is presented. Fully-integrated gate-based dispersive readout of silicon quantum dots at 6-8 GHz is demonstrated. Time-multiplexed readout of silicon quantum dots in reflectometry through access transistors and frequency-multiplexed readout across two different resonators are also shown. Finally, combined time- and frequency-multiplexed readout is demonstrated. The presented results pave the way for the realization of future scalable architectures for silicon quantum computers in standard CMOS technologies.

6 Low-frequency cryogenic CMOS multiplexers

The work presented in this chapter was in part published in the paper:

[123] **A. Ruffino**, Y. Peng, and E. Charbon, "Interfacing Qubits via Cryo-CMOS Front Ends," *2018 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Beijing, November 2018.

In this work, I conceived the circuit, I designed the chip, I performed the measurements with a setup at TU Delft, and I wrote the manuscript.

6.1 Introduction

Scalable readout and control schemes for qubits are required for the realization of practical quantum computers, to tackle the need of accessing many quantum devices, while reducing the complex interconnections between the quantum processor and classical controllers [22].
Multiplexing schemes have been therefore proposed to access multiple qubits, while sharing the same readout and control electronics. Frequency or time multiplexing are usually employed. In the case of frequency multiplexing or FDMA, the qubits are tuned at different frequencies and a single high bandwidth interconnect allows to address them simultaneously [23]. For time multiplexing or TDMA, physical multiplexing structures are used and each qubit is addressed for a portion of the total readout or control time [115].
As shown in Chapter 5 with the presented quantum-classical interface matrix, time-and frequency-multiplexing can be combined to maximize the number of qubits that can be read out with a single wire. Results were presented from a top-level perspective targeting specifically the scalable readout of a matrix of integrated quantum devices.
In this chapter instead, the focus is only on low-frequency physical time-multiplexers that can be used to sequentially read out or control multiple quantum devices. These results contributed to the development of the quantum-classical interface matrix for the time-multiplexing part, but are not limited to it, as they can be applied to any low-temperature sequential switching scheme.

	Specification
Operating temperature	100 mK - 4.2 K
Power consumption	1 mW
Number of channels	4
Bandwidth	100 kHz

Table 6.1 – List of specifications for the design of low temperature multiplexers.

Low-temperature CMOS analog and digital (de)multiplexers have been designed to operate at cryogenic and deep-cryogenic temperatures and to be used in TDMA schemes [123]. Specifications have been drafted first, then different designs have been explored for performance comparison and simulations have been performed to optimize the designs. The layout has been realized and a chip has been taped-out and fabricated. Finally, measurements have been performed both at 300 K and at 4.2 K.
The mentioned steps are explained in detail in the following.

6.2 Specifications

Multiplexers have to be connected directly to the qubits, so ideally they should operate at the base temperature of around 100 mK. Operation of MOSFET devices was characterized down to 100 mK [26] at the time of the design, however, even simple circuits require models to be designed, which were not available then. For this reason, multiplexers have been originally designed targeting 4.2 K operation, where primitive circuit models were available [64]. With this approach, operation at mK temperature cannot be accurately predicted, but a proven functionality at 4.2 K would be a good indicator.
The operating temperature directly sets the maximum power consumption. The cooling power of state-of-the-art dilution fridges at 100 mK is 1 mW, therefore the maximum power consumption is set to this limit, to ensure the possibility to operate the multiplexers also at base temperature.
Given the reduced power budget, circuit complexity should be reduced as much as possible. For this reason, the target number of qubits to be multiplexed is set to 4, in line with the current state-of-the-art in spin qubit fabrication. This limit can be further increased once a demonstrator has been proven.
The target bandwidth for the input signal and for the switching frequency of the designed multiplexers is set to 100 kHz, to explore a low-frequency regime in presence of large input/output loads, such as for off-chip connections.
The ON resistance R_{ON} should be minimized as much as possible, in order to improve transmission and minimize the added noise in series with the signal path. For this reason, the target ON resistance is set to 5 Ω.
The OFF capacitance C_{OFF} should also be minimized, in order to reduce the leakage and improve the isolation. A maximum value of parasitic capacitance of 100 fF is targeted.
Finally, the linearity of the system is relaxed, in consideration of the low power levels typically employed to address the qubits.
The mentioned specifications are summarized in Table 6.1.

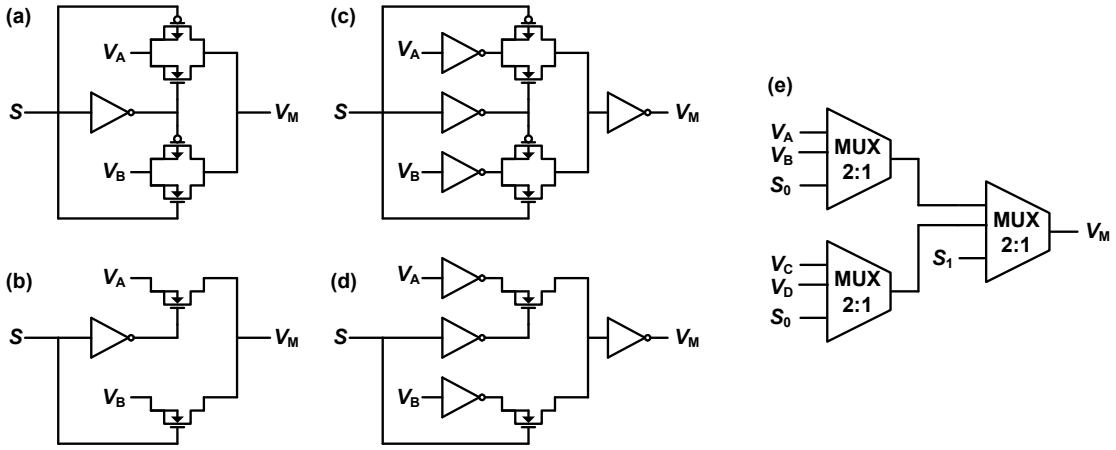

Figure 6.1 – Set of 2-to-1 multiplexer cores designed and included on chip: (a) analog transmission gate multiplexer, (b) analog pass transistor multiplexer, (c) digital transmission gate multiplexer, (d) digital pass transistor multiplexer. (e) Tree structure of the 4-to-1 multiplexer.

Corner	Width	Length
SS	120 nm	40 nm
SL	120 nm	0.4 µm
LS	1.2 µm	40 nm
LL	1.2 µm	0.4 µm

Table 6.2 – List of devices used for the design of custom multiplexers at 4.2 K.

6.3 Circuit design

4-to-1 multiplexers have been designed in a 40-nm process in different variants. Analog and digital versions, with CMOS and nMOS-only switches, with custom and standard cell transistor sizes, have been included, thus amounting to a total of 8 variants. The circuit topologies of the designed multiplexers are shown in Figure 6.1 (a)-(d).
Analog multiplexers are based on a transmission gate design, where the switch is obtained by connecting nMOS and pMOS in parallel, or pass transistor design in the case of nMOS-only switches. Transistors used in the design of custom multiplexers have been limited to specific sizes, representing the four corners in size (SS, SL, LS, LL), since they were previously measured and proved to be working at cryogenic temperature. The sizes are shown in Table 6.2.
Digital multiplexers have been derived from the corresponding analog versions by adding an inverter at the input and at the output. In this case, CMOS transmission-gate-based designs have been chosen to optimize performance in terms of area, power and delay, due to the reduced number of transistors with respect to standard NAND-based digital multiplexers.
2-to-1 multiplexers have been used as core cells and 3 such units have been connected in a tree structure to create 4-to-1 multiplexers, as shown in Figure 6.1 (e). This approach was selected to minimize the skew.
Simulations have been performed at 300 K with the standard design kit, while specific cryogenic device models have been used for simulations at 4.2 K [64].

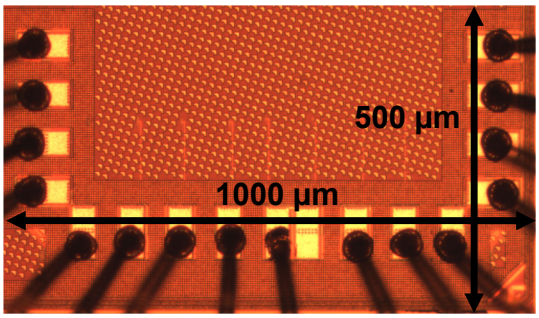

Figure 6.2 – Micrograph of the fabricated chip.

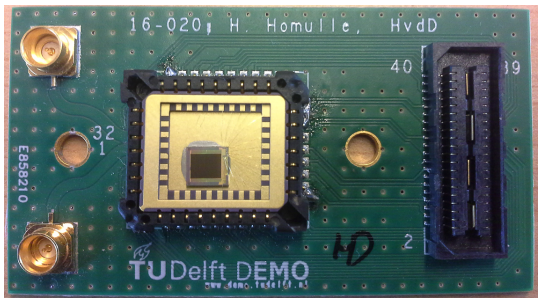

Figure 6.3 – Picture of the PCB used for cryogenic measurements.

The various designed multiplexers have been laid out in a 40-nm process and post-layout simulations have been realized, to verify the circuit performance with respect to the derived specifications.
All the designed multiplexers have been included on a single chip. Due to the reduced area of the active circuits, the chip floorplanning has been limited by the padring. In order to minimize the number of pads, the inputs (A, B, C, D), the control signals (S_0, S_1) and power signals (GND, VDD) have been shared among the different multiplexers, while a dedicated pad has been used for each output.

6.4 Test and measurement

The chip has been fabricated, then it has been glued and bonded to a ceramic package, which was then inserted in a PCB, already proven to be working at cryogenic temperature. A micrograph of the fabricated chip and a picture of the PCB are shown in Figure 6.2 and Figure 6.3 respectively.
Finally, a custom-made connector has been realized to interface the PCB with the dipstick to be used for immersion in the liquid helium dewar. This specific setup formed by package, PCB and connector could be used with very minor modifications also for 100 mK measurements in a dilution fridge.
A preliminary set of measurements has been performed to verify the circuit functionality at room temperature using the same setup as for the cryogenic tests, requiring the dipstick. Two arbitrary waveform generators (Tektronix 5014C and Rigol DG4202) have been used to generate the 4 sinusoidal/square wave inputs (A, B, C, D) at different frequencies and the 2 square wave control signals (S_0, S_1), while an oscilloscope (Rohde & Schwarz RTO 1044) has been used to inspect the output signals.
Subsequently, cryogenic measurements at 4.2 K have been performed in the liquid helium bath.
Both analog and digital multiplexers show correct functionality, with the proper selection of the input signal based on the controls. The measured signals from the analog transmission-gate custom-sized multiplexer at 4.2 K are shown in Figure 6.4. In this case, a maximum frequency of 4 kHz and an amplitude of 100 mV have been used for the input signals. The test value for the switching frequency was chosen to evaluate the performance of the multiplexers in a context similar to the quantum-classical matrix presented in Chapter 5,

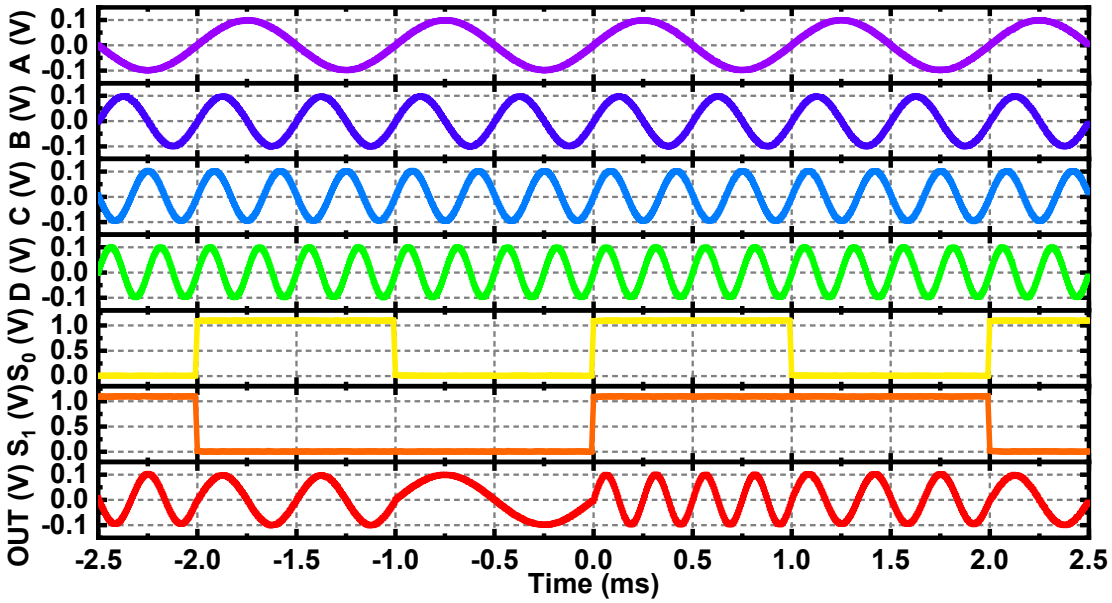

Figure 6.4 – Measured low frequency signals for the analog transmission-gate custom-sized 4-to-1 multiplexer at 4.2 K.

where sequential switching does not occur at frequencies higher than 1 kHz.
The output swing for the selected signal shows almost no reduction, while the leakage of the non-selected signals is below the maximum oscilloscope sensitivity (1 mV/division).
At cryogenic temperature, the immersion in liquid helium shows a small improvement in the output swing with respect to room temperature, while the frequency behavior is mostly unchanged.

6.5 Conclusion

Analog and digital cryogenic CMOS multiplexers have been designed, laid out and fabricated in a 40-nm process. The chip has been bonded to a package, which has been inserted in a PCB designed for cryogenic measurement, useful both in a dipstick setup and in a dilution fridge.
The set of measurements performed at room temperature and cryogenic temperature demonstrate the circuit functionality, both for analog and digital multiplexers, with a slightly improved output swing and frequency performance at 4.2 K with respect to 300 K.
The proposed multiplexers could be used at 1-4 K or possibly lower temperatures for the time-multiplexing of low-frequency qubit signals, either in readout or in control, or they could be useful in qubit arrays requiring few DC voltages per component, by holding the programmed voltage with a high retention time. Moreover, they have posed the basis for the realization of the time-multiplexing part of the quantum-classical matrix presented in Chapter 5.

7 A cryogenic CMOS radio-frequency circulator

The work presented in this chapter has been published in the papers:

[105] **A. Ruffino**, Y. Peng, F. Sebastiano, M. Babaie, and E. Charbon, "A 6.5-GHz Cryogenic All-Pass Filter Circulator in 40-nm CMOS for Quantum Computing Applications," *2019 IEEE Radio-Frequency Integrated Circuits Symposium (RFIC)*, Boston, June 2019;

[124] **A. Ruffino**, Y. Peng, F. Sebastiano, M. Babaie and E. Charbon, "A Wideband Low-Power Cryogenic CMOS Circulator for Quantum Applications," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 55, no. 5, pp. 1224-1238, May 2020.

In this work, I conceived the circuit and designed the chip, I performed the measurements, analyzed the data and wrote both manuscripts.

7.1 Introduction

Cryogenic circulators are widely used components in qubit systems [126, 20], in particular in dispersive readout setups, as described in Chapter 1. Circulators allow to decouple incident and reflected waves and are therefore a fundamental element in a gate-based reflectometry platform, as the one described in Chapter 5 and across this thesis.
However, currently, they are realized by bulky discrete ferrite devices [125] that prevent integration of the complete system. Compact Hall effect circulators have been demonstrated [127, 128], but they still employ magnetic fields. Hence, a non-magnetic cryogenic integrated circuit implementation of a circulator would be a significant step towards overall system scalability.
Integrated non-magnetic circulators operating at room temperature have recently been proposed [129, 130, 131, 132, 133, 134, 135] in CMOS technology in the field of full-duplex radios. Such circulators exploit Linear Periodic Time-Variant (LPTV) circuit operation to create non-reciprocity. Such technique resulted in a variety of implementations targeting shared-antenna interfaces for different communication standards, at frequencies below 1 GHz [129, 130, 133, 134], at 25 GHz [131, 132], and at 60 GHz [135].

	Specifications	Ferrite circulators [125]
Working temperature	0.02-4 K	0.02-300 K
Center frequency	6.5 GHz	6 GHz*
Bandwidth	2 GHz	4 GHz*
Insertion loss	< 1 dB	0.4 dB*
Isolation	18 dB	18 dB*
Noise temperature	< 1 K	7 K*
Area	$< 5 \times 5$ mm^2	35×45 mm^2
Power consumption	< 2 mW	0

*Reported data are at 77 K.

Table 7.1 – Design specifications of cryogenic circulators for quantum computing [124].

However, the design requirements of such implementations and the circuit techniques proposed so far for CMOS circulators for full-duplex are not well suited to the needs of circulators for qubit readout. The frequency of interest for cryogenic circulators for quantum applications is in the 5-8 GHz range. This is the band where most superconducting qubit frequencies lie [19] and it can also be interesting for spin qubits, as shown in Chapter 5, for integrated gate-based radio-frequency reflectometry [117] and spin-photon coupling experiments [118, 119], if the qubit readout frequency is increased, since compact integrated *LC* resonators can be designed at this frequency, so that currently employed directional couplers [15] can be replaced by RF circulators. Moreover, full-duplex circulators have shown a trend for high power handling [133, 134] due to transmitter requirements, while circulators for quantum computing are inherently small signal circulators only.
Active CMOS circulators have been explored in the frequency of interest [136, 137], however their noise performance has been shown to be insufficient.
Circulators for qubit readout are currently implemented by ferrite circulators [125], whose performance, indicated in Table 7.1, sets the ideal design requirements. However, in order to address miniaturization with an integrated circuit realization, some design compromises need to be made. Circulators for qubits require cryogenic operation, as they are commonly placed at temperatures between 0.02-4 K inside dilution fridges. This imposes very stringent requirements on *power consumption*, so as to meet the limited cooling power budgets of the cryostats. At the base temperature, the maximum cooling power is in the order of 10 µW, which is currently out of reach for integrated circulator solutions. If the circulator is operated at higher temperatures (1-4 K), at the cost of higher noise, the power budget can be set to 2 mW [108, 109], especially if the circulator is shared among multiple qubits. Cryogenic circulators must also have a *small area*, since they will ultimately need to be integrated into a compact, *scalable* integrated circuit controller. Therefore a maximum design target of few mm by few mm is set. The operational frequency of the circulator should be in the 6.5 GHz band [19]. Moreover, scalability calls for multiplexing techniques, since large area and power savings can be obtained by sharing the same electronics for multiple qubit channels, so frequency-encoded readout, such as frequency multiplexing, is advisable, thus requiring *bandwidth maximization*. If a 10 MHz bandwidth is set for each qubit, with a 10 MHz spacing, then one could multiplex 100 qubits in a 2 GHz circulator bandwidth, in line with the size of currently available quantum processors. Finally, meeting the performance of passive discrete circulators in terms of insertion loss (and noise) is

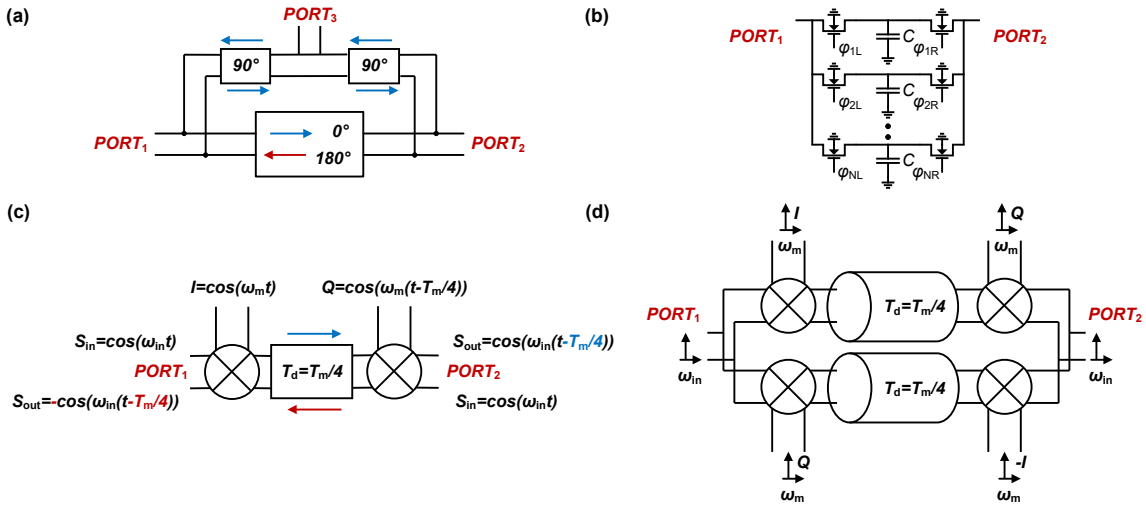

Figure 7.1 – Block diagram of (a) staggered-commutation circulators, showing (b) the N-path filter implementation of the non-reciprocal branch, (c) the single branch and (d) the I/Q double branch implementation of the broadband gyrator.

quite challenging in an integrated circuit, so the target insertion loss should be smaller than 1 dB, and isolation should be at least 18 dB. The insertion loss specification converts to a noise-equivalent temperature specification of less than 1 K. If scalability is the main requirement, then area, power consumption and bandwidth become high priority design targets. The presented design specifications are summarized in Table 7.1.
In order to address these requirements, this chapter presents a detailed discussion of the first integrated cryo-CMOS circulator [105, 124], based on a proposed architecture exploiting all-pass filters, targeting low power and wideband operation for quantum computing applications. This work represents a proof-of-concept of cryogenic integrated CMOS circulators, it explores the implications of an integrated solution, and as such, it is only a first step towards the full replacement of current setups. In the following sections, the theory, the design, the implementation, and the characterization of the proposed cryo-CMOS circulator are explained.

7.2 Wideband low-power staggered commutation circulators

Integrated CMOS circulators have been recently proposed by exploiting time-varying circuits to break Lorentz reciprocity, thus realizing staggered commutation [138]. From a top-level perspective, as shown in Figure 7.1 (a), they have been realized with a loop, composed by two reciprocal branches, providing 90° phase shift in either direction, and a non-reciprocal branch, causing a 0°/180° phase shift, depending on the signal direction. In this way, constructive interference (360°) is achieved in one direction of circulation, and destructive interference (180°) is obtained in the opposite direction.
Two families of circuits have been built on such block diagram, depending on the implementation of the different branches: the N-path filter family [129, 130] and the broadband gyrator family [131, 132, 133, 134, 135]. Correspondingly, the LPTV section has been

implemented either by an N-path filter for Global System for Mobile communications (GSM) band below 1 GHz [129, 130], or by a gyrator using a switched transmission line for K-band at 25 GHz [131, 132], or a switched band-pass filter at 60 GHz [135].

7.2.1 *N*-path filter circulators

In the N-path filter approach, the reciprocal branches are realized as CLC low-pass filter T-sections, while the non-reciprocal branch incorporates a switched capacitor filter, namely a two-port N-path filter, shown in Figure 7.1 (b), where the two sets of switches are controlled by low duty cycle non-overlapping phase-shifted clocks. Such phase shift can introduce non-reciprocity in the filter phase response [139], which is inherited by the branch. When the phase shift is set to 90°, this creates a 90°/−90° non-reciprocity. When a reciprocal 90° branch is added, the required non-reciprocal 0°/180° branch is formed. Such an approach has some disadvantages: the clock frequency needs to be the same as the input frequency, so high-frequency circulators would require high-frequency clocks, causing large power consumption; moreover, the bandwidth of the circulator's non-reciprocal response is limited to the sharp band-pass response of N-path filters.

7.2.2 Broadband gyrator circulators

The broadband gyrator approach implements the non-reciprocal branch by employing a passive filter between two sets of I/Q mixers. A differential implementation of such a structure is shown in Figure 7.1 (c). When there is an incoming signal at frequency ω_{in}, the mixers commute at clock frequency ω_{m}, with $\omega_{\mathrm{m}} < \omega_{\mathrm{in}}$. The internal filter is producing a phase shift, or equivalently, a time-delay T_{d}, which is equal to $T_{\mathrm{m}}/4$, where $T_{\mathrm{m}} = 2\pi/\omega_{\mathrm{m}}$ is the clock period. In the forward direction, this gives a transmission with a delay of $T_{\mathrm{m}}/4$, while in the reverse direction the system yields a delay of $T_{\mathrm{m}}/4$ and a sign flip. The periodical time variance caused by mixers results in non-reciprocal behavior. Under such assumptions, the S-parameters of the two-port gyrator can be represented by [132]:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & -e^{-\mathrm{j}\frac{\pi}{2}\left(\frac{\omega_{\mathrm{in}}}{\omega_{\mathrm{m}}}\right)} \\ +e^{-\mathrm{j}\frac{\pi}{2}\left(\frac{\omega_{\mathrm{in}}}{\omega_{\mathrm{m}}}\right)} & 0 \end{bmatrix}. \tag{7.1}$$

This gives lossless non-reciprocal transmission at odd multiples of the clock frequency $\omega_{\mathrm{in}} = (2n-1)\,\omega_{\mathrm{m}}$ [132]. Such property is ideally obtained over substantial bandwidth, limited only by the internal filter bandwidth.
This structure suffers, however, from S-parameter degradation in the presence of duty cycle mismatch. In order to mitigate this problem, the architecture can be modified to include a parallel quadrature path similar to the path presented above, where clock signals are shifted by 90° [132]. Such a double branch implementation, shown in Figure 7.1 (d), can achieve 90° or −90° phase shift according to the signal direction at odd multiples of the clock frequency. So, when it is embedded into an additional reciprocal 45° section on each side, it can perform the required 0°/180° gyrator function.

In recent implementations [131, 132, 133, 134], the internal filter has been realized as multi-section lumped-element Bragg-limited $\lambda/4$ transmission line at the clock frequency, to achieve the required $T_m/4$ time delay. The clock frequency was chosen to be $\omega_m = \omega_{in}/3$. Also the other filters in the reciprocal branches have been implemented with artificial transmission lines, to realize a circulator at 25 GHz. Another circulator implementation at 60 GHz [135] has employed some extra inductors at the input and output of each I/Q mixer to tune out the capacitance of the mixer switches and mitigate the trade-off between a small switch R_{ON} and additional unwanted parasitic capacitance C_p. However, such an approach still uses a multi-section transmission line to realize the required delay.

7.2.3 All-pass filter circulators

The presented solutions cannot be applied directly to the design of a low-power wideband circulator in the frequency of interest. The N-path filter approach would require low duty cycle non-overlapping phases at the 6.5 GHz operating frequency ω_{in}, which would require extremely power-hungry clock drivers. The switched transmission line approach, instead, would impose a $\lambda/4$ transmission line at the clock frequency. A reduction of clock frequency, to minimize power, would result in a too large and lossy transmission line implementation at the frequency of interest.
Indeed, in order to reduce the circulator's power consumption, the clock frequency ω_m needs to be reduced, since the switching of mixer capacitance at the clock rate is the primary source of power dissipation. If ω_m is reduced, the equivalent time delay required by the filter becomes larger. In a transmission line, this would require a longer line, which could be realized only with more equivalent LC sections, causing more area and insertion loss, or reduced bandwidth, if a smaller number of sections is used.
In the artificial transmission line approach, shown in a differential implementation in Figure 7.2 (a), each lumped element section provides a unit delay $t_d = \sqrt{L \cdot C}$. So, multiple sections are required to achieve the required delay $T_d = T_m/4$. However, the filter behaves like a transmission line only within its bandwidth, that is until half of the Bragg frequency, $\omega_B = \frac{2}{\sqrt{L \cdot C}}$, as shown in Figure 7.2 (b). By setting such a limit for ω_{in}, one can obtain:

$$t_d = \sqrt{L \cdot C} = \frac{1}{\omega_{in}}. \tag{7.2}$$

This can, in turn, determine the number of sections required to achieve the desired time delay:

$$n = \frac{T_d}{t_d} = \frac{\pi}{2} \cdot \left(\frac{\omega_{in}}{\omega_m}\right). \tag{7.3}$$

If one considers the values of inductors and capacitors required to implement the artificial unit section, namely $L = \frac{Z_0}{\omega_{in}}$ and $C = \frac{1}{Z_0 \cdot \omega_{in}}$, where Z_0 is the characteristic impedance, one can also calculate the total inductance required as:

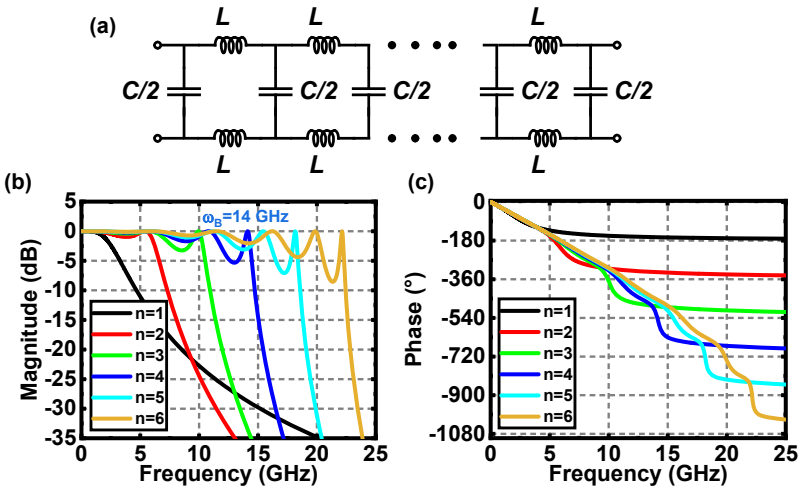

Figure 7.2 – Multi-section artificial transmission line (a) schematic, (b) transfer function magnitude and (c) phase for different number of sections. The lines have been designed to all achieve the same time delay $T_\mathrm{d} = T_\mathrm{m}/4$ for $\omega_\mathrm{in}/\omega_\mathrm{m} = 3$ and input frequency $f_\mathrm{in} = 6.5\,\mathrm{GHz}$.

$$L_\mathrm{t} = n \cdot L = \frac{\pi}{2} \cdot \left(\frac{\omega_\mathrm{in}}{\omega_\mathrm{m}}\right) \cdot \frac{Z_0}{\omega_\mathrm{in}}. \tag{7.4}$$

As one can see, the lower the clock frequency ω_m for a given input frequency ω_in, the larger the total inductance required. This demonstrates the undesirable trade-off between reduction of the dynamic power consumption and optimization of area/insertion loss.
Moreover, the phase relationship for an n-section line is given by the following equation, as shown in Figure 7.2 (c):

$$\theta(\omega) = -n \cdot 2 \cdot \arcsin\left(\frac{\omega}{\omega_\mathrm{B}}\right). \tag{7.5}$$

Consequently, the group delay can be calculated as:

$$\tau(\omega) = -\frac{d\theta(\omega)}{d\omega} = \frac{2n/\omega_\mathrm{B}}{\sqrt{1 - \left(\frac{\omega}{\omega_\mathrm{B}}\right)^2}}. \tag{7.6}$$

This analysis applies to both the transmission line implementation [132] and the case where the transmission line is embedded into tuned resonators [135], since the properties of the multi-section lumped-element artificial line still apply.
In order to mitigate these problems, an alternative architecture needs to be used.
To better capture the mechanisms of the non-reciprocal branch, one should analyze it in the frequency domain. To do so, the double branch architecture is generalized to include mixer clocks shifted by a phase shift ϕ, as shown in Figure 7.3. In this case, a signal

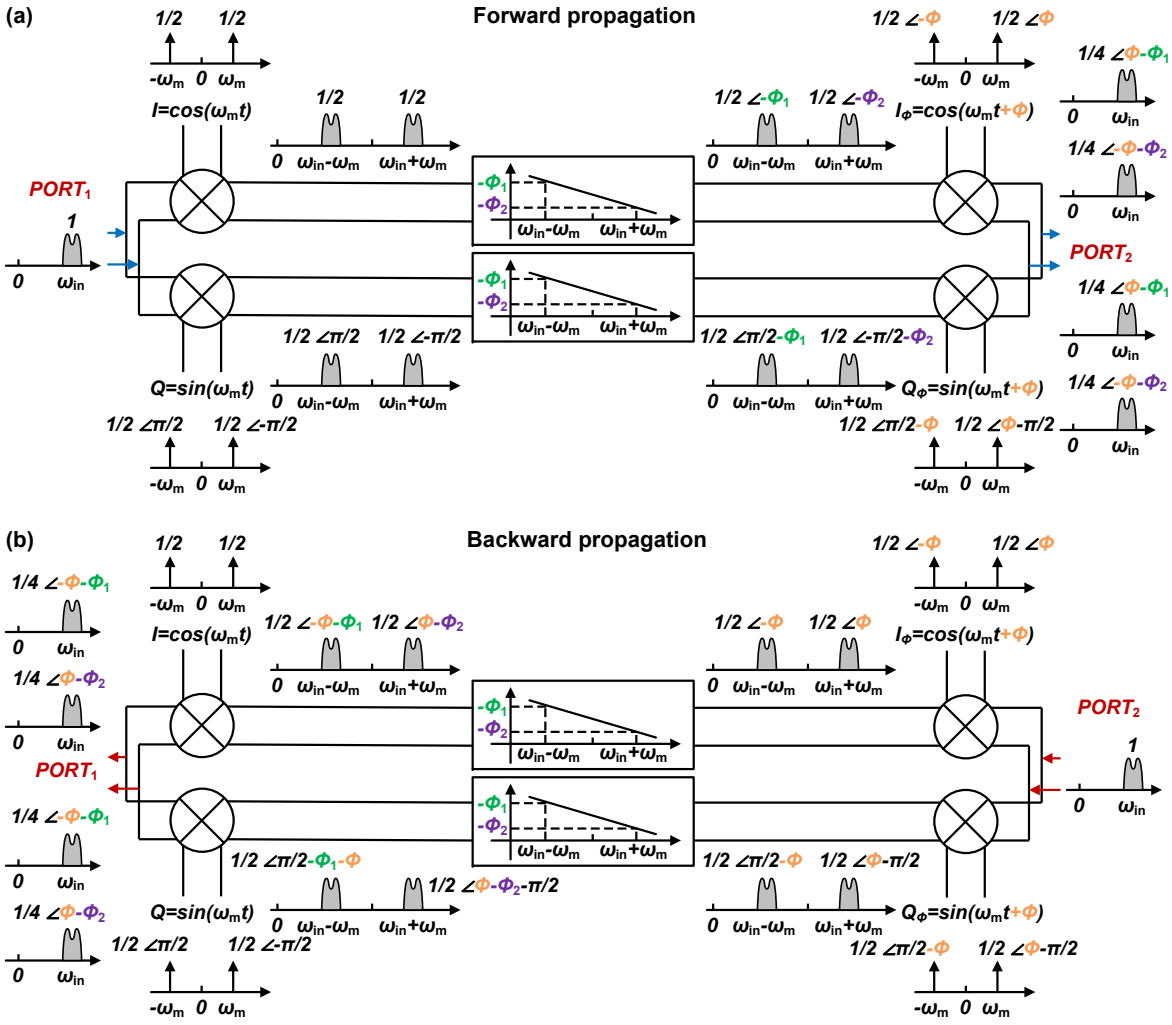

Figure 7.3 – Phase-frequency domain analysis of (a) forward propagation and (b) backward propagation in the non-reciprocal branch of the all-pass filter circulator.

traveling at frequency ω_{in} is mixed in the two parallel paths with I/Q clocks at frequency ω_m, generating two mixing products at $\omega_L = \omega_{in} - \omega_m$ and $\omega_H = \omega_{in} + \omega_m$ in each of the two branches, with different phase shifts due to the I/Q mixing. In each branch, difference and sum-frequency components undergo additional phase shifts $\phi_1 = (\omega_{in} - \omega_m)\tau$ and $\phi_2 = (\omega_{in} + \omega_m)\tau$ respectively, caused by the internal filter. Finally, the two frequency components in the I and Q paths remix again at frequency ω_m, but in this case with ϕ-shifted I/Q polarity, thus generating mixing products at $\omega_{in} - 2\omega_m$, ω_{in} and $\omega_{in} + 2\omega_m$. The two components at $\omega_{in} - 2\omega_m$ and $\omega_{in} + 2\omega_m$ are out of phase with each other, and therefore they cancel out. The four components at ω_{in} can instead add up constructively if one imposes that they all have the same phase, meaning $\phi - \phi_1 = -\phi - \phi_2$ or $\phi_1 - \phi_2 = 2\phi$. In this case, lossless transmission with a phase shift $\phi - \phi_1$ can be obtained. In the reverse direction, the same analysis can show that, if $-\phi - \phi_1 = \phi - \phi_2$ or $\phi_1 - \phi_2 = -2\phi$, lossless transmission can be obtained with a different phase shift $-\phi - \phi_1$. Under such assumptions, the resulting S-parameters are:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & +e^{-\mathrm{j}(-\phi-\phi_1)} \\ +e^{-\mathrm{j}(\phi-\phi_1)} & 0 \end{bmatrix}. \tag{7.7}$$

The only possibility for both conditions $\phi_1 - \phi_2 = 2\phi$ and $\phi_1 - \phi_2 = -2\phi$ to be true at the same time is that $2\phi = -\pi$. Under the presented analysis, the phase domain conditions for non-reciprocal operation can be then expressed as:

$$\begin{cases} \phi = -\pi/2 \\ \phi_1 - \phi_2 = 2\phi = -\pi \\ \phi_1 = \pi/2. \end{cases} \tag{7.8}$$

These equations are the fundamental design equations of the circulator.
Now, in order to address the requirements of circulator design for quantum computing (i.e., 5-8 GHz band, low power consumption, and small area), the parameters in these equations, and consequently the circuit architecture, need to be appropriately chosen.
In order to mitigate the adverse effect of duty cycle mismatch, the phase shift between clock signals has to be 90°, thus yielding a differential I/Q clock scheme; this is represented by the first design condition in Equation (7.8).
To achieve a power target of 2 mW, operation with a clock frequency around 1 GHz is chosen, therefore, given the band of interest centered around 6.5 GHz, a clock frequency $\omega_\mathrm{m} = \omega_\mathrm{in}/5$ is selected, with a resulting modulation index $m = \omega_\mathrm{in}/\omega_\mathrm{m}$ equal to 5.
The core functionality of the circulator is then described by the second condition in Equation (7.8), which establishes that the phase shifts of the difference-frequency ω_L and the sum-frequency ω_H need to be 180° apart. If ω_m is reduced to minimize power consumption, then the two components ω_L and ω_H become closer to each other, requiring the internal filter in the non-reciprocal branch to be highly dispersive.
Under these assumptions, artificial transmission lines would require too many first-order sections to provide the required phase shifts at closely spaced frequencies ω_L and ω_H, falling into the usual trade-off with loss.
For this reason, the use of a second-order filter is proposed, and in particular an all-pass filter, capable of providing phase shift ideally without affecting the amplitude. A filter that can satisfy such conditions at the required frequency is a bridged-T *LC* all-pass filter, of which a differential implementation is shown in Figure 7.4 (a).
The values of the different components for the single-ended case are [140]:

$$L_1 = \frac{2Z_0}{\omega_0 Q} \tag{7.9}$$

$$L_2 = \frac{QZ_0}{2\omega_0} \tag{7.10}$$

$$C_1 = \frac{Q}{\omega_0 Z_0} \tag{7.11}$$

$$C_2 = \frac{2Q}{\omega_0 (Q^2 - 1) Z_0}, \tag{7.12}$$

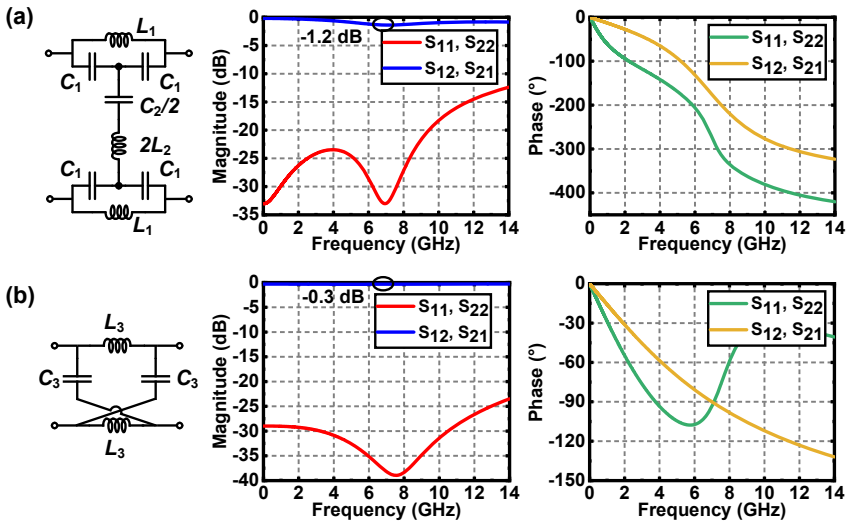

Figure 7.4 – Schematic and transfer function post-layout simulation at 300 K of (a) a second-order bridged-T all-pass filter and (b) a first-order lattice all-pass filter.

where Z_0 is the characteristic impedance of the filter, ω_0 is its center frequency and Q is its quality factor. The transfer function of such filter can be expressed as:

$$H(s) = \frac{s^2 - \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}. \tag{7.13}$$

Consequently, the magnitude of the filter transfer function is:

$$|H(\omega)| = \frac{\sqrt{(\omega_0^2 - \omega^2)^2 + \frac{\omega_0^2\omega^2}{Q^2}}}{\sqrt{(\omega_0^2 - \omega^2)^2 + \frac{\omega_0^2\omega^2}{Q^2}}} = 1. \tag{7.14}$$

The phase response of this filter can instead be expressed as:

$$\angle H(\omega) = -2\arctan\left(\frac{\omega \cdot \omega_0}{Q \cdot (\omega_0^2 - \omega^2)}\right). \tag{7.15}$$

Consequently, the group delay of the second-order all-pass filter is calculated as:

$$\tau(\omega) = -\frac{d\angle H(\omega)}{d\omega} = \frac{2Q\omega_0(\omega_0^2 + \omega^2)}{Q^2(\omega_0^2 - \omega^2)^2 + \omega_0^2\omega^2}. \tag{7.16}$$

The center frequency of the circulator ω_{in} can be placed at the center of the all-pass filter ω_0, where the phase shift is 180°, while the two components ω_L and ω_H can be placed where the phase shift of the filter is 90° and 270°, respectively. Such a second-order filter allows to satisfy the fundamental non-reciprocity condition at frequencies closer to the center frequency, due to the steep phase response, as required by the choice $\omega_m = \omega_{in}/5$. The two phase shifts at the difference and sum-frequency can be expressed as:

$$\phi_1|_{\omega=\omega_L=\omega_0-\omega_m} = -2\arctan\left(\frac{1}{Q}\frac{\omega_0}{\omega_m}\frac{\omega_0-\omega_m}{2\omega_0-\omega_m}\right) \tag{7.17}$$

$$\phi_2|_{\omega=\omega_H=\omega_0+\omega_m} = +2\arctan\left(\frac{1}{Q}\frac{\omega_0}{\omega_m}\frac{\omega_0+\omega_m}{2\omega_0+\omega_m}\right). \tag{7.18}$$

Now, using the assumption that $\omega_0 \gg \omega_m$ one can express the difference between the two phase shifts as follows:

$$\phi_2 - \phi_1 = 4\arctan\left(\frac{1}{Q}\cdot\frac{\omega_0}{2\omega_m}\right). \tag{7.19}$$

By imposing $\phi_2 - \phi_1 = \pi$, one can express the required Q as:

$$Q = \frac{1}{2}\left(\frac{\omega_0}{\omega_m}\right). \tag{7.20}$$

One can then calculate the total inductance required for the all-pass filter implementation as follows:

$$L_t = L_1 + L_2 = \frac{Z_0}{\omega_{in}}\cdot\left(\frac{2}{Q}+\frac{Q}{2}\right). \tag{7.21}$$

If one uses the expression found for Q in Equation (7.20), one can write:

$$L_t = \frac{Z_0}{\omega_{in}}\cdot\left(4\frac{\omega_m}{\omega_{in}}+\frac{1}{4}\frac{\omega_{in}}{\omega_m}\right). \tag{7.22}$$

This expression is valid for a single I or Q branch. The transmission line architecture can operate with a single path (I or Q), as shown in [133, 134, 135], since all the mixing harmonics created by the square wave clock are passed within its bandwidth. In principle, also an all-pass filter can operate with a single path, however this increases the sensitivity of insertion loss to duty cycle mismatch [132] in the I/Q clock generation. This can be mitigated by adding tunability to the phase of the I/Q clock, but at the cost of increased

power consumption.
If Equation (7.22) is compared to Equation (7.4) obtained in the case of the transmission line implementation, the total inductance values for $\omega_{in}/\omega_m = 5$ are respectively 2.05 Z_0/ω_{in} and 7.85 Z_0/ω_{in} for a single branch implementation in both cases, while such values are doubled for an I/Q double path realization. This shows that the inductance required by the all-pass filter approach is always smaller, even comparing the presented double branch I/Q all-pass filter with a single path transmission line implementation.
Although this approach was conceived to reduce clock frequency, addressing power reduction, the first requirement set for cryogenic circulators, at the same time it benefits compactness, the second requirement. Indeed, a smaller number of smaller passives (in particular inductors) is used with respect to a multi-section transmission-line approach (with or without band-pass filter). This favors insertion loss and noise figure as well, since fewer inductors are in series with the signal path.
Finally, thanks to the phase choices in the second-order all-pass filter, one can choose the non-reciprocal branch insertion phase to be 90°, as described by the third design condition in Equation (7.8). This allows eliminating the need for additional 45° sections as used in [131, 132]. This again reduces the number of passive components, improving compactness and insertion loss of the circulator.
To close the circulator loop, it is proposed to implement the reciprocal branches with *LC* all-pass filters as well, but in this case first-order lattice filters are enough for the required 90° phase shift. The schematic of the filter is shown in Figure 7.4 (b) and the values of the components are:

$$L_3 = \frac{Z_0}{\omega_0} \tag{7.23}$$

$$C_3 = \frac{1}{\omega_0 Z_0}. \tag{7.24}$$

The resulting transfer function can be expressed as:

$$H(s) = \frac{\omega_0 - s}{\omega_0 + s}. \tag{7.25}$$

The magnitude of the transfer function can be demonstrated to be constantly equal to 1 also in this case:

$$|H(\omega)| = \frac{\sqrt{\omega_0^2 + \omega^2}}{\sqrt{\omega_0^2 + \omega^2}} = 1. \tag{7.26}$$

The phase can instead be expressed as:

$$\angle H(\omega) = -2\arctan\left(\frac{\omega}{\omega_0}\right). \tag{7.27}$$

This completes the architecture of the proposed circulator.
Now the last property of the circulator, the bandwidth, can be discussed, since it arises from the interaction in the phase domain between the phase relationships of the non-reciprocal branch and the two reciprocal branches.
The use of the all-pass filter approach shows to have benefits on bandwidth as well. The second-order all-pass filter can provide phase shift in all frequency regions, apart from the two plateaux, where it flattens out to 0° and 360°. The phase response of such filter is highly linear around its center frequency, which means that the required phase relationship set by the second design condition in Equation (7.8) can be maintained over a large frequency band. As the input frequency deviates from the designed center of the all-pass filter, the components ω_L and ω_H move accordingly and the phase relationship is maintained as long as they both are in the linear region, until one of the two falls into the phase plateaux. This contributes to set the bandwidth of the circulator.
While this happens in the phase domain, there is ideally no filtering in the magnitude domain. This is a significant advantage with respect to high-order multi-section low-pass or band-pass filters, in which the phase relationship needs to be maintained while inside the filter bandwidth, to avoid magnitude attenuation of the frequency components. For such filters, one must extend the bandwidth to achieve phase shift at frequencies far from the cut-off.
If one considers the phase response of the second-order all-pass filter expressed in Equation (7.15), it is possible to calculate the phase shifts ϕ_1, obtained when $\omega = \omega_L = \omega_{in} - \omega_m$, and ϕ_2, obtained when $\omega = \omega_H = \omega_{in} + \omega_m$, for variable ω_{in}. Their difference $\phi_2 - \phi_1$ determines how the second design condition in Equation (7.8) is satisfied across variable input frequency, and when this diverts from the designed 180°, non-reciprocity is affected and bandwidth is limited. This phase difference is equal to 180° at the center of the all-pass filter, and is always smaller than that, so it varies non-monotonically around it, showing a plateau (with zero derivative).
If one then considers the phase response of the first order all-pass filter ϕ_3 expressed in Equation (7.27) obtained when $\omega = \omega_{in}$ for variable input frequency, this phase is equal to 90° at the center of the all-pass filter ω_0 and varies monotonically around it.
The overall condition for circulation is set by $\phi_2 - \phi_1 = 180°$ in the non-reciprocal branch and $\phi_3 = 90°$ in the two reciprocal branches, so one can combine them into one equation, namely $\phi_{tot} = \phi_2 - \phi_1 - 2\phi_3 = 0$. This quantity is plotted in Figure 7.5 (a).
In the case of an artificial transmission line implementation, the phase shifts ϕ_1 and ϕ_2 of the non-reciprocal branch, the phase shift ϕ_3 of the two $\lambda/4$ reciprocal branches and the phase shift ϕ_4 of the additional $\lambda/8$ sections can all be expressed by Equation (7.5). They vary monotonically around the center frequency ω_0.
The overall condition for circulation in this case is $\phi_2 - \phi_1 = 180°$ in the non-reciprocal branch, $\phi_3 = 90°$ in the two reciprocal branches and $\phi_4 = 45°$, so one can combine them into one equation, namely $\phi_{tot} = \phi_2 - \phi_1 - 2\phi_3 - 2\phi_4 + 90° = 0$. This quantity is plotted in Figure 7.5 (a) for both ideal and artificial transmission lines, designed to achieve the same circulator function for the same ω_0 and ω_m as the designed all-pass filter architecture.

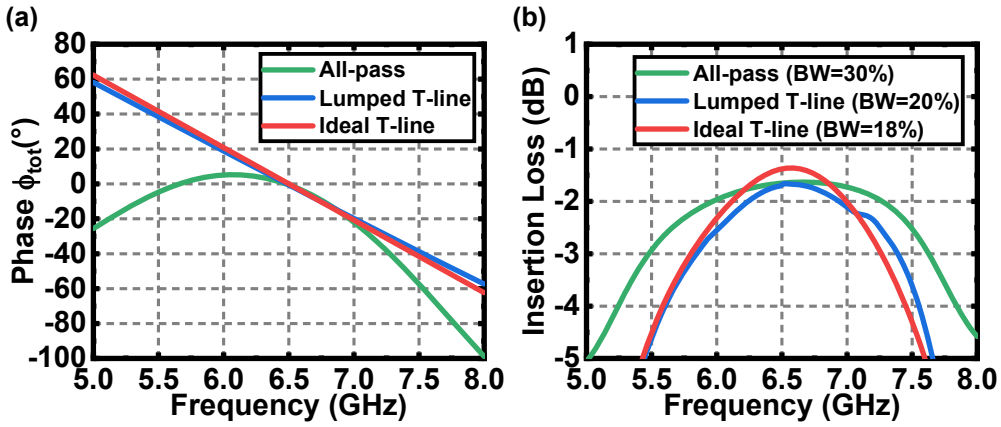

Figure 7.5 – (a) Comparison between the all-pass filter, the artificial transmission line and the ideal transmission line approach, for $\omega_{in}/\omega_m = 5$, in terms of overall constructive/destructive circulator phase relationship. (b) Simulated insertion loss and 1-dB bandwidth of an entire circulator constructed for each of the elements in the comparison using ideal mixers with $R_{ON}=10\,\Omega$.

As one can see, if an error of 20° is tolerated in the overall constructive/destructive circulator phase relationship, the bandwidth over which this condition is satisfied is extended for the all-pass filter approach with respect to the transmission line case.
The reason is that the non-monotonic deviating phase of the second-order all-pass filter in the non-reciprocal branch partially compensates for the deviation of phase in the two reciprocal branches. In the transmission line case, there is no compensation and actually deviations from the ideal value at the center of the circulator are enhanced both at low and high frequencies, thus reducing the bandwidth. This explains why the bandwidth of the circulator can be extended. If a complete circulator structure is simulated for each of the elements in the comparison, the resulting insertion loss 1-dB Band-Width (BW) is considerably larger for the all-pass filter implementation, as shown in Figure 7.5 (b).

7.3 Circuit design and implementation

The proposed circulator, shown in Figure 7.6, has been implemented in a 40-nm CMOS technology with ultra-thick top metal layer option. The overall architecture includes two reciprocal branches realized by first-order lattice *LC* all-pass filters, and a non-reciprocal branch with two parallel I/Q paths including a second-order bridged-T *LC* all-pass filter and passive mixers.
Inductors in the *LC* filters have been realized as multi-turn (3-4) spiral inductors with ultra-thick metal layer conductor and thick layer underpass. Capacitors have been realized as multi-finger interdigitated MoM capacitors. Inductors and capacitors have been designed to achieve the required phase shifts at the design frequency, according to the presented equations. Mixers have been implemented as differential nMOS-only passive mixers with aspect ratio $W_g/L_g = 50\,\mu m / 40\,nm$ in a deep n-well to isolate from substrate noise. MOSFETs have been optimized to trade-off R_{ON} resistance, causing additional insertion loss, since in series with the signal path, and parasitic capacitance C_p, which produces unwanted phase shifts in the signal. The design values for the final implementation are

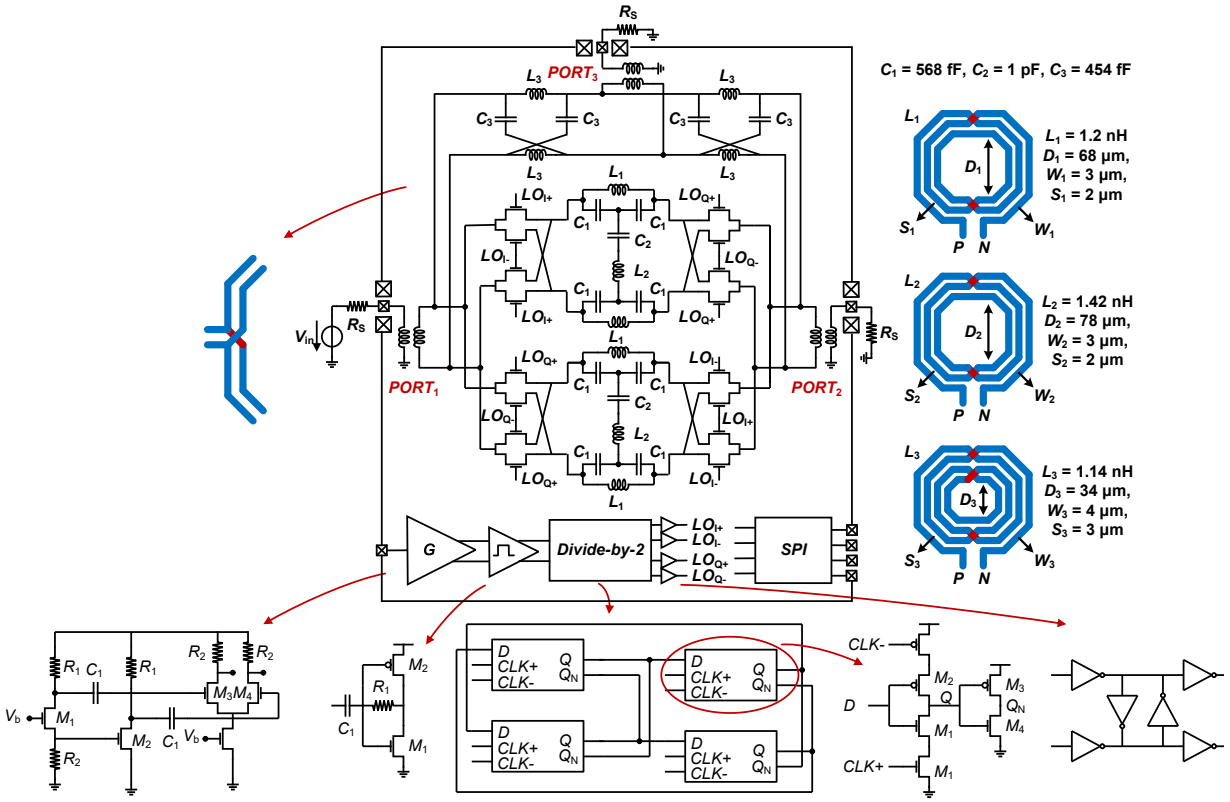

Figure 7.6 – Circuit schematic of the designed circulator, including the circulator core and details of the auxiliary structures.

$R_{ON} = 10\,\Omega$ and $C_p = 15\,fF$ at 300 K.
In the transmission line implementation [131, 132, 133, 134] (and with extra inductors in [135]), the parasitic capacitance C_p can be absorbed in the transmission line and reciprocal sections. However, with the proposed all-pass filter approach, the topology does not include shunt capacitors, so this feature cannot be exercised. Therefore, mixer parasitic capacitance and connections over non-negligible distance cause unwanted phase shifts in the reciprocal and non-reciprocal sections. The reciprocal parasitic phase shift is estimated from post-layout and electro-magnetic simulation to be in total 12° at 300 K. Such parasitic reciprocal and non-reciprocal phase shifts have been compensated for in their respective sections, with an empirical redesign of the first-order and second-order all-pass filters to embed this extra phase shift, by tuning the component values to achieve an ideal circulator function in the overall system. The transfer functions of the modified filters are then less close to ideal values, and therefore more sensitive to phase variations. The consequent trade-off is that the parasitic capacitance of mixers should be kept to a minimum, to make the compensation feasible. This amounts to reducing the size of the nMOS mixers, which in turn increases R_{ON} resistance. This has been mitigated by using low threshold voltage devices.
Moreover, in the final implementation, a T-to-π transformation has been applied to the capacitors C_1-C_2-C_1 in the second-order all-pass filter, to achieve smaller capacitance values and consequently, higher quality factors and better accuracy.

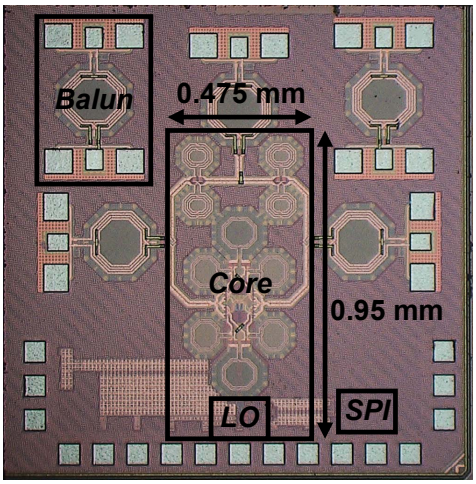

Figure 7.7 – Chip micrograph of the designed circulator, showing the circulator core, transformer baluns, clock generation path and auxiliary structures.

In order to realize connections between first-order and second-order all-pass filters over a non-negligible distance, microstrip edge-coupled differential lines in the topmost ultra-thick metal layer have been used. Cross-swapping has been used to obtain the same length for the two paths.
The system has been designed to be differential. Therefore transformer baluns have been included to convert the 50 Ω differential signal to 50 Ω single-ended for RF probing with GSG probes. A 50 Ω (tunable) on-chip termination resistor has been included at the secondary of the transformer for testing purposes, in particular for noise measurements at cryogenic temperature. Separate transformers have been included on-chip to de-embed their influence from the measurement results of the circulator. Auxiliary structures for SOLT calibration and de-embedding have been included on a separate chip.
The system has been designed for a target circulator center frequency ω_{in} of 6.5 GHz, with a clock signal $\omega_{\text{m}} = \omega_{\text{in}}/5$, yielding 1.3 GHz.
In order to generate the four required differential I/Q clock signals, an on-chip clock generation circuitry has been designed. A sinusoidal input at double frequency (2.6 GHz) is provided externally. An active Common Source (CS) Common Gate (CG) single-ended-to-differential amplifier generates a differential signal, which is then clipped to a square wave by further gain stages. This signal is fed into a C^2MOS latch based divider, which generates the four I/Q differential phases, and finally phase aligners and buffers drive the clock into the mixers. The devices used in the mixers and clock driver circuits are low threshold voltage, standard oxide nMOS/pMOS transistors with a nominal supply voltage of 1.1 V. The maximum tolerable gate-oxide voltage for such devices is 1.6 V. Therefore, the maximum safe operating region signal that the circulator can tolerate, to avoid oxide breakdown, is in the order of +14 dBm. This is well above the region where the circulator is going to be operated in the target application.
The local oscillator path and especially its input amplifier stages have been largely overdesigned to guarantee the circuit operation under large variations of circuit parameters, expected at cryogenic temperatures, therefore its power consumption has not been optimized.

Together with the analog and RF circuitry, a digital Serial-to-Parallel Interface (SPI) is included on chip, to control tunability in the amplifier biasing points and especially to tune the controllable port impedance during testing.
The chip micrograph of the fabricated circulator is shown in Figure 7.7. Its core area, thanks to the all-pass filter approach, occupies only 0.45 mm^2.

7.4 Cryogenic temperature design and modeling

The circulator has been designed for operation from room temperature to cryogenic temperature, where it is supposed to be used in the target application. Room temperature operation has been used as a benchmark for functionality, while performance targets have been set for cryogenic operation at 4.2 K.
As explained in Chapter 1 and Chapter 3, at cryogenic temperatures, active devices, such as MOSFETs, experience an increase in threshold voltage V_{th}, an increase in transconductance g_m and lower channel resistance. Therefore, for transistors used as switches, like those used in the nMOS passive mixers, one expects a reduction of R_{ON} resistance, hence an improvement in conversion loss. In transistors used in saturation as amplifiers, like those in the LO path, one expects reduced voltage headroom due to threshold voltage increase and larger gain for the same bias current. This justifies the large overdesign of the LO path, to guarantee operation under all conditions.
On the other hand, as explained in Chapter 4, passive devices, such as capacitors, inductors and transformers, increase their quality factor at cryogenic temperatures. Capacitor values increase slightly, while inductance is slightly decreased. The same quality factor increase happens to all high-frequency differential lines, which exhibit lower insertion loss at 4.2 K.
While predictive models exist for room temperature, there are no established models for cryogenic circuit design. For this reason, the measurement-based models for passives developed in Chapter 4 have been used for a first prediction of the circulator performance at 4.2 K (since the circuit is mostly passive).
The developed modified lumped-element models have been used for capacitors and inductors in the design kit, while the modified substrate for EM simulation has been used for custom-designed passives, like transformers, to predict their behavior at 4.2 K. For transistors, only a modified channel resistance has been included in the model, to capture the main effect of R_{ON} resistance reduction in the mixer switches. Finally, reduced metal resistance has been included in post-layout extraction for the ultra-thick top-metal layer only (used for all high-frequency lines).
Simulations have been carried out at 300 K with the standard design kit and S-parameter results are overlaid in Figure 7.8. Simulations have also been performed with the modified cryogenic models and substrate, to predict the performance of the passive circulator core at 4.2 K, and the S-parameter results are shown in Figure 7.9.
The circulator has been designed for operation at cryogenic temperature, however it could not be fully optimized, as the device models which have been established are still only partial. Active devices behavior, including parasitics and noise performance, are not captured in such models, so this still represents a further optimization margin with respect to a full simulation with PDK models available at room temperature.

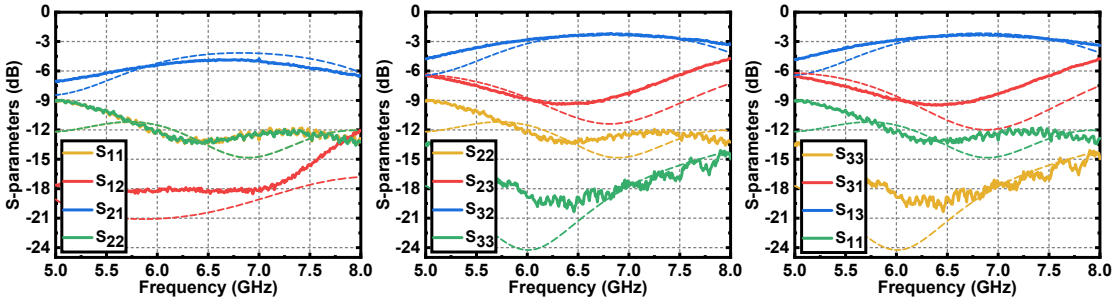

Figure 7.8 – Circulator *S*-parameter simulation (dashed line) and measurements (solid line) at 300 K.

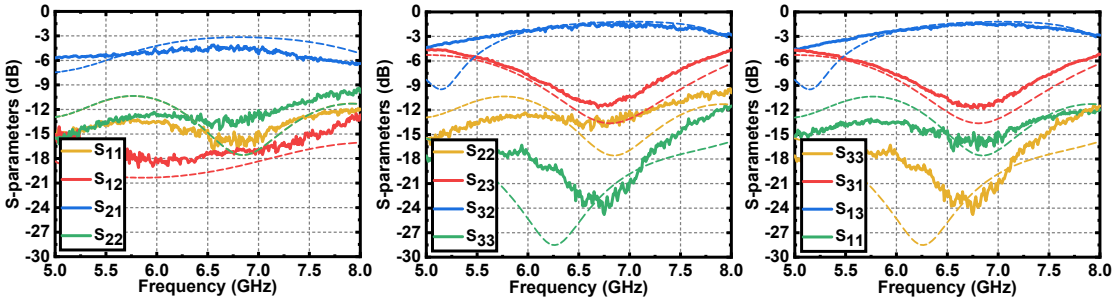

Figure 7.9 – Circulator *S*-parameter simulation (dashed line) and measurements (solid line) at 4.2 K.

7.5 Measurements

The fabricated circulator prototype has been bonded to a PCB for room temperature and cryogenic RF measurements in a probe station. The DC, analog low frequency and digital lines have been connected to the PCB with phosphor bronze lines for thermal isolation, while the GSG pads have been left exposed for RF probes.

7.5.1 DC measurements

DC measurements have been performed in the presence of an external 2.6 GHz sinusoid, to generate the required I/Q differential 1.3 GHz clock signals. The circulator core, including the on-chip frequency divider and the phase aligners with buffers driving the mixers, consumes 2.3 mA from 1.1 V power supply, thus resulting in 2.5 mW power dissipation at 300 K. The additional amplifiers and gain stages consume 9 mA, thus resulting in additional 9.9 mW power dissipation, for structures required by on-chip testing. The overall power consumption of the prototype chip at 300 K is 12.4 mW.
When the circuit is cooled down to 4.2 K under the same voltage biasing conditions, the circulator core consumes 1.9 mA, resulting in 2.1 mW power dissipation, while the auxiliary circuitry consumes 7.7 mA, contributing to an additional 8.4 mW power dissipation at cryogenic temperature.

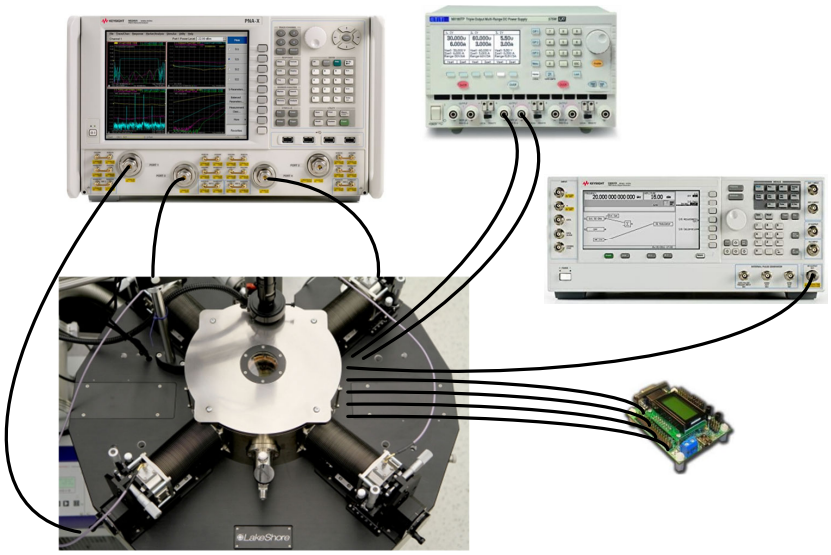

Figure 7.10 – Diagram of the test setup used for S-parameter measurements.

7.5.2 S-parameter measurements

The circulator S-parameters have been measured with RF probing in a Lake Shore CPX probe station. A Keysight N5245A PNA-X has been used as vector network analyzer to measure S-parameters, Aim-TTi MX100TP power supplies for biasing, and a Keysight PSG E8267D signal generator was employed to provide the external LO signal. The complete measurement setup is shown in Figure 7.10. SOLT calibration has been performed prior to measurements to de-embed the effect of cables and probes, while transformer baluns at each of the three ports have been de-embedded thanks to test structures on-chip.
The S-parameter results at 300 K are reported in Figure 7.8: the circuit operates with a 1-dB insertion loss and isolation bandwidth from 5.6 GHz to 7.4 GHz, with a minimum insertion loss of 2.2 dB and a maximum isolation of 18 dB. The bandwidth of the circulator is defined [132] as the frequency overlap $[f_1, f_2] \cap [f_3, f_4]$ between the 1-dB bandwidth $[f_1, f_2]$ of the insertion loss parameter (e.g., S_{32}) and the 1-dB bandwidth $[f_3, f_4]$ of the isolation parameter (e.g., S_{12}). This results in non-reciprocity over a 28% fractional bandwidth, while impedance matching at all ports is maintained below -10 dB. This is in line with expectations from post-layout simulations.
As suggested by the circuit symmetry, the S-parameters involving ports 1-3 and ports 2-3 show the same trend, while circulation between ports 1-2 is different, since signal goes through the non-reciprocal section directly. The insertion loss involving ports 1-2 is higher than the others due to the loss of the passives in the second-order all-pass filters and also due to imperfect constructive interference, originated by imperfect matching to the required phase relationship. The reduced isolation between ports 3-2 and 1-3 is due to the fact that they are comprised between the two reciprocal branches, so they experience weaker non-reciprocity, and is also subject to imperfect destructive phase interference. The insertion loss can be improved in the same design by using a single path implementation, as in [133, 134, 135], (at the cost of more sensitivity to duty cycle mismatch [132]), instead of a double I/Q branch, and by improving the quality factor of the designed

passives or using a better RF technology. The imperfect interference can be improved, with benefit on both insertion loss and isolation, by adding tunability to the filter capacitors and by adding phase control to the I/Q clock generation, to achieve more perfect phase matching. Moreover, in this work, a second-order all-pass filter is used. In principle, if a higher order filter is used, one could think that a higher isolation can be achieved, by using the increased degrees of freedom to achieve better inter-stage impedance matching and more accurate phase matching. However, in the real implementation, many more passives, especially inductors, would be required, and their limited Q factor would result in extra loss, which would decrease the final destructive interference. Therefore, this might not result in better isolation, depending on the technology.
S-parameters have been measured at 4.2 K as well, and the results are shown in Figure 7.9. The same measurement setup as for 300 K has been used, but SOLT calibration has been repeated at 4.2 K, taking care to correct for the reduced reference load resistance in the calibration kit. New transformer measurements have been taken to de-embed their (reduced) loss at 4.2 K. In particular, the insertion loss of de-embedding baluns is measured to be 2.1 dB at 300 K, while it becomes 1.3 dB at 4.2 K. The circulator operates over a 1-dB insertion loss and isolation bandwidth between 5.8 GHz and 7.6 GHz, while the minimum insertion loss is reduced to 1.3 dB and the maximum isolation becomes 17 dB.
As expected from cryogenic behavior, the operational bandwidth is slightly shifted towards higher frequency: this can be explained by a decrease in inductance, while capacitor values are almost kept constant. The minimum insertion loss is reduced, since the quality factor of passives is increased and the R_{ON} resistance of switches is smaller.

7.5.3 Noise measurements

The noise performance of the circulator has been measured at 300 K using the source-mismatch-corrected noise figure measurement capabilities of the PNA-X with the same measurement setup as for S-parameters. Full 3-port S-parameter calibration and noise source calibrations have been performed. The measured results are shown in Figure 7.11 and they show good agreement with insertion loss measurements from S-parameters, with a minimum noise figure of 2.4 dB. This shows low degradation from conversion of clock Phase Noise (PN) into additive noise in the signal path. The measurement accuracy with such setup is ± 0.1 dB, which is the noise figure of a reference through after all calibrations.
Noise measurements of the circulator at 4.2 K have also been performed. The circulator is a no-gain (actually lossy) device, whose noise temperature is too small to be measured directly when cooled to 4.2 K. Therefore in this case, the cold attenuator technique [141] has been adopted here.
An integrated attenuator (Analog Devices HMC658) was wire-bonded to the circulator at the input port, to attenuate room temperature noise, while a cryogenic amplifier (custom-designed 4-8 GHz cryo-CMOS LNA described in Chapter 8) was wire-bonded to the output to amplify the output noise of the chain to levels above the sensitivity of the low-noise receiver of the PNA-X. A 20-dB attenuator and a 20-K average noise-equivalent temperature LNA with tunable 20-40 dB gain were used for this experiment. Input and output ports of the system were probed, while the third port was terminated on-chip by controlling the digitally tunable termination polysilicon resistor (included for this measurement) with the

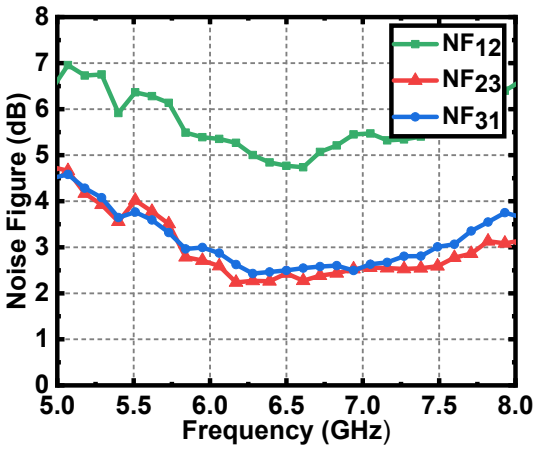

Figure 7.11 – Circulator noise figure measurements at 300 K.

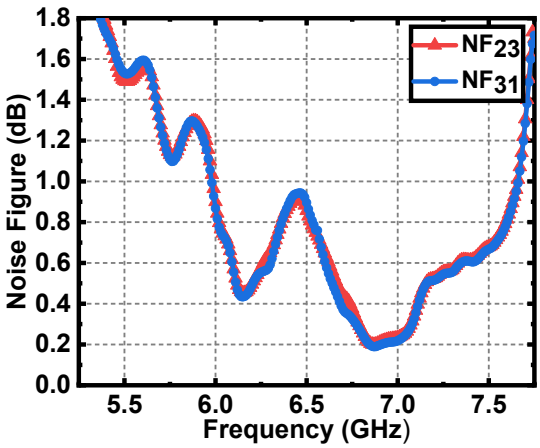

Figure 7.12 – Circulator noise figure measurements at 4.2 K.

SPI, to avoid room temperature noise from the third probe. Moreover, a sharp band-pass Surface Acoustic Wave (SAW) filter (Taiyo Yuden F6KA2G535L4AM-Z) was used on PCB to filter the LO signal, and reduce noise injection from the external room temperature signal. This whole system was operated at 4.2 K.

Full *S*-parameter and noise calibrations were used to move the reference plane to the probe tips, while separate measurements of the attenuator wire-bonded to the input transformer and of the output transformer wire-bonded to the LNA were used to de-embed the effect of the additional measurement blocks and refer the noise to the actual circulator core only. This procedure was repeated for each of the two-port pairs showing minimal insertion loss (ports 2-3 and ports 3-1), which could be used for signal transmission. The measured results are presented in Figure 7.12.

The noise of the circulator at 4.2 K, excluding contributions from clock feedthrough, is determined by the passive core, whose noise should be the same as the measured 1.3-dB insertion loss at 4.2 K, namely yielding a noise temperature of 1 K. The measured results present a degradation with respect to this theoretical prediction, with a minimum noise figure of 0.2 dB, yielding a noise-equivalent temperature of 15 K.

The noise floor of the circulator core is higher than expected. The increase of measured noise floor can be due to phase noise of the sinusoidal clock, which is filtered in the far-out region from the carrier at 2.6 GHz by the band-pass filter on PCB, but is then divided to 1.3 GHz and converted into a square wave, whose noise is mixed into in-band circulator noise. Using a lower noise signal generator could improve the results. Moreover, a spike can be seen at the 5^{th} harmonic of the on-chip LO signal (1.3 GHz), due to clock feedthrough, which can cause local noise increase at the frequency of odd clock harmonics that fall in the band of the circulator. Clock feedthrough could be mitigated by further reducing the clock frequency, so that only higher harmonics of the clock fall in band.

Such a cryogenic noise measurement is incredibly challenging, and presents several potential sources of inaccuracy that can also affect the measured result. Port mismatch is corrected in the noise measurement only up to the system measured by probe tips. Therefore, mismatch among the different elements (attenuator, circulator, LNA, termination resistor) is not taken into account. This can be very critical, especially for a correct

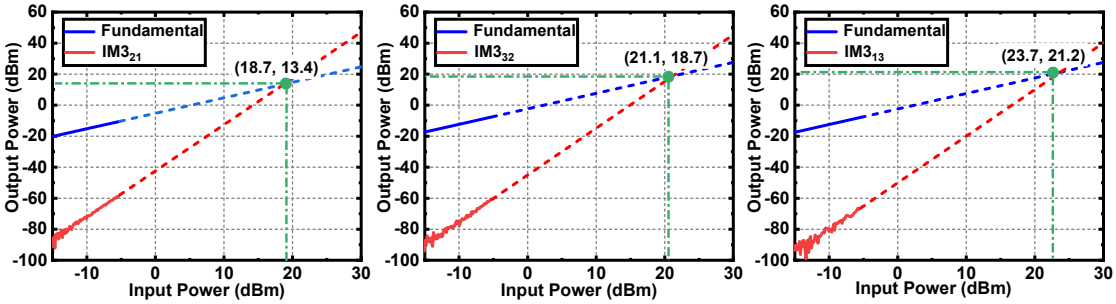

Figure 7.13 – Circulator linearity measurements at 300 K.

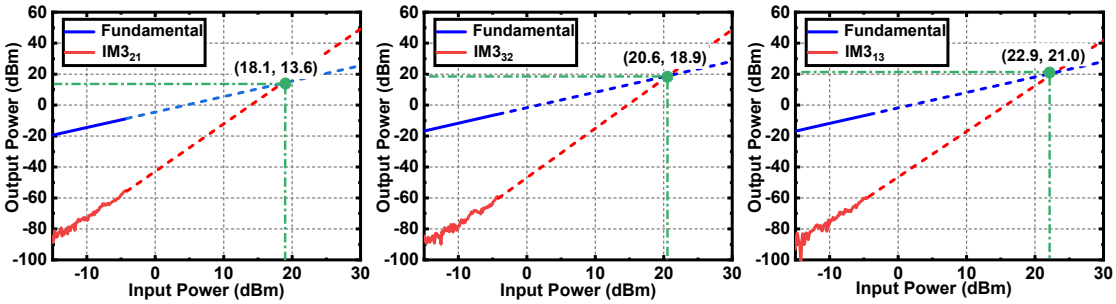

Figure 7.14 – Circulator linearity measurements at 4.2 K.

estimation of the actual LNA noise temperature when connected in this specific system. The accuracy of the 50 Ω termination resistor is also limited by the digital tuning range. All the mentioned sources of inaccuracy are very difficult to estimate and they require further investigation.

7.5.4 Linearity measurements

Finally, the circulator's linearity has been measured at 300 K, using the PNA-X as for *S*-parameters, performing *S*-parameter and power calibrations. The 3rd order Inter-Modulation (IM3) versus input power has been measured to derive the 3rd order Input Intercept Point (IIP3) and the 3rd order Output Intercept Point (OIP3), and the measured results are shown in Figure 7.13. The measured IIP3 is higher than +18.7 dBm in all directions of circulation.
Linearity has been measured at 4.2 K as well, without a modified setup, and the results are plotted in Figure 7.14. The measured IIP3 is larger than +18.1 dBm in all directions of circulation, which is sufficient for quantum computing applications, since the handled signal is very small (−90 dBm) and well below the non-linear region.

7.6 Discussion

The proposed circulator is targeting quantum computing applications, but it is worth mentioning that it could also be used for full-duplex transceiver applications, as the proposed techniques are also useful at 300 K. The closest application could be for 5th

	This work		[130]	[132]	[134]	[135]	[136]
Technology	40-nm CMOS		65-nm CMOS	45-nm SOI	180-nm SOI	45-nm SOI	45-nm SOI
Working temperature (K)	4.2	300	300	300	300	300	300
Architecture	All-pass		N-path	T-line	T-line	Band-pass	Active
Frequency (GHz)	5.8-7.6	5.6-7.4	0.61-0.97[1]	22.7-27.3	0.86-1.08	50-56.8	5.3-7.3[1]
Modulation index	5		1	3	3	7	N.A.
Insertion loss 2-3/ANT-RX (dB)	1.3	2.2	1.7	3.2	2.1	3.1	5
Isolation (dB)	17	18	>20	18.5	>25	>20	>30
Fractional bandwidth[2] (%)	28	28	4.3	18	17	14.5	6.3
Noise figure 2-3/ANT-RX[3] (dB)	0.2-1.5	2.4-3.4	4.3	3.3-4.4	2.9-3.1	3.2	20
IIP3 (dBm)	>+18.1	>+18.7	+27.5	+20.1	+50	+19.4	+20
Core area	0.45 mm^2 λ^2/4727		25 mm^2 λ^2/5760	2.16 mm^2 λ^2/67	16.5 mm^2 λ^2/5789	1.72 mm^2 λ^2/18	1.57 mm^2 λ^2/1442
Power consumption (mW)	2.1/10.5[4]	2.5/12.4[4]	59	78.4	170	41	415
Normalized power P_{DC}/f_0 (mW/GHz)	1.6	1.9	75	3.1	175	0.8	66

[1]Range of center frequency tunability, [2]1-dB insertion loss and isolation bandwidth, [3]Data is at 300 K for all other works, [4]Core (divider and mixer buffers) power and overall power consumption respectively.

Table 7.2 – Comparison table with state-of-the-art integrated circulators.

Generation (5G) new radio in the sub-6 GHz band, where the presented design techniques could be adapted without major modifications. In this case, however, the design targets would be quite different: power consumption should still be minimized, but large power handling and linearity should become a priority to meet transmitter requirements. In order to achieve this, techniques to enhance linearity such as the one proposed in [142] should be applied and the use of device stacking and thick-oxide transistors, as in [134], should be chosen.

7.7 Conclusion

In this chapter a 40-nm CMOS circulator operating from 300 K to 4.2 K, designed for qubit readout, has been presented. A staggered commutation circulator with a new all-pass filter architecture has been designed to address reduction of power consumption, bandwidth extension and compact area. A performance summary and complete comparison with state-of-the-art room temperature circulators is provided in Table 7.2.
A power consumption of only 2.5 mW is achieved at 300 K, while this is reduced to 2.1 mW at 4.2 K. A fractional bandwidth of 28% between 5.6 GHz and 7.4 GHz is achieved at 300 K, with a 2.2 dB minimum insertion loss, 18 dB isolation and 2.4 dB noise figure. While keeping the same fractional bandwidth, the circulator operates between 5.8 GHz

and 7.6 GHz with a 1.3 dB minimum insertion loss and 17 dB isolation at 4.2 K. The active area of the circuit is only 0.45 mm^2.
Thanks to the use of a second-order bridged-T all-pass filter, a large modulation index $m=5$ is achieved, thus reducing power consumption while using smaller area than multi-section transmission line approaches [132, 134, 135]. Thanks to the linear phase response, the fractional bandwidth is also extended with respect to state-of-the-art [132]. The noise figure is slightly lower than previous approaches [134], and parameters such as insertion loss and isolation are in line with previously proposed designs [130, 134]. If compared to active circulators designed in a similar frequency range [136], noise figure and power consumption are much better, thus showing the value of passive circulators for the proposed application.
Such circuit allows circulator miniaturization and multiplexing for multi-qubit readout systems in power-constrained cryostats, for example in the gate-based reflectometry readout proposed throughout this thesis.

8 Cryo-CMOS RF front-end circuits

The work presented in this chapter is included in the published or submitted papers:

[143] Y. Peng, **A. Ruffino**, and E. Charbon, "Analysis on Noise Requirements of RF Front-End Circuits for Spin Qubit Readout," *2019 International Conference on Noise and Fluctuations (ICNF)*, Neuchâtel, June 2019;

[144] Y. Peng, **A. Ruffino**, and E. Charbon, "A Cryogenic Broadband Sub-1 dB NF CMOS Low Noise Amplifier for Quantum Applications," under revision in *IEEE Journal of Solid-State Circuits (JSSC)*, December 2020;

[145] **A. Ruffino***, Y. Peng*, T.-Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba and E. Charbon, "A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots," accepted and to appear in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, February 2021.

In these works, I participated in the analyses and simulations for the derivation of noise specifications, then the presented low noise amplifier and oscillator have been conceived and designed by Yatao Peng, a colleague in AQUA laboratory, I performed the measurements and data analysis on the two chips with him, then I participated in the writing of the first two manuscripts and wrote the last one.

8.1 Introduction

In order to read out the state of quantum devices, this thesis focuses on RF probing techniques, which have been described in detail in Chapter 1. To derive the specifications required for the design of the proposed integrated cryogenic front-end, appropriate equivalent electrical models need to be established for the quantum devices and for the corresponding signals to read out [143]. This is presented in the following.
The RF reflectometry readout with a QPC is shown in Figure 8.1 (a), where the L_M-C_M resonator is used to match the output impedance of the QPC to 50 Ω at the operating

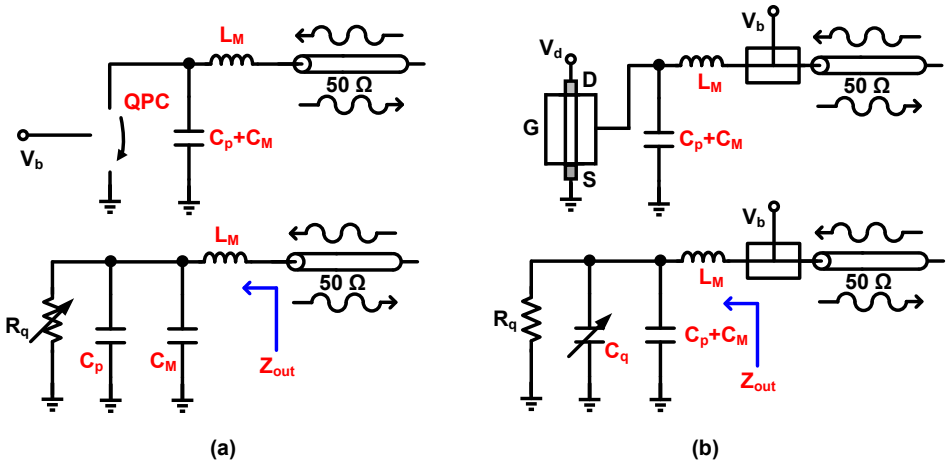

Figure 8.1 – RF readout techniques for quantum dots and their equivalent circuit for readout: (a) RF reflectometry, (b) gate-based dispersive readout.

frequency f_0. As the state of the quantum device changes, the conductance of the QPC (g_0) changes accordingly (by ~10%) [15]. This is modeled as a variable resistor R_q. The changes of R_q then modulate the RF carrier power reflected by the matching network at resonance. C_p represents any additional parasitic capacitance.
Similarly, the gate-based dispersive readout is illustrated in Figure 8.1 (b), where, according to the state of the quantum device, the gate capacitance changes and the additional quantum capacitance is modeled as a variable capacitor C_q. C_p represents the parasitic capacitance and R_q is the gate resistance of the quantum device.
It is important to recall that for the RF reflectometry readout with a QPC, the amplitude variation of the reflected signal is detected, while for the gate-based dispersive readout, the phase change of the reflected signal is the parameter of interest.
In order to estimate the quantities that need to be read out, one should analyze the variation of the reflected signal in the proposed models. The reflection of a microwave signal depends on the change of the load impedance, according to:

$$V_\mathrm{r} = V_\mathrm{in} \cdot \Gamma = V_\mathrm{in} \frac{Z_\mathrm{out} - Z_0}{Z_\mathrm{out} + Z_0}, \tag{8.1}$$

where V_in is the input signal, V_r is the reflected signal, Γ is the reflection coefficient, Z_0 is the characteristic impedance of the transmission line and Z_out is the output impedance of the quantum device with L_M-C_M impedance matching network. Z_out is given by:

$$Z_\mathrm{out} = \frac{R_\mathrm{q}}{1 + \mathrm{j}\omega R_\mathrm{q}(C_\mathrm{M} + C_\mathrm{p})} + \mathrm{j}\omega L_\mathrm{M}. \tag{8.2}$$

Consequently, upon change of the state of the quantum device, the amplitude variation ΔA of the reflected signal for RF reflectometry can be derived as [122]:

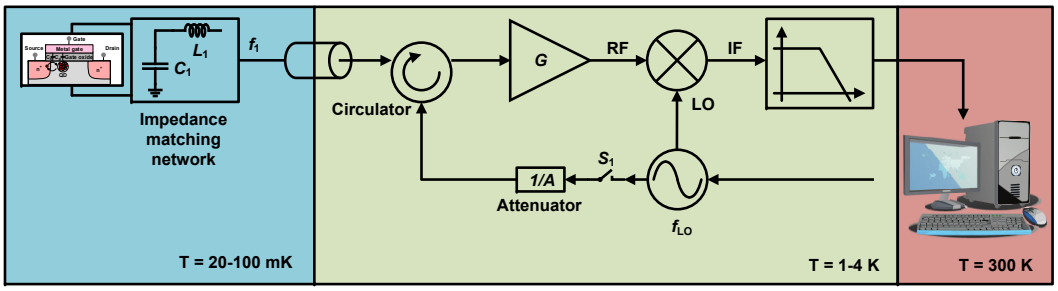

Figure 8.2 – Schematic diagram of the gate-based reflectometry readout circuit for spin qubits.

$$\Delta A \simeq |V_{\text{in}}||\Gamma_0| \frac{2\,Z_0\,Z_{\text{R}}^3\,(Z_0^2\,R_{\text{q}}^2 - Z_0^2\,Z_{\text{R}}^2 - Z_{\text{R}}^4)}{Z_{\text{R}}^8 + 2\,Z_{\text{R}}^4\,Z_0^2\,(Z_{\text{R}}^2 - R_{\text{q}}^2) + Z_0^4\,(Z_{\text{R}}^2 + R_{\text{q}}^2)^2} Q \frac{\Delta R_{\text{q}}}{R_{\text{q}}}, \tag{8.3}$$

where Γ_0 is the reflection coefficient of state $|0\rangle$, $Z_{\text{R}} = \sqrt{L_{\text{M}}/(C_{\text{p}} + C_{\text{M}})}$ is the resonator impedance, Q is the quality factor of the matching network and ΔR_{q} is the change of R_{q}. Similarly, the phase variation $\Delta\varphi$ of the reflected signal for gate-based dispersive readout can be derived as [18]:

$$\Delta\varphi \simeq \arctan\left[\left(\frac{1 - |\Gamma_0|}{1 + |\Gamma_0|}\right) \cdot Q \cdot \frac{2\Delta C_{\text{q}}}{C_{\text{p}} + C_{\text{M}}}\right] \simeq -\frac{\pi Q \Delta C_{\text{q}}}{C_{\text{p}} + C_{\text{M}}}, \tag{8.4}$$

where Γ_0 is the reflection coefficient of state $|0\rangle$, Q is the quality factor of the matching network, while ΔC_{q} is the change in quantum capacitance of the quantum device.
In order to read out these quantities, the presented radio-frequency techniques employ readout front-ends very similar to RF receivers for wireless communication systems [25]. In particular, the readout circuit proposed throughout this thesis is shown in Figure 8.2: it mainly consists of an *LC* impedance matching network operating at mK, a directional coupler or circulator (used to decouple the incident RF signal from the reflected signal carrying the readout information), a low-noise amplifier, a mixer and a voltage-controlled oscillator working directly at 1-4 K. The VCO generates an incident RF signal (attenuated not to affect the state of the quantum device) and this is guided down to the quantum device through the circulator and impedance matching network. Then, the signal is reflected by the quantum device. The reflected signal travels through the direct path of the circulator and is amplified by the LNA. Finally, the high-frequency signal is mixed with a local oscillator signal and the mixer down-converts it in a low-IF (or zero-IF) detection scheme, to be then digitized by an analog-to-digital converter. Differently from current measurement setups of semiconductor qubits for theoretical demonstration and verification, the demodulator and the VCO are moved to 1-4 K to simplify the electrical connections between cryogenic and room temperature circuits.
To guide the system-level circuit design, noise specifications of RF front-end circuits for qubit readout are analyzed, mainly focusing on noise figure of the low noise amplifier and phase noise of the voltage-controlled oscillator.
The two main spin qubit readout techniques, RF reflectometry and RF dispersive gate

sensing, should both detect weak reflected signals as low as −120 dBm and distinguish <2% amplitude or phase variation, which imposes high sensitivity and low noise requirements for the readout circuits, to achieve high measurement fidelity. For the analysis, the RF reflectometry and RF-DGS are modeled as demodulators respectively of an ON-OFF Keying (OOK) signal and a Phase Shift Keying (PSK) signal from qubits. From this, a first estimate of the required NF and PN for a given fidelity and readout bandwidth is given, as well as an insight into the relationship between phase resolution of RF-DGS and performance degradation due to PN of the VCO.
In order to prevent the incident signal from affecting the state of the quantum dot, the input power P_{in} sent to the quantum device should be set to less than −100 dBm for both readout techniques [14].
For the amplitude-based radio-frequency reflectometry, assuming a variation of the QPC resistance around 10%, and a minimum reflection coefficient $S_{11}=-18$ dB between the S_{11} for state $|0\rangle$ and the S_{11} for state $|1\rangle$, then the minimum reflected power to be read out is $P_r=-118$ dBm.
For a non-return to zero OOK signal, the Bit Error Rate (BER) of the detection is related to the output signal-to-noise ratio of the front-end circuit by the expression [146]:

$$\mathrm{BER}_{\mathrm{OOK}} = \frac{1}{2}\mathrm{erfc}\left(\frac{1}{2\sqrt{2}}\sqrt{\mathrm{SNR}_{\mathrm{out}}}\right). \tag{8.5}$$

Assuming a required readout fidelity $F_R = 1 - \mathrm{BER}=99.9\%$, resulting in a BER=0.1%, then the minimum required output SNR is found to be 16 dB.
The noise at the output of the LNA at deep-cryogenic temperature is mostly contributed by the LNA and the thermal noise of the L_M-C_M matching network. In order to relate input and output SNR, one can use the expression for the noise factor F of the front-end circuit, namely $F = \mathrm{SNR}_{\mathrm{in}}/\mathrm{SNR}_{\mathrm{out}} = P_r/(k_B\,T\,\mathrm{BW}\cdot\mathrm{SNR}_{\mathrm{out}})$, which becomes, when using dB scale:

$$\mathrm{NF} = P_r - 10\cdot\log\left(\frac{k_B\,T\,\mathrm{BW}}{1\,\mathrm{mW}}\right) - \mathrm{SNR}_{\mathrm{out}}. \tag{8.6}$$

Assuming an operating temperature for the quantum device $T=20$ mK, a readout frequency $f_0=6$ GHz, a quality factor of the matching network $Q=50$, resulting in a bandwidth $\mathrm{BW}=f_0/Q=120$ MHz, then the noise figure specification for the LNA can be calculated as NF=0.8 dB.
For the RF dispersive gate sensing readout, the reflected signal reaching the input port of the LNA is determined by the performance of the LC impedance matching network. Generally, the change in quantum capacitance ΔC_q is less than 1 fF [122]. Therefore, to increase $\Delta\varphi$, the impedance matching network should be endowed with a high Q-factor and well matched to 50 Ω. For instance, given $\Delta C_q=0.5$ fF, $C_p + C_M=200$ fF, $Q=50$ and $|\Gamma_0|=0.1$, then using Equation (8.4), one obtains $\Delta\varphi=11.5°$.
This means that the reflected signals can be modeled as a pair (corresponding to states $|0\rangle$ and $|1\rangle$) of M-ary phase shift keying (M-PSK) signals, where the order M is given by the closest integer such that $M > 360°/\Delta\varphi = 360°/11.5°$. This results in a 32-PSK modulation,

		Noise figure
Quality factor	$Q = 45$	0.54 dB
	$Q = 50$	0.9 dB
	$Q = 55$	1.4 dB

Table 8.1 – Low noise amplifier noise figure requirements for dispersive gate sensing.

for which the minimum phase discrepancy would be $360°/M = 360°/32 = 11.25°$, thus still achieving some margin. For a M-PSK signal, the BER of the detection is related to the output signal-to-noise ratio of the detection circuit by the relationship [147]:

$$\mathrm{BER}_{M-\mathrm{PSK}} \simeq \frac{1}{\log_2 M} \sum_{n=0}^{\frac{M}{2}-1} \frac{1}{2} \mathrm{erfc}\left(\frac{1}{\sqrt{2}} \sqrt{2 \cdot \mathrm{SNR}_{\mathrm{out}} \log_2 M} \cdot \sin\left(\frac{(2n+1)\pi}{M} \right) \right). \tag{8.7}$$

In order to achieve a fidelity $F_{\mathrm{R}} = 99.9\%$ and consequently a BER $= 0.1\%$ for 32-PSK signals, the output SNR of the readout chain is calculated to be 18.8 dB.
Assuming now a minimum reflection scattering parameter $S_{11} = -15$ dB, the sensed power at the input port of the LNA can be estimated to be $P_{\mathrm{r}} = -115$ dBm. Using again the expression $F = \mathrm{SNR}_{\mathrm{in}}/\mathrm{SNR}_{\mathrm{out}} = P_{\mathrm{r}}/(k_{\mathrm{B}}\, T\, \mathrm{BW} \cdot \mathrm{SNR}_{\mathrm{out}})$ in the form of Equation (8.6), one can calculate the noise figure requirements. Considering an operating temperature for the quantum device $T = 20$ mK, a readout frequency $f_0 = 6$ GHz, a bandwidth $\mathrm{BW} = f_0/Q$, the NF requirements of the LNA can be calculated to be 0.54 dB for $Q = 45$, 0.9 dB for $Q = 50$ and 1.4 dB for $Q = 55$.
If the phase change of the reflected signal is smaller than 1° [16], then the demodulation of the reflected signal should be modeled as a high-order M phase shift keying signal, such as 512-PSK or 1024-PSK, depending on the Q-factor of the matching network. Based on the results in [147], the required SNR for 512- and 1024-PSK under BER $= 0.1\%$ are approximately 35 dB and 40 dB, with some margin respectively. Then the NF requirements would become prohibitive to meet, thus highlighting the need for a large phase shift and high quality factor matching network.
Based on the presented derivations, the noise figure requirements considered for the LNA design are summarized in Table 8.1.
To demodulate, the reflected signals are mixed with the LO signal provided by the VCO. The demodulation of phase-modulated signals requires a low phase noise local oscillator, since the phase noise of the LO corrupts the retrieved phase from the input signals. The effect of demodulation in presence of noise and, in particular, phase noise of the local oscillator, is shown in Figure 8.3. The phase error caused by the phase noise of the LO can be expressed as:

$$\beta_\varphi \simeq \frac{180°}{\pi} \sqrt{2 \int_{f_{\mathrm{a}}}^{f_{\mathrm{b}}} \mathcal{L}(f)\, \mathrm{d}f}, \tag{8.8}$$

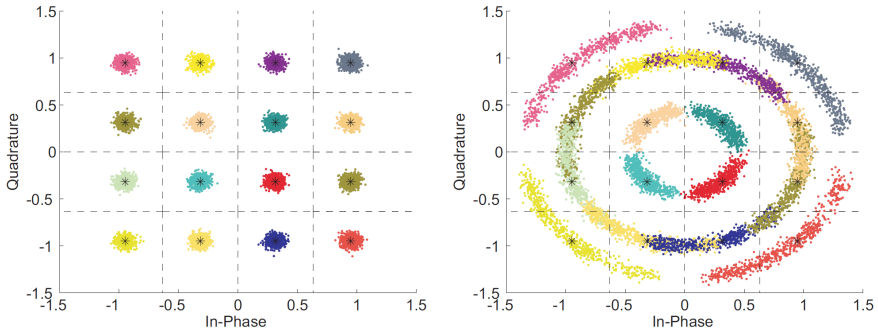

Figure 8.3 – Received signal constellation diagram of a 16-Quadrature Amplitude Modulation (QAM) system. **(a)** Pure Additive White Gaussian Noise (AWGN) channel with SNR=25 dB. **(b)** AWGN channel with SNR=25 dB affected by PN with an increment variance of 10^{-4} rad^2/symbol duration [148].

		Phase noise	
		$\beta_\varphi < 0.1°$	$\beta_\varphi < 0.05°$
Offset from the carrier	10 kHz	-90 dBc/Hz	-100 dBc/Hz
	100 kHz	-110 dBc/Hz	-120 dBc/Hz
	1 MHz	-120 dBc/Hz	-130 dBc/Hz
Calculated β_φ		0.06°	0.03°

Table 8.2 – Oscillator phase noise influence and requirements for the RF-DGS readout system.

where $\mathcal{L}(f)$ is the PN of the LO, typically characterized by a close-in phase noise region with $1/f^3$ frequency dependence, followed by a region with $1/f^2$ frequency dependence. f_a and f_b are then respectively the low frequency end of the $1/f^3$ portion of the phase noise power spectral density (for example 1 kHz) and the high frequency end of the $1/f^2$ portion of the spectrum (for example 10 MHz). In general, β_φ should be smaller than 1/10 of the real phase to be retrieved from the modulated signal. According to the typical minimum phase variation of the RF-DGS qubit readout technique and the above equation, the PN target for the VCO is set according to Table 8.2.

8.2 A cryogenic CMOS wideband low-noise amplifier

8.2.1 Specifications

The cryogenic low noise amplifier (cryo-LNA) is a critical block in the qubit readout chain, since it is the first block that amplifies the weak signals carrying quantum information from the qubits [144].
The most important specification for the LNA is the noise figure (-equivalent temperature), for which specific conclusions have been derived in the previous section. Considering them, and noise scaling at cryogenic temperatures, an LNA with NF $<$ 1 dB is targeted.
Moreover, when scaling up the number of qubits, frequency multiplexing should be used. For this, N rows of LC matching networks centered at different but unique frequencies (f_1,

	Noise figure	Frequency	Bandwidth	Power	Gain	P_{1dBin}
Specifications	< 1 dB	6 GHz	3.6 GHz	< 50 mW	> 40 dB	> -80 dBm

Table 8.3 – LNA specifications for gate-based qubit readout at 4.2 K.

f_2, ... f_N) should be designed to guide the signals to each quantum device (or each cluster of quantum devices), and act as a frequency multiplexer, as shown in Chapter 5. So far, sub-1 GHz frequencies have been used in RF-reflectometry qubit detection because lower frequency is more suitable for discrete RF circuits used in typical readout systems. However, in the fully-integrated vision presented in this thesis, higher readout frequencies around 6 GHz are chosen, since at higher frequencies a more compact footprint of integrated LC matching networks can be achieved, along with higher Q-factor on-chip inductors, wider absolute bandwidth to handle more qubits, and higher charge sensitivity [18].
Assuming the Q-factor of the LC matching network of the n-th quantum device is Q_n (3-dB readout bandwidth f_n/Q_n), to reduce crosstalk between the rows, the frequency spacing between row $n-1$ and row n should be $\Delta f_n = f_n/X$, where X is a variable determined by Q_n and probing signal quality, and it should be reasonably large. The bandwidth for N-qubit readout can then be calculated as:

$$\mathrm{BW} = \sum_{n=1}^{n=N} \left(\frac{f_n}{Q_n} + \frac{f_n}{X} \right). \tag{8.9}$$

If the Q-factors of the LC matching networks are assumed to be $Q = 50$ and one sets $X = 50$, i.e. the same bandwidth and frequency spacing for each qubit, from Equation (8.9), the bandwidth of the readout chain required for $N=20$ qubits is found to be ~ 3.6 GHz with center frequency at 6 GHz [144]. If then, time-multiplexing as in Chapter 5 is also considered, qubit readout for > 100 qubits is achievable.
In this multiplexing scenario, the power consumption for the entire readout chain is set to 1 mW/qubit, due to cooling power limitations [25], and half of it is allocated to the LNA. The gain of the LNA then should be sufficiently high, not only to amplify the weak qubit signals, but also to ensure that the overall chain noise factor F_{tot} is not degraded beyond the LNA noise factor F_1 by the noise factor F_2 of subsequent stages in the receiver, so that the previously calculated requirements for SNR are respected. These quantities are related by the Friis formula for cascaded noise factors, namely:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1}, \tag{8.10}$$

where G_1 is the LNA gain in linear scale. In order to ensure that the overall chain noise factor F_{tot} is close to the LNA noise factor F_1, one must ensure that $F_1 \gg (F_2 - 1)/G_1$, that is $G_1 \gg (F_2 - 1)/F_1$. Assuming a noise figure of 1 dB for the LNA ($F_1 = 1.25$) and a noise figure for the subsequent stages of 15 dB ($F_2 = 31$), then $G_1 \gg 25$. The LNA gain is therefore set to 40 dB, also to reduce the gain requirement for broadband IF signals.
Finally, the LNA 1-dB input compression point (P_{1dBin}) requirement is set to -80 dBm,

considering the input power to be read is normally less than −100 dBm.
Based on this analysis, the target specifications for the LNA are listed in Table 8.3.

8.2.2 Cryogenic amplifiers

Since the end of 1990s, RF cryo-LNAs were implemented exclusively using III-V devices [149, 150] since their cryogenic RF characteristics were much better than those of contemporary silicon-based amplifiers. SiGe HBTs have been exploited to design cryo-LNAs since the 2000s as their current gain and cut-off frequency improved state-of-the-art performance.
The recent proposal [22] of cryogenic CMOS electronics for quantum computing has then revived interest in CMOS technology to realize cryogenic LNAs. Early attempts to reach this goal started with a 500-MHz cryo-CMOS LNA for quantum computing designed in a 0.16 µm bulk CMOS process [25]. The LNA was based on a Noise Cancelling (NC) topology and obtained ~0.1 dB noise figure at 4.2 K. In [151], a narrow-band 2.025-2.12 GHz LNA operating at 77 K fabricated in 0.18 µm CMOS technology was proposed for space applications and it showed 0.5 dB cryogenic NF. A 7-GHz cryogenic CMOS parametric amplifier with >1.25 dB NF at 8 K was presented in [106]. In literature, however, no works on CMOS LNAs with sub-1 dB NF operating at high frequency (~6 GHz) have been reported to date.
Common approaches for wideband CMOS LNAs include common gate amplifiers with resistive feedback [152], noise-cancelling amplifiers [153], and common source amplifiers with broadband *LC*-ladder input impedance matching [154]. CG amplifiers are broadband since the input impedance matching can be easily achieved by proper sizing of the transistor transconductance. These structures, however, suffer from inferior NF (>2 dB), which is heavily deviating from the device intrinsic minimum noise figure NF_{min}. The NC amplifier utilizes an auxiliary amplifier to generate an out-of-phase noise signal path with respect to the main amplifier, and adds the noise signals at the output port. Ideally, the noise of the main amplifier can be totally nullified. However, the unequal parasitic capacitances of the auxiliary and main signal paths and especially the deterioration of mismatch for CMOS devices at cryogenic temperature [68], can result in noise phase misalignment at the output port, which weakens the effect of noise-cancellation at high frequencies. In addition, the auxiliary amplifier still contributes considerable noise. Thus, these structures are not attractive for high frequency qubit readout.

8.2.3 Circuit analysis of a wideband *LC*-loaded RF amplifier

Given that some of the traditional topologies fail to apply to the needs of this system, the CS cascode amplifier with Inductive Degeneration (ID) and resistive and capacitive (*R*-*C*) loading impedance is adopted as the basic structure [155, 156]. Several modifications are applied to suit the proposed quantum application. Firstly, the off-chip large inductor (>100 nH), which is used to reduce the noise contribution of the cascode transistor, is discarded, so as to achieve a fully integrated LNA. Second, an inductor is added to the gate of the cascode transistor to suppress its noise contribution further. Third, a transformer-based tank is utilized as the load of the first stage to extend the bandwidth. In addition,

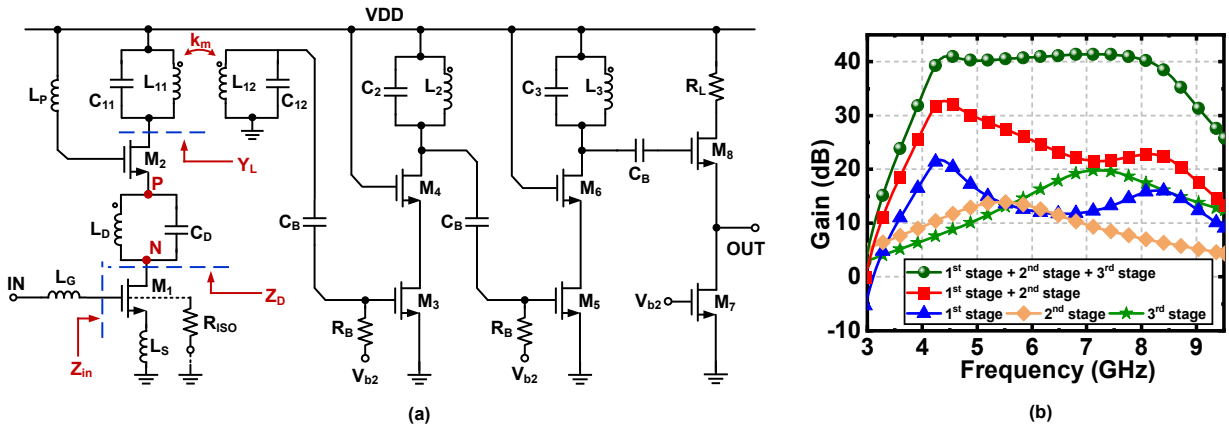

Figure 8.4 – (a) LNA structure. (b) Simulated gains of the various stages [144].

some further circuit design considerations for cryogenic operation are also included in the LNA design.

The LNA topology is shown in Figure 8.4 (a): it features three cascode stages, i.e., one input low noise stage and two gain boost stages, with an output buffer for output impedance matching. The first stage is a CS cascode amplifier with inductive degeneration, loaded by an LC parallel tank (L_D and C_D). The gate-drain capacitance of the input transistor M_1 (C_gd1) will involve the L_D-C_D tank and the transconductance of M_2 into the input impedance matching, while virtually not affecting noise. The transformer-based tank constructed by L_{11}, C_{11}, L_{12}, C_{12} is applied as the load of the cascode stage to extend the operating bandwidth.

Gain analysis

The voltage gain of the first stage can be calculated as $\sim G_\mathrm{m1}/Y_\mathrm{L}$, where the effective transconductance of M_1 is $G_\mathrm{m1} \simeq g_\mathrm{m1}/(1+\mathrm{j}\omega L_\mathrm{S} g_\mathrm{m1})$, with g_m1 gate transconductance of M_1 and L_S source degeneration inductor. The load admittance Y_L seen from the cascode stage can be calculated as [102]:

$$Y_\mathrm{L} = \mathrm{j}\frac{\omega^4 L_{11}L_{12}C_{11}C_{12}(1-k_\mathrm{m}^2) - \omega^2(L_{11}C_{11}+L_{12}C_{12})+1}{\omega^3 L_{11}L_{12}C_{12}(1-k_\mathrm{m}^2)+\omega L_{11}}, \tag{8.11}$$

where k_m is the coupling coefficient of the transformer. Setting Y_L=0, the two resonant frequencies of the tank can be obtained as:

$$f_{1,2}^2 = \frac{1+\eta \mp \sqrt{1+\eta^2-2\eta(1-2k_\mathrm{m}^2)}}{8\pi^2 L_{12}C_{12}(1-k_\mathrm{m}^2)}, \tag{8.12}$$

where $\eta = L_{12}C_{12}/L_{11}C_{11}$. f_1=4.2 GHz and f_2=8.2 GHz are set to cover the operating frequency with $k_\mathrm{m} \simeq 0.55$. As shown in Figure 8.4 (b), the simulated gain of the first stage

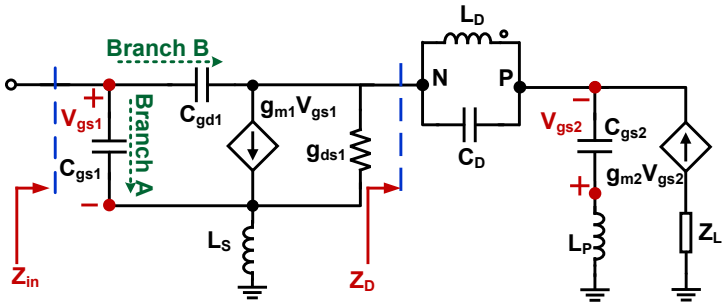

Figure 8.5 – Small signal equivalent circuit of the input stage for Z_{in} derivation.

is higher than 11 dB between 3.7 GHz and 9 GHz, which is sufficient to suppress the noise contribution of subsequent stages by a factor higher than 12.6. The magnitude ratio of transformer-based tank impedance at the two resonances is $R_{p2}/R_{p1} \sim (1-k_m^2)(1+\eta)/6$. R_{p2} tends to be smaller than R_{p1} when η is set to a reasonable value (<5), which results in gain inequality at resonances. Also, the gain decreases as the frequency deviates from f_1 and f_2 and a deep gain valley appears at the central frequency between the two peaks. The large gain ripple of the first stage is flattened by second and third stages. These stages are CS-cascode structures loaded by LC parallel tanks resonating at 5.5 GHz with a 6.5 Q-factor and 7.2 GHz with an 8.2 Q-factor, respectively. Both Q-factors account for the influence of the output resistance of transistors. The gain ripple of the four-stage amplifier is within ±0.5 dB in the operating band (Figure 8.4 (b)). The transformer-based tank load has the advantage to be compact and consume low power for wideband operation. Moreover, suppression of harmonics is also achieved thanks to its band-pass characteristics.

Input impedance matching analysis

The input impedance of the first stage of the LNA (Z_{in}) can be derived from the small signal equivalent circuit in Figure 8.5:

$$Z_{in} = \frac{(1+j\omega C_{gd1}Z_D)(1+M) + Z_D g_{ds1}(1-\omega^2 L_S C_{gs1})}{j\omega(Z_D + j\omega L_S)[g_{ds1}C_T + C_{gd1}(g_{m1} + j\omega C_{gs1})] + j\omega C_T}, \tag{8.13}$$

where

$$Z_D = \frac{1-\omega^2 L_P C_{gs2}}{j\omega C_{gs2} + g_{m2}} + \frac{j\omega L_D}{1-\omega^2 L_D C_D}, \tag{8.14}$$

then $M = j\omega L_S(g_{m1} + j\omega C_{gs1} + g_{ds1})$ and $C_T = C_{gs1} + C_{gd1}$. Z_D is the impedance seen from the drain of M_1, g_{m1} is the transconductance of M_1, g_{ds1} is the output conductance of M_1, and g_{m2} is the transconductance of M_2.
Z_{in} is composed of two parallel networks, namely branch A through C_{gs1} and branch B through C_{gd1}. If $C_{gd1} = 0$ and $g_{ds1} = 0$ are assumed, only branch A in Figure 8.5 conducts

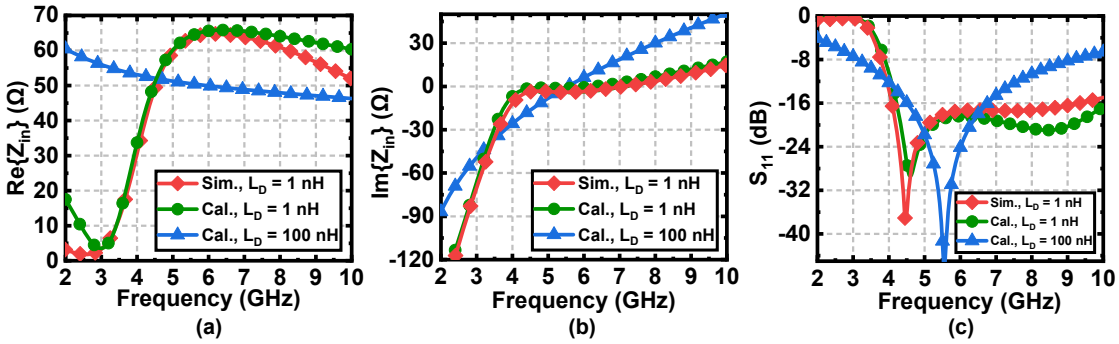

Figure 8.6 – Calculation and simulation results of (a) real part of $Z_{\rm in}$, (b) imaginary part of $Z_{\rm in}$, (c) S_{11} of the LNA input stage.

AC signals and performs the input impedance matching. The real part of $Z_{\rm in}$ is then $\Re\{Z_{\rm in}\} = g_{\rm m1}L_{\rm S}/C_{\rm gs1}$, which is independent from frequency, while the imaginary part of $Z_{\rm in}$, $\Im\{Z_{\rm in}\} = \omega L_{\rm S} - 1/(\omega C_{\rm gs1})$, is cancelled by $L_{\rm G}$, which results in the narrowband behavior for the classical CS-inductively source degenerated LNA [157]. For a sub-1 dB LNA design, a wide transistor is required for $\rm M_1$ ($\sim$ 300 µm) to obtain a large $g_{\rm m1}$ for high gain and low noise figure, in which case $C_{\rm gd1}$ is large enough ($\sim$ 0.1 pF) to involve $Z_{\rm D}$ into input impedance matching. From a qualitative perspective, if frequency is high enough, the impedance seen from branch B is resistive and determined by $g_{\rm ds1}$ and $\Re\{Z_{\rm D}\}$, which is less sensitive to frequency. When taken in parallel with the impedance seen from branch A, the real part of which ($\sim g_{\rm m1}L_{\rm S}/C_{\rm gs1}$) is also insensitive to frequency, then the real part of $Z_{\rm in}$ can be designed to be $\sim$50 Ω wideband. On the other hand, the imaginary part of $Z_{\rm in}$ is nulled by the resonance of an effective capacitance introduced by the capacitive load and the effective inductance due to $L_{\rm S}$, without using matching components at the input port [155]. Due to the low Q-factor of the resonance, relatively broadband matching was achieved in [155]. Moreover, $Z_{\rm D}$ was realized by a resistor in series with a capacitor explicitly, connecting in parallel to an RF choke to supply voltage. This, however, relied on the GaAs transistor's excellent intrinsic gain ($g_{\rm m}/g_{\rm ds}$) performance to achieve high voltage gain without a cascode transistor for the input stage to suppress the noise contribution of the subsequent gain stages.

In general, a cascode transistor is imperative for the input CS-transistor to enhance output impedance and thus the intrinsic voltage gain in deep-submicron CMOS processes. An LC parallel tank was proposed in [156] to be inserted between the drain of the input transistor and the cascode transistor so as to create a capacitive load while the resistive part is provided by the transconductance of the cascode common-gate stage implicitly. In [156], the inductor in the tank is off-chip with a value of 100 nH and Q>60, to obtain a more pronounced and easily-controlled capacitive load. However, an off-chip inductor introduces extra parasitic capacitances at nodes P and N, due to the bonding pads and PCB routes, which increases the noise contribution of $\rm M_2$, therefore here the LC-tank ($L_{\rm D}$ and $C_{\rm D}$) is integrated on chip. Neglecting the parasitic capacitances at nodes P and N, $Z_{\rm D} \simeq 1/g_{\rm m2} + {\rm j}\omega L_{\rm D}/(1-\omega^2 L_{\rm D}C_{\rm D})$ given that $g_{\rm m2} \gg \omega C_{\rm gs2}$ and $\omega^2 L_{\rm P}C_{\rm gs2} \ll 1$. If the resonant angular frequency $1/\sqrt{L_{\rm D}C_{\rm D}}$ is well below the operating frequency, one can still have a proper capacitive load for $\rm M_1$. Now, the effective capacitance $C_{\rm D}^{\rm e}(\omega)$, increases with frequency in the operating band. This is different from the cases in [155, 156], where

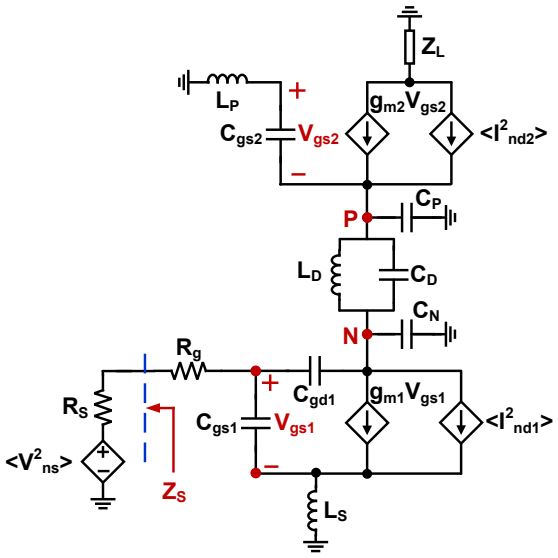

Figure 8.7 – Small signal equivalent circuit for noise figure analysis.

the effective capacitance is almost constant in the operating band due to the large L_D or RF choke. The small $C_D^e(\omega)$ at low frequency may lead to a real part of impedance seen from branch B, more sensitive to frequency. However, as the calculated results from Equation (8.13) and a simulation using BSIM4 transistor models show in Figure 8.6 (a), (b), with the help of non-constant $C_D^e(\omega)$, $\Re\mathrm{e}\{Z_{in}\}$ stays near 50 Ω and $\Im\mathrm{m}\{Z_{in}\}$ remains near 0 in a large band. This result is better than using a large L_D, where the imaginary part increases constantly. The gate inductor (L_G) is used for noise matching and can further enhance input impedance matching performance. In this design, g_{m2} is also adjusted to optimize S_{11}, hence the dimensions of M_1 and M_2 are not necessarily identical. The comparison of S_{11} calculation (L_D=1 nH and L_D=100 nH) and simulation results (L_D=1 nH) is shown in Figure 8.6 (c), and both cases can achieve wideband matching.
At the resonant frequency of L_D and C_D, the high impedance $|Z_D|$ may induce the LNA to oscillate. To avoid oscillation, an off-chip high-pass bias circuit was applied in [156] to guide the potential low frequency oscillating signals to ground. Actually, as long as $\Re\mathrm{e}\{Z_{in}\}$ is positive, the circuit is stable. This condition is not so difficult to satisfy because of the limited Q-factor of the tank and the high g_{ds1} of short-channel transistors. Relatively large L_S and lower g_{m2} help to ensure $\Re\mathrm{e}\{Z_{in}\} > 0$. In addition, the multistage cascode structure of the LNA has good isolation which ensures the global stability.

Noise analysis

The noise analysis of the LNA is based on the small signal equivalent circuit including the noise sources of the first stage shown in Figure 8.7. This section focuses on the noise of the input transistor. The additional noise generated by the cascode transistor is analyzed in the following section and will be included later. The noise contribution of the loss of L_S is neglected, since in general it is small enough to be fulfilled by a slab inductor with high Q-factor [158]. The gate-induced noise is also ignored because of its low contribution

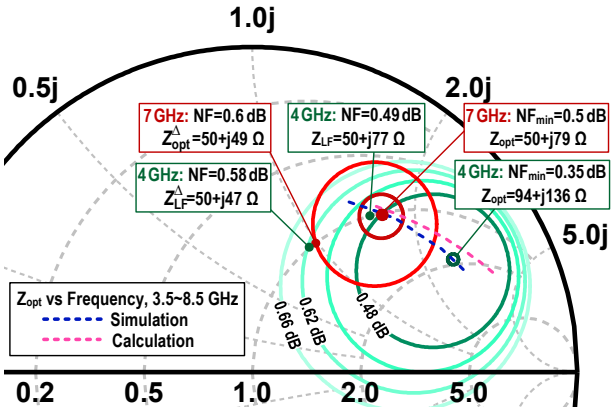

Figure 8.8 – Noise circles and NF_{min} versus frequency of the input transistor.

(<0.5%) for short-channel devices [159]. The noise of R_g, $\langle V_{Rg}^2 \rangle = 4k_B T R_g \Delta f$ and channel thermal noise $\langle I_{nd1}^2 \rangle = 4k_B T \gamma g_{m1} \Delta f / \alpha_g$ are considered in this design. Here, $\alpha_g = g_{m1}/g_{d01}$, where g_{d01} is the drain-to-source channel conductance with $V_{ds} = 0$, and γ is the thermal noise excess factor. According to linear noise network circuit theory [160], the noise factor of M_1 (F_{M_1}) and its noise parameters with $L_S(F_{min}, Z_{opt} = R_{opt} + jX_{opt})$ can be derived as:

$$F_{M_1} = F_{min} + \frac{\gamma \omega^2 C_T^2}{\alpha_g g_{m1} R_S} \left((R_S - R_{opt})^2 + (X_S - X_{opt})^2 \right), \tag{8.15}$$

$$F_{min} = 1 + 2\frac{\gamma \omega^2 C_T^2}{\alpha_g g_{m1}} \left(\sqrt{R_g^2 + \frac{\alpha_g g_{m1} R_g}{\gamma \omega^2 C_T^2}} + R_g \right), \tag{8.16}$$

$$Z_{opt} = \sqrt{R_g^2 + \frac{\alpha_g g_{m1} R_g}{\gamma \omega^2 C_T^2}} + j\left(\frac{1}{\omega C_T} - \omega L_S \right), \tag{8.17}$$

where R_S and X_S are the real and imaginary part of the source impedance seen from the gate of M_1, i.e., $Z_S = R_S + jX_S$. From Equation (8.16), F_{min} is determined by a parameter $N = R_g C_T^2 / \alpha_g g_{m1}$. For a MOSFET in saturation, one has [157]:

$$I_D = W_g C_{ox} v_{sat} V_{od} \frac{\rho_g}{\rho_g + 1} = W_g C_{ox} v_{sat} \frac{V_{od}^2}{V_{od} + L_g E_{sat}}, \tag{8.18}$$

$$g_{m1} = \mu_{eff} C_{ox} \frac{W_g}{L_g} V_{od} \alpha_g, \tag{8.19}$$

$$\alpha_g = \frac{1}{n} = \frac{g_{m1}}{g_{d01}} = \frac{1 + \rho_g/2}{(1 + \rho_g)^2}, \tag{8.20}$$

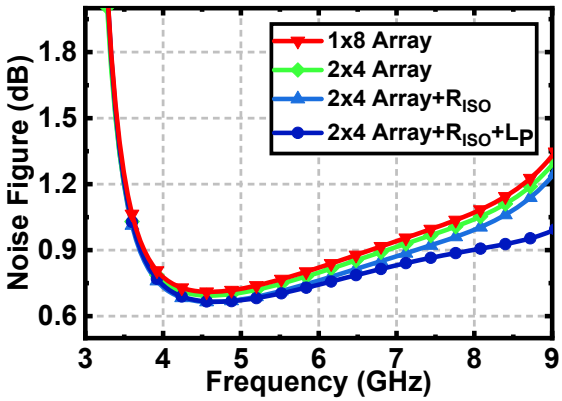

Figure 8.9 – Noise figure comparison for the used noise optimization techniques.

where W_g/L_g is the dimension of transistor M_1, $\rho_g = V_{od}/L_g E_{sat}$, V_{od} is the gate overdrive voltage, E_{sat} is the velocity saturation field strength, υ_{sat} is the saturation velocity, μ_{eff} is effective channel mobility, and n is the slope factor. C_T is proportional to $W_g \cdot L_g$ and has a weak dependence on the bias in saturation region. These expressions are valid for both short and long channel transistors, but depending on the value of ρ_g, the two different regimes can be identified. For short channel transistors $\rho_g \gg 1$, while for long channel transistors $\rho_g \ll 1$. Since the input transistor M_1 is normally a short channel device, the expressions can be simplified using the assumption $\rho_g \gg 1$.
Based on Equations (8.16), (8.18), (8.19), (8.20), for a power-constrained design (i.e., given I_D with fixed supply voltage), minimum channel length and high V_{od} are preferred to lower F_{min}. However, V_{od} needs to follow $V_{od} < V_{ds}$ well, to ensure M_1 is working in saturation region and the width of the transistor W_g also needs to adhere to metal current density rules for circuit reliability considerations. Therefore, F_{min} actually has a limited optimization margin (<0.1 dB). A simple principle to choose V_{od} and W_g/L_g is to maximize g_{m1} for a given I_D. Generally, performing impedance matching to the optimal noise impedance Z_{opt}, so to achieve $F_{M_1} = F_{min}$ according to Equation (8.15), is more important compared to lowering F_{min} [159]. *LC*-ladder matching networks can be exploited for a broadband match of 50 Ω to Z_{opt} [154], but due to the high loss of inductors, more NF performance is usually lost rather than gained. In this design, a single inductor L_G is used at the gate. Therefore, for noise matching, one obtains $\Re\{Z_{opt}\}$=50 Ω and $\Im\{Z_{opt}\} = \omega L_G$, i.e.:

$$\frac{\alpha_g g_{m1} R_g}{\gamma \omega^2 C_T^2} = 50 \tag{8.21}$$

$$\frac{1}{\omega C_T} - \omega L_S = \omega L_G. \tag{8.22}$$

Obviously, the above conditions can only be met at a single frequency. Since F_{min} rises rapidly with frequency according to Equation (8.16), the matching frequency is set slightly higher than the center frequency to balance the in-band NF variation. To determine the target noise matching impedance, the simulated noise circles of M_1 without L_S are

plotted in Figure 8.8, where V_{od} and W_g/L_g are set to meet Equation (8.21) and achieve a maximum g_{m1}=0.22 S at 7 GHz. It can be seen that both $\Re\{Z_{opt}\}$ and $\Im\{Z_{opt}\}$ decrease with frequency, which is consistent with Equation (8.17), and the discrepancies between calculation and simulation results of Z_{opt} are because of the neglected gate-induced noise and g_{ds1} in this analysis.
Now, the choice of Z_{opt} needs to consider the noise of the transistor and the extra noise brought by the necessary inductors for noise matching. One can see that, if Z_{opt}=(50+j80) Ω at 7 GHz is set as the target matching impedance, the calculated $L_S + L_G$ is ~1.5 nH based on Equation (8.22), which also tunes 50 Ω to Z_{LF}=(50+j77) Ω at 4 GHz (low frequency edge f_L), and Z_{LF} is located on a noise circle of 4 GHz with NF=0.49 dB, deviating only 0.15 dB from its NF_{min}. However, if one matches 50 Ω to an impedance Z^{Δ}_{opt}=(49+j50) Ω at 7 GHz instead of Z_{opt}, NF degrades only by 0.1 dB at 7 GHz, while the inductance $L_G + L_S$ scales down by 38%, so the noise contribution of the parasitic resistances of the inductors will reduce accordingly. For an inductor with Q-factor $Q \sim 15$, the NF reduction due to the inductance decrease is >0.1 dB. If the inductor area factor is also considered, Z^{Δ}_{opt} is then more attractive.

Noise of the cascode transistor

The channel thermal noise of the cascode transistor M_2 $\langle I^2_{nd2}\rangle$ contributes considerable noise at high frequency if the parasitic capacitances at node P and N (C_P and C_N) are too large to be ignored [161]. C_N is composed by gate-to-drain capacitance of M_1 (C_{gd1}), drain-to-bulk capacitance of M_1 (C_{db1}), while C_P is comprised of source-to-bulk capacitance of M_2 (C_{sb2}). In addition, both C_N and C_P are raised by the routing capacitance (C_{rtN} and C_{rtP}). Thus, $C_N = C_{gd1} + C_{db1} + C_{rtN}$ and $C_P = C_{sb2} + C_{rtP}$. The admittance at node P can be derived as:

$$Y_P \simeq j\omega C_P + \frac{j\omega C_N(1-\omega^2 L_D C_D)}{1-\omega^2 L_D(C_D+C_N)}. \tag{8.23}$$

If $C_D \gg C_N$, $Y_P \simeq j\omega(C_P + C_N)$. Actually, the equivalent parasitic capacitance at node P with the L_D-C_D tank is smaller compared to the case without L_D-C_D tank, which is beneficial to design a smaller L_P as described below. The noise factor of M_2 can be then calculated as:

$$F_{M_2} = \frac{(Y_P - j\omega C_{gs2} - \omega^2 L_P C_{gs2} Y_N)^2 \langle I^2_{nd2}\rangle}{4g^2_{m2} G^2_{m1} k_B T R_S}\left(\frac{Z_{in}+R_S}{Z_{in}}\right)^2. \tag{8.24}$$

Equation (8.24) reveals that if $L_P = (Y_P - j\omega C_{gs2})/\omega^2 C_{gs2} Y_N$, the noise contribution of M_2 will be nulled. On the other hand, L_P cannot be set too large since it will also decrease $\Re\{Z_{in}\}$ according to Equation (8.13), which further enlarges the discrepancy of Z^*_{in} and Z_{opt} of M_1. Based on the layout parasitic extraction results, $C_P + C_N \simeq 195$ fF and $C_{gs2} \simeq 95$ fF. Then, L_P is calculated to be ~0.85 nH. Figure 8.9 shows the NF of the first stage with and without L_P, where a ~0.1 dB NF improvement due to L_P can be seen.

Transistors	Dimensions	Components	Values
M_1	384 µm/60 nm	L_G	0.86 nH
M_2	160 µm/60 nm	L_S	0.25 nH
M_3-M_6	64 µm/40 nm	L_D	0.96 nH
M_7	24 µm/40 nm	C_D	2.5 pF
M_8	32 µm/240 nm	L_P	0.85 nH
		L_{11}	1.9 nH
		L_{12}	1.6 nH
		C_{11}	0.4 pF
		C_{12}	0.4 pF

Table 8.4 – LNA circuit component values.

8.2.4 Cryogenic design and implementation

Cryogenic circuit design considerations

The presented circuit analysis explains the proposed LNA design in the general case, however operation at cryogenic temperature requires adjustments in the LNA design. Since device models at cryogenic temperatures are not available in the foundry PDKs, most of the cryogenic design considerations are based on the cryogenic device behavior explained in Chapter 3 and Chapter 4 and some additional measurement results reported in literature [64, 65].
Due to the increase in the transistor's threshold voltage at cryogenic temperatures, as explained in Chapter 1 and Chapter 3, all the cascode stages (M_2, M_4 and M_6) are implemented as low threshold voltage transistors available in the PDK and the bias voltages of M_1, M_3 and M_5 can be set externally, to allow more tuning range. These are the main adjustments based on DC considerations. The cryogenic design modifications based on AC considerations are reported in the following.

Gain: the voltage gain of the LNA will increase by up to 10 dB at cryogenic temperature due to the higher mobility. On the other hand, the Q-factors of the inductors, transformers and capacitors will increase as the temperature decreases [79], as shown in Chapter 4. This means that the gain at the resonances of each LC tank load will be boosted. Hence, the flatness of the gain will be deteriorated, which can increase the design complexity of the analog-to-digital converters further along the down-conversion chain after the LNA. As previously shown, the inductance value decreases slightly at 4.2 K, while the Q-factor is $\sim 2.7\times$ higher than at 300 K, thus yielding approximately 8 dB gain enhancement. To reduce the gain variation, the inductors are put in series with small polysilicon resistors (5-10 Ω), so that the Q-factor of the tanks will be mostly determined by the polysilicon resistors and not only by the metal parasitic resistance. This will reduce, in part, the in-band gain fluctuation at cryogenic temperature.

Input impedance matching: since the gate-to-source/drain capacitances of the transistors have considerable influence on input impedance matching and noise matching, their

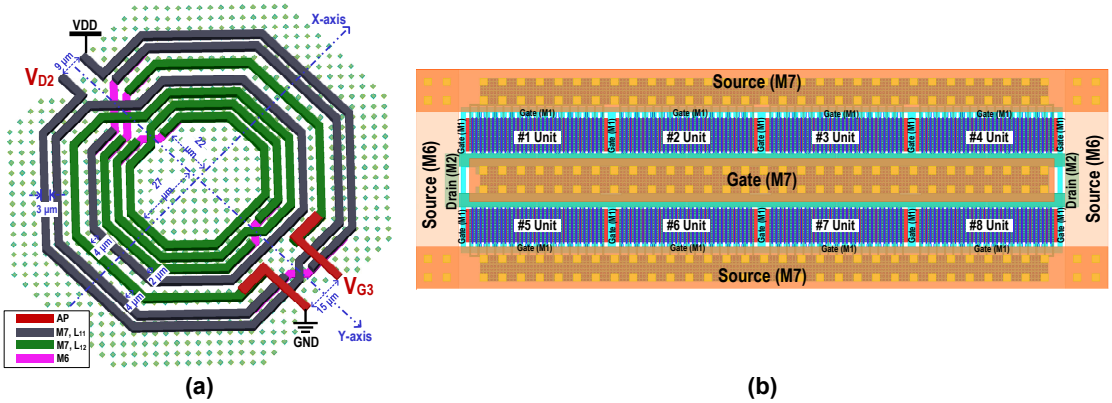

Figure 8.10 – (a) Layout of the transformer in the used 40-nm CMOS process with ultra-thick top metal. (b) M_1 layout.

variation at cryogenic temperature should be taken into account. Unfortunately, only few references exist in literature on small signal AC models of MOS transistors (especially in deep-submicron processes) at cryogenic temperature [162, 163, 72], and even in these references the explanations on the change of the parasitic capacitances at cryogenic temperature are not detailed. Therefore, for the design of this LNA, the variations of such capacitances were estimated from first principles and circuit parameters for cryogenic operation were modified based on such deductions.

For a transistor operating in saturation region, the gate-to-source capacitance mainly consists of the oxide capacitance between the gate and the channel, $C_1 \propto W_g L_g C_{ox}$, where C_{ox} is the gate-oxide capacitance per unit area, and of the capacitance due to the overlap of the gate polysilicon with the source and drain areas, $C_2 \propto W_g C_{ov}$, where C_{ov} is the overlap capacitance per unit length [164]. The second part also contributes to most of the gate-to-drain capacitance. At cryogenic temperature, on one hand, the neutral regions around the interface of the polysilicon gate and n^+ source/drain regions will be frozen-out, thus resulting in reduction of electric conduction [162], therefore C_{ov} (which determines C_{gd1}) will decrease at 4.2 K. On the other hand, the depletion region at the polysilicon-SiO_2 interface will become larger at low temperature, acting as an additional capacitor in series with the gate oxide capacitor [163]. This will reduce C_{ox} (which mainly determines C_{gs1}). Hence, it is considered that the gate-to-source/drain capacitances of the MOSFET should reduce during cryogenic operation.

Measurement results in [162, 163, 72] support this reasoning. By using a linear fitting of the trend reported by such works, it is estimated that the capacitance of M_1 will reduce $\sim$ 18% at 4.2 K. Therefore, in this design, the inductance $L_G + L_S$ is scaled up by about 18% to compensate for the capacitance reduction when achieving NF matching at a frequency around 7 GHz.

Noise: as transistor dimensions shrink to deep sub-micron, the channel noise is not solely thermal noise, since quasi-ballistic transport of carriers causes shot-like noise to also appear in the channel. Therefore, channel noise, including both types of noise, can be expressed as:

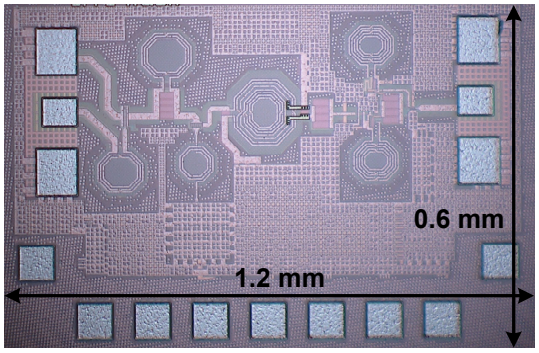

Figure 8.11 – Micrograph of the LNA.

$$\frac{\langle I_{nd}^2 \rangle}{\Delta f} = 4k_B T \frac{\gamma}{\alpha_g} g_{m1}(1-\tau_s)^2 + 2e\sigma I_D \tau_s^2, \tag{8.25}$$

where

$$\tau_s = \frac{R_b}{R_{ch} + R_b}. \tag{8.26}$$

In such equations e is the elementary charge, σ is the excess noise factor for shot noise, τ_s is known as the shot noise suppression factor [165], R_b is the equivalent barrier resistance inducing shot noise, which is inversely proportional to the gate-source voltage V_{gs}, and R_{ch} is the channel resistance including the source and drain contact resistance. The proportion of shot noise in the channel is highly dependent on the channel length and bias of the transistor [165]. For long-channel devices, $R_b \ll R_{ch}$, and the simple thermal noise model is accurate. For short-channel devices, shot noise becomes more important and in 40-nm channel length transistors it is estimated that shot-like noise can contribute $\sim$ 25% of the total noise power at room temperature, based on the measurement results in [166]. Thermal noise is considered to scale down with temperature, while shot noise, despite the weak temperature dependence through the current, is not expected to have major variations with temperature, so it is expected that the overall channel noise will be dominated by shot noise at cryogenic temperatures. In general, for LNAs designed for room temperature operation, thermal noise is expected to be the dominant source of noise, so the minimum channel length (40 nm) is set for the input transistor, since the noise factor F_{M_1} contains a term inversely proportional to g_{m1} and therefore proportional to the channel length L_g, as shown in the previous section. However, for LNAs operating at cryogenic temperatures, shot noise is expected to be dominant and a larger shot-like noise proportion with respect to the total channel noise is expected, therefore larger channel length is preferable to reduce the initial shot noise contribution, which is estimated not to change substantially when cooling down. Therefore, in this design, the channel length of M_1 and M_2 is set to 60 nm, for which it is estimated that the shot-like noise proportion at room temperature can be less than 10% of the total noise power. For the other transistors, the minimum channel length is still used, to reduce their parasitic capacitance.

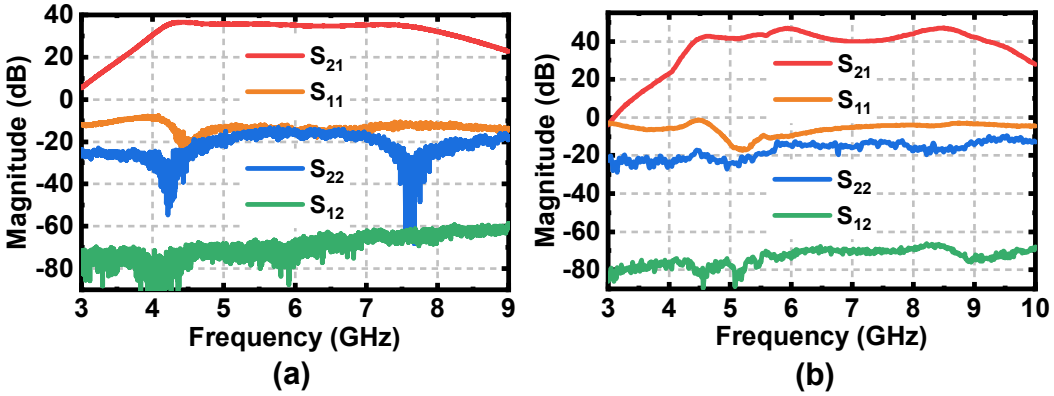

Figure 8.12 – S-parameter measurement results of the LNA at (a) 300 K and (b) 4.2 K.

LNA implementation

Based on the previous considerations, the LNA was designed according to the following steps: 1) for a given power consumption (i.e., I_D, since the power supply voltage is set by the process), V_{od} and W_g/L_g are determined according to Equation (8.21) at 7 GHz, where channel length is pre-set to 60 nm to reduce the shot-type noise; 2) the noise circles of M_1 are simulated and Z_{opt}^{Δ} is set, so as to obtain a value of $L_G + L_S$ based on Equation (8.22) at room temperature, which is then scaled up by ~ 18% to compensate for the transistor capacitance reduction at cryogenic temperature; 3) the L_D-C_D tank and the cascode transistor are added, then the S_{11} is optimized by tuning L_D, C_D, g_{m2}, and by proper distribution of L_G and L_S while keeping $L_G + L_S$ constant; 4) the parasitic capacitances at nodes P and N are extracted to define the inductance L_P; 5) the transformer-based tank, second, third stage and the output buffer are designed to satisfy the gain specifications. After some optimization, all the main parameters of the LNA in Figure 8.4 (a) are determined, and their final values are shown in Table 8.4. All the transistors are designed in deep n-wells to reduce substrate noise coupling. To further suppress the noise coupled through body terminals, large resistors R_{ISO} (~30 kΩ) have been used to bias the p-type body inside the deep n-wells to ground (Figure 8.4 (a)). Such resistors also prove to have a noise reduction effect, which is shown in Figure 8.9.

The layout of the transformer in the first stage is illustrated in Figure 8.10 (a). It is a combined tapped and interleaved transformer to keep a compact area (125 µm × 125 µm) while obtaining a medium coupling coefficient (k_m=0.55). The layout of M_1 is also critical for noise optimization, due to its large area. To minimize the transistor and interconnect parasitic resistances, the large transistor is divided into 8 unit cells and each cell consists of 32 fingers of width of 1.6 µm. Each gate node (finger) is laid out from both sides by metal 1 and then connected to the ultra-thick top metal, a technique which can theoretically reduce the effective gate resistance by a factor of 4 [167]. The 8 cells are placed in a 2-row and 4-column array (2 × 4 array, with fingers in vertical) as shown in Figure 8.10 (b). This layout reduces the effective interconnect route length of gate nodes within the units, and the post-layout simulation shows about 0.03 dB NF improvement, when compared with a 1 × 8 array [156], as depicted in Figure 8.9.

The cryo-CMOS LNA has been fabricated in a standard bulk 40-nm process with 7 metal

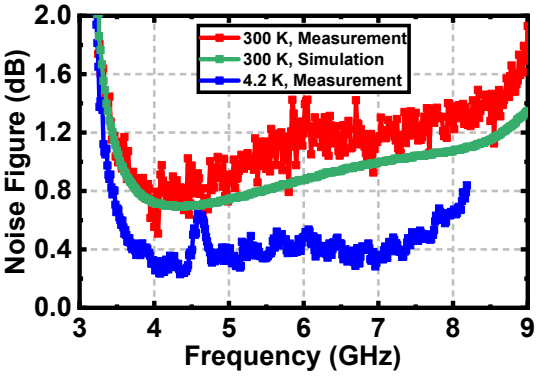

Figure 8.13 – Noise figure simulation and measurement results.

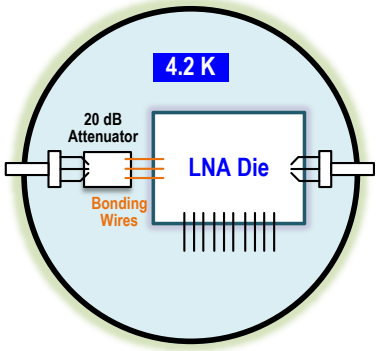

Figure 8.14 – Cryogenic noise figure measurement setup.

layers, including an ultra-thick metal layer. Figure 8.11 shows the micrograph of the LNA die, whose total area, including pads, is 1200 µm × 600 µm.

8.2.5 Measurement results

The fabricated die was glued and wire-bonded to a PCB for DC biasing, while the RF signals were tested by a pair of GSG probes. The LNA was measured in a Lake Shore CPX probe station at 300 K and 4.2 K, by using a Keysight PNA-X network analyzer N5245A, with embedded options for noise figure and linearity measurement. The SOLT calibrations were performed before the actual circuit measurements both at room temperature and cryogenic temperature.

At room temperature, the chip power supply was set to 1.4 V and the static current of the first stage was 24.5 mA, with a M_1 gate bias voltage V_{b1}=0.72 V. The other gain stages and the output source follower consume about 12 mA in total, with bias voltage V_{b2}=0.75 V.

At cryogenic temperature (4.2 K), the supply voltage was kept at 1.4 V. By tuning the input transistor bias, the bias current of the first stage was set to 19.3 mA. This bias current change from room temperature was chosen to obtain low input return loss at 4.2 K, and this is a reasonable adjustment that benefits noise optimization since the optimum noise impedance at cryogenic temperature tends to be closer to the conjugate of input impedance [72]. At 4.2 K, the second, third and output stages consume a total of 8.6 mA.

The S-parameter measurement results at 300 K are shown in Figure 8.12 (a). It can be seen that the gain is 35 dB with a good flatness (less than ±0.6 dB variation) from 4.15 GHz to 7.5 GHz, while the 3-dB bandwidth is 4.1 GHz to 8.2 GHz (~ 65% fractional bandwidth). Within the 3-dB frequency band, S_{11} is smaller than −12 dB, which indicates that the broadband power matching works well at room temperature. At the same time, the output port shows good return loss (S_{22}<−15 dB), since the transconductance of the output buffer is designed to be ~20 mS.

At 4.2 K, the chosen biasing conditions are enough to keep the total gain higher than 40 dB, as shown in Figure 8.12 (b). The gain center frequency deviates to higher values, which can be explained by the decrease in the inductance of the LC tanks and decrease

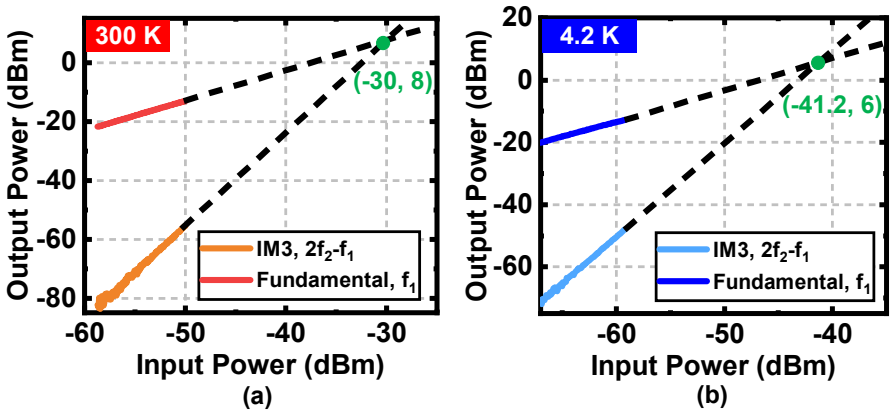

Figure 8.15 – IIP3 measurement results for a 6 GHz power sweep at (a) 300 K and (b) 4.2 K.

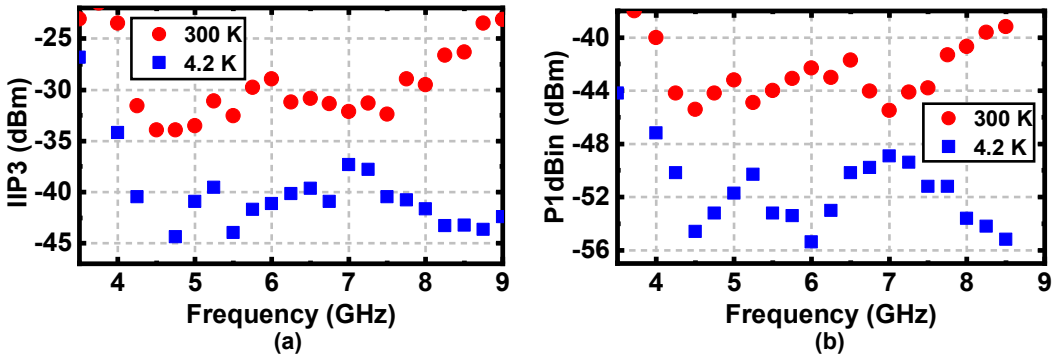

Figure 8.16 – (a) IIP3 measurement results and (b) $P_{1\mathrm{dBin}}$ measurement results versus frequency.

in transistor capacitance at low temperature. The gain of the LNA at 4.2 K is (42 ± 3) dB in the frequency band from 4.4 GHz to 8.2 GHz. The best S_{11} is ∼−18.2 dB at 5.2 GHz, which deteriorates to −5.6 dB at 8.5 GHz. The worse input match performance at 4.2 K is most likely due to the unwanted variation of C_{gs1} and C_{gd1}.

The noise measurement results are shown in Figure 8.13. At room temperature, the NF is as low as 0.75 dB at 4.5 GHz and it increases with frequency. The NF ranges from 0.75 dB to 1.3 dB over the entire operating frequency. The measurement results show good agreement with simulations performed using BSIM4 transistor models, which use an expanded version of Equation (8.25).

The NF at 4.2 K was measured with a cold attenuator technique, using the setup shown in Figure 8.14. A 20-dB attenuator die (Analog Devices HMC658) was mounted close to the LNA die on the same PCB, and GSG wire-bonding was employed for connection between them. This setup can ensure that the physical temperature of the attenuator is 4.2 K, the same as the LNA positioned on the sample stage of the probe station. In order to de-embed the noise of attenuator and bonding wires, the same attenuator was wire-bonded to a calibration die containing a reference through, implemented in the same process as the LNA. Once the noise equivalent temperature of the attenuator and LNA ($T_{\mathrm{eq,\,ATT+LNA}}$), and the insertion loss in linear scale of the attenuator with the de-embedding structure ($\mathrm{IL_{ATT}}$) are measured, the noise-equivalent temperature of the LNA ($T_{\mathrm{eq,\,LNA}}$) at 4.2 K can

be calculated by [168]:

$$T_{\text{eq, LNA}} = \frac{T_{\text{eq, ATT+LNA}} - 4.2\,\text{K} \cdot (\text{IL}_{\text{ATT}} - 1)}{\text{IL}_{\text{ATT}}}. \tag{8.27}$$

The cryogenic NF measurement results are shown in Figure 8.13. It can be seen that the NF is less than 0.5 dB from 4 GHz to 7.8 GHz and that the best noise figure is 0.21 dB at ~4.5 GHz, i.e. 15 K noise-equivalent temperature. This is in line with expectations from the experimental noise-equivalent temperature scaling at cryogenic temperatures reported in [72].
The small signal linearity performance (IIP3) of the LNA was tested by a two-tone measurement using sinusoidal signals with 1 MHz frequency spacing. The IIP3 at the central frequency of 6 GHz is −30 dBm at 300 K and −41.2 dBm at 4.2 K, as shown in Figure 8.15. The cryogenic IIP3 is greater than −45 dBm across the whole operating frequency band, as shown in Figure 8.16 (a). The linearity degradation at cryogenic temperature can be attributed to the higher overall gain of the LNA, due to increased mobility, which degrades the IIP3 for a fixed OIP3. Moreover, since the threshold voltage of transistors is increased, their overdrive voltage is reduced, which decreases the current and inversion coefficient, forcing them to enter moderate or even weak inversion, thus reducing their linearity. This is particularly important for the last stage, which determines the overall LNA linearity when the inter-stage gains are sufficiently high. Since the signals reflected by the quantum devices are sufficiently small, the linearity degradation at 4.2 K can be accepted. The large signal linearity performance measurements of the LNA, meaning the input 1-dB compression point P_{1dBin}, are shown versus frequency at 300 K and 4.2 K in Figure 8.16 (b). It can be seen that P_{1dBin} is always higher than −56 dBm at 4.2 K, which is much higher than the reflected signal power coming from the quantum devices.

8.2.6 Discussion

The proposed LNA was based on a CS cascode stage with inductive source degeneration and resistive/capacitive impedance loading technique. The capacitive load was created by an on-chip *LC* parallel tank and the resistive load was provided by the transconductance of the cascode transistor implicitly. Limited inductance in the *LC* tank introduced non-constant in-band equivalent capacitance, which was proven to be beneficial to input impedance matching. An inductor was added to the gate of the cascode transistor to suppress its noise contribution and a transformer-based resonator was employed as load of the first stage to extend the bandwidth.
The measured performance of the LNA is summarized in Table 8.5. The presented LNA exhibits excellent performance in terms of bandwidth and gain. Without using high quality off-chip impedance matching components, the sub-1 dB NF performance is comparable with LNAs designed in InP High-Electron-Mobility Transistor (HEMT) and SiGe processes, both at room and cryogenic temperature.
The cryo-LNA meets the performance requirements for the gate-based dispersive readout of spin qubits, and it has been integrated in a full receiver, as shown in Chapter 9, to realize a fully-integrated qubit readout platform.

	Performance	
Technology	40-nm CMOS	
Working temperature (K)	300	4.2
Frequency (GHz)	4.1 ~ 7.9	4.5 ~ 8.2
Gain (dB)	35.5 ~ 36.5	39.2 ~ 44.8
Input match (dB)	-22 ~ -12	-19 ~ -6
Noise figure (dB)	0.75 ~ 1.3	0.21 ~ 0.65
IIP3 (dBm)	>-35	>-45
P_{1dBin} (dBm)	>-46	>-55
Area (mm^2)	0.72	
Power supply (V)	1.4	
Power consumption (mW)	51.1	39

Table 8.5 – Measured LNA performance at 300 K and at 4.2 K.

8.3 A cryogenic CMOS *LC* voltage-controlled oscillator

8.3.1 Specifications

The other fundamental block in the qubit readout chain is the voltage controlled oscillator [145]. The VCO has two functions in the system shown in Figure 8.2. First, the VCO provides the probing input signal going into the circulator, to sense the state of the qubit. Second, the VCO provides the local oscillator signal for demodulation of the reflected signal.
The specifications for the design of the VCO are based on the target phase-based dispersive gate sensing spin qubit readout and are described in the following.

Frequency: the target readout frequency is ~ 6 GHz, which is consistent with the LNA presented in the previous section and the overall receiver vision. In order to demodulate the reflected signal and retrieve the phase information, quadrature demodulation should be employed in the spin qubit readout system. Therefore, a quadrature local oscillator structure is required. For this scope, a frequency divider by 2 can be used to generate broadband quadrature signals. Therefore, the design frequency of the VCO can be around 11-16 GHz, which means the Frequency Tuning Range (FTR) is 5 GHz. The design target is set to 10.5-16.5 GHz (44% FTR) with some design margin, to accommodate for process variation.

Phase noise: based on the previous discussion, the calculated phase noise requirement of the VCO should be better than -115 dBc/Hz in the sub-flicker noise corner region and better than -137 dBc/Hz at 10 MHz offset from the carrier in the thermal noise region [25].

Power consumption: the power consumption of the VCO should be kept as low as possible, to relax the cooling requirements, consequently, 5 mW is set here as the design target.

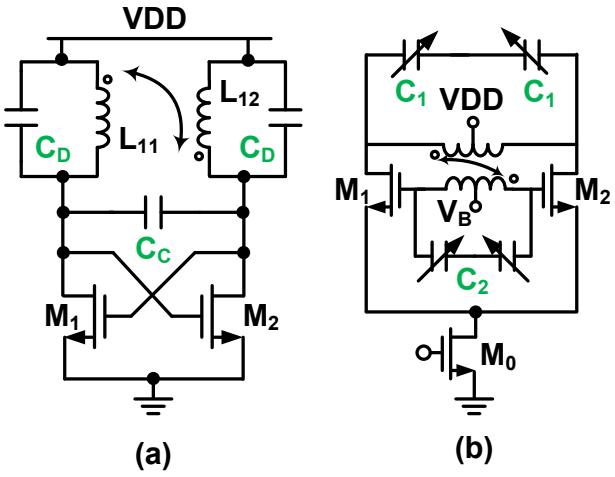

Figure 8.17 – Typical *LC*-tank oscillator structures to achieve low phase noise. (a) Transformer-based VCO with implicit common-mode resonance and second harmonic optimization [169]. (b) Transformer-based class-F VCO with third harmonic optimization [102].

8.3.2 Cryogenic oscillators

Ring oscillators are one of the typical oscillator structures, and they provide broadband tuning range and compact area. The drawback of ring oscillators is high phase noise, due to the absence of a frequency selective network to filter the broadband transistor noise. Ring oscillators have been designed and measured for cryogenic temperatures [170], but such choice is not very attractive for multi-GHz low phase noise oscillators.

LC-tank oscillators are a more commonly used structure for low phase noise requirement applications, since the *LC* resonator network shapes and suppresses the phase noise introduced by the negative transconductance pair. However, the frequency tuning range is limited by the capacitance variation range, usually given by switched capacitor arrays and/or varactors. PN and FTR are two figures of merit requiring compromise in the design of *LC* tank VCOs. To achieve low PN for *LC*-tank VCOs, partial FTR can be sacrificed by designing the varactors with minimum length to increase the quality factor Q of the *LC*-tank. Also *LC*-tank oscillators have been proposed at cryogenic temperatures already [171, 25].

At cryogenic temperatures, the flicker noise of CMOS transistors increases [25] and the bandwidth of Phase-Locked Loops (PLLs) is limited, so when designing VCOs at 4.2 K for qubit readout, both the thermal noise region ($1/f^2$) and the flicker noise region ($1/f^3$) should be treated seriously. Recently, harmonic oscillator techniques were proposed to optimize the phase noise of the VCO [172], where the second harmonic is used to lower the flicker noise corner and the third harmonic is applied to reduce the Impulse Sensitivity Function (ISF), and thus PN, due to thermal noise. A typical VCO structure with second harmonic optimization is illustrated in Figure 8.17 (a) [169], where the *LC* tank resonates at both operating frequency and second harmonic. The PN of the VCO is -139.7 dBc/Hz at $\Delta f = 3$ MHz from 3 GHz, and the flicker noise corner is $\sim$ 200 kHz. Figure 8.17 (b) depicts a class-F VCO implemented by a transformer, where the tank shows high impedance at fundamental frequency and third harmonic [102], and the VCO achieves extremely low

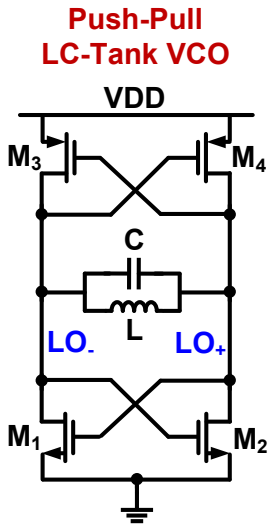

Figure 8.18 – Schematic of the designed push-pull *LC* VCO.

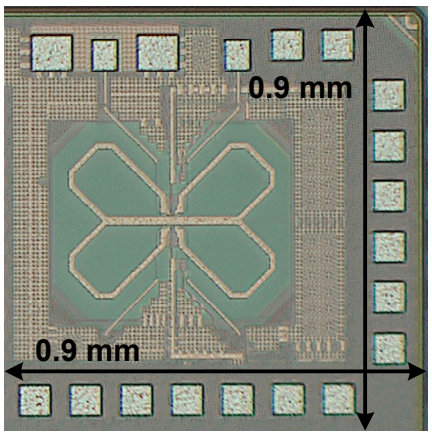

Figure 8.19 – Chip micrograph of the designed push-pull *LC* VCO.

PN of -142.5 dBc/Hz at $\Delta f = 3$ MHz from a 3.7 GHz fundamental, and the $1/f^3$ corner is $\sim$ 300 kHz. Therefore, both low PN and low flicker noise corner VCO can be achieved for qubit readout when both second and third harmonics are considered for the tank design. In this design, since large variability has to be considered, a broadband *LC*-tank VCO is chosen for spin qubit readout, while considering also the high PN requirement for the demodulation of the reflected signals.

8.3.3 Circuit design and implementation

In order to fulfill the design requirements, a differential complementary *LC* tank VCO structure is proposed. A pMOS and an nMOS cross-coupled pair are arranged in push-pull configuration, around a tunable *LC* resonator, as shown in Figure 8.18.
The push-pull configuration is chosen to reduce power consumption. Moreover, in order to enlarge the tuning range of the VCO, while lowering the phase noise, a dual mode-switched VCO is proposed [173]. The VCO has two oscillation modes, that cover approximately half of the tuning range each. The frequency range for the low mode (L-Mode) and the high mode (H-Mode) are 10.5-13.2 GHz and 13.0-16.5 GHz, respectively. Moreover, the capacitor is made tunable by using a 5-bit binary-weighted switched capacitor array for coarse frequency tuning, and varactors with optimum quality factor for fine frequency tuning. This slightly decreases the tank quality factor, but allows greater flexibility on the VCO design.
The proposed VCO is designed to achieve wide tuning range and low phase noise. The push-pull architecture is indeed also exploited to reduce the $1/f^3$ flicker noise contribution to phase noise by using both pMOS and nMOS in the cross coupled pairs. The use of pMOS is favorable, since it can normally have 1/10 of the flicker noise contribution of an nMOS.
The phase noise of an *LC*-tank VCO can be expressed as [174, 175]:

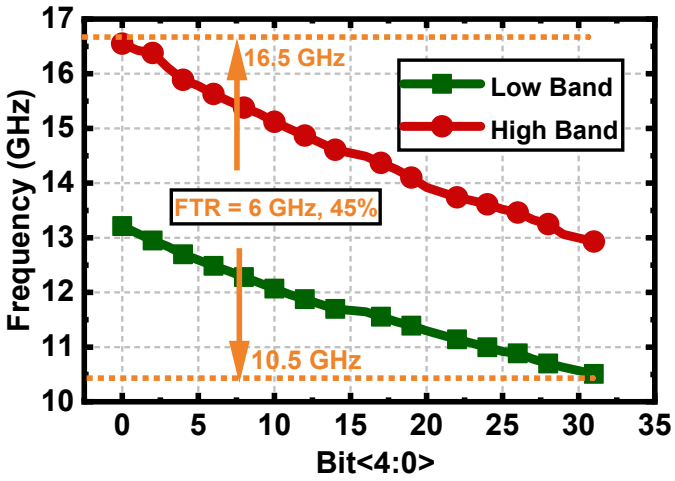

Figure 8.20 – Measured tuning range of the VCO at 3.5 K.

$$\mathcal{L}(\Delta\omega) = 10\log\left(F \cdot \frac{k_B T}{V_d^2} \cdot \frac{L}{Q_T} \cdot \frac{\omega_0^3}{(\Delta\omega)^2}\right), \tag{8.28}$$

where F is the device excess noise factor, V_d is the differential oscillation amplitude, L is the tank inductance, ω_0 is the LC tank resonance frequency, $\Delta\omega$ is the offset from the carrier and Q_T is the tank quality factor, which is determined by the quality factor of the inductor, varactor, and the output resistance of $-g_m$ cells.
Consequently, in order to minimize the phase noise, it is beneficial to maximize the oscillation amplitude V_d and reduce the inductance, or better, the L/Q_T ratio.
The dual mode-switched VCO has been implemented using a 40-nm CMOS process with 7 metal layers, one of which is an ultra-thick layer. The micrograph of the chip is shown in Figure 8.19. As can be seen, the proposed inductor is horizontally and vertically symmetric, which makes the VCO immune to frequency pulling.
To alleviate the effect of bonding wires, the area surrounding the VCO core is filled by decoupling capacitors. An open drain buffer is used to lead the oscillating signal to the GSG pad for test, since a single ended signal is used for measurement. To balance the other path, an open drain buffer is also added to the other branch.

8.3.4 Measurements

The presented VCO has been measured with GSG probing in a Lake Shore CRX-4K probe station at 296 K and 3.5 K. At room temperature, namely 296 K, the oscillator consumes 6.3 mA from a 1.255 V power supply, for a total 7.9 mW power consumption. When the oscillator is cooled down to 3.5 K, the oscillator draws 3.7 mA current from an increased 1.3 V power supply, for an overall power consumption of 4.8 mW. The power supply has been increased to compensate for the increased threshold voltage of transistors in the cross-coupled pair, and guarantee operation in saturation.

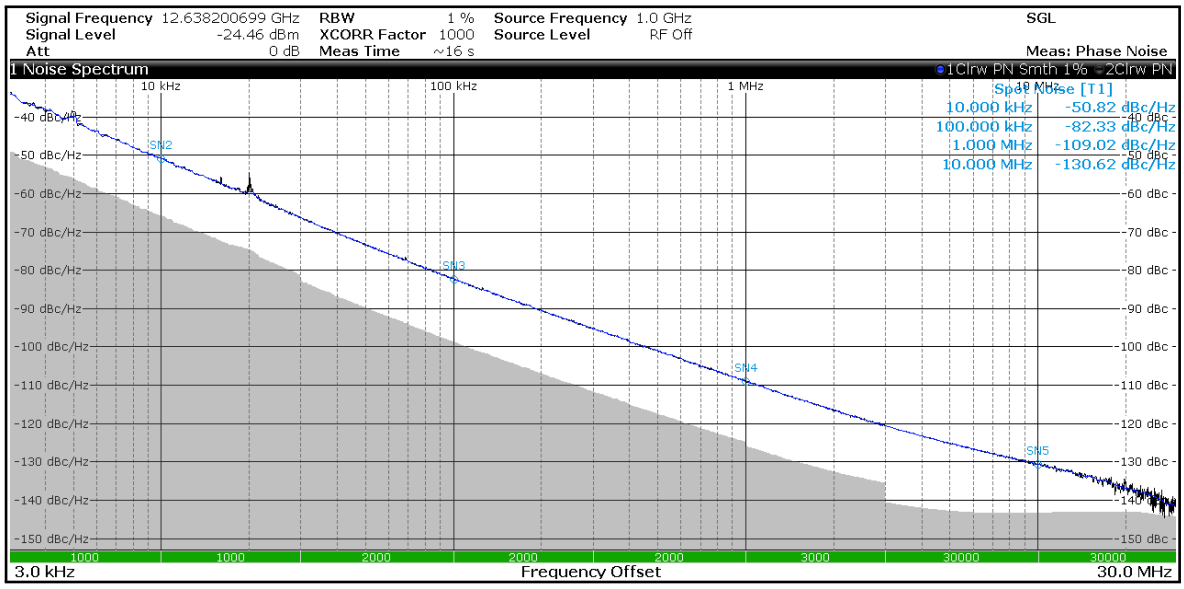

Figure 8.21 – Measured phase noise of the VCO at 296 K.

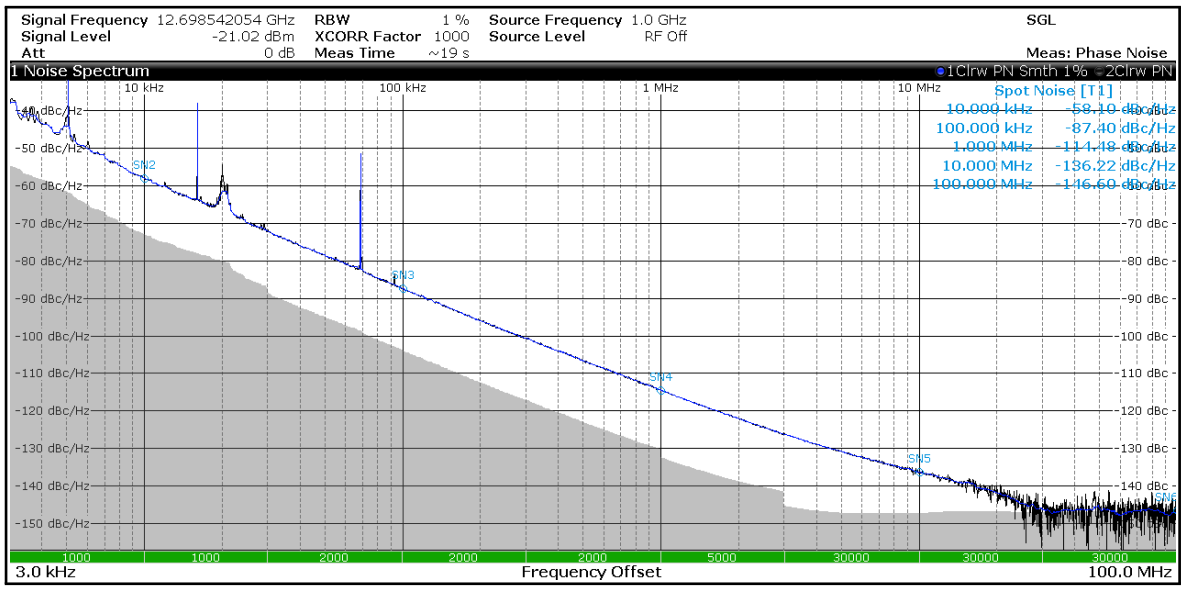

Figure 8.22 – Measured phase noise of the VCO at 3.5 K.

The oscillator operation has been tested sweeping across the two operating bands and across the various tuning bits for each band. The tuning range at 296 K has been found to be between 10.4 GHz and 16.4 GHz, thus achieving a 45% relative tuning range. At 3.5 K, the oscillation frequency is slightly shifted towards higher values, but the overall tuning range remains similar, between 10.5 GHz and 16.5 GHz. The measured tuning range at 3.5 K is shown in Figure 8.20.
Performance of the oscillator has been then measured at the center of its tuning range, where it is supposed to operate, around 13 GHz, which is also where power consumption

	Performance	
Technology	40-nm CMOS	
Working temperature (K)	296	3.5
Tuning range (GHz)	10.4 ~ 16.4	10.5 ~ 16.5
Carrier frequency (GHz)	12.6	12.7
Phase noise at 1 MHz offset (dBc/Hz)	-110	-115
Phase noise at 10 MHz offset (dBc/Hz)	-130	-137
Area (mm^2)	0.81	
Power supply (V)	1.25	1.3
Power consumption (mW)	7.9	4.8

Table 8.6 – Measured VCO performance at 296 K and at 3.5 K.

data are reported.
The phase noise of the oscillator has been measured at 296 K and the results are shown in Figure 8.21, while the measurement results obtained at 3.5 K are reported in Figure 8.22. As one can see, at cryogenic temperatures, for a 12.7 GHz carrier, the phase noise at 1 MHz offset from the carrier is -115 dBc/Hz, while it becomes -145 dBc/Hz in the noise floor region.
From the reported data, it is possible to calculate the Figure Of Merit (FOM), which is defined as:

$$\mathrm{FOM} = -\mathrm{PN} + 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) - 10 \cdot \log\left(\frac{P_{\mathrm{DC}}}{1\,\mathrm{mW}}\right). \tag{8.29}$$

This results at 296 K in a FOM=183 dBc/Hz, while at 3.5 K this corresponds to a FOM=190 dBc/Hz, both calculated at 1 MHz offset from the carrier.

8.3.5 Discussion

The presented VCO was realized with a push-pull architecture, implemented to reduce power consumption, and included mode-switching and a tunable switched capacitor array with varactors to enlarge the available tuning range.
The measured performance of the VCO is summarized in Table 8.6.
The obtained results are consistent with the requirements derived for gate-based dispersive readout, and allow to use the proposed VCO as an integrated solution for signal generation at cryogenic temperatures, as shown in Chapter 9.

8.4 Conclusion

In this chapter, the fundamental requirements for RF reflectometry have been presented and specifications for the most important blocks in the readout front-end, namely LNA and VCO, have been derived.
Subsequently, a cryogenic CMOS low-noise amplifier operating at 4.2 K between 4-8 GHz,

with 40 dB gain and 0.21 dB noise figure has been presented, to be used to amplify the weak signals coming from the qubits.
Moreover, a cryogenic CMOS push-pull *LC* VCO operating at 3.5 K between 10.5 GHz and 16.5 GHz has been shown, so as to generate probing and down-conversion LO signal to demodulate phase-modulated signals coming from qubits in a gate-based dispersive readout scheme.
These two circuits constitute important blocks in the fully-integrated dispersive readout vision presented throughout this thesis, and satisfy the specifications derived for it. In this chapter they have been presented and characterized individually, just to give the background required for their co-integration in a single cryogenic CMOS fully-integrated receiver with frequency synthesizer, presented in Chapter 9, which collects all the work previously presented.

9 A cryo-CMOS I/Q low-noise low-IF down-conversion RF receiver

The work presented in this chapter has been published in the paper:

[145] **A. Ruffino***, Y. Peng*, T.-Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba and E. Charbon, "A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots," accepted and to appear in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, February 2021.

In this work, I conceived the architecture and designed the receiver, while the co-integrated frequency synthesizer has been conceived and designed by Yatao Peng, a colleague in AQUA laboratory, then I performed the measurements with him and I wrote the manuscript.

9.1 Introduction

Recently, important milestones have been reached by integrated classical electronics for qubit control, with the demonstration of fully-integrated control of spin qubits [110, 111] and transmons [108, 109] implemented in a cryo-CMOS technology operating at 1-4 K. Moreover, simple cryo-CMOS circuits have been co-integrated with quantum dots in FDSOI technology [54], but a fully-integrated readout circuit has not yet been addressed in the literature.
Some attempts have focused on integrated RF architectures for sub-THz qubit readout [176], but have only been demonstrated at 300 K, thus reducing the usefulness of an integrated circuit solution. Moreover, plenty of knowledge is available in the field of cryogenic radio-astronomy receivers [177], that could be transferred to qubit readout and exploited to realize a cryogenic qubit receiver.
To complement the achievements of qubit control, this chapter presents the first fully-integrated cryo-CMOS System on Chip (SoC) with a receiver and frequency synthesizer for scalable multiplexed RF reflectometry readout of qubits [145].
This chapter represents the conclusion of the work presented throughout this thesis and collects circuits presented in the previous chapters, as it describes the co-integration of

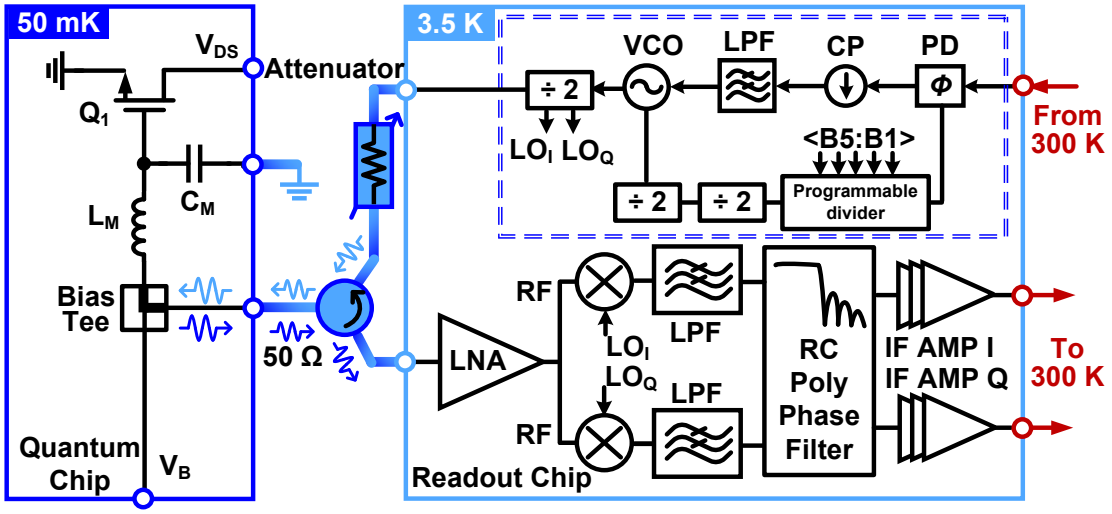

Figure 9.1 – General block diagram of the proposed I/Q receiver with frequency synthesizer and its application to RF reflectometry of integrated quantum dots.

a receiver based on the LNA design detailed in Chapter 8, with a frequency synthesizer built around the VCO described in Chapter 8, and its goal is to be able to read out the quantum-classical interface matrix described in Chapter 5.

9.2 Circuit design and architecture

An in-phase/quadrature receiver with on-chip phase-locked loop operating at 5-6.5 GHz is proposed, for phase-sensitive readout of qubit signals at 3.5 K.
The choice of the operating RF band comes from the fact that, so far, as described in Chapter 5 and Chapter 8, gate-based readout has been performed typically below 1 GHz [18], preventing integration of *LC* matching networks, especially for a scalable, multiplexed approach. However, higher frequency operation, for example in the 5-6.5 GHz band, can lead to more compact and sensitive *LC* resonant circuits [117], facilitating co-integration with quantum devices. Wide bandwidth is chosen for frequency-multiplexed readout and a non-zero intermediate frequency down-conversion is proposed to suppress the effects of flicker noise at cryogenic temperatures. Image Rejection (IR) is implemented for in-band noise reduction and I/Q outputs for direct phase measurement. For scalability reasons, and differently from what previously done for qubit control [108, 109, 110, 111], a PLL is integrated on chip for frequency generation.
The proposed receiver and PLL block diagram is shown in Figure 9.1, while the details of the main blocks are shown in Figure 9.2.
The general receiver architecture is structured as follows: an LNA at the input directly amplifies the high-frequency weak qubit signal, which is then quadrature down-converted to non-zero intermediate frequency, generating sum and difference frequency. The sum frequency is implicitly low-pass filtered at the output of the mixers, then a complex I/Q polyphase network rejects the noise coming from the image band (which is also amplified within the LNA), and then finally I and Q signals are amplified independently, to allow

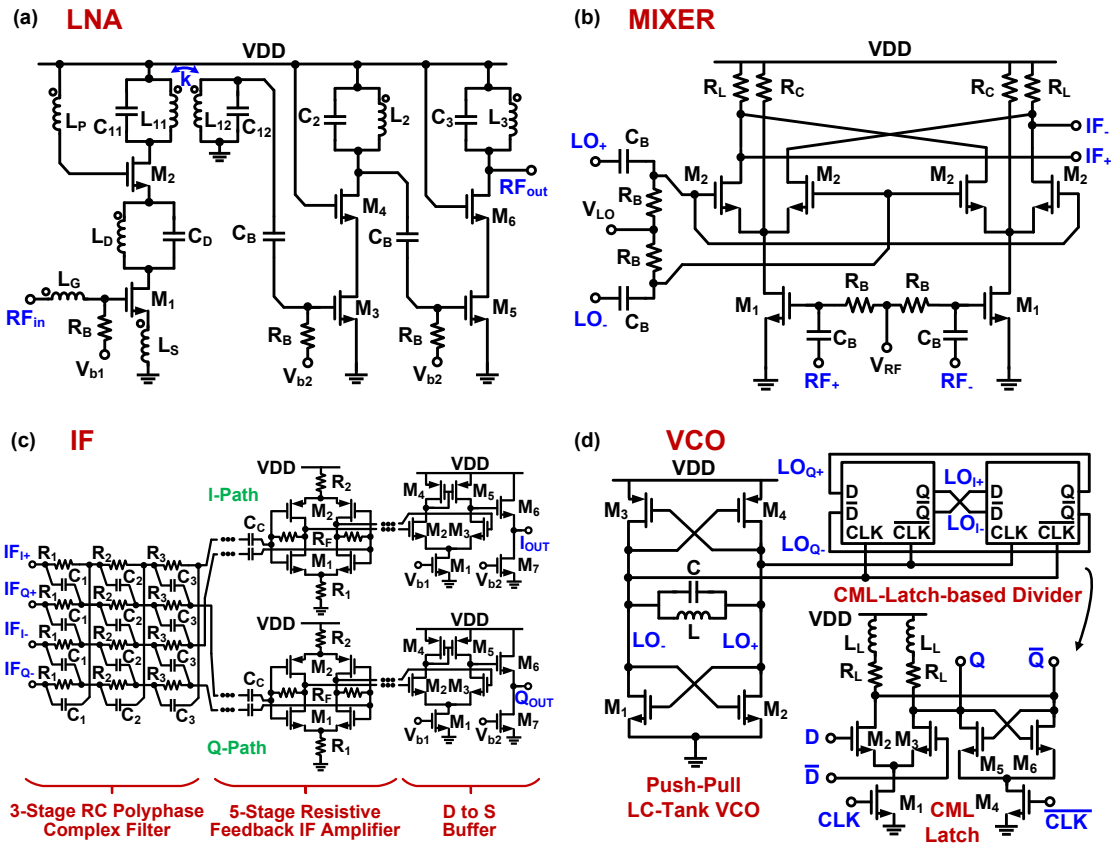

Figure 9.2 – Detailed schematic of the main blocks for the proposed cryo-CMOS I/Q non-zero IF receiver and PLL. (a) Low-noise amplifier, (b) mixer, (c) intermediate-frequency chain, (d) voltage-controlled oscillator and I/Q generation.

amplitude and phase retrieval.

The receiver front-end consists of a wideband LNA, described in Chapter 8, implemented as a single-ended inductively degenerated common-source stage with cascode and *LC* tank load for optimal input and noise impedance, and transformer-coupled cascaded gain stages, as shown in Figure 9.2 (a). The LNA achieves a 40-dB gain in a band between 4.5 GHz and 8.5 GHz, which is planned to extend the receiver bandwidth in a future implementation with a second IF path using low-side injection and swapping gain and image bands.

A transformer balun performs single-ended to differential conversion and is connected to a single-quadrature I/Q differential mixer for Single Side-Band (SSB) down-conversion, implemented as two Gilbert cell active mixers, with resistor current bleeding for increased voltage headroom at cryogenic temperature, as shown in Figure 9.2 (b). The mixer is driven by a differential quadrature local oscillator at 6.4 GHz, to obtain a 0.1-1.5 GHz IF with a 4.9-6.3 GHz RF input signal.

The mixer is followed by a 3-stage *RC* passive complex Poly-Phase Filter (PPF) for wideband > 20-dB Image Rejection Ratio (IRR). This circuit is followed by a wideband, 5-stage IF I/Q 30-dB gain amplifier chain formed by differential inverter-based resistive feedback amplifiers, as shown in Figure 9.2 (c). The IF amplifiers have common mode resistors to

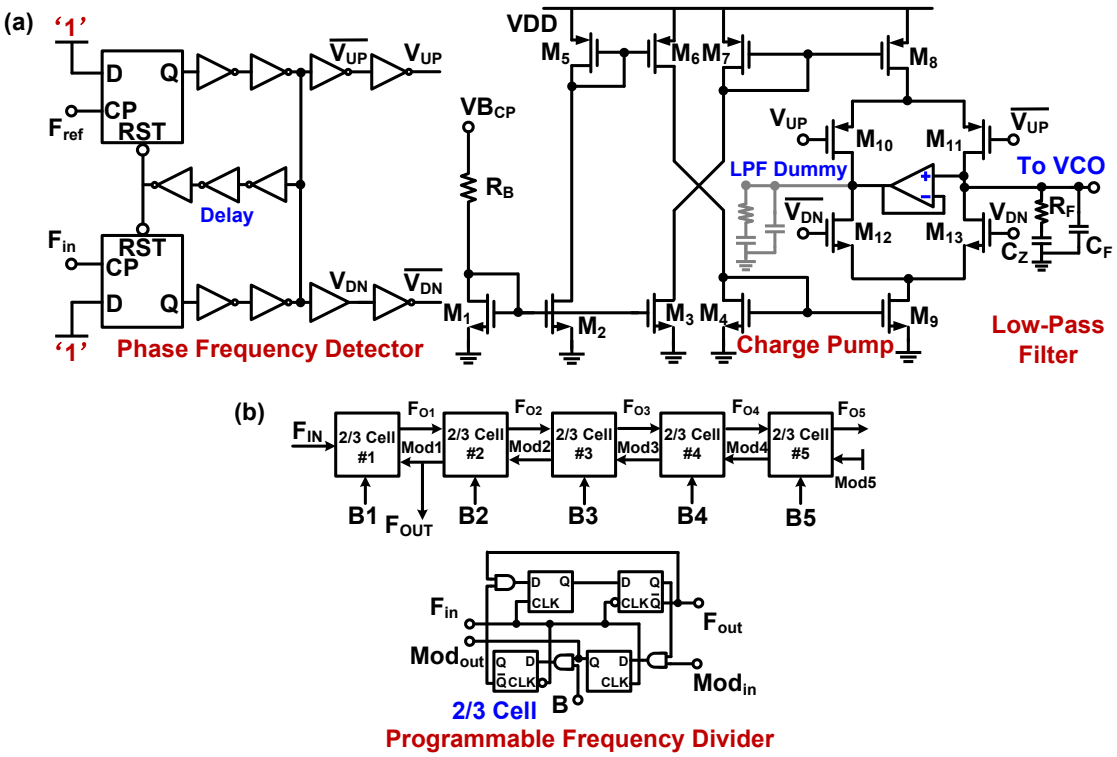

Figure 9.3 – Extra circuit implementation details for the PLL, showing (a) the phase-frequency detector, the charge pump, the low-pass filter and (b) the programmable frequency divider.

ground and supply, to increase the Common Mode Rejection Ratio (CMRR), which helps to suppress the LO leakage. They are designed with a distributed gain-bandwidth product, by means of a scaled-up gain, and the IF bandwidth is determined by a controlled output *RC* time constant, rather than by explicit filtering, to merge functions and save power. Finally, there is a differential-to-single-ended buffer for 50 Ω output match.

In a future implementation, the IF amplifier chains can be followed directly by high-speed ADCs and a Digital Signal Processor (DSP) for baseband down-conversion in the digital domain, avoiding flicker noise (at the cost of increased power consumption).

The LO signal for down-conversion is generated on-chip by an analog charge-pump integer-N PLL built around a 12.8 GHz *LC* voltage-controlled oscillator, described in Chapter 8, followed by a Current-Mode Logic (CML) divider by 2, to generate a 6.4 GHz quadrature signal, as shown in Figure 9.2 (d). The VCO is tunable between two bands in a range between 10.5 GHz and 16.5 GHz, thus resulting in an LO signal that can be tuned between 5.25 GHz and 8.25 GHz. The divider by 2 is a CML-latch based divider, with resistive-inductive load, to increase the operating bandwidth.

The PLL is formed by a Phase-Frequency Detector (PFD), a Charge Pump (CP) and an *RC* Low-Pass Filter (LPF), and it uses a 5-bit programmable divider to ensure locking range to the reference clock. The implementation details are shown in Figure 9.3 (a), (b). The PFD is realized by two edge-triggered, resettable D flip-flops, while the CP is balanced, to reduce mismatch and charge injections and the LPF sets the PLL bandwidth to 1.5 MHz, while a dummy LPF balances the two paths.

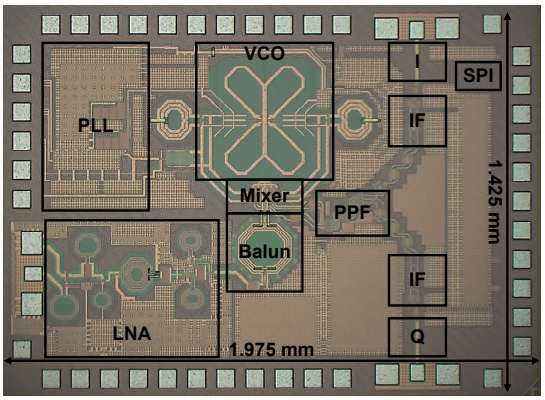

Figure 9.4 – Die micrograph of the 40-nm cryo-CMOS fully-integrated receiver and frequency synthesizer.

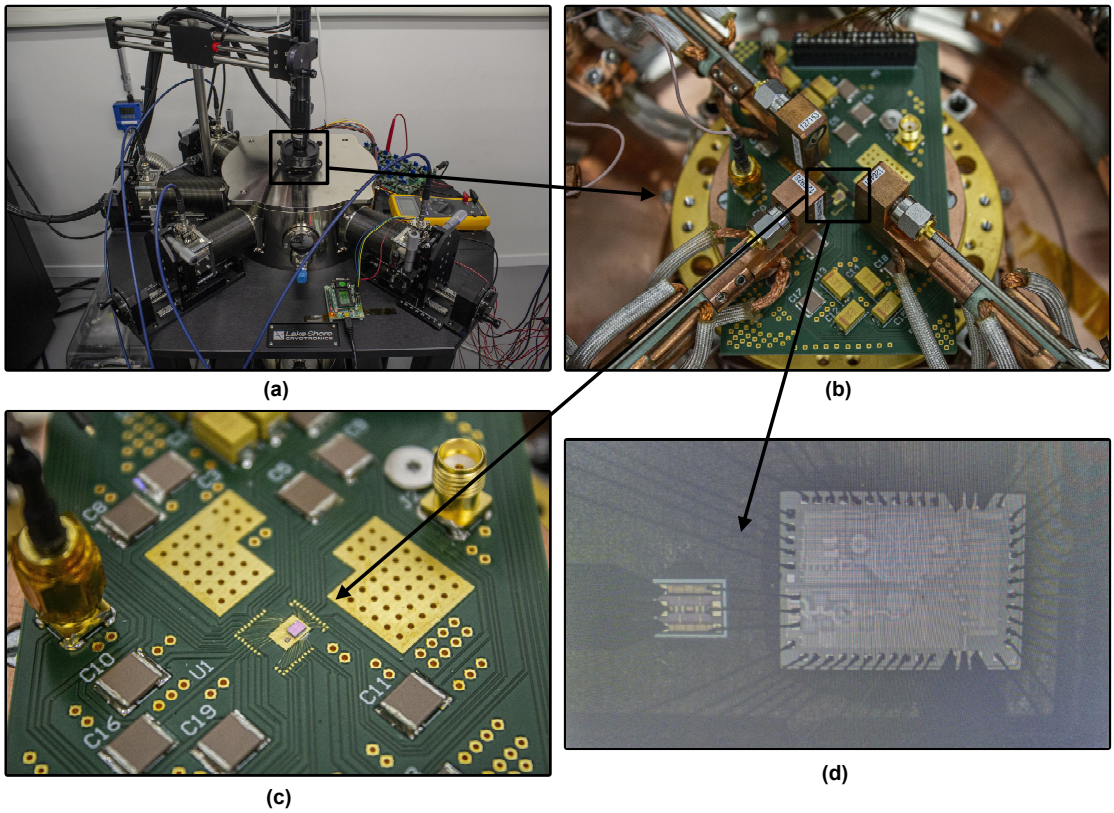

Figure 9.5 – Measurement setup with (a) cryogenic probe station, (b) printed circuit board, (c) chip-on-board bonding and (d) wafer probing with GSG probes.

Moreover, there is also a digital part, which is used to give flexibility to the presented architecture. A serial-to-parallel interface is used for digital control and tunability of the VCO and programmable divider during testing, as it allows to switch oscillating modes, VCO tuning bits and loop division ratio.

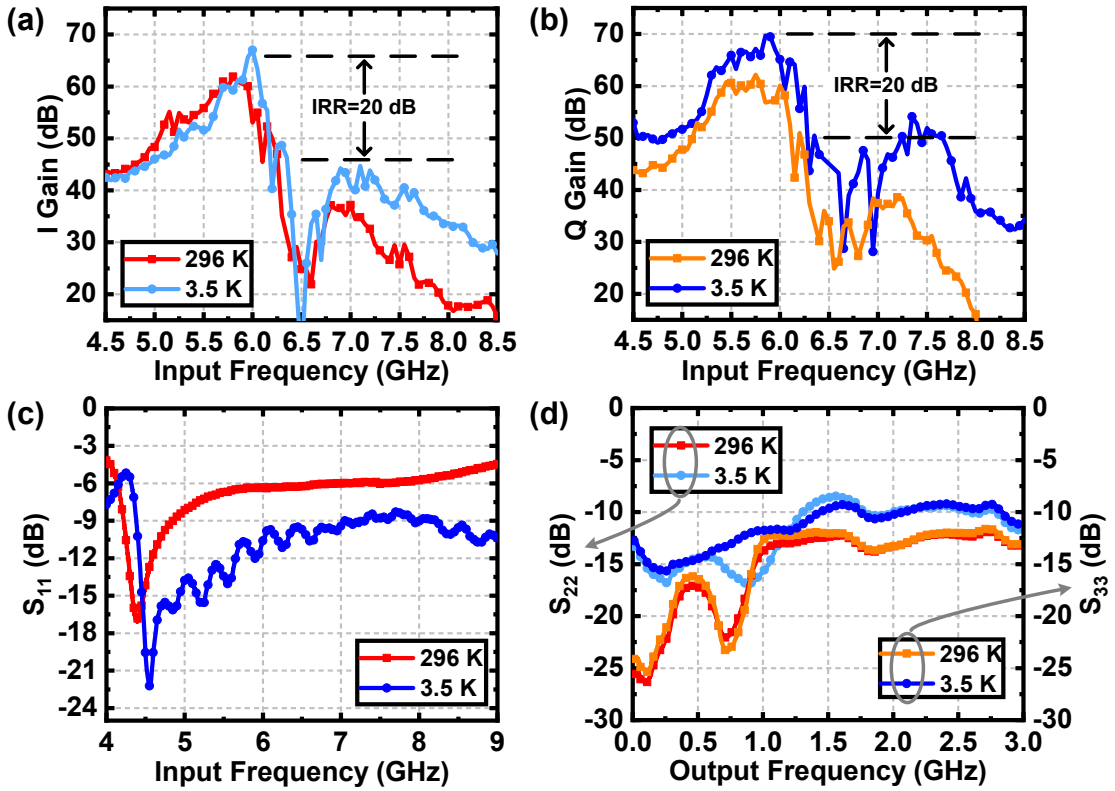

Figure 9.6 – Measured (a) I conversion gain and (b) Q conversion gain, (c) input match and (d) output match of the receiver at 296 K and 3.5 K.

9.3 Measurements

The proposed SoC has been implemented in a standard 40-nm CMOS technology. The chip micrograph is shown in Figure 9.4, with its main blocks highlighted. The chip has been measured at 296 K and cooled down to 3.5 K for performance evaluation with GSG probing in a Lake Shore CRX-4K cryogenic probe station. The measurement setup is shown in Figure 9.5.

At 296 K, the circuit shows a maximum 60 dB I/Q conversion gain, with a 1.1 GHz bandwidth, and an average 20 dB image rejection ratio, while the input and output match is better than −6 dB, as shown in Figure 9.6.

At 3.5 K, the circuit exhibits a 70 dB maximum I/Q conversion gain and a better than −10-dB input and output match, as shown in Figure 9.6. The bandwidth is 1.4 GHz, between 100 MHz and 1.5 GHz of IF frequency, due to the chosen non-zero IF architecture. An average IRR of 20 dB is achieved.

The circuit is designed to operate with a ∼ −100-dBm input signal reflected by the qubits. The small signal non-linearity is measured at the center band of the receiver, at 650 MHz IF frequency, with two-tones having 1 MHz spacing, performing a power sweep. At 3.5 K, a third order input intercept point of −68 dBm is obtained, as shown in Figure 9.7 (a), sufficiently far from the operational region, and largely limited by the 50 Ω output driver non-linearity.

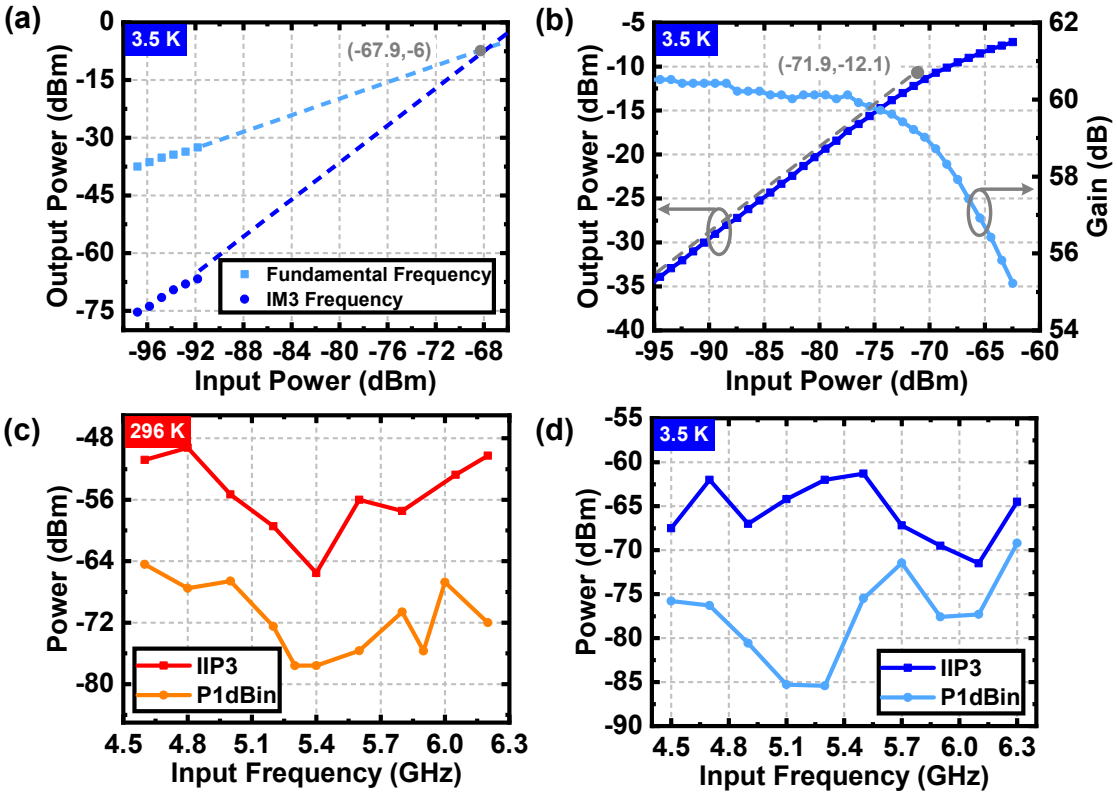

Figure 9.7 – Measured receiver (a) small signal non-linearity (IIP3, OIP3) and (b) large-signal non-linearity ($P_{1\text{dBin}}$, $P_{1\text{dBout}}$) versus power at 3.5 K. Measured receiver IIP3 and $P_{1\text{dBin}}$ versus frequency (c) at 296 K and (d) at 3.5 K.

Subsequently, the large-signal non-linearity is measured at the center of the receiver bandwidth, namely 650 MHz IF frequency, performing a power sweep. At 3.5 K, the obtained 1-dB input compression point ($P_{1\text{dBin}}$) is -72 dBm, as shown in Figure 9.7 (b). Also in this case, the obtained value still allows operation in the required range and it is limited by the 50 Ω output driver compression point $P_{1\text{dBout}}$.

IIP3 and $P_{1\text{dBin}}$ are also measured across the whole receiver bandwidth performing a frequency sweep, both at 296 K (Figure 9.7 (c)) and 3.5 K (Figure 9.7 (d)). The IIP3 is better than -64 dBm across the band at 296 K, while it is better than -72 dBm over the whole bandwidth at 3.5 K. On the other hand, $P_{1\text{dBin}}$ is measured to be > -76 dBm across the band at 296 K, while it becomes > -85 dBm over the receiver bandwidth at 3.5 K. All such values stay within the operational bounds.

Subsequently, the SSB noise figure of the receiver is measured with a cold-attenuator wire-bonded to the receiver input at 3.5 K, as shown in Figure 9.5 (d), and scalar NF measurements are performed, as shown in Figure 9.8.

The minimum NF is 0.55 dB, with degradation at low and high frequency, where the limited bandwidth of the PPF achieves less efficient image noise rejection. Separate noise measurements of the LNA alone, in Chapter 8, confirm compatible results for the noise figure, thus showing that the LNA gain is enough to suppress any subsequent stage noise, the image-reject architecture allows enough noise rejection from the 6.5-8 GHz image

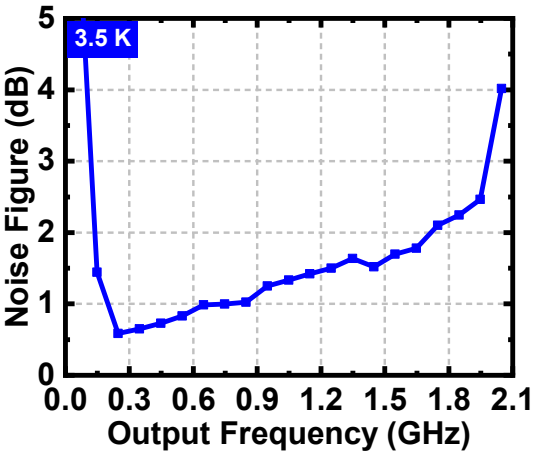

Figure 9.8 – Measured noise figure of the receiver at 3.5 K.

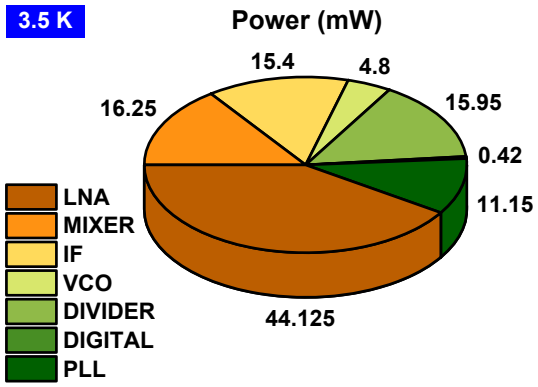

Figure 9.9 – DC power consumption per block at 3.5 K.

band and the phase-locked loop noise at cryogenic temperature does not increase the receiver noise floor considerably.

Nonetheless, given the stringent noise requirements of semiconductor qubit readout, the achieved noise figure might not be sufficient for direct qubit readout, requiring long integration times to achieve a good signal-to-noise ratio. Consequently, the achieved noise figure should be improved in a future design, or an additional (discrete) cryogenic preamplifier could be used in front of the current receiver.

The VCO output phase noise at 3.5 K with a 12.7 GHz fundamental is -115 dBc/Hz at 1 MHz offset from the carrier, and -145 dBc/Hz in the noise floor region, as shown in Chapter 8.

The power consumption per block at 3.5 K is shown in Figure 9.9, and the overall power consumption is 108 mW.

Finally, the time-domain performance of the receiver is evaluated by acquiring the real-time I/Q outputs at 3.5 K, with an external oscilloscope, obtaining a phase imbalance of 6°, as shown in Figure 9.10 (a).

The phase sensitivity is then measured directly by sending a linear Amplitude Modulated (AM) and Phase Modulated (PM) signal at the receiver input at 3.5 K with a vector signal generator, and measuring the I/Q output waveforms in the time-domain, sampling them with a high sampling rate oscilloscope and reconstructing the baseband signals with digital signal processing off-chip at 296 K. As shown in Figure 9.10 (b), the receiver is capable of amplifying and down-converting the input signal, while the demodulated waveforms track amplitude and phase of the input signal in the I/Q polar constellation diagram.

The overall circuit consumes 108 mW with a 1.4 GHz bandwidth. Considering a 10 MHz bandwidth for each qubit, which allows readout in the time-domain faster than the qubit decoherence time, and 10 MHz spacing for each qubit, the proposed system allows frequency-multiplexed readout of up to 70 qubits, resulting in 1.5 mW/qubit power consumption.

The proposed SoC was designed for spin qubit readout, but it could also be used for superconducting qubits, thanks to its operating frequency range.

A comparison with state-of-the-art integrated circuits for qubit readout and high perfor-

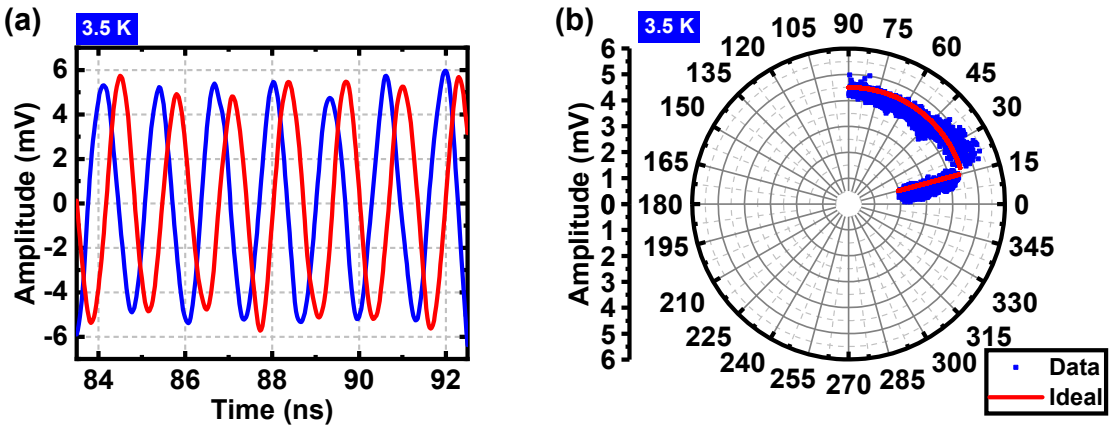

Figure 9.10 – (a) Time-domain I/Q signals at 3.5 K and (b) derived I/Q constellation plot for linearly amplitude modulated and phase modulated input signals, showing tracking in the I/Q plane at 3.5 K.

mance cryogenic receivers is shown in Table 9.1. Previous work addressing integrated qubit readout has focused on DC readout techniques based on transimpedance amplifiers [54]. This configuration resulted in smaller power consumption, allowing operation at lower temperature, but lacked the possibility to scale through multiplexing approaches. Alternatively, RF readout has been proposed at much higher frequencies, close to THz [176], resulting however in highly insufficient noise figure performance and extreme power consumption, furthermore without actual functionality verification at cryogenic temperature. Finally, when compared to high-performance cryogenic receivers for radio-astronomy applications [177], the designed receiver performs well in terms of gain and noise. Therefore, it is evident from literature that the proposed receiver is actually the first fully-integrated receiver with frequency synthesizer dedicated to the scalable readout of silicon qubits.
As an application for the presented receiver, the readout of the quantum-classical matrix described in Chapter 5 is proposed. The combination of such platforms, thanks to its compactness, integration and scalability, could form the basis of future silicon quantum computing systems.

9.4 Conclusion

In this chapter, the realization of the fully-integrated readout vision advocated in this thesis was presented.
As a result, the first single-chip cryogenic CMOS system-on-chip with receiver and frequency synthesizer operating at 3.5 K for gate-based readout of semiconductor quantum dots was presented.
The receiver operates at 3.5 K in a frequency range between 5-6.5 GHz, with a maximum conversion gain of 70 dB, a minimum noise figure of 0.55 dB, and it consumes 108 mW, allowing frequency-multiplexed readout of 70 qubits with 1.5 mW/qubit power consumption.
The work presented here represents the conclusion of this thesis, as it collects and inte-

	This work	[54]	[176]	[177]
Operating temperature	3.5 K	0.11 K	300 K	100 K
Qubit platform	*Spin qubits*, transmons	Silicon quantum dots	Si/SiGe spin qubits	N.A. (Radio astronomy)
Architecture	Non-zero IF I/Q receiver	DC TIA readout	Intermediate IF I/Q down-converter	Discrete receiver
System	Full receiver, PLL	Double quantum dot, VCO, TIA	Down-converter, VCO, divider	Antenna, LNA, feedthroughs
RF Frequency	5-6.5 GHz	DC	240 GHz	0.4-3 GHz
Bandwidth	1.4 GHz	1.1 kHz	59 GHz	2.6 GHz
Gain	70 dB	[1] 11.3 MΩ	23 dB	34 dB
Input/output match	<-10 dB	N.A.	<-5 dB	N.R.
Noise figure	0.55 dB	[2] 300 fA/$\sqrt{\text{Hz}}$	24.5 dB	0.5 dB
IIP3	>-72 dBm	N.R.	N.R.	N.R.
P1dBin	>-85 dBm	N.R.	>-27.3 dBm	N.R.
Phase noise at 1 MHz offset	-115 dBc/Hz	N.R.	-82 dBc/Hz	N.A.
VCO tuning range	6 GHz	4 GHz	27 GHz	N.A.
Technology	40-nm CMOS	28-nm FDSOI	55-nm SiGe	GaAs HEMT, discrete
Area	2.8 mm^2	[3] 1.4 mm^2	1.8 mm^2	>1 m^2
Power consumption	108 mW	295 µW	859 mW	N.R.

[1]Transimpedance amplifier gain, [2]Input referred noise, [3]Estimated from chip micrograph.

Table 9.1 – Comparison table with state-of-the-art circuits for qubit readout and high performance cryogenic receivers.

grates the results described in the previous chapters, realizing the proposal presented in the initial part.
The knowledge of the cryogenic behavior of transistors, presented in Chapter 3, and the study of integrated passives at low temperature, described in Chapter 4, contributed to the design choices in this receiver, while the low-noise amplifier and voltage-controlled oscillator presented in Chapter 8 are an integral part of the design itself. Moreover, this receiver is proposed to read out, thanks to the circulator presented in Chapter 7, the quantum-classical matrix presented in Chapter 5, which in turn benefited from the realization of integrated quantum devices in CMOS shown in Chapter 2, and from the low-frequency multiplexers presented in Chapter 6.
The final realization of this work is the combination of all the presented blocks in a single system.

10 Conclusions

10.1 Outlook

The realization of quantum computers promises to revolutionize the computational possibilities available to us, with an exponential speed-up of certain algorithms over the classical counterpart, opening new avenues in chemical synthesis, cryptography, and supercomputing.
A quantum computer, however, is an extremely complex system, requiring the co-existence and co-operation of a large number of blocks. The quantum processor is its fundamental part, and in its currently most promising solid-state implementations, as superconducting or spin qubits, it requires low-temperature operation. On the other hand, a large electronic infrastructure is required to read-out and control the quantum processor, and it is currently implemented mostly as discrete components and instruments at room temperature.
For the realization of a scalable fault-tolerant quantum computer, it is expected that millions of qubits will be required, therefore, not only the quantum processor complexity will increase, but also the corresponding readout and control electronics. In order to achieve this goal, the current approach is not viable and the two worlds, the quantum processor and the electronic infrastructure, will need to meet mid-way. On one side, qubits should possibly be operated at higher temperatures (1-4 K) and on the other side, electronics should be integrated and operated directly at cryogenic temperatures, with the final goal to co-integrate the two layers on the same chip, and possibly in the same technology.
For this reason, in the thesis, cryo-CMOS integrated circuits for qubits have been investigated, with a particular focus on the readout of spin qubits.
In the context of the quantum world, silicon-based CMOS quantum dots have been explored as a solution to realize quantum devices in standard technology allowing to be co-integrated with classical electronics, and also operated at higher cryogenic temperatures.
In the context of classical electronics, integrated circuits in standard CMOS technology have been proposed for operation directly at cryogenic temperatures. The thesis has explored cryogenic modeling for active and passive devices, and has mostly focused on the design of wideband, low-power, low-noise cryogenic CMOS radio-frequency integrated circuits for scalable readout of silicon quantum processors, establishing a complete infrastructure, going from a fully-integrated quantum-classical multiplexing interface, through a circulator and a low-noise receiver operating at cryogenic temperatures.

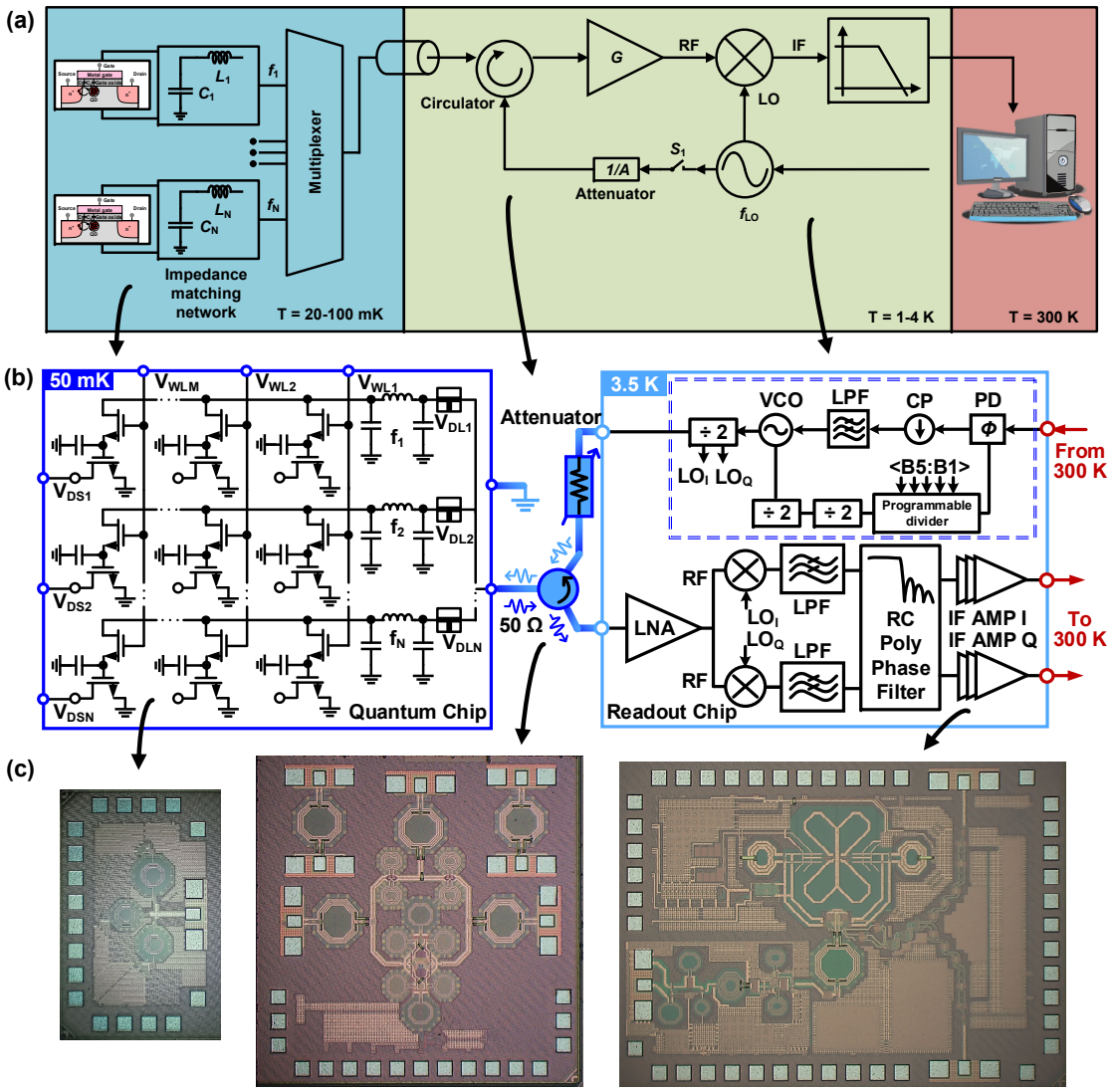

Figure 10.1 – (a) Proposal, (b) implementation and (c) realization of the fully-integrated gate-based readout platform proposed in this thesis.

10.2 Thesis outcome

Within the presented context, the main results achieved in this thesis are the following. Quantum dots in standard bulk CMOS technology have been realized in minimum size MOSFETs and their properties have been described in Chapter 2. This is the first realization of quantum dots in a standard bulk CMOS deep-sub-micron node. Such quantum dots show regular Coulomb oscillations at 50 mK and they are quite reproducible in terms of variability.

Characterization and modeling of active devices, namely CMOS transistors, has been investigated at deep cryogenic temperatures (50 mK) and cryogenic temperatures (4.2 K) in Chapter 3. As expected, the transistor's threshold voltage increases, subthreshold swing

improves and transconductance also increases. This presents a rough understanding of the DC behavior of MOSFETs in advanced technology nodes at low temperature and allows first insights into the change of typical analog/RF design parameters for circuit designers.
The first accurate characterization of on-chip passive devices (capacitors, inductors, transformers) in bulk CMOS at 4.2 K has been described in Chapter 4, providing lumped element models and EM models, used to allow predictive integrated circuit designs. The developed models could successfully reproduce the performed measurements on capacitors, inductors and transformers, and were used to validate the circuit designs described in the subsequent chapters.
The realization of a quantum-classical integrated circuit co-integrating quantum dots, transistors and passive resonators operating at 50 mK was described in Chapter 5. It presents a new matrix, based on a DRAM-like scalable architecture and it demonstrates, for the first time, fully-integrated gate-based dispersive readout at 6-8 GHz, time-, frequency- and the combined time-and-frequency multiplexed readout of silicon quantum dots. The presented architecture contains, in a nutshell, all the features for a scalable co-integrated readout.
Additionally, low-frequency time-multiplexers have been presented in Chapter 6, to be used for low-temperature sequential switching schemes.
A new cryogenic CMOS circulator has been presented in Chapter 7, and thanks to an innovative all-pass filter architecture, it allows to enhance the circuit bandwidth, while reducing power consumption and insertion loss. This represents the first proposal for a fully-integrated cryogenic circulator in standard CMOS technology.
A low-noise amplifier and *LC*-tank voltage-controlled oscillator have been presented and characterized in Chapter 8, and they meet the requirements derived for gate-based dispersive qubit readout.
Finally, in Chapter 9, a complete system has been designed, by combining the results of the previously designed amplifier and oscillator to realize a fully-integrated cryogenic CMOS low-noise receiver with frequency synthesizer operating at 3.5 K between 5-6.5 GHz for the readout of silicon qubits.
This is the first fully-integrated readout circuit for spin qubits and it completes the whole readout chain, going from the quantum layer, to the multiplexing interface, circulator, low-noise amplifier and down-conversion chain, to deliver an amplified I/Q wideband downconverted signal carrying the qubit information to room temperature.
Apart from the individual results presented in each chapter, the most important aspect of this thesis is the vision it intends to deliver, which consists in a fully-integrated cryogenic RF readout (and control) going from the quantum processor, across temperature boundaries, to the classical world at room temperature.
From this point of view, it is interesting to compare the *traditional scheme* for readout (and control) systems, presented in Chapter 1 in Figure 1.8, employing discrete components and room-temperature instruments, with the group-wide proposed *plan* shown in Chapter 1 in Figure 1.9, representing the single-chip integrated cryogenic RF transceiver vision, and observe how this was implemented in this thesis.
As one can see from Figure 10.1, the envisioned cryogenic transceiver plan was translated into a specific *proposal* (Figure 10.1 (a)), resulting in the choice of a clear readout technique, gate-based radio-frequency reflectometry, operating at higher readout frequencies, to allow extensive multiplexing and large absolute readout bandwidth, and of a dedicated

circuit architecture to allow sensitive and scalable readout. This was then translated into a specific circuit *implementation* (Figure 10.1 (b)), resulting in the circuit diagrams of the quantum-classical matrix, the circulator and the complete I/Q receiver with frequency synthesizer, and finally, resulted in the *realization* of the multi-chip system (Figure 10.1 (c)), covering, across different temperature regions, all the required blocks from the quantum world to the classical user interface.

10.3 Open problems

Despite advances and innovations proposed in this thesis, given the complexity of the final system, several open problems remain to be addressed.
In the quantum layer, quantum dots are proposed in bulk CMOS technology and implemented as minimum size transistors. This allows the realization of arrays of quantum dots in standard technology co-integrated with classical electronics, but it still does not allow to directly realize CMOS-standard *qubits*. The presented quantum devices behave as few-electron quantum dots, but they do not allow trapping of a single electron in the channel to encode quantum information in the single-electron spin. Moreover, the realization of a double quantum dot, to create a singlet-triplet qubit, is also not possible in the proposed fully-standard implementation. The reason is that two adjacent tunnel-coupled quantum dots with a single electron each would be required, thus demanding a very closely spaced short-pitch double-gate transistor, breaking standard design rules. Additionally, the realization of 2D arrays of interacting quantum devices, to perform quantum operations, would also require closely spaced short-pitch gates, which is not possible with current design rules.
A possible solution towards the ultimate goal of CMOS-standard qubits (instead of electron-beam gate-defined qubits) is the implementation of such structures in smaller technology nodes, where single-electron trapping in the channel is possible, but this should also be accompanied by customization of standard processes to make *new* standard cryo-CMOS processes. The creation of new technologies with tighter gate pitch would also address the requirements for the realization of 2D arrays of interacting quantum devices for quantum operations.
From the modeling point of view, apart from the basic DC characterization and EKV modeling presented in this thesis, several other aspects should be addressed to have a complete understanding of transistors at cryogenic temperatures. Small-signal AC and RF studies, noise and mismatch of single transistors should be accurately addressed in terms of characterization and modeling. Moreover, the realization of parametric lumped-element models for various types of capacitors, inductors and resistors available in standard design kits should be addressed, to allow the realization of a true cryogenic process design kit for predictive industry-level cryogenic circuit design. This is the next step required for the design of very complex scalable integrated cryogenic transceivers for qubit readout and control. Several early stage attempts have been initiated, but the realization of a complete unified model extending the temperature range of standard design kits is yet to come.
From the architectural point of view, the proposed DRAM-like quantum-classical interface allows to alleviate the scalability issue heavily with time- and frequency- multiplexing, but it would still be insufficient in the case of a post-Noisy Intermediate-Scale Quantum

(NISQ) processor, with millions of qubits, which would require arrays of $\sim 1000 \times 1000$ qubits. This would require having thousands of resonators on the same chip, which is currently not feasible, given their required inductance and therefore their size in standard technologies. Moreover, the quality factors available for such resonators are still too low for single-shot qubit readout in an error-corrected processor architecture. In order to address these issues, a possibility would be to try to integrate superconducting layers into standard CMOS processes and exploit the kinetic inductance of such layers in the superconducting state to realize very compact, high Q-factor spiral inductors for aggressive frequency multiplexing.
Moving along the chain, the circulator covers a very crucial role in the proposed overall architecture. Despite the innovation allowing to reduce power consumption, insertion loss and increase bandwidth (therefore allowing to read out more qubits), the presented circulator still cannot be operated at mK temperature, where its discrete counterparts are typically placed, because its power consumption is too high. Moreover, as shown in the noise measurements at 4.2 K, the noise-equivalent temperature of the circulator is still too high to be placed directly at the front of the readout chain, as it is, since clock feedthrough from the clock harmonics is too large. A possible solution to mitigate this could be to use harmonic-rejection mixers in the gyrator core, but this would further increase the power consumption, which still remains the most critical problem for the direct replacement of discrete circulators. The only viable approach for the proposed circulator remains a usage at 1-4 K, where enough cooling power is available, but with an increased noise figure and insertion loss with respect to direct mK operation.
Finally, for what concerns the fully-integrated receiver, despite the demonstrated functionality of such a complex system, performance improvements are still required. In order to achieve single-shot qubit readout, without the need for a preceding cryogenic amplifier, much lower noise figure is needed, then gain should also be increased and I/Q gain imbalance and phase imbalance should be reduced. Such improvements at cryogenic temperature can only come from the availability of more accurate models, allowing complete system simulations at cryogenic temperature during the design phase, which becomes much more critical when the number of interacting blocks gets larger.

10.4 Future work

Apart from addressing the mentioned open problems, each of which could be a specific research direction, the work presented in this thesis could be extended by addressing qubit control and trying to integrate both control and readout on the same chip.
Moreover, this thesis has a natural continuation, which consists in trying to accomplish experimentally the vision presented here, by measuring the described quantum-classical interface matrix with the designed low-noise receiver and try to reproduce the gate-based dispersive readout measurements performed with a discrete setup, now with a fully-integrated chip.
Several challenges lie ahead in the realization of such an experiment. The frequency range where the receiver has been proven to be functional during measurements (5-6.5 GHz) does not exactly match the frequency band of the designed resonators in the quantum-classical matrix (6.5-8 GHz), due to the non-ideal behavior of the complex SoC in its final

implementation. A possibility could be to exploit the wide tuning range of the on-chip frequency synthesizer to tune the local oscillator for down-conversion in such a way that the input RF band is shifted towards higher frequency for a constant IF frequency at the output, at the cost, however, of non-symmetrical gain and image bands in the image-reject architecture.
Moreover, the noise figure of the designed receiver, combined with the relatively low quality factor of the resonators, could be too high to allow readout of the weak reflectometry signal, while the gain of the fully-integrated chain could be too low. Additionally, the noise-equivalent temperature of the presented circulator could also be too high to be placed directly in front of the readout chain. For this reason, a discrete circulator and a discrete cryogenic amplifier could be still employed in front of the receiver to attempt such measurement.
Such experiment would be the completion of the vision presented in this thesis, showing the complete system working together, spanning from the quantum layer with an array of quantum dots, to the classical readout with the time-and-frequency multiplexing interface, the circulator and the low-noise receiver fully-integrated in a single deep-submicron standard CMOS technology and in just 3 chips, separated by the required temperature boundaries in the measurement setup.
It is a strong belief that the proposed and realized platform, and its subsequent improvements, thanks to compactness, integration and scalability, could form the basis of future silicon quantum computers.

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List of Publications

Journals

[J1] B. Patra, M. Mehrpoo*, **A. Ruffino***, F. Sebastiano, E. Charbon and M. Babaie, "Characterization and Analysis of On-Chip Microwave Passive Components at Cryogenic Temperatures," *IEEE Journal of the Electron Devices Society (JEDS)*, vol. 8, pp. 448-456, April 2020.

[J2] **A. Ruffino**, Y. Peng, F. Sebastiano, M. Babaie and E. Charbon, "A Wideband Low-Power Cryogenic CMOS Circulator for Quantum Applications," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 55, no. 5, pp. 1224-1238, May 2020.

[J3] T.-Y. Yang, **A. Ruffino**, J. Michniewicz, Y. Peng, E. Charbon and M. F. Gonzalez-Zalba, "Quantum Transport in 40-nm MOSFETs at Deep-Cryogenic Temperatures," *IEEE Electron Device Letters (EDL)*, vol. 41, no. 7, pp. 981-984, July 2020.

[J4] Y. Peng, **A. Ruffino**, and E. Charbon, "A Cryogenic Broadband Sub-1 dB NF CMOS Low Noise Amplifier for Quantum Applications," under revision in *IEEE Journal of Solid-State Circuits (JSSC)*, December 2020.

[J5] **A. Ruffino***, T.-Y. Yang*, J. Michniewicz, Y. Peng, E. Charbon^{+} and M. F. Gonzalez-Zalba^{+}, "Integrated multiplexed microwave readout of silicon quantum dots in a cryogenic CMOS chip," submitted to *Nature*, arXiv:2101.08295 [quant-ph], January 2021.

Conference Proceedings

[C1] A. Beckers, F. Jazaeri, **A. Ruffino**, C. Bruschini, A. Baschirotto, and C. Enz, "Cryogenic Characterization of 28 nm Bulk CMOS Technology for Quantum Computing," *2017 IEEE European Solid-State Device Research Conference (ESSDERC)*, Leuven, September 2017.

[C2] **A. Ruffino**, Y. Peng, and E. Charbon, "Interfacing Qubits via Cryo-CMOS Front Ends," *2018 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Beijing, November 2018.

[C3] **A. Ruffino**, Y. Peng, F. Sebastiano, M. Babaie, and E. Charbon, "A 6.5-GHz Cryogenic All-Pass Filter Circulator in 40-nm CMOS for Quantum Computing Applications," *2019 IEEE Radio-Frequency Integrated Circuits Symposium (RFIC)*, Boston, June 2019.

[C4] Y. Peng, **A. Ruffino**, and E. Charbon, "Analysis on Noise Requirements of RF Front-End Circuits for Spin Qubit Readout," *2019 International Conference on Noise and Fluctuations (ICNF)*, Neuchâtel, June 2019.

[C5] **A. Ruffino***, Y. Peng*, T.-Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba and E. Charbon, "A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots," accepted and to appear in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, February 2021.

Conference Talks/Posters

[O1] **A. Ruffino**, M. Babaie, F. Sebastiano, and E. Charbon, "Cryo-CMOS Circulators for Spin and Superconducting Qubits," *2017 Silicon Quantum Electronics Workshop*, Portland, August 2017.

[O2] **A. Ruffino**, Y. Peng, and E. Charbon, "Cryo-CMOS Circuits for Spin and Superconducting Qubits," *2018 Silicon Quantum Electronics Workshop*, Sydney, November 2018.

Chip Gallery

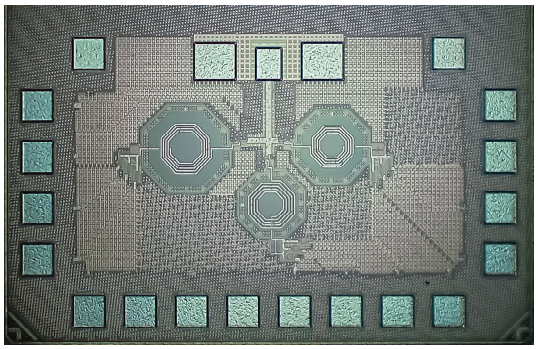

Figure A.1 – Quantum-classical matrix in 40 nm.

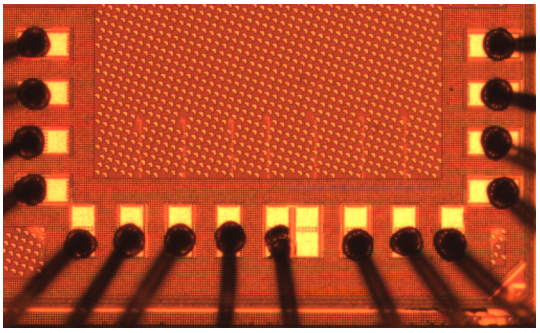

Figure A.2 – Cryogenic CMOS multiplexers in 40 nm.

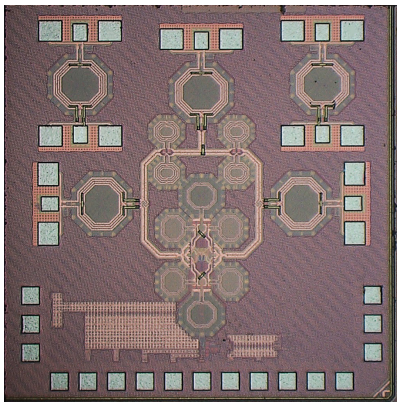

Figure A.3 – Cryogenic CMOS circulator in 40 nm.

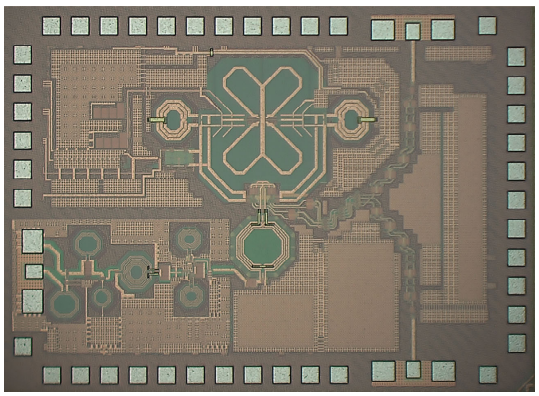

Figure A.4 – Cryogenic CMOS receiver in 40 nm.

Andrea Ruffino

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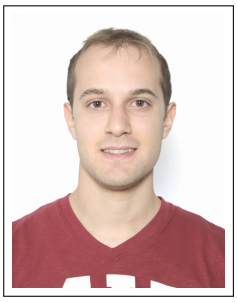

Experience

2016–present **EPFL**
Doctoral Assistant

2017–2018 **TU Delft**
Visiting Doctoral Assistant
- Research on cryogenic CMOS analog and RF integrated circuits for quantum computing applications
- Study, design, tape-out and measurement of low power, low noise, wideband integrated circuits and systems for qubit readout and control

2015–2016 **HYPRES, Inc.**
Integrated Circuit Designer/Intern/Master's Thesis
- Design of a superconducting digital readout circuit for superconducting nanowire single photon detectors

June 2014–August 2014 **Max-Planck-Institut für Quantenoptik**
Assistant Engineer/Summer Intern
- Study of the electron photoemission from metallic nanotips exposed to intense laser pulses

Education

2016–present **EPFL**
Ph.D. in Microsystems and Microelectronics
Thesis title: "Cryogenic CMOS Integrated Circuits for Scalable Readout of Silicon Quantum Computers"

2014–2015 **Politecnico di Torino, Grenoble INP, EPFL**
Joint Triple Master Degree in Micro and Nanotechnologies for Integrated Systems
Grade: 110/110 cum laude
Thesis title: "Superconducting Rapid Single-Flux Quantum read-out circuit for Superconducting Nanowire Single Photon Detectors"

2011–2013 **Politecnico di Torino**
Bachelor Degree in Engineering Physics
Grade: 110/110 cum laude
Thesis title: "Quantum effects in electronic devices: Single Electron Transistors and Josephson Junctions"

Competences

Training	Cryogenics, microwave measurements and low temperature engineering for quantum technology, Quantum Information in Condensed Matter Physics, Quantum Information Processing, Low Power Analog IC design, Advanced Analog IC Design, Ultra-Low Power RF Circuits for IoT, Wireless RF Front-End Design, Oscillators and PLLs, SERDES Design for Wireline and Optical Communications, High Performance Data Converters, Practical Aspects in Mixed Signal ICs
Measurement	Probe station, Cryostat, Dilution Fridge, Vector Network Analyzer, Vector Signal Generator, Spectrum Analyzer, Semiconductor Analyzer, Oscilloscope
Software	**Analog Design**: Cadence Virtuoso **RF Design**: Keysight ADS, Momentum, Sonnet **Digital Design**: Mentor Graphics ModelSim, Cadence Genus, Innovus, Synopsys Design Compiler, IC Compiler **Verification**: Cadence Assura, Mentor Graphics Calibre (DRC, LVS, PEX) **PCB Design**: Altium Designer FEM modeling: COMSOL, Ansys Other: Matlab, LabVIEW, Origin, Mathematica
Computer languages	HDL: VHDL, Verilog General: Skill, Tcl, Perl, C, C++, Bash, Csh, LaTeX, Python

Skills

Languages	**Italian** - Native **English** - Fluent **French** - Conversational **German** - Conversational

Awards and prizes

Papers	Best Student Paper Award Finalist at IEEE RFIC Symposium 2019
Achievements	IEEE Solid-State Circuits Society Predoctoral Achievement Award 2020-2021

Activities and interests

Academic activities	- Teaching assistant for Bachelor and Master courses - Reviewer for IEEE conferences and journals - Volunteer assistant for IEEE conferences ESSCIRC/ESSDERC 2016 and DATE 2017 in Lausanne
Sports	Football player for 15 years at regional level
Interests	Photography, Modern Literature, Philosophy