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A generalized EKV charge-based MOSFET model including oxide and interface traps

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ABSTRACT

This paper presents a generalized EKV charge-based MOSFET model that includes the effects of trapped charges in the oxide bulk and at the silicon/oxide interface. It is shown that in the presence of oxide- and interface-trapped charges, the mobile charge density can still be linearized but with respect to both the surface potential and the channel voltage. This enables us to derive closed-form expressions for the mobile charge density and the drain current. These simple formulations demonstrate the effects of charge trapping on MOSFET characteristics and crucial device parameters. The proposed charge-based analytical model, including the effect of velocity saturation, is successfully validated through measurements performed on devices from a 28-nm bulk CMOS technology. Ultrahigh total ionizing doses up to 1 Grad(SiO_2) are applied to generate oxide-trapped charges and activate passivated interface traps. Despite a small number of parameters, the model is capable of accurately capturing measurement results over a wide range of device operation from weak to strong inversion. Explicit expressions of device parameters also allow for the extraction of the oxide- and interface-trapped charge densities.

1. Introduction

The downscaling of CMOS technologies brings numerous benefits including higher speed, reduced power consumption, and extended functionality [1,2]. It also poses significant reliability challenges, partly due to hybrid gate dielectrics and imperfect material interfaces [1,3]. Two prominent reliability issues are bias-temperature instability and hot-carrier damage [4,5], both involving charge trapping in the oxide bulk and at the silicon/oxide interface. Apart from scaling-related reliability issues, high-energy ionizing radiation can generate electron–hole pairs in dielectrics and likewise contribute to charge buildup in the oxide bulk [6,7] and the activation of passivated interface traps [8,9]. Oxide- and interface-trapped charges can seriously degrade MOSFET characteristics and even cause circuit failures [10,11]. To better understand how oxide- and interface-charge trapping influences device performance and predict relevant degradation in harsh operating conditions, the effects of oxide- and interface-trapped charges have to be included in MOSFET models.

The voltage reduction resulting from CMOS scaling has progressively pushed the MOSFET operating point from strong inversion towards moderate and even weak inversion [12]. This brings new challenges to circuit designers for making optimal trade-offs among various design parameters and makes the simple threshold-voltage-based quadratic model, which has been in use since the development of the MOSFET in the 1960s, no more valid [13–15]. Pennsylvania State University and Philips Research have jointly developed an advanced surface-potential-based model, i.e., the PSP model, for nanoscale MOSFETs [16]. This model contains an accurate but complex description of the major physical effects responsible for the characteristics of nanoscale MOSFETs. Esqueda et al. have studied defect-related effects by introducing oxide- and interface-trapped charges into the surface potential equation and solving the surface potential with some techniques of the PSP model while inheriting its complexity [17].

The EKV MOSFET model, which is based on the mobile charge that directly relates the drain current, intuitively and physically describes device characteristics [18]. This charge-based model and its concept of

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inversion coefficient have demonstrated their effectiveness in describing large- and small-signal characteristics of MOSFETs in all inversion conditions [19,20]. The simplified EKV MOSFET model employs only a few parameters and much less complex formulas, which is advantageous for designers to explore the design space and identify the optimal operation before running more accurate simulations with the foundry-provided process design kits. In addition, the key of this simple model, together with its charge-related basis, is normalization, which strips off the dependence of voltage, temperature, and technology from the model by a few parameters and makes it suitable as a benchmark for CMOS technologies.

To extend this simplicity and efficiency to defect-related device modeling and support relevant circuit design with nanoscale CMOS technologies, we propose to incorporate oxide- and interface-trapped charges into the EKV charge-based MOSFET model. The simplicity of the original EKV MOSFET model strongly relies on the mobile charge linearization with respect to the surface potential. It is truly this crucial step that enables a simple formulation of the current as a function of the mobile charge density evaluated at the source and drain ends of the channel. Although these charges might seem quite abstract for designers, they are actually directly proportional to the transconductance, which is the most important parameter for circuit design [18]. It is therefore key to find out how to include the effects of oxide- and interface-trapped charges while still being able to linearize the mobile charge density. This is the focus of this paper.

This paper starts in Section 2 with a short review of oxide- and interface-charge trapping mechanisms and their various effects on MOSFET electrostatics. Section 3 is the central part of this work, where we show that the mobile charge density can still be linearized when including oxide- and interface-trapped charges. The generalized EKV charge-based MOSFET model that accounts for oxide- and interface-trapped charges is composed of two parts: one equation relating the mobile charge density to the terminal voltages in Section 4 and the other expressing the drain current versus the mobile charge density evaluated at the source and drain ends of the channel in Section 5. Nowadays in the nanoscale area, even a simple model needs to account for short-channel effects, among which velocity saturation is probably the most important. This is handled in Section 6. The proposed charge-based analytical model is finally validated in Section 7 against a 28-nm bulk CMOS technology with pre-radiation and radiation measurements of various MOSFETs up to 1Grad(SiO_2) of total ionizing dose (TID).

2. Oxide- and interface-charge trapping

2.1. General remarks on trapped charges

Interface traps above the neutral trap energy level E_0 are of acceptor type and below it are of donor type [21]. Depending on the trap energy level E_t with respect to the Fermi level E_F, interface traps can be positively or negatively charged or remain neutral. Assuming E_0 to be at the intrinsic Fermi level E_i, interface traps above it are acceptors (green circles in Fig. 1) and those below it are donors (blue circles in Fig. 1). An acceptor-like interface trap is negatively charged when accepting an electron if below the electron quasi-Fermi level E_{Fn} and electrically neutral when being empty if above it. A donor-like interface trap is positively charged when emitting an electron if above the hole quasi-Fermi level E_{Fp} and electrically neutral when being occupied if below it. In inversion, an *n*MOSFET has a negative interface-trapped charge contribution, while a *p*MOSFET has a positive counterpart, as shown in Fig. 1.

Integrating the interface-trap density per unit area per unit energy D_{it} and its corresponding Fermi–Dirac occupation probability $f(E_t) = 1/\{1+g_t\exp[(E_t-E_F)/kT]\}$ over the whole band-gap gives the interface-trapped charge density per unit area Q_{it}, where k is the Boltzmann constant, T is the absolute temperature, and g_t is the ground-state degeneracy factor. Under the non-equilibrium condition, E_F corresponds to

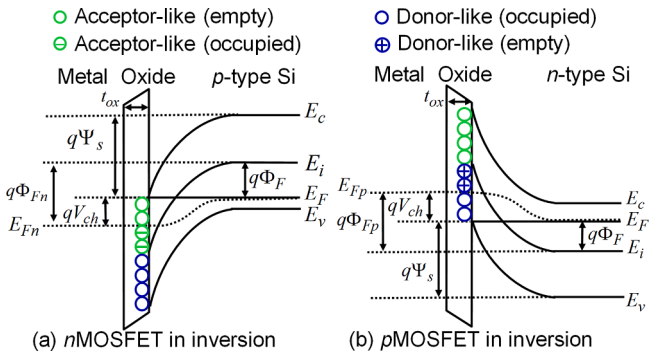

Fig. 1. Energy band diagrams illustrating interface-charge trapping in (a) a bulk *n*MOSFET and (b) a bulk *p*MOSFET in inversion. The quasi-Fermi level of the minority carriers, E_{Fn} or E_{Fp}, is split from that of the majority carriers E_F by the channel voltage V_{ch}.

the quasi-Fermi level. Unfortunately, this integral or even a discretized summation of single-trap energy levels cannot lead to a closed-form analytical solution [22]. To obtain a simple model for supporting circuit design while accounting for the effects of oxide- and interface-trapped charges, interface traps are assumed to be uniform across the band-gap and the occupation probability of the trap energy levels of interest is assumed to be unity. These assumptions have provided a direct link between defects and key device parameters while showing representative device behaviors of double-gate MOSFETs in [22]. They have also proven to be sufficient for describing defect-related effects and supporting circuit-level simulations [23]. Under these assumptions, Q_{it} can be expressed as [21–23]

$$Q_{it} = -q^2 D_{it}\left(\Psi_s - \Phi_F - V_{ch}\right), \tag{1}$$

where q is the elementary charge, Ψ_s is the surface potential, $\Phi_F = U_T\ln(N_b/n_i)$ is the Fermi potential, $U_T = kT/q$ is the thermal voltage, N_b is the channel doping concentration, n_i is the silicon intrinsic carrier concentration, and V_{ch} is the channel voltage equal to the source-to-bulk voltage V_{SB} at the source and the drain-to-bulk voltage V_{DB} at the drain.

Oxygen vacancies from incomplete oxidation can trap holes generated by total ionizing radiation or tunneling from the conductive channel [7,24]. Deep oxide-trapping centers generally do not interfere with the bias condition. Their slow charge-state transitions result in a fixed oxide-trapped charge density per unit area $Q_{ot} = qN_{ot}$, where N_{ot} is the oxide-trap density per unit area. Oxide-trapping centers near the silicon/oxide interface with energy levels close to the intrinsic Fermi level (i.e., border traps or switching oxide traps [25]) may respond promptly to external bias changes and therefore are included into interface traps for the following model development.

2.2. Impact of trapped charges on MOS electrostatics

We begin with a long-channel *n*MOSFET, for which the gradual channel approximation remains valid. Trapped charges are assumed to be in a charge sheet of negligible thickness at the oxide side of the silicon/oxide interface and hence do not need to be included in the Poisson's equation [26,27]. Solving the 1-D Poisson's equation for the total silicon charge density $Q_{si} = Q_m + Q_b$, subtracting the depletion charge density $Q_b = -\Gamma_b C_{ox}\sqrt{\Psi_s}$ solved from the charge-sheet approximation, and neglecting the hole contribution gives the mobile charge density per unit area Q_m, as (3.38) in [18]:

$$-\frac{Q_m}{C_{ox}} = \Gamma_b\left[\sqrt{U_T\exp\frac{\Psi_s-(2\Phi_F+V_{ch})}{U_T}+\Psi_s}-\sqrt{\Psi_s}\right], \tag{2}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate-oxide capacitance per unit area, ε_{ox} is the

gate-oxide permittivity, t_{ox} is the gate-oxide thickness, $\Gamma_b = \sqrt{2qN_b\varepsilon_{si}}/C_{ox}$ is the substrate modulation factor, and ε_{si} is the silicon permittivity. Note that neglecting the hole contribution makes this charge-based model invalid in the accumulation region.

Introducing oxide- and interface-trapped charges into the charge balance equation yields

$$Q_G + Q_f + Q_{si} = -\left(Q_{ot} + Q_{it}\right), \tag{3}$$

where $Q_G = C_{ox}V_{ox}$ is the gate charge density per unit area, $V_{ox} = V_{GB} - \Phi_{ms} - \Psi_s$ is the voltage drop across the gate oxide, V_{GB} is the gate-to-bulk voltage, Φ_{ms} is the metal-silicon work function difference, and Q_f is the fixed oxide-charge density per unit area. Substituting each charge contribution with its full expression and solving for the mobile charge density per unit area Q_m leads to

$$-\frac{Q_m}{C_{ox}} = V_{GB} - \left[V_{FB} + c_{it}\left(\Psi_s - V_{ch}\right) + \Psi_s + \Gamma_b\sqrt{\Psi_s}\right], \tag{4}$$

where $c_{it} \triangleq q^2 D_{it}/C_{ox}$ is the normalized interface-charge capacitance and will later link interface-trapped charges to the subthreshold swing. Here, V_{FB} is the flatband voltage defined under the equilibrium condition as the particular value of the gate-to-bulk voltage at which the silicon energy band is flat [17]:

$$V_{FB} \triangleq \Phi_{ms} - \frac{Q_f}{C_{ox}} - \left(\frac{qN_{ot}}{C_{ox}} + c_{it}\Phi_F\right). \tag{5}$$

Unfortunately, Eq. 2 and Eq. 4 cannot be reversed, making it impossible to solve the surface potential and the mobile charge density versus the terminal voltages in a closed-form expression. The surface potential is therefore set in Eq. 2 for solving the mobile charge density. The corresponding values of the surface potential and the mobile charge density are then put into Eq. 4 for solving the gate-to-bulk voltage. The surface potential and the mobile charge density are now plotted versus the gate-to-bulk voltage in Fig. 2 as solid lines for four typical cases: case I, no charge trapping; case II, oxide-charge trapping only; case III, interface-charge trapping only; and case IV, both oxide- and interface-charge trapping.

One important defect-related effect is the subthreshold swing degradation induced by interface-trapped charges [21]. This is usually observed from MOSFET transfer characteristics. It can also be perceived from the relation of the surface potential and the mobile charge density with the gate-to-bulk voltage. Another important defect-related effect is the threshold voltage shift. For an *n*MOSFET, positive oxide-trapped charges shift the curves to the left, whereas negative interface-trapped charges move the curves to the right. However, these two types of trapped charges tend to counterbalance the effect of each other and eventually result in a moderate threshold voltage shift. For a *p*MOSFET, both oxide- and interface-trapped charges are positive, leading to a significant threshold voltage shift. The discrepancy between the exact results and the EKV MOSFET model at low values of V_{GB} refers to the invalidity of this model in the accumulation region.

3. Mobile charge linearization

The mobile charge linearization with respect to the surface potential is a fundamental step towards the development of the original EKV charge-based MOSFET model that does not account for charge trapping [18,28]. This section demonstrates that in the presence of oxide- and interface-trapped charges, the mobile charge density can still be linearized, leading to explicit expressions for the mobile charge density and crucial device parameters. They are similar to those of the original EKV MOSFET model in [18] but with an additional scaling factor and revised device parameters. Since oxide-trapped charges simply reduce the flatband voltage without influencing the linear behavior of the mobile charge density, this section will focus on interface-trapped charges.

In the absence of interface-charge trapping and at a given value of

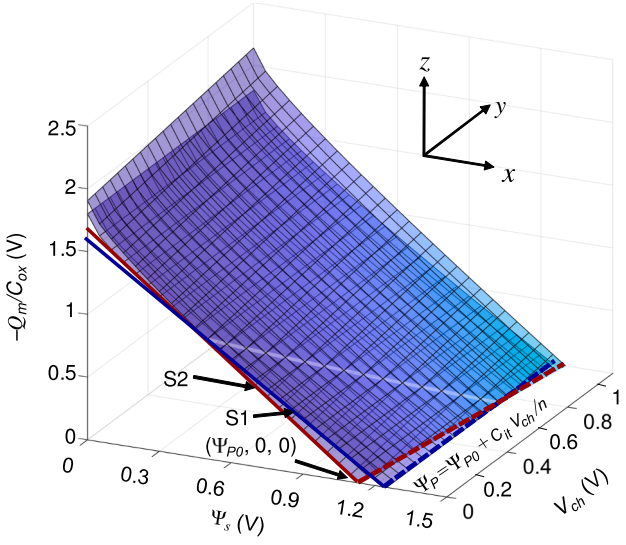

Fig. 3. Mobile-charge-density-related potential $-Q_m/C_{ox}$ versus the surface potential Ψ_s and the channel voltage V_{ch} at a given value of the gate-to-bulk voltage $V_{GB} = 1.1$V for a bulk *n*MOSFET. S1 and S2 refer to a zero value and $3 \times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$ of the interface-trap density D_{it}, respectively.

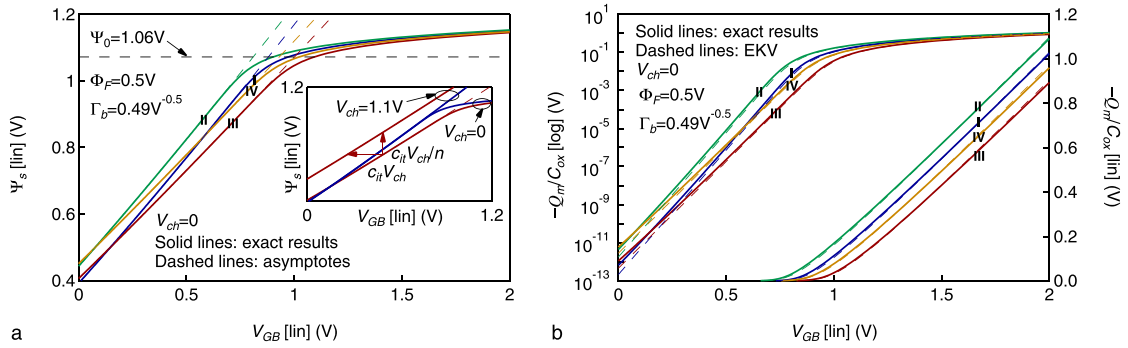

Fig. 2. (a) Surface potential Ψ_s and (b) mobile-charge-density-related potential $-Q_m/C_{ox}$ versus the gate-to-bulk voltage V_{GB} at different values of the oxide-trap density N_{ot} and the interface-trap density D_{it} for a bulk *n*MOSFET: case I, $N_{ot} = D_{it} = 0$, $V_{FB} = -0.7$V; case II, $N_{ot} = 1 \times 10^{12}\text{cm}^{-2}$, $D_{it} = 0$, $V_{FB} = -0.77$V; case III, $N_{ot} = 0$, $D_{it} = 3 \times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$, $V_{FB} = -0.81$V; case IV, $N_{ot} = 1 \times 10^{12}\text{cm}^{-2}$, $D_{it} = 3 \times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$, $V_{FB} = -0.88$V. Solid lines plot the exact results solved from Eq. 2 and Eq. 4. Dashed lines in (a) plot the asymptotes in strong and weak inversion operation regions, while dashed lines in (b) plot the simulated results of the charge–voltage formula Eq. 18.

the gate-to-bulk voltage, the mobile charge density given by Eq. 4 is independent of the channel voltage, as shown by the surface S1 in Fig. 3. The surface potential at which the mobile charge density becomes zero is defined as the pinch-off surface potential Ψ_P [18]. It is also independent of the channel voltage, as illustrated in Fig. 3 by the blue dashed line that corresponds to the intersection of the surface S1 and the floor plane defined by $Q_m = 0$. Furthermore, the mobile charge density is almost linear with the surface potential [18], as evidenced in Fig. 3 by the blue solid line that corresponds to the intersection of the surface S1 and the vertical plane defined by $V_{ch} = 0$. This is consistent with the weak dependence of the slope factor $n(\Psi_s) = d(-Q_m/C_{ox})/d\Psi_s = 1+\Gamma_b/(2\sqrt{\Psi_s})$ on the surface potential in the region of inversion, as demonstrated in Fig. 4 by the blue line for a zero value of D_{it}.

In the presence of interface-charge trapping, the mobile charge density depends on the channel voltage in addition to the surface potential. Hence, the pinch-off surface potential becomes a function of the channel voltage, as illustrated in Fig. 3 by the red dashed line that corresponds to the intersection of the surface S2 and the floor plane. Setting $Q_m = 0$ in Eq. 4 leads to a function that relates the pinch-off surface potential to the gate-to-bulk voltage:

$$V_{GB} \cong V_{FB} + c_{it}\left(\Psi_P - V_{ch}\right) + \Psi_P + \Gamma_b\sqrt{\Psi_P}. \tag{6}$$

Solving Eq. 6 for the pinch-off surface potential gives

$$\Psi_P = \frac{1}{\theta}\left[V^*_{GB} - \Gamma_b^2\left(\sqrt{\frac{V^*_{GB}}{\theta\,\Gamma_b^2} + \frac{1}{(2\theta)^2}} - \frac{1}{2\theta}\right)\right], \tag{7}$$

where $V^*_{GB} \triangleq V_{GB} - V_{FB} + c_{it}V_{ch}$ and $\theta \triangleq 1 + c_{it}$. Setting $c_{it} = 0$ or equivalently $\theta = 1$ in Eq. 7 brings the original expression of Ψ_P, i.e., (3.37) in [18]. Setting $V_{ch} = 0$ or equivalently $V^*_{GB} = V_{GB} - V_{FB}$ in Eq. 7 gives the pinch-off surface potential under the equilibrium condition Ψ_{P0}.

Since the surface S2 in Fig. 3 remains "flat" in the regions of interest, the mobile charge density in Eq. 4 can still be linearized but with respect to both the surface potential and the channel voltage. Linearizing Eq. 4 versus Ψ_s and V_{ch} around the point $\Psi_s = \Psi_{P0}$ and $V_{ch} = 0$ results in

$$-\frac{Q_m}{C_{ox}} \cong -n\left(\Psi_s - \Psi_{P0}\right) + c_{it}\,V_{ch}, \tag{8}$$

where

$$n \triangleq -\left.\frac{\partial(-Q_m/C_{ox})}{\partial\Psi_s}\right|_{\Psi_s=\Psi_{P0},V_{ch}=0} = 1 + \frac{\Gamma_b}{2\sqrt{\Psi_{P0}}} + c_{it} \tag{9}$$

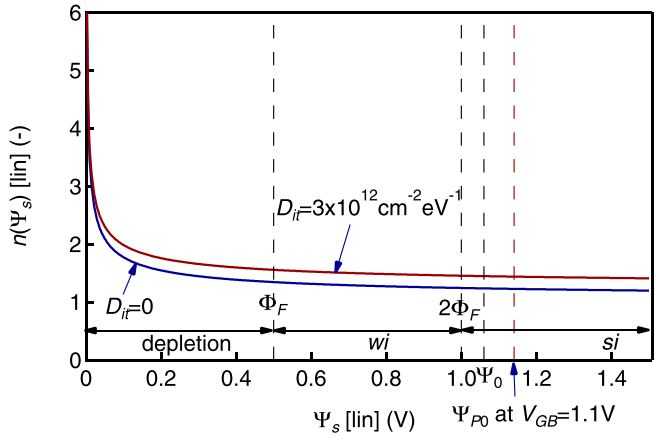

Fig. 4. Slope $n(\Psi_s)$ of the mobile-charge-density-related potential $-Q_m/C_{ox}$ versus the surface potential Ψ_s at a given value of the gate-to-bulk voltage $V_{GB} = 1.1$V and two different values of the interface-trap density D_{it} for a bulk *n*MOSFET.

is the slope factor $n(\Psi_s) = 1+\Gamma_b/(2\sqrt{\Psi_s})+c_{it}$ degraded by interface-trapped charges and evaluated at $\Psi_s = \Psi_{P0}$. The latter $n(\Psi_s)$ is plotted versus Ψ_s as the red line in Fig. 4 for a high value of D_{it}. As shown in Fig. 4, n is still a weak function of Ψ_s in the region of inversion and can therefore be approximated as a constant:

$$n \cong 1 + \frac{\Gamma_b}{2\sqrt{\Psi_0}} + c_{it} = n_0 + c_{it}, \tag{10}$$

where $n_0 = 1+\Gamma_b/(2\sqrt{\Psi_0})$ is the slope factor without interface-charge trapping and $\Psi_0 = 2\Phi_F + mU_T$ is a constant slightly larger than $2\Phi_F$ (m is typically between 2 and 4) [18].

Setting $Q_m = 0$ in Eq. 8 and solving for the surface potential leads to an approximation of the pinch-off surface potential

$$\Psi_P \cong \Psi_{P0} + \frac{c_{it}}{n}V_{ch}, \tag{11}$$

which corresponds to the intersection of the approximated surface of S2 and the floor plane, as plotted by the red dashed line in Fig. 3. Introducing it into Eq. 8 yields

$$-\frac{Q_m}{C_{ox}} \cong -n\left(\Psi_s - \Psi_P\right), \tag{12}$$

which is identical to (3.39) in [18], except that the pinch-off surface potential now depends on the channel voltage.

In weak inversion (*wi*), the mobile charge density remains negligible compared to the depletion charge density. Combining Eq. 2 and Eq. 4 and neglecting the exponential term gives an expression of the gate-to-bulk voltage versus the surface potential for *wi* [29]:

$$V_{GB} \cong V_{FB} + c_{it}\left(\Psi_s|_{wi} - V_{ch}\right) + \Psi_s|_{wi} + \Gamma_b\sqrt{\Psi_s|_{wi}}, \tag{13}$$

which is identical to Eq. 6. Solving it for $\Psi_s|_{wi}$ gives the weak inversion asymptote of the Ψ_s versus V_{GB} curves, as plotted by the colored dashed lines in Fig. 2a. By definition, the pinch-off surface potential solved from Eq. 6 actually falls on the weak inversion asymptote of the Ψ_s versus V_{GB} curves. The inserted figure in Fig. 2a presents the dependence of the pinch-off surface potential on the channel voltage in the presence of interface-charge trapping.

4. Charge–voltage relation

The approximate expression of the mobile charge density Eq. 8 can now be used to express the surface potential as a function of the mobile charge density and the channel voltage and substitute it in Eq. 2 to obtain an explicit expression of the charge-voltage relation. To do this, it is convenient to first rewrite Eq. 2 in its normalized form as

$$\psi_s - 2\phi_f - v = \ln\left[q_m\frac{2n}{\gamma_b}\left(q_m\frac{2n}{\gamma_b} + 2\sqrt{\psi_s}\right)\right], \tag{14}$$

where $q_m \triangleq Q_m/Q_{spec}$ with $Q_{spec} \triangleq -2nU_TC_{ox}$ as the *specific charge*, $\psi_s \triangleq \Psi_s/U_T$, $\phi_f \triangleq \Phi_F/U_T$, $v \triangleq V_{ch}/U_T$, and $\gamma_b \triangleq \Gamma_b/\sqrt{U_T}$. The surface potential obtained from Eq. 8 is normalized as

$$\psi_s = \psi_{p0} + \frac{c_{it}}{n}\,v - 2q_m, \tag{15}$$

where $\psi_{p0} \triangleq \Psi_{P0}/U_T$. Replacing the normalized surface potential in Eq. 14 with Eq. 15 and rearranging the terms results in

$$2q_m + \ln q_m = \psi_{p0} - 2\phi_f - \frac{n_0}{n}v - \underbrace{\ln\left[\frac{2n}{\gamma_b}\left(q_m\frac{2n}{\gamma_b} + 2\sqrt{\psi_{p0} + \frac{c_{it}}{n}v - 2q_m}\right)\right]}_{v_{sh}}, \tag{16}$$

where the voltage shift labelled by v_{sh} is a weak function of q_m, ψ_{p0} and v. It can therefore be assumed to be constant at $m = v_{sh} \cong \ln(4n_0\sqrt{\psi_{p0}}/\gamma_b) \cong 2.8$ for this 28-nm bulk CMOS technology.

The normalized pinch-off voltage $v_p \triangleq V_P/U_T$ is defined as the particular value of the normalized channel voltage v at which the LHS of Eq. 16 is equal to zero:

$$v_p = \frac{n}{n_0}\left(\psi_{p0} - 2\phi_f - v_{sh}\right). \tag{17}$$

Introducing Eq. 17 in Eq. 16 finally leads to the important charge–voltage equation

$$2q_m + \ln q_m = \frac{n_0}{n}\left(v_p - v\right), \tag{18}$$

which introduces a scaling factor $n_0/n = 1/(1+c_{it}/n_0)$ into the original expression, i.e., Eq. (3.48) in [18], to account for the effects of interface-trapped charges.

To further simplify the model, we propose to find an approximate expression of the pinch-off voltage with the strong inversion approximation. The pinch-off voltage in strong inversion (*si*) is defined as the particular value of the channel voltage at which the mobile charge density becomes zero. In the presence of oxide- and interface-charge trapping, it still tends to saturate to $\Psi_s|_{si} \cong \Psi_0 + V_{ch}$, as shown in Fig. 2a. Introducing this strong inversion approximation into Eq. 4 and setting $Q_m = 0$ in Eq. 4 leads to a function that relates the gate-to-bulk voltage to the pinch-off voltage

$$V_{GB} \cong V_{FB} + \left(1 + c_{it}\right)\Psi_0 + V_P + \Gamma_b\sqrt{\Psi_0 + V_P}. \tag{19}$$

Eq. 19 is plotted in Fig. 5, which demonstrates an almost linear relation between the gate-to-bulk voltage and the pinch-off voltage for any of those four typical cases investigated in Fig. 2. This is consistent with the almost constant derivative of Eq. 19 versus the pinch-off voltage $dV_{GB}/dV_P = 1 + \Gamma_b/(2\sqrt{\Psi_0 + V_P}) \cong 1 + \Gamma_b/(2\sqrt{\Psi_0})$, which corresponds to the slope factor without interface-charge trapping n_0.

Now we define the threshold voltage under the equilibrium condition as the value of the gate-to-bulk voltage when the mobile charge density is equal to zero

$$V_T = \underbrace{\Phi_{ms} - \frac{Q_f}{C_{ox}} + \Psi_0 + \Gamma_b\sqrt{\Psi_0}}_{V_{T0}} + \underbrace{c_{it}\left(\Psi_0 - \Phi_F\right) - \frac{qN_{ot}}{C_{ox}}}_{\Delta V_T}, \tag{20}$$

where V_{T0} is the threshold voltage without charge trapping and ΔV_T is the threshold voltage shift induced by the opposite effect of oxide- and interface-charge trapping. Note that unlike for an *n*MOSFET, both oxide- and interface-trapped charges tend to reduce the threshold voltage of a *p*MOSFET.

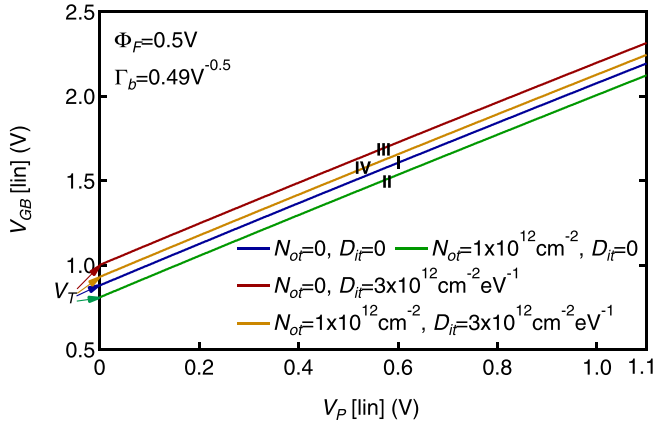

Fig. 5. Gate-to-bulk voltage V_{GB} versus the pinch-off voltage V_P at different values of the oxide-trap density N_{ot} and the interface-trap density D_{it} for a bulk *n*MOSFET in strong inversion.

The pinch-off voltage can now be approximated as

$$V_P \cong \frac{V_{GB} - V_T}{n_0}. \tag{21}$$

Note that we have $dV_{GB}/d\Psi_{P0} = dV_{GB}/d\Psi_P \cong n$ from Eq. 6 and $dV_{GB}/dV_P = (n_0/n)(dV_{GB}/d\Psi_{P0})$ from Eq. 17, which leads to $dV_{GB}/dV_P \cong n_0$. This agrees with the above discussion about the pinch-off voltage in strong inversion.

The dashed lines in Fig. 2b plot the approximate mobile charge density solved from Eq. 18 and Eq. 21. The approximate results present an excellent match with their exact counterparts, demonstrating the sufficient accuracy of these explicit expressions for a simple model including the effects of oxide- and interface-trapped charges.

5. Current-charge relation

The drain-to-source current relies on the classical drift–diffusion transport according to

$$I_D = \mu_0 W\left(-Q_m\frac{d\Psi_s}{dx} + U_T\frac{dQ_m}{dx}\right), \tag{22}$$

where μ_0 is the low-field channel mobility that is assumed constant along the channel, W is the channel width, and x is the position along the channel from the source to the drain. Solving for the surface potential with Eq. 8 and introducing it into Eq. 22 yields

$$I_D = \mu_0 W\left[\left(U_T - \frac{Q_m}{nC_{ox}}\right)\frac{dQ_m}{dx} - \frac{c_{it}}{n}Q_m\frac{dV_{ch}}{dx}\right]. \tag{23}$$

Normalizing Eq. 23 gives

$$i_d \triangleq \frac{I_D}{I_{spec}} = -\left(1 + 2q_m\right)\frac{dq_m}{d\xi} + \frac{c_{it}}{n}q_m\frac{dv}{d\xi}, \tag{24}$$

where i_d is the normalized drain-to-source current, $I_{spec} \triangleq I_{spec\square}W/L$ is the *specific current*, $I_{spec\square} \triangleq 2n\mu_0 C_{ox}U_T^2$ is the *specific current per square*, L is the channel length, and $\xi \triangleq x/L$ is the relative position along the channel from the source. Eq. 24 is almost identical to (4.21) in [18], except for the additional last term as a result of interface-charge trapping.

To obtain a full charge expression of the current that can then be integrated in the charge domain as in the original EKV MOSFET model, a charge expression of the last term in Eq. 24 needs to be found. This can be done by differentiating Eq. 18 with respect to ξ:

$$\frac{dv}{d\xi} = -\frac{n}{n_0}\left(2 + \frac{1}{q_m}\right)\frac{dq_m}{d\xi}. \tag{25}$$

Introducing Eq. 25 in Eq. 24 results in a charge-based expression of the drain current that includes the effects of oxide- and interface-charge trapping:

$$i_d = -\frac{n}{n_0}\left(1 + 2q_m\right)\frac{dq_m}{d\xi}. \tag{26}$$

The drain current is then simply obtained as in the original EKV MOSFET model by integrating Eq. 26 from the source to the drain in the charge domain:

$$i_d = \frac{n}{n_0}\left[\left(q_s^2 + q_s\right) - \left(q_d^2 + q_d\right)\right], \tag{27}$$

where q_s and q_d are the normalized mobile charge densities evaluated at the source and drain ends of the channel, respectively [18]. Eq. 27 is

almost identical to the original expression (4.22) in [18], except for the additional scaling factor n/n_0 that accounts for the effects of interface-trapped charges. Note that q_s and q_d are linked to the terminal voltages through Eq. 18 by replacing q_m and v with q_s and $v_{sb} \triangleq V_{SB}/U_T$ at the source and q_d and $v_{db} \triangleq V_{DB}/U_T$ at the drain. Solving the obtained formulations of q_s and q_d with Eq. 27 finally relates the drain current to the terminal voltages for long-channel devices.

6. Velocity saturation effect

Velocity saturation is certainly one of the most important short-channel effects. It causes the degradation of the drain current and transconductance in strong inversion. This effect has been included into the EKV MOSFET model via the velocity saturation parameter $\lambda_c = L_{sat}/L$, which represents the fraction of the channel $L_{sat} = 2U_T\mu_0/v_{sat}$ where the carrier velocity fully saturates [30]. Since L_{sat} is proportional to μ_0 and interface-trapped charges degrade μ_0 via Coulomb scattering, the velocity saturation parameter $\lambda_c = 2U_T\mu_0/(v_{sat}L)$ varies with interface-charge trapping.

When the carrier velocity is saturated close to the drain, the drain current cannot increase anymore and saturates to i_{dsat}. The mobile charge density at the drain is not pinched-off to zero but remains at a finite value q_{dsat} for the saturated current to flow. Accounting for oxide- and interface-charge trapping, the saturated drain current and the saturated mobile charge density at the drain are linked by [30]

$$i_{dsat} = \frac{2q_{dsat}}{\lambda_c}, \tag{28}$$

where the simple piecewise mobility model is assumed. The expression of the drain current given by Eq. 27 is now modified by the effect of velocity saturation according to

$$i_{dsat} = \frac{n}{n_0}\left[\left(q_s^2 + q_s\right) - \left(q_{dsat}^2 + q_{dsat}\right)\right]. \tag{29}$$

Solving Eq. 28 and Eq. 29 for i_{dsat} gives

$$i_{dsat} = \frac{4\frac{n}{n_0}\left(q_s^2 + q_s\right)}{\sqrt{\left(\frac{n}{n_0}\lambda_c\right)^2(2q_s+1)^2 + 4\left(\frac{n}{n_0}\lambda_c + 1\right)} + \frac{n}{n_0}\lambda_c + 2}. \tag{30}$$

The drain current under velocity saturation given by Eq. 30 needs to be combined with Eq. 18 where q_m is replaced by q_s and v by v_{sb}. An explicit expression of the drain current versus the terminal voltages can unfortunately not be obtained. However, a voltage-current relation can be obtained by first solving Eq. 30 for q_s:

$$q_s = \frac{1}{2}\left[\sqrt{(\lambda_c i_{dsat} + 1)^2 + 4\frac{n_0}{n}i_{dsat}} - 1\right]. \tag{31}$$

Introducing it into $2q_s + \ln q_s = n(v_p - v_{sb})/n_0$ from Eq. 18 gives the important current–voltage expression for short-channel devices in saturation

$$\frac{n_0}{n}\left(v_p - v_{sb}\right) = \sqrt{(\lambda_c i_{dsat} + 1)^2 + 4\frac{n_0}{n}i_{dsat}} + \ln\left[\sqrt{(\lambda_c i_{dsat} + 1)^2 + 4\frac{n_0}{n}i_{dsat}} - 1\right] - (1 + \ln 2). \tag{32}$$

The EKV parameters defined in Sections 3–5 include most of the physical quantities of a specific technology and efficiently captures defect-related effects on a specific device geometry. To provide a more tangible description of the drain current, the EKV parameters are brought back to Eq. 32, yielding

$$\frac{V_{GB} - V_T - n_0 V_{SB}}{nU_T} = \sqrt{\left(\lambda_c\frac{I_{Dsat}}{2n\beta U_T^2} + 1\right)^2 + 4\frac{n_0}{n}\frac{I_{Dsat}}{2n\beta U_T^2}} + \ln\left[\sqrt{\left(\lambda_c\frac{I_{Dsat}}{2n\beta U_T^2} + 1\right)^2 + 4\frac{n_0}{n}\frac{I_{Dsat}}{2n\beta U_T^2}} - 1\right] - (1 + \ln 2), \tag{33}$$

where $\beta = \mu_0 C_{ox} W/L$ is the transfer parameter.

Setting $\lambda_c = 0$ in Eq. 32 brings the short-channel model back to the long-channel counterpart. Compared to the original EKV MOSFET model, interface-charge trapping introduces a scaling factor $n_0/n = 1/(1 + c_{it}/n_0)$ in front of the normalized current i_{dsat} and the normalized saturation voltage $v_p - v_{sb}$, in addition to the shifted threshold voltage and the degraded slope factor. These newly developed expressions are quite similar to the original version and maintain many properties of the original EKV MOSFET model.

7. Model validation

To validate the proposed model, ionizing radiation has been applied to generate oxide-trapped charges and activate passivated interface traps. When a MOSFET is exposed to high-energy ionizing radiation, electron–hole pairs are generated in dielectrics and holes escaping the initial recombination can be trapped in oxide defects [6,31]. Positive protons, formed via the interaction of radiation-generated holes with hydrogen-contained oxide defects, could break the silicon-hydrogen bonds and activate the passivated interface traps [32,33]. The proposed EKV charge-based MOSFET model can therefore be validated with pre-radiation and radiation measurements of the same MOSFETs. The devices under test are from a commercial 28-nm bulk CMOS technology. More measurement details can be found in [34].

Model parameters are extracted, using an approach similar to that in [19,35] while handling the scaling factor n_0/n carefully. In addition to the effects on the threshold voltage and the slope factor, both $I_{spec\square}/n$ and L_{sat}, which are proportional to the low-field channel mobility μ_0, also degrades with TID due to Coulomb scattering. Since $I_{spec\square}/(nL_{sat}) = C_{ox}U_T v_{sat}$ is constant, $I_{spec\square}/(nL_{sat})$ is maintained constant during the whole extraction procedure. The measured and modeled drain current of long- and short-channel n- and pMOSFETs in saturation is plotted in Fig. 6. Despite a small number of parameters, the newly developed model shows an excellent agreement with measurement results in a broad range of device operation from weak to strong inversion. The effects of TID on MOSFET characteristics are efficiently captured by $\Delta n = c_{it}$ for the subthreshold swing degradation, ΔV_T for the threshold voltage shift, and $(I_{specsq}/n)/(I_{specsq}/n)_0$ or λ_c/λ_{c0} for the low-field channel mobility reduction, as partly listed in Table 1.

The TID-induced drain leakage current of nMOSFETs flows from the parasitic conduction paths created by positive charges trapped in the shallow trench isolation oxides, as addressed in [34]. It is modeled as a constant current flowing through a gateless charge-controlled device. Our recent study also demonstrates that the counterpart of pMOSFETs comes from the substrate instead of the source, which is almost independent of the gate-to-bulk voltage and can also be assumed constant. For both n- and pMOSFETs, a constant value will therefore be added to the EKV charge-based MOSFET model for accounting for the drain leakage current induced by radiation-induced oxide- and interface-

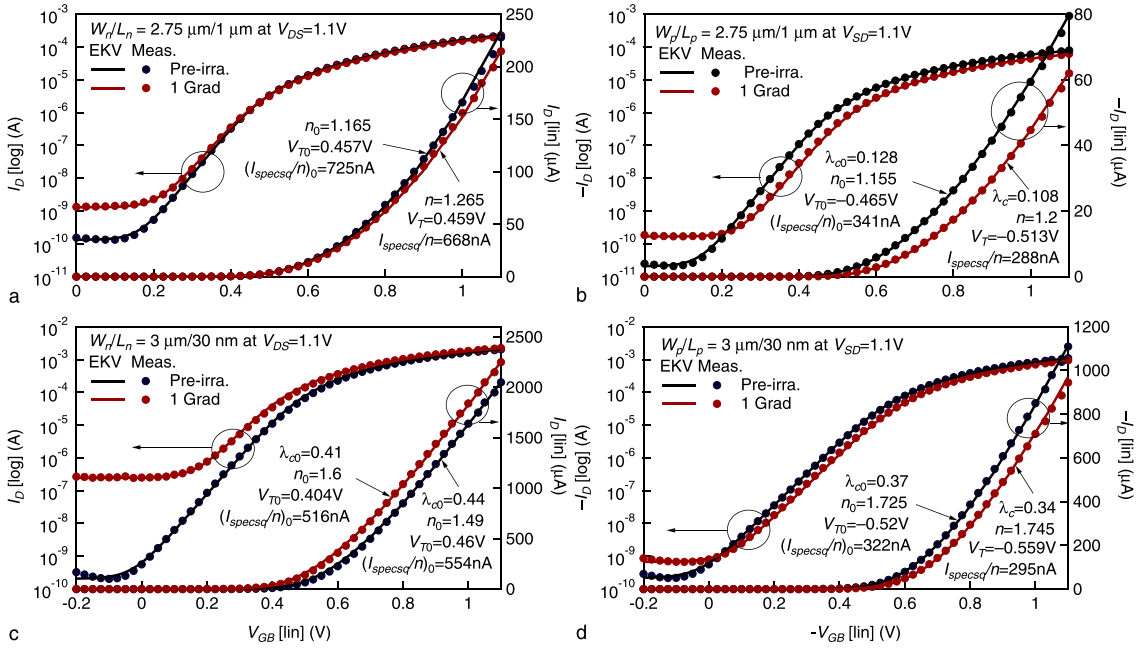

Fig. 6. Measured (markers) and modeled (lines) drain current $|I_D|$ versus the gate-to-bulk voltage $|V_{GB}|$ curves of (a,b) long- and (c,d) short-channel (a,c) *n*- and (b,d) *p*MOSFETs in saturation ($|V_{DS}|$ = 1.1V) corresponding to pre-radiation and 1 Grad(SiO_2) of total ionizing dose.

trapped charges.

Explicit expressions of device parameters allow us to extract the oxide- and interface-trapped charge densities at each radiation step, which can then be linked to TID for compact modeling. The interface-trap density is extracted from the slope factor increase $c_{it} = q^2 D_{it}/C_{ox}$. Since $\Psi_0 = 2\Phi_F + 2.8U_T$ for this 28-nm CMOS technology, the total threshold voltage shift is expressed as $\Delta V_T = q[qD_{it}(\Phi_F + 2.8U_T) - N_{ot}]/C_{ox}$ for *n*MOSFETs and $\Delta V_T = -q[qD_{it}(\Phi_F + 2.8U_T) + N_{ot}]/C_{ox}$ for *p*MOSFETs. Having D_{it} from the slope factor increase enables us to calculate the threshold voltage shift due to interface-trapped charges $\Delta V_{it} = q^2 D_{it}(\Phi_F + 2.8U_T)/C_{ox}$. Deducting it from the total threshold voltage shift gives the threshold voltage shift induced by oxide-trapped charges ΔV_{ot}, from which the oxide-trap density N_{ot} can be extracted. Since short-channel *n*MOSFETs demonstrate radiation-enhanced drain-induced barrier lowering (DIBL) effects [36], the relevant oxide-trapped density should be extracted after deducting the radiation-induced DIBL factor. This will be investigated in our future work together with a comprehensive discussion of radiation effects on this 28-nm bulk CMOS technology using this generalized EKV charge-based MOSFET model.

Table 1
Model parameters.

Device type	*n*	*n*	*p*	*p*
W (µm)	2.75	3	2.75	3
L (µm)	1	0.03	1	0.03
Δn	0.1	0.11	0.045	0.02
ΔV_T (mV)	2	−56	−48	−39
N_{ot} (cm^{-2})	7.8×10^{11}	9.1×10^{11}	3.2×10^{11}	3.9×10^{11}
D_{it} ($cm^{-2}eV^{-1}$)	1.4×10^{12}	1.6×10^{12}	6.3×10^{11}	2.8×10^{11}

Fig. 7 plots the slope factor increase and the threshold voltage shift with respect to TID for long-channel MOSFETs, indicating the radiation-induced oxide- and interface-charge trapping. For the long-channel *n*MOSFET, the threshold voltage first decreases and then increases, suggesting the counterbalancing effects of oxide- and interface-trapped charges. Even though the threshold voltage shift at 1Grad(SiO_2) is quite small, the extracted density of oxide- ($7.8 \times 10^{11} cm^{-2}$) and interface-trapped charges ($1.4 \times 10^{12} cm^{-2} eV^{-1}$), as indicated in Table 1, still implies the effects of TID. For the long-channel *p*MOSFET, the extracted density of oxide- ($3.2 \times 10^{11} cm^{-2}$) and interface-trapped charges ($6.3 \times 10^{11} cm^{-2} eV^{-1}$) are not significant. However, due to the accumulated effects of oxide- and interface-trapped charges, the

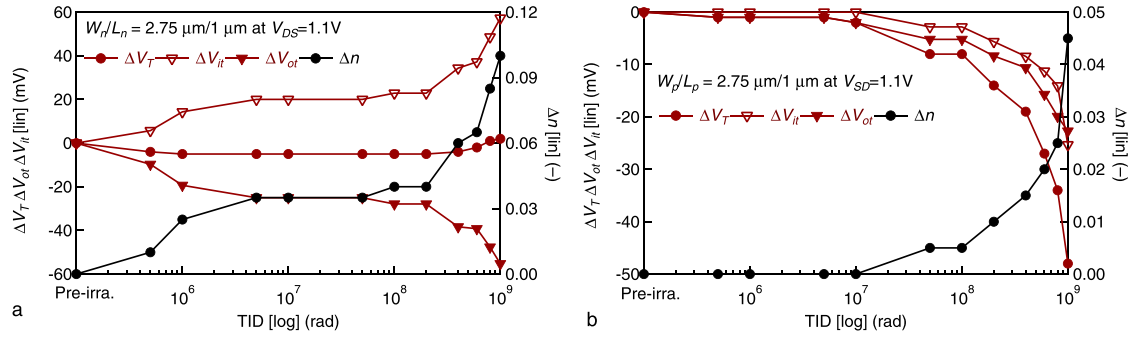

Fig. 7. Threshold voltage shift (ΔV_T on the left axis) and slope factor increase (Δn on the right axis) with respect to total ionizing dose for (a) a long-channel *n*MOSFET and (b) a long-channel *p*MOSFET (b) in saturation ($|V_{DS}|$ = 1.1V).

threshold voltage shift is still quite high at 1Grad(SiO_2), as shown in Table 1.

8. Conclusions

This work presents a generalized EKV charge-based MOSFET model that includes the effects of trapped charges in the oxide bulk and at the silicon/oxide interface and can be applied for modeling effects of total ionizing dose, bias-temperature instability, and hot-carrier injection. Oxide-charge trapping simply reduces the effective gate-to-bulk voltage without influencing the linear behavior of the mobile charge density with the surface potential. Interface-charge trapping introduces a dependence of the pinch-off surface potential on the channel voltage. Using a two-dimensional approximation, the mobile charge density at a given gate-to-bulk voltage is linearized with respect to both the surface potential and the channel voltage, in the presence of oxide- and interface-trapped charges. This allows the derivation of explicit expressions for the charge–voltage relation and the current-charge relation. Finally, the effect of velocity saturation is included to model short-channel devices.

The newly derived expressions are similar to those of the original EKV MOSFET model with an additional scaling factor and revised device parameters representing the effects of oxide- and interface-trapped charges. The impact of oxide-trapped charges is captured by a threshold voltage shift, whereas the effects of interface-trapped charges are manifested as a threshold voltage shift and a slope factor increase. The proposed charge-based analytical model is successfully validated against a 28-nm bulk CMOS technology with measurements of various MOSFETs. Total ionizing doses up to 1Grad(SiO_2) are applied to generate oxide-trapped charges and activate the passivated interface traps. Despite a small number of parameters, the model accurately captures the effects of radiation-induced oxide- and interface-trapped charges, resulting in an excellent fit with measurement results over a very wide range of device operation from weak to strong inversion. Explicit expressions of device parameters allow for the extraction of the oxide- and interface-trapped charge densities at each radiation step, which can serve for compact modeling of total ionizing radiation effects.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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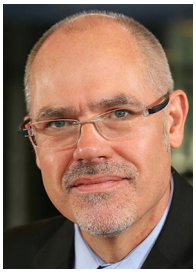

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