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Hybrid Modular Multilevel Converter for Variable DC Link Voltage Operation

Miodrag Basić and Dražen Dujić

***Abstract*—Modular Multilevel Converter secured its place in applications where high reliability, efficiency and effortless voltage/power scalability are of paramount importance. Without compromising these benefits, this paper proposes a novel control and appropriate design approach for Hybrid-MMC topology, comprising a mix of Full-Bridge and Half-Bridge submodules in converter branches, as a grid-side stage of a back-to-back MMC, enabling operation at variable DC link voltage and arbitrary power factor. In the midst of transition to Renewable Energy Sources-dominated power systems, variable DC link voltage operation opens door to the use of Hybrid-MMC in retrofit of large Pumped Hydro Storage Plants to variable speed operation, where existing machines would not tolerate high common-mode voltage stress imposed by fixed-DC-link-voltage operated machine-side MMC stage. In this way, highly flexible grid-scale energy storage use of existing hydro capacities is enabled. Converter design approach and additional control layers have been developed and verified through a set of test scenarios. Sizing and operation at typical operating points are compared to equally-rated Full-Bridge-based MMC. Improvements over the existing Hybrid-MMC solutions include unity-power-factor operation at the entire attainable DC link voltage range and equal loading of upper and lower phase-leg branches regardless of the operating point.**

***Index Terms*—Modular Multilevel Converter, mixed-cell converter, Active Front-End, hydroelectric power generation, retrofit.**

I. Introduction

HISTORICALLY, Modular Multilevel Converter (MMC) was first developed for and deployed in high voltage DC inter-ties, where unrestricted voltage scalability and redundancy made it superior to competing topologies. In such a utility-scale system, typical MMC implementation is made utilizing low-loss Half-Bridge (HB) Submodules (SMs) as converter building blocks [1].

More recently, under a persistent increase of installed Renewable Energy Sources (RES) generation capacities, predominantly photo-voltaic and wind turbines, we are witnessing an imminent transition towards RES-dominated power systems, where the need for high-volume highly-flexible energy storage systems emerges. With the highest share of grid-scale installed capacity and minute-range start-up times, large (Table I) Pumped Hydro Storage Plants (PHSPs) already offer significant balancing potential. More specifically, Variable Speed (VS) PHSPs offer further flexibility through variable pumping power, i.e. grid frequency control in both pumping and generating modes of operation. This is essential as the excess of energy produced by non-dispatchable RES can be balanced, while eliminating the need for fossil-fuel-based units [2], [3]. Further efficiency increase through the selection of optimal operating speed [4], and increased revenue from participating at ancillary services market [5], are clear motivations for retrofit of existing PHSP units to VS.

TABLE I
Typical machine ratings in large PHSPs.

Stator voltage	V_{LL}	6 kV to 21 kV
Stator current	I_{RMS}	2 kA to 8 kA
Apparent power	S_n	80 MVA to 400 MVA

Historically, components- and topologies-related limitations in available power electronics converters restricted large VS units to the use of Doubly-Fed Induction Machine (DFIM). Consequently, compared to total installed PHSP generating capacity ($\approx$160 GW), share of large VS units (above 100 MW) is dominated by DFIM, at approximately 10 GW, with only one Converter-Fed Synchronous Machine (CFSM)-based VS-retrofitted unit in operation [6], rated at 100 MW [7], [8].

Significant potential lays in retrofit of existing fixed speed PHSPs to CFSM-based VS units. While keeping the original machine, CFSM enables turbine/pump change-over without de-watering, grid-side dynamical behaviour only limited by the fast current control loops, low-voltage ride-through handling superior to DFIM, with full control over the fault current and grid support. However, unlike [6], a highly scalable design is necessary to mitigate the need for additional voltage matching transformers.

Owing to inherent scalability and high-quality voltage waveform, MMC is a good candidate for machine ratings from Table I [8]. In AC-AC applications, such is a Variable Speed Drive (VSD) of the PHSP, either a matrix-like direct MMC, or a back-to-back Indirect MMC (I-MMC) can be considered. Direct MMC is an efficient solution if machine- and grid-frequency differ, making it suitable for new installations, with unrestricted choice of machine parameters [9]. I-MMC, on the other hand, decouples AC systems of the machine and the grid, being suitable for arbitrary ratio of machine- and grid-frequency, including equal values. This is essential for retrofit of existing fixed speed PHSP units, where ideally no machine modifications should occur (Fig. 1).

As already well documented in the literature, there are issues associated with operation of MMC at low output fre-

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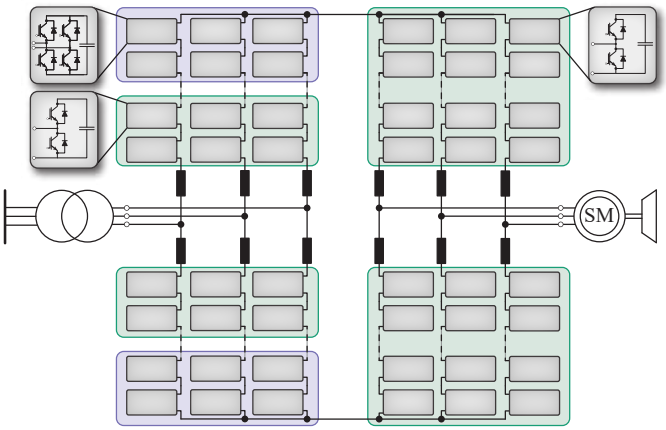

Fig. 1. H-MMC topology, presented as grid-side stage of an I-MMC solution to retrofit of an existing PHSP with H-MMC for conversion to VS operation, without machine modifications. Machine-side MMC is a standard HB SM based unit, not analyzed in this paper, while grid-side stage is a H-MMC based on mix of FB and HB SMs, acting as AFE; its design and operating principles are presented in the paper.

quency [10]. The additional machine stress that these methods impose, in terms of high Common Mode (CM) voltage amplitudes at Low Frequency (LF), up to rated winding voltage, can prove prohibitively high when retrofitting units that were originally designed for sine-wave grid supply.

Research community has recognized the potential of variable DC link voltage operation of machine-side MMC stage, as machine-friendly CM-free operation can be performed by varying the DC link voltage with output machine frequency, in the range $(0, V_{\mathrm{DC,n}}]$, where $V_{\mathrm{DC,n}}$ denotes rated DC link voltage. The efficient all-HB MMC AFE, however, can only operate in narrow band around $V_{\mathrm{DC,n}}$, due to fixed AC-side grid voltage amplitude. The use of all-FB grid-side MMC stage, able to operate at $[-V_{\mathrm{DC,n}}, V_{\mathrm{DC,n}}]$, is discussed in [11], as the most extreme alternative in terms of additional power losses and cost. In [12], a switch is introduced to the DC link, constant voltage of an ideal DC source, which could be replaced by HB-based MMC, is chopped to achieve appropriate average V_{DC}. The entire converter reliability, however, relies on the newly introduced switch, thus redundancy is compromised. A two-quadrant solution is proposed in [13], utilizing cascaded H-bridge as the grid-side stage.

Variable DC voltage operation through the use of H-MMC topologies, comprising a mix of HB and FB SMs has been studied in the literature. In [14], hybrid grid-side MMC stage is proposed, while two fixed-frequency operating points of the machine were observed. High current stress imbalance among the upper and lower branches of grid-side stage at certain operating points is inherent to the presented technique, calling for non uniform SMs' current ratings. H-MMC topology has also been addressed in [15], where operation at lower-than-rated DC link voltage requires proportional increase in reactive power towards the grid, making it unsuitable for the observed grid-connected PHSP application, since an arbitrary power factor, including unity, can be requested by the Transmission System Operator, regardless of the converter's internal operating point.

This paper focuses on design and control of H-MMC AFE for variable DC link voltage operation, with the key contributions being: 1) a control method for H-MMC AFE, comprising a mix of HB and FB SMs in phase branches (Fig. 1), for variable DC link voltage operation, enabling converter to be operated at arbitrary power factor, including unity, over the designed DC link voltage operating range, and at equal upper- and lower branches loading; 2) a design approach for selection of optimal FB to HB SM ratio for the desired DC voltage operating range. Thus, a solution specially suitable for, but not limited to, retrofit of existing PHSPs to highly flexible VS operation is developed.

The rest of the paper is organized as follows. Section II briefly discusses the variable DC link voltage operation requirements of machine-side MMC stage. Further, grid-side H-MMC stage branch-level energy dynamics between DC link, AC terminals, and FB and HB Submodule Clusters (SMCs) is observed for the reduced DC link voltage operation. SMC energy balancing method is presented in Section III, where additional balancing current and voltage capacity requirements are determined. Starting from desired DC link voltage reduction level, Section IV develops H-MMC design path in a generalized form, resulting in optimal FB to HB SM ratio for the operating range. Section V outlines the H-MMC control system, insertion voltage calculation, concept of virtual HB SM and appropriate modulator. Representative test scenarios and results of high fidelity switched-model simulations are presented and discussed in Section VI. Conclusions are brought up in the final Section.

II. Reduced DC link voltage operation

While HB-based I-MMC is a highly energy-efficient and machine-friendly VS PHSP conversion candidate in terms of multilevel voltage waveform, fixed-DC-link-voltage operation calls for machine-side converter control strategies that involve high-amplitude CM voltage stress in LF operating region [10]. In retrofit, we are faced with machines designed for sine-wave grid supply, which leads to insulation reinforcement requirements for windings and bearings, or even complete machine replacement.

In case grid-side HB-based stage is swapped with H-MMC mixed-SM topology, as presented in left half of Fig. 1, the converter can be operated at variable DC link voltage, allowing for machine-side stage to be HB-based, but without need to use high-amplitude CM voltage control methods [11]. No machine modifications are needed, while no additional balancing current load is imposed on machine-side MMC stage.

Even at partial reduction of DC link voltage, advantages can be obtained, either in conjunction with CM voltage LF operation strategy [16], or through reduction of SM reference voltage level that allows for higher SM voltage oscillation margin [17]. Relying on [16] and [11], partially reduced DC link voltage leads to lower required machine-side CM voltage amplitude for energy oscillation suppression, without further increase in LF circulating current amplitude. Thereby, CM voltage amplitude is kept below (existing) machine limitations.

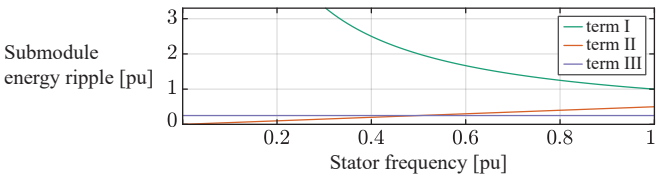

Fig. 2. Frequency dependence of SM energy ripple components (3). The first term is dominant in LF region.

As only partial reduction of DC link voltage is sufficient, which can be achieved replacing a fraction of AFE MMC's HB SMs with FB units, this is an attractive field to consider as a compromise between PHSP I-MMC-based VSD with all-FB and all-HB AFE.

A. LF machine-side operation requirements

At first, a short analysis of LF MMC-based VSD operation is presented, where variable DC link voltage is considered as an alternative to CM-voltage-based techniques.

For operation at reduced DC link voltage, defined by factor $k_{\mathrm{DC}} \in (0, 1]$ such that $V_{\mathrm{DC}} = k_{\mathrm{DC}} V_{\mathrm{DC,n}}$, inserted upper- and lower-branch voltages (1) and branch current (2) are obtained, assuming an ideally balanced converter, i.e. no balancing circulating current components $i_{\mathrm{c,bal}}$ and neglecting phase index.

$$v_{\{\mathrm{p,n}\}} = \frac{k_{\mathrm{DC}} V_{\mathrm{DC,n}}}{2} \mp \frac{m_s V_{\mathrm{DC,n}}}{2} \cos(\omega_s t + \theta_s) \tag{1}$$

$$i_{\{\mathrm{p,n}\}} = \frac{I_{\mathrm{DC}}}{3} \pm \frac{\hat{i}_s}{2} \cos(\omega_s t + \varphi_s) \tag{2}$$

The following notation is adopted: m_s – modulation index, ω_s – AC-side angular frequency, θ_s – AC-side voltage angle, i_s – AC-terminal current, φ_s – angle between AC-side voltage and current phasors.

Starting from (1)-(2), assuming equal voltage distribution among the SMs, instantaneous zero-average SM energy components are obtained. Positive (upper) branch is observed.

$$\tilde{w}_{\mathrm{SM}} = \frac{1}{N_{\mathrm{SM}}} \int \tilde{p}\, \mathrm{d}t = \frac{k_{\mathrm{DC}} V_{\mathrm{DC,n}} \hat{i}_s}{4 N_{\mathrm{SM}}} \Bigg\{ \underbrace{\frac{1}{\omega_s} \sin(\omega_s t - \varphi)}_{\text{(I) decreases with } \omega_s} - \underbrace{\frac{m_s^2}{2\omega_s} \cos(\varphi) \sin(\omega_s t)}_{\text{(II) increases with } \omega_s} - \underbrace{\frac{m_s}{4\omega_s} \sin(2\omega_s t - \varphi)}_{\text{(III) constant}} \Bigg\} \tag{3}$$

At $k_{\mathrm{DC}} = 1$, assuming constant-torque operation of the machine, i.e. $\hat{i}_s = \text{const}$, energy oscillations increase with frequency decrease, as visualized in Fig. 2 where all three components of (3) are drawn. This calls for either very high SM capacitance or additional CM corrective action [10]. Varying DC link voltage with machine-side frequency, $k_{\mathrm{DC}} V_{\mathrm{DC,n}} / \omega_s = \text{const}$, ensures constant SM capacitor energy ripple without further control actions.

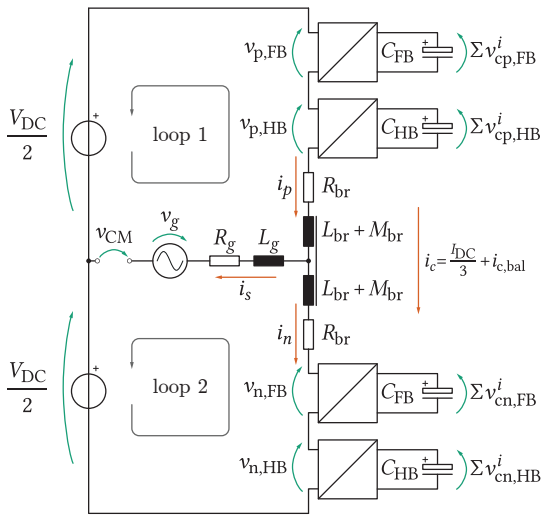

Fig. 3. Equivalent circuit of one phase of a hybrid MMC, where all the SMs are presented as two units, being equivalent to the SMCs of FB and HB SM installed. The following notation is applied: C_{FB}, C_{HB} – equivalent capacitance, $\Sigma v^i_{\mathrm{c\{p,n\},FB}}$, $\Sigma v^i_{\mathrm{c\{p,n\},HB}}$ – total voltage of the corresponding SMC, $v_{\{\mathrm{p,n}\},\mathrm{FB}}$, $v_{\{\mathrm{p,n}\},\mathrm{HB}}$ – total inserted voltage of the corresponding SMC.

B. H-MMC equivalent circuit and energy dynamics

Following Fig. 1, all the SMs of H-MMC branch can be presented as two equivalent SMCs, corresponding to N_{FB} and N_{HB} individual SMs, as in Fig. 3. At the moment, the actual number of FB and HB SMs is irrelevant, and will be discussed later. If the full potential of FB units is used for negative voltage insertion, reference waveforms of the FB (4) and the HB (5) strings are derived from (1), assuming $\theta_s = 0$.

$$v^*_{\{\mathrm{p,n}\},\mathrm{FB}} = \mp \frac{m_s V_{\mathrm{DC,n}}}{2} (1 - k_{\mathrm{DC}}) \cos(\omega_s t) \tag{4}$$

$$v^*_{\{\mathrm{p,n}\},\mathrm{HB}} = \mp \frac{m_s V_{\mathrm{DC,n}}}{2} k_{\mathrm{DC}} \cos(\omega_s t) + \frac{k_{\mathrm{DC}} V_{\mathrm{DC,n}}}{2} \tag{5}$$

Average FB (6) and HB (7) SMC energies within one branch reveal that, even though total branch energy averages to zero, i.e. $\overline{w}_{\{\mathrm{p,n}\},\mathrm{FB}} + \overline{w}_{\{\mathrm{p,n}\},\mathrm{HB}} = 0$, SMC energies are diverging (Fig. 4), as HB SMC has positive bias in exchange with DC link, while FB SMC only exchanges energy with AC terminals. Note that DC current amplitude is presented as a function of AC-side current, derived from the AC and DC active power equality requirement (2). Thus, insertion references modification is necessary to ensure zero-average energy of individual SMCs.

$$\overline{w}_{\{\mathrm{p,n}\},\mathrm{FB}} = \underbrace{-\frac{m_s V_{\mathrm{DC,n}} \hat{i}_s \cos(\varphi_s)}{8} (1 - k_{\mathrm{DC}}) t}_{\overline{w}_{\mathrm{AC}} \text{ non-zero average}} \tag{6}$$

$$\overline{w}_{\{\mathrm{p,n}\},\mathrm{HB}} = \underbrace{-\frac{m_s V_{\mathrm{DC,n}} \hat{i}_s \cos(\varphi_s)}{8} k_{\mathrm{DC}} t}_{\overline{w}_{\mathrm{AC}} \text{ non-zero average}} + \underbrace{\frac{m_s V_{\mathrm{DC,n}} \hat{i}_s \cos(\varphi_s)}{8} t}_{\overline{w}_{\mathrm{DC}} \text{ non-zero average}} \tag{7}$$

It is evident that only FB SMs can be used to insert negative portion of the branch voltage during the corresponding part of the cycle, which can be defined as $\omega_s t \in [\theta_1, \theta_2]$ (see

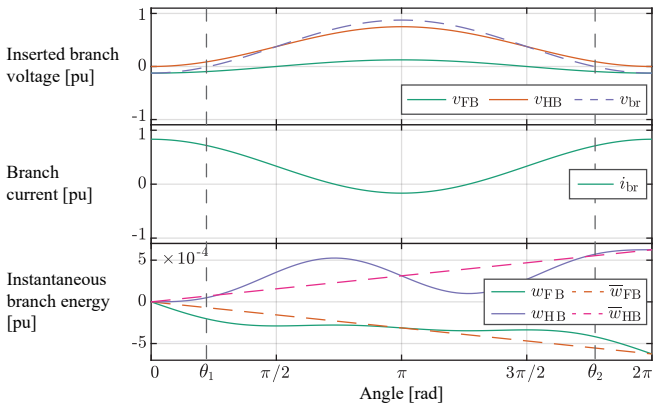

Fig. 4. Per unit branch-level waveforms over one fundamental cycle of H-MMC AFE stage, for the following parameters: $m_s = 1$, $\hat{i}_s = 1$, $\cos(\varphi_s) = 1$, $k_{\mathrm{DC}} = 0.75$. From top to bottom: inserted branch voltage of FB-, HB-string, and total inserted voltage; branch current; instantaneous and average power of FB and HB strings, instantaneous and average energy of FB and HB strings. Angles θ_1 and θ_2 denote zero-crossing of inserted branch voltage.

Fig. 4). The duration of branch-level negative voltage insertion requirement can be determined from zero-crossing of (1), as an interval $\theta \in (\theta_2, \theta_1)$, $\theta_{\{1,2\}} = \pm\left(\arccos\left(k_{\mathrm{DC}}/m_s\right) - \theta_s\right)$.

Once the branch-level inserted voltage reference is positive, i.e. in $\theta \in (\theta_1, \theta_2)$ interval, insertion references of FB (4) and HB (5) SMCs can be altered, to achieve zero-average power and energy, consequently equal loading of the two SMCs over the fundamental period.

$$\overline{w}_{\{\mathrm{p,n}\},\mathrm{FB}} = \overline{w}_{\{\mathrm{p,n}\},\mathrm{HB}} = 0 \tag{8}$$

As the zero-crossing instants of the inserted branch-level voltage v_{br} differ when varying either k_{DC} or m_s, FB SM insertion reference alteration can as well be performed at zero-crossing of AC component of (4) and (5), which is always equal to $\theta_{\{1,2\}} = \{\pi/2 - \theta_s, 3\pi/2 - \theta_s\}$. Branch-level insertion voltage is always positive for the given range, thus insertion references can be altered in a way presented in Fig. 5. During negative AC-side voltage reference value, all the SMs of the FB SMC are inserting AC-only voltage (4), while all the SMs of the HB SMC are inserting AC voltage with DC offset (5). During this half-period, FB SMC only exchanges energy with AC-side, thus SMs are discharged, while HB SMC exchanges a portion of AC-side energy and all DC-side energy, causing corresponding SMs to charge. Once the branch-level AC voltage component is positive, FB SMC insertion reference must be added a certain DC component, such that energy can be exchanged with DC link as well, and satisfy (8).

Starting from (6)-(7), keeping in mind that voltage insertion reference is to be altered once per half-cycle, it is straightforward to derive required SMCs' inserted DC voltage component reference modification. Energy exchange share over the negative AC voltage half-cycle is given in Table II.

Each SMC must exchange equal energy with DC and AC terminals to ensure equilibrium. The required FB and HB average energy over the positive AC voltage half-cycle is

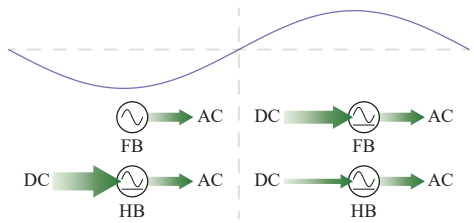

Fig. 5. Insertion strategy of the FB and HB SMs. During negative value of AC component of inserted branch voltage (left), FB SMC inserts AC-only voltage (4), while HB SMC inserts AC components with DC offset (5). Energy imbalance between SMCs is caused by non-equal energy share. During positive value of AC component of inserted branch voltage (right), FB SMC is inserting AC voltage with DC offset. In this way, FB SMs are charged from DC side to compensate for the unequal loading. HB SMC DC voltage insertion component is proportionally reduced.

TABLE II
AVERAGE ENERGY EXCHANGE SHARE BETWEEN FB AND HB SMC OF ONE CONVERTER BRANCH, OVER THE NEGATIVE AC VOLTAGE HALF-CYCLE, FOR INSERTION REFERENCES (4)-(5).

Terminals	HB SMC	FB SMC
AC	k_{DC}	$1 - k_{\mathrm{DC}}$
DC	1	0

defined by DC voltage insertion compensation factors, k_{cFB} and k_{cHB} (9), where $T_{\mathrm{fund}} = 1/\omega_s$.

$$\frac{k_{\mathrm{DC}}}{1 - k_{\mathrm{DC}}} = \frac{k_{\mathrm{DC}} + k_{\mathrm{cHB}}}{0 + k_{\mathrm{cFB}}} \cdot \frac{T_{\mathrm{fund}}}{2} \tag{9}$$

Compensation factors are chosen to not alter the total inserted DC voltage amplitude, $k_{\mathrm{DC}} = k_{\mathrm{cHB}} + k_{\mathrm{cFB}}$.

$$k_{\mathrm{cHB}} = k_{\mathrm{DC}}(2k_{\mathrm{DC}} - 1) \quad (10) \qquad k_{\mathrm{cFB}} = 2k_{\mathrm{DC}}(1 - k_{\mathrm{DC}}) \quad (11)$$

Positive AC voltage half-cycle SMC references are obtained.

$$\begin{aligned} v^*_{\{\mathrm{p,n}\},\mathrm{FB,pos}} &= \mp\frac{m_s V_{\mathrm{DC,n}}}{2}(1 - k_{\mathrm{DC}})\cos(\omega_s t) \\ &\quad + V_{\mathrm{DC,n}} k_{\mathrm{DC}}(1 - k_{\mathrm{DC}}) \end{aligned} \tag{12}$$

$$\begin{aligned} v^*_{\{\mathrm{p,n}\},\mathrm{HB,pos}} &= \mp\frac{m_s V_{\mathrm{DC,n}}}{2} k_{\mathrm{DC}}\cos(\omega_s t) \\ &\quad + \frac{V_{\mathrm{DC,n}}}{2} k_{\mathrm{DC}}(2k_{\mathrm{DC}} - 1) \end{aligned} \tag{13}$$

Due to HB SMs being limited to positive insertion voltage operation, presented compensation method is applicable to the DC link voltage reduction range of (14), as illustrated in Fig. 6.

$$V_{\mathrm{DC}} \in [k_{\mathrm{DC,min}}, 1] V_{\mathrm{DC,n}} \quad (14) \qquad k_{\mathrm{DC,min}} = 1/2 \quad (15)$$

Average SMC energies are integrated starting from (12)-(13) and (2).

$$\begin{aligned} \overline{w}_{\{\mathrm{p,n}\},\mathrm{FB,pos}} &= \underbrace{\frac{m_s V_{\mathrm{DC,n}} \hat{i}_s \cos(\varphi_s)}{4}(1 - k_{\mathrm{DC}})t}_{\overline{w}_{\mathrm{DC}} \text{ non-zero average}} \\ &\quad - \underbrace{\frac{m_s V_{\mathrm{DC,n}} \hat{i}_s \cos(\varphi_s)}{8}(1 - k_{\mathrm{DC}})t}_{\overline{w}_{\mathrm{AC}} \text{ non-zero average}} \end{aligned} \tag{16}$$

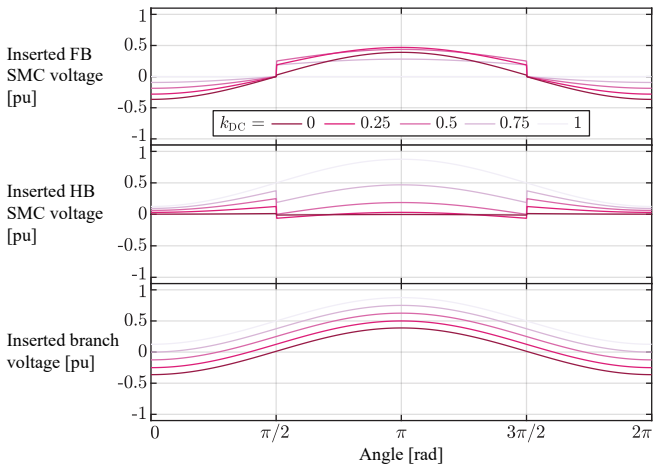

Fig. 6. Modified insertion references for FB and HB SMCs, compensating for discrepancies in constant power delivered from the two SMCs of a branch.

$$\overline{w}_{\{p,n\},HB,pos} = \underbrace{\frac{m_s V_{DC,n}\hat{i}_s \cos(\varphi_s)}{8}(2k_{DC}-1)t}_{\overline{w}_{DC}\text{ non-zero average}} - \underbrace{\frac{m_s V_{DC,n}\hat{i}_s \cos(\varphi_s)}{8}k_{DC}t}_{\overline{w}_{AC}\text{ non-zero average}} \tag{17}$$

Energy imbalance of the FB and HB SMCs over one fundamental cycle is further obtained (18)-(19).

$$\Delta w_{FB,cycle} = \int_{-\pi/2}^{\pi/2} p_{\{p,n\},FB,neg}\,dt + \int_{\pi/2}^{3\pi/2} p_{\{p,n\},FB,pos}\,dt = -\frac{V_{dc,n}\hat{i}_s \cos(\varphi_s)}{\omega_s}k_{DC}(1-k_{DC}) \tag{18}$$

$$\Delta w_{HB,cycle} = \int_{-\pi/2}^{\pi/2} p_{\{p,n\},HB,neg}\,dt + \int_{\pi/2}^{3\pi/2} p_{\{p,n\},HB,pos}\,dt = \frac{V_{dc,n}\hat{i}_s \cos(\varphi_s)}{\omega_s}k_{DC}(1-k_{DC}) \tag{19}$$

$$\Delta w_{br,cycle} = \Delta w_{FB,cycle} + \Delta w_{HB,cycle} = 0 \tag{20}$$

Even though non-oscillatory instantaneous power components of the negative AC voltage half-cycle have been identified and compensated for in the positive AC voltage half-cycle (Fig. 6), the fact that oscillatory members of instantaneous power equations are now also being altered twice per cycle results in non-zero-average energy originating from such oscillatory components. Following (18)-(19), additional active power of exchange between FB and HB SMCs must equal (21) over the fundamental period. In constant-torque VSD application, where active power is proportional to machine angular frequency, i.e. to k_{DC}, maximal value is seen at $k_{DC} = 2/3$.

$$P_{\Delta SMC} = \frac{V_{DC,n}\hat{i}_s \cos(\varphi_s)}{2\pi}k_{DC}(1-k_{DC}) \tag{21}$$

The power amplitude requirement of newly introduced balancing component (21) is presented over the operating range (14) in Fig. 7, for $m_s = 1$.

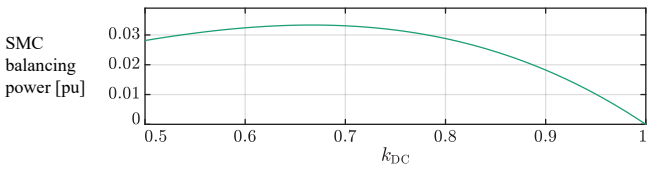

Fig. 7. SMC balancing power amplitude requirement over the operating range of variable DC link voltage. If the converter supplies constant-torque machine, i.e. active power is proportional to angular frequency, maximal value is seen at $k_{DC} = 2/3$ (21).

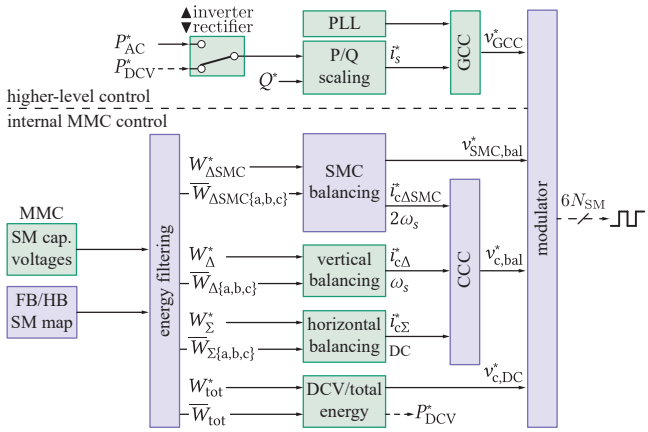

Fig. 8. H-MMC control outline is presented. Starting from standard MMC control (green), SMC balancing layer is added to the internal control. A FB/HB SM map is required for proper SMC energy measurement and control. Modulator is presented in more details in Fig. 11. Upper-level control is unaffected, comprising grid-code-compliant scaling of active (P) and reactive (Q) power references, followed by grid current controller (GCC), synchronized to the grid through phase-locked loop (PLL).

III. H-MMC Energy Balancing

The concept adopted is to preserve internal control of a conventional MMC, i.e. horizontal, vertical and total energy control, while adding a control layer to balance FB and HB SMCs at the branch level.

A. Branch-level energy balancing

From the branch-level up, H-MMC topology control is identical to conventional MMC, as highlighted in green on Fig. 8. Higher-level control comprises active (P^*_{AC}) and reactive (Q^*) power reference tracking, followed by reference scaling with respect to converter current capacity and grid-code-imposed requirements. AC-side voltage references are generated by phase-locked loop-enabled grid current control.

Horizontal, vertical and total energy balancing is performed as described by the first method of [18]. Horizontal and vertical balancing actions are purely internal to the MMC. Current references are passed to Circulating Current Control (CCC), and the action is not visible from either AC or DC terminals. Total energy controller has a different role for rectifier and inverter operation. In the first case, grid-side power reference is generated (P^*_{DCV}) to match DC-side power demand, keeping the total converter state-of-charge constant. In the second case, DC link current is controller to supply AC-side reference power of the converter.

B. SMC energy balancing

Within converter branches, an additional control layer is required to compensate for unequal DC-side energy exchange of the SMCs (21), highlighted in violet in Fig. 8. To establish active power transfer between FB and HB SMCs within the same converter branch, without altering AC and DC terminal values of the converter, additional circulating current and voltage components are used, ensuring these will only produce non-zero-average active power transfer between themselves. Such components must not interfere with DC and fundamental frequency AC components, thus multiples of two of fundamental frequency can be considered. AC circulating current at $2\omega_s$ is employed (22), along with additional FB and HB SMC voltage references at $2\omega_s$ (23).

$$i_{\mathrm{c}\Delta\mathrm{SMC}} = \hat{i}_{\mathrm{c}\Delta\mathrm{SMC}} \cos(2\omega_s t) \tag{22}$$

$$v^*_{\mathrm{SMC,bal,\{FB,HB\}}} = \pm\hat{v}_{\mathrm{SMC,bal}} \cos(2\omega_s t) \tag{23}$$

To satisfy zero-sum current at DC terminals, a symmetrical three-phase system is introduced, satisfying (24).

$$\sum \vec{i}_{\mathrm{c}2\omega\{\mathrm{a,b,c}\}} = 0 \tag{24}$$

This current component flows through both upper and lower branch of a phase leg, interacting with AC and DC components of the inserted FB and HB SMCs.

- **Interaction with DC voltage components** introduces zero-average oscillating power at $2\omega_s$.
- **Interaction with AC voltage components** at ω_s introduces zero-average oscillating power components at ω_s and $3\omega_s$, as AC voltage insertion reference is kept unchanged over the fundamental cycle (4),(5),(12),(13).
- **Interaction with balancing AC voltage component** at $2\omega_s$ introduces non-zero-average active power and a zero-average oscillating component at $4\omega_s$.

Due to opposing phase of (23), exchange of energy between the SMCs of the same branch is compensating the energy imbalance over the fundamental cycle (18)-(19).

As the number of SMs within FB and HB SMCs can be non-equal, SMC differential energy reference is defined by the FB to HB ratio (25). Note that differential energy reference (25) shall be multiplied by two in the corresponding controller, as phase-leg-level circulating current controls SMC energy balancing in both upper and lower branch.

$$\begin{aligned} W^*_{\Delta\mathrm{SMC}} &= \frac{1}{2}\left(\frac{(\Sigma V_{\mathrm{SM,HB}})^2}{N_{\mathrm{HB}}} - \frac{(\Sigma V_{\mathrm{SM,FB}})^2}{N_{\mathrm{FB}}}\right) C_{\mathrm{SM}} \\ &= \frac{C_{\mathrm{SM}} V^*_{\mathrm{SM}}}{2}(N_{\mathrm{HB}} - N_{\mathrm{FB}}) \end{aligned} \tag{25}$$

Compared to the phase-leg-level vertical balancing, SMC energy balancing shares the same control approach, however on a branch-level. Thus, the same control structure can be used [19], as implemented in the first method of [18]. Firstly, balancing current components are calculated per-phase. Further, for each phase current component, reactive components are injected into the remaining two phases, to satisfy (24).

As in other energy balancing actions, SMC controller feedback is a filtered-out differential energy, determined from capacitor voltage measurements based on (25). Thus, SM mapping, i.e. disposition of FB and HB SMs within a branch is fed to the energy controller (Fig. 8).

TABLE III
H-MMC PARAMETERS USED IN THE TEST SCENARIOS, GIVEN IN BOTH ABSOLUTE AND PER UNIT VALUES, WITH LINE VOLTAGE AND THREE-PHASE APPARENT POWER BEING BASE VALUES. PLEASE NOTE THAT CAPACITANCE AND INDUCTANCE IMPEDANCE VALUES ARE GIVEN FOR FUNDAMENTAL FREQUENCY, I.E. 50 Hz.

Parameter	Symbol	Value	Per-unit
Line voltage	U_{n}	6 kV	1 pu
Apparent power	S_{n}	0.5 MVA	1 pu
Grid frequency	f_{n}	50 Hz	-
Number of SMs per branch	N_{SM}	16	-
SM voltage	V_{SM}	650 V	0.108 pu
SM capacitance (tolerance ±10%)	C_{SM}	2.25 mF	0.02 pu
Branch inductance	L_{br}	2.5 mH	0.011 pu
Branch inductance coupling coeff.	k_{br}	0.3	-
Branch resistance	R_{br}	50 mΩ	$7 \cdot 10^{-4}$pu
Switching frequency	f_{sw}	1 kHz	-

IV. H-MMC DESIGN

With the control concept defined, the first step in H-MMC design assumes deciding on minimal required DC link voltage, i.e. selecting $k_{\mathrm{DC,min}}$ from the available range (15). This determines the amplitude of negative insertion voltage needed for an ideally balanced converter (4), which still does not lead to the correct selection of FB/HB SM ratio. As presented in Section III, additional SMC balancing voltage and current requirements must be taken into account, which affect the insertion voltage amplitude requirement of FB and HB SMCs. Relying on these results, and adding energy balancing requirements of a uniform-SM MMC, insertion voltage budget has been calculated for each of the control loops. As a design example, values corresponding to a medium-voltage MMC unit are introduced in Table III, both in absolute and per unit manner, with converter line voltage and three-phase apparent power chosen as base units. These ratings are used in test scenarios later on. Please note that, since inductance and capacitance represent frequency-dependent impedances, these are given for fundamental 50 Hz frequency in per unit system. Scaling to another frequency, e.g. for second harmonic impedance, is straightforward.

A. SMC insertion voltage waveform

The next step in converter design assumes defining FB and HB SMC insertion voltage waveforms. Insertion references are derived for the two AC-side voltage half cycles of Fig. 5 – negative in (4)-(5) and positive in (12)-(13). A generalized expression over the fundamental cycle is given (26)-(27), expanding the above equations to comprise converter control voltage components: $\hat{v}_{\mathrm{c,bal}}$ – circulating current control, $\hat{v}_{\mathrm{c,bal},2\omega_s}$ – SMC-balancing current control, $\hat{v}_{\mathrm{c,bal,SMC}}$ – SMC-balancing voltage component.

Analogously to improvement in DC link utilization through injection of CM voltages to AC-side phase voltage waveforms, third harmonic of SMC balancing voltage is introduced. Waveforms (26)-(27) are graphically

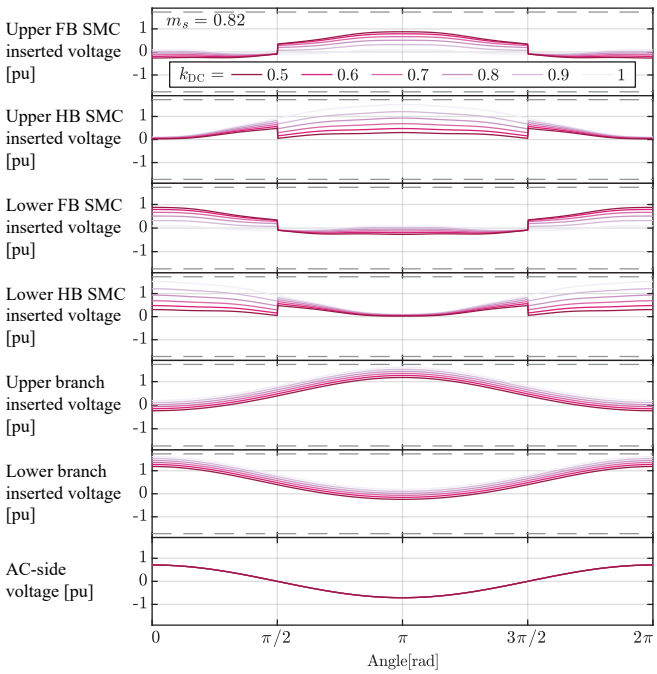

Fig. 9. Branch insertion indexes of phase a are presented, comprising all the voltage components (26)-(27), of the amplitudes calculated within the voltage budget section. Voltage budget utilization is improved through third harmonic injection for SMC balancing voltage, at $6\omega_s$. The minimal voltage of HB SMC reference equals $0.029\,\mathrm{pu}$ at $k_{\mathrm{DC}} = 0.5$. Dashed lines represent available branch voltage.

presented in Fig. 9, for required modulation index of $m_{\mathrm{s,req}} = 2\hat{v}_{\mathrm{ph}}/(1.15V_{\mathrm{DC,n}}) = 0.821$. Minimal voltage of HB SMCs over the cycle, for attainable DC voltage reduction factor range $k_{\mathrm{DC}} \in [0.5, 1]$ equals $0.029\,\mathrm{pu}$, meaning the converter can be realized with selected design choices without violation of HB electrical limit.

$$\begin{aligned} v^*_{\{\mathrm{p,n}\},\mathrm{FB,cycle}} &= \mp\frac{m_s V_{\mathrm{DC,n}}}{2}(1-k_{\mathrm{DC}})\cos(\omega_s t) \\ &+ \frac{N_{\mathrm{FB}}}{N_{\mathrm{SM}}}\left[\hat{v}^*_{\mathrm{c,bal}}\cos(\omega_s t+\pi/2) + \hat{v}^*_{\mathrm{c,bal},2\omega_s}\cos(2\omega_s t+\pi/2)\right] \\ &+ \hat{v}^*_{\mathrm{c,bal,SMC}}\cos(2\omega_s t) \\ &+ \begin{Bmatrix} V_{\mathrm{DC,n}}k_{\mathrm{DC}}(1-k_{\mathrm{DC}})(v_s \le 0) & \{\mathrm{p,n}\} = \mathrm{p} \\ V_{\mathrm{DC,n}}k_{\mathrm{DC}}(1-k_{\mathrm{DC}})(v_s \ge 0) & \{\mathrm{p,n}\} = \mathrm{n} \end{Bmatrix} \end{aligned} \quad (26)$$

$$\begin{aligned} v^*_{\{\mathrm{p,n}\},\mathrm{HB,cycle}} &= \mp\frac{m_s V_{\mathrm{DC,n}}}{2}k_{\mathrm{DC}}\cos(\omega_s t) \\ &+ \frac{N_{\mathrm{HB}}}{N_{\mathrm{SM}}}\left[\hat{v}^*_{\mathrm{c,bal}}\cos(\omega_s t+\pi/2) + \hat{v}^*_{\mathrm{c,bal},2\omega_s}\cos(2\omega_s t+\pi/2)\right] \\ &+ \hat{v}^*_{\mathrm{c,bal,SMC}}\cos(2\omega_s t+\pi) + (k_{\mathrm{DC}}V_{\mathrm{DC,n}}/2)\cdot \\ &\cdot \begin{Bmatrix} [(v_s \ge 0) + (2k_{\mathrm{DC}}-1)(v_s \le 0)] & \{\mathrm{p,n}\} = \mathrm{p} \\ [(v_s \le 0) + (2k_{\mathrm{DC}}-1)(v_s \ge 0)] & \{\mathrm{p,n}\} = \mathrm{n} \end{Bmatrix} \end{aligned} \quad (27)$$

B. Determination of required FB/HB share

Due to higher device count and consequently higher losses of FB SMs compared to HB alternative, their number is selected as the minimal value that satisfies voltage insertion requirement (26). For the case of arbitrary k_{DC}, with CM voltage injection for both AC-side voltage and SMC balancing voltage, maximum FB SMC voltage requirement is obtained from (26) and Fig. 9. In the worst-case scenario of the minimal DC link voltage attainable by this method (15), maximal FB insertion voltage reference (28) leads to FB SM count (29). The same can be determined for an arbitrary DC link voltage reduction ratio, as in Table IV.

TABLE IV
H-MMC FB SMs REQUIREMENT FOR VARIOUS DEGREES OF DC LINK VOLTAGE REDUCTION.

k_{DC}	$\max(\hat{v}_{\mathrm{ins,FB}})$ [pu]	$N_{\mathrm{FB,min}}$[%]	N_{FB}
1	0	0.0%	0
0.95	0.196	11.3%	2
0.9	0.32	18.5%	3
0.85	0.434	25.1%	5
0.8	0.537	31.0%	5
0.75	0.63	36.3%	6
0.7	0.711	41.0%	7
0.65	0.782	45.1%	8
0.6	0.843	48.6%	8
0.55	0.893	51.5%	9
0.5	0.933	53.8%	9

$$\max_{k_{\mathrm{DC}}=0.5}\left(\hat{v}_{\mathrm{ins,FB,\{p,n\}}}\right) = 0.878\,\mathrm{pu} \quad (28)$$

$$N_{\mathrm{FB}} = \left\lceil \frac{\max_{k_{\mathrm{DC}}=0.5}\left(\hat{v}_{\mathrm{ins,FB,\{p,n\}}}\right)V_{\mathrm{b}}}{V_{\mathrm{SM}}} \right\rceil = 9(56\,\%) \quad (29)$$

V. Virtual SMs at variable DC voltage operation

A number of SMs $N_{\mathrm{FB,sel}}$ selected for a certain $k_{\mathrm{DC,sel}}$ will also enable operation at any higher DC link voltage value up to rated, i.e. $k_{\mathrm{DC}} \ge k_{\mathrm{DC,sel}}$, through appropriate control actions.

A. Virtual SM concept

For converter operation at lowest designed level of DC link voltage, e.g. $k_{\mathrm{DC,sel}} = 0.5$, the required number of FB and HB SMs corresponds to the actual number of installed SMs, (29). Phase-Shifted Carrier (PSC) pulse-width modulation is implemented, thus SMs of individual SMCs are provided with a set of PSCs, as presented in the leftmost part of Fig. 10.

As the operating point is shifted towards higher DC voltage values, $k_{\mathrm{DC}} > k_{\mathrm{DC,sel}}$, the minimal required share of FB SMs reduces (Table IV). For an example of $k_{\mathrm{DC}} = 0.8$ (center part of Fig. 10), the minimal number of FB SMs are assigned (mapped) to FB SMC, and quantified as N_{FBv}. The remaining number on installed FB units, $N_{\mathrm{FB}} - N_{\mathrm{FBv}}$, is mapped to the HB SMC, and operate as virtual HB SMs. The new number of SMs operating as HB thus increases to $N_{\mathrm{HBv}} = N_{\mathrm{SM}} - N_{\mathrm{FBv}}$. The corresponding PSCs are assigned to N_{FBv} and N_{HBv}, as in middle section of Fig. 10. Further increase in DC voltage leads to the other extreme – for $k_{\mathrm{DC}} = 1$, all the FB SMs operate as virtual HB, as in rightmost section of Fig. 10.

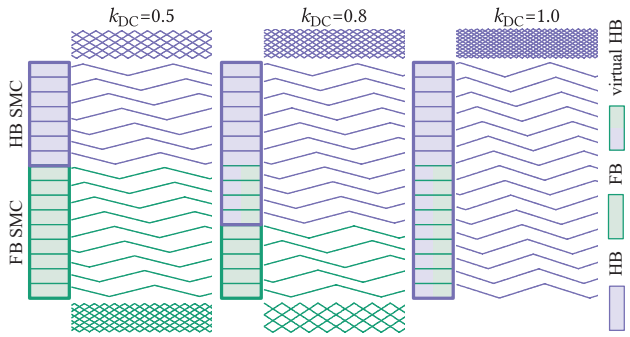

Fig. 10. PSC generation strategy is presented. The leftmost column presents operation at lowest k_{DC} value. Increasing DC link voltage value, a certain number of FB SMs must be operated as HB, denoted *virtual HB*, following Table IV. Note that actual switching frequency of unipolar-modulated FB operated with positive-only reference is 50 % lower compared to FB operation.

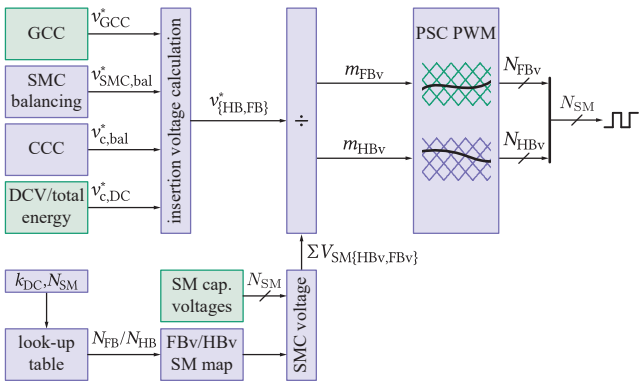

Fig. 11. Modulation scheme of H-MMC is presented, with conventional MMC control blocks in green and newly-introduced blocks in violet. Required FB/HB ratio for operating point (k_{DC}) and SM count (N_{SM}) is determined from the look-up Table IV. As k_{DC} rises, a part of FB SMs is being assigned to HB SMC and operated as *virtual HB*. Resulting SM mapping is used to correctly sum available SMC voltages, and calculate insertion indexes. Two sets of PSCs are generated, as illustrated in Fig. 10.

B. H-MMC modulation

To perform correct control of H-MMC, modulation is performed as illustrated in Fig. 11. In case $N_{FB} = N_{FBv}$, insertion voltage references (26)-(27) are compared to available voltages of FB and HB SMCs, thus insertion indexes are obtained, as presented in the leftmost part of Fig. 11. These are fed to two sets of PSCs, determined as in Fig. 10, to generate gate pulses for individual SMs of the SMCs.

With further rise in DC voltage reference, e.g. $k_{DC} = 0.8$, some FB SMs are assigned to HB SMC (Fig. 10, middle). Starting from the actual number of installed SMs, N_{FB} and N_{HB} and their disposition within converter branch, all the SMs are reassigned to virtual N_{FBv} and N_{HBv} SMC strings and mapped to corresponding SMCs. Measured SM capacitor voltages are then added-up to determine available SMC voltages, denoted $\Sigma V_{SM\{HBv,FBv\}}$. Closed-loop control is performed, where insertion voltage references (26)-(27) are divided by available measured voltages, to generate modulation indexes for SMs of the two SMCs – m_{FBv} and m_{HBv}. Two sets of PSCs are used, assigned to individual SMs as in Fig. 10. Gate signals are fed to corresponding SMs using the determined FBv/HBv SM map. Concerning SMC energy balancing described in Subsection III-B, SM map from Fig. 8 is replaced by the FBv/HBv SM map of Fig. 11.

VI. Test scenario and results

H-MMC-based AFE converter performance have been verified through high-fidelity switched-model simulations of the medium-voltage ratings converter (Table III). Three test scenarios were observed – unity- and variable power factor operation, at rated DC current value being the worst-case, as well as constant-torque machine start-up sequence at variable DC voltage.

A. Unity power factor operation

The ability to operate converter at unity power factor is demonstrated in test scenario of Fig. 12. DC link voltage reference is gradually increased from $k_{DC} = 0.5$ in 0.1 steps up to the rated value. DC load is controlled to maintain rated DC current value. Operating at unity power factor, active- and reactive (zero) power references are correctly tracked, while sum- and differential capacitor voltages are kept well below marked $\pm 10\,\%$ limit.

B. Variable power factor operation

Converter operation is tested at variable reactive power demand, for two DC link voltage operating points – the lowest ($k_{DC} = 0.5$) and the highest, i.e. rated value, as presented in Fig. 13. DC link current is kept at rated value throughout the test, while reactive power reference is varied in $\pm 0.2 S_n$ range. Both active and reactive power references are tracked correctly by the AFE control, while sum- and differential branch-level capacitor voltages are kept below the introduced $\pm 10\,\%$ limits.

C. Constant-torque machine start-up

While presented variable DC voltage H-MMC operation is clearly not limited to supplying VSDs, the paper is dominantly motivated by this application. Thus, the third test-scenario presents constant-torque machine start-up sequence of a 6 kV, 0.5 MVA synchronous unit, matching the MMC ratings (Table III). Machine-side MMC is HB-based (Fig. 1, right), supplied from a H-MMC AFE stage.

Following machine-side MMC energy ripple expression (3), we can conclude that energy oscillation of the dominant (first) term will be constant if ratio of DC link voltage to output frequency is constant. Thus, for this specific application, we will aim to maintain $k_{DC} V_{DC,n} / \omega_{sm} = \text{const}$, where w_{sm} denotes electrical angular frequency of the machine. As the presented H-MMC control method has a maximal DC link voltage range of $[0.5, 1] V_{DC,n}$, DC link voltage reference when supplying an electrical machine is obtained as follows.

$$V_{DC} = \begin{Bmatrix} V_{DC,n}/2 & |\omega_{sm}| \in (0 \ldots 0.5]\, \omega_{sm,rated} \\ k_{DC} V_{DC,n} & |\omega_{sm}| \in (0.5 \ldots 1]\, \omega_{sm,rated} \end{Bmatrix} \quad (30)$$

In the LF operating region, below half the rated speed, where $k_{DC} V_{DC,n} / \omega_{sm} \neq \text{const}$, capacitor voltage balancing is

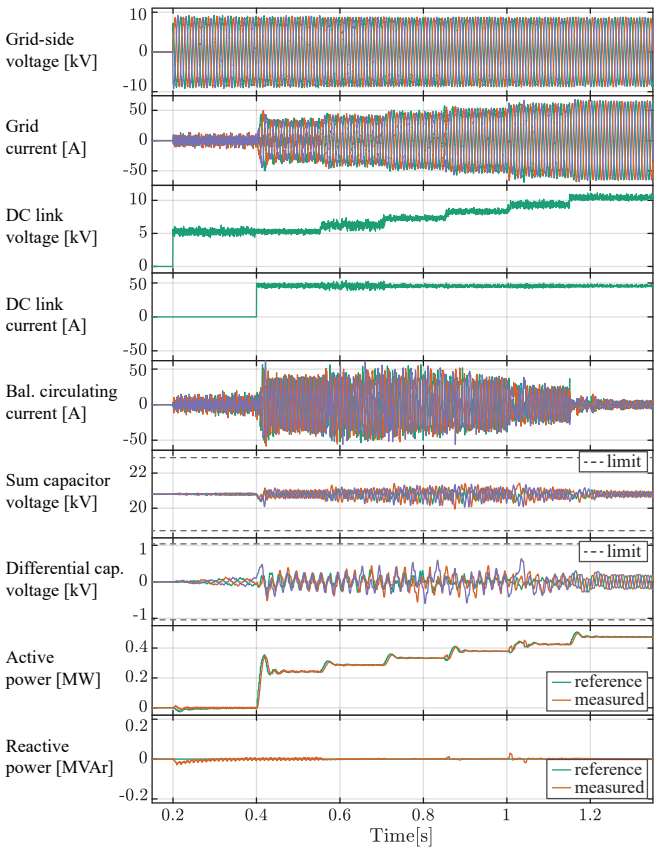

Fig. 12. H-MMC operation sequence at variable DC link voltage and rated DC link current operation over the complete operating range and unity power factor. Active and reactive power references are correctly tracked, while sum- and differential capacitor voltages ripple is driven well below marked 10 % limit.

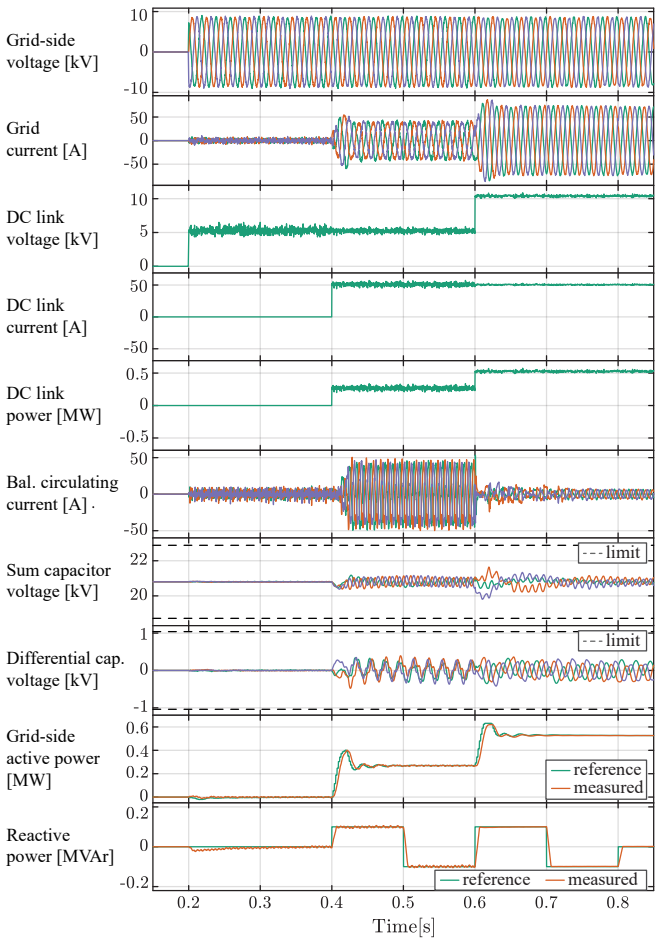

Fig. 13. H-MMC converter opeartion for two extreme DC link voltage setpoints, under varying power factor, is presented. Branch-level sum- and differential capacitor voltages are kept under balance, while active and reactive power references are correctly tracked. DC link current is kept at rated value throughout the test sequence.

performed utilizing CM voltage and appropriate circulating current components as in [10]. Following (3) and aforementioned DC voltage limit, DC link voltage reference is kept at the lowest level up to 50 % of rated machine frequency. Further, it is set in proportion to the output frequency, in steps of $0.1V_{\mathrm{DC,n}}$. This strategy decreases CM voltage amplitude by 50 % in the lowest machine frequency region, compared to [10], keeping the same circulating balancing current amplitude limit and allowed capacitor voltage ripple. Being less severe load to H-MMC compared to constant DC current test scenario of Subsection VI-A, only machine-side MMC performance has been presented here.

D. Spectral analysis of grid-side current

According to the "Recommended practice and requirements for harmonic control in electric power systems", published under IEEE 519-2014 guideline [20], harmonic current distortion limits are defined in percent of maximum demand load current, while Total Harmonic Distortion (THD) is normally related to ratio of all harmonics to fundamental component of the observed operating point.

Firstly, THD of the grid current for unity power factor test scenario, presented under Subsection VI-A, is calculated for each of the operating points. Further, Total Demand Distortion (TDD) is calculated by scaling the obtained partial load THD values to the rated value of fundamental grid current component, to comply with IEEE 519-2014 [21]. Maximal demand current rating was taken as fundamental current component at rated DC link voltage, $I_{1,\mathrm{rated}} = 71.6\,\mathrm{A}$, following Table V. TDD is calculated as $\mathrm{TDD_i} = \mathrm{THD_i} I_1 / I_{1,\mathrm{rated}}$.

Both sets of values are presented in Table V. While IEEE 519-2014 proposes TDD limit of 5 % for connection voltage up to 69 kV, the presented H-MMC approach surpasses this limit, having a maximal value of 6.1 %. Please note, however, that grid-code compatibility in terms of THD was not of primary concern when choosing converter ratings. In this light, either a slight increase in branch inductance value, or an addition of a line inductor, would pull down current THD below the proposed limit. Finally, a grid current spectrum has been presented at rated operating DC voltage, in Fig 15. Higher-order harmonics are present around the apparent switching frequency, i.e. $N_{\mathrm{SM}} f_{\mathrm{sw}} = 16\,\mathrm{kHz}$, while lower-order harmonics are of significantly lower amplitudes.

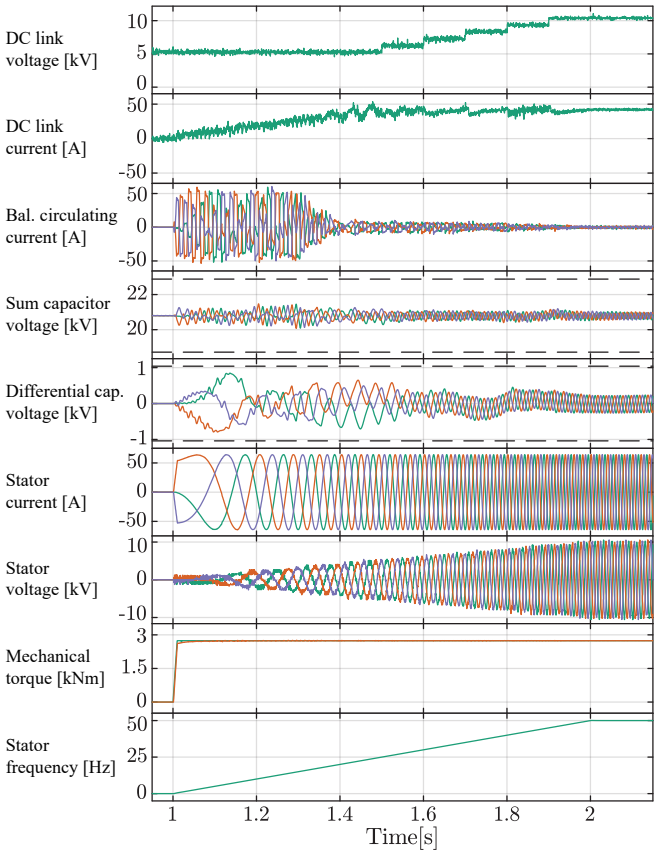

Fig. 14. Machine-side MMC operation during constant-torque machine start-up is presented. Below 50 % of rated frequency, DC link voltage is kept at the minimal value ($V_{\mathrm{DC,n}}/2$), resulting in 50 % lower CM voltage amplitude requirement for capacitor ripple limitation [10]. Further, above 50 % of rated frequency, DC voltage amplitude is incremented in proportion to output frequency, in steps of $0.1V_{\mathrm{DC,n}}$. In this way, SM capacitor ripple is kept well below the limits over the entire operating range.

TABLE V
H-MMC GRID CURRENT THD AND TDD FOR VARIOUS DC VOLTAGE REDUCTION VALUES, UNDER CONSTANT DC LINK CURRENT. I_1 REPRESENTS FUNDAMENTAL AC CURRENT COMPONENT AMPLITUDE, WHICH IS USED TO CALCULATE TDD AT PARTIAL LOADS, ACCORDING TO [20].

k_{DC}	0.5	0.6	0.7	0.8	0.9	1.0
I_1 [A]	37.0	43.2	50.3	57.4	64.3	71.6
$\mathrm{THD_i}$ [%]	11.8	7.0	4.5	3.9	5.1	1.7
$\mathrm{TDD_i}$ [%]	6.1	4.2	3.2	3.1	4.6	1.7

E. SMC energy control

SMC energy balancing controller action is presented in more details in Fig. 16, for test scenario of Subsection VI-A. Based on k_{DC} value, FB/HB ratio is determined from Table IV. Further, SMC balancing current limit is dynamically calculated and set, based on required balancing power at the operating point (21) and applied SMC balancing voltage component $\hat{v}_{\mathrm{c,bal,SMC}}$ (26)-(27), as seen in the third subplot of Fig. 16. Differential SMC energy reference of (25) is correctly tracked in all the phase-legs, as presented on the lowermost graph.

Capacitor voltage ripple of individual SMs grouped in FB and HB SMCs of upper and lower branch of a phase-leg, are presented in Fig. 17. Capacitance tolerance of $\pm 10\,\%$ is introduced in the converter model. Results confirm correct SM-level capacitor voltage control, as all units converge to the reference value of 650 V, over all values of k_{DC}, including transition between operating points.

F. Current capacity requirements of H-MMC

As elaborated in Subsection III-B, an additional control layer is introduced to H-MMC to enable energy equilibrium of FB and HB SMCs. As certain power of exchange between the two SMCs needs to be established through dedicated voltage and current components' interaction, there is a degree of freedom in favouring either lower voltage or lower current amplitudes for the task. Naturally, to keep the losses low, lower current is a preferred choice. On the other hand, converter branch voltage budget is limited, thus there is a limitation in SMC balancing voltage component increase. In this paper, SMC balancing voltage amplitude is set to a fixed amplitude of $\hat{v}_{\mathrm{c,bal,SMC}} = 0.132\,\mathrm{pu}$, excluding rated DC link voltage operation, where SMC balancing is obsolete, following zero power demand (21).

Peak current budget of a conventional MMC with either all-HB or all-FB SMs can be obtained neglecting SMC balancing demands. At the branch-level, the peak current budget is determined by per-branch AC- and DC-side current components, levied by balancing circulating current budget, chosen at $\hat{i}_{\mathrm{br,lim}} = 0.25\,\mathrm{pu}$.

$$\hat{i}_{\mathrm{br,lim}} = \hat{i}_{\mathrm{c,bal,lim}} + \frac{i_{\mathrm{DC,n}}}{3} + \frac{\hat{i}_{\mathrm{s,n}}}{2} = 0.852\,\mathrm{pu} = 71\,\mathrm{A} \quad (31)$$

Converter current components are presented in more details in Fig. 18. Three topmost graphs depict conventional horizontal and vertical MMC balancing components, as well as H-MMC-specific SMC balancing current. These references are summed up, and controlled by a single circulating current controller as in Fig. 8, realized through PIR controller, i.e. proportional, integral and resonant action, as it should control both AC and DC circulating current components. Total balancing circulating current reference and actual value are presented in the fourth subplot. Further, constant DC link current, and increasing AC-side current are presented. The lowermost graph plots the six branch currents and compares them to the peak current limit of the conventional MMC design approach (31). The maximum amplitude reached by the branch current of H-MMC in the test pattern of Subsection VI-A equals 82.5 A, or 16.2 % above the conventional design peak limit.

The obtained value represents the peak current over the entire operating range, at the worst-case scenario of rated DC current, corresponding to constant-torque machine operation in PHSP application (Fig. 1). Following (21), Fig. 16 and Fig. 18, SMC balancing current depends on both active power being transferred and DC link voltage reduction.

While this result definitely calls for SM peak current oversizing compared to HB- of FB-based MMC, the observed PHSP application should be kept in mind. Low DC link

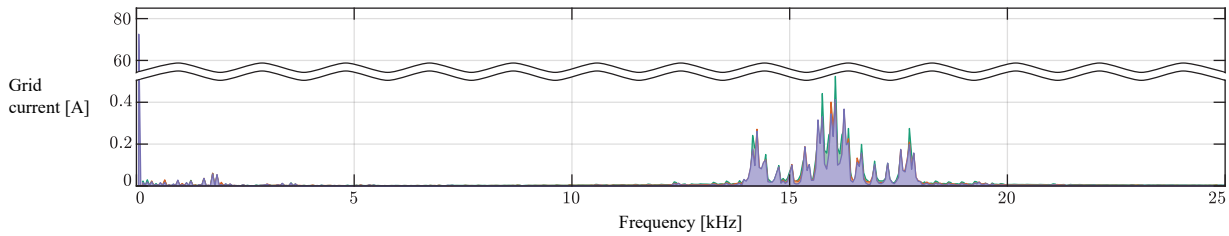

Fig. 15. Spectral composition of grid current is presented for rated DC link voltage and rated load. Please note the y-axis is cut for easier readout of both sub-ampere harmonic components' amplitudes and the dominant fundamental 50 Hz component. Higher harmonic amplitudes are dominant around apparent switching frequency of $N_{\mathrm{SM}} f_{\mathrm{sw}} = 16\,\mathrm{kHz}$.

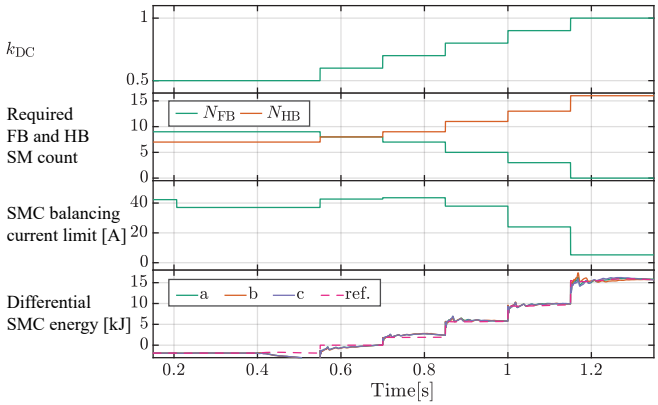

Fig. 16. SMC differential energy controller operation for test scenario of Fig. 12. For instantaneous ratio of $N_{\mathrm{FB}}/N_{\mathrm{HB}}$ SMs, differential energy reference is calculated using (25). Control action is limited as a function of AC-side output current, at constant value of SMC balancing voltage (23). Differential SMC controller tracks the reference correctly.

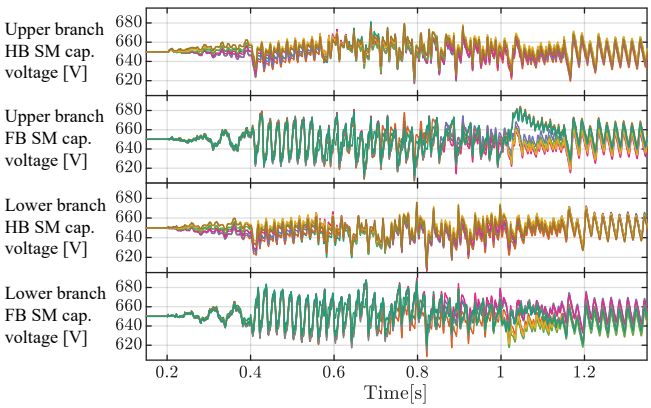

Fig. 17. HB and FB SMC capacitor ripple for test sequence is presented, for both upper and lower branch of a phase-leg. Voltage ripple is below $\pm 7\,\%$, i.e. 606 V to 692 V, at variable DC link voltage and rated DC link current operation over the complete operating range at $\cos\varphi_s = 1$.

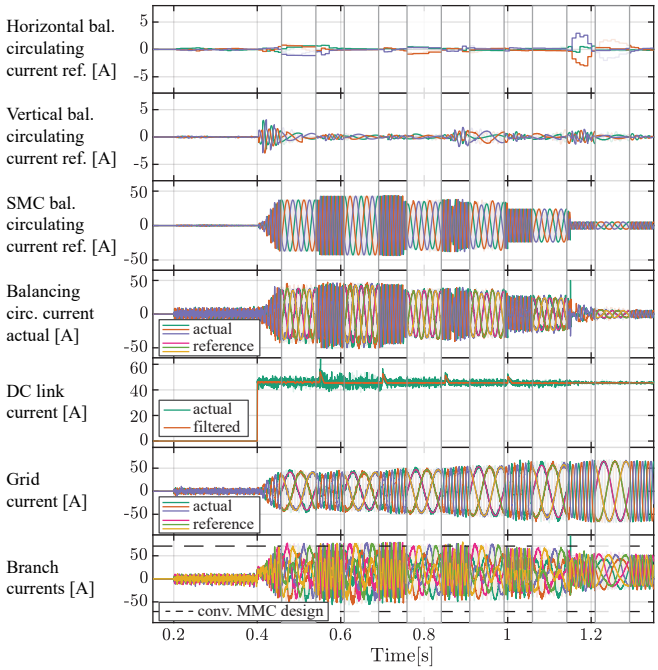

Fig. 18. Current components contributing to converter branch stress are presented for the first test scenario, i.e. unity power factor operation at variable DC link voltage reference. MMC-internal circulating currents are already presented per-branch. DC link current contributes as $i_{\mathrm{DC}}/3$ while AC-side current contributes with half of its amplitude. Lowermost graph presents the six branch currents and the peak branch current limit of conventional MMC design (71 A). In terms of peak current carrying capability, the maximal overload compared to conventional MMC is 82.5 A, or 16.2 %. For each operating point, i.e. for each DC link voltage value from $0.5V_{\mathrm{DC,n}}$ to rated, a zoomed-in semi-transparent area has been added to the graph, which represents waveforms in more details.

voltage value corresponds to low output machine frequency (3). In steady-state operation, machine output frequency is in a certain band around rated, typically up to 10 % below [22], where additional current stress is only slightly above design limit (Fig. 18).

As low speeds are used during pump/turbine change-over of operating regimes, the over-current scenario is likely to only happen in these transients. Moreover, if the machine is not operated in constant-torque, but rather towards natural quadratic torque pump characteristics, i.e. if active power is not linearly proportional to frequency, overload level can be additionally decreased. Further, the obtained current limit (31) can be decreased if voltage budget allows for increase in SMC balancing voltage component (23).

G. H-MMC to FB MMC comparison

At reduced DC link voltage operation, additional H-MMC SMC balancing control layer introduces certain additional current stress to semiconductors, compared to all-FB based

TABLE VI
SWITCHING AND CONDUCTING DEVICES COUNT OF H-MMC IN THREE OPERATING POINTS, COMPARED TO ALL-FB MMC. ALL NUMBERS ARE GIVEN RELATIVE TO THE TOTAL SM COUNT, WHILE DIODES ARE NEGLECTED.

kDC	Nfb	Nhb	FBv	HBv	switching	conducting
$[-1, 1]$	1	0	1	0	2	2
0.5	0.56	0.44	0.56	0.44	1.56	1.56
0.8	0.56	0.44	0.31	0.69	1.31	1.56
1	0.56	0.44	0	1	1	1.56

MMC (18). A question of H-MMC benefit thus arises, taking into account higher SM current rating that translates into higher initial converter cost and potentially higher losses. Starting from the presented H-MMC design (Table III), a comparison to its FB counterpart is made in Table VI, for three values of k_{DC}. At the lowest attainable value of $k_{\mathrm{DC}} = 0.5$, active semiconductor count is lower in H-MMC, however higher current stresses reduce this advantage. Further increase in DC link voltage amplitude causes an increasing fraction of FB SMs to operate as virtual HB units. Considering unipolar modulation, such a FB SM will only receive non-negative reference, upper switches will change state, while only one of the lower two will permanently conduct within the cycle. The closer to rated DC voltage the operating point is, the more pronounced this effect is. Finally, at $k_{\mathrm{DC}} = 1$, the same number of semiconductors is actively switching as in HB MMC.

Considering an application like VS PHSP, where low DC link voltage values occur only during transients, and operating range is in a certain range around rated frequency, the initially higher current requirements are compensated through exploitation benefits.

CONCLUSION

Variable DC link voltage operation of MMC-based AFE converter is a promising enabling technology for retrofit of high number of large PHSPs to VS operation, in pursue of highly-flexible grid-scale energy storage.

A H-MMC realized using a mix of FB and HB SMs is presented. Converter design, in terms of minimal FB SM share for desired DC link voltage operating range is derived. Additional control layers required for correct energy balancing of FB and HB SMCs are developed and verified.

Operation at unity power factor, as well as at arbitrary non-unity power factor is enabled over the entire attainable operating range. Both upper and lower branch of each phase-leg are equally loaded in terms of current and voltage requirement, leading to uniform SM devices selection and thermal design. While somewhat higher SM current rating is required compared to FB-based MMC, the lower total number of switching actions, especially at higher DC link voltage amplitudes, compensates for this downside.

Redundancy inherent to conventional MMC topology has not been compromised in H-MMC. Design and control approach have been verified through an extensive set of high-fidelity switched-model simulations.

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