Conformal passivation of Multi-Channel GaN power transistors for reduced current collapse

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Abstract—**Multi-channel power devices, in which several AlGaN/GaN layers are stacked to achieve multiple two-dimensional electron gases (2DEGs), have recently led to a significant increase in the device conductivity while maintaining high breakdown voltage, resulting in excellent DC performances. However, their dynamic performance is yet to be demonstrated, especially due to the absence of an effective passivation technique for their 3D structure. Here, we present a surface passivation technology for multi-channel devices based on a conformal deposition of a thin SiO_2 interlayer followed by a low-pressure chemical vapor deposition (LPCVD) Si_3N_4 layer around the multi-channel fins, which enables to effectively reduce the electron traps both at the AlGaN top surface and at the fin sidewalls. This approach led to a significant reduction of the dynamic on-resistance (R_{ON}) in multi-channel devices under large off-state voltages of 350 V and comparable dynamic performance with passivated single-channel reference devices. This work proves that, in addition to the excellent DC performance, the multi-channel technology can offer reduced current collapse, unveiling the potential of this platform for future power electronic applications.**

***Index Terms*— Multi-channel, AlGaN/GaN, Tri-gate, HEMT, current collapse, LPCVD Si_3N_4, passivation**

I. Introduction

GaN-on-Si lateral devices have demonstrated outstanding potential for low- and medium-power conversion applications and a tremendous improvement in their performance has been achieved in recent years [1], [2]. Yet, the performance of current GaN High-Electron-Mobility Transistors (HEMTs) is still far below what the GaN material properties could offer [3]. In particular, the high-power figure-of-merit for state-of-the-art GaN devices is still much lower with respect to the material limit, which translates into a larger specific on-resistance ($R_{ON,SP}$) for a given breakdown voltage (V_{BR}).

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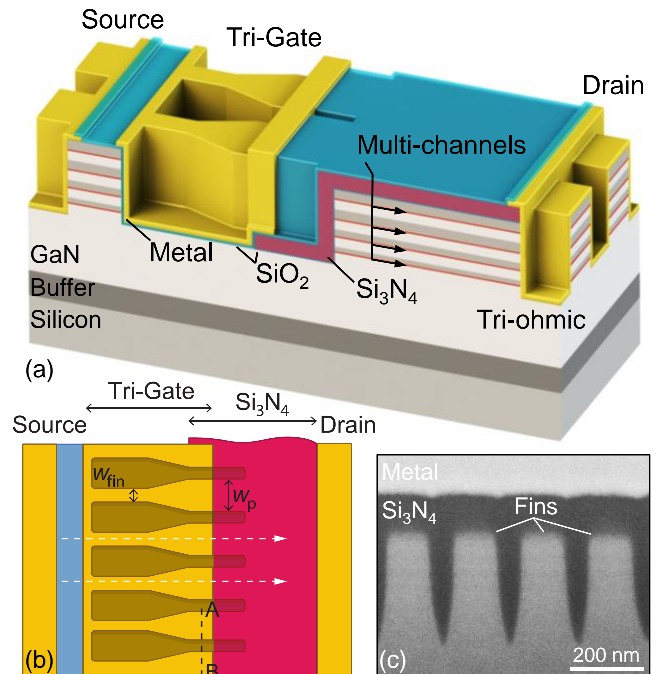

Fig. 1. (a) 3D schematics of the multi-channel tri-gate MOSHEMT with LPCVD Si_3N_4 passivation layer. (b) Top-view schematics of the Tri-gate region indicating the fin dimensions. (c) Focused Ion Beam (FIB) cross-section along the AB line in Fig. 1(b) showing the passivated multi-channel fins conformably covered by the LPCVD Si_3N_4 passivation layer.

Recently, multi-channel heterostructures, in which several AlGaN/GaN layers are stacked to achieve multiple 2DEGs [4], [5], have been proposed to increase the heterostructure conductivity. While such structures were first proposed for RF applications [6]–[10], recent works have demonstrated multi-channel devices for power applications [11]–[14], showing excellent DC performance and revealing the potential of the multi-channel platform for power conversion applications. In particular, a reduction of about 3 times in $R_{ON,SP}$ with respect to conventional single-channel devices was achieved while maintaining similar V_{BR} [13].

Despite the encouraging perspectives, previous works have focused solely on the DC characterization of multi-channel devices while their performance during switching operation is yet to be demonstrated. AlGaN/GaN power devices suffer from severe current collapse during high-voltage switching mainly due to electron trapping by surface trapping states. For conventional single-channel devices, this is typically addressed by the deposition of a passivation layer to eliminate the trapping sites at the top AlGaN surface [15]–[17].

In multichannel structures, it has been shown that tri-gate-based

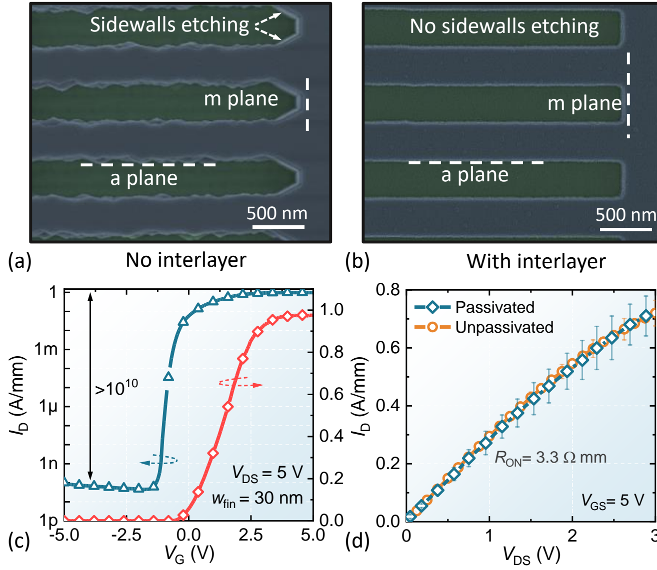

Fig. 2. (a) SEM image of multi-channel fins after the 100 nm LPCVD Si_3N_4 deposition without and with (b) a 2 nm-thick SiO_2 protective interlayer. (c) DC transfer curve of the passivated device after the Si_3N_4 etching in the Tri-gate region. W_p was set to 100 nm (d) DC output curve of multi-channel devices with and without the passivation layer showing similar R_{ON}.

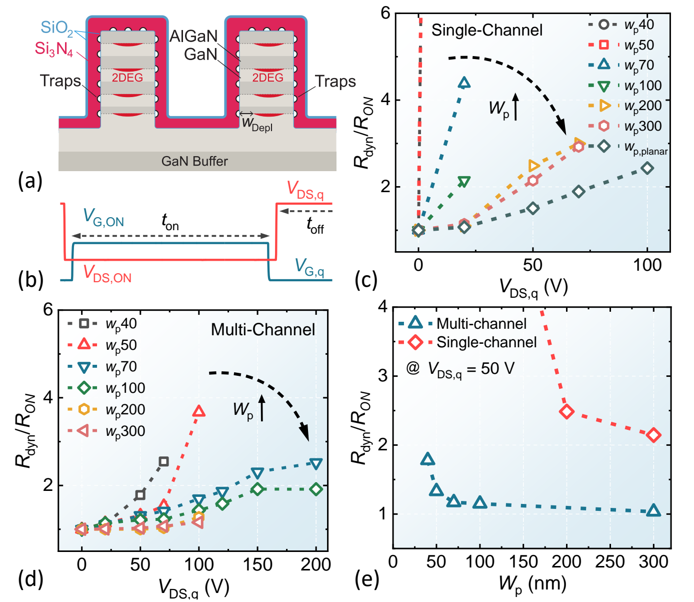

Fig. 3. (a) Cross-section illustration of the passivated multi-channel fins highlighting the presence of sidewalls traps. (b) Schematics of the $R_{ON,dyn}$ measurement. (c) Normalized R_{dyn} for the single-channel reference devices and the multi-channel devices (d) as a function of $V_{DS,q}$ for different tri-gate termination widths w_p. $w_{p,planar}$ stands for the conventional termination for single-channel devices on the planar region. w_{fin} was set to 30 nm. (e) Normalized R_{dyn} comparison as a function of w_p for single- and multi-channel devices at $V_{DS,q}$ of 50 V.

field-plate structures [13], [18] are required to manage the large off-state electric fields (Fig. 1 (a-b)). Such architecture demands effective passivation of both the top AlGaN surface and the fins sidewalls, which combined with the presence of multiple 2DEGs, poses additional challenges for the passivation of multi-channel devices. This leaves unanswered the important question of whether multi-channel devices can be effectively passivated and whether conventional surface passivation techniques can be applied to such devices.

In this work, we present a surface passivation technology for multi-channel devices based on a conformal SiO_2/Si_3N_4 layer around the multi-channel fins, which enables to effectively reduce the electron traps both at the AlGaN top surface and at the fin sidewalls. Thanks to this approach, we demonstrate that multi-channel devices can be effectively passivated, offering reduced current collapse at high-voltage operation, which represents a key advance on the development of the multi-channel technologies for power applications.

II. Device Fabrication

The multi-channel AlGaN/GaN heterostructure included 4 parallel 2DEG channels. The top 3 channels were composed of 20 nm Si-doped AlGaN barrier (with Si concentration of 10^{19} cm^{-3}), 1 nm AlN spacer, and a 20 nm GaN channel layer, while the last channel consisted of 10 nm AlGaN barrier with 5×10^{18} cm^{-3} Si doping, 1 nm AlN spacer and 20 nm GaN channel. More details on the design of such heterostructure can be found in Ref. [13]. The Hall mobility and carrier concentration of the multi-channel structure were 1930 $cm^2 \cdot V^{-1} s^{-1}$ and 3.9×10^{13} cm^{-2} respectively, resulting in a sheet resistance of 83 Ω/sq.

The fabrication started with electron-beam lithography to define the device mesa and the tri-gate structures in the gate region (Fig. 1 (a-c)). The sample was then etched by Cl_2-based inductively coupled plasma etching (ICP) to a depth of 280 nm. The design of the tri-gate region is shown in Fig. 1 (b) and is similar to the one described in Ref. [13]. An O_2 plasma/ HCl cycled treatment was performed to minimize etching damages on the fins sidewalls, followed by RCA cleaning of the sample. A 100 nm-thick LPCVD Si_3N_4 passivation layer was deposited at 770° C with a flow of 30 sccm of SiH_2Cl_2 and 180 sccm of NH_3 at a chamber pressure of 100 mT.

After the LPCVD deposition, fin structures aligned along the m-direction showed a strong crystallographic etching which caused significant damages to their sidewalls (Fig. 2 (a)) and even their complete removal for widths below 300 nm. No significant etching was instead observed for the m- and c-planes. This issue was possibly due to GaN surface desorption during the LPCVD process [19], [20], and was successfully resolved by the introduction of a 2 nm-thick SiO_2 interlayer. The SiO_2 was deposited by atomic layer deposition (ALD) before the LPCVD deposition and effectively protected the surface, resulting in no etching of the tri-gate sidewalls (Fig. 2 (b)). This was particularly important since the slanted portions of the fins would be completely deformed after the LPCVD Si_3N_4 deposition.

The LPCVD Si_3N_4 was removed in the gate and contact regions with low power (30 W) RIE etching. Since the 100 nm-thick Si_3N_4 filled the trenches between the fins (Fig. 1 (c)), about 150 nm of over-etching was performed to remove the passivation layer and enable the formation of the tri-gate structure around all of the embedded channels. Ohmic contacts were formed by a Ti/Al/Ti/Ni/Au metal stack, and annealed at 780° C for 30 s. A 25 nm-thick layer of SiO_2 was deposited by ALD at 300° C and served as the gate oxide, followed by a Pt/Au (40 nm / 100 nm) gate metal stack. The device dimensions are L_{GS} = 1 μm, L_G = 1.5 μm and L_{GD} = 10 μm.

Reference single-channel devices were co-fabricated in the same batch undergoing the same fabrication process. w_{fin} was set to 30 nm throughout the paper since, while beneficial to tune the device threshold voltage, it showed no impact on the dynamic on-resistance. All quantities reported in the

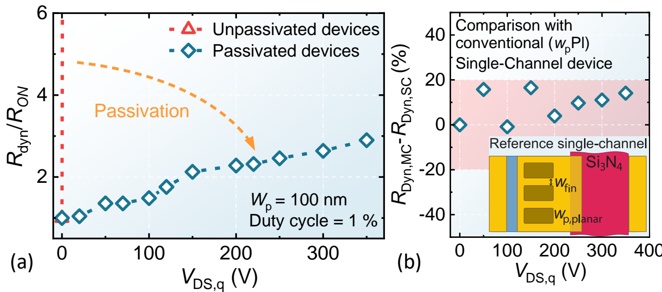

Fig. 4. (a) Normalized R_{dyn} comparison for the multi-channel devices with and without the LPCVD Si_3N_4 passivation layer. (b) Difference (normalized by the average) between normalized R_{dyn} for multi- and single-channel devices. Single-channel devices with conventional planar gate termination ($w_{p,planar}$) were considered for the comparison (bottom right inset).

manuscript have been normalized by the total device width (W = 60 µm).

III. Device Characterization

The transfer characteristic of a multi-channel tri-gate device having fin width (w_{fin}) of 30 nm is shown in Fig. 2 (c). The Si_3N_4 removal in the trenches between fins allowed to form the tri-gate structure around all of the embedded channels. This leads to excellent control over the multi-channel structure, resulting in high I_{ON}/I_{OFF} above 10^{10}. Thanks to the optimized etching recipe and the large carrier density of the multi-channel heterostructure, the Si_3N_4 over-etching in the trench region did not significantly affect the device output curve. A very low DC on-resistance (R_{ON}) of 3.3 Ω·mm was measured, which corresponds to a specific on-resistance ($R_{ON,sp}$) of 0.51 mΩ·cm^2. This value is very similar to the one from reference un-passivated devices (Fig. 2 (d)), confirming no noticeable degradation as a result of the Si_3N_4 removal.

To effectively manage the high off-state field in such conducting heterostructures, multi-channel devices require tri-gate-based field-plate solutions with the gate electrode terminating in the fin region rather than on the planar portion [13] (Fig. 1 (a-b)). This leads to the exposure of new crystal surfaces after the fin etching and damages during the dry etching process, potentially resulting in additional trapping sites on the fin sidewalls (Fig. 3 (a)). To investigate the effect of sidewalls traps on the dynamic behavior, devices with different tri-gate termination width w_p (see Fig. 1 (a)) were fabricated both on single- and multi-channel heterostructures and their dynamic on-resistance (R_{dyn}) was extracted by pulsed I-V characteristics (Fig. 3 (b)). The device was stressed in the OFF state at quiescent drain voltage ($V_{DS,q}$) for a time (t_{off}) and then suddenly turned ON for a short time t_{on} during which the output curve was measured. For this measurement t_{on} was set to 50 µs and t_{off} to 5 ms, resulting in a duty cycle of 1%. In the OFF state, the quiescent gate voltage ($V_{G,q}$) was -3 V while the quiescent drain voltage ($V_{DS,q}$) was varied. In the ON state, V_G was 5 V and V_{DS} was swept from 0 V to 3 V.

Fig. 3 (c) shows the normalized R_{dyn} as a function of $V_{DS,q}$ at different w_p for the reference single-channel devices. Despite the passivation layer, devices with small w_p show highly degraded dynamic performance, which drastically improved as w_p increases. Such behavior confirms the presence of sidewalls traps, whose effect increases significantly as the fin termination width is reduced, degrading R_{dyn}. While a similar trend of R_{dyn} with w_p is observed for multi-channel devices (Fig. 3 (d)), its increase is lower with respect to the single-channel case and becomes considerable only for small $w_p < 50$ nm. Such an effect can be explained by the reduced effectiveness of the trapped electrons, acting as a virtual gate [21], in depleting the multi-channel fins. This is due to the much higher carrier density in the multi-channel heterostructure (almost 4x larger than the single-channel case) and to the weak influence exerted by the top AlGaN surface traps on the buried channels. Similarly to the channel control by the tri-gate structure for which, at a given fin width, a larger gate voltage is required to turn-off a multi-channel device [13], trapped electrons acting as virtual gate are much less effective in depleting a multi-channel fin rather than a single-channel one. For this reason, much smaller values of w_p are required to have a good dynamic performance for multi-channel devices, which is shown in Fig. 3 (e) where R_{dyn} as a function of w_p is compared for single- and multi-channel devices at a fixed $V_{DS,q}$. While multi-channel devices present quite constant R_{dyn} for w_p above 70 nm, single-channel devices require w_p of 200-300 nm to obtain a reasonable but still much higher R_{dyn} than for multi-channels. Most importantly, effective multi-channel device passivation can be achieved in the w_p range between 70 – 150 nm (Fig. 3 (e)), which is the range required to achieve proper electric field management, as larger w_p designs result in degradation of the device blocking capability [13].

The dynamic behavior of multi-channel devices with and without the passivation layer is shown in Fig. 4 (a). While un-passivated devices present almost no current for $V_{DS,q}$ as low as 20 V, passivated devices show reduced R_{dyn} up to $V_{DS,q}$ of 350 V, demonstrating that effective passivation at high operating voltage can be achieved for multi-channel devices. Notably, their dynamic performance is comparable to the one of reference single-channel MOSHEMTs with a planar gate termination, which is the conventional and optimal architecture for single-channel devices (Fig. 4 (b)). This indicates that the presence of traps on the multi-channel fin sidewalls can be effectively suppressed and that good dynamic performance, comparable to the single-channel devices for a given passivation technique, can be achieved for multi-channel MOSHEMTs. Further improvements are possible by tuning the etching process to reduce the damages to the fin sidewalls and by optimizing the deposition of the protective interlayer and LPCVD Si_3N_4.

IV. Conclusions

In this work, we presented a surface passivation technology for multi-channel devices based on a conformal SiO_2/Si_3N_4 passivation layer around the multi-channel fins. Thanks to this approach, multi-channel MOSHEMTs with significantly reduced dynamic R_{ON} up to large charging voltages of 350 V and comparable dynamic performance with respect to single-channel reference devices were achieved. These results prove that the multi-channel devices can present excellent DC and dynamic performances, showing the potential of this technology for future power devices.

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