EPFL

Thèse n° 7710

GaN vertical power devices on silicon substrates

Présentée le 26 janvier 2021

Faculté des sciences et techniques de l'ingénieur
Laboratoire de dispositifs semiconducteurs de puissance
Programme doctoral en génie électrique

pour l'obtention du grade de Docteur ès Sciences

par

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École polytechnique fédérale de Lausanne

2021

So, verily with the hardship, there is relief,
verily with the hardship, there is relief.
— Qur'an 94:5-6

To my parents…

Acknowledgements

My stay at Ecole Polytechnique Federale de Lausanne towards attaining a Ph.D. degree has been challenging yet so endearing and satisfying at the same time. I would not have wanted it any other way. I am extremely grateful to my thesis supervisor Prof. Elison Matioli for selecting me for this prestigious Ph.D. program in his lab and having confidence in me. You have made me not just a better researcher but also gave me valuable life lessons that continue to help me. I wish to also express my gratitude to my Ph.D. jury president Prof. Andras Kis from EPFL, external experts Dr. Niels Posthuma from IMEC and Dr. Lars Knoll from Hitachi ABB Power Grids, and internal expert Prof. Nicolas Grandjean from EPFL, for providing a fair and critical assessment of my Ph.D. work.

I wish to thank my parents, Dr. M Abdul Khadar and Dr. P A Najeema Beevi for their continuous love, dedication,and for instilling in me a scientific temper. I am what I am today because of you both. A big thanks to my loving brother - Rameez, the catalyst behind my academic successes, my sister-in-law Shabana and my nephew Farid. Thank you for being there for me during my most stressful times.

I am very thankful to the process engineers at CMi and IPHYS cleanrooms at EPFL for providing me the correct guidance and for timely help that has had a profound impact on my experimental work. In particular, I wish to express my gratitude to Remy Juttin, Joffrey Pernollet, Patrick Madliger, Zdenek Benes, Nicolas Leiser and Damien Trolliet.

Muriel- Thank you for being so kind and being such a wonderful person and helping me with all the administrative stuffs. My fellow colleagues at POWERlab were the biggest source of help, motivation and inspiration. I am lucky I had such amazing team members who were always helpful and friendly. A big shout out to present and previous POWERlabians - Reza, Chao, Jun, Alessandro, Giovanni, Armin, Minghua, Taifang, Luca, Remco, Katya, Mohammad, Nirmana, Georgios, Martel, Mehdi and Pirouz. I will miss you all.

VJ, you have been my closest friend after coming to Switzerland. Thank you so much for being such a honest person and for all the support and the delicious food that you have cooked for me. Hafiz, my roommate of 4 years, thank you for being an amazing friend and a brother. I wish to thank all my friends from Switzerland - Andrei, Arif, Asalam, Akshay, Anwar for all the good

times we had that definitely helped me relieve of the stress from the Ph.D. life. I also wish to use this opportunity to thank my friends back at home.

Above all, I thank God Almighty for all the countless blessings He has showered upon me.

Lausanne, 09 December 2020 Riyaz Abdul Khadar

Abstract

Gallium Nitride (GaN) is a wonder material which has widely transformed the world by enabling energy-efficient white light-emitting diodes. Over the past decade, GaN has also emerged as one of the most promising materials for developing power devices which can operate at significantly higher power densities, higher temperatures, and higher frequencies, thanks to inherently superior material properties like higher bandgap, 10x higher critical electric field, and 3x higher electron saturation velocity, compared to silicon.

Lateral GaN high electron mobility transistors (HEMTs) based on the AlGaN/GaN heterostructures capable of switching at high frequencies over 10 MHz have been already commercialized and are the device of choice for implementing modern-day adapters and for wireless charging solutions. However, for high-voltage and high-current applications, it is envisaged that vertical GaN power devices will play a crucial role given that these devices don't scale in size for increasing the BV unlike HEMTs, and are not affected by surface trap related reliability issues. The main bottleneck towards the commercialization of vertical GaN devices on bulk GaN substrates is the high cost and small size availability of these substrates. Similar to lateral GaN HEMTs, GaN epitaxial layers grown on silicon substrate could also become a game-changer for vertical GaN power devices considering that silicon substrates are significantly cheaper and are available in large sizes up to 12-inch diameters which can greatly accelerate viable commercialization. However, there are several roadblocks arising from the growth as well as fabrication perspective that has limited the demonstration of high-performance power devices on GaN-on-Si.

In this thesis, we discuss the key hindrances and our solutions for improving the feasibility of GaN-on-Si vertical power devices. All the necessary fabrication steps were first optimized from scratch to develop state-of-the-art power devices. As a first demonstration, we could develop a GaN p-i-n diode with an ultra-low $R_{on,sp}$ of 0.33 mΩ cm^2 and record BV of 820 V with a voltage blocking GaN layer of just 4 μm.

A quasi-vertical MOSFET was then demonstrated for the first time on GaN-on-Si platform with excellent ON- and OFF-state performances. We then probed the limits of current crowding, a main deterrent to the current up-scaling of quasi-vertical devices by exploring large area quasi-vertical MOSFETs. A novel and robust method for achieving a fully-vertical design for GaN-on-Si devices was developed which led to an exemplary improvement in the ON-state performance of

quasi-vertical MOSFETs.

Device integration has been identified by many leading power semiconductor companies as the way forward due to significant advantages to be had, as a result of lower parasitics and simplified packaging. Taking a cue from these developments, we demonstrated vertical GaN power MOSFETs with integrated freewheeling diodes and reverse blocking capability as described in Chapter 4.

In the last chapter, we introduce p-type NiO as a possible substitute for p-GaN for realizing high-performance p-i-n diodes and as junction termination extensions (JTEs) for Schottky barrier diodes. Our initial results point to a strong future for p-NiO to be used for realizing a myriad of reliable GaN power devices.

Key words: GaN-on-Si, p-i-n diode, SBD, MOSFET, quasi-vertical, fully-vertical, integration, p-NiO, TCAD.

Résumé

Le nitrure de gallium (GaN) est un matériau prodigieux qui a largement transformé le monde en permettant diodes électroluminescentes blanches à haute efficacité énergétique. Au cours de la dernière décennie, le GaN est également apparu comme un des matériaux les plus prometteurs pour développer des dispositifs de puissance qui peuvent fonctionner à des densités de puissance, à des températures et à des fréquences plus élevées, grâce à propriétés du matériau comme une bande interdite plus élevée, un champ électrique critique 10x plus élevé et une vitesse de saturation des électrons 3x plus élevé, par rapport au silicium.

Transistors latéraux à haute mobilité électronique (HEMT) en GaN basés sur hétérostructures AlGaN / GaN capables de commuter à des fréquences élevées supérieures à 10 MHz ont déjà été commercialisés et sont l'appareil de choix pour la realisation d'adaptateurs modernes et pour les solutions de charge sans fil. Cependant, pour les applications à haute tension et à courant élevé, il est envisagé que dispositifs verticaux en GaN joueront un rôle crucial étant donné que la taille de ces appareils n'augmente pas les tensions du breakdown contrairement aux HEMTs, et ne sont pas affectés par les problèmes de fiabilité liés aux pièges de surface. Le principal goulot d'étranglement vers la commercialisation de dispositifs verticaux en GaN sur des substrats natifs en GaN est le coût et la disponibilité en petite taille de ces substrats. Similaire aux HEMTs latéraux en GaN, les couches épitaxiales de GaN deposé sur un substrat en silicium pourraient également changer la donne pour les dispositifs verticaux en GaN étant donné que les substrats de silicium sont nettement moins chers et sont disponibles dans de grandes tailles allant jusqu'à 12 pouces de diamètre, ce qui peut grandement accélérer une commercialisation viable. Pourtant il y a plusieurs obstacles découlant de la croissance ainsi que de la fabrication qui ont limité la démonstration de dispositifs de puissance à hautes performances sur GaN-on-Si.

Dans cette thèse, nous discutons des principaux obstacles et de nos solutions pour améliorer la faisabilité des dispositifs de puissance verticaux en GaN-on-Si. Toutes les étapes de fabrication nécessaires ont d'abord été optimisées à partir de zéro pour développer des dispositifs de puissance à la pointe de la technologie. Comme première démonstration, nous avons développé une diode p-i-n en GaN avec une $R_{on,sp}$ de 0.33 mΩ cm^2 et une tension de breakdown record de 820 V, avec un couche de GaN bloquant la tension de seulement 4 μm.

Un MOSFET quasi-verticaux a ensuite été démontré pour la première fois sur une plateforme

GaN-on-Si avec excellentes performances à l'état ON et OFF. Nous avons ensuite sondé les limites d'encombrement de courant, un frein majeur à la mise à l'échelle actuelle des dispositifs quasi-verticaux en explorant MOSFETs quasi-verticaux à grande surface. Une méthode nouvelle et robuste pour réaliser une conception entièrement-verticale pour des dispositifs GaN-on-Si ont été développés, ce qui a conduit à une amélioration exemplaire des performances à l'état ON de MOSFETs quasi-vertical.

L'intégration de dispositifs a été identifiée par de nombreuses entreprises de premier plan dans le domain des semi-conducteurs de puissance comme la voie à suivre en raison des avantages importants à avoir, du fait de la réduction des parasites et packaging simplifié. En nous inspirant de ces développements, nous avons démontré MOSFETs verticaux en GaN avec diodes de roue libre intégrées et capacité de blocage inverse comme décrit dans le Chapitre 4.

Dans le dernier chapitre, nous introduisons NiO de type p comme substitut possible du GaN de type p pour réaliser diodes p-i-n à hautes performances et extensions de terminaison de jonction (JTE) pour diodes Schottky. Nos premiers résultats indiquent un avenir solide pour le p-NiO à utiliser pour réaliser une myriade de dispositifs de puissance en GaN fiables.

Mots clefs : GaN-on-Si, diode p-i-n, SBD, MOSFET, quasi-verticaux, entièrement-verticale, intégration, p-NiO, TCAD.

Contents

List of Figures

List of Tables

1 Introduction

Power conversion is a necessity in almost all electrical application that we witness in the modern world ranging from charging our cell phones to satellite power systems. While the complexity and the stages of the power conversion system can vary depending on the application, the basic building blocks are the power electronic switches. The first power electronic devices used for converting power were the mercury-arc valves [1]. In modern systems, the conversion is performed with semiconductor switching devices like power diodes, thyristors, transistors and IGBTs [2–5]. These have the advantage over their bulky counterparts that they are much more reliable, compact, can switch at higher frequencies and offer much better voltage and current handling capacity [6, 7]. Also, since ~ 40 % of the world's current energy requirement is met from electrical sources, semiconductor power devices play a key role in the generation-storage-distribution cycle [8]. To cite an example, a modern day car incorporates several power electronic modules as shown in Fig. 1.1 [9], to realize a slew of essential functionalities like engine and battery management, braking, infotainment systems, power steering, power windows, etc. which would not be possible without the use of efficient and compact power semiconductor switches tailored for each application.

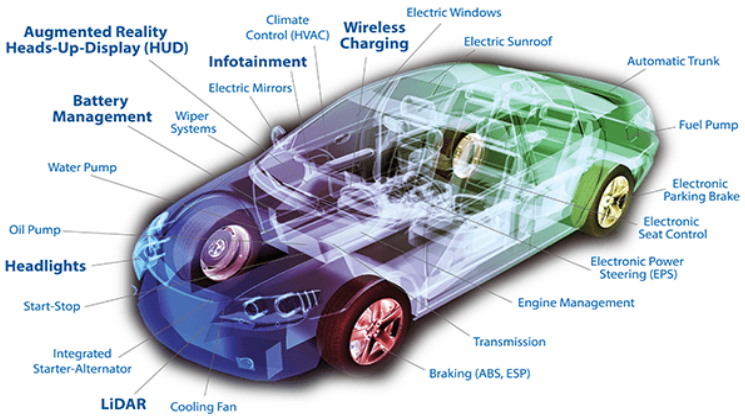


Figure 1.1 – Applications of power electronics in automotive electronics

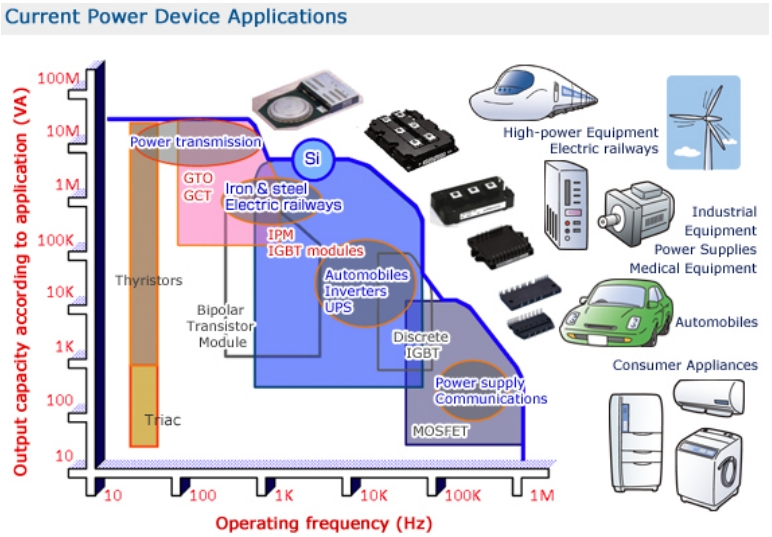


Figure 1.2 – Application space of Si power devices

1.1 Current state of Si, SiC and GaN power devices

Since the commercialization of the early power semiconductor devices like the thyristor, bipolar transistors and MOSFETs in the early 1960s, these devices have been used in wide spread applications including power grid modules, aircrafts, industrial machinery, consumer electronics to name a few, and have accelerated the development of various new power electronic devices which have significantly impacted the modernization of the world as we know it. Majority of these power devices are still based on silicon as a direct consequence of the easy availability, low cost and high quality of bulk silicon wafers which are available till 12-inch diameters [10]. Fig. 1.2 presents the application space of the silicon power devices mainly the insulated gate bipolar transtistors (IGBTs) and intelligent power modules (IPMs), as a function of the operating frequency and power output required [11]. Currently, the silicon power market is valued at a whopping $ 38.2bn [12].

The performance of power devices like diodes and transistors contribute significantly to the overall efficiency of a power electronic system. As such, these devices should offer low ON-state resistance and low OFF-state leakage, while also presenting the possibility of high frequency switching. With technological developments accelerating at an exponential pace, the material limitations inherent to silicon like low critical electric field (E_c), low thermal conductivity (k), low frequency device operation, etc., became more glaring, and led to the investigation of wide band gap (WBG) semiconductors like Silicon Carbide (SiC) and Gallium Nitride (GaN) for future power electronic devices. SiC has excellent properties as compared to Si with 6-8 × higher E_c, 3.5 × higher k, 2 × higher saturation velocity (v_s), etc. These properties allow SiC devices to have 1/100 lower ON-resistance and better heat extraction as compared to silicon based devices with the same voltage rating [13]. The first commercial SiC power MOSFET was launched by Cree in 2011 [14]. Since then, a number of companies including Infineon, ON semiconductors, ROHM to name a few have established their presence in the SiC power market by introducing

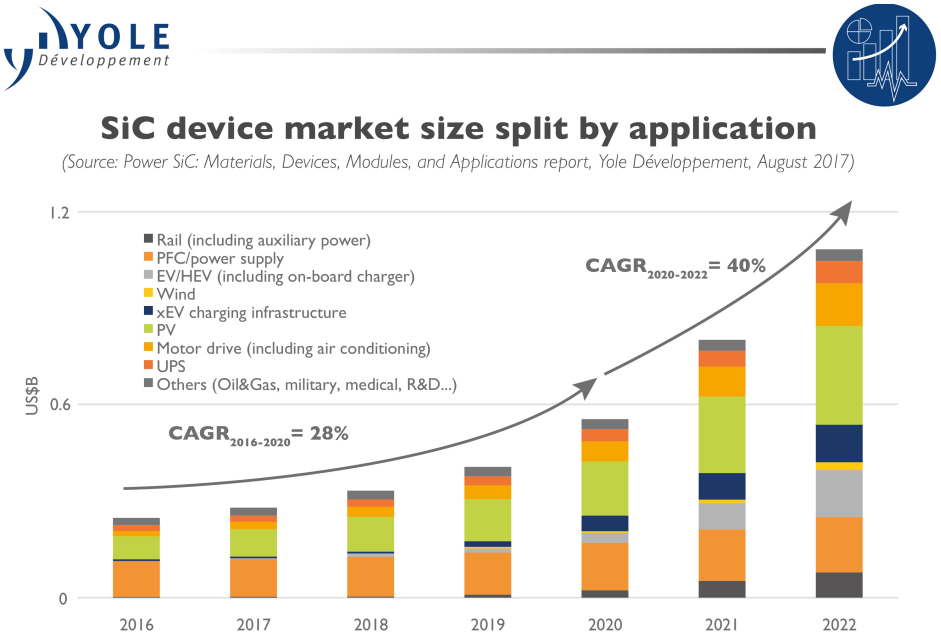


Figure 1.3 – SiC device market projection

an array of SiC diodes and transistors [15–17]. These SiC devices are ideal for applications like solar string inverters, low loss and efficient servo drives, traction inverters of electric vehicles (EVs), on board charger (OBC) systems for EVs, among various others [16]. Fig. 1.3 shows the projected SiC growth by application area and predicts the SiC market to grow by 40% compound annual growth rate (CAGR) from 2020 to more than $ 1bn in 2022. The large scale availability of high quality 6-inch SiC substrates having a cost parity with the more mature 4-inch substrates will be crucial in achieving such an ambitious target [13]. Commercially, up to 100 A, 1200 V, and 200A, 650 V single chip junction barrier Schottky (JBS) diodes are now available, with ratings similar to silicon soft-recovery diode levels. In the SiC transistor space, the main main device structures are trench MOSFETs from ROHM and Infineon, trench JFET from USCi and planar MOSFETs from Wolfspeed, Panasonic, Mitsubhishi, ST and GE. Cascode technology based on trench MOSFETs from UnitedSiC provide more than 10 × lower $R_{on,sp}$ (specific ON-resistance, also know as $R_{ds} \times A$ where R_{ds} is the ON-state resistance and A is the area of the active region of the device), lower capacitances and a cost effective alternative to commercial Si superjunction devices [18].

GaN is another wide band gap material which has been attracting a lot of interest of late. The interest in developing GaN based power devices stems from the fact that it has better material properties like higher bandgap (E_g), saturation velocity (V_{sat}), electron mobility (μ) and critical electric field than SiC and Si as shown in Fig. 1.4a [19]. Thus GaN has much better Figure of Merit (FOM) like the Baliga's Figure of Merit (BFOM) [19], Johnson's Figure of Merit (JFOM) [20] and Baliga's High Frequency Figure of Merit (BHFFOM) [21] than SiC and Si as shown in Fig. 1.4b. The foray of GaN into power switches was made possible with the invention of the AlGaN/GaN based high electron mobility transistor (HEMT) [22]. These group-III nitrides with

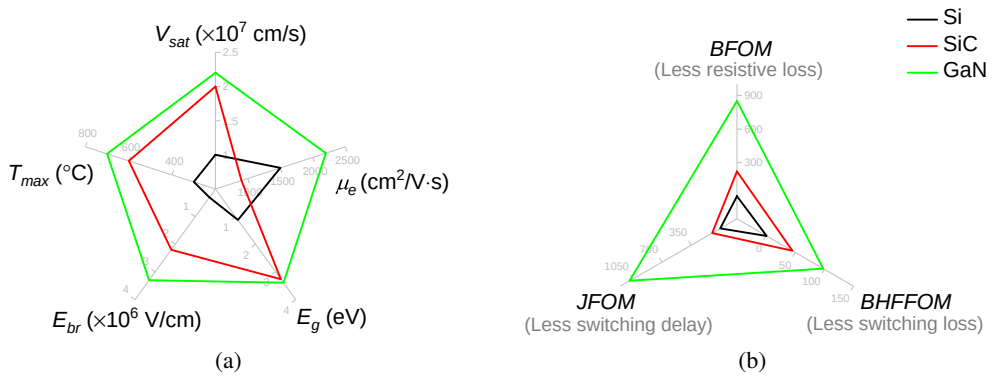


Figure 1.4 – Comparison of Si, SiC and GaN based on (a) normalized fundamental properties [19] and (b) normalized figure of merits (FOM) [20, 21].

wurtzite crystal structure have large spontaneous and piezoelectric polarizations [23]. When an AlGaN layer is grown on top of a GaN layer, there is a discontinuity in these polarizations which leads to the formation of a 2 dimensional electron gas (2DEG) with high mobility (2000cm^2/Vs) owing to low scattering. This combination of high electron mobility and higher band gap provides GaN with significant reduction on device on-resistance (R_{DS} (on) or R_{ON}) for a given reverse hold-off voltage capability than both SiC and Si devices. Increasingly, these lateral HEMTs are becoming the device of choice for low power electronics (1-15 KW) [24]. Devices from our lab as well as other research institutions have demonstrated excellent performance as compared to Si and SiC based switches [25–34].

A large number of companies have already started mass producing AlGaN/GaN HEMT based discrete devices as well as power modules, the main players being, Power Integrations, EPC, GaN systems, Transphorm, Navitas and Infineon technologies. The biggest demand for power GaN market is from fast charging applications for cellphones, with a lot of OEMs including OPPO, Samsung, REALme having adopted integrated power GaN devices for their fast chargers [12]. This could result in a compound annual growth rate (CAGR) of 55% between 2017 and 2023 indicated by the base case scenario of Fig. 1.5. However, several market research firms, including Yole, report about a killer application - wireless charging for mobile phones - which could cause the GaN power device market to explode [35]. As per their reports, Apple is believed to be interested in adopting GaN based technology for their wireless charging solution. This could result in a more bullish CAGR of 93 % from 2017 to 2023 (Fig. 1.5).

The first commercial GaN devices were released by a start-up named EPC in 2011. Ever since, the list of pure-GaN start-up players is only getting longer with the likes of Transphorm, Navitas, GaN systems, etc., actively promoting GaN technology. Most of these start-ups follow the foundry model with TSMC, Epsil or X-Fab as their partner. The foundry model affords these fabless start-ups the possibility of ramping up quickly if the market suddenly takes off [12]. Recently, industry giants like Infineon, STMicroelectronics, ON semiconductors, etc., have entered the power GaN market. The incorporation of GaN devices in power electronic modules

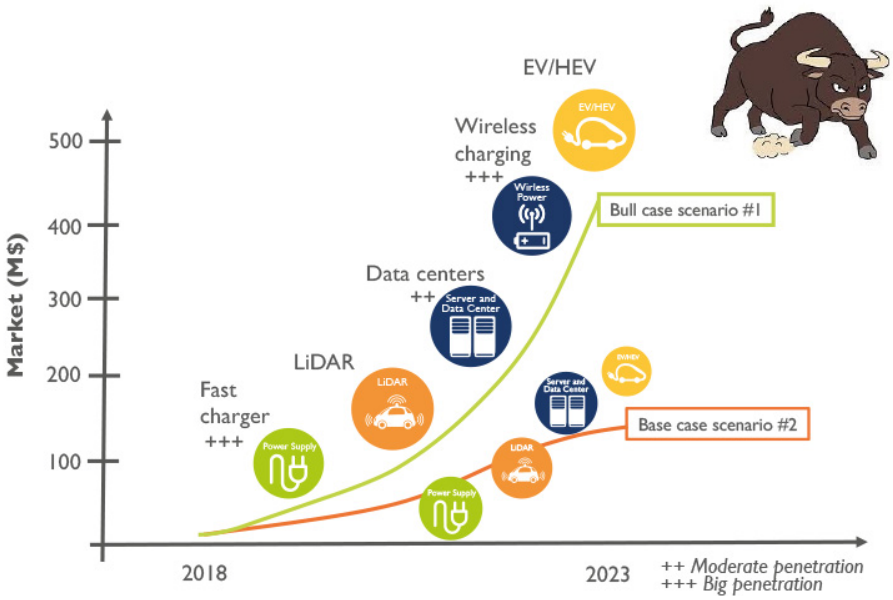


Figure 1.5 – Projected evolution of power GaN market with 2 scenarios [35].

like photovoltaic inverters, UPS, DC EV chargers and battery chargers used for energy storage, etc., could improve the overall efficiency and reduce the size of the passive components as the system can work at higher frequencies [12, 36]. However, the main hurdle towards this adoption is the high cost involved. The overall production and packaging cost of GaN based devices is still significantly higher than very popular Si MOSFET available with high quality and reliability. Currently, only EPC claims to have GaN based discrete devices at the same price level as Si MOSFET. As per the Yole report, many companies like Texas instruments, Exagan, Navitas have started offering integrated systems and system-in-package solutions to be cost competitive [35] (Fig. 1.6).

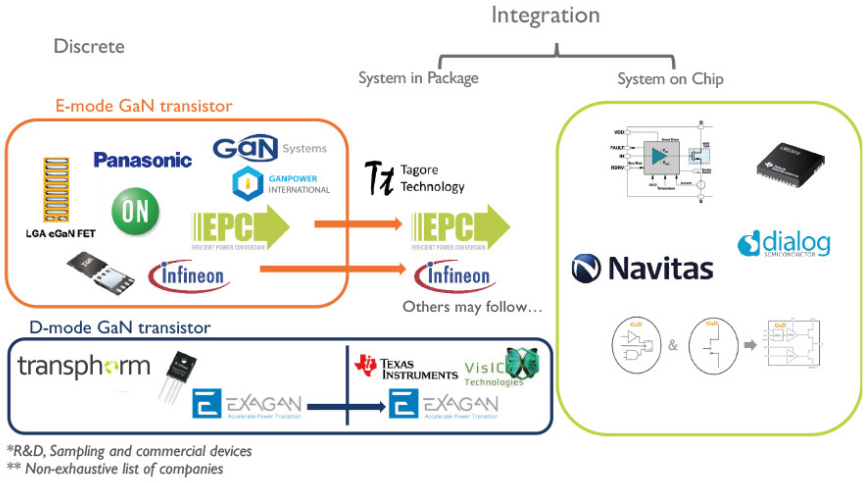


Figure 1.6 – Power GaN industry - integration roadmap [35].

It is important to note that all the current commercial GaN discrete devices are based on the lateral AlGaN/GaN HEMT since the technology is more mature since its discovery 1993 [22]. However these devices are not without their drawbacks. To increase the breakdown voltage in a lateral device, we have to increase the gate to drain distance, thus increasing the ON resistance and the chip size area. Current flows near the surface in a lateral HEMT and thus, electrons are more sensitive to surface states causing current collapse phenomenon [37–39] and increase in dynamic on resistance. Also, it's better to have the high electric field region far from the surface as there are a lot of acceptor- type traps which degrades the forward and reverse bias performance [40, 41]. Conventional Si and SiC based power switches were always based on the vertical architecture where current flows vertically between different layers [42]. The breakdown voltage can be increased by increasing the size of drift layer in the vertical direction, thus the chip size area doesn't change. This also allows for higher current density than lateral devices and the region of peak electric field is always away from the surface. A vertical structure is thus more suitable for high-power applications because it has better scalability to higher current and voltage, and it is less sensitive to passivation and surface states. A brief survey of lateral and vertical GaN power devices is presented next.

1.2 Lateral GaN power devices

Currently, the dominant platform for developing GaN based power electronic devices is based on the lateral AlGaN/GaN HEMT technology. When a thin layer of $Al_xGa_{1-x}N$ layer is grown on a Ga-polarity or Ga-face GaN, the tensile strain created by this growth results in a piezoelectric polarization P_{pz} which adds to the net spontaneous polarization P_{sp} in a manner given by [43].

$$P(x) = P_{pz} + P_{sp} \tag{1.1}$$

$$= -[(3.2x - 1.9x^2) \times 10^{-6} - 5.2 \times 10^{-6}x]Ccm^{-2} \tag{1.2}$$

This results in a net positive charge in the AlGaN side of the AlGaN/GaN hetero-interface which creates a 2 dimensional electron gas (2DEG) at the GaN side of the interface. The resulting band diagram is as shown in Fig. 1.7 (b). This 2DEG presents excellent conductivity as a result of the high concentration and high mobility of the electrons which results in low ON-state resistance in these HEMTs (Fig. 1.7(a)).

The HEMT structure shown in Fig. 1.7 (a) results in a normally-ON device which is not ideal for the safe operation of power electronic systems. Hence its necessary to have a normally-OFF mode of operation for these device which could be achieved by:

1. A cascode configuration which combines a low voltage Si-MOSFET and a high voltage GaN HEMT.

2. By having a thin p-GaN layer on the AlGaN barrier in the gate region which depletes the 2DEG.

3. By recessing the AlGaN barrier in the gate region.

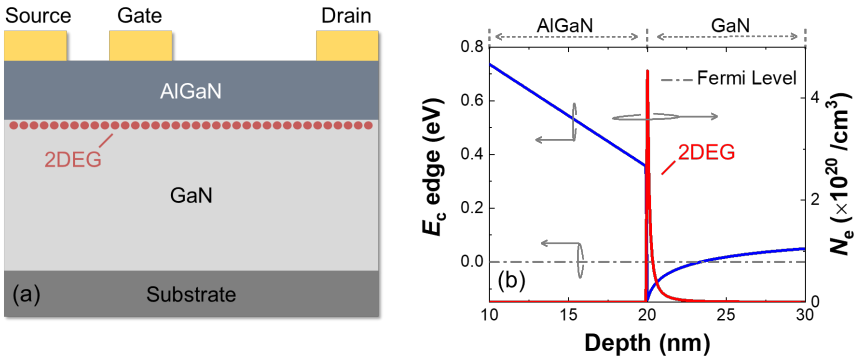
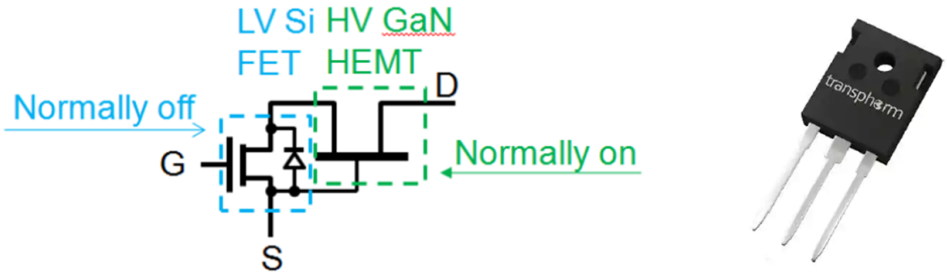


Figure 1.7 – (a) cross-sectional schematic of an AlGaN/GaN HEMT [44]. (b) simulated band diagram of the AlGaN/GaN heterostructure clearly showing the 2DEG at the interface [44].

In a cascode configuration (Fig. 1.8a, 1.8b), a high voltage depletion mode HEMT is matched with a low voltage enhancement mode Si-MOSFET to obtain a normally-OFF operation. The advantage of this configuration is the possiblity to have a large threshold voltage (V_{th}) as the gate control is through the gate of the Si-MOSFET and not directly to the gate of the GaN-HEMT. However, since slew rate is very important for the safe operation and reduction of ringing noises in power systems, a direct control of the GaN HEMT gate is essential [45]. Hence true normally-OFF HEMTs which can be driven by on-chip or off-chip gate driver circuits are highly desired. One such method to achieve a normally-OFF operation is by introducing a p-GaN layer between



(a) (b)

Figure 1.8 – (a) Schematic of a cascode configuration [46]. (b) The GaN + Si cascode device in T0-220 package [46].

the gate electrode and the AlGaN barrier layer as shown in Fig. 1.9a [47]. The negative ions in the p-GaN layer at the gate region effectively screens the 2DEG below the AlGaN layer and lifts the conduction band above the Fermi level, thus creating a normally-OFF behavior. This device is also known as a gate injection transistor (GIT) if the gate forms an ohmic contact to the p-GaN. These devices still suffer from the dynamic R_{on} increase and current-collapse phenomenon which plague the ON-state performance of AlGaN/GaN HEMTs. To solve these issues, a hybrid-drain-embedded GIT (HD-GIT) was proposed which employs an additional p-GaN layer grown near to the drain terminal and electrically connected to it as shown in Fig.

1.9b [48]. This p-GaN layer injects holes into the epilayer and compensates for the electron trapping during the OFF-state. Thus the gate-drain access region is not negatively charged during OFF-state and this results in drastic suppression of the current collapse and therefore negligible increase in the dynamic R_{on} as shown in Fig. 1.9c. Another method is to etch away the AlGaN barrier below the gate region to remove the 2DEG . A thin dielectric is then deposited to reduce the leakage to the gate terminal and thus form a MISFET [45].

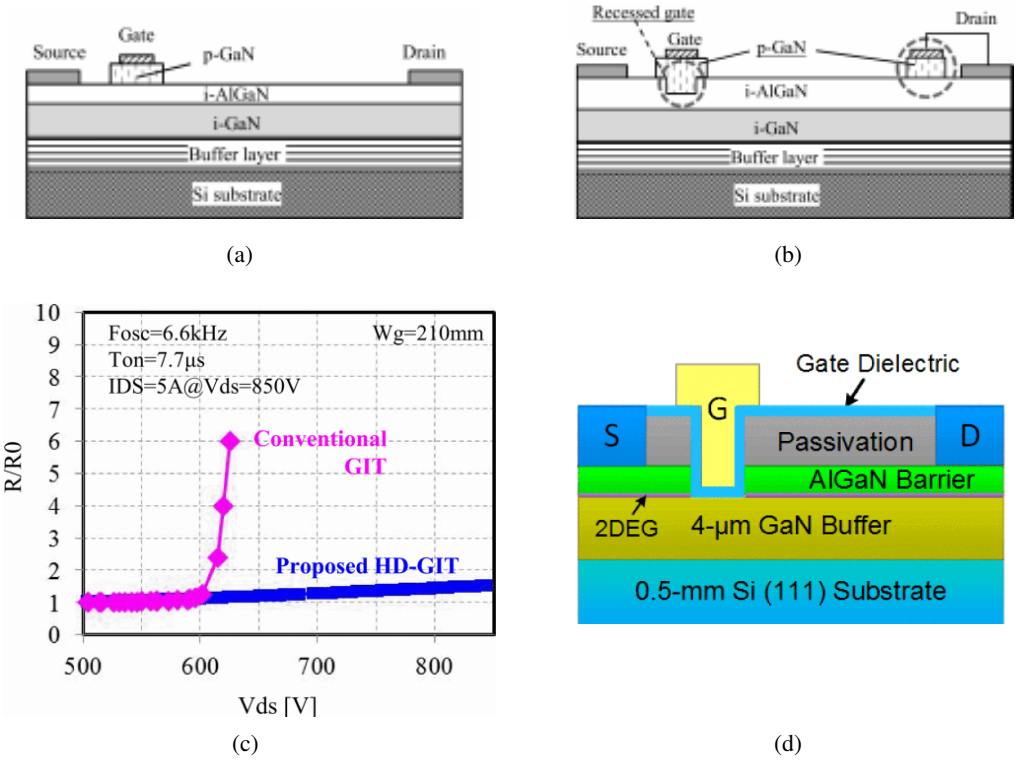


Figure 1.9 – (a) Schematic of a conventional p-GaN gate FET (GIT) [48], and (b) a hybrid-drain-embedded GIT (HD-GIT) [48]. (c) Comparison of dynamic R_{on} of the HD-GIT and the GIT, normalized by the DC values [48]. (d) Schematic cross section of a MISFET formed by etching away the AlGaN barrier followed by LPCVD SIN_x [45].

In order to improve the ON- and the OFF-state performance of the AlGaN/GaN HEMTs and SBDs, several methods have been reported including field plates at the gate terminal for improving the BV, tri-gate technologies for improving leakage current and BV and multi channel AlGaN/GaN HEMTs for reducing the R_{on}.Tri-gate technologies have proved to be very successful in reducing the leakage current under OFF-state by pinching-off the channel by a tri-gate MOS action [49, 50] (Fig. 1.10a). A field plate redistributes the electric field to crate a more uniform distribution, thus reducing the chance of a premature breakdown [51]. Fig. 1.10b shows a conventional field plate employed for AlGaN/GaN HEMTs [52] and Fig. 1.10c presents a a tri-gate structure incorporating a slanted field plate which improves both the leakage current and BV dramatically [26]. For the purpose of improving the R_{on}, the most effective method is to increase the number

of conduction channels as in [53] (Fig. 1.10d). Here a number of AlGaN/GaN heterostructure pairs are stacked on top of each to create parallel conducting channels which increase the current and reduce the R_{on}.

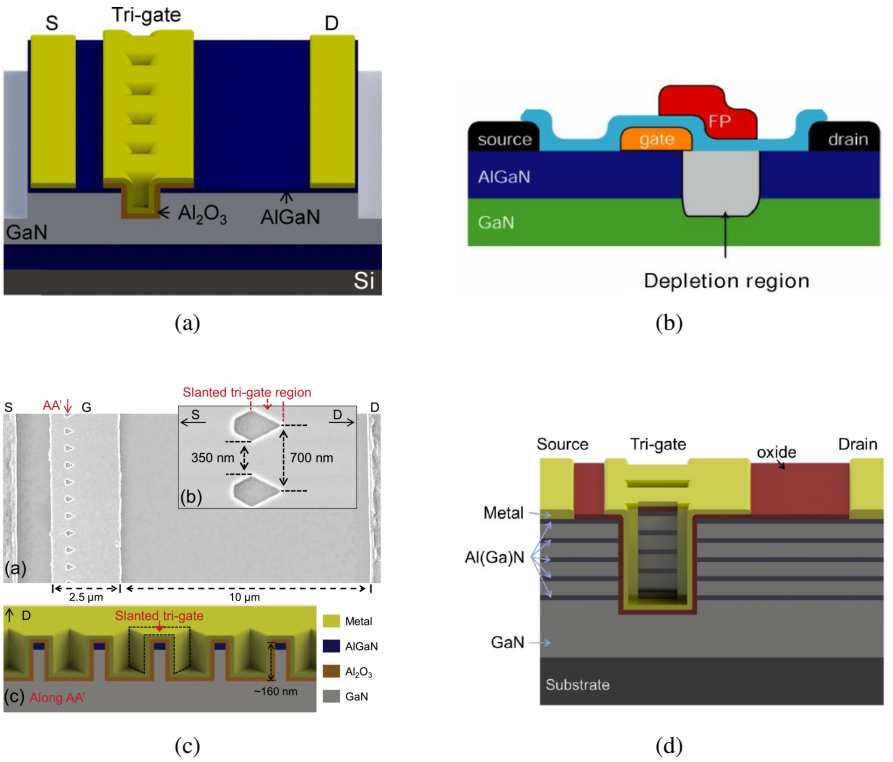


Figure 1.10 – (a) Schematic of a tri-gate HEMT [44]. (b) Schematic depicting the effect of a gate field plate on a HEMT [52]. (c) Scanning electron micrograph of HEMT employing a tri-gate with an integrated slanted field plate and a schematic of it [26].(d) Schematic of a multi-channel HEMT clearly showing all the conduction channels [53].

1.3 Vertical GaN power devices

Vertical power devices on GaN are different from their lateral counterparts in that the current flows vertically ie, parallel to the growth direction of the epitaxial GaN layers. Majority of the conventional power devices based on Si and SiC have a vertical topology. For GaN, the vertical topology offers several distinct advantages over the lateral power HEMTs. In lateral HEMTs, in order to improve the breakdown voltage, the gate to drain distance has to be increased which results in an increase in the size of the device and thus, a lower effective current density (Fig. 1.11). In a vertical power device, the thickness of the voltage blocking layer is increased and thus the area remains the same for the same current rating (Fig. 1.11). Also since the size of the lateral HEMTs have to be increased, it results in increased parasitic capacitances which degrade the switching speed and thus, the efficiency. Current flows near the surface in a lateral HEMT and thus, electrons are more sensitive to surface states causing current collapse phenomenon and increase in dynamic on resistance [40, 41, 54]. Also, it is better to have the high electric field

region far from the surface as there are a lot of acceptor-type traps which degrades the forward and reverse bias performance [52, 55]. The peak electric field in a vertical device appears inside a vertical device and since current conduction is vertically through the bulk of the device, it is not affected by surface states like in a lateral device. Another major reason is that lateral the HEMTs have a threshold voltage (V_{th}) in the region of 1-2 V [56, 57] which is not adequate to prevent false operation by noise [58], while most vertical MOSFETs can easily achieve a $V_{th} > 5$ V [58]. The most significant advantage of a vertical GaN device is the avalanche capability. Lateral HEMTs do not have p-n junctions in their structure and hence suffer catastrophic breakdown under voltage stress above the designed BV. This translates to a large margin which needs to implemented over the rated BV to ensure that the device never suffers a destructive breakdown.

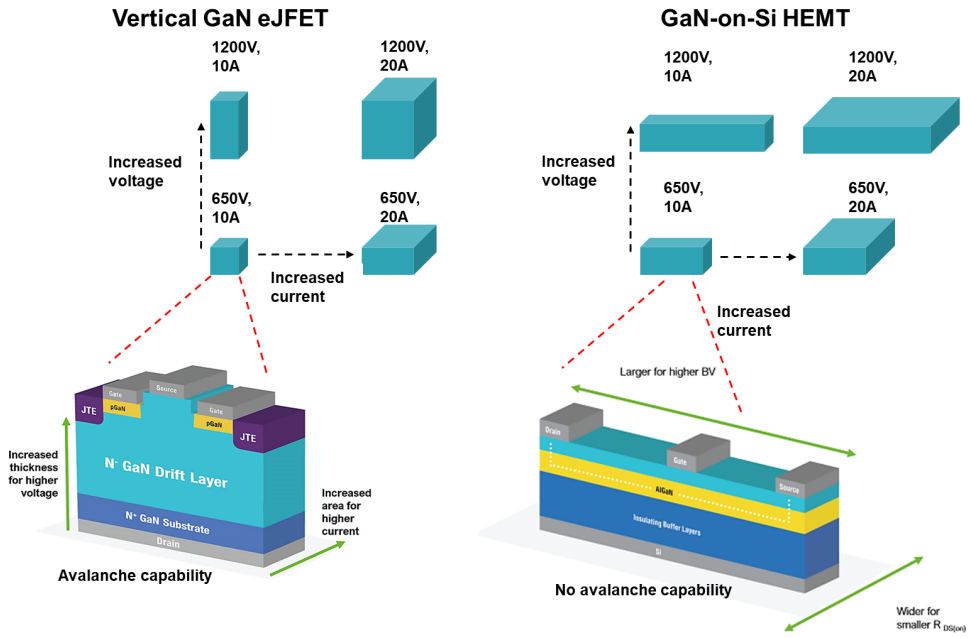


Figure 1.11 – Vertical GaN vs lateral AlGaN/GaN HEMT design consideration for various ratings [59].

Vertical GaN power devices could be fabricated on GaN homoepitaxial layers grown on bulk GaN subtrates or GaN heteroepitaxial layers grown on Si and sapphire substrates. Bulk GaN substrates inherently have the lowest defect density of around 10^3-10^5 /cm^2 and have zero lattice and coefficient of thermal expansion (CTE) mismatch. Thick layers of GaN (> 40 μm) can be easily grown with BV > 4000 V, which is far more superior as compared to AlGaN/GaN HEMTs. The next subsection details a brief summary of the state-of-the art GaN vertical devices which served as a benchmark for the projects detailed in this thesis

1.3.1 Review of GaN vertical power devices

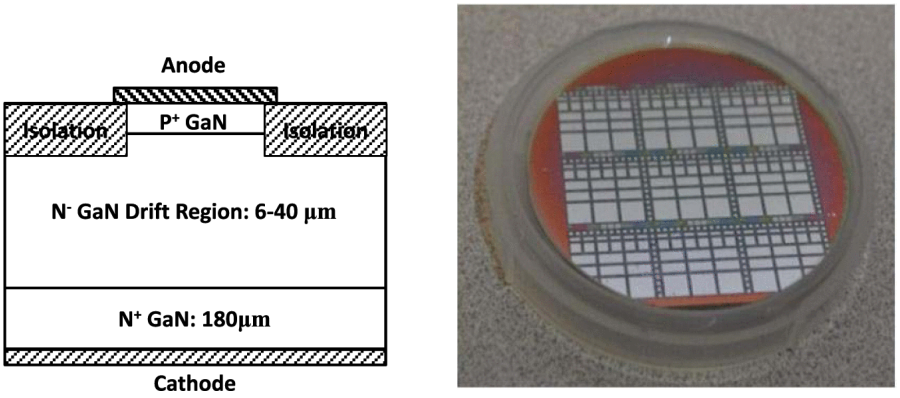
The vertical power devices on GaN could be either p-i-n diodes, Schottky barrier diodes (SBDs) or MOSFETs. Even though SBDs and power MOSFETs rule the roost in terms of number of applications, p-i-n diodes give useful information regarding critical electric field, impact

ionization coefficients, conductivity modulation, defect levels (form the analysis of the emission spectrum), etc. Also p-n junctions are integral components of trench MOSFETs, junction barrier Schottky (JBS) diodes, merged p-i-n Schottky diodes, and junction termination extension structures. The following section presents the developmental trends of vertical GaN power devices.

P-I-N diodes

The first report on GaN p-i-n diodes on bulk GaN substrates date back to 2005 [60]. However, high voltage p-i-n diodes with $BV > 1$ kV were reported only after 2010 [61]. Rapid developments in the growth and fabrication of p-i-n diodes ensued, especially by startups like Avogy Inc. and researchers from Cornell university, Hosei University, Toyoda Gosei, etc.

Avogy Inc. first reported on avalanche capability in p-i-n diodes with BV of 2.6 kV [62] and 3.7 kV [63]. They employed an implantation based proprietary edge termination for better distribution of electric field peaks to achieve avalanche capability as shown in Fig. 1.12a. They were also able to reduce the reverse leakage current by over 4 orders of magnitude by introducing a slight miscut angle of ~ tenth of a degree which increased the velocity of the step-flow growth overwhelming the spiral growth around dislocations, thus resulting in a much smoother surface [58, 64]. In 2015 [65], they were the first group to evaluate the reliability of vertical power devices on bulk GaN like , high temperature reverse bias (HTRB), temperature cycling (TC), temperature humidity bias (THB), and inductive avalanche ruggedness tests (Fig. 1.12b).



(a) (b)

Figure 1.12 – (a) Schematic of the Avogy p-i-n diode with implanted edge termination [64]. (b) 2-inch GaN wafer with fabricated p-i-n diodes [66].

The research group of Prof. Tohru Nakamura at Hosei University presented a p-i-n diode in 2015 with triple drift layer (layer responsible for holding the BV). The drift layer forming the p-n junction was doped to low 10^{15} cm^{-3} to create a near-flat electric field profile and thus reduce the electric field (Fig. 1.13a). Subsequent drift layers were moderately doped to reduce the $R_{on,sp}$ to 1.7 mΩ cm^2, while still presenting a high BV of 4.7 kV [67]. In 2018, they also demonstrated a novel p-i-n diode with a guard-ring termination, as shown in Fig. 1.13b. This structure resulted

in lower leakage current and an improvement in BV by 200 V to obtain a high blocking voltage of 5 kV [68].

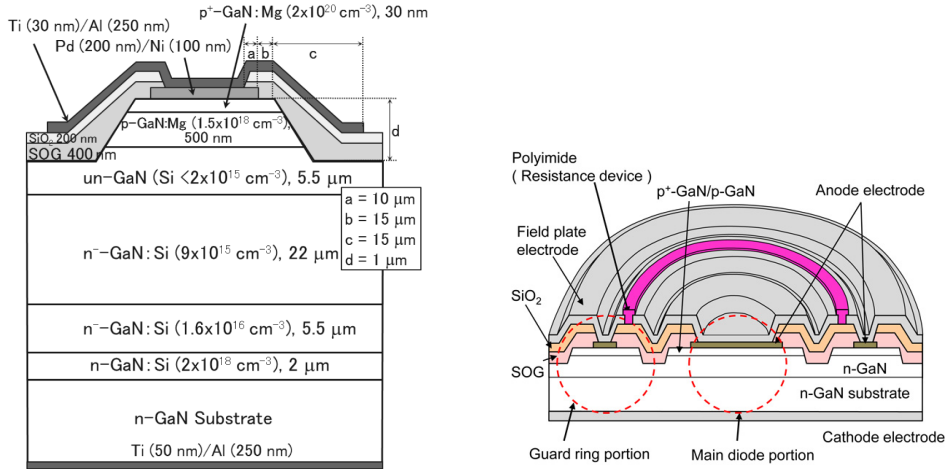
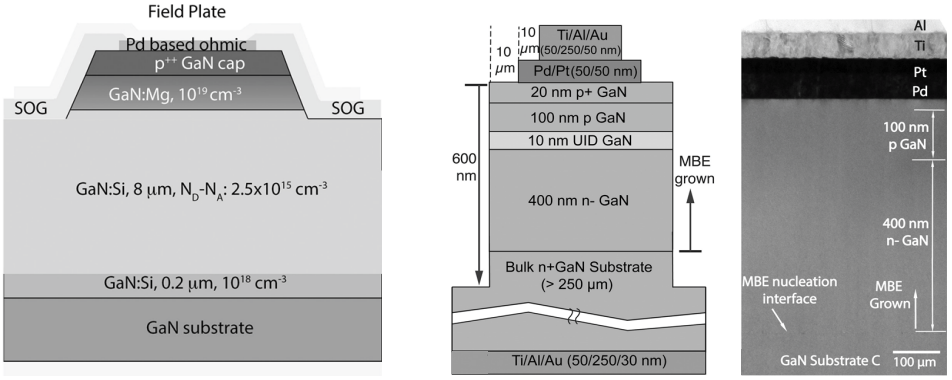


Figure 1.13 – (a) Schematic cross sections of GaN p-n junction diodes with the triple drift layers [67]. (b) Schematic cross section of guard-ring structure used for improving the BV in a p-i–n diode. [68].

Cornell University demonstrated the growth of high quality GaN layers by metal organic chemical vapor deposition (MOCVD) resulting in a low Schottky Reed Hall lifetime of 12 ns [69] (Fig. 1.14a). As a consequence, their p-i-n diodes exhibited an ultra-low $R_{on,sp}$ of 0.12 mΩ cm^2 coupled with a high $BV > 1.4$ kV, thus resulting in a record Baliga's Figure Of Merit (BFOM) of 16.5 GW/cm^2 [69]. They have also demonstrated high BV GaN p-i-n diodes with p-GaN grown by molecular beam epitaxy (MBE) [70, 71], to circumvent the issues faced during p-GaN growth by MOCVD like Mg-memory effect and hydrogen passivation of Mg dopants in p-GaN (Fig. 1.14b). This study also provides an alternative for p-GaN regrowth by MOCVD which could result in impurity incorporation at the growth interface [72, 73] and issues arising from non-planar growth like high leakage currents [74].

Schottky barrier diodes

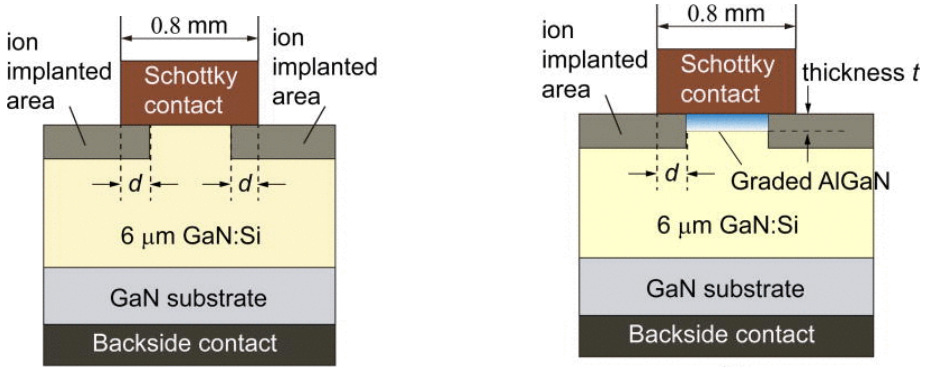
Schottky barrier diodes with $BV >$ than 1 kV were first reported in 2010 by Sumitomo technologies [75]. They perfected the growth of low defect density GaN layers resulting in SBDs with $R_{on,sp}$ of 0.71 mΩ cm^2 and BV over 1100 V achieved using a field plate structure. Large anode diodes of area 1.3 mm × 1.3 mm exhibiting a forward current of 6 A at a forward voltage of 1.46 V and BV of 600 V were also demonstrated. The same group demonstrated the excellent reverse recovery behavior of GaN devices as compared to Si and SiC devices , in 2014. The group at Toyoda Gosei reported high current SBDs presenting a forward current of 50 A at 2 V while also providing an excellent BV of 790 V [76]. These results provided evidence that the scale-up of GaN diodes can provide high forward currents without sacrificing on the BV due to the defects present in GaN substrate.



(a) (b)

Figure 1.14 – (a) Schematic cross section of a GaN p-n junction diodes with passivation and field plate [69]. (b) Schematic structure and cross-section TEM of fabricated vertical MBE-grown p-n diodes [71].

SBDs normally suffer from a trade off between on-current and reverse bias breakdown. The team at HRL Laboratories LLC in USA developed a GaN vertical tunneling Schottky barrier diode in 2016, which gives a good combination of ON- as well as OFF- state performance [77, 78]. The tunneling barrier consisted of 5 nm of graded AlGaN with Al concentration varying from 0 % to 23 % obtained by linearly ramping the flow of trimethyl-aluminum precursor during the MOCVD growth (Fig. 1.15a, 1.15b). These diodes presented almost similar $R_{\text{on,sp}}$ while providing almost double the BV as compared to the control SBD with no tunnel barrier.

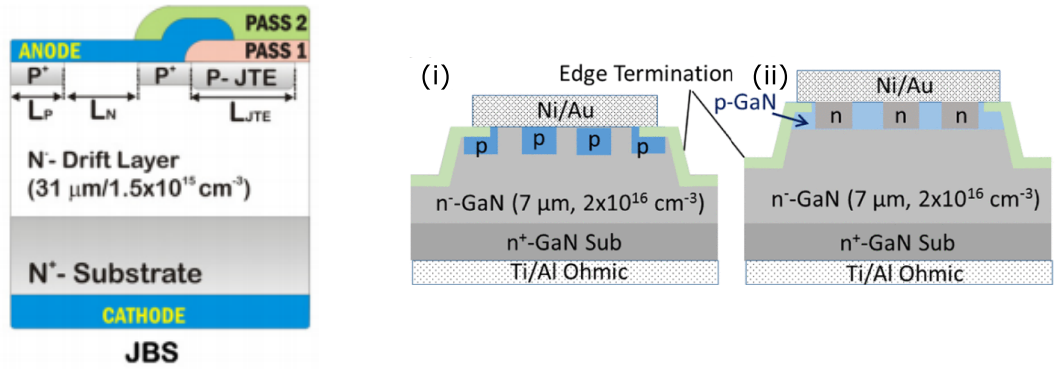


(a) (b)

Figure 1.15 – (a) Schematic cross section of the control SBD [77], and (b) SBD with AlGaN tunnel barrier [77].

In Si and later in SiC, a class of devices called the junction barrier Schottky (JBS) and merged p-i-n Schottky diodes were introduced to improve the off state leakage. Essentially, these devices consisted on p-type doped regions which were created by ion-implantation, adjacent to the

Schottky surface [79] (Fig. 1.16a). These p-doped regions create a depletion region which spreads when a reverse bias is applied to the diode and deplete the electrons near the Schottky surface, thus reducing the leakage current. In the case of GaN, ion implantation is still very



(a) (b)

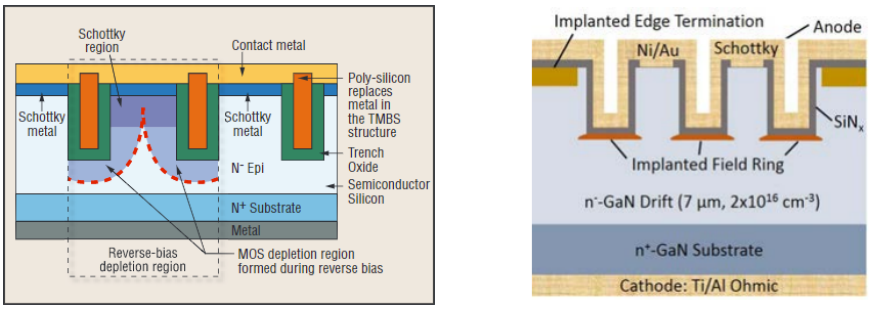
Figure 1.16 – (a) Schematic cross section of SiC JBS diode [79], and (b) GaN JBS diodes with Mg (i) and Si (ii) implantation.

immature and requires specialized instruments capable of handling very high pressures ~ 1 GPa, and high temperatures ~ 1200 °C [80]. However, the group at MIT have demonstrated GaN JBS diodes by implanting Mg in n-GaN and Si in p-GaN [81] (Fig. 1.16b). The implanted Mg was activated using a specific annealing process called the symmetrical multi-cycle rapid thermal annealing (SMRTA) at ~ 1350 °C and the Si by standard rapid thermal annealing (RTA) at ~ 1050 °C. The fabricated diodes presented an $R_{on,sp}$ of 1.5-2.5 mΩ cm^2 for the Mg implanted sample and 7-9 mΩ cm^2 for the Si implanted sample. A BV of 500-600 V was obtained in both the cases.

Compared to the complicated fabrication process involved in the development of GaN based JBS diodes, trench metal barrier Schottky (TMBS) devices are quite easy to fabricate. A TMBS diode consists of a trench metal insulator semiconductor (MIS) structure as shown in Fig. The MIS structure does not contribute to the forward conduction phase but in the reverse bias condition, the two adjacent MIS structures depletes the semiconductor region between them thus, reducing the leakage current and improving the BV [82]. The group at MIT demonstrated a GaN TMBS diode with implanted field rings as shown in Fig. The TMBS diode improved the leakage current by 10^4 fold and improved the BV from 400 to 700 V [83].

Transistors

GaN trench MOSFETs were first reported by ROHM in 2007 [84]. These MOSFETs were fabricated on GaN layers grown by MOCVD on sapphire substrates. They trialled 2 different gate dielectrics; electron cyclotron resonance (ECR) deposited SiO_2/Si_xN_y and PECVD SiO_2. A reduction in V_{th} from 25.5 V to 5.1 V was observed by using the ECR deposited dielectric pair. This work also reported on a high channel mobility of 133 cm^2/Vs. In 2008, the same group



(a) (b)

Figure 1.17 – (a) Schematic cross section of SiC TMBS diode clearly indicating the spreading of the depletion region under reverse bias [82], and (b) GaN TMBS diode [83].

demonstrated the first fully-vertical MOSFET on bulk GaN substrates with similar performance figures as the previous report [85]. Improvements in BV and $R_{on,sp}$ of GaN trench MOSFET were reported by researchers from the Toyoda Gosei corporation in 2014. They demonstrated a GaN trench MOSFET with a field plate termination achieving a BV of over 1.6 kV and $R_{on,sp}$ of 12.1 mΩ cm^2 [86]. In 2015, they reported a similar device with $R_{on,sp}$ improved to 1.8 mΩ cm^2, along with a high BV of 1.2 kV. Large area trench MOSFETs with over 10 A on-state current still maintaining the high BV of over 1.2 kV was also reported by them in 2016 which verify that high dislocation densities in the bulk GaN substrates do not necessarily become a bottleneck for obtaining both high BV and high on-state current with large area devices [58, 87].

Another topology of GaN vertical transistors that was introduced in 2004 is called as the current aperture vertical electron transistor (CAVET) [88], with a structure similar to double-diffused MOS (DDMOS) [89] as shown in Fig. 1.19a. The CAVET structure comprises of an AlGaN/GaN heterostructure at the top, current blocking layers (CBLs) and a n-type doped GaN layer at the bottom. The source terminals form an ohmic contact to the 2DEG and the gate forms a Schottky contact to AlGaN. The CBL restricts the flow of current to a small aperture region which sits just below the gate. By applying a gate bias, the 2DEG below the gate can be switched off or on thus resulting in a transistor behavior.The main foreseen advantage was that under voltage blocking condition, the high field region would sit under the gate in the bulk of the device unlike a lateral HEMT and thus may support large BV as surface related breakdown was eliminated. However, in reality, the device was plagued with leakage issues arising from regrowth steps involved in the fabrication of the device and hence had a poor BV [90–92]. The on-state performance was also very sensitive to the doping of the aperture region which was difficult to control due to the complicated fabrication process. Avogy Inc. in 2014 reported on an improved version of this device with a BV of 1.5 kV and $R_{on,sp}$ of 2.2 mΩ cm^2 [93]. However, the reverse leakage in these devices were also high at 1 mA/cm^2 at 800 V.

For a trench MOSFET, the channel resistance (R_{ch}) is the main bottleneck towards achieving a low R_{ON}. This is due to the fact that the gate trench is made by dry etching which creates defects in the trench sidewall. These defects act as charged species which increase the scattering

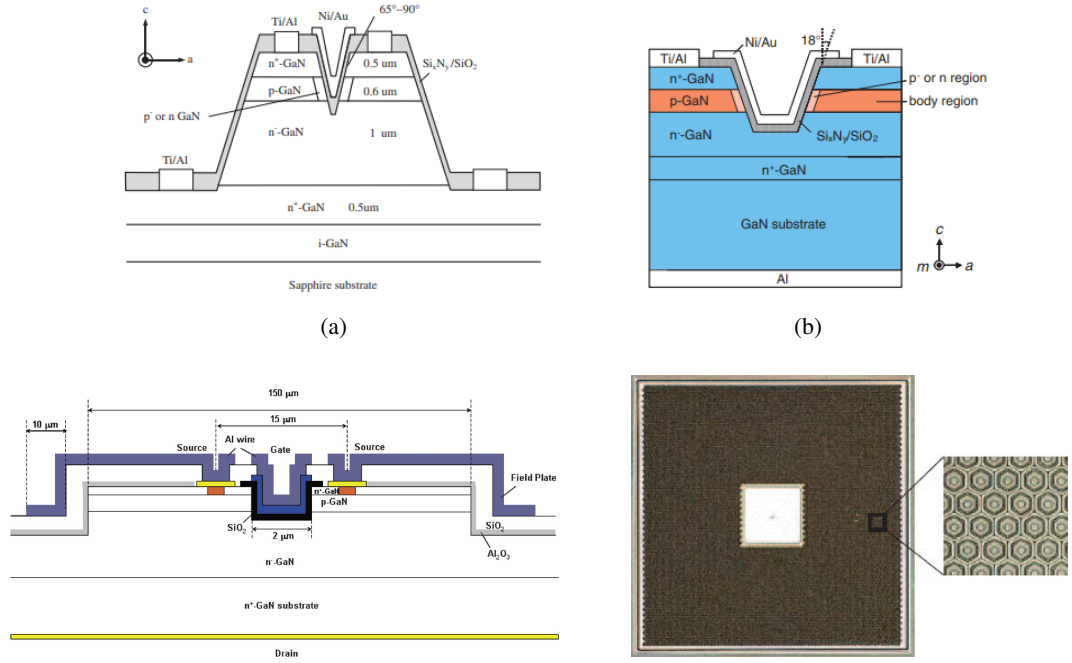


Figure 1.18 – (a) Schematic cross section of a GaN trench gate MOSFET on sapphire substrate [84], and (b) GaN trench gate MOSFET on bulk GaN [85].(c) Schematic of a GaN trench MOSFET with a field plate termination [86]. (d) Chip micrograph of a fabricated multi-cell vertical GaN trench MOSFET of dimension 1.5mm×1.5mm, capable of 10 A on-state current [87].

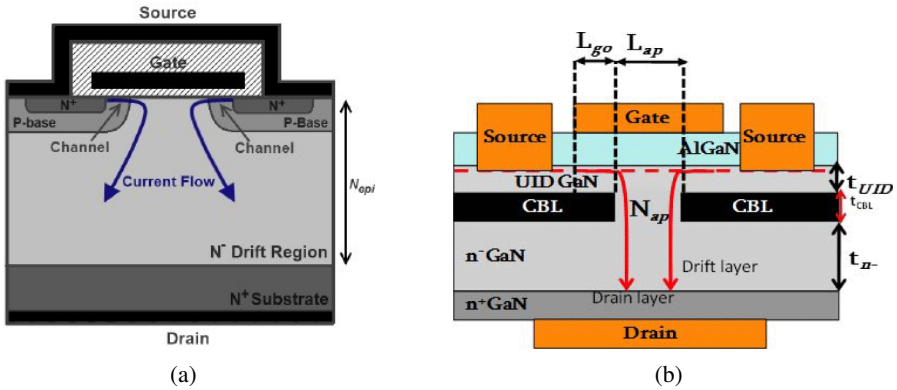
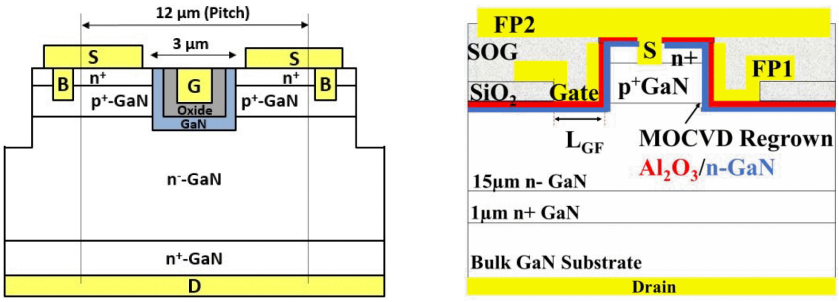


Figure 1.19 – (a) Schematic cross section of a SiC double- diffused MOSFET (DDMOS) [89], and (b) GaN CAVET [24]

of inversion channel charge carriers and thus reduce the effective mobility and the on-state current. Specifically to solve this issue, the group of Prof. Mishra at UCSB devised a new trench MOSFET structure wherein after the gate trench etching, a thin layer of undoped GaN is regrown over the trench along with an in situ Al_2O_3 gate dielectric [94] (Fig. 1.20a). As the inversion

channel is now formed on the thin layer of undoped GaN, the effective channel mobility improved dramatically to as high 185 cm^2/Vs, the highest reported for GaN trench MOSFETs [95]. This device called as the OG-FET provides enhancement mode operation with V_{th} of 3 V, low $R_{on,sp}$ of 2.6 mΩ cm^2 and BV of 1 kV [96]. A novel double field plated geometry improved the BV to 1.4 kV [95] as shown in Fig. 1.20b.

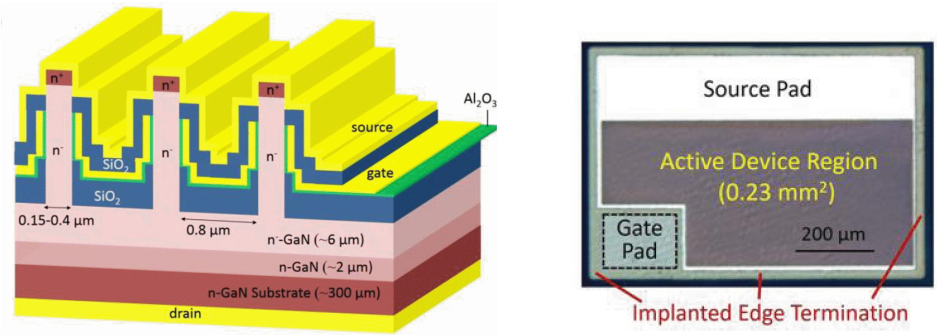


(a) (b)

Figure 1.20 – (a) Schematic of an In-Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET (OG-FET) [96], and (b) OG-FET with gate and source field plate [95].

In recent years, vertical fin power FETs have been demonstrated with sub micron fins on bulk GaN substrates [97]. These devices have the advantage over classical trench MOSFETs that they dont require a p-GaN layer to block the voltage. The gate region of these devices consist of dielectric/gate metal on the fin sidewalls which deplete the charge carriers in the fin due to the work function difference between the gate metal and the GaN, providing a normally-off operation (Fig. 1.21a. However, the fin needs to be sufficiently narrow (< 500 nm) to be completely depleted. The initial devices presented a V_{th} of 1 V, $R_{on,sp}$ of 0.36 mΩ cm^2, and a BV of 800 V [97] (Fig. 1.21a. Large area devices with 5 A on-state current and an excellent BV of 1.2 kV have been recently reported [98] (Fig. 1.21b. These devices break catastrophically possibly due to the absence of p-GaN layers to modulate the electric field peaks. Also the fabrication and control of the fin width could increase the fabrication cost. Since the V_{th} is relatively low, for normal power switching applications, trench MOSFETs should be the best bet.

Thus, high performance vertical p-i-n diodes, SBDs and transistors have been demonstrated on bulk GaN substrates taking advantage of the high quality of these substrates. For p-i-n diodes, the most promising devices were developed by Avogy Inc. as they optimized the growth as well their devices passed several reliability checks. The most promising termination schemes appear to be Ar-implantation at the anode periphery (to create a resistive region) or field plate termination. Complicated termination schemes like guard-ring structures do not provide sufficient improvements in the BV and are difficult to implement from a commercial point of view. With regards to SBDs, since conventional junction termination extensions (JTEs) methods are not mature for GaN due to difficulties in Mg ion-implantation and activation, several other schemes were devised including a graded AlGaN barrier at the top surface and by using plasma terminations at the anode periphery [100, 101]. The plasma termination schemes although



(a) (b)

Figure 1.21 – (a) Side-view three-dimensional schematic of the vertical gan fin power field-effect transistors (fets) with multiple fins [99], and (b) Optical microscopy image of the fabricated large-area device [98].

are very effective, the adoption of such techniques from a commercial point of view is still questionable as the stability of these plasma treatments to subsequent device processing steps involving high temperature or chemical ambient is not known. Incorporation of graded AlGaN barrier and the trenched metal barrier Schottky (TMBS) devices seems to be the way forward for commercializing low leakage and high BV devices. Transistors are the most commonly used power devices and several interesting concepts have been experimentally demonstrated for GaN based FETs. However, not all of these are suitable for commercialization. Vertical GaN finfets demosntrated excellent ON- as well as OFF-state performance however, these devices employ electron beam lithography for obtaining sub micron fins. Although deep-UV lithography systems are on the rise, from power device fabrication point of view, these finfets are quite complicated to implement. Also, since they provide a V_{th} of only $\sim$ 1-2 V similar to lateral HEMTs. The most promising vertical transistor device concept appears to be the OGFET [96]. This device takes care of the low channel mobility of the trench gate MOSFETs and also by adopting novel field plate methods, a high BV can also be achieved [95].

1.4 Motivation

The ideal solution for obtaining high quality GaN layers with defect density less than $10^6/cm^2$ would be homo-epitaxy ie, GaN grown on bulk GaN, as there won't be any lattice mismatch between substrate and epitaxial layer. As a consequence, majority of the devices presented in the previous section were based on bulk GaN substrates. However, even after the demonstration of high performance diodes and transistors with excellent ON- as well as OFF-state characteristics, the commercialization of vertical GaN power devices have been hindered by the high cost and the small diameter of these bulk GaN substrates. Currently, these expensive substrates are being used only for niche applications in LED and laser as shown in Fig. 1.22 [102]. Hence, in order to take advantage of the material benefits that GaN offer for power device applications, further improvements in wafer size and reduction in cost is highly desirable. However, over the past decade, not much improvements have been made, especially in the wafer size which is critical

in reducing the production cost per unit of the device. A strategy to tackle this issue is by

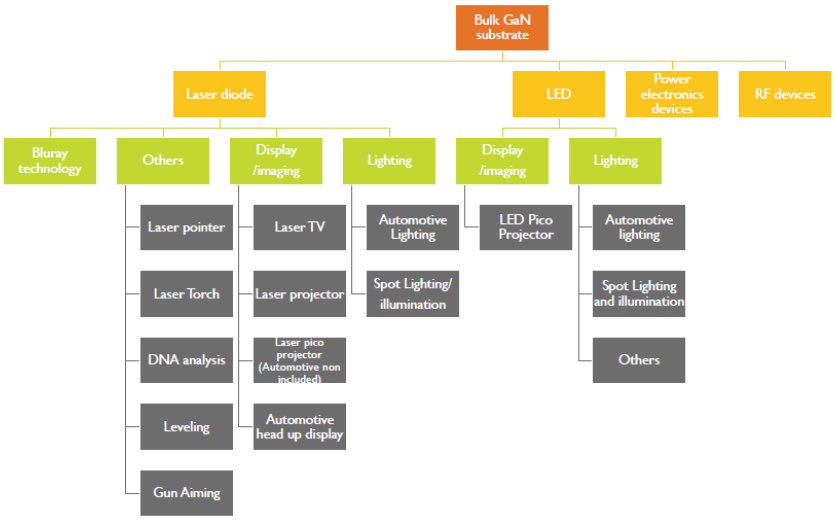


Figure 1.22 – Current application space for bulk GaN substrates [102].

adopting GaN grown on cheaper foreign substrates like Si and sapphire. GaN-on-Si substrates have been widely researched and commercialized for the lateral GaN HEMT technology. A similar approach could be embraced for vertical power devices as well. As observed from Fig. 1.23, GaN-on-Si substrates could give 10-100 times lower wafer + epitaxy cost as compared to bulk GaN [103]. Silicon substrates also provide better thermal and electrical conductivity as compared to sapphire. But the main advantage is that Si substrates are commercially available up to 12-inch diameters which could drastically reduce the overall cost per unit of the device. This could lead to an average cost of manufacturing per device of ~ 1$ similar to silicon based power devices. The adoption of Si substrates could also allow current CMOS compatible fabs to mass produce GaN-on-Si device thus saving the high cost normally required for setting up new technology fabs. Recently, a new class of engineered Si substrates with a poly-AlN core has been introduced. The main advantage of these substrates are that they are coefficient of thermal expansion (CTE) matched to GaN and thus enables the growth of thick, high quality stress free GaN with lower defect density as compared to GaN-on-Si substrates [30, 104]. Thus the future for GaN-on-Si vertical devices seem very promising.

In this thesis I propose to utilize the epitaxial GaN layers grown on silicon substrates to realize high-performance vertical power devices which could further the development of this field towards commercialization. As will be evident from the succeeding chapters, we were able to develop and demonstrate p-i-n diodes, Schottky barrier diodes and power MOSFETs with state-of-the-art ON- and OFF-state performance.

1.5 Major Challenges

GaN-on-Si substrates faces these following major challenges:

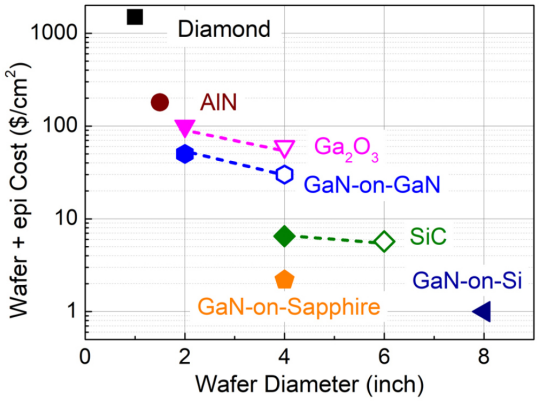


Figure 1.23 – Approximate cost and wafer diameters of substrates for power device applications. The solid symbols show current mainstream cost. The dashed lines and hollow symbols are based on prediction[103].

Large dislocation density

The mismatch in lattice constant and the CTE between GaN and Si is about 17 % and 54 % [65] which results in a high dislocation density of ~ 10^9/cm^2. This also limits the thickness of the GaN layer which can be grown on Si substrates to ~ 3-4 μm, which is not suitable for vertical power device applications. Hence it is necessary to optimize the epitaxy of the GaN on Si substrates to achieve higher thickness while also reducing the defect density.

Inherent quasi-vertical design

When GaN is grown on Si or sapphire substrates, contacting the bottom GaN layer is not possible from the back side of the substrate. A mesa structure is thus made by dry etching to access the GaN bottom layer from the top and thus the contacts are made on the same side of the wafer. This results in a non uniform distribution of current, especially in the ON-state of the device. The current first flows vertically from the anode through the various GaN layers and then spreads laterally to the cathode contact. This creates several bottlenecks especially for current up scaling and also results in non uniform temperature distribution in the device, thus reducing the reliability and life time of the device.

Device termination methods

Si and SiC devices rely on mature and efficient selective doping using ion implantation to create regions of p-doped pockets (for a n-type substrate) around the anode contact. These p-pockets called as junction termination extensions (JTEs) create a depletion region around the anode contact periphery which distributes the electric field in a gradual manner under reverse bias operation, and thus prevents premature breakdown of the device due to localized electric field peaks. these structures also guarantee avalanche breakdown if properly designed. For GaN, unfortunately, ion implantation technique is very immature or requires high temperature and high pressure conditions, calling for the use of highly specialized instruments. Other edge termination methods like field plate, mesa etching, bevel termination, etc., could be used, but they do not

guarantee avalanche characteristics or requires complicated design. Thus a effective method for obtaining reliable devices is still lacking.

1.6 Thesis outline

This thesis aims to overcome the challenges outlined above by developing novel fabrication methods and new materials to obtain high performance p-i-n diodes, Schottky barrier diodes and power MOSFETs.

Chapter 2 reports initially on seminal work regarding to simulation and optimization of fabrication process steps which paved way for high performance devices described in this thesis. A high-performance p-i-n diode with record low on-resistance and breakdown voltage, designed and fabricated based on these optimizations is then described.

Chapter 3 reveals the demonstration of power MOSFETs. A quasi-vertical MOSFET with excellent electrical characteristics is first presented. An investigation into high current power MOSFETs based on this quasi-vertical structure is then reported. Finally, a robust method of achieving a fully-vertical power MOSFET with superior electrical performance is then described which potentially solves the issue of current crowding in quasi-vertical devices.

Chapter 4 discloses one of the main advantages of a quasi-vertical design; device integration. Mainly, we report on power MOSFETs with monolithically integrated freewheeling diode which allows a reverse current to flow during off-state and a reverse blocking (RB) MOSFET which provides protection to the devices against spurious voltage spikes.

Chapter 5 demonstrates a simple and scalable method of achieving p-type JTEs on n-GaN using RF-sputtered highly doped p-type NiO. We report on the initial studies which provide many promising insights. A p-NiO/GaN heterojunction diode and p-NiO JTE for GaN Schottky barrier diode is demonstrated with excellent performance figures.

2 GaN p-i-n diodes on Silcon

In this chapter, we will discuss about the theory, simulation, growth and fabrication of p-i-n diodes on heteroepitaxially grown GaN layers on silicon substrates [45, 105]. The chapter initially gives a theoretical insight about the working principle of power diodes in section 2.2. The section 2.3 talks in detail about the simulation of p-i-n diodes prior to fabrication. As I was the first student of Prof. Elison who conducted research on GaN based vertical devices, a detailed description about the optimization of various fabrication steps are described in the section 2.4. In the subsection 2.4.2, we report the results that we obtained on fabricated GaN-on-Si p-i-n diodes and in subsection 2.4.3, we present the near-junction cooling of these diodes using copper heat spreaders. Finally we conclude with a small summary and benchmarking of our devices. The results presented are from [106] and [107].

2.1 Introduction

A p-i-n rectifier is an ubiquitous device which has found an array of applications in high power circuits, RF switches and attenuators [108–110] . For power applications, even though Schottky rectifiers are preferable due to their low reverse recovery time during switching transients, p-i-n diodes still find applications for motor control and as high power RF attenuators [111–113]. PN junctions are also an integral part of a slew of modern vertical power devices like junction barrier Schottky (JBS) diodes and vertical MOSFETs and thus merits a comprehensive study. Furthermore, pn junctions are helpful in elucidating various material parameters like critical electric field (E_c), doping density, impact ionization coefficients etc. Thus, it becomes easy to elucidate the behavior of complex power devices if the characteristics of basic devices like pn and p-i-n diodes are well understood.

2.2 Theory of p-i-n diodes

In this section we will briefly discuss about the working principle of power p-i-n diodes. Many of the concepts discussed here is from the book of J.Baliga [6]. The 1D structure of a basic p-i-n diode is presented in Fig. 2.1 and displays a thin highly doped p-type (p) region, a thick intrinsic/undoped (i) region and a highly doped n-type (n) region. The thick undoped region also called the drift region is required for blocking high reverse voltage.The electrical behavior can be

Figure 2.1 – Schematic of a p-i-n diode intended for power applications

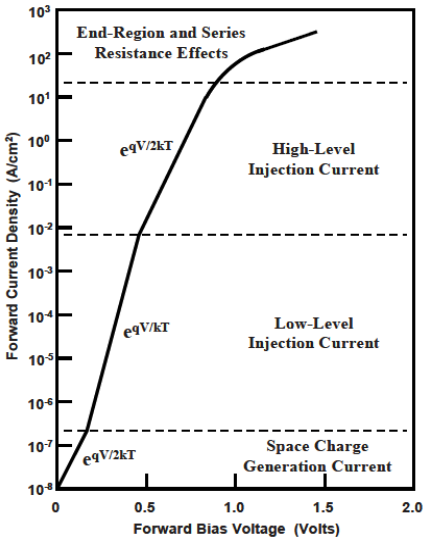


Figure 2.2 – ON-state characteristics of a p-i-n diode

broadly classified into ON-and OFF-state. During the ON-state, the diode is forward biased and the current flowing through the diode and the voltage across it depends on the injection level as shown in Fig. 2.2. At very low-current levels, generation current in space-charge region of the pn junction, proportional to $e^{\frac{qV_a}{2kT}}$ is the dominant phenomenon, where V_a is the applied forward voltage. As V_a is increased further, low level injection of minority carriers into the undoped drift region increases resulting in a current proportional to $e^{\frac{qV_a}{kT}}$. After this voltage regime, high level injection of minority carriers occur which results in conductivity modulation of the drift region and thereby a rapid increase in the current flowing through the diode and the current again becomes proportional to $e^{\frac{qV_a}{2kT}}$.For power applications, it is desirable to have a low specific ON-resistance (R_{ON}) defined by $\frac{\delta V}{\delta J}$, where J is the current density . This can be achieved by doping the drift layer to increase the conductivity but then it increases the reverse leakage current and reduces the maximum reverse breakdown voltage (BV). Thus, there is always a trade-off between the R_{ON} and BV which depends on the type of application for which the devices will be used. In the OFF-state operation, the diode is reverse biased and the voltage-blocking capability is determined by the electric field (E) profile in the drift region of the p-i-n diode. Since p-i-n diodes follow a punch-through design philosophy, whereby a thin 'i' region of very low doping is sandwiched between two heavily doped p and n layers, the electric field follows a trapezoidal distribution as opposed to a triangular shape observed for normal pn diodes as shown in Fig. 2.3.

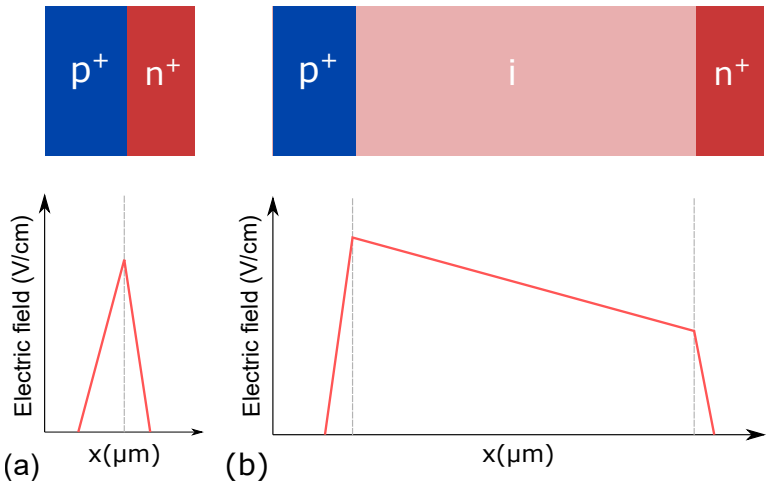


Figure 2.3 – Electric field profile in a (a) pn diode and (b) p-i-n diode at reverse bias

Thus, as the electric field follows a more gradual distribution, it is possible to achieve a higher breakdown voltage as compared to a pn diode with similar doping levels for p and n layers. It is interesting to note that the drift region in a p-i-n diode becomes completely depleted at a low reverse bias given by:

$$V_{dep} = \frac{qN_D(2d)^2}{2\epsilon_s} \tag{2.1}$$

After this voltage, the depletion region remains almost independent as the end p and n regions are heavily doped.

The main contributors to leakage current in a reverse biased pn junction is from space-charge generation current and diffusion current. The carriers generated in the space-charge region drift towards either side of the depletion region depending on their charge and the electric field direction. An analytical formula for this generation current is given by

$$J_{sc,leakage} = \frac{qW_{\mathrm{D}}n_i}{\tau_{sc}} \tag{2.2}$$

where $J_{sc,leakage}$ is the space charge leakage current, W_{D} is the depletion region width, τ_{sc} is the space-charge generation lifetime and n_{i} is the intrinsic carrier concentration of the semiconductor. The diffusion component of the leakage current arises from the minority carrier generated near to the depletion region boundary and which are then swept by the electric field in the depletion region to either sides of the junction. The total diffusion current due to this minority carrier

generation is given by

$$J_{diff,leakage} = \frac{qD_{\mathrm{p}}{n_i}^2}{L_{\mathrm{p}}N_{\mathrm{D}}} + \frac{qD_{\mathrm{n}}{n_i}^2}{L_{\mathrm{n}}N_{\mathrm{A}}} \tag{2.3}$$

These equations are valid for semiconductors with low defect density layers. However for semiconductor layers like GaN grown on Si and Sapphire, where the defect density is in the order of ~ 1 $\times 10^8$ to ~1×10^9 /cm^2, other mechanisms like variable range hopping (VRH) contribute additionally to the leakage current. This will be discussed in more detail in 2.4.2.

2.3 Simulation of GaN p-i-n diodes

Simulation provides important insights into the electrical and thermal behavior thus aiding a great deal in optimizing the design of a semiconductor device. For GaN-based power devices, the simulation tool ATLAS, by Silvaco, is the most widely used TCAD tool as it is very efficient in providing accurate simulations of the device behavior [114]. ATLAS has a wide array of capabilities thanks to a comprehensive set of physical models and sophisticated numerical methods available for obtaining a convergent solution. These physical models and numerical methods are then used for solving Poisson and current continuity equations in 2D/3D for electrons and holes to obtain electrical characteristics of the device. Thus, selection of these models/methods are vital for the accurate simulation of a device. For GaN, the physical models of relevance are regarding impact ionization, electron and hole mobility, carrier recombination and velocity saturation. These material properties have been widely investigated by a lot of research groups and the model parameters describing these properties are available in literature determined either from Monte Carlo simulations or from experiments.Some of the important models which are required for the accurate simulation of GaN-based vertical devices are briefly described as following [115].

IMPACT IONIZATION : In any space charge region caused by sufficiently high reverse bias, the free carriers are accelerated by the high electric field which creates additional collisions with lattice atoms to create other free carriers. This phenomenon is called Impact ionization and is very important phenomenon happening in semiconductors at high reverse bias. This defines the onset of avalanche breakdown and an accurate representation for GaN is obtained including the Selberherr's impact ionization model which is a variation of the classical Chynoweth model. The expressions for impact ionization coefficients α_n and α_p for electron and hole in this model is given by

$$\alpha_n = \mathrm{AN}\exp\left[-\left(\frac{BN}{E}\right)^{BETAN}\right] \qquad \alpha_p = \mathrm{AP}\exp\left[-\left(\frac{BP}{E}\right)^{BETAP}\right] \tag{2.4}$$

, where AN,AP are the impact ionization coefficients for electrons and holes, BN and BP are the critical electric field values for GaN with n and p type doping. BETAN and BETAP are power factors for electrons and holes. The parameters values of the parameters used for fitting this model for GaN is given in the table 2.1.

AN (cm^{-1})	BN (V/cm)	AP (cm^{-1})	BP (V/cm)	BETAN	BETAP
2.52×10^{8}	3.41×10^{7}	5.37×10^{6}	1.96×10^{7}	1	1

Table 2.1 – default values for the Selberherr impact ionization parameters

MOBILITY : For modelling electron and hole mobility, velocity saturation and velocity overshoot, the GANSAT.P and GANSAT.N statements are specified in the mobility section of the simulation.These models can accurately model the velocity variation with respect to field for various low-field mobilities as shown in Fig. 2.4.

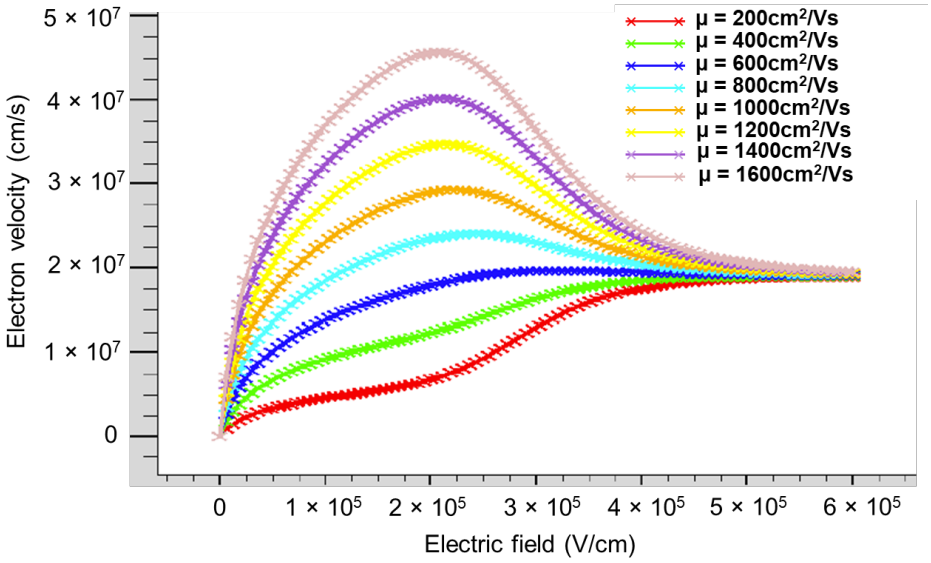


Figure 2.4 – Simulated velocity-field curves for pure GaN for various low-field mobilities

The mobilty for electrons and holes in GaN follow the analytical expressions:

$$\mu_n = \frac{\mu_{n0}(T,N) + VSATN\frac{E^{N1N.GANSAT-1}}{ECN.GANSAT^{N1N.GANSAT}}}{1 + ANN.GANSAT\left(\frac{E}{ECN.GANSAT}\right)^{N2N.GANSAT} + \left(\frac{E}{ECN.GANSAT}\right)^{N1N.GANSAT}} \tag{2.5}$$

$$\mu_p = \frac{\mu_{p0}(T,N) + VSATP\frac{E^{N1P.GANSAT-1}}{ECP.GANSAT^{N1P.GANSAT}}}{1 + ANP.GANSAT\left(\frac{E}{ECP.GANSAT}\right)^{N2P.GANSAT} + \left(\frac{E}{ECP.GANSAT}\right)^{N1P.GANSAT}} \tag{2.6}$$

VSAT is the saturation velocity, μ_{n0} and μ_{p0} are low field mobility terms, ECN and ECP are critical electric field values for n-type and p-type bulk GaN, ANN, ANP, N1N,N1P, N2N, N2P are fitting parameters. The parameter values for electrons are enlisted in the table 2.2. The model is only calibrated for electrons and for holes it is necessary to find a set of real default values from literature. CARRIER RECOMBINATION : The major carrier recombination mechanism

VSATN (cms^{-1})	ECN.GANSAT (kV/cm)	N1N.GANSAT	N2N.GANSAT	ANN.GANSAT
1.9064×10^7	220.8936	7.2044	0.7857	6.1973

Table 2.2 – default parameter values from Monte Carlo fits for electron mobility model

occurring in GaN is the non-radiative Schottky Read Hall (SRH) mechanism. Here, charge carriers are released or excited to trap or dopant levels in the forbidden bandgap with the release of phonons instead of photons. It can be modelled as:

$$R_{SRH} = \frac{pn - {n_i}^2}{TAUP0\left[n + n_i \exp\left(\frac{ETRAP}{kT_L}\right)\right] + TAUN0\left[p + n_i \exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \tag{2.7}$$

$ETRAP$ is the energy difference between the trap level and the intrinsic Fermi level, T_L is the lattice temperature, and $TAUN0$ and $TAUP0$ are the electron and hole lifetimes. In GaN, $TAUN0$ and $TAUP0$ are in the range of ns.

BAND-TO-BAND TUNNELING :P-I-N diodes are normally designed to support large reverse bias voltages. At high enough reverse bias, the band bending is sufficient enough to allow electrons to tunnel from valence band to conduction band thus generating an additional electron in conduction band and a hole in the valence band. This generation rate G_{BBT} is given by:

$$G_{BBT} = D \times BB.A \times E^{BB.GAMMA} \times \exp - \left(\frac{BB.B}{E}\right) \tag{2.8}$$

Where E is the magnitude of the electric field , D is a statistical factor, and $BB.A$ and $BB.B$ are parameters which depend on the electron effective mass ($MASS.TUNNEL$) and bandgap ($EG300$), and is given by:

$$BB.A = \frac{q^2\sqrt{(2 \times MASS.TUNNEL \times m_0}}{h^2\sqrt{EG300}} \tag{2.9}$$

$$BB.B = \frac{\pi^2 EG300^{\frac{3}{2}}\sqrt{\frac{MASS.TUNNEL \times m_0}{2}}}{qh} \tag{2.10}$$

$$BB.GAMMA = 2 \tag{2.11}$$

2.3.1 Optimization of forward characteristics of a GaN p-i-n diode

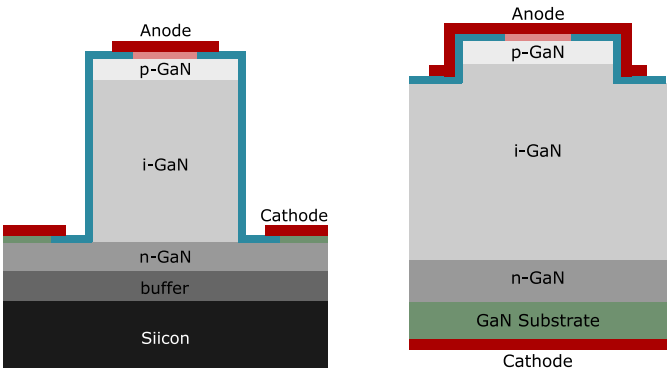
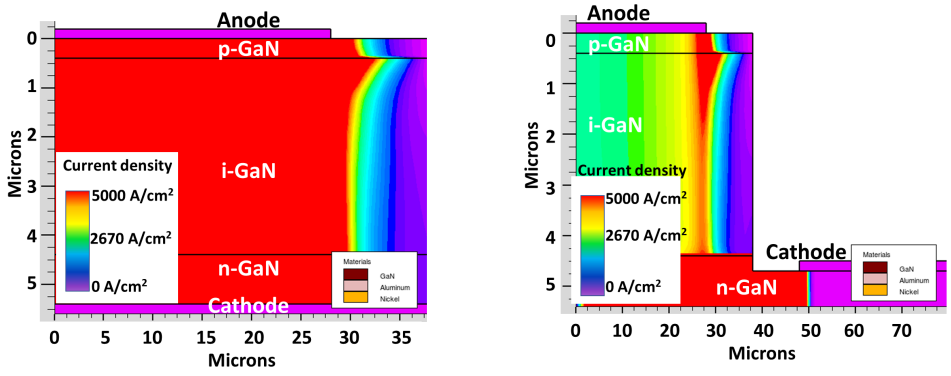


Figure 2.5 – Schematic of a GaN (a) quasi-vertical and (b) fully-vertical p-i-n diode.

Fig. 2.5a and Fig. 2.5b shows the schematic of a quasi- and a fully-vertical p-i-n diode. The structure as shown reveals a thin p-type layer, a thick undoped i-layer,a thin n-type doped layer and either a Si or GaN substrate at the bottom. In the case of a fully-vertical diode, the current flows vertically as evident from the current density plot @ 10 V forward bias in Fig. 2.6b and the specific ON-resistance ($R_{on,sp}$) defined as $\frac{\Delta V}{\Delta J}$ depends only on the GaN material parameters like doping, mobility etc and the contact resistance offered by the ohmic contact to p-and n-type GaN. In a quasi vertical p-i-n diode, like in the case of GaN grown on Silicon substrates, the situation is a bit more complex as a consequence of the bottom n-type layer not being accessible like in the case of a fully vertical diode. Hence it is necessary to etch the GaN surrounding the anode contact to access the n-type GaN and form the cathode contact on the same side as the anode. Since the cathode is no longer placed diametrically opposite to the anode, the current distribution is more complicated as obvious from Fig. 2.6a. The current first flows down vertically through the GaN layers and then flows laterally to the cathode. Also the majority of the current flows through the region around the edge of the anode contact.We studied the impact of this non-uniform current distribution on the $R_{on,sp}$ of the devices by varying the anode size, the thickness of the drift layer, thickness and doping of n-GaN layer as summarized below. The p-i-n epitaxial structure used in this simulation consisted of 0.4 µm-thick p-GaN ($N_A \sim 3\times 10^{17}$ cm^{-3}), 4 µm-thick GaN drift layer ($N_D \sim 2\times 10^{16}$ cm^{-3}), 1 µm-thick n-GaN ($N_D \sim 1\times 10^{19}$ cm^{-3}).

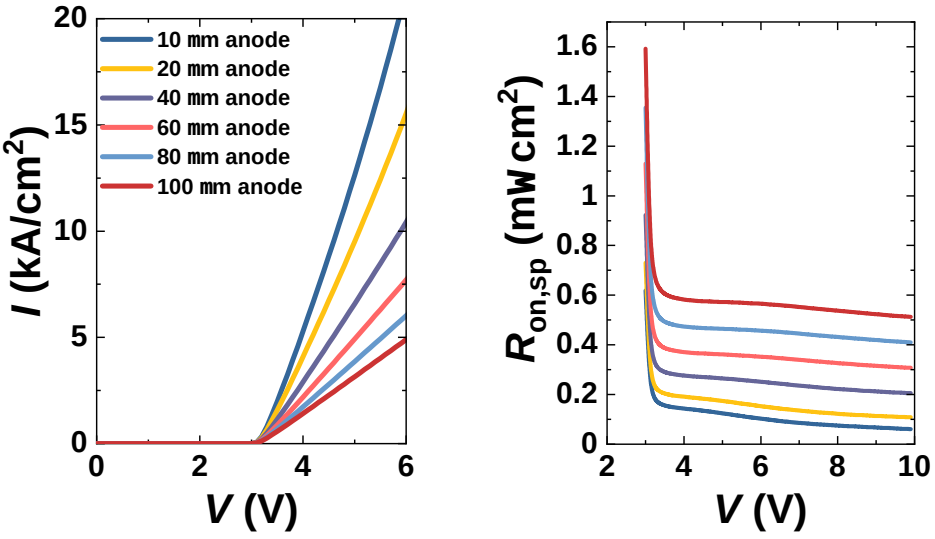
IMPACT OF ANODE SIZE: As shown in Fig. 2.6b, the current flow in a quasi-vertical p-i-n diode is slightly complicated as compared to a fully-vertical p-i-n diode. A major part of the current flows vertically from under the anode electrode through the p- and the i-GaN layer to the n-GaN layer and then the laterally to the cathode contact. Since there is a change in direction of flow of the current, it creates an undesirable phenomenon called current crowding near the cathode. This is evident from the high current density near the cathode terminal in Fig. 2.6a. It is basically an introduction of resistance to the current flow as a result of the constriction formed by the mesa edge and the cathode placement. The extent of current crowding depends on the thickness and the doping of the n-GaN layer and on the amount of current flowing through the



(a) (b)

Figure 2.6 – TCAD simulation of current distribution @ 10 V in (a) fully-vertical and (b) quasi-vertical p-i-n diode.

device. Keeping these parameters as constant, we varied the anode size and observed the changes in electrical parameters due to current crowding.



(a) (b)

Figure 2.7 – (a) *I-V* characteristics of the p-i-n diodes with varying radii. (b) Comparison of $R_{on,sp}$ of these diodes

Forward characteristics of p-i-n diodes of radii 10 µm, 20 µm, 40 µm, 60 µm, 80 µm and 100 µm were simulated incorporating the required models as explained before. Since the device is symmetric in the y-axis, only half of the device was simulated as shown in Fig 2.6b. Fig. 2.7a shows the *I-V* plot of diodes with various radii. As observed, the best current density (I) is obtained for the diode with the smallest radius of 10 µm. As the anode radius is increased, the current density gets degraded. This can be explained as follows. For a fully-vertical design, if we increase the size of the anode, the current increases proportional to the increase in area as

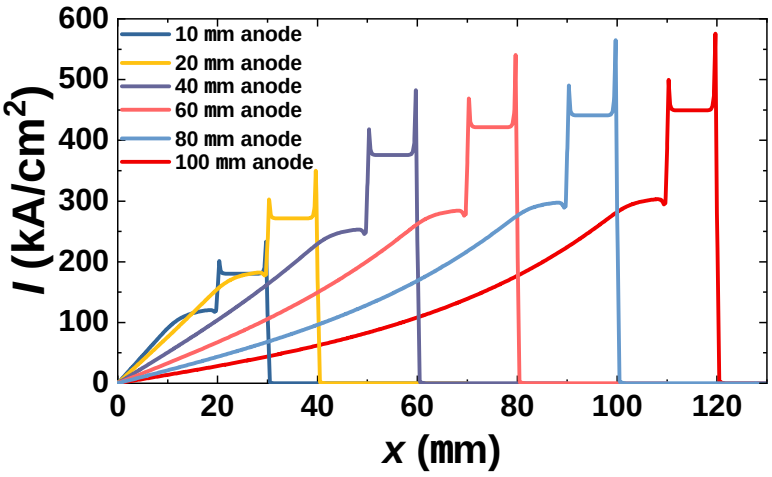
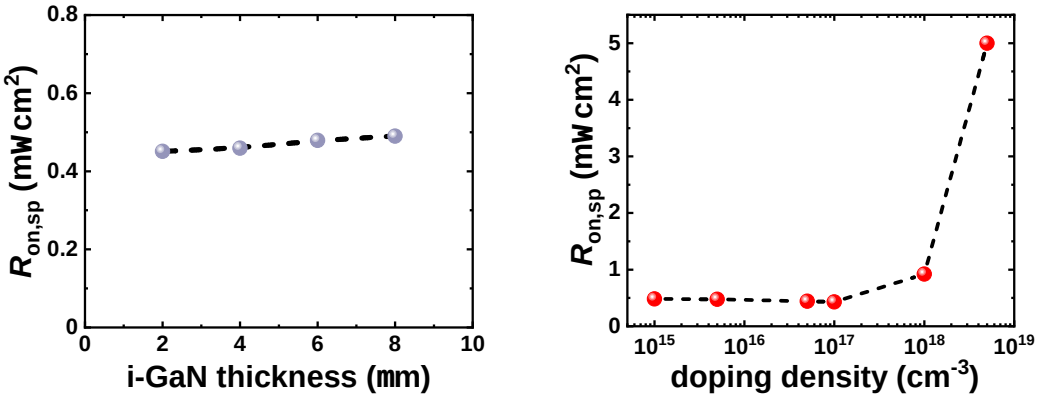


Figure 2.8 – Current density distribution in the bottom n-GaN layer for diodes with various anode sizes.

the current flows vertically from anode to cathode without any additional parasitic resistance. However, for a quasi-vertical diode, since the current conduction is not completely vertical, any increase in anode area doesn't result in a proportional increase in current due to a phenomenon called current crowding where a lateral current injection creates a potential drop in non-zero resistivity layers [116, 117]. This creates a region of non-uniform current density (current crowding) in a quasi-vertical device which could lead to device degradation in localized areas. Thus, it is a design issue which limits the device operating parameters to values smaller than what the material can tolerate without degradation. The current crowding effect in the bottom n-GaN layer close to the cathode increases when we try to flow more current by increasing the area of the anode. Fig. 2.8 presents the local current density in the n-GaN layer near the cathode in quasi-vertical p-i-n diodes of various anode radii. The peak region corresponding to each radius indicates the region of the n-GaN close to the cathode. As observed, the current density increases with increasing the anode radius as more current is flowing through the device and thus the current crowding is higher. However, when we increase the anode radius beyond a certain value, the sheet resistance of the bottom n-GaN layer can no longer support any more increase of current and thus the current density saturates as shown in Fig 2.8 which shows the evolution of the current density at the n-GaN layer close to the cathode, with the anode radius.

IMPACT OF DRIFT LAYER THICKNESS AND DOPING The drift layer (i-GaN) thickness of a quasi-vertical p-i-n diode was varied from 2 µm to 8 µm in the simulation to understand the effect of drift layer thickness on the $R_{on,sp}$. The thickness and the doping of all other layers were kept constant (0.4 µm-thick p-GaN ($N_A \sim 3\times 10^{17}$ cm^{-3}), 1 µm-thick n-GaN ($N_D \sim 1\times 10^{19}$ cm^{-3})). From Fig. 2.9a we observe that the $R_{on,sp}$ remains fairly constant for various thickness of the i-GaN. Thus, we understand that the resistance offered by the i-GaN layer is not a significant contributor to the total $R_{on,sp}$. We also tried varying the doping of the i-GaN layer from 1×10^{15}cm^{-3} to 1×10^{17}cm^{-3} keeping the thickness constant at 4 µm. As observed from Fig. 2.9b, there is little change to the $R_{on,sp}$ with resistivity of the i-GaN layer.



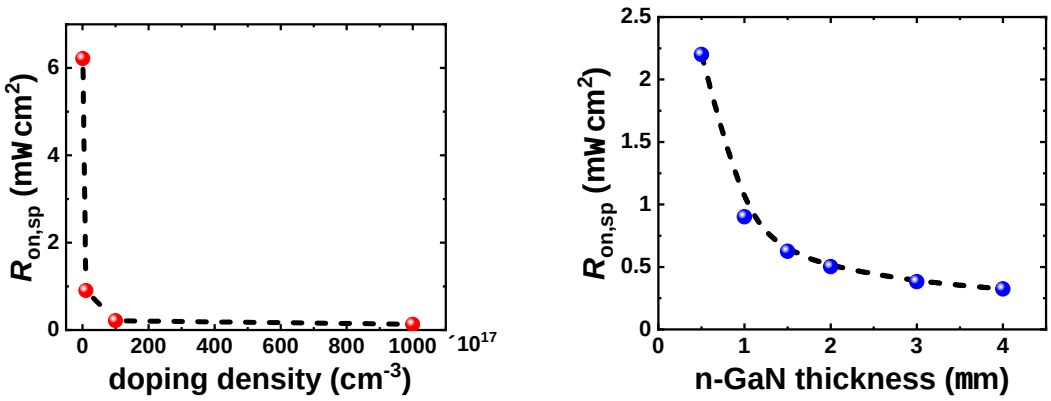
(a) (b)

Figure 2.9 – (a) $R_{on,sp}$ vs thickness of the i-GaN layer, @ 5 V. (b) $R_{on,sp}$ vs doping of the i-GaN layer, @ 5 V.

IMPACT OF n-GaN LAYER PROPERTIES The impact of the doping as well as the thickness of the n-GaN layer was studied using TCAD simulations keeping the thickness and doping of other layers constant (0.4 µm-thick p-GaN ($N_A \sim 3\times 10^{17}$ cm^{-3}), 4 µm-thick GaN drift layer ($N_D \sim 2\times 10^{16}$ cm^{-3})).This analysis is of great importance in the case of GaN-on-Si substrates due to the limitation in the total thickness of GaN which can be grown without film cracking. Typically, the thickness of n-type GaN layer is ~ 1 μm. So an accurate knowledge of the impact of the doping and the thickness of the n-GaN layer is of paramount importance. For a quasi-vertical diode as in the case of Fig. 2.6a, the doping of the bottom n-GaN layer was varied from 1×10^{17}cm^{-3} to 1×10^{20}cm^{-3}, keeping the thickness of the n-GaN layer the same at 1 µm. As seen in Fig. 2.10a, the $R_{on,sp}$ is the smallest for the highest doping which corresponds to the lowest sheet resistance (R_{sh}) of the n-GaN layer. This is because, a higher doping can allow a higher current to pass through before current crowding sets in. The impact on $R_{on,sp}$ with the thickness of the n-GaN layer was also investigated keeping the doping of the n-GaN layer at 1×10^{19} cm^{-3}. In order to obtain a clear picture, the doping of the n-GaN layer for this study was kept at a moderate value of 1×10^{18}cm^{-3} and the thickness was varied from 0.5 µm - 4 µm. As seen from Fig. 2.10b, increasing the thickness of the n-GaN layer reduces the R_{sh} given by $1/q\mu N_D$, where µ is the mobility and N_D is the doping density of the GaN layer; and thus improves the current crowding. These results indicates that the $R_{on,sp}$ of a quasi-vertical diode is determined mainly by the R_{sh} of the bottom n-GaN layer and not so much by the resistivity of the i-GaN layer.

2.3.2 Optimization of reverse characteristics of a GaN p-i-n diode

A reverse bias simulation provides key insights which are helpful in designing a p-i-n diode for a required BV rating. The three main regions of critical importance in a reverse bias simulation are the i-GaN layer, the p-i junction and the anode contact as shown in Fig. 2.5a and Fig. 2.5b. During reverse bias, the depletion region extends more in the i-GaN as it is only lightly doped in comparison to p-GaN ($N_D \sim 0.01 N_A$). Hence much of the reverse bias voltage is held by the i-GaN layer. Thus the doping and the thickness of the i-GaN layer play an important role in



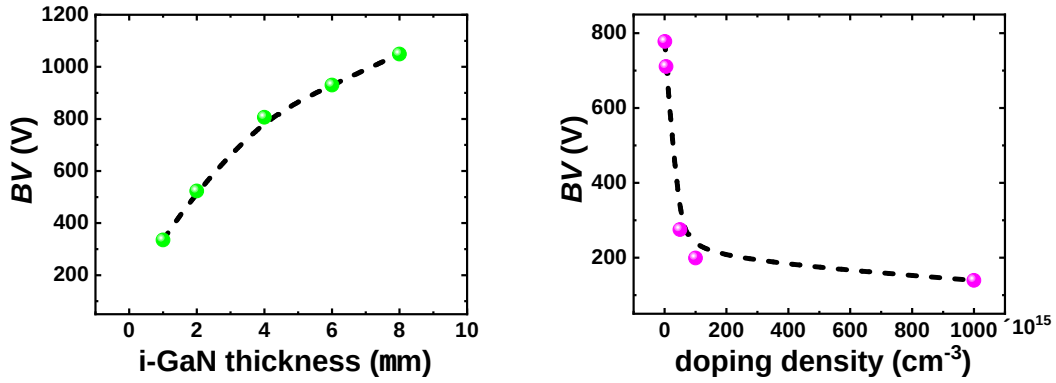
(a) (b)

Figure 2.10 – (a) $R_{on,sp}$ @ 5 V vs doping density of the n-GaN layer. (b) $R_{on,sp}$ @ 5 V vs thickness of n-GaN layer.

deciding the maximum achievable BV and leakage current through the device. From the electric field point of view, the distribution in a p-i-n diode follows a triangular or trapezoidal shape depending upon the applied reverse bias with the peak value observed at the p-i junction which is linearly dependant on the doping of i-type GaN layer in a punch through diode. Also, since the anode contact is of finite dimension, the electric field peaks in GaN at the location of the anode contact edge. Thus for the proper design of a p-i-n diode, all these design consideration have to be taken into account. We investigated the effect of i-GaN material attributes like thickness/doping and junction termination methods like field plate, mesa etching and bevel termination etc as described below.

IMPACT OF i-GaN LAYER THICKNESS AND DOPING Fig. 2.11a shows the impact of increasing the i-GaN layer thickness on the BV (0.4 µm-thick p-GaN ($N_A \sim 3\times 10^{17}$ cm^{-3}), 1 µm-thick n-GaN ($N_D \sim 1\times 10^{19}$ cm^{-3})). As the i-GaN thickness is increased, the electric field in the vertical direction distributes over a higher thickness and thus the reverse voltage at which the peak electric field in the device approaches the critical electric field (E_c) is higher. For a 4 µm thickness of i-GaN layer, the BV decreases with increasing the doping of the i-GaN layer as shown in Fig. 2.11b as the electric field in the device is proportional to the doping of the i-GaN layer and thus the E_c is reached at a lower reverse voltage.

IMPACT OF TERMINATION METHODS Power devices require stable and effective edge termination methods for effective distribution of electric field crowding at the periphery of the device active area, thus guaranteeing their safe and reliable operation. The most common edge termination methods include field rings, junction termination extension (JTE), field plates, trench termination, bevel termination etc. From among these, a well designed JTE spreads the electric field uniformly without any local peaks. For power devices based on Si, and SiC, it is possible to create JTE and field rings by either implantation or diffusion of p-type dopant species. However, for GaN, doping by implantation/diffusion is still in incipient stages. Hence, the most common methods of edge termination for GaN based power devices are trench termination, bevel termi-



(a) (b)

Figure 2.11 – (a) BV vs thickness of the i-GaN layer. (b) BV vs doping of the i-GaN layer.

nation, by using field plates. A brief description about these methods are as follows. Fig. 2.12 shows a quasi-vertical power diode employing a trenched mesa structure. Such a structure can be easily realized by a shallow GaN dry etch around the anode region using the anode as the hard mask. The use of such a termination distributes the electric field crowding from the anode edge to the trenched mesa. However, this termination has to be carefully designed with respect to the trench depth. As observed in the Fig. 2.12, an electric field peak can form at the edge of the mesa trench leading to premature breakdown.

Fig. 2.13 shows the bevel termination on a quasi vertical p-i-n diode. A bevel shaped termination can be obtained by using a hard or softmask which has a slanted sidewall. During the GaN etching, the slantness of the mask is transferred to GaN. The bevel termination has the advantage that if the angle of the bevel is sufficiently low (< 10 °), then the electric field distribution at the p-GaN/i-GaN interface is more uniform than without any termination. Also, if carefully designed (thickness, doping of p-GaN), the electric field peak will happen within the bulk of GaN thus increasing the chance of a reversible avalanche breakdown. We observed from TCAD simulations that a 2 ° shallow bevel angle along with increasing the p-GaN layer thickness to 0.8 µm can effectively contain the electric field peak to inside the bulk GaN layers. This will be elaborated in more details in section 6.2

Fig. 2.14 represents a p-i-n diode with a field plate termination. For materials like GaN, this type of termination is the most effective and the easiest. The field plate consists of a a portion of the anode terminal overhanging a dielectric layer. Such a structure creates a depletion region under the dielectric overlapped region, thus creating a depletion region and redistributing the electric field peak which appears at anode contact edge in the case of a diode without any termination. The effectiveness of the field plate can be modulated by changing the overhanging length, increasing/decreasing the thickness of the dielectric, the dielectric constant of the dielectric, etc. For this simulation setup, a field plate length of 5 µm and SiO_2 dielectric of 100nm thickness was observed to be the optimum field plate length for maximizing the BV. Please note that in Fig. 2.14, the electric field inside the dielectric is 0 as the simulation result is shown at a low reverse

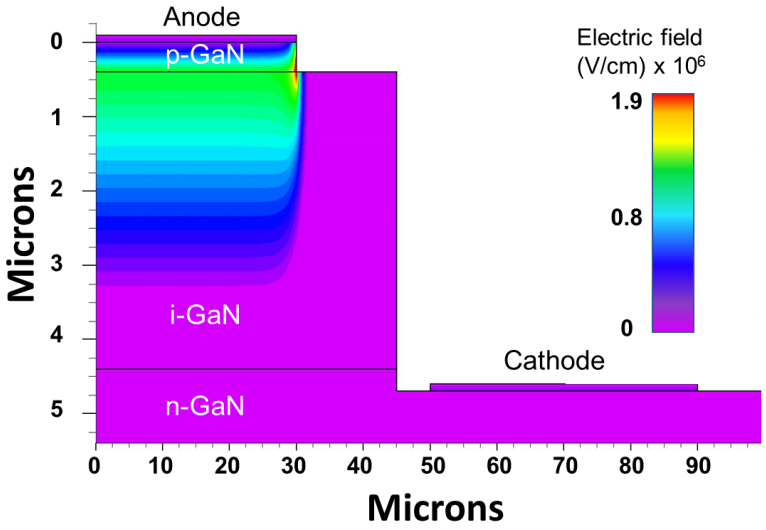


Figure 2.12 – Electric field distribution at a reverse bias of 200 V, revealing a peak at the mesa edge.

bias of 200 V when the electric field in the p-GaN layer hasnt yet reached the top anode metal layer incorporating the field plate.

2.4 GaN-on-Si p-i-n diode

GaN-on-Silicon substrates provide a cost-effective platform as compared to bulk-GaN for the future adoption of GaN-based power devices.Recent demonstrations of GaN-on-Si p-i-n diodes and power MOSFETs reveal the great promise of such substrates [118–121]. Fully-vertical p-i-n diodes have also been demonstrated by substrate removal reaching a BV up to 500V [119, 121]. However, these values are much below the performances demonstrated in bulk GaN and for their use in practical applications, both the BV and $R_{on,sp}$ need to be significantly improved. In this section we will first describe about the growth of the p-i-n layers by Metal Organic Chemical Vapor Deposition (MOCVD), followed by fabrication and then the electrical behavior of quasi-vertical p-i-n diodes fabricated on GaN-on-Si providing the highest reported BV of 820 V, lowest reported $R_{on,sp}$ of 0.33 mΩ cm^2, resulting in a record Baliga's Figure of Merit (BFOM) of 2.0 GWcm^{-2}, the highest reported for GaN grown on foreign substrates like Si and Sapphire [106]. The details mentioned here are from our paper [1].

Growth of p-i-n epitaxial layers on Silicon

This part of the project was done in collaboration with Enkris Semiconductors[122]. The p-i-n epitaxial structure consisted of 0.4 µm-thick p-GaN ($N_A \sim 3\times 10^{17}$ cm^{-3}), 4 µm-thick GaN drift layer ($N_D \sim 2\times 10^{16}$ cm^{-3}), 1 µm-thick n-GaN ($N_D \sim 1\times 10^{19}$ cm^{-3}) and 1.1 µm-thick buffer layer grown on p-type Si, as shown in Fig. 2.15. All the GaN layers were grown by metal-organic

[1] R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, "820-V GaN-on-Si Quasi-Vertical p-i-n Diodes With BFOM of 2.0 GW/cm^2," IEEE Electron Device Letters, vol. 39, no. 3, pp. 401–404, Mar. 2018. Contribution: First author.

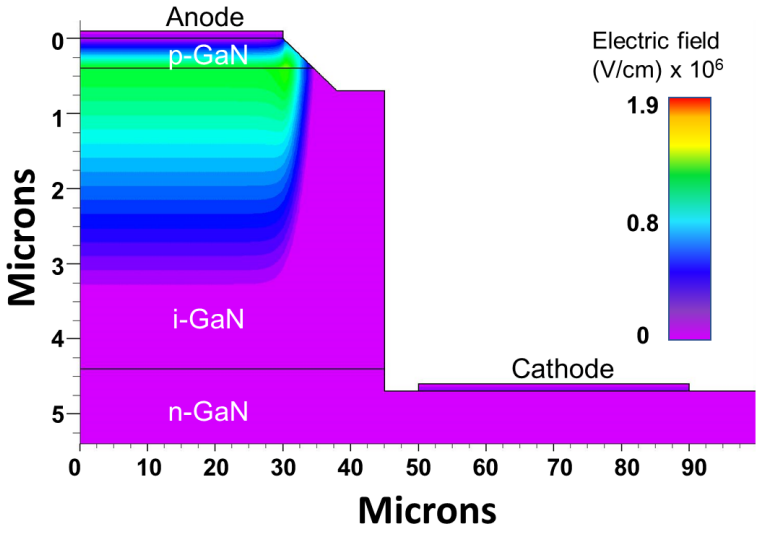


Figure 2.13 – Electric field distribution at a reverse bias of 200 V, revealing a slight localized peak inside the GaN bulk.

chemical vapor deposition (MOCVD) on 6-inch Si (111) substrates.

High quality buffer layers with low defect densities are important to grow thick GaN-on-Si with low threading dislocation densities, especially the AlN nucleation layer. AlN on Si with high crystalline quality with (002) X-ray rocking curve (XRC) of less than 1000 arc sec and smooth surface was obtained by optimizing the AlN growth. With high quality buffer layer, thick GaN on Si was grown without relaxation of the compressive stress during growth. High resolution x-ray diffraction (HRXRD) was used to characterize the crystalline quality of the as-grown p-i-n structure on Si. The full width at half maximum (FWHM) of the X-ray omega rocking curves for (002) and (102) orientations were 235 arcsec and 307 arcsec, respectively. From the FWHM values we estimated a threading dislocation density (TDD) of $2.95 \times 10^8 \text{cm}^{-2}$ through empirical equations from [123]. A similar TDD of about $2 \times 10^8 \text{cm}^{-2}$ was obtained from cathodoluminescence (CL) microscopy of the GaN grown on Si as shown in Fig. 2.16a. In addition to TDD, impurity control such as carbon, silicon and oxygen is also critical. To achieve high breakdown voltage and low leakage current in GaN diodes, the background impurities, including both Si and O, have to be controlled to less than $1 \times 10^{16} \text{cm}^{-3}$. Large O or Si background concentrations, for example, in the range of $1 \times 10^{17} \text{cm}^{-3}$, require intentional carbon doping to compensate the shallow donors of Si or O in order to achieve high breakdown voltage. However, the presence of C may significantly degrade the electron mobility of Si-doped n-GaN. As it is shown in Fig. 2.16b, the non-optimized n-type GaN sample, which has a relatively high C concentration of $\sim 8 \times 10^{16} \text{cm}^{-3}$, presented an electron mobility of $\sim 200\ \text{cm}^2\text{Vs}^{-1}$ at a doping level of $1 \times 10^{17} \text{cm}^{-3}$. By tuning the growth parameters, the C concentration was reduced to less than $1 \times 10^{16} \text{cm}^{-3}$, leading to a much larger mobility of $720\ \text{cm}^2\text{Vs}^{-1}$ at a Si doping level of $2 \times 10^{16} \text{cm}^{-3}$. Furthermore, from SIMS measurements of our un-intentionally doped GaN samples, the Si or O background level was below $1 \times 10^{16} \text{cm}^{-3}$, and thus not requiring extra

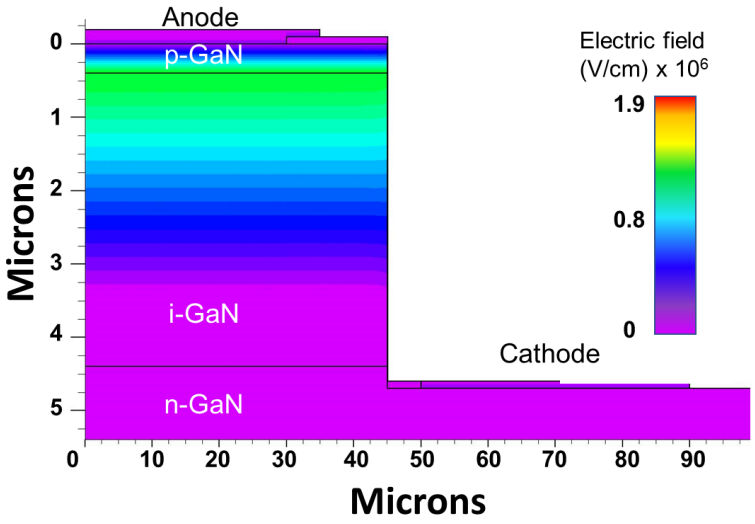


Figure 2.14 – Electric field distribution at a reverse bias of 200 V, revealing almost no localized peaking.

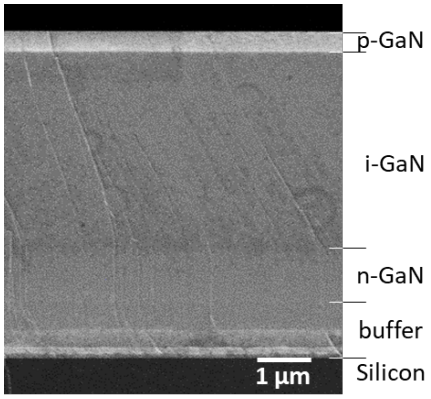
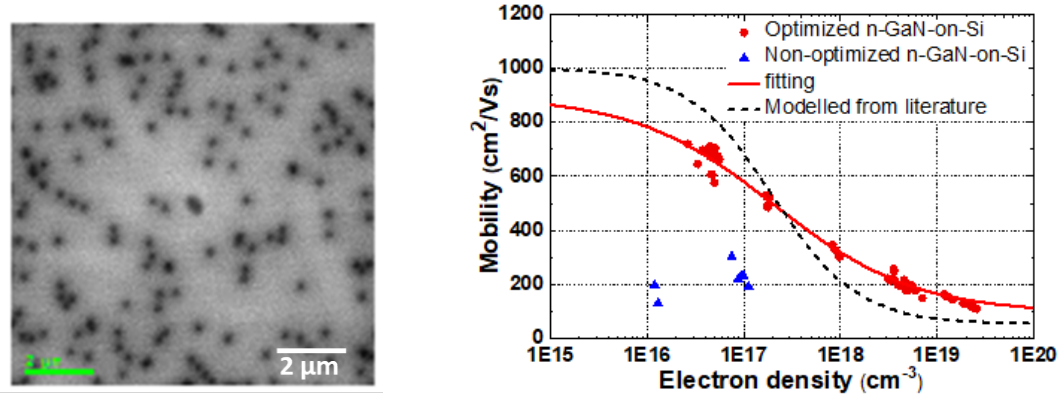


Figure 2.15 – Cross sectional scanning electron microscope (SEM) image of the GaN-on-Si wafer revealing clearly the different layers.

C doping. Fig. 2.16b shows the mobility of n-GaN/i-GaN/buffer/Si samples as a function of electron density obtained using an Accent HL5500 Hall system.

2.4.1 Optimization of fabrication steps

The main fabrication steps involved in the realization of a quasi-vertical p-i-n diode are as shown in the Fig. 2.17b. The fabrication process of the quasi-vertical diodes (Fig. 2.17a) started with the activation of p-GaN by thermal annealing in N_2 ambient at 750°C for 15 min. The p-electrode layer was formed by Ni (20 nm)/Au (50 nm) subsequently annealed at 480°C in N_2/O_2 ambient for 10 min for ohmic contact formation. This was followed by mesa isolation through a deep etching of GaN using inductively coupled plasma-reactive ion etching (ICP-RIE) to access the bottom n-GaN layer. The sample was then treated with 25% Tetra Methyl Ammonium Hydroxide



(a) (b)

Figure 2.16 – (a) Cathodoluminescence (CL) image of the as-grown GaN layer on Si. (b) Electron mobility versus electron density of the optimized and non-optimized n-GaN layers compared against the model from literature [124].

(TMAH) at 85°C for 1 hour to smoothen the sidewalls and heal the damages occurred during the deep-etching step. Cr (50 nm)/Au (250 nm) bi-layer was deposited for ohmic contact to n-GaN. The etched sidewalls were passivated with 100 nm-thick SiO_2, deposited by atomic layer deposition (ALD), and the field plates (FP) were formed with Ti (50 nm)/Au (300 nm) bi-layer. Since our lab was relatively new and I had no prior experience in the field of vertical power devices on GaN , a considerable amount of time was spent on optimization of most of the steps involved. A brief description of the same is provided below.

Ohmic contact to p-type GaN

Ohmic metal contact to p-GaN with low specific contact resistance is particularly challenging due to:

- Mg dopant species forms a stable complex with hydrogen during growth which can be dissociated only by low-energy electron beam irradiation (LEEBI) techniques or high temperature annealing with low activation efficiency < 1% [125–129].
- The Mg dopant species forms a deep acceptor level (~ 180 meV or higher) in GaN resulting in low hole concentration of $1 \times 10^{17} \sim 1 \times 10^{18}$ cm^{-3} [129].
- Absence of metals having work function larger than that of p-GaN (7.5 eV).

However, a lot of research has already been conducted to resolve this issue, boosted by the GaN LED technology and it is now possible to have ohmic contact to p type GaN with resistivity in the order of 10^{-4} Ω cm^2. After comprehensive literature review, it was decided to try the following three different metal stacks [130–132].

- Pd/Au – thickness of 20/100nm and 50/150nm annealed at 400-600°C in N_2 ambient for 1min

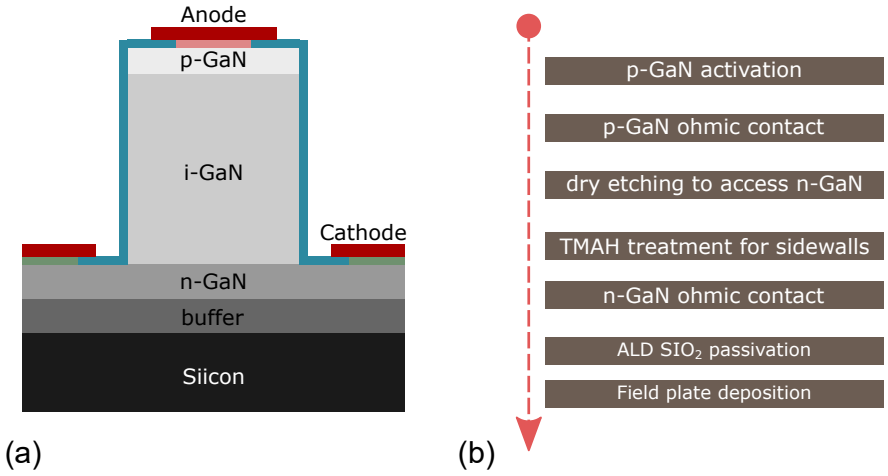


Figure 2.17 – (a) Schematic of a GaN quasi-vertical p-i-n diode and (b) fabrication process flow.

- Pd/Ni/Au - 10/20/30nm at various annealed at 400-600°C in N_2 ambient for 1min
- Ni/Au – 20/20nm annealed at 400-550°C in O_2 ambient for 10mins.

Transmission line method (TLM) was used to quantify the quality of the contacts. The wafer used was a standard p-i-n hetero structure grown on sapphire substrate in the Metal Organic Chemical Vapor Deposition (MOCVD) reactor at physics department, EPFL. The grown wafers were annealed at 750°C in N_2 ambient for 15 mins. This is for the activation of Mg dopants in the p type GaN. Standard photo lithography methods were adopted to pattern the wafer in EPFL clean room facility (CMi) and the different metal stacks were deposited using electron beam deposition tool present at the physics department clean room (IPHYS). After proper lift off process, the samples were annealed under different conditions. A LabVIEW program was created for simplifying the process for TLM and Hall measurements (for elucidating mobility, carrier concentration and other parameters). This program controls two Kiethley 2636 Semiconductor Measurement Units (SMUs). After successful characterization, it was observed that the Ni/Au contact gave a value of 3.94×10^{-4} Ω cm^2 for contact resistivity which is similar to that reported in literature ($\sim 1 \times 10^{-4}$ Ω cm^2). The other two combinations gave non-ohmic behavior in the spectrum of the annealing temperature that was tested. Even so, it was observed that this ohmic nature of the Ni/Au stack was not always reliable and gave non-ohmic behavior during some trials of p-i-n diode fabrication. Another variant of the Ni/Au metal stack involving a higher thickness of Au (50nm) was tested and this metal stack when annealed at 480°C provided a stable and low contact resistance of $\sim 1 \times 10^{-5}$ Ω cm^2. Fig. 2.18 shows the TLM data for the Ni (20nm)/Au (50nm) annealed metal stack on p-GaN exhibiting a very linear curve typical of an ohmic contact. Table 2.3 summarizes the optimization experiments undertaken to obtain ohmic contact to p-GaN.

The reason for low contact resistance with Ni/Au metal stack is attributed to the formation of p-type NiO by the oxidation of Ni [130]. The post-deposition annealing in $O_2 + N_2$ is believed to have converted the Ni to p-NiO and the Au to discontinuous islands on top of the p-GaN. p-NiO

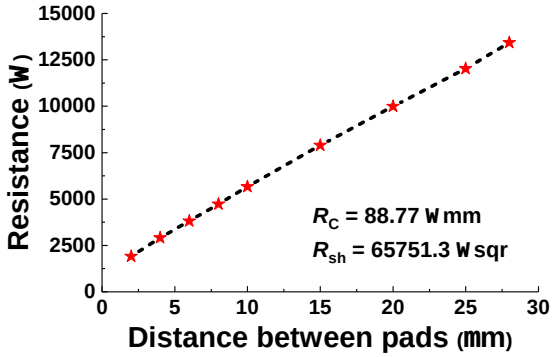


Figure 2.18 – TLM plot of Ni (20nm)/ Au (50nm) alloyed ohmic contact to p-GaN.

thin films by itself has been reported to be very resistive. However in this case, the Au islands dispersed in the p-NiO matrix enhance the conductivity of the p-NiO film. This p-NiO has a small barrier height of ~ 0.185 eV for holes which is easily surpassed by the application of voltage bias. The ohmic behavior seen in case of Pd/Au metal stack with no post-deposition annealing is ascribed to tunneling through Schottky barrier [131].

METAL	Annealing Temp (°C)	Annealing time (mins)	Contact resistance value (Ω cm^2)
Ni-20nm/Au-20nm	500°C in O_2	10	3.94× 10^{-4}
Pd-20nm/Au-100nm	400-600°C in N_2	1	too high
Pd-50nm/Au-150nm	400-600°C in N_2	1	too high
Pd-10nm/Ni-20/Au-30nm	400-600°C in N_2	1	too high
Ni-20nm/Au-50nm	480°C in O_2 + N_2	10	~ 1× 10^{-5}
Pd-50/Au-100nm	no annealing	-	~ 1× 10^{-2}

Table 2.3 – Summary of trialled ohmic metal schemes to p-GaN

Ohmic contact to n-type GaN

Ohmic contact to n doped GaN is quite easy to obtain as there are quite a few combinations of metals with work function near to or lower than the electron affinity of n doped GaN. The contact can be alloyed or non-alloyed. In an alloyed contact the different metals making the stack mix to varying proportions to form an alloy upon heat treatment. In non-alloyed, there is no annealing step and so there is no mixing of the metals. Both the types were studied. For the alloyed contact two different metal stacks were studied [133, 134].

- Ti/Al/Ni/Au - 15/220/40/50nm annealed at 900°C in N_2 ambient for 30s.
- Ti/Al/Ti/Al/Ti/Au – 30/30/30/30/30/60nm annealed at 830°C in N_2 ambient for 30s.

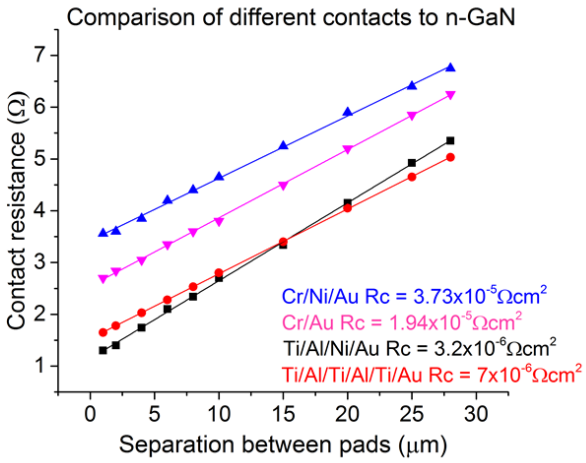


Figure 2.19 – Comparison of TLM data for contact to n-type GaN.

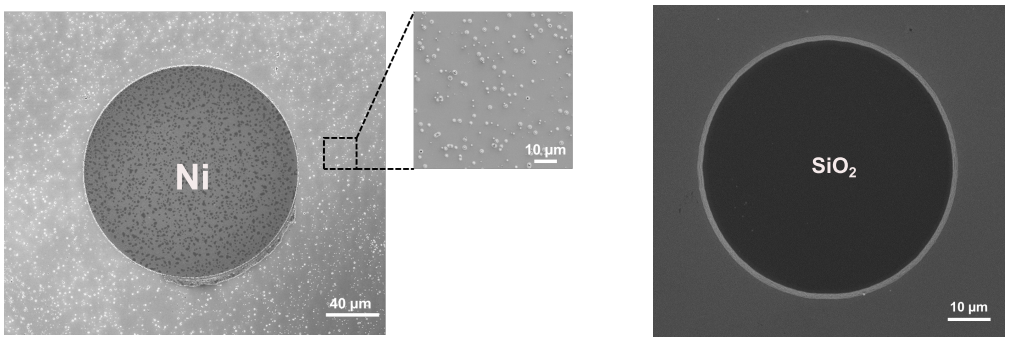
The same TLM method used for p contact optimization was adopted. The fabrication steps were similar. As observed from the Fig. 2.19, the Ti/Al/Ni/Au gave a contact resistivity of 3.2×10^{-6} Ω cm^2 which is better than the other metal stack. Often during the processing of vertical devices, it has been observed that having a non-alloyed contact for the n type GaN is preferable as this makes the fabrication process simpler. If we use an alloyed contact, it's imperative that the p contact can be made only after the annealing of the n contact as otherwise it would mean that the ohmic p contact will also be subjected to high temperature (~ 800-900°C) treatment required for the n contact. It has been observed that patterning the p contact after deep etching and n contact formation using thick photoresist often leads to bad alignment and focus issues. Thus non alloyed contacts were explored. Cr/Au and Cr/Ni/Au seemed to be the best candidates after much literature survey [135, 136]. TLM measurement revealed that Cr/Au gave a contact resistivity value of 1.9×10^{-5} Ω cm^2 and thus is better than Cr/Ni/Au. Fig. 2.19 shows the comparison of TLM data for various contacts. It is evident that Ti/Al/Ni/Au is the best alloyed contact and Cr/Au combination works well as a non-alloyed contact. The slight difference in the slope of the curves (depends on the sheet resistance of the semiconductor material, which in this case is the same n-GaN layer) is due to variations arising from fabrication process.

Deep etching of GaN

The fabrication of GaN vertical devices grown on hetero epitaxial substrates like sapphire and Si often requires deep etching of GaN to form contact to the n-GaN layer. As a result of the chemical inertness and the high bond strength of the nitrides, there is no wet etching chemistry available which etches GaN at an appreciable speed and uniformly in all crystal plane directions. The deep etching is often carried out using dry etching mechanisms like Reactive Ion Etching (RIE) or the Inductive Coupled Plasma RIE (ICPRIE). These work by the principle of generating

chemically reactive plasma with a RF powered magnetic field and using this plasma to etch the surface. Dry etching of GaN relies very much on the process conditions. An un-optimized etching process can result in surface morphologies that include pits and/or pillars. While the GaN etching process produces (volatile) chemical byproducts such as $GaCl_3$, the etching will not proceed without sufficient energetic ion bombardment due to the high bond strength of the material. Defects in the GaN appear to be particularly sensitive to etching conditions and respond by etching faster or slower than the surrounding material, ultimately forming pits or pillars. After elaborate literature review [137–139], it was understood that the gas chemistry which is most useful in deep etching of GaN is the Cl_2/Ar combination in the ratio of 1:3 to 1:4. Various other parameters which affect the etching are

- Type of hard mask used
- The chamber pressure
- The ICP power
- The gas ratio and total gas flow
- Chamber temperature



(a) (b)

Figure 2.20 – (a) Etching of GaN using Ni hard mask resulting in defects as shown in the inset. (b) Clean surface observed using a SiO_2 hard mask and adding BCl_3 to the gas mixture.

To study the etching process, a Nickel hard mask formed by lithography and subsequent wet etching was initially used. An ICP power of 200W, RF power of 100W and etch chemistry comprising of Cl_2/Ar was used. The etching time was 5 mins. A control sample containing blanket Nickel deposited on a dummy sapphire was used to assess the selectivity of the etching. A glass coverslip was used to cover one portion of the control sample so as to obtain a step profile after etching. The GaN sample was inspected under microscope. It was observed that the etched surface looked rough. The etch depth in GaN and Nickel control sample was obtained using a surface profiler. The etching rate of GaN was close to 140 nm/min and that of the Ni turned out to be approximately 20 nm/min giving a selectivity of 7:1. The etched surface of the GaN was further analyzed using Scanning Electron Microscope (SEM). The surface contained many micro pillars and pits similar to Fig. 2.20a. This might have happened due to incomplete wet

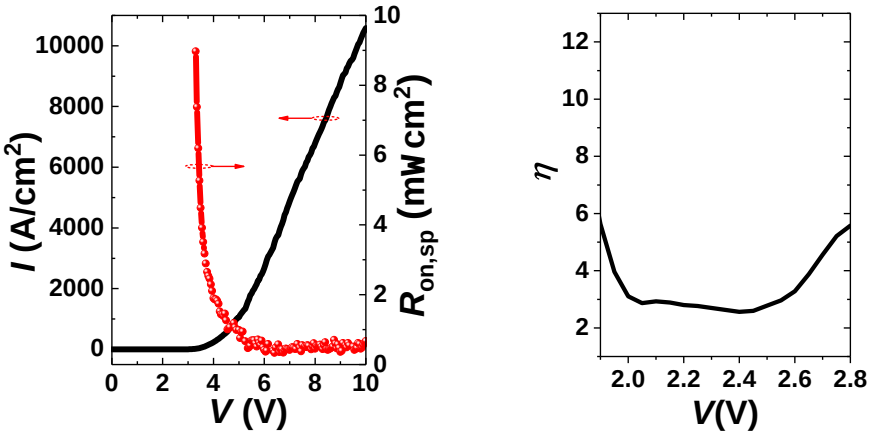
etching of Ni while defining the area of the GaN wafer to be etched. The unetched particles remaining on the surface could have formed micro hard masks which propagated down as the etching progressed. Subsequent trials were undertaken after carefully over etching the Ni region to be removed. The quality of the etched surface of the GaN did not improve. Next, we tried using SiO_2 as the hard mask. With the same chemistry, the surface still had the defect pillars after etching. After perusal of some relevant literature, it was understood that adding BCl_3 gas to the current chemistry could improve the etching [139]. The gas chemistry was modified keeping all other parameters the same. After etching for 5 mins, it was observed in SEM that the etched surface was very clean with little or no defects Fig. 2.20b. Adding the BCl_3 gas played the role in etching away any SiO_2 particles which were getting dispersed as a result of the etching process and thus surface of GaN was kept clean.

2.4.2 Electrical characteristics

ON-state behavior

Fig. 2.21a shows the forward current density versus voltage (I - V) characteristics and the $R_{on,sp}$ of p-i-n diodes with passivation and FP. We observed no difference in the forward characteristics between the passivated and the un-passivated devices. The diode anode diameter was 56 µm. The turn-on voltage ($V_{turn\ on}$), extracted at a current density of 20 A/cm^2 was 3.3 V which is close to the bandgap of GaN. The $R_{on,sp}$ extracted from the forward I - V plot at 6.4 V was 0.33 mΩ cm^2, while the equivalent on-resistance calculated by voltage over current at 6.4 V was 1.56 mΩ cm^2. For quasi-vertical diodes, the on-resistance is mainly determined by the current crowding in the n-GaN layer towards the n-GaN contact [140], which was significantly alleviated in these devices due to the highly-doped 1 µm-thick n-GaN layer presenting a low sheet resistance of 26 Ωcm. For larger anode contacts, we observed an increase in $R_{on,sp}$ since the higher current leads to a much more severe current crowding at the n-GaN layer. Current crowding can be further reduced by modifying the device structure from a quasi- to a fully-vertical structure, by substrate removal for instance [121]. Another main contribution to the $R_{on,sp}$ comes from the thick drift layer, which was minimized in our devices by optimizing the electron mobility and doping of the GaN drift layer. This resulted in a much smaller $R_{on,sp}$ than in previous reports of GaN-on-Si p-i-n diodes, even compared to fully vertical structures [121] and to devices with larger doping in n-GaN layers [119].

Our diodes presented a very high current density (normalized by the anode surface), larger than 10 kA/cm^2 at 10 V, which to our knowledge is the highest value reported for GaN diodes grown on foreign substrates [119, 121, 141–145]. Despite the thick GaN layers grown on Si, a small ideality factor of 2.56 was extracted at a forward voltage of 2.4 V, reflecting the excellent quality of the epitaxial layers (Fig. 2.21b). Fig. 2.22 shows the temperature dependence of the forward I - VV characteristics. As expected, the turn-on voltage decreased at higher temperatures due to bandgap narrowing and thermally-enhanced carrier diffusion. We observed very little change in $R_{on,sp}$ and drift in the current density with temperature, as opposed to degradation or inconsistencies observed in previously reported papers [119, 121]. These excellent results are comparable to fully vertical diodes fabricated on GaN substrates [62, 146].



(a) (b)

Figure 2.21 – (a) Forward I - V and specific on-resistance measurement. (b) Ideality factor (η) of the p-i-n diode.

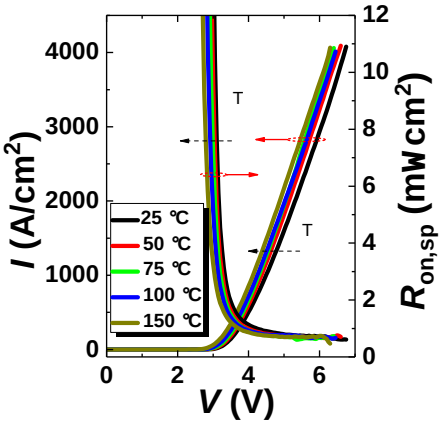
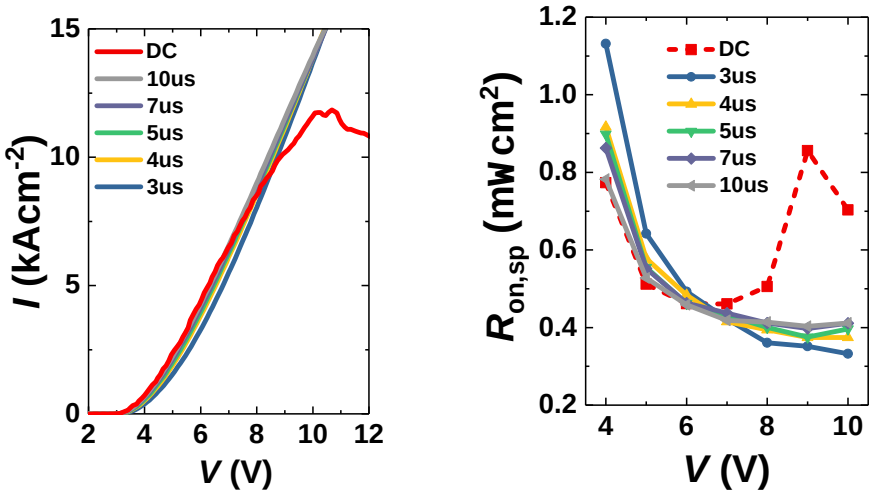


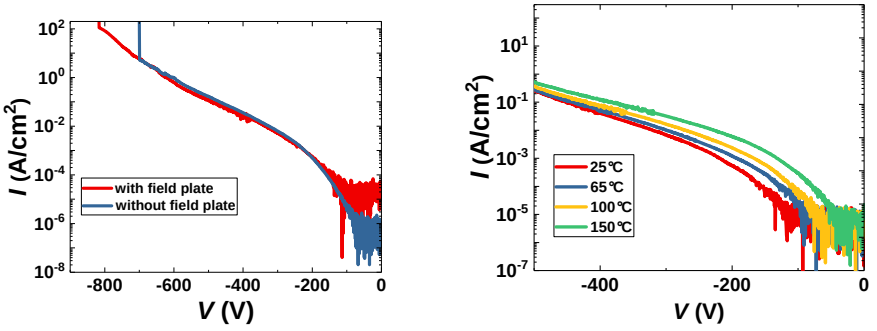
Figure 2.22 – Forward I - V and specific on-resistance measurement at various temperatures.

The pulsed ON-state performance was also analysed with the help of AMCAD pulse IV system. In DC conditions, the p-i-n diode $R_{on,sp}$ degrades after about 7 V due to series resistance and self heating issues (Fig. 2.23a and Fig 2.23b). This behavior was observed for a large number ($>$ 20) and re-measurement of these devices revealed a broken device with a short circuit characteristics. The pulse width was varied from 3µs to 10µs. The I - V characteristics shows two different regions as shown in Fig. For anode voltages in the range 2.5-10 V, the current density decreases progressing from 10µs to 3µs pulse width. The larger pulse width signals generate more heat in the devices and thus the current increases due to bandgap narrowing similar to the DC measurement. For voltages $>$ 10 V, the effects of self heating become prominent with current density decreasing with increasing the pulse width.



(a) (b)

Figure 2.23 – (a) DC and pulsed measurements (with different pulse widths) of forward characteristics and (b) variation of on-resistance with voltage for the different types of measurements.



(a) (b)

Figure 2.24 – (a) Reverse *I*-*V* measurement of the best performing devices. (b) Reverse *I*-*V* measurement at various temperatures.

OFF-state behavior

Fig. 2.24a shows the reverse current density versus voltage (*I* - *V*) curve of the diode in logarithmic scale, performed on an insulating chuck. The *BV* of the diode without field plate (FP) was 700 V, which was significantly improved to 820 V by the 5µm-long FP, corresponding to an average electric field in the drift layer of 2.1 MV/cm. To the best of our knowledge, this is among the best *BV* among all previously reported quasi/fully-vertical GaN-on-Si p-i-n diodes. This enhancement was confirmed by 2D-TCAD simulations as shown in Fig 2.25. For a non-terminated anode, the electric field at a reverse bias of 690 V peaks at the edge of the electrode to about 2.8 MV/cm. The field plate spreads the electric field in two peaks at the edge of the anode and of the FP, resulting in an electric field peak of ~ 2.7 MV/cm at a much higher voltage of 823 V. The measured leakage current density was $\sim 5 \times 10^{-3}$ A/cm^2 and $\sim 4 \times 10^{-2}$

A/cm^2 at -300 V and -500 V, respectively. Such low reverse leakage current can be attributed to the high crystalline quality of the GaN epi layers grown on Si substrate, since it is dominated by space charge limited current (SCLC), mainly due to traps in the thick epi-layers [141, 147]. According to the model from [147], the epitaxial GaN grown on Si contains both acceptor- as well as donor- type traps. At low reverse voltages, the acceptor traps start getting filled with electrons. As the reverse voltage increases, the Fermi level moves up towards the conduction band and the ionized donor traps start getting filled. At the point where all the trap states get filled, denoting the onset of the trap filled voltage, the current increases sharply as the Fermi level reaches the conduction band. The leakage current in log-scale, prior to the trap filled voltage, is proportional to V^n. A value of n ~ 6.39 was obtained by fitting the Fig. 2.24a, which is comparable to previous reports of p-i-n diodes on GaN-on-Si [121, 141]. We have not observed a significant difference in leakage current with and without passivation, which we believe is due to the effective healing of the etching damages on the sidewalls by the TMAH treatment [148]. Fig. 2.24b shows the reverse I - V characteristics of the diodes at different temperatures, revealing a slight increase in leakage current with temperature due to thermal carrier generation.

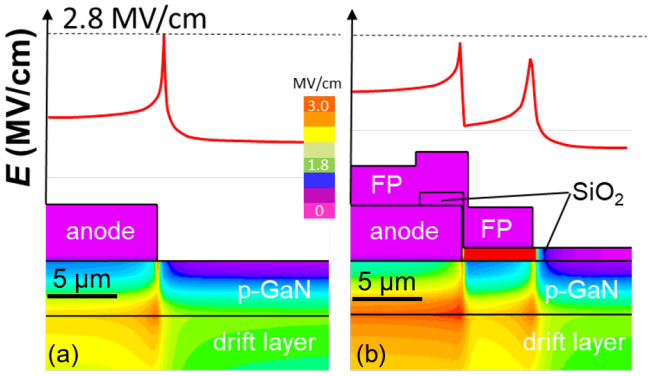
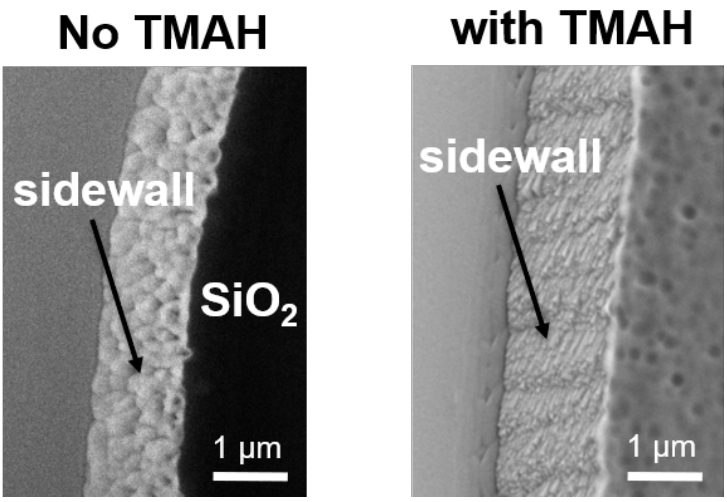


Figure 2.25 – Simulated electric field in a non-terminated (at 690 V) and terminated diode (at 823 V).

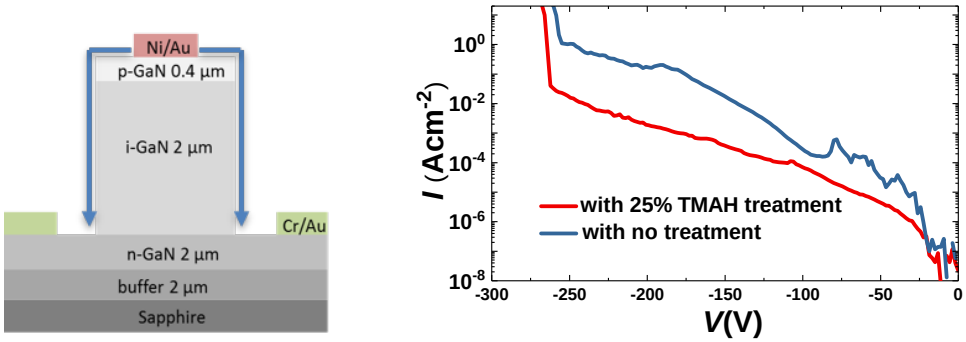
We also studied the effect of tetra methyl ammonium hydroxide (TMAH) treatment on the dry etched mesa sidewalls, on the reverse leakage current. The TMAH etches GaN in all planes except for c-plane (0001) and m-plane ($1\bar{1}00$). Pottasium hydoxide (KOH), on the other hand doesnt etch GaN in the c-plane (0001) and a-plane ($11\bar{2}0$). The inclusion of TMAH treatment before the sidewall passivation was found to improve the leakage current by almost two orders on a test p-i-n diode fabricated on GaN-on-Sapphire substrates (Fig. 2.27a and Fig. 2.27b). The Fig. 2.27b is representative of majority of the devices measured for this comparison. The mesa sidewall surface after dry etching is very uneven and damaged from the bombardment of the ions (Fig. 2.26a).

The TMAH treatment for 1 hr etched this sidewall and the resulting surface comprises of miniature m-planes as is evident from the Fig. 2.26b (SiO_2 hard mask was removed after TMAH treatment, before SEM). This process is believed to have removed all the defective GaN layers on the surface



(a) (b)

Figure 2.26 – (a) Tilted view SEM of the etched sidewall of a p-i-n diode before TMAH treatment and (b) after treatment, revealing miniature m-plane facets.



(a) (b)

Figure 2.27 – (a) Schematic showing the p-i-n diode structure and leakage path through etched sidewall. (b) Comparison of reverse I-V measurement with and without TMAH treatment.

from the dry etching process and thus improved the leakage current.

We also trialled different dielectric materials to use as passivation layer and understand their effect on the leakage current. The layers were 100 nm atomic layer deposited (ALD) SiO_2, 100 nm ALD Al_2O_3, 100 nm plasma enhanced chemical vapor deposited (PECVD) SiO_2 and 200 nm PECVD Si_3N_4. Proper cleaning of samples using acetone, iso propyl alcohol (IPA) and oxygen plasma treatment was done prior to loading the samples into the ALD/PECVD chamber. Before doing the deposition, the chamber was cleaned and conditioned by performing several dummy deposition runs followed by purging of the gas lines. As observed from Fig. 2.28, the diodes with different passivation layers exhibited almost identical leakage current levels till the reverse-voltage they broke. The p-i-n diodes with ALD SiO_2 consistently provided higher BV

than others. This is due to the higher quality of the ALD SiO_2. The ALD Al_2O_3 passivated samples had a slightly lower BV than those with ALD SiO_2. This could be from the higher dielectric breakdown strength of SiO_2 protecting the FP edge from breaking through the dielectric. In general, the quality of ALD deposition is better than PECVD and this was observed in the case of PECVD SiO_2 and PECVD Si_3N_4 passivated samples which had a lower BV than those using ALD dielectric passivation.

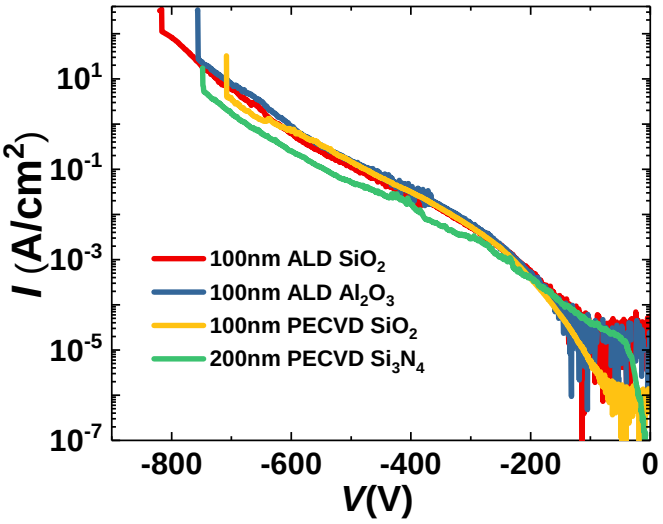


Figure 2.28 – Comparison of reverse leakage current of diodes using different passivation dielectrics.

2.4.3 Near-junction heat spreaders for hot spot thermal management of p-i-n diodes

The increasing power density of high power electronic and optoelectronic devices, radio frequency (RF) devices, and power ICs leads to large heat fluxes in the active region of the devices. The hot spot heat flux has to be conducted through several thermal resistances such as the bulk substrate material, thermal boundary resistances (TBRs), packaging, and thermal interfacial materials (TIMs) before being extracted from the chip [149]. High power devices can reach power densities, as high as 50 W/mm in GaN devices [150, 151], that can result in extremely large heat fluxes, as high as 300 kW/cm2.The generated heat can be very confined in some cases (e.g., at drain side of the gate in GaN high-electron-mobility transistors) [152]; thus, the heat flux faces thermal spreading resistances before being extracted from the chip, which limits the cooling of the device [153]. In the case of GaN, as the device power density increases, its thermal conductivity [154] becomes insufficient to handle the hot spots and provide enough heat spreading, leading to large peak temperature rises. This problem is more troublesome for emerging oxide electronic devices. Ga2O3 has a large Baliga Figure of Merit (almost four times that of GaN) and, therefore, is very promising for future high power density devices [155]. However, its extremely poor thermal conductivity (ten times lower than GaN) results in limited thermal conduction and heat spreading [156]. As a result, the large thermal resistances of Ga2O3 devices [157, 158] impose a severe

limit on the device power density and, without proper thermal management, would strongly affect their performance, reliability, and lifetime.

To address the localized heat fluxes and limited heat spreading, it is common to use high thermal conductivity substrates, such as SiC and diamond, which results in enhanced thermal and electrical performances [159–161]. Nonetheless, the potential advantages of such technologies should be considered together with the issues of the limited available size of these substrates, coefficient of thermal expansion mismatch for heteroepitaxy, and high system-level cost [30, 162]. In addition, a larger impact on heat spreading requires the use of high thermal conductivity materials as close as possible to the hot spots to spread the heat away from the heat source to larger areas on the chip [163], which is the basis for the concept of near-junction heat spreaders. In this experiment we experimentally evaluated the performance of Cu near-junction heat spreaders on GaN-on-Si vertical p-i-n diodes. The details mentioned here are from our paper [2]

Device fabrication and Results The p-i-n diodes used in this study have an anode radius (r_A) of 10 μm and presented a large breakdown voltage of 820 V (similar to mentioned in section 2.4.2) and low specific on-resistance of 0.25 mΩ cm^2, along with a large current density of 15 kA/cm^2. To provide electrical isolation between the device and the Cu heat spreaders, a 2 μm-thick SiO_2 layer was deposited at 300 °C using plasma-enhanced chemical vapor deposition (PECVD) and then patterned by dry etching to access the anode and cathode electrodes. Finally, a 6.5 μm-thick layer of Cu was electroplated and patterned on top of the devices. The scanning electron microscope (SEM) top and cross-sectional view images of a p-i-n diode with Cu heat spreader are shown in Figs. 2.29a and b . Thermal measurements were performed using a Quantum Focus Instrument (QFI) IR microscope with a 512-by-512-pixel array of cooled IR detectors, which with a 20× magnification lens and filters provided a high special resolution and accuracy. The IR microscope was equipped with a precise thermal stage, which enabled an accurate emissivity correction using the two-temperature emissivity calculation method as well as the factory-provided calibration data. In addition, to increase the emissivity of the chips and to avoid errors due to the IR transparency of the layers, black paint was used on top of the chips. For all of the measurement points in this work, accurate pixel-by-pixel emissivity calibrations were performed to ensure valid measurements.

The temperature at the top surface of the devices were measured at different biases. Since the heat source in the p-i-n diode is located below the heat spreader, the maximum temperature measured at the top surface of the heat spreader is not representative of the maximum device temperature because of a temperature drop in the thickness of the heat spreader. To estimate the maximum device temperature in the fabricated devices, the temperature profile was simulated using COMSOL, and the surface temperature in the model was matched with the experimental measurements. The thermal model of the devices is depicted in Fig. 2.29c, in which a volumetric heat source is located at the i-GaN layer in the structure to represent the joule heating in the

[2] R. Soleimanzadeh, R. A. Khadar, M. Naamoun, R. van Erp, and E. Matioli, "Near-junction heat spreaders for hot spot thermal management of high power density electronic devices," Journal of Applied Physics, vol. 126, no. 16, p. 165113, Oct. 2019, publisher: American Institute of Physics. Contribution: Second author, assisted with the design, fabrication and electrical measurements.

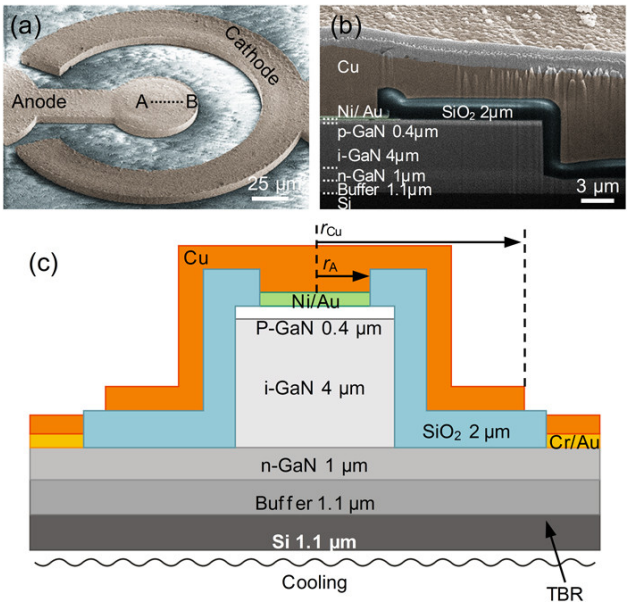


Figure 2.29 – (a) SEM image of a GaN vertical PiN diode with a Cu heat spreader. (b) Cross-sectional image of the device across AB indicated in (a). (c) Schematic of the device structure simulated in COMSOL.

device, and the device is cooled at the bottom by convective cooling. Thermal boundary resistance (TBR) of 70 m^2K/GW were set between GaN and Si, and 20 m^2K/GW between diamond and GaN. The natural convection of air at the surface was neglected due to the small surface area of the device; therefore, all other boundary conditions were considered adiabatic. The SEM and thermal microscope images of two diodes with an anode radius of 10 μm and heat spreaders of 15 μm and 60 μm are shown in Figs. 2.30a and b, respectively, which were measured at a dissipation power of 0.9 W, corresponding to a very large heat flux of 102 kW/cm^2 (normalized by the surface area of the i-GaN layer under the anode).

Such large heat flux caused a high hot spot temperature rise of about 180 °C and high temperature gradients near the edge of the heat source for the device with a small heat spreader, as shown in Fig. 2.30a. The use of a 60 μm heat spreader resulted in a reduction of 73 °C in the maximum temperature, and much smaller thermal gradients in the device footprint, as shown in Fig. 2.30b. Fig. 2.30c shows an excellent agreement between the thermal resistances measured from the maximum surface temperatures on the fabricated devices (symbols) and the COMSOL simulations (dashed lines). However, the device thermal resistance (solid lines), calculated from the maximum device temperatures in the i-GaN layer, are slightly higher due to a temperature drop in the heat spreader along with its thickness. By using 60 μm-radius Cu heat spreaders, a significant drop in the thermal resistance was observed [Fig. 2.30c], which resulted in a reduction of 2.3×, 1.7×, 1.4×, and 1.37× on the total thermal resistance for the devices with anode radii of 5, 10, 20, and 30 μm, respectively.

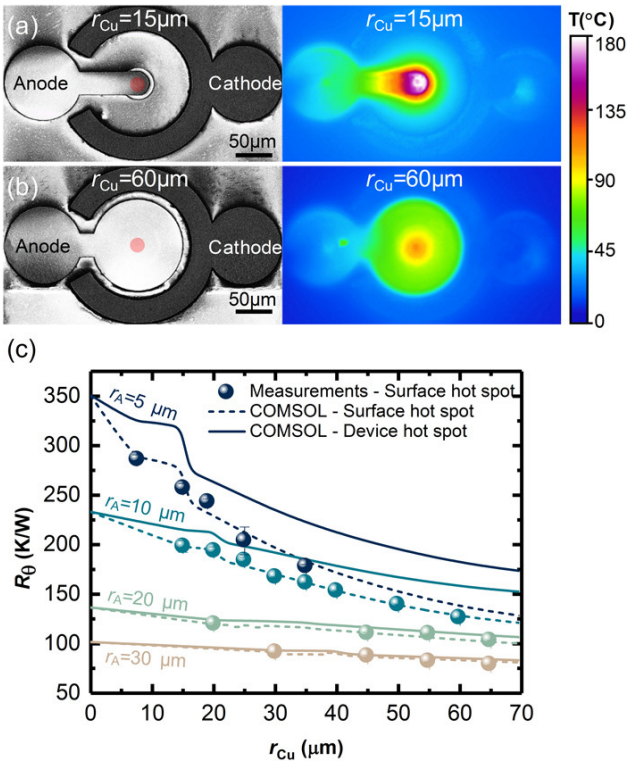


Figure 2.30 – (a) SEM and IR microscope image of the device with an anode radius of 10 μm and heat spreader radii of 15 μm and (b) 60 μm, both operated at 0.9 W, respectively. (c) Total thermal resistance (R_θ) as a function of Cu heat spreader radius (rCu) at different anode radii (rA). Dashed lines are from COMSOL simulations matching the experimental points (symbols), based on the hot spot temperature at the top surface, and solid lines are the device thermal resistance calculated from the maximum device temperature from COMSOL simulations.

2.5 Conclusion

In this chapter, we first reported on the simulation and the fabrication techniques which were developed as the first goal of my Ph.D.

Based on this learning, we demonstrated a high performance quasi-vertical GaN-on-Si p-i-n diode with record performance, achieved with a 4 μm-thick drift layer. The growth and doping of the GaN drift layer were optimized, leading to a remarkable electron mobility of 720 cm^2/Vs for a doping level of 2× 10^{16} cm^{-3}. A low $R_{on,sp}$ of 0.33 mΩ cm^2, high forward current density of 10 kA/cm^2 at 10 V, and a record breakdown voltage of 820 V were achieved. As a result, our diodes presented a BFOM of 2.0 GW/cm^2, which is the best achieved on GaN-on–Si diodes. The benchmarking of our p-i-n diodes as compared to other p-i-n diodes on bulk GaN, Si and sappire substrates us as shown in Fig. 2.31. We also investigated the heat generation in these p-i-n diodes under forward bias conditions and devised a novel method for distributing the heat from the hot spots, thus improving the reliability.

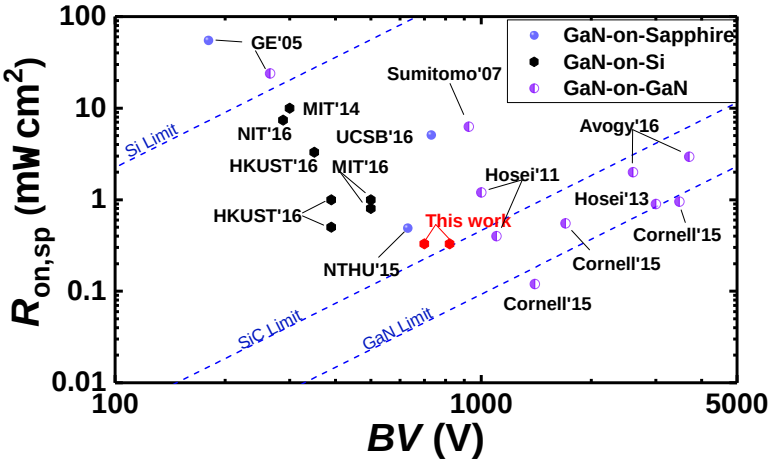


Figure 2.31 – Benchmarking of our GaN-on-Si diodes against other reported bipolar p-i-n diodes in literature using *R*on,sp and *BV* as parameters.

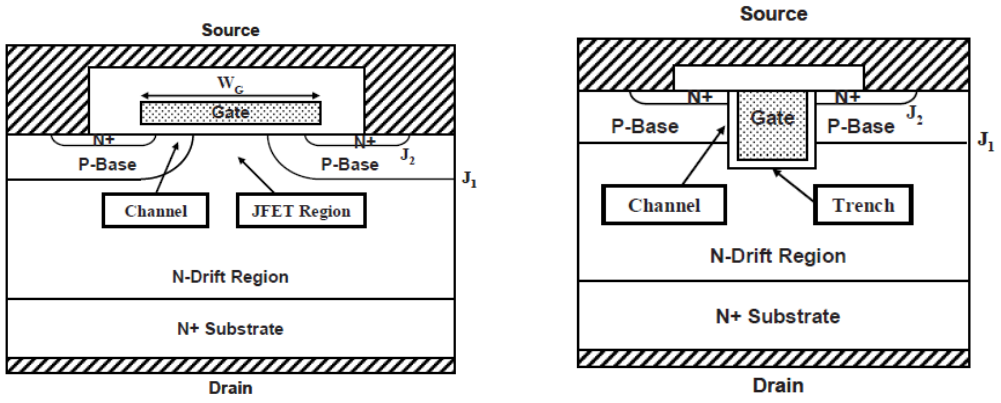
These results demonstrate the enormous potential of GaN-on-Si diodes for low-cost high-voltage power devices.

3 GaN-on-Si power MOSFETs

A power MOSFET is the one of the most common active device used in electrical circuits employed for high-voltage/high-current switching applications. In this chapter, we will discuss about the theory,fabrication, simulation and electrical performance of power MOSFETs fabricated on GaN-on-Si. A quasi-vertical device design is the most obvious choice for power MOSFETs fabricated on GaN layers grown on Si/SiC/sapphire substrates. As such, a quasi-vertical MOSFET is first presented. In order to alleviate the issues associated with current crowding in a quasi-vertical design, a novel and robust method for making a fully-vertical power MOSFET was developed and the fabricated device was characterized. Some important optimization steps involved with improving the gate channel conductivity are also included. Finally, we conclude the chapter with a small summary and discussion on how to improve the performance even further. Most of the results are from our paper [120, 164].

3.1 Introduction

Power MOSFETs were introduced in mid 1970s as a replacement for bipolar junction transistors (BJTs) which suffered from low current-gain when developed for high reverse breakdown voltage, and inability to be used at high frequencies due to the large storage time of the injected carriers in the drift region of the device [6]. In addition, the metal oxide semiconductor (MOS) gate structure of the power MOSFET simplified gate-drive circuits due to their inherently large input impedance and provided superior switching speed in the range of 10-50 kHz. The power MOSFETs also provide lower switching losses, lower ON-resistances and are less susceptible to thermal runaway as compared to BJTs [6]. As a result, power MOSFETs are the most widely used power device in the world and are used for a range of applications like switching power supplies, RF power amplifiers, automotive and communication systems. The first commercial power MOSFET was the vertically diffused (VD) MOSFET on Silicon containing two diffused regions on the drift layer as shown in Fig 3.1a. The channel region was formed by controlling the doping, depth and width of the diffused regions. However, these MOSFETs suffered from parasitic junction field effect transistor (JFET) elements which impaired the total on-resistance. Hence, with improvements made in the etching of Si, trench MOSFET/U-MOSFET was developed which eliminated these JFET regions and provided improved on-resistance values as well as higher switching speeds



(a) (b)

Figure 3.1 – (a) Schematic of a VD MOSFET [6]. (b) U MOSFET structure [6].

close to 1 MHz. The basic operating principle of a trench MOSFET is as follows. Fig. 3.1b shows the schematic of a trench MOSFET, in this case a GaN-trench MOSFET. As displayed, the device structure is made up of 4 distinct GaN layers. The bottom high doped n-GaN layer acts as a current collection layer, especially for a quasi-vertical device as will be explained in next section. The drift layer (i-GaN) layer is the voltage blocking layer as in the case of p-i-n diodes in Chapter 2, and the thickness of this layer normally determines the maximum BV attainable by the device. The p-GaN layer has two functions: 1) It forms the channel region. 2) It forms a p-n junction with the i-GaN layer which prevents current conduction and blocks voltage when the gate voltage is below the threshold voltage (V_{th}). The p-GaN layer doping is normally much higher than the doping of the i-GaN layer and so the depletion region during OFF-state operation ($V_{\text{DS}} >> 0$ V, $V_{\text{GS}} = 0$ V) extends primarily into the i-GaN layer. The top highly doped n-GaN layer acts as the source contact layer. It is important to notice that such a structure results in an enhancement mode MOSFET. When a positive gate bias is applied above the (V_{th}), an inversion layer is formed in the p-GaN layer adjacent to the gate terminal. The (V_{th}) in this case depends on the gate oxide material properties, thickness, the work function of the gate metal used, and on the doping of the p-GaN layer as expressed by the equation:

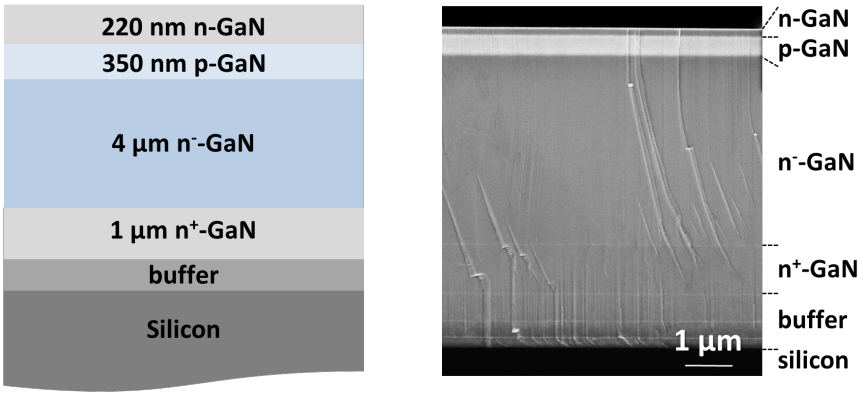
$$V_{\text{th}} = V_{\text{FB}} + 2\phi_{\text{B}} + \frac{\sqrt{2\epsilon_{\text{s}} q N_{\text{A}} \left(2\phi_{\text{F}} + V_{\text{SB}}\right)}}{C_{\text{ox}}} \tag{3.1}$$

where V_{FB} is the flat band voltage (which depends on the gate metal work function), ϕ_{B} is the bulk potential (which depends on the p-GaN doping), V_{SB} is the substrate bias and C_{ox} is the gate oxide capacitance (which depends on the material and thickness of the gate oxide). When a voltage $V > V_{\text{th}}$ is applied to the gate terminal (V_{GS}) and a positive drain to source voltage (V_{DS}) is applied, the MOSFET starts to conduct through the inversion channel. The current through the channel increases with V_{GS}. The OFF-state performance is measured by setting $V_{\text{GS}} = 0$V and then increasing the V_{DS} to the point till breakdown happens. For MOSFETs with no special

termination structures like field plate (FP) on the source terminal and gate protection structures [95, 165] , the breakdown mostly happens due to high electric field at the gate trench bottom which ruptures the gate oxide. The gate leakage current becomes very high after that and the device fails due to hard breakdown. In the case of GaN, the most obvious choice of device structure is the trench MOSFET [58, 84–87]. This is further supported by the fact that selective doping in GaN by diffusion and ion implantation is at an incipient stage and not suitable in the current state. There are many reports of GaN vertical MOSFETs on bulk-GaN substrates employing different designs like trench MOSFETs, current aperture vertical electron transistor (CAVET), Oxide-GaN interlayer FET (OGFET) etc. exhibiting high-performance device behavior. However all these reports are of devices grown on bulk GaN substrate which is available only in small wafer sizes and is still prohibitively expensive as compared to Si substrates. Thus, for the future adoption and commercialization of GaN vertical power devices, it is desirable to develop such devices in low-cost large-area substrates, such as Si.

3.2 Quasi-vertical GaN-on-Si power MOSFETs

GaN-on-Si technology has been developed extensively for several different areas, such as high-brightness light emitting diodes [166], high-power lateral HEMTs [26, 50, 167] and high-power vertical diodes [119, 121, 142, 168, 169]. However, there have been no reports up-to-date on GaN-on-Si vertical transistors, due to the challenge in obtaining high-quality n-p-i-n GaN heterostructures on silicon substrates. On one hand, the doping profile needs to be carefully engineered for abrupt heterojunctions; and on the other hand, a thick and continuous GaN drift layer with high electron mobility and low defect density is highly desired for low on-resistance and large breakdown voltage. This is especially challenging on silicon substrates considering the large mismatch between GaN and Si, both in lattice constant and thermal expansion coefficient. In this work, we demonstrate the first GaN-on-Si vertical transistors fabricated on a 6.7 µm-thick n-p-i-n heterostructure grown on 6-inch silicon substrates. The heterostructure contained a 4



(a) (b)

Figure 3.2 – Cross-sectional (a) schematic, and (b) SEM image of the as-grown np-n heterostructure on 6-inch silicon substrates.

μm-thick GaN drift layer, with a Si dopant concentration of 2×10^{16}cm^{-3}. With an optimized buffer and doping profile, the lateral electron mobility in the drift layer was as high as 720 cm^2/Vs as mentioned in Chapter 2. The fabricated vertical trench MOSFETs exhibited enhancement-mode (E-mode) operation with a threshold voltage (V_{th}) of 6.3 V and an on/off ratio of over 10^8. A specific on-resistance of 15.3 mΩ cm^2 and a high off-state breakdown voltage of 645 V were achieved. This excellent performance shows the great potential of GaN-on-Si to serve as a platform for future power electronic applications. The details mentioned in this section are based on our paper [1].

3.2.1 Growth of n-p-i-n structure

Fig.3.2a shows the cross-sectional schematic and Fig. 3.2b presents scanning electron microscopy (SEM) image of the n-p-i-n heterostructure used in this work grown on 6-inch Si (111) substrates by metal organic chemical vapor deposition (MOCVD). From bottom to top, the n-p-i-n structure consisted of a 1.1 μm-thick buffer layer, a 1 μm-thick n-GaN layer (Si: $\sim 1 \times 10^{19}$cm^{-3}), a 4 μm-thick unintentionally n-type doped i-GaN layer (Si: $\sim 2 \times 10^{16}$cm^{-3}), a 350 nm-thick p-GaN layer (Mg: $\sim 4 \times 10^{19}$cm^{-3}), a 200 nm-thick n-GaN layer (Si: $\sim 5 \times 10^{18}$cm^{-3}), and a 20 nm-thick n-GaN layer (Si: $\sim 1 \times 10^{19}$cm^{-3}). The x-ray diffraction (XRD) omega-rocking curves showed a small full width at half-maximum (FWHM) value of 235 arcsec and 307 arcsec near the GaN (002) and (102) reflections, respectively. As mentioned previously in section 3.1, the p-GaN layer forms the gate region and the thickness and the doping of the p-GaN layer has profound impact on the ON- and OFF-state behavior of the MOSFET. On one hand the doping and the thickness of this layer should be sufficient for blocking the reverse voltage applied during the OFF-state operation without occurrence of punch-through and on the other hand, the doping and the thickness of this layer should not be that large that it results in too high a V_{th} according to Eq. 3.1 and a high $R_{\text{on,sp}}$ due to increased scattering from the Mg dopant atoms in the p-GaN channel. Thus a careful balance is very essential for extracting the best device performance. This optimization was conducted using TCAD simulations prior to designing the n-p-i-n heterostructure for growth. The top n-GaN layer with a thickness of 200 nm is mainly for a good ohmic contact to the source terminal. This layer also creates a connection to the inversion channel electrons at the onset of the MOSFET turn-on, thus completing the current flow path from the drain to the source. For the growth of thick, continuous GaN on Si with low threading dislocation density, high quality buffer layers are important, especially the AlN nucleation layer. AlN buffer on Si with high crystalline quality (FWHM (002) < 1000 arcsec) and smooth surface was obtained by optimizing the AlN growth technology. With the high-quality AlN buffer layers, thick GaN on Si was grown without relaxation of the compressive stress during growth, which is important for compensating the tensile stress during cooling down. The value for wafer bowing after growth was X∼-57 μm, Y∼-45 μm. The lateral mobility of the n-type GaN drift layer was 720 cm^2 /Vs for a Si dopant concentration of 2×10^{16}cm^{-3}, measured with a Hall system on n-GaN/i-GaN/buffer/Si structure.

[1] C. Liu, R. A. Khadar, and E. Matioli, "GaN-on-Si Quasi-Vertical Power MOSFETs," IEEE Electron Device Letters, vol. 39, no. 1, pp. 71–74, Jan. 2018. Contribution: Second author, Development of TMAH wet etch process, ohmic contacts, gate-trench etch optimization, simulation and electrical measurements

3.2.2 Fabrication process

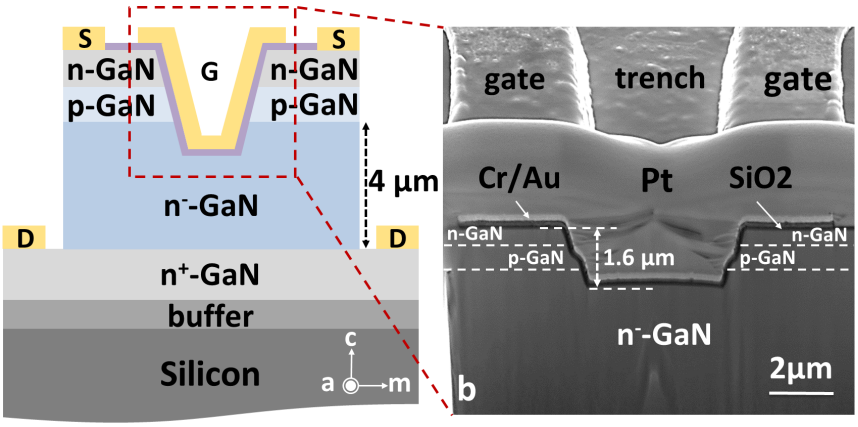


Figure 3.3 – Cross-sectional schematic, and SEM image of the fabricated quasi-vertical trench gate MOSFETs on Si substrate.

Fig. 3.3 depicts a cross-sectional schematic of the fabricated quasi-vertical trench gate MOSFET, in which the gate trench is aligned along the a-axis.The device process starts with deposition of 500 nm of SiO_2 by PECVD followed by patterning the SiO_2 by photolithography. The patterned SiO_2 is then etched using reactive ion etching (RIE) using CHF_3/Ar chemistry to expose GaN in the gate trench region. After stripping the photoresist using O_2 plasma, the GaN is etched using a inductive coupled plasma reactive ion etching (ICPRIE) employing a Cl_2/BCl_3/Ar recipe to a depth of 1.6 µm. The sample was then treated with 5% tetra methyl ammonium hydroxide (TMAH) solution at 85 °C for 60 minutes. The TMAH wet etch was found to be effective in removing the damages from the dry-etched GaN sidewalls. To activate the buried p-type GaN, a rapid thermal annealing (RTA) was performed at 850°C for 20 minutes in a N_2 ambient. Subsequently, a 100 nm-thick SiO_2 gate dielectric for the vertical MOSFETs was deposited on the top surface and trenches by atomic layer deposition (ALD). After opening contact holes on the SiO_2 by reactive ion etching (RIE) to access the top n-GaN layer, a double-layer metal stack of Cr/Au was evaporated to form both the source and gate electrodes for the vertical MOSFETs. Finally, a 5 µm-deep etching was performed using a Cl_2/BCl_3/Ar- based ICPRIE etch, followed by the evaporation of Cr/Au drain electrodes. The depth of the trench should be such that it overlaps the p-GaN region. Else, the device wont turn on at V_{DS} = 0 V even though a $V_{GS} > V_{th}$ has been applied and thus results in a turn-on voltage typically around 3.0-3.4 V. From the point of view of $R_{on,sp}$, any trench depth which extends beyond the p-GaN layer is beneficial as the current can flow along the inversion channel created by the gate which is normally more conductive than the surrounding i-GaN layer. However, the depth cannot be too large as during OFF-state operation, the gate oxide at the trench bottom could be subject to high electric fields which could lead to premature breakdown. So an optimal gate trench depth would be around 1.5 µm.

Fig. 3.3 also includes the cross-sectional image of the quasi-vertical MOSFETs taken by focused ion beam-scanning electron microscope (FIB-SEM), in which a 3 µm-thick Pt was deposited at

the gate region for surface protection. The depth in the etched trench was 1.6 µm, reaching the drift layer, and the trench sidewalls were inclined by 13.2 ° from the c-axis. The trench width was 4.0 µm and 5.5 µm at the bottom and the top, respectively. The angle of the trench sidewall can be improved with optimized dry etching conditions and further smoothened with longer TMAH treatment [148, 170, 171]. The small kink observed at the middle of the sidewall might be due to erosion of the SiO_2 hard mask edge during dry etching.

3.2.3 Electrical characteristics

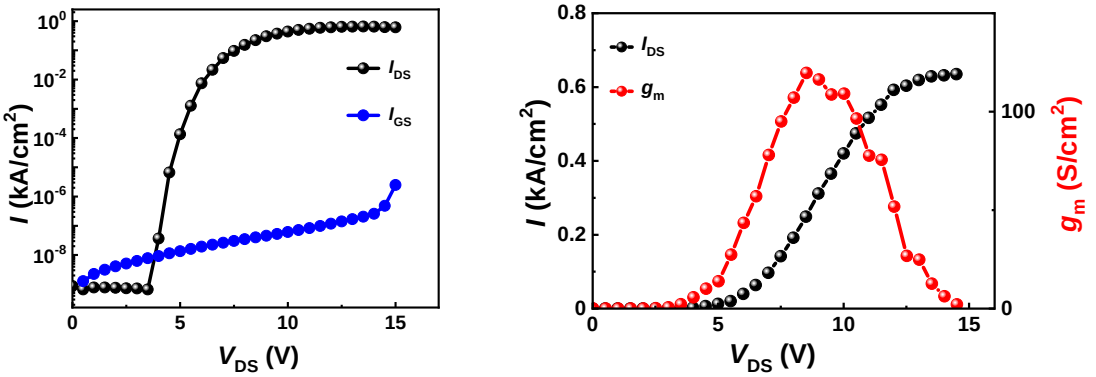


Figure 3.4 – (a) Semi-log, and (b) linear-scale transfer characteristics of the vertical trench gate MOSFETs on silicon substrate.

The transfer characteristics of the vertical trench MOSFETs in Fig. 3.4a show a current on/off ratio of over 1×10^8 and a sub-threshold slope of 250 mV/dec. The low off-state leakage current level, below 1×10^{-8} kA/cm^2, reveals the effective current blocking by the n-p-i-n heterostructure in off state. The slight increase in gate leakage from 1.2×10^{-9} kA cm^{-2} at $V_{GS} = 0$ V to 2.5×10^{-6} kA cm^{-2} at $V_{GS} = 15$ V can be further reduced by optimizing the trench fabrication and the gate dielectric. Fig. 3.4b shows normally-off operation with a threshold voltage of 6.3 V (obtained by linear extrapolation) and peak transconductance of 269 S/cm^2. The high V_{th} is preferable for high-power applications to guarantee a safe operation and better noise immunity. The channel mobility (μ_{ch}) extracted using the equation from [84] in the linear region was 17.8 cm^2/(Vs), which is comparable to the value in [172] but lower than those from [84] and [85] (this value is underestimated due to additional series resistance induced by the thick drift layer (4 µm) [173]). The lower μ_{ch} is likely due to the typically larger defect density of GaN on silicon compared to that on bulk GaN substrates. In addition, μ_{ch} can be enhanced by improving the sidewall smoothness with an optimized TMAH treatment process [148, 170]. The output characteristic (I_D-V_{DS}) (Fig. 3.6) was normalized by the trench area ([174]) including 2 µm on each side of the trench to account for the current spreading. This is evident from the Fig. 3.5 which shows the TCAD simulation of conduction current density at a V_{DS} of 10 V and V_{GS} of 12 V. As observed from the calculation mentioned in Fig. 3.5, the majority contribution to the $R_{on,sp}$ is from the channel region. Good saturation behavior and an on-state current of ~ 1.3 kA/cm^2 were observed

at V_{GS} = 12 V and V_{DS} = 11 V. The $R_{on,sp}$ estimated from the linear region was 15.3 mΩcm^2. The larger channel resistivity is mainly due to our poorer channel mobility of 17.8 cm^2/(Vs), compared to 131 cm^2/(Vs) in [85].

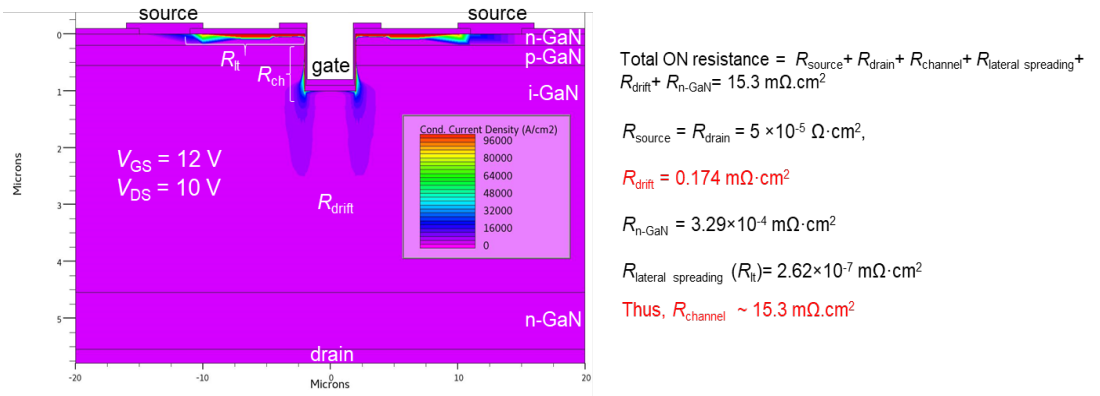


Figure 3.5 – TCAD simulation of conduction current density in a GaN trench MOSFET and calculations showing the various contributions to $R_{on,sp}$.

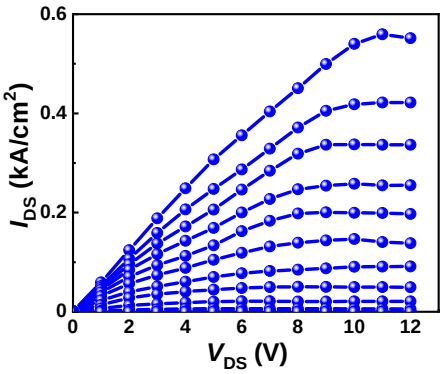
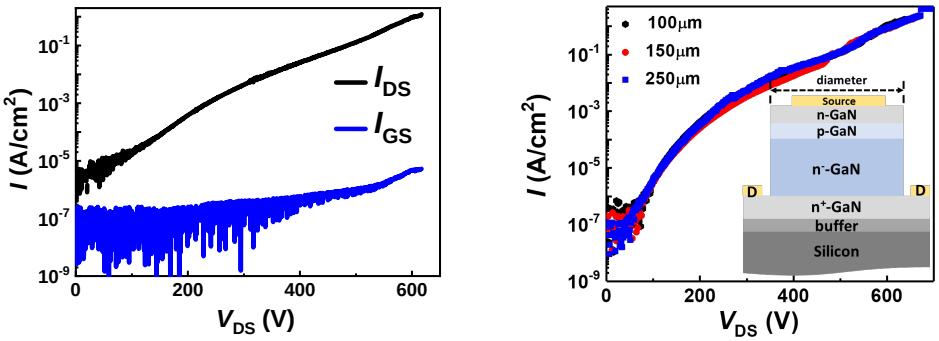


Figure 3.6 – Output I-V characteristics of the fabricated vertical trench gate MOSFETs on silicon substrate.

Fig. 3.7a shows the off-state I-V characteristics measured at V_{GS} = 0 V for the fabricated trench gate MOSFET with floating substrate. The vertical MOSFETs exhibited a large hard breakdown voltage (BV) of 645 V, while the gate current remained at a low value below 1×10^{-5} A/cm^2, indicating that the breakdown occurred mainly between the source and drain terminals. This was confirmed by remeasuring the devices which revealed a immediate jump to the current compliance value once a small V_{DS} was applied. The observed breakdown was destructive and mainly happened at the mesa edges. By introducing field plates (FP) and edge-termination technologies to these devices, the electric field at the junction edge could be reduced, which would further enhance their breakdown voltage. However, the performance observed even without edge termination is quite remarkable which reveals the enormous potential for GaN on Si vertical



(a) (b)

Figure 3.7 – (a) Off-state I-V characteristics measured at V_{GS} = 0 V for the fabricated trench gate MOSFETs on silicon substrate, and (b) two terminal I-V characteristics of the as-grown n-p-n structure. The inset shows the schematic view of the measured n-p-n structure.

transistors. The measured BV was consistent with the vertical breakdown voltage measured from two-terminal circular n-p-i-n test structures of 679 V (Fig. 3.7b).

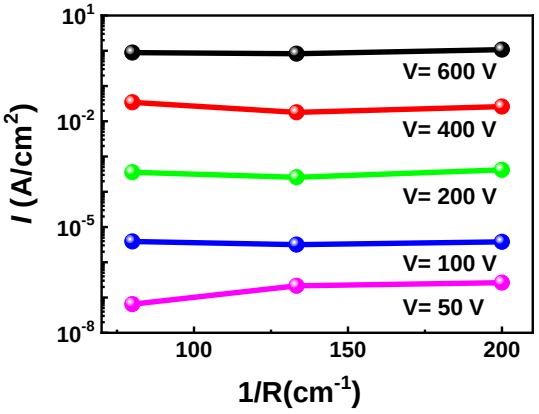


Figure 3.8 – Leakage current density of the two-terminal circular n-p-n test structure with different mesa radius R.

The measured leakage current mainly flows through the n-p-n heterostructures, instead of the etched surfaces. To test this, we have measured the leakage current from two-terminal circular n-p-n test structures with different mesa radius (R = 50 μm, 75 μm, and 125 μm), and found the exact same leakage current density with different radius (no dependence of leakage current density on the mesa periphery in Fig. 3.8). This indicates that the device leakage current is mainly through the heterostructure instead of the etched sidewall. The relation between leakage current density (I) and the average electric field (E) in the drift layer reveals the off-state leakage mechanism [148]. The nearly linear dependence of $\ln(I) \propto E$ (extracted from Fig. 3.7a) for the vertical MOSFETs indicates that the dominant leakage mechanisms in our devices is variable-range hopping [175]. The BV of 645 V and $R_{on,sp}$ of 15.3 mΩ cm^2 resulted in a very good Baliga

figure-of-merit (FOM) of 61 MW/cm^2, which is superior than devices fabricated on sapphire substrates. The FOM of these GaN-on Si vertical MOSFETs can be significantly improved:

1. By utilizing TMAH treatment in the trenches with higher TMAH concentrations and longer durations to reduce $R_{on,sp}$.
2. By designing field plates and edge terminations to enhance the BV.
3. By substrate removal, as a fully vertical transistor would significantly reduce current crowding in the bottom n-GaN layer towards the drain contact, thus reducing $R_{on,sp}$.

3.3 Large-area quasi-vertical GaN-on-Si power MOSFETs

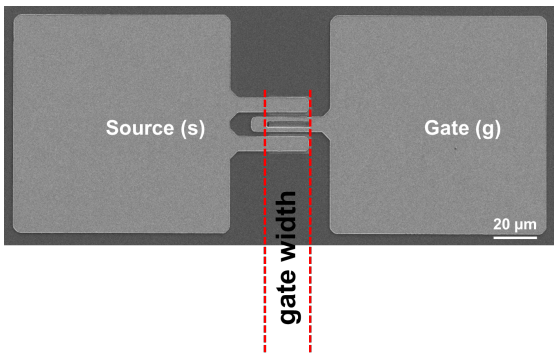
As discussed before in Chapter 1, for power applications of 10 KW and higher, a vertical device structure is more preferable as compared to a lateral one as a vertical design allows higher current per chip area and BV scaling without scaling the chip size, and thus is the more economical solution. In order to validate this advantage of vertical devices, it is necessary to demonstrate GaN vertical devices with high-current capability. The devices mentioned in section 3.2 had a peak I_{DS} of $\sim$ 3 mA at a V_{GS} = 12 V. For high power applications, it is necessary to demonstrate > 1A output current capability which has been demonstrated in bulk GaN vertical p-i-n diodes and MOSFETs [98, 176]. However, it is important to investigate whether it is possible to achieve high-current capacity in GaN-on-Si devices. Here we discuss the implementation of large-area high-current GaN-on-Si vertical MOSFET. The device architecture is quasi-vertical and thus is not the ideal choice for demonstrating high-current devices due to inherent current crowding issues associated with a quasi-vertical design for power devices. However, such an experiment will reveal the limits of current capability for a quasi-vertical design and thereby the potential application areas for these quasi-vertical devices.

3.3.1 Device structure and Fabrication

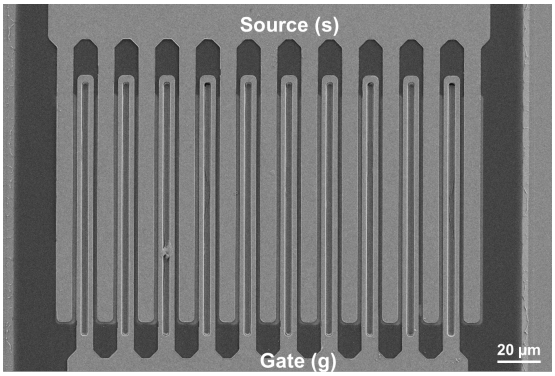
The device mentioned in section 3.2 is a single-finger device in the sense that it has a single linear finger section which constitutes the gate terminal of the MOSFET, as shown in Fig. 3.9a. The gate region in a MOSFET controls the amount of current flowing through the device in ON-state and thus in order to increase the current capacity of the MOSFET, we need to increase the gate width (Fig. 3.9a). This can be achieved in many ways:

- by increasing the width of the single-finger device (Fig. 3.9a).
- by implementing a multi-finger gate terminal design (Fig. 3.9b).
- by implementing a circular, square or hexagonal gate cell array (Fig. 3.9c)

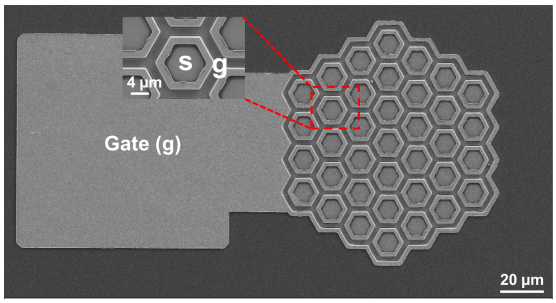
However, implementing a high-current MOSFET just by increasing the width of a single-finger device results in devices which very long in one dimension and makes device packaging difficult and inefficient especially for currents > 50 mA. While a multi-finger solution as shown in Fig. 3.9b is a better option, in order to maximize the gate width per unit area, the best approach is to have a square or hexagonal gate cell array. Similar structure was adopted for Si power MOSFETs



(a)



(b)



(c)

Figure 3.9 – SEM image of (a) single finger trench MOSFET, (b) multi-finger trench MOSFET, and (c) hexagonal gate cell array.

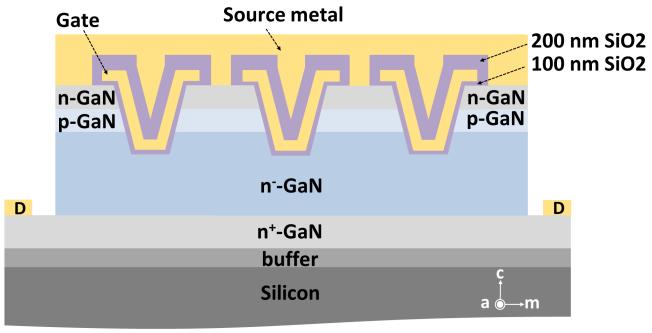
(called as HEXFETs [177])for increasing the current capacity per unit area of the semiconductor, with excellent results. For a square gate cell array, during the gate trench etching step if we align one side of the square in such a way that the trench sidewall face is m-plane, the adjacent side will have an a-plane sidewall face. This creates an issue especially after the TMAH etching step to smoothen the damages created by the dry etching. After hot TMAH treatment at 85 °C, the a-plane side wall face becomes very rough and this reduces the mobility of the electrons in the channel region. However if we use a hexagonal gate cell array, and align one side in such a way

that the trench sidewall face is m-plane, all other sides will have an m-plane sidewall face. This is very advantageous as after the TMAH treatment, all the 6 sidewalls of the hexagonal cell array will be smooth and thus doesnt deteriorate the effective channel mobility. For this reason, we resorted to using a hexagonal gate cell array for achieving high-current vertical MOSFET.The main bottleneck towards the reliability of these devices is related to the uniformity and quality of the gate oxide used. A low quality gate oxide could rupture during OFF-state operation leading to the gate and entire device failure at local gate oxide weak spots. Thus a high quality gate oxide deposition method is very essential for improving the reliability of the device. Also in a large area device, the p-GaN channel region is bigger and thus an adequate activation annealing time is necessary for the proper functioning of the device. If the activation annealing step is short in duration, there could be regions in the device where the p-GaN is not properly annealed and could result in undesirable shape in the output I-V characteristics. This could be either shallow slope of the I-V curve or appearance of small turn-on voltage.

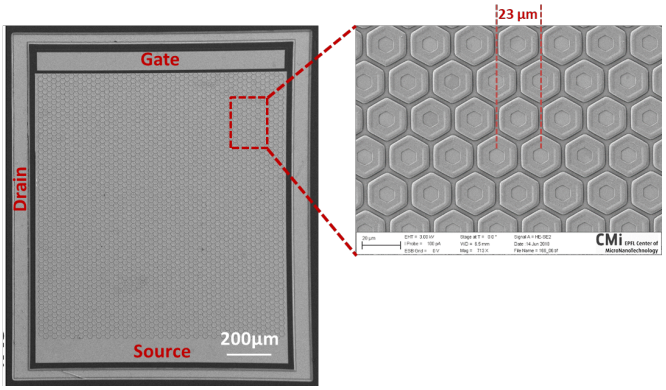
Fig .3.10a shows the cross sectional schematic of a large-area quasi-vertical MOSFET on GaN-on-Si and Fig. 3.10b shows the top view SEM image of one such fabricated MOSFET. Quasi-vertical MOSFETs of different active areas were fabricated. Active area in this case was defined as the total area occupied by the hexagonal cells incorporating the gate and source terminal as shown in Fig 3.10b. The fabrication process is similar to that mentioned in subsection 3.2.2 with the modification that the source metal deposition is not done together with the gate. After the depositing Cr/Au 50/200 nm to for the gate electrode, an additional 200nm SiO_2 is deposited on the top by PECVD. This is to provide electrical isolation between the source and the gate metal. Then contact holes are formed by photolithography followed by dry etching of (200 + 100) nm of SiO_2 to access the top n-GaN layer. Cr/Au bilayer (50/200 nm) is deposited to form the source electrode. Finally, a 5 μm-deep etching was performed using a Cl_2/BCl_3/Ar- based ICPRIE etch, followed by the evaporation of Cr/Au drain electrodes.

3.3.2 Electrical characteristics

The ON-and OFF-state characteristics of the large-area quasi-vertical MOSFETs of different sizes were analysed and compared against the performance of the smallest one. This was to understand the impact of the current crowding arising from the quasi-vertical design on device performance. As discussed above, the active area of these MOSFETs (i.e., the normalization factor for converting current to current density) is defined by the area of the hexagonal cell array and not the gate trench area which was used for normalization of current of the single-finger quasi-vertical MOSFET mentioned in section 3.2. This is because even though the real normalization factor should be the total gate trench area, given by the total gate width × trench width, for large-area MOSFETs, it is difficult to extract the total gate width easily and for sake of convenience, the area of the hexagonal array is taken. Fig. 3.11a shows the output characteristics of the quasi-vertical MOSFET of size 0.1 × 0.1 mm^2. The peak current which the device can provide at a V_{GS} of 20 V is 24 mA, which is already a step up on the ~ 3mA current provided by the single-finger MOSFET mentioned in section 3.2. The slight non-linearity observed in the shape of the output characteristics is believed to be from the insufficient p-GaN activation annealing time which results in localized regions where the p-GaN is not completely activated.



(a)

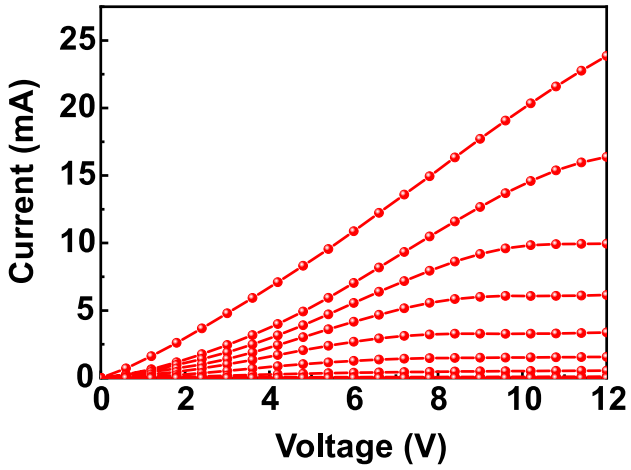


(b)

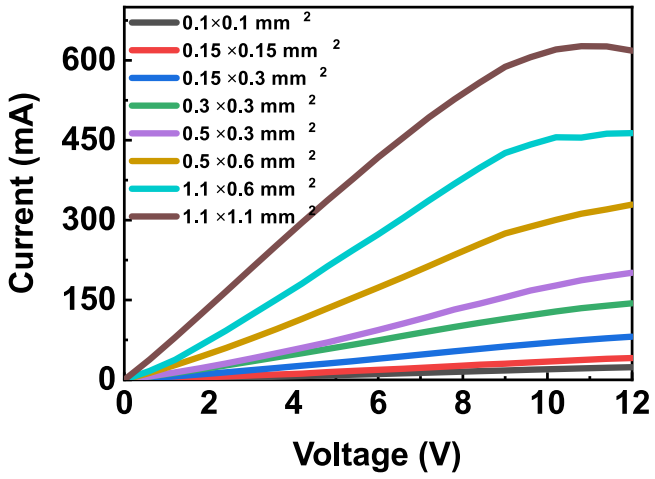
Figure 3.10 – (a) Cross sectional schematic of a large-area MOSFET. (b) Top view SEM image of a large-area MOSFET.

This could be alleviated by increasing the activation annealing time to 30 mins from 20 mins. Fig. 3.11b compares the peak output current at V_{GS} of 20 V for the MOSFETs of various sizes. As observed, the largest MOSFET with a size of 1.1 × 1.1 mm^2 provides a peak current of 0.63 A. However, this device was designed to provide 2 A by scaling the gate width as compared to a single-finger quasi-vertical MOSFET. This drastic reduction in current is mainly due to the current crowding occuring in the bottom n-GaN layer near the drain contact. Table 3.1 shows the $R_{on,sp}$ for all the MOSFETs. As we observe, the $R_{on,sp}$ degrades with increasing the size of the MOSFET which is again a direct consequence of current crowding.

Fig. 3.12 shows the trend in current up scaling with the area of the MOSFETs. Here again we see no linearity in current scaling with area,which is due to the detrimental effect of current crowding. The curve shows three distinct slopes. These three regions can be identified as three levels of current crowding. In the range of 0 to 0.1 mm^2 marked region I, corresponding to a current level of 0 to 144 mA, the current scales almost linearly with area and effect of current crowding is negligible. This was also verified on quasi-vertical p-i-n diodes of 80 µm anode diameter which showed no degradation in the $R_{on,sp}$ upto a current level of 120 mA. For the MOSFET active area in the range 0.1 to 0.33 mm^2 marked by region II, the effect of current crowding



(a)



(b)

Figure 3.11 – (a) Drain to source I-V characteristics of large-area MOSFET with size 0.1 × 0.1 mm^2 with V_{GS} varying from 0 to 20 V with a step of 2 V. (b) Comparison of I-V at V_{GS} of 20 V.

starts to kick in and thus the slope of scaling decreases. For area in the range of 0.33 to 1.3 mm^2 marked region III, the current crowding becomes very prominent and degrades the current scaling with area as evidenced by the sharp reduction the slope. This is also clear from table 3.1 displaying the variation of $R_{on,sp}$ with area. The $R_{on,sp}$ increases drastically for large-area MOSFETs of size > 0.3 mm^2. The $R_{on,sp}$ of the 0.01 mm^2 was also calculated by using the gate trench area normalization used for the single-finger MOSFET in section 3.2. The $R_{on,sp}$ obtained is 9.8 mΩcm^2 which is close to what was achieved for the single-finger MOSFET. In the absence of current crowding a vertical MOSFET of size 1.2 mm^2 should provide a current > 2 A which can be obtained by extrapolating the first region of the scaling curve. Thus a fully-vertical

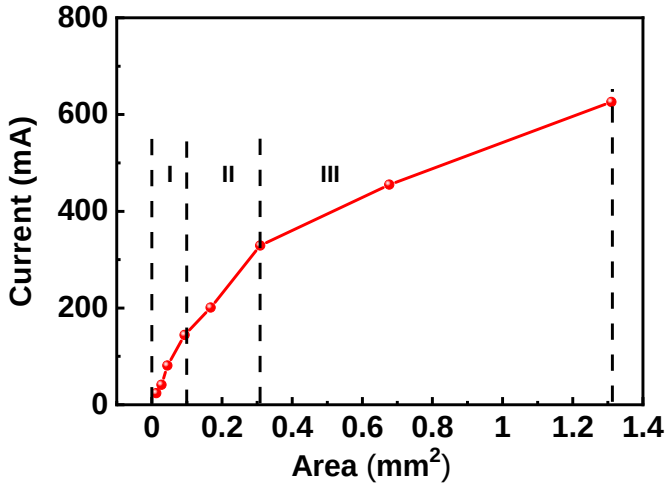


Figure 3.12 – Current up scaling trend with area of the trench MOSFET

design is absolutely essential to keep the scaling curve linear and thus realize vertical devices of high-current (> 2 A) capability.

Area (mm^2)	0.01	0.023	0.045	0.09	0.15	0.3	0.66	1.2
$R_{on,sp}$ ($m\Omega cm^2$)	49	52	58	63	82	92	131	193

Table 3.1 – $R_{on,sp}$ variation of large area quasi-vertical MOSFETs

Fig. 3.13a and Fig. 3.13b shows the OFF-state reverse leakage measurements on the devices at a V_{GS} of 0 V. We couldn't observe any improvement in the BV with the introduction of a mesa and short (5 µm) field plate (FP), which could be rectified by a proper simulation study. However, the devices with termination consistently provided lower leakage at low V_{DS} < 100 V. This is possibly due to the termination mesa which reduces leakage current through the dry etched sidewalls adjacent to the drain terminal. The low BV of 200 ~ 300 V for devices of various sizes was attributed to low quality of gate oxide as observed from Fig. 3.13c which shows hard breakdown happening at the gate region. Similar BV was reported for large-area trench MOSFET on bulk GaN employing a drift layer thickness of 10 µm, with breakdown occurring due to gate oxide failure [176]. Thus improving the quality of the gate oxide and termination methods is imperative for achieving reliable high BV devices capable of delivering high-current. The maximum power which can be delivered by these devices is around 180 W. From the Fig. 3.14 displaying the current and voltage requirements for different power applications, we can elucidate that these devices could be used for applications like display drive and telecom. If these devices were capable of providing high-current in the range of 15-20 A, it would widen the application areas to power supplies and automotive as well. However, for achieving this, a fully-vertical device design is imperative and a demonstration of such a device is discussed in the next section.

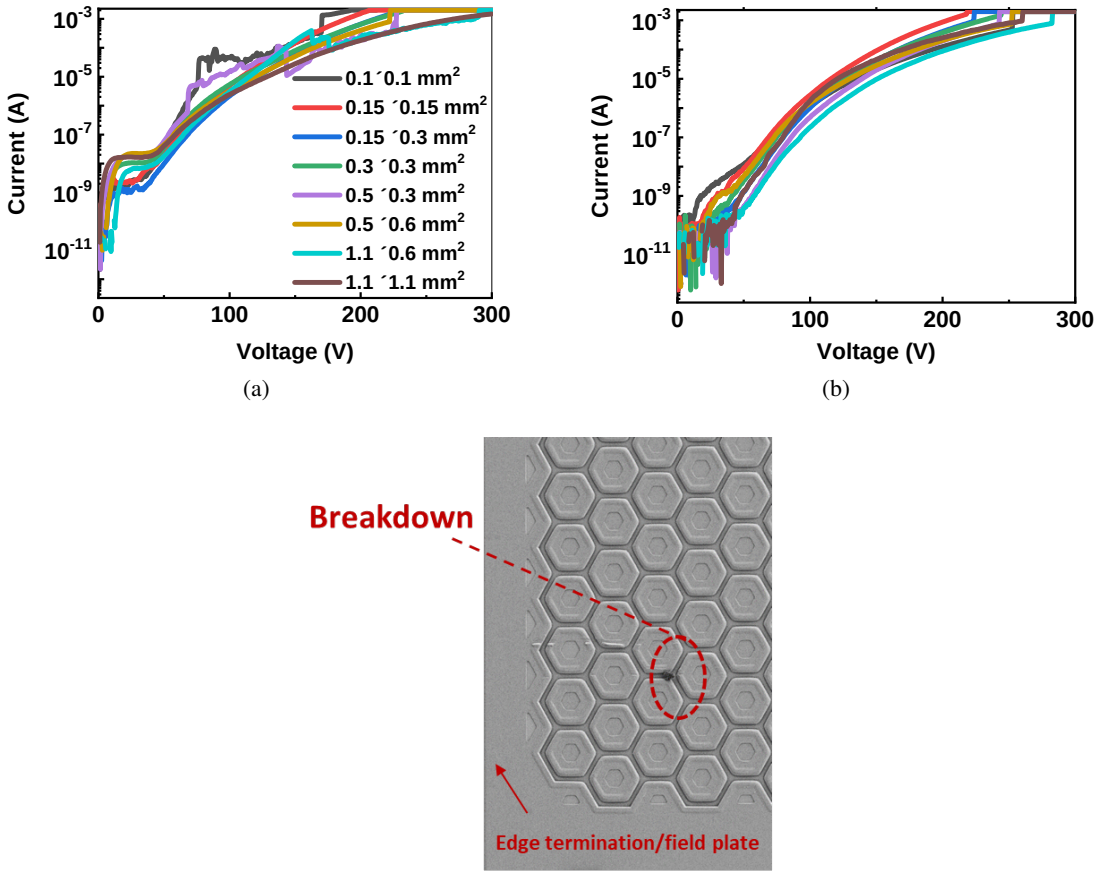


Figure 3.13 – Reverse I-V characteristics of large-area MOSFET of various sizes which are (a) un terminated and (b) terminated with a mesa and short field plate. (c) SEM image showing the area where the gate broke under reverse bias application.

3.4 Fully-vertical GaN-on-Si power MOSFET

Recently, high-voltage GaN-on-Si quasi-vertical transistors [120] and high-performance quasi- and fully-vertical p-i-n diodes [106], [169] have been demonstrated, but their performance (quasi-vertical) is severely limited by current crowding in the bottom n-GaN layer [140], which significantly increases the $R_{on,sp}$, especially in large area devices as evidenced in the previous section. While the $R_{on,sp}$ can be improved by increasing the doping and thickness of the bottom n-GaN layer, this restricts the remainder thickness of the drift layer which can be grown without wafer cracking, thus limiting the effective BV. In addition, quasi-vertical designs require a larger device area since all pads occupy the top surface of the wafer. These challenges can be addressed by a fully-vertical design which is not affected by current crowding due to the vertical nature of the current flow, offering therefore a much larger current capability and significantly smaller $R_{on,sp}$. In addition, a fully-vertical design would provide a larger number of devices per unit area of the wafer compared to quasi-vertical designs, since the drain contact is made at the bottom of

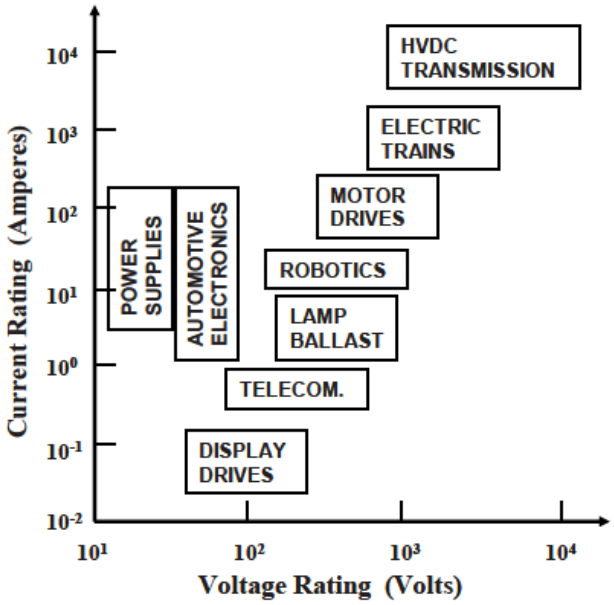


Figure 3.14 – System ratings for power devices [6].

the wafer.

In this work, we demonstrate the first fully-vertical GaN-on-Si power MOSFET based on a robust fabrication process to selectively remove the Si substrate and resistive buffer layers under the devices, followed by a conformal deposition of a 35-µm-thick copper layer on the backside by electroplating, which provided excellent mechanical stability and electrical contact to the bottom n-GaN layer. The devices were fabricated on a 6.6 µm-thick n-p-i-n GaN epitaxial structure grown on 6-inch Si substrate. The fabrication process of the gate trenches, including alignment, etching mask and surface treatment was optimized to increase the channel field effect mobility and device output current. Fully-vertical GaN-on-Si power MOSFETs are demonstrated presenting large forward current density up to 1.6 kA/cm^2 and small $R_{on,sp}$, down to 5 mΩcm^2, along with high BV of 520 V. These results open a promising pathway for the development of GaN-on-Silicon vertical devices for future power applications. The results mentioned here are from our publication paper [2].

3.4.1 Device structure and fabrication

The n-p-i-n structure used for this device fabrication is the same mentioned for the quasi-vertical MOSFET described in section 3.2. The fabrication process started with a 1.27 µm deep dry-etching of the gate trench using two different types of hard masks - metal (Ni) and oxide (SiO_2) – fabricated on separate chips for comparison. Each chip also had quasi- and fully-vertical devices for accurate analysis of electrical performance. A subsequent treatment by 25% Tetra Methyl Ammonium Hydroxide (TMAH) was performed at 85 °C for 1 hour to smoothen the etched

[2] R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, "Fully Vertical GaN-on-Si power MOSFETs," IEEE Electron Device Letters, vol. 40, no. 3, pp. 443–446, Mar. 2019. Contribution: First author

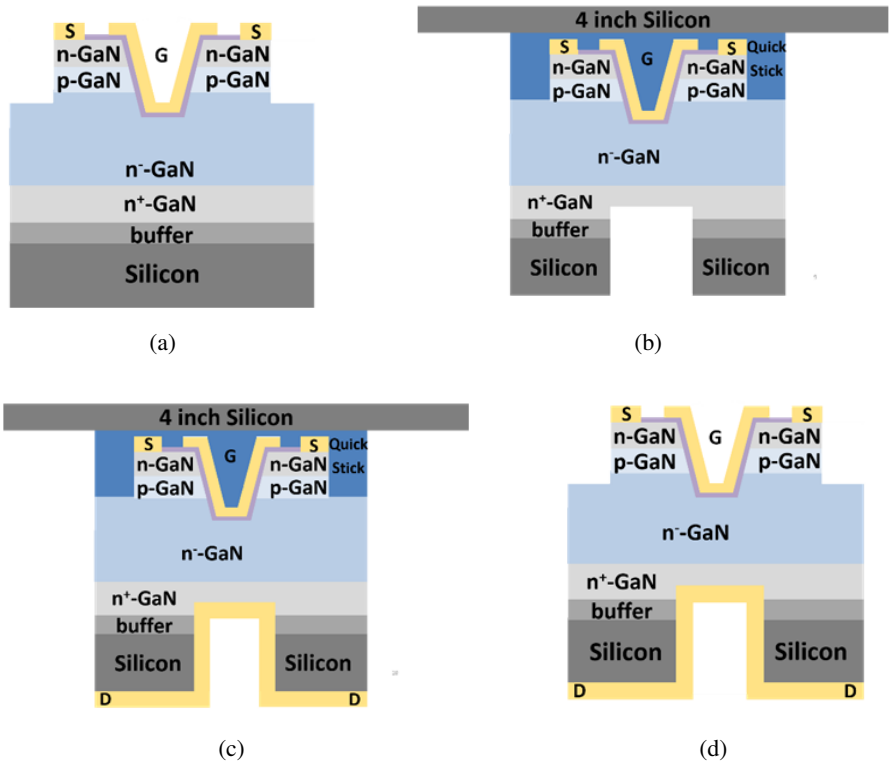


Figure 3.15 – Fabrication process of fully-vertical GaN-on-Si MOSFETs. (a) Schematic of the device structure after definition of source and gate pads and thinning of the silicon substrate. (b) The drain contact is defined at the backside via a support wafer attached to the device using QuickStick 135. (c) Schematic of the device after deposition of back contact and copper electroplating. (d) After releasing from the silicon wafer.

surface and remove dry-etching damages at the gate trench sidewalls [148]. A rapid thermal anneal (RTA) was then carried out at 750 °C for 20 min in N_2 ambient to activate the buried p-GaN layer through the sidewalls. The devices were isolated by 1.35 µm-deep Cl_2-based mesa etch, followed by 100 nm-thick SiO_2 gate oxide deposited by atomic layer deposition (ALD) at 300 °C using bis(tertiary-butylamino)silane and ozone as precursors. The thick oxide layer protects the gate terminal against the high electric field regions at the bottom of the gate trench during reverse bias operation. After opening the source contact by dry etching of SiO_2, Cr/Au (50/250 nm) were deposited as gate and source contacts . For the remainder of the fully-vertical device fabrication, the Si substrate was first thinned by grinding from 1000 µm to 500 µm (Fig. 3.15a). The chip was then attached to a Si support wafer by a temporary mounting wax (QuickStick 135) for the backside processing . After patterning the regions of the backside under each device, the Si substrate was completely dry-etched by bosch deep-reactive-ion-etch process, followed by a Cl_2-based dry-etching of the resistive GaN buffer (Fig. 3.15b). Cr/Au (50/250nm) metal stack was deposited as ohmic contact for the drain by e-beam evaporation, followed by a 35-µm-thick electroplated Cu layer, which offered excellent mechanical stability to the thin GaN

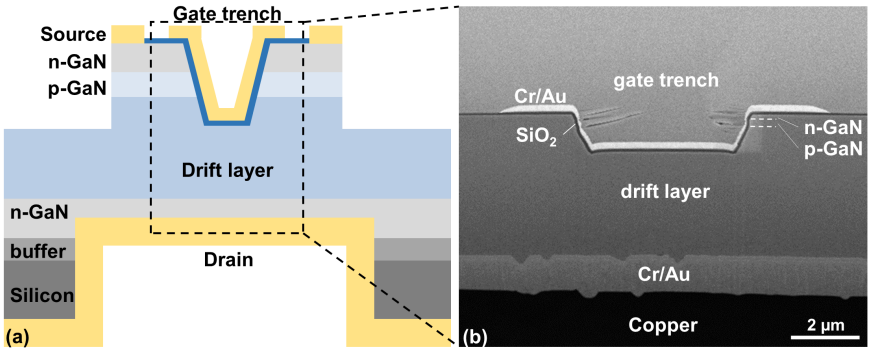


Figure 3.16 – Cross-sectional SEM image of the fabricated fully-vertical GaN-on-Si MOSFET.

membrane (Fig. 3.15c). The chips were then released from the Si support wafer by immersion in hot acetone to dissolve the QuickStick 135 mounting wax ((Fig. 3.15d)). Fig. 3.16 shows the cross-sectional SEM image of the fabricated device. Such a fully-vertical device results in an overall device area which is 60% smaller than an equivalent quasi-vertical device as a result of the drain terminal being on the bottom side.

3.4.2 Electrical Characteristics

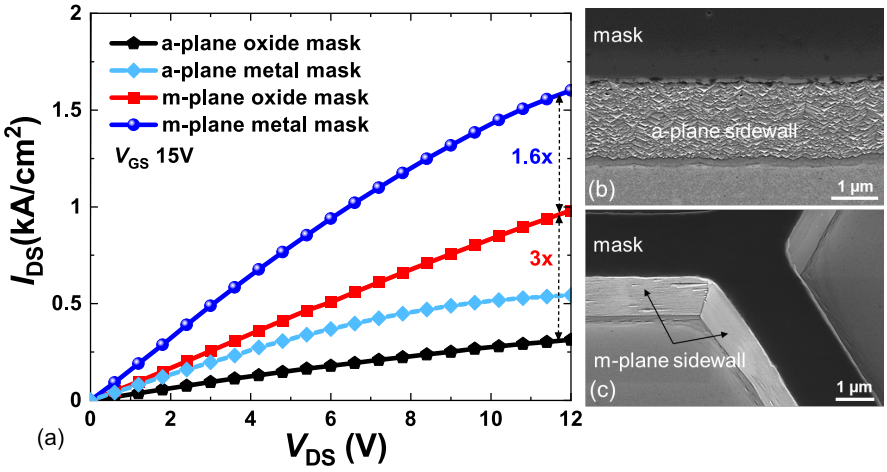


Figure 3.17 – (a) Comparison of the I_{DS}-V_{DS} of the fabricated vertical MOSFETs with gate trench aligned along m- and a-plane, using metal and oxide hard masks. SEM images of the trench sidewall aligned along the (b) a-plane and (c) m-plane, after TMAH wet treatment. Notice the much smoother m-plane sidewalls compared to the a-plane.

To optimize the device performance, we investigated the effect of orientation and etch mask used to define the gate trench, on the electrical characteristics of the devices. Gate trenches were aligned along the m- and a-planes of GaN followed by a TMAH surface treatment. The width and length of the gate trench were 32 μm and 6 μm respectively. The Cl_2-based dry-etching process was performed using metal and oxide hard masks. As shown in Fig. 3.17a, vertical MOSFETs with gate trench aligned along the m-plane presented 3x-higher drain current and

3x-lower $R_{on,sp}$ as compared to those aligned along the a-plane. Such a significant enhancement is due to the much smoother m-plane sidewall after TMAH treatment compared to the a-plane, as evident from Fig. 3.17b and Fig. 3.17c, which resulted in a much improved electron mobility in the MOSFET channel (similar observation was reported in [172]). An additional 1.6x-fold improvement in output current was achieved by utilizing a metal (Ni) hard mask to etch the gate trenches, instead of SiO_2 hard mask. Fig. 3.18a shows the extracted field-effect mobility from the transconductance of vertical MOSFETs fabricated with metal and oxide hard masks, at V_{DS} of 0.1, 1, 2, 5 and 10 V using the relation $g_m = \left(\frac{Z}{L}\right) \times \mu \times C_o \times V_{DS}$ with an average g_m obtained from double-sweep measurement. A much higher field average effective mobility was observed for the device processed with metal hard mask of 41 cm^2/Vs as compared to 21 cm^2/Vs for the oxide mask. To the best of our knowledge, this is the highest mobility reported on GaN trench gate MOSFETs grown on foreign substrates. This is possibly due to fact that the angled trench

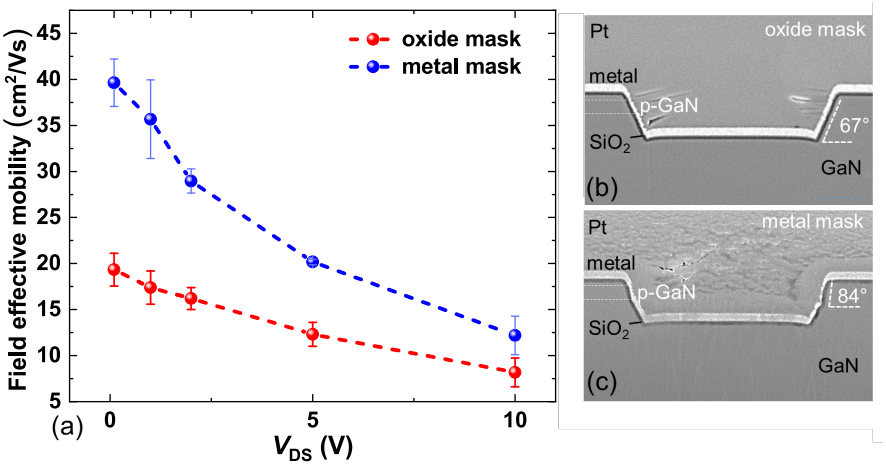
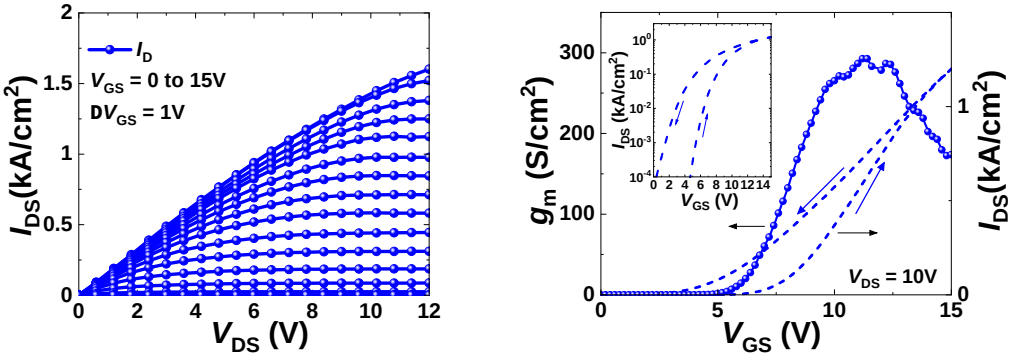


Figure 3.18 – (a) Field effect mobility extracted from devices with metal mask and oxide mask etched gate trench (b) Cross-sectional SEM of oxide mask etched gate trench presenting slanted side walls (67°) and (c) metal mask etched gate trench showing near-vertical (84°C) sidewalls at the channel (p-GaN) region.

sidewall (67°) created by the oxide mask is oriented mostly at a semi-polar GaN plane [178, 179] very close to the $10\bar{1}1$ plane [170], which is not charge neutral, leading to more scattering and reduced electron mobility in the inversion channel. On the other hand, the metal mask offers a near-vertical (84°) and smooth sidewall for the p-GaN channel [171]. However, further studies are needed to accurately understand this improvement in mobility. Fig. 3.19a shows the output characteristics of the fabricated vertical MOSFETs with metal mask, revealing a very high current density of 1.6 kA/cm^2 and a $R_{on,sp}$ of 5 mΩcm^2. These values were normalized by the device active area, defined by the gate trench area of 10 µm × 36 µm [174], after accounting for a lateral current spreading of 2 µm from all the sides of the gate trench (which was confirmed by TCAD simulations). These devices exhibited 2.8×-better current density and 3×-lower $R_{on,sp}$ as compared to quasi-vertical MOSFETs on a similar GaN epitaxial structure on Si substrate [120], which was described in the first part of this chapter. This improvement in electrical performance is mainly due to the fully-vertical design of the device [140] and the improved mobility in the



(a) (b)

Figure 3.19 – (a) I_{DS}-V_{GS} characteristics of metal mask vertical MOSFET for V_{GS} varying from 15 V to V in steps of 1 V. (b) Transfer and transconductance (g_m) characteristics. Inset figure shows the transfer curve in semi-log scale.

p-GaN inversion channel. The p-GaN inversion channel is the major limiting factor to the $R_{on,sp}$, as the resistance of the i-GaN layer was 0.33 mΩcm^2 and of the bottom n-GaN layer was 6.2 × 10^{-4} mΩcm^2. The lateral spreading resistance from the source contact to the p-GaN inversion channel was 2.62 × 10^{-7} mΩcm^2 and the source and drain contact resistances were 5 × 10^{-5} mΩcm^2. These values are much smaller than the measured 5 mΩcm^2, indicating that the $R_{on,sp}$ is mainly determined by the resistance of the p-GaN inversion layer.

Fig. 3.19b shows the the I_{DS}-V_{GS} and the g_m-V_{GS} characteristics of the metal mask device. The device presented a V_{th} of 7.9 V (from extrapolation in linear scale) along with a 125%-higher g_m, up to 300 S/cm^2 as compared to the quasivertical device [23]. The V_{th}, defined at I_{DS} of 20 A/cm^2, was 6.4 V. Such a relatively small V_{th} value is mainly due to donor-type N-vacancies present in the trench sidewall as a result of defects from the dry-etching process [93, 180, 181]. The negative hysteresis of ~ 2 V (at a current density of 0.2 kA/cm^2) observed in the I_{DS}-V_{GS} curves is likely due to bulk oxide traps [182], which can be addressed with a better quality gate oxide deposition and post-deposition annealing.

The GaN-on-Si vertical MOSFETs exhibited an excellent off-state behavior, with BV of 520 V, which was achieved without deploying any particular field plate or edge termination techniques (Fig. 3.20), along with a small drain to source leakage current (I_{DS}) lower than 1 × 10^{-1} A/cm^2 (normalized by the mesa area of 110 µm × 197 µm as in [94, 96, 120]). The nearly-linear dependence in log-scale of the drain-to-source leakage current (I_{DS}) with applied electric field at high bias is an indication of variable range hopping mechanism [175]. The gate leakage current remained below 1 × 10^{-4} A/cm^2 until the breakdown happened at the gate edge.

3.5 Conclusion

To conclude, we demonstrated two versions of GaN power MOSFETs on silicon substrates. The quasi-vertical MOSFET which was developed first provided excellent ON- and OFF-state behaviour, especially considering that it was the first demonstration of a GaN power MOSFET

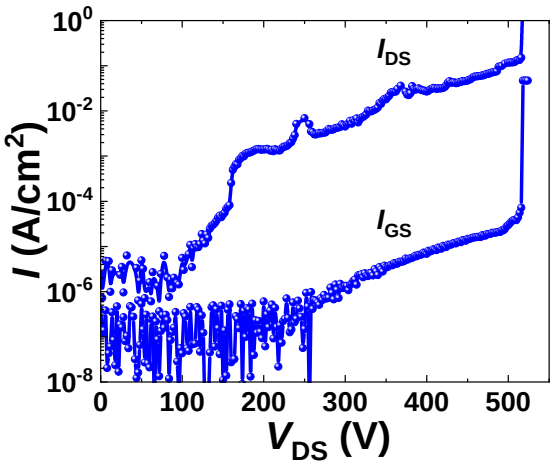


Figure 3.20 – Off-state blocking performance of the metal mask vertical MOSFET measured at a V_{GS} of 0 V.

on silicon substrates. $R_{on,sp}$ as low as 15.3 mΩcm^2 and a high V_{th} of 6.3 V, ideal for power electronic applications were obtained. The device also presented an excellent BV of 645 V, which is the highest reported for power MOSFETs on GaN-on-Si, till date. Next, we invsetigated the scale-up of a quasi vertical power MOSFET by developing a large area power MOSFET that should be capable of delivering an ON-state current of 2 A. The device also had a hexagonal gate cell array for maximizing the output current per unit area of the device. However, due to the detrimental effects of current crowding, we could achieve only a peak current of 600 mA at a V_{GS} of 20 V. This motivated us to find a solution for the current crowding in quasi-vertical structures by developing a unique and novel fully-vertical structure. The fabricated fully-vertical MOSFET presented state-of-the-art ON-state performance with an improvement in $R_{on,sp}$ by 3x to 5 mΩcm^2, while providing a comparable BV as the quasi-vertical MOSFET. Fig. 3.21 presents the benchmarking of our quasi- and fully-vertical GaN-on-Si MOSFETs against other GaN vertical transistors demonstrated on bulk GaN and Si substrates. Further enhancement in breakdown voltage is envisaged by employing properly designed field plates at the source and gate contacts together with thick passivation layers, as demonstrated in bulk GaN MOSFETs [86, 94, 181].

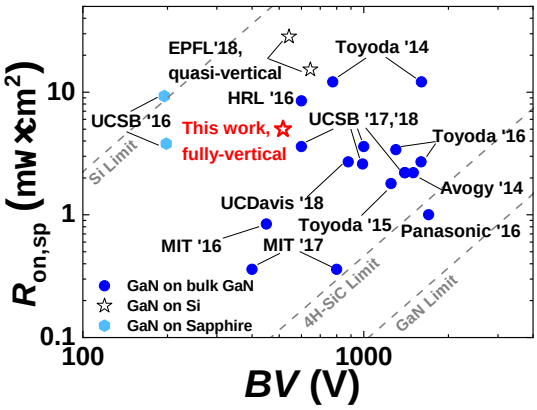
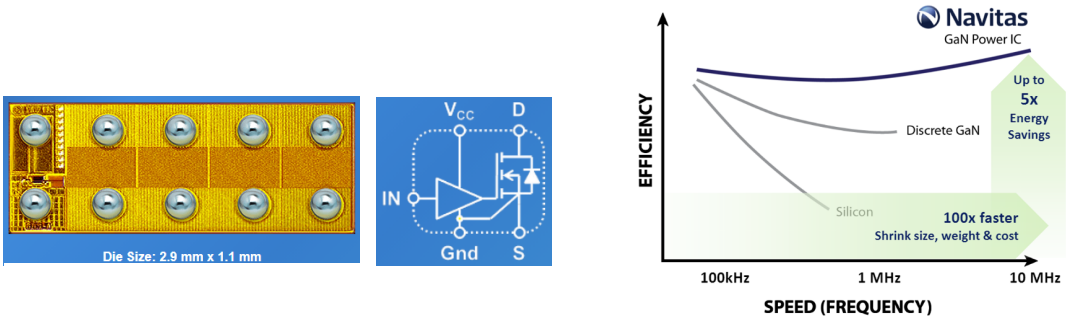


Figure 3.21 – $R_{on,sp}$ vs BV benchmarking of the metal mask device against other reported GaN vertical transistors on bulk GaN and Si substrates.

4 MOSFET Integration

GaN-on-Si technology offers an unique advantage for the possible integration of several different devices on the same chip to realize integrated circuits (IC) which have evident benefits like smaller IC foot print, greatly reduced parasitic capacitance and resistance arising from wire bonding of discrete devices leading to higher efficiency, lower cost, etc. To date several different integration schemes on GaN-on-Si lateral technology has been demonstrated including integrated lateral field effect rectifier with normally-off HEMT for switched mode power supply converters [183], integration of high-density low power Si MOS logic with high power HEMTs [184], three-stage W-band GaN monolithic microwave integrated circuit power amplifier (MMIC PA) [185], monolithically integrated enhancement/depletion-Mode AlGaN/GaN HEMT inverters and ring oscillators [186], integration of silicon CMOS and GaN transistors in a current mirror circuit [187], monolithic integration of HEMT with vertical-structure LEDs [188], integration of gate driver and p-GaN power HEMT for MHz-switching [189], reverse blocking MOSHEMTs (RB-MOSHEMTs) [190], MOSHEMTs with integrated tri-anode freewheeling diodes [191], etc among many others. Companies like EPC and Navitas has commercialized discrete GaN power HEMTs and also integrated circuits with added functionalities. EPC has products like integrated gate driver ICs, E-mode HEMTs with integrated reverse gate clamp diode, E-mode HEMT half bridge ICs in addition to their wide array of discrete GaN HEMT devices catering primarily to low voltage (upto 200 V) and medium current (upto 90 A) applications like DC-DC converters, BLDC motor drives, class D audio, wireless power transfer, etc [192] (Fig.4.1a). Navitas has introduced their propreitary GaNFast ICs where an E-mode HEMT, analog gate driver and digital logic circuits all within the same chip which makes it 100x faster and 5x more energy savings than Si solutions [193] (Fig. 4.1b).

All the devices and ICs mentioned above are based on the lateral HEMT on GaN-on-Si. Since the research on vertical power devices on GaN is still in its early stages, there are almost no reports on vertical integrated power devices on GaN, to the best of our knowledge. However, similar to the case with lateral GaN power HEMTs, for practical purposes it is very beneficial to have integrated devices with additional functionalities that can greatly improve the efficiency and cost of production. Here we explore two such integration schemes, mainly;



(a) (b)

Figure 4.1 – (a) EPC2112: 200 V, 10 A Integrated Gate Driver eGaN IC. (b) Benefits of Navitas GaN power ICs.

- Quasi-vertical GaN-on-Si MOSFETs With monolithically integrated freewheeling Schottky barrier diodes [194] and,
- Quasi-vertical GaN-on-Si reverse-blocking (RB) power MOSFETs

which are described in detail in the following sections.

4.1 MOSFETs With monolithically integrated Freewheeling Schottky Barrier Diodes

In several topologies of power converters, such as buck/boost converters, voltage-source inverters, and resonant converters, where an inductive load is controlled by switches, an extra freewheeling diode is required to allow a reverse flow of current when the supply current to the load is suddenly reduced or interrupted [35]. In Si and SiC power MOSFETs, the built in body diodes are often utilized for this purpose [195, 196]. For GaN vertical MOSFETs,the intrinsic body p-i-n diode embedded in GaN vertical MOSFET structure could work as a freewheeling diode. However, its large turn-on voltage would increase the losses during switching events. One solution lies on the integration of a Schottky barrier diode (SBD) with the MOSFET, which would be preferable for efficient converter topologies due to its much smaller turn-on voltage, lower resistance, and faster switching properties [197]. Nevertheless, the large parasitic inductance of an externally connected SBD would result in circuit ringing and system instability due to the external wiring. A monolithic integration of these devices would be very desirable for a reduced footprint, smaller parasitic components, and simplified packaging [198]. But so far there have been no reports on GaN vertical transistors with monolithically integrated SBDs.

In this work, we demonstrate the first vertical GaN MOSFET with monolithically-integrated freewheeling SBD on 6-inch silicon substrates. The integrated MOSFET-SBD exhibited enhancement-mode (E-mode) operation with a threshold voltage (V_{th}) of 3.9 V, an on/off ratio of over 10^8, and a drastic improvement in reverse conduction, without degradation in on-state performance of the MOSFET. The integrated SBD exhibited excellent performance, with a specific on $R_{on,sp}$ of

1.6 mΩcm^2, a turn-on voltage of 0.76 V, an ideality factor of 1.5, along with a state-of-the-art breakdown voltage of 254 V compared to vertical GaN-on-Si SBDs. These results reveal the great potential of GaN-on-Si vertical MOSFETs with integrated freewheeling SBD for power converters. The results mentioned here are based on our paper [1].

4.1.1 Device structure and Fabrication

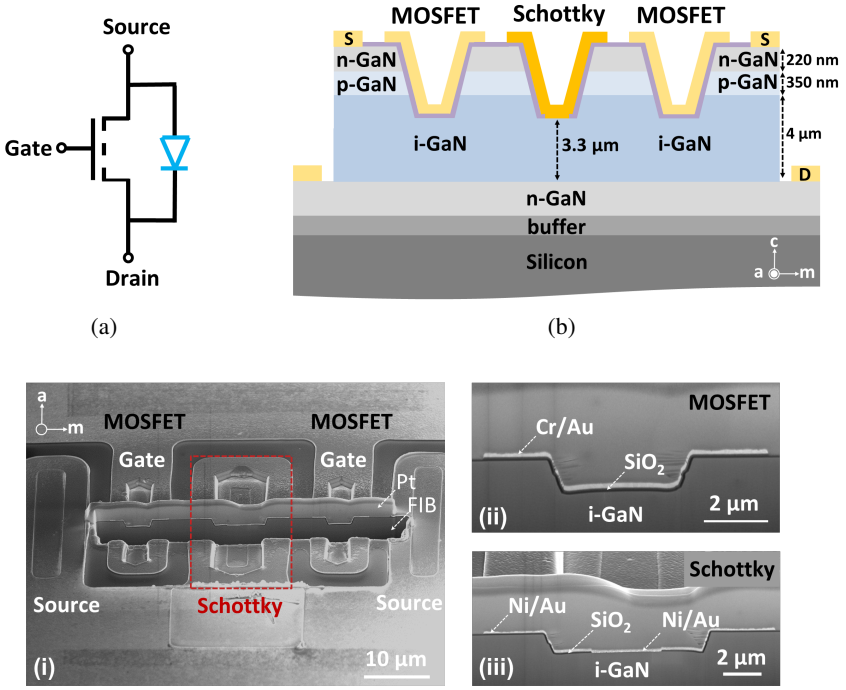
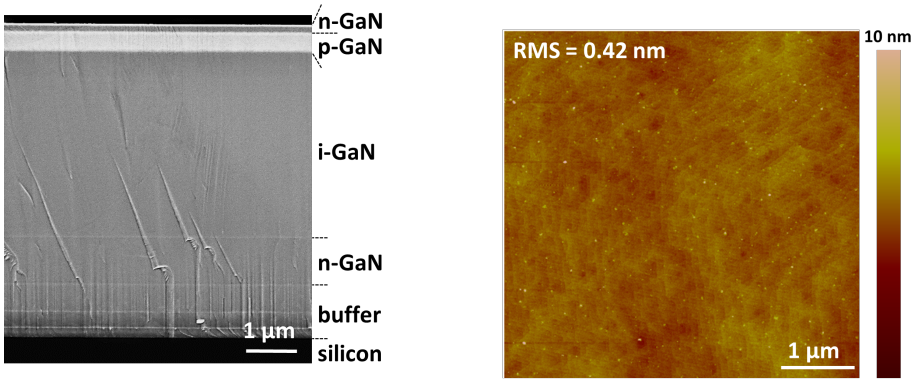


Figure 4.2 – (a) Equivalent circuit, (b) Schematic of integrated vertical MOSFET-Schottky barrier diode (SBD). (c) SEM image of integrated vertical MOSFET-SBD (i) with cross-sectional SEM image of the integrated vertical MOSFET (ii), and of the integrated vertical SBD (iii).

Fig. 4.2a depicts an equivalent circuit of the monolithically integrated vertical MOSFET-SBD, along with a cross-sectional schematic presented in Fig. 4.2b. Both the integrated vertical MOSFET and SBD feature a trench structure along the a-axis of GaN. A tilted-view scanning electron microscope (SEM) image of the integrated vertical MOSFET-SBD is shown in Fig. 4.2c(i). The etched middle region corresponds to a crosssectional cut by focused ion beam (FIB). It shows the anode of the SBD integrated in the source pad of the MOSFET, while the cathode is directly connected to the MOSFET drain through the bottom n-GaN layer. As a result, the interconnection metal wires between the MOSFET and SBD could be eliminated, leading to a minimized footprint, reduced parasitic components, and enhanced switching speed. Fig. 4.2c(ii) and Fig. 4.2c(iii) show the cross-sectional SEM images of the integrated MOSFET and SBD,

[1] C. Liu, R. A. Khadar, and E. Matioli, "Vertical GaN-on-Si MOSFETs With Monolithically Integrated Freewheeling Schottky Barrier Diodes," IEEE Electron Device Letters, vol. 39, no. 7, pp. 1034–1037, Jul. 2018. Contribution: Second author, contributed to design, fabrication and simulation of these devices.

respectively. The depth of the etched trench was 1.3 µm for both devices, which was sufficient to reach the i-GaN drift layer. A direct contact of the Schottky metal (Ni/Au) to the i-GaN drift layer can be observed in Fig. 4.2c(iii), which forms the integrated vertical SBD. The cross-sectional



(a) (b)

Figure 4.3 – (a) Cross-sectional SEM image of the as-grown n-p-i-n GaN structure on 6-inch silicon, (b) AFM image of the Schottky region after dry-etching to reach the n-GaN layer, followed by 25% TMAH treatment at 85 °C for 90 min.

SEM image of the n-p-i-n epitaxial structure grown on 6 inch Si (111) in Fig. 4.3a shows a total thickness of 6.7 µm, with abrupt junction interfaces and a drift layer thickness of 4 µm. The device fabrication started with a plasma-based dry etching process to form the trench structures for the vertical MOSFET and SBD. The samples were then treated with a 25% Tetra Methyl Ammonium Hydroxide (TMAH) solution at 85 °C for 90 minutes to smooth the sidewall and bottom of the etched trenches [170]. Fig. 4.3b reveals the very smooth surface morphology of the trench bottom after TMAH treatment, with a root-meansquare (RMS) roughness of 0.42 nm, which is crucial to achieve good Schottky contacts. More details of the epitaxial structure and fabrication process used in this work can be found in Chapter 3.

4.1.2 Results and Discussion

The output characteristics (I_{DS}-V_{DS}) of the integrated MOSFET-SBD and discrete reference MOSFET are shown in Fig. 4.4a. Both devices presented good saturation behavior, an on-state current density of ~ 0.35 kA/cm^2, and a similar $R_{on,sp}$(19.1 mΩcm^2 and 24 mΩcm^2, normalized by the trench area including 2µm on all sides to account for current spreading). The difference in $R_{on,sp}$ is within the variation observed for devices of the same kind in this wafer. Fig. 4.4b plots the transfer characteristics (I_{DS}-V_{GS}) of the integrated MOSFET-SBD and discrete MOSFET at V_{DS} = 10 V. Both devices exhibited E-mode operation with a V_{th} (obtained by linear extrapolation) of ~ 3.9 V, a current on/off ratio of over 10^8, and a sub-threshold swing (SS) of ~ 218 mV/dec. The off-state leakage current level of the integrated MOSFET-SBD is slightly higher as compared to the discrete MOSFET. This can be attributed to the integrated SBD, which is under reverse bias during forward operation of the integrated MOSFET. Despite this, the overall leakage current level value for the integrated MOSFET-SBD was below 10^{-8} kA/cm^2, revealing a very effective

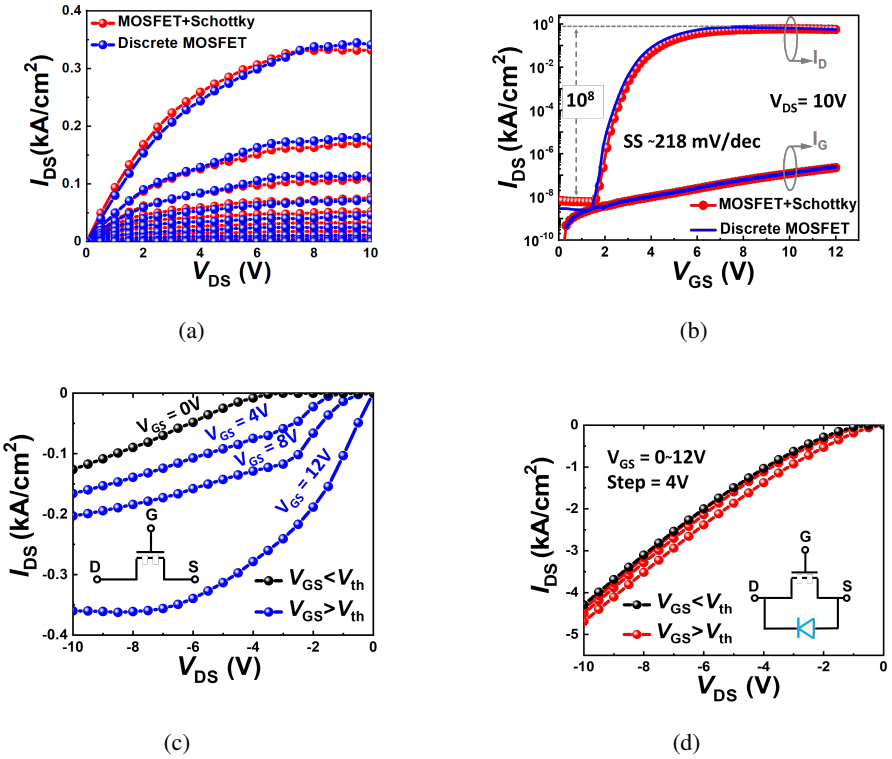
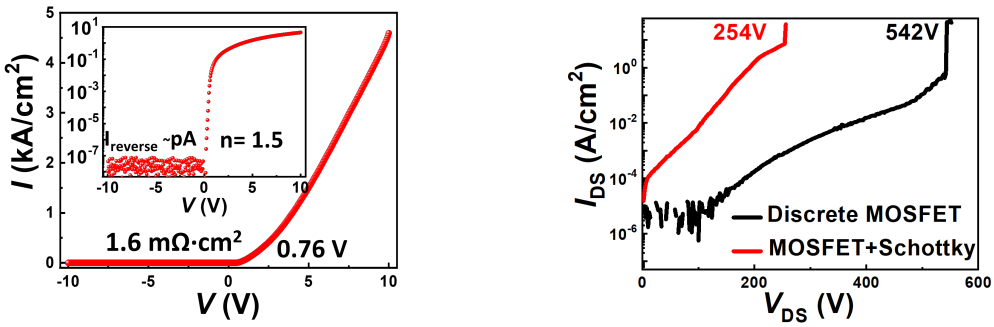


Figure 4.4 – (a) Output and (b) Transfer characteristics of the vertical MOSFET with/without integrated freewheeling SBD with V_{GS} ranging from 1-10 V in steps of 1 V. Reverse-bias characteristics of (c) the discrete vertical MOSFET and (d) integrated vertical MOSFET-SBD

current blocking from the integrated MOSFET-SBD in off state. The minor gate leakage increase, from 6×10^{-10} kA/cm^2 at V_{GS} = 0 V to 2×10^{-7} kA/cm^2 at V_{GS} = 12 V, can be eliminated by improving the quality and conformity of gate dielectric.

Fig. 4.4c illustrates the reverse characteristics of the discrete vertical MOSFETs. In the on-state ($V_{GS} > V_{th}$), the current flows through the MOSFET channel from source to drain with an $R_{on,sp}$ of 18 mΩcm^2, comparable to that in the forward conduction. In the off-state ($V_{GS} < V_{th}$), the current in the MOSFET channel is blocked, resulting in a large V_{ON} of -3.7 V, corresponding to the built-in p-i-n diode, as well as a high resistance in the reverse current path. In this case, a voltage spike could occur during switching, causing arcing on contacts or possibly destroying transistors. The reverse characteristics of the integrated MOSFET-SBD are depicted in Fig. 4.4d. A drastically improved reverse conduction is observed in off-state ($V_{GS} < V_{th}$), thanks to the integrated anti-parallel SBD. In the reverse condition, the electrons can flow through the drift region via the Schottky contacts to the source, even if the channel under the MOSFET gate is pinched-off. In on-state ($V_{GS} > V_{th}$) of the integrated MOSFET, an additional current can flow through the MOSFET channels from drain to source, which explains the minor gate modulation observed and adds to the forward current of the integrated SBD. Fig. 4.5a shows the forward current density (normalized by the anode area) versus voltage (I-V) characteristics of the SBD.



(a) (b)

Figure 4.5 – (a) I-V characteristics of the integrated SBD. The inset shows semi-log scale of the I-V curves, and (b) Off-state breakdown characteristics of the integrated vertical MOSFET-SBD and of discrete MOSFET.

The V_{ON}, extracted at a current density of 20 A/cm^2 was 0.76 V, which is among the lowest values reported in vertical GaN diodes so far [199]. The $R_{on,sp}$ extracted from the forward I-V plot at 8.7 V was 1.6 mΩcm^2. The inset plots the forward current density I in logarithmic scale as a function of bias. A small ideality factor of 1.5 was extracted at a forward voltage of 0.4 V, together with an extremely low reverse current, in the range of pA. A combination of such low $R_{on,sp}$ and good ideality factor is a result of the excellent drift-layer quality with low defect density, high electron mobility [106], as well as excellent Schottky contact formed on the smooth i-GaN surface subject to TMAH treatment. Fig. 4.5b plots the off-state I_{DS}-V_{DS} characteristics measured at a V_{GS} = 0 V for the discrete vertical MOSFET and integrated vertical MOSFET-SBD. The discrete vertical MOSFETs exhibited a large breakdown voltage (BV) of 542 V, while the integrated vertical MOSFET-SBD presented a BV of 254 V, which was limited by the BV of the integrated SBD.

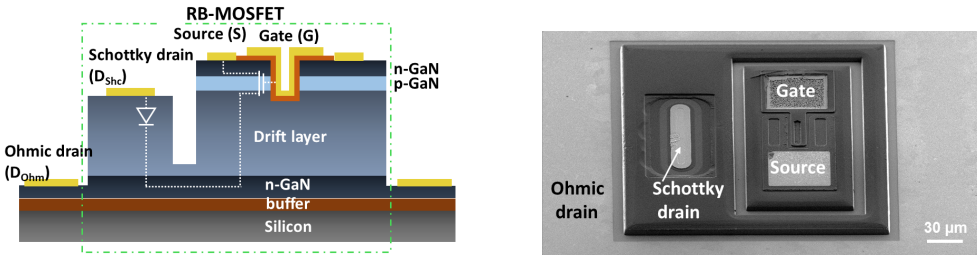
4.2 GaN-on-Si reverse blocking (RB) MOSFETs

Several applications demand reverse-blocking (RB) capability from power transistors, such as in protection systems against reverse battery connections as well as negative voltage pulses appearing at the drain electrode [200–202]. Moreover, by connecting two antiparallel RB transistors, it is possible to obtain low-loss bidirectional switches, which find applications, among others, in matrix converters [203], multilevel inverters [204] and battery management systems [205]. Si IGBTs and SiC MOSFETs with RB capability have been proposed in previous years [206, 207]. Recently, monolithically-integrated bidirectional switches based on normally-off GaN high-electron mobility transistors (HEMTs) have been also demonstrated [208, 209], exhibiting unrivalled performance in bidirectional converters [208, 210] thanks to the high critical electric field and high mobility of AlGaN/GaN heterostructures [211]. Nevertheless, similarly to conventional normally-off GaN HEMTs, they also suffer from low threshold voltage V_{th} (< 2 V) that may not be compatible with practical circuit designs.

On the other hand, a high V_{th} can be easily obtained in vertical GaN MOSFETs which, compared to lateral AlGaN/GaN transistors, also present a lower sensitivity to surface trap states, hence mitigating the current collapse issues. In addition, vertical devices can potentially hold larger voltages by increasing their drift-layer thickness, thus enabling more devices per wafer [58].In this work, we demonstrate a vertical GaN-on-Si MOSFET with RB capability by monolithically integrating a Schottky diode at the drain contact of a quasi-vertical GaN MOSFET. The quasi-vertical configuration enables a simple monolithic integration of devices, while benefiting from the vertical architecture. The proposed devices, based on a 6.7 µm-thick n-p-i-n GaN epitaxial structure grown on 6-inch Si wafers, exhibit a specific on-state resistance $R_{on,sp}$ as small as 4.5 mΩcm^2, and excellent forward and reverse blocking voltages of 570 V and ~ 300 V respectively, with no degradation observed in the forward current conduction compared to a conventional quasi-vertical GaN MOSFET with ohmic drain. High-quality Schottky drain contacts on dry-etched i-GaN were obtained upon surface treatment with tetramethylammonium hydroxide (TMAH), presenting an ideality factor close to unity and an I_{ON}/I_{OFF} ratio of ~ 10^9. This represents state-of-the-art performance comparable to GaN Schottky diodes [100, 101, 199, 212]. These promising results show the potential of GaN-on-Si RB-MOSFETs as power devices, as well as showcase the potential integration of vertical devices on a low-cost GaN-on-Silicon platform. The results are from our recently submitted paper [2].

4.2.1 Device structure and fabrication

The n-p-i-n structure used for device fabrication is the same which is described in Chapter 3.The device fabrication is similar to that of the quasi-vertical MOSFET mention in Chapter 3 except for the additional steps involving the fabrication of the Schottky drain. The Schottky drain region was formed by etching away the top n- and p-GaN layers by ICP-RIE followed by 25% TMAH treatment at 85 °C to smoothen the dry-etched surface for 3 hrs. The RMS roughness after TMAH improved from 2.49 nm to 0.59 nm, which is pivotal towards achieving a low-leakage and high-quality Schottky contact. Subsequently, a 4 µm-deep GaN etch was made around the gate and source terminals to partially isolate the Schottky drain (Fig. 4.6a). Fig. 4.6b shows the tilted-view SEM image of the fabricated RB-MOSFET.



(a) (b)

Figure 4.6 – (a) Schematic of an RB-MOSFET. (b) Tilted view SEM of a fabricated RB-MOSFET.

[2] "Quasi-vertical GaN-on-Si Reverse-Blocking (RB) power MOSFETs", R. A. Khadar, A. Floriduz, C. Liu, R. Soleimanzadeh and E. Matioli, submitted to IEEE EDL. Contribution: First author.

4.2.2 Results and Discussion

The quality of the Schottky contact forming the Schottky drain in an RB-MOSFET is of paramount importance for its performance, and this is particularly challenging on an etched GaN surface. This issue was addressed by the 3h-long TMAH treatment at 85 °C right after etching. Fig. 4.7a shows the atomic force microscopy (AFM) image of the etched i-GaN surface after TMAH treatment revealing a smooth surface with low RMS roughness of 0.59 nm, which is ideal for the realization of a good Schottky contact. The current density-voltage (I-V) characteristics of the Schottky diode formed between the Schottky and ohmic drain contacts revealed excellent performance with turn-on voltage ($V_{\text{turn-on}}$) of 0.7 V at 30 A/cm^2, very high current density $I >$ 10 kA/cm^2 at 9 V and ultra-low specific on-resistance ($R_{\text{on,sp}}$) of 0.6 mΩcm^2 at 7 V (Fig. 2(b,c)). The diode also presented a very low ideality factor (η) of 1.13 at 0.4 V and an excellent ON-OFF ratio ($I_{\text{ON}}/I_{\text{OFF}}$) of $\sim 10^9$ (Fig. 2(b)). A Schottky barrier height ($q\phi_B$) 0.66 eV was extracted at the Ni/i-GaN interface from the I_0/T^2 vs 1000/T plot (Fig. 2(d)) following the equation: $ln\left(\frac{I_0}{T^2}\right) = \frac{q\phi_B}{kT} + ln(AA*)$ where I_0 is the saturation current density, A is the area of the Schottky contact, $A*$ is Richardson's constant, q is the elementary charge, and k the Boltzmann's constant. The low ideality factor of 1.13 at 0.4 V demonstrates the high quality of the Ni/i-GaN interface and the effectiveness of TMAH in smoothening out the surface. This exceptional ON-state performance is comparable with the best reported SBDs on bulk GaN [100, 101, 199, 213] and GaN-on-Si [141, 212].

Fig. 4.8a presents the comparison of output characteristics of the RB-MOSFET measured using the Schottky and ohmic drain contact, normalized by the gate trench area of 10 µm × 34 µm after accounting for a lateral current spreading of 2 µm from all the sides of the gate trench. Even though the Schottky drain is electrically at twice the distance of the i-GaN thickness from the source, both contacts provided similar high output current densities of ~ 0.9 kA/cm^2 and $R_{\text{on,sp}}$ of 4.43 mΩcm^2 at V_{DS} of 0.9 V with ohmic drain and 4.75 mΩcm^2 at V_{DS} of 0.9 V, with the Schottky drain. This is because the extra 4 µm thickness of i-GaN adds only 0.17 mΩcm^2 to the $R_{\text{on,sp}}$ according to the relation $R = \frac{t}{q\mu N_{\text{D}}}$, where t, μ and N_{D} are the thickness, mobility and carrier concentration of the i-GaN layer [213]. The device also presented excellent transfer characteristics (I_{DS}-V_{GS}) as shown in Fig. 4.8b and 4.8c. A threshold voltage (V_{th}) of ~ 6.5-7 V was obtained by linear extrapolation at an I_{DS} of ~ 50 A/cm^2 on both curves. Negative hysteresis of ~ 1.5-2 V were observed in the I_{DS}-V_{GS} curves for both ohmic and Schottky drain, which is possibly due to bulk oxide traps [182], and could be improved by post-deposition annealing.

The RB-MOSFET exhibited an excellent V_{RB} of ~ 300 V at a V_{GS} of 15 V (ON-state), and V_{RB} of 570 V at a V_{GS} of 0 V (OFF-state) (Fig. 4.9a). The low leakage current in the forward blocking operation exhibited a linear dependence with the applied voltage, which is an indication of variable-range hopping mechanism [175]. The device also presented a small leakage current in the reverse blocking operation and the increase in leakage current between -130 V and -300 V is due to thermionic field emission (TFE)) [101]. As evident from Fig. 4.9b, the inclusion of a Schottky drain improves the reverse leakage current by over 10^7 times as compared to the ohmic drain of a conventional MOSFET, thus providing superior protection against negative voltage spikes. The gate leakage (I_{G}) remained below 10^{-4} A/cm^2 during both sets of measurements. The

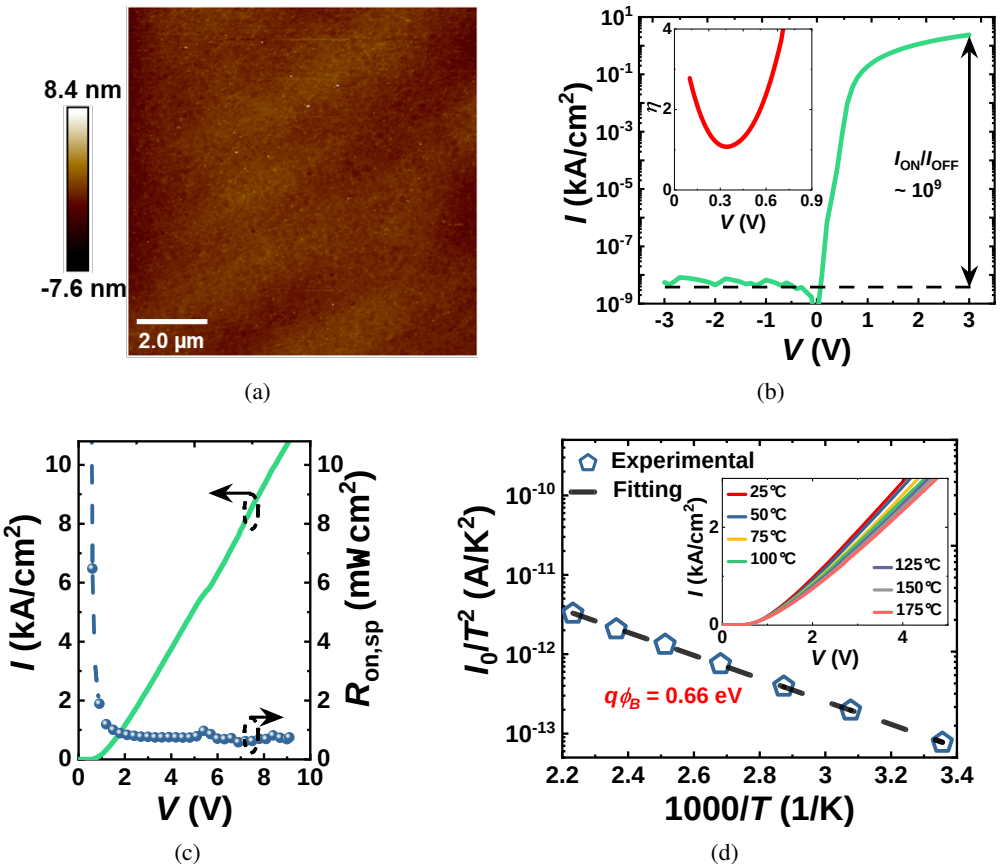


Figure 4.7 – (a) AFM image of the Schottky drain surface of area 10 µm × 10 µm after TMAH treatment. (b) I-V characteristics of the Schottky diode formed by Schottky drain (anode) and ohmic drain (cathode) in semi-log scale and ideality factor (η) in inset figure. (c) I-V characteristics (linear scale) of the Schottky diode and $R_{\text{on,sp}}$. (d) Richardson's plot for extraction of SBH. Inset figure shows the I-V-T characteristics in linear scale.

TCAD simulation of RB-MOSFET at a V_{DS} of -200 V and V_{GS} of 15 V (Fig. 4.9c) demonstrates the blocking capability of the Schottky drain (evident from the low current density at the drain contact. We also investigated the effect of isolation mesa depth (d_m) on the V_{RB} using TCAD simulation (Fig. 4.9d), and observed V_{RB}'s consistent with our fabricated device. A deep isolation mesa effectively increases the distance between the Schottky drain and the source and thus improves the V_{RB}.

The V_{RB} can be significantly improved by implementing a TMBS structure [83] for the Schottky drain as shown in Fig. 4.10a . Fig. 4.10b presents the variation of leakage current and VRB with the trench depth (d_t) of the TMBS structure. The leakage current reduces with increasing the d_t due to improved depletion of electrons in the TMBS i-GaN pillar. The best V_{RB} was obtained for a d_t of 1 µm and reduces thereafter as electric field peaks at the bottom corner of the TMBS SiO_2, thereby resulting in premature breakdown.

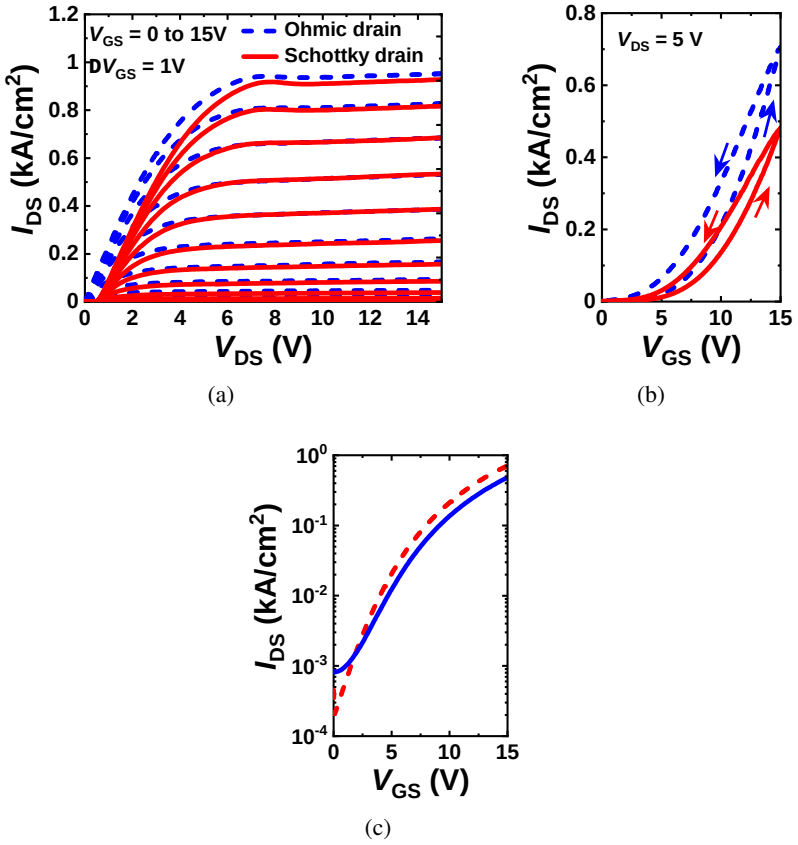


Figure 4.8 – (a) I_{DS}-V_{DS} characteristics of the RB-MOSFET with Schottky and ohmic drain. (b) Transfer characteristics of the RB-MOSFET. (c) Transfer characteristics in semi-log scale.

4.3 Conclusion

In summary, monolithic integration of power devices leads to reduced parastics, which improve the overall efficiency of the power system. In this chapter we discussed about two such integrations for vertical power devices. First, we demonstrated how a free wheeling diode can be integrated with a quasi-vertical power MOSFET to provide a path for reverse current to flow to release the stored inductor energy at switching events. The integrated SBD in this work was benchmarked against state-of-the-art vertical SBDs on silicon, sapphire and GaN substrates in Fig. 4.11, revealing state-of-the-art performance compared to vertical GaN-on-Si SBDs [75–77, 81, 141, 199, 213–219]. The V_{BR} of the integrated MOSFET-SBD can be significantly improved:

- By using low-defect-density GaN substrates [75, 199, 218];
- By increasing the drift layer thickness and further reducing the background carrier concentration from 2×10^{16}cm^{-3} in this work to $\sim 10^{15}$cm^{-3} [77, 213];
- By employing field plate, edge termination, and guard ring technologies [76, 217, 219];
- By utilizing trench or junction SBD architecture [81, 83].

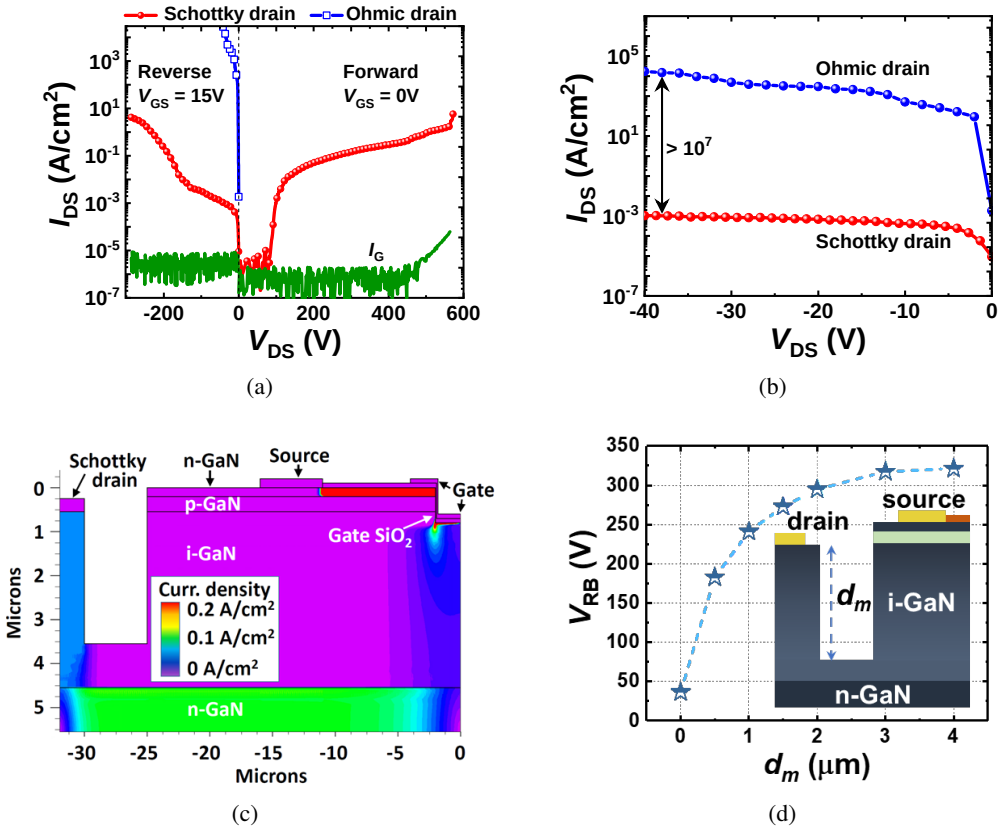


Figure 4.9 – (a) Measured forward and reverse blocking performances. (b) Measured reverse blocking performance using Schottky and ohmic drain contacts. (c) Simulation of reverse blocking capability of the RB-MOSFET clearly showing the current density distribution at V_{DS} = -200 V and V_{GS} = 15 V.(d) Variation V_{RB} with d_m obtained from simulations.

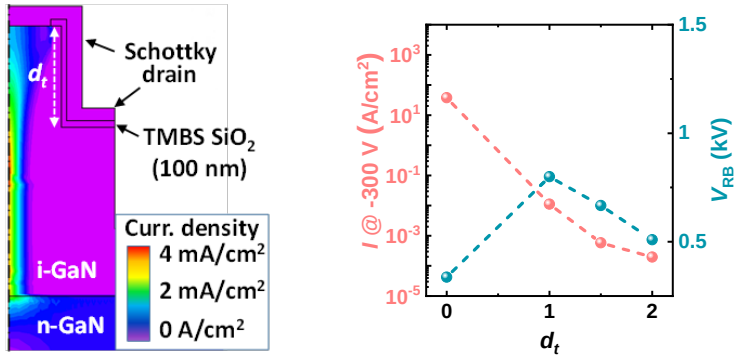


Figure 4.10 – (a) Simulation of current density distribution @ -300 V in the TMBS structure. (b) Variation of reverse leakage current and VRB with d_t.

Next, we saw how we could provide protection to discrete MOSFETs by introducing a Schottky

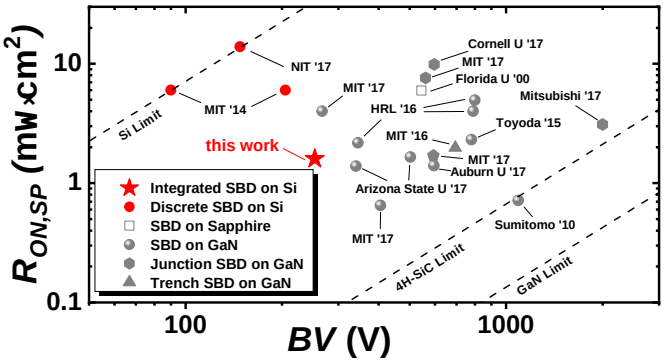


Figure 4.11 – $R_{on,sp}$ versus BV benchmark of the vertical SBD against state-of-the-art vertical SBDs on Si, sapphire and GaN substrates.

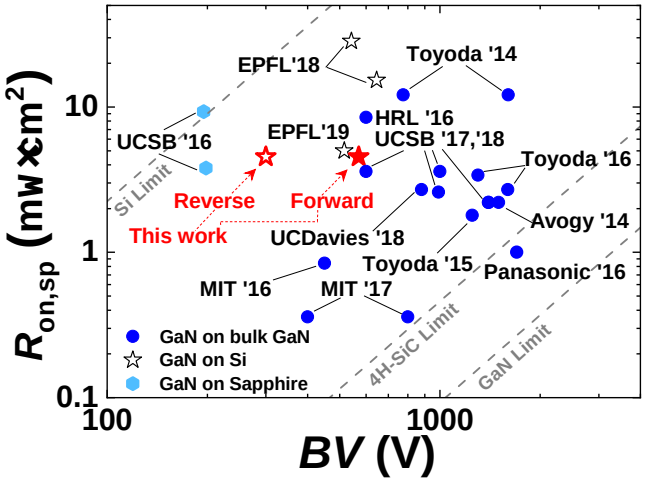


Figure 4.12 – $R_{on,sp}$ versus V_{BR} benchmark of the RB-MOSFET against other reported GaN vertical transistors on bulk GaN, sapphire and Si substrate.

contact to the drain terminal to form a reverse blocking (RB) MOSFET. Finally, the RB-MOSFET was benchmarked against other GaN vertical MOSFETs fabricated on bulk GaN, sapphire and on Si substrates [87, 93–97, 120, 164, 180, 220–223] as shown in Fig. 4.12. The RB-MOSFET simultaneously offers high forward and reverse blocking voltages, thus eliminating the need of a discrete transistor in series with an SBD. The proposed quasi-vertical RB-MOSFET enables a reduction in the device size and parasitics, and illustrates the potential of monolithic integration of vertical and, possibly, lateral devices on GaN-on-Si platform.

5 p-type NiO/GaN heterostructures

P-type doped layers are an indispensable part of high-performance p-i-n diodes, SBDs as well as power MOSFETs. In p-i-n diodes, they form the p-layer which plays an integral part in reducing the $R_{on,sp}$ by conductivity modulation (injection of holes into the i-type layer) and provides an energy barrier in the OFF-state. In SBDs, p-doped layers are commonly used as junction termination extension (JTE) structures which improve the BV and reliability, and also as p-doped pockets for junction barrier Schottky (JBS) and merged p-i-n Schottky diodes. For MOSFETs, p-doped layers form the channel region of enhancement mode n-channel MOSFETs. They also provide blocking capability similar to a p-i-n diode under OFF-state. Furthermore, p-doped layers are quintessential for achieving avalanche capability for power devices.

The discovery of p-type doping and dopant activation in GaN revolutionized the LED industry so much that the researchers responsible for this discovery were awarded the 2014 Nobel prize for Physics [224]. In GaN, p-type doping is usually achieved during MOCVD growth by flowing the Cp_2Mg precursor which dopes the GaN p-type with Mg. However this doping process is not very straightforward. The Mg atoms from the precursor reacts with hydrogen atoms released from the NH_3 source to form stable Mg-H complex. As a result, the as-grown p-GaN requires an activation annealing at high temperatures close to 750 °C to break the Mg-H bond so that the Mg atoms can take part in doping the GaN. Even so, the activation efficiency is normally only around 1 % [225, 226]. While this hasn't hindered the development and wide commercialization of LEDs, for power devices, this low activation efficiency is not that desirable. A high Mg doping of around 10^{19} /cm^3 is required to provide a net hole concentration of 10^{17} /cm^3 which is required for most power applications. The un-activated dopant atoms scatter the holes and thus results in poor hole mobility of around 20-25 cm^2/Vs. This increases the $R_{on,sp}$ in the case of p-i-n diodes and for MOSFETs where p-GaN forms the channel region, this high concentration of un-activated dopant atoms result in scattering of the inversion channel electrons thus reducing their field effect mobility. There are also pertinent issues related to the selective p-type doping of GaN. Si and SiC devices rely on ion implantation to form selectively doped p/n regions catering to a particular design of the device. For GaN, doping by ion implantation is still at an infancy stage and the very few methods which work, rely on high temperature (> 1200 °C) and/or high pressure (~ 1 GPa) treatments [80, 227]. Selective area re-growth by metalorganic chemical vapor deposition

(MOCVD) is also very difficult due to the presence of a high concentration (> 10^{18} cm^{-3}) of Si atoms at the interface of the regrown GaN, leading to large leakage currents [72, 228] in addition to substantially increasing costs.

In this work, we evaluated the use of highly-doped RF-sputtered p-type NiO as a possible replacement for p-type GaN in p-i-n diodes and JTEs. We demonstrated this technology on quasi-vertical devices on GaN-on-Si substrates due to their low-cost and large-scale availability, up to 12 inches. First, we investigated the electrical behavior of a p-NiO/i-GaN/n-GaN heterojunction diode which revealed excellent forward characteristics, with on-resistances similar to that of a GaN p-i-n diode, but with much lower turn-on voltage, together with holding high peak electric fields in reverse bias. Next, we explored this conductive p-NiO as JTEs for Schottky barrier diodes (SBD). An SBD with a single zone JTE presented an ON-state behavior similar to a control SBD without any termination, while significantly improving the BV. The results of this work has been recently submitted to IEEE EDL [1].

5.1 Device structure and Fabrication

The SBD epitaxial structure consisted, from bottom to top, of 1.07 µm-thick buffer layer, 1 µm-thick n-GaN ($N_D \sim 1\times 10^{19}$ cm^{-3}) and 4 µm-thick i-GaN ($N_D \sim 2\times 10^{16}$ cm^{-3}). All the GaN layers were grown by MOCVD on a 6-inch Si (111) by Enkris semiconductors. The fabrication process started with the deposition of p-NiO by RF-sputtering to form the p-layer of the p-i-n heterojunction diode and the JTE region for the SBD, followed by lift-off. The RF sputtering was done at room temperature with RF bias of 150 W, chamber pressure of 0.4 Pa, and Ar + O_2 ambient with a flux ratio of 3:1. Ni/Au (200/150 nm) bilayer was then deposited to form ohmic contact to p-NiO and also to serve as Schottky contact to i-GaN for the control SBD and the SBD with JTE. This was followed by deep-etched mesa isolation using inductively coupled plasma-reactive ion etching (ICP-RIE) to access the bottom conductive n-GaN layer. Cr/Au (50/250 nm) was then deposited for ohmic contact to n-GaN. The schematic of the various types of devices along with a focused ion beam microscopy image of their anode region is shown in Fig. 5.1.

5.2 Results and Discussion

The bandgap of p-NiO was elucidated from optical transmittance measurements on a thin film of NiO (60 nm) deposited on a transparent fused silica glass (Fig. 5.2a). X-ray photoelectron spectroscopy (XPS) measurements were also carried out on NiO layers deposited on a similar GaN wafer used for the device fabrication, under the same deposition conditions, to obtain the values for the conduction and valence band offsets (ΔE_c and ΔE_v). A type-II band-alignment was thus observed at the p-NiO/i-GaN interface with a built-in potential of 1.48 V as shown in Fig. 5.2b. A hole concentration of 2 × 10^{20} cm^{-3} and a hole mobility of 0.23 cm^2/Vs were extracted for the p-NiO layer using Hall measurements. Considering a hole effective mass of 0.8

[1] "p-NiO/GaN heterostructures for p-i-n diodes and junction termination extensions", R. A. Khadar, A.Floriduz, T. Wang, C. Erine, R. V. Erp, L.Nela, R. Soleimanzadeh, P. Sohi and E. Matioli, submitted to IEEE EDL. Contribution: First author.

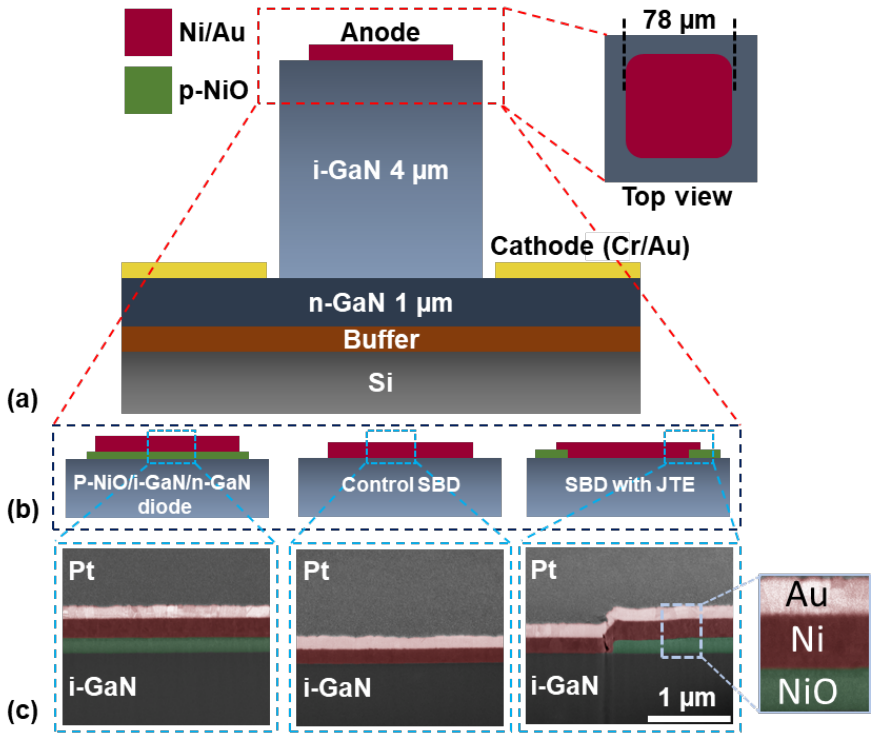


Figure 5.1 – (a) Schematic structure of the diodes presented in this work. (b) Schematic representation of the anode region corresponding to the fabricated p-NiO/i-GaN/n-GaN diode, SBD without JTE and with JTE. (c) Focused ion-beam (FIB) cross-sectional SEM images of the regions marked in (b).

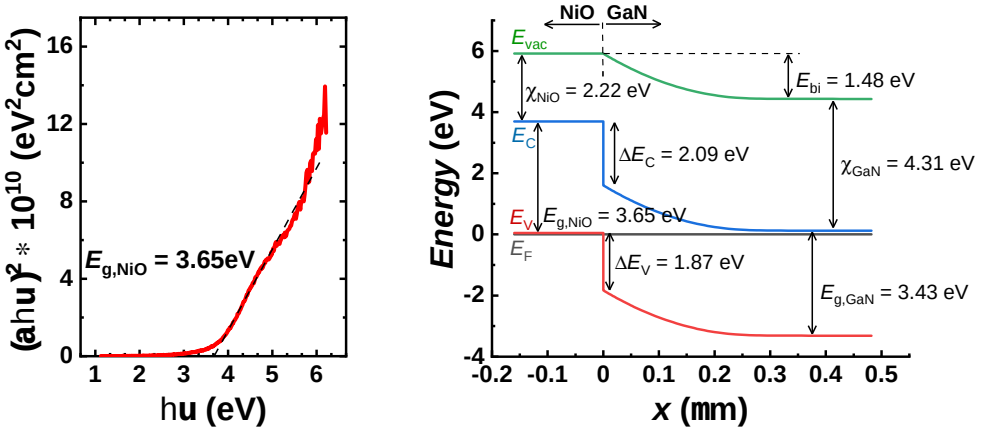


Figure 5.2 – (a) Absorption spectrum and extracted band-gap of p-NiO obtained from the transmittance measurements. (b) Experimentally obtained energy band diagram at zero bias of the p-NiO/i-GaN heterojunction.

m_0, where m_0 is the electron rest mass, and assuming a spherical parabolic two-band model, the effective valence band density of states for the p-NiO is calculated as 1.81×10^{19} cm^{-3} [229]. Thus with a hole concentration of 2×10^{20} cm^{-3}, the p-NiO is degeneratively doped as shown in Fig. 2(b). The origin of this high hole concentration is believed to be due to the formation of Ni3+ from Ni2+ nearby Ni vacancies, by reaction with excess oxygen atoms, thus creating holes localized on the Ni sites [230, 231]. These localized holes form 'large polarons' which follow a band-like transport as opposed to 'small polarons' which follow a thermally-activated hopping mechanism leading to much lower hole mobilities « 0.1 cm^2/Vs [232, 233].

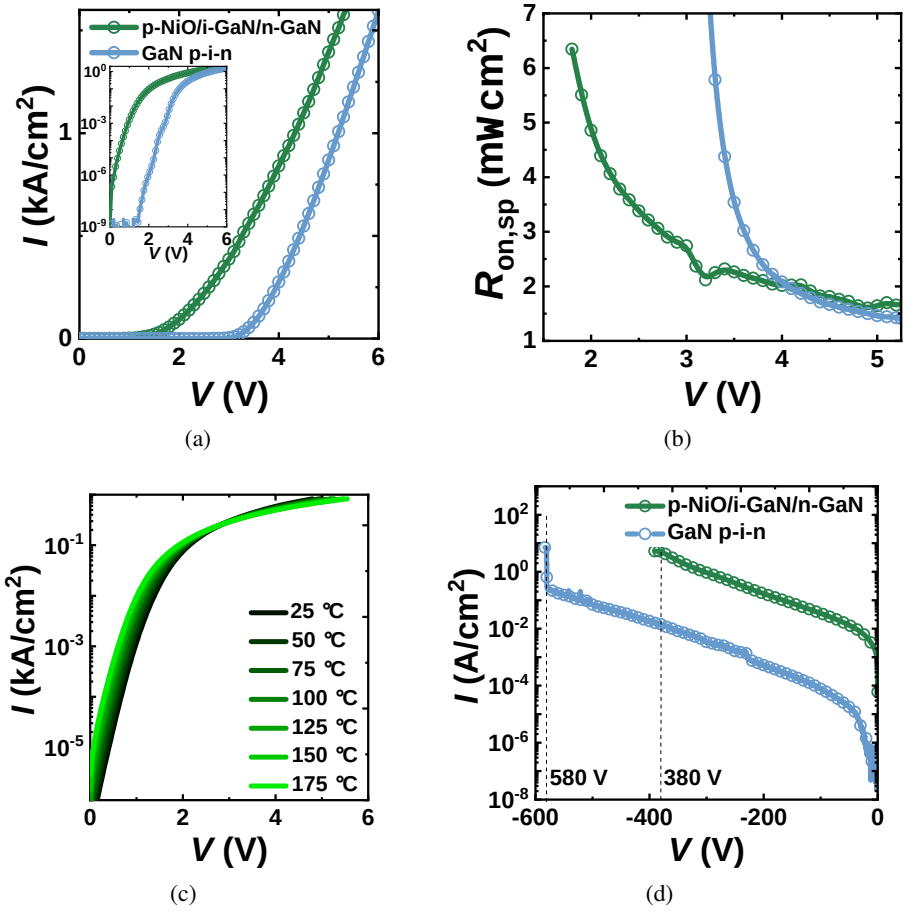


Figure 5.3 – (a) Comparison of $I-V$ charateristics of the p-NiO/i-GaN/n-GaN diode and the GaN p-i-n diode. The inset shows the $I-V$ curves in semi-log scale. (b) $R_{\text{on,sp}}$ vs V plot for both the diodes. (c) $I-V-T$ curves for the p-NiO/i-GaN/n-GaN diode. (d) Reverse breakdown performance of both the diodes. The legend of (b) is the same as (a) and (d)

Fig. 5.3a presents the forward $I-V$ characteristics of the p-NiO/i-GaN/n-GaN heterojunction diodes compared to a GaN-on-Si p-i-n diode, similar to the one reported in [1] but with no passivation and field plate. The p-NiO/i-GaN/n-GaN diode presented a much smaller turn-on voltage ($V_{\text{turn-on}}$) of 1.6 V as compared to 3.3 V for the GaN p-i-n diode, both extracted at a current density of 30 A/cm^2. Such low $V_{\text{turn-on}}$, consistent with the built-in potential of 1.48

V, would suggest interface trap recombination [234] as the main conduction mechanism of the forward current (Fig. 5.3a), analogous to what has already been proposed for NiO/β-Ga_2O_3 heterojunctions [235, 236]. However, this model invariably predicts an ideality factor (η) of 2 [234], while in our case an η = 4.3 was observed at 0.6 V, indicating that tunneling plays a non-negligible role in the forward current. Indeed, we believe that our experimental data can be explained by a tunneling-enhanced interface trap recombination mechanism [237], which has been previously applied to Cu(Ga,In)Se_2 type-II heterojunctions. In this model, the ideality factor can assume values > 2 and can be expressed as $\eta=\frac{E_{00}}{k_BT}coth\frac{E_{00}}{k_BT}$ [238], where E_{00} is a characteristic energy representing the tunneling barrier transparency; in our case, we determined E_{00}=109 meV. A nearly similar low $R_{on,sp}$ of 1.6 mΩ cm^2 and 1.4 mΩ cm^{2}2 were extracted for the p-NiO/i-GaN/n-GaN diode and the GaN p-i-n diode at 4.9 V, revealing the excellent transport at the heterojunction (Fig. 5.3b). The current was normalized by the anode area including 10 μm on all sides to account for current spreading. Fig. 5.3c shows the temperature dependence of the p-NiO/i-GaN/n-GaN heterojunction p-i-n diode in a semi-log scale, demonstrating its excellent stability till 448 K. The reduction in $V_{turn\text{-}on}$ at higher temperatures is due to a decrease in barrier width as a result of thermal diffusion of holes [239]. The p-NiO/i-GaN/n-GaN diode presented a reasonable BV of 380 V (corresponding to a peak electric field of 1.8 MV/cm, obtained from TCAD simulations), which is however lower than the 580 V observed for the GaN p-i-n diode, in addition to a higher leakage current (Fig. 5.3d. These observations are understandable due to the higher trap density present at the p-NiO/i-GaN interface, resulting in a larger leakage current by trap-mediated tunneling [237, 240]. This could be alleviated by exploring different deposition conditions like reducing the RF power during sputtering, and also by improving the sample surface cleaning [230]. Nevertheless, the p-NiO/i-GaN/n-GaN diode provides excellent ON- and OFF- state performance, comparable to a GaN p-i-n diode. In addition, in this work the p-NiO was used as a substitute for p-GaN in a simple JTE as shown in Fig. 5.1. Fig. 5.4a presents the ON-state characteristics of the SBD with p-NiO JTE and that of the control SBD. Both diodes presented similar $V_{turn\text{-}on}$ of 0.7 V at 30 A/cm^2, and $R_{on,sp}$ of 3 mΩ cm^2 for the SBD with JTE and 3.7 mΩ cm^2 for the control SBD (Fig. 5.4b). The lower $R_{on,sp}$ for the SBD with JTE is due to the additional current conduction through the JTE, similar to the p-NiO/i-GaN/n-GaN diode described before. The SBD with JTE presented a higher ideality factor of 1.4 at 0.5 V as opposed to 1.1 at 0.5 V for the control SBD, which is believed to be due to recombinations happening at the p-NiO/i-GaN interface of the JTE during forward conduction. A Schottky barrier height ($q\phi_B$) of the Ni/i-GaN Schottky contact of 0.67 eV was extracted from the I_0/T^2 vs 1000/T plot obtained from temperature-dependent measurements (Fig. 5.4c). As observed from Fig. 5.4d, the inclusion of a p-NiO JTE significantly improved the BV from 270 V, for the control SBD, to 430 V corresponding to a peak electric field of 1.9 MV/cm as compared to 1.3 MV/cm at 270 V for the SBD without JTE. This 1.6x-improvement in BV is due to the effectiveness of the p-NiO JTE in spreading the electric field peak by creating a depletion region in the i-GaN below the p-NiO JTE. This was confirmed by TCAD simulations for current density at a reverse voltage of -200V, as presented in Fig. 5.5a and 5.5b. In the control SBD without any termination, the electric field peaks at the edge of the anode and results in high leakage current. The p-NiO creates an additional depletion region (indicated by the white boundary line), thus spreading the

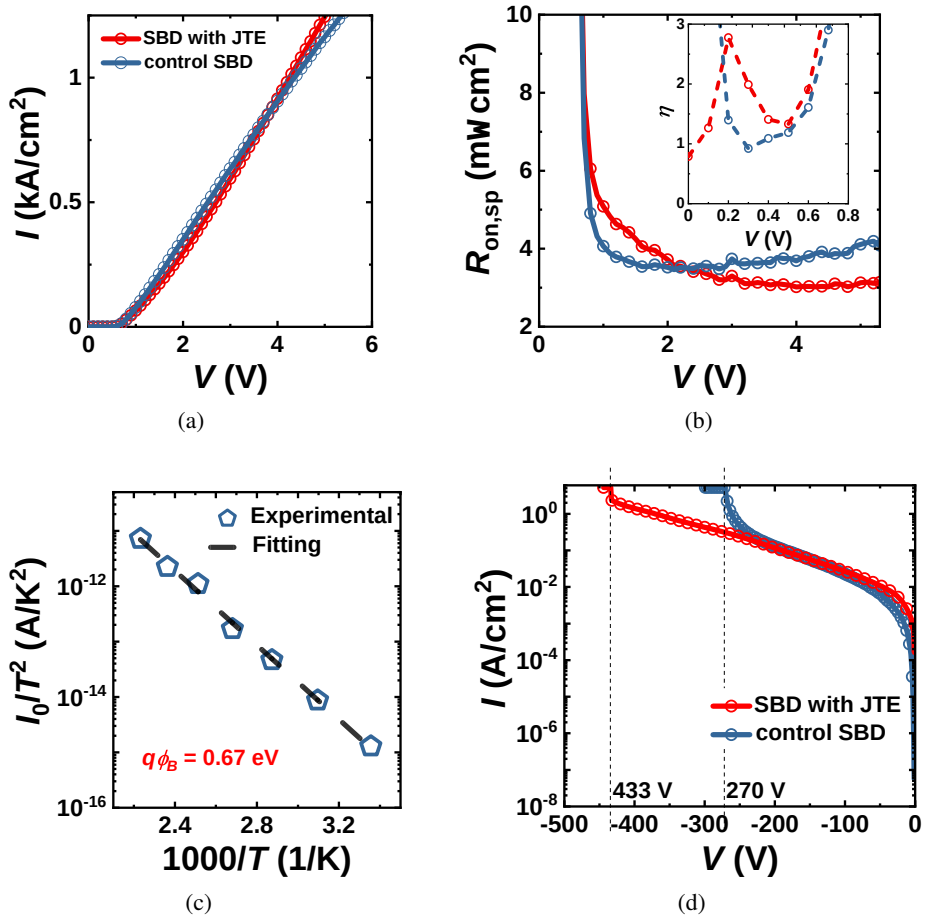


Figure 5.4 – (a) $I-V$ charateristics of the SBD with p-NiO JTE and the one without the JTE (control SBD). (b) $R_{on,sp}$ vs V plot for both the diodes and ideality factor in the inset figure. (c) Richardson's plot for extraction of $q\phi_B$. (d) Reverse breakdown performance of both the diodes. Inset schematic shows the anode region of an SBD with JTE.

electric field more uniformly. The $ln(I)$ at high reverse bias (> 100 V) as observed in Fig. 5.4d is proportional to the electric field (E), which is signature of dominant variable range hopping (VRH) model of conduction [175]. It is also interesting to note that the p-NiO/i-GaN/n- GaN diode provided a 1.4x-improvement in BV and 2.3x-reduction in $R_{on,sp}$ as compared to the control SBD. Fig. 5.5c presents the benchmarking of our GaN-on-Si SBDs against other reported GaN SBDs on bulk GaN, sapphire, and Si [83, 141, 194, 199, 212, 214, 241–244]. Compared to other GaN-on-Si SBDs, the p-NiO JTE SBDs presented here provided the highest reported BV of 433 V together with a low $R_{on,sp}$ resulting in a record Baliga's figure of merit (BFOM) of 63 MW/cm^2 for GaN-on-Si vertical SBDs.

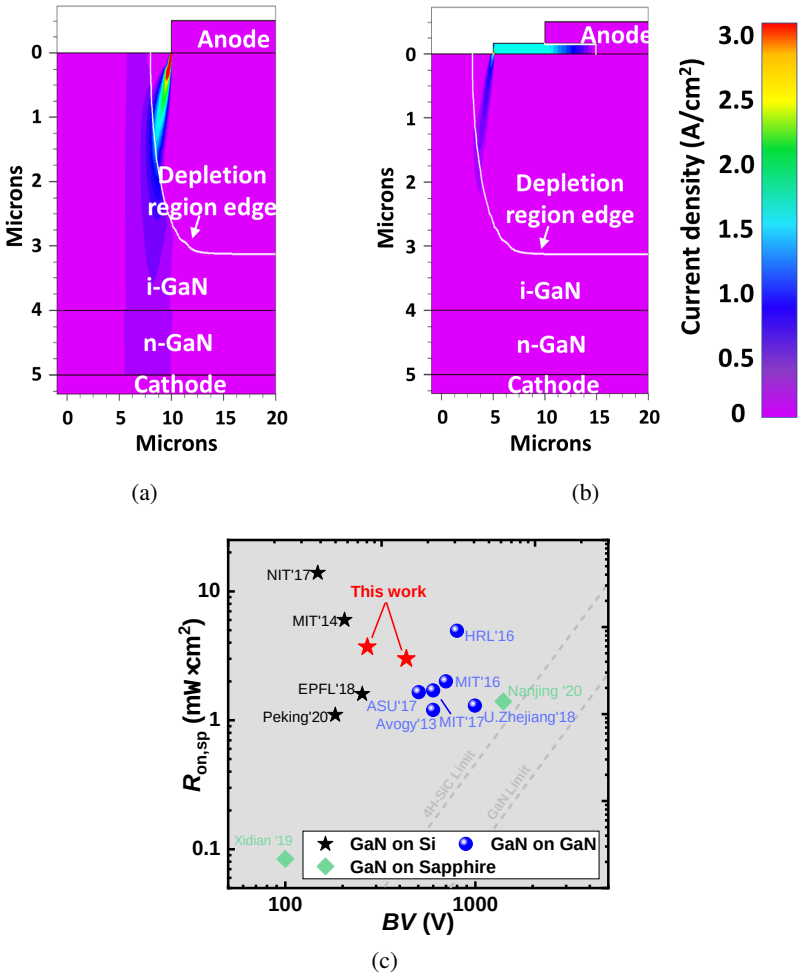


Figure 5.5 – (a) TCAD simulation of conduction current density at -200 V in the control SBD and (b) SBD with JTE. (c) $R_{on,sp}$ vs BV benchmarking of our GaN-on-Si SBDs against other reported GaN SBDs on bulk GaN, sapphire and Si.

5.3 Conclusion

To conclude we demonstrated the initial results which indicate that p-NiO could be an ideal candidate as a viable replacement for p-GaN for future power device applications. We first presented a p-NiO/GaN heterojunction p-i-n diode with a lower $V_{turn\text{-}on}$ of 1.6 V as compared to 3.4 V for a homoepitaxial GaN p-i-n diode and similar $R_{on,sp}$ and high forward current densities. The diode also provided a respectable BV of 380 V considering that the p-NiO was deposited by a easy and flexible RF-sputtering method. We also investigated the efficacy of this p-NiO for JTE applications where we observed an excellent 1.6x improvement in BV for the SBD with p-NiO JTE as compared to an SBD without any termination.The SBD with p-NiO JTE also provided better ON-state characteristics as well. These excellent results make a strong case for p-NiO to be used as simple,flexible and scalable alternative for p-GaN, for future power devices on GaN.

6 Conclusion and Future perspectives

6.1 Conclusion

In this thesis, we investigated about the viability of adopting GaN-on-Si substrates for demonstrating high performance vertical GaN power devices. GaN-on-Si substrates offers significant advantages over bulk GaN susbtrates like much lower cost and availability of wafers in large sizes upto 12-inches. As a result of exhaustive design, simulation and fabrication process optimisations we were able to demonstrate state-of-the art p-i-n diodes, Schottky barrier diodes and power MOSFETs which all have been published/submitted to well reputed journals like the IEEE EDL.

The first step towards realizing high-performance power devices is the proper optimisation of the myriad of process steps involved in the fabrication of a power device like ohmic and Schottky contact, p-GaN activation, dry and wet etching, passivation, etc. The first year of my Ph.D. was spent on accomplishing this goal. A demonstration of a p-i-n diode based on these optimisations followed. The p-i-n diode exhibited state-of-the-art ultra-low $R_{on,sp}$ of 0.33 mΩ cm^2 and the highest reported BV of 820 V for GaN p-i-n diodes on cost-effective Si substrates.

Since power MOSFETs are the most commonly used power devices, the demonstration of power MOSFETs on GaN-on-Si substrates ensued. We reported the first demonstration of quasi-vertical MOSFETs with excellent ON-state $R_{on,sp}$ of 15.3 mΩ cm^2 and BV as high as 645 V. We then probed the extend of current crowding which occurs on a quasi-vertical power MOSFET by fabricating and characterising large area quasi-vertical power MOSFETs. We observed that beyond an active area of 0.1 mm^2, current crowding degrades the maximum current capacity of the device and thus increases the $R_{on,sp}$. This led us to the development of fully-vertical MOSFET. A novel and robust fabrication process was developed to create the first fully-vertical MOSFET on GaN-on-Si substrates. The MOSFETs provides 3x lower $R_{on,sp}$, 2.2x higher curent density and 3.2x higher transconductance as compared to a quasi-vertical MOSFET. We also improved the gate etching process to realise the highest reported channel mobility of 41 cm^2/Vs for MOSFETs fabricated on GaN grown on foreign substrates like Si and Sapphire.

Integration of power devices with either additional functionalities or with modules like gate driver, logic blocks, etc, required for the safe operation of the device is garnering a lot of interest in the GaN HEMT commercial domain. The main advantages resulting from this integration is

understood to be reduction in the parasitic components leading to improved efficiency, smaller size and simplified packaging. We utilized the quasi-vertical topology inherent to GaN-on-Si devices to our advantage here and demonstrated MOSFETs with two special capabilities:

- Integration of a free wheeling diode and,
- Reverse blocking function.

Both the devices provided excellent ON- as well as OFF- state performance in addition to providing the additional functionality.

Lastly, we tried to address an age-old issue related to GaN electronic devices; selective doping. We proposed to employ p-type conductive NiO as a substitute for p-GaN and demonstrated high-performance p-i-n diodes and SBDs with junction termination extensions formed by p-NiO. The advent of p-type NiO could potentially solve the issues relating to reliability of vertical GaN power devices by providing a simple, scalable and easy method to form highly effective termination structures.

Thus we developed and demonstrated state-of-the-art power devices which open a promising pathway for the development of GaN-on-Si vertical devices for future power applications.

6.2 Future perspectives

In all fairness, the main obstacle that would prevent the adoption of GaN-on-Si vertical power devices for future power applications is the high dislocation density in the GaN layers as a result of large thermal and lattice mismatch of 54% and 17%. This dislocation density is about 2 to 3 orders higher than for bulk GaN substrates and is also the reason why the reverse leakage current of GaN-on-Si vertical devices mentioned in this thesis is higher than those reported on bulk GaN. In order to create reliable devices the current dislocation density of $\sim 5 \times 10^8$ /cm^2 has to be improved. Recently, Qromis Inc. has released a special Si substrate with an engineered poly-AlN core [104]. This substrate is coefficient of thermal expansion (CTE) matched to GaN which make it possible to grow thick GaN layers ($\sim$ 30 µm) without any cracking. Moreover, the dislocation density of GaN layers grown on these substrates can be as low as $\sim 5 \times 10^7$ /cm^2. They are also available in large sizes upto 12-inches which can aid the commercialization of these devices. The growth of GaN layers on these substrates have to be first optimized to minimize the defect density following which high voltage-high current devices could be demonstrated unlocking the full potential of GaN and the substrate.

Another main concern regarding GaN-on-Si vertical device reliability is the avalanche capability. Although avalanche breakdown has been reported for many p-i-n diodes based on bulk GaN, till date this very feature has not been reported for GaN-on-Si diodes. The demonstration of this feature in p-i-n diodes on GaN-on-Si will greatly leverage the future adoption of GaN-on-Si technology. One major requirement for avalanche to happen in a p-i-n diode is a uniform electric field profile in the device when the device is in the blocking mode. This however requires a proper design of doping and the thickness of the p-GaN layer as well as the type of termination used. We envisage that a shallow bevel termination with a bevel angle of $\sim 2\,^\circ$ could smoothen

the electric field peak as compared to a a traditional mesa termination as shown in the Fig. 6.1, obtained from TCAD simulations. The p-GaN thickness has been also increased (keeping the doping same as described through out the thesis) so that the electric field in the p-GaN never reaches the anode metal and cause breakdown at the anode contact edge. The most difficult part would be to create a 2 ° bevel angle during the fabrication of such a device. However, we have been able to achieve this by a combination of wet etch to create this angle on a SiO_2 hardmask deposited on the GaN and then transferring this angle to the GaN by ICP-RIE dry etching as shown in Fig. 6.2. The successful completion of this project will have far reaching implications in the future adoption of vertical GaN power devices based on GaN-on-Si substrates.

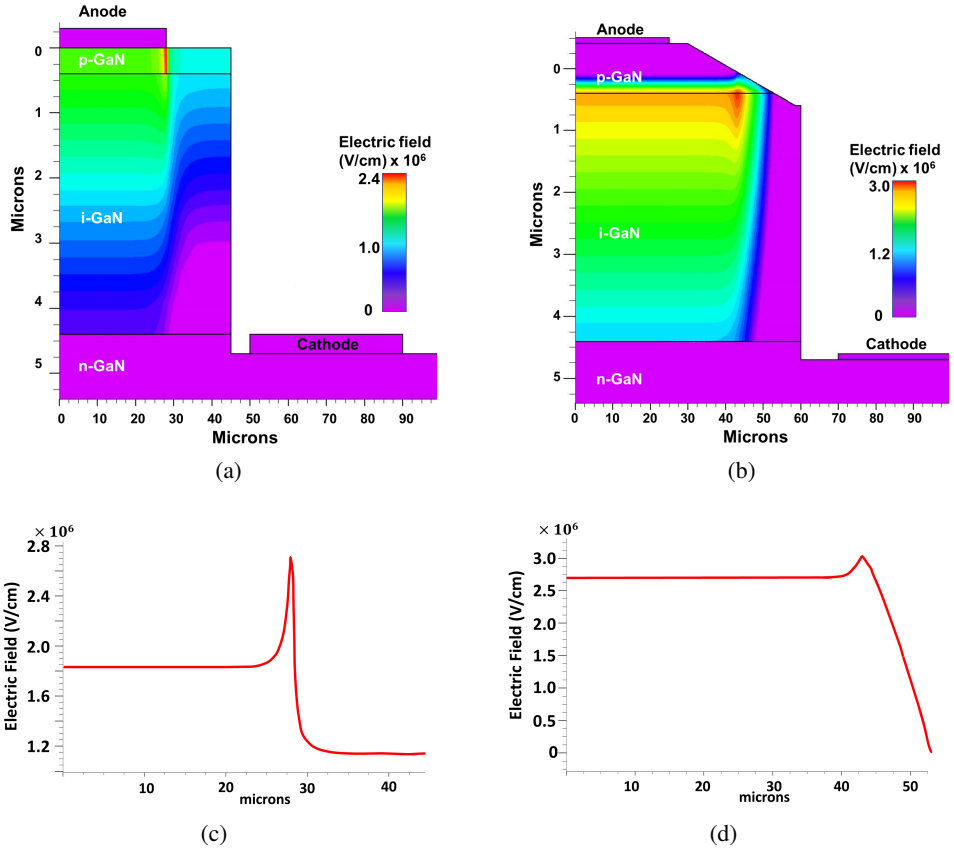


Figure 6.1 – (a) TCAD simulation of electric field at -400 V of a p-i-n diode described in 2 with no termination and (b) of a p-i-n diode with a bevel termination at -800 V. The bevel angle is 2 ° and the thickness of the p-GaN has been increased to 800nm. The electric field is only in the bulk of GaN and not reaching the anode even at a much higher reverse voltage of -800 V. (c) Electric field magnitude at the p-i junction of the diode mentioned in (a) revealing a huge overshoot where the anode contact ends. (d) A much smoother electric field distribution using the bevel termination. Also the peak appears well inside the bulk of GaN.

In Chapter 5, we discussed the potential of p-NiO as a replacement for p-GaN by demonstrating high-performance p-i-n diodes and Schottky diodes with p-NiO junction termination extensions. Based on these excellent results, the use of p-NiO could be extended for many other types of

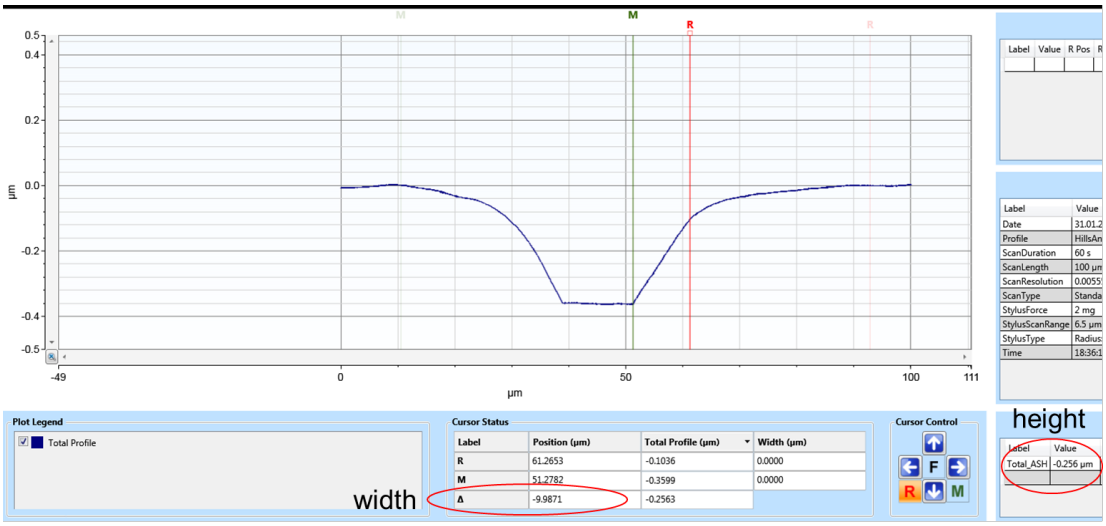


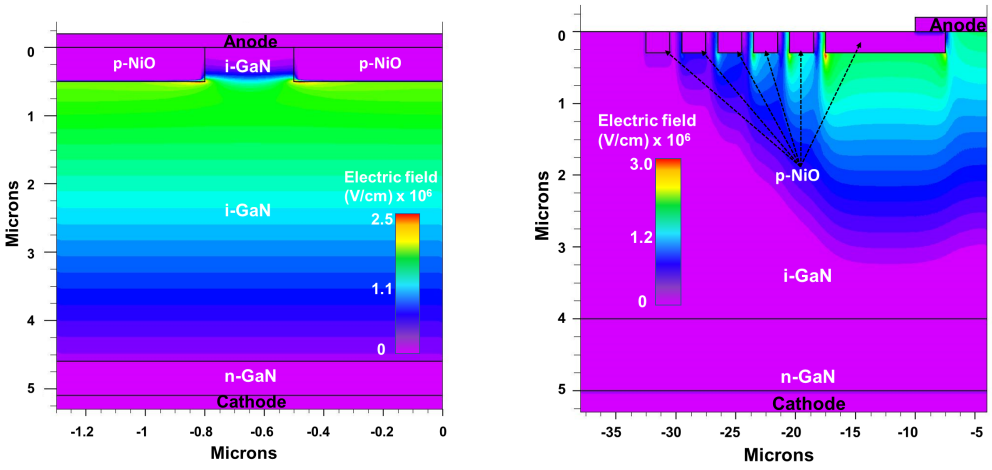
Figure 6.2 – Profilometer measurements of the GaN surface after dry etching using a SiO_2 hard mask incorporating a < 2 ° sidewall. The height of the slanted portion (in between the green and red measurement bars) in the figure is 0.256 µm and the width is 9.98 µm, resulting in a bevel sidewall angle of 1.5 °.

devices like:

- Junction barrier Schottky (JBS) and merged p-i-n Schottky (MPS) diodes that require selective p-doped pockets for their proper functioning (Fig. 6.3a)
- Advanced edge termination mechanisms like multi-zone JTEs (Fig. 6.3b).

Thus, in this section we have identified and laid out the cornerstone projects which could lead to the commercialization of low cost vertical GaN power devices on Si substrates. The adoption of QROMIS substrates could make it possible to have vertical GaN-on-Si devices with $BV > 5$ kV with a drift layer thickness of about ~ 20-25 µm. Methods to make fully vertical devices on these substrates have been already demonstrated [245]. Lateral GaN HEMTs are normally designed to have a large margin in BV over the rated value for surge voltage protection since they don't exhibit avalanche capability, which increases the cost per device. GaN-on-Si vertical devices with avalanche capability will be a major game changer which can allay fears of reliability of these devices. Also, the introduction of p-type conductive oxides like NiO, TiO_2, Cu_2O could finally provide a simpler solution to obtain efficient and highly-reliable edge termination of vertical power devices.

In summary, as observed from the results presented in this thesis,the future for vertical GaN power devices on Si substrates looks very promising. Continuous strides in research in this area could definitely leverage the fast adoption of this technology for cost-effective, highly-efficient, high voltage-high current devices for future power converters.



(a) (b)

Figure 6.3 – (a) TCAD simulation of electric field distribution in a vertical GaN JBS diode with p-NiO pockets. The p-NiO effectively shields the anode Schottky contact by creating a depletion region and thus reduces the leakage current. (b) TCAD simulation of electric field distribution of a GaN SBD with multi zone JTE. The p-NiO pockets as indicated spread the depletion region over a larger region and thus prevent any premature breakdown from happening at the anode contact edge.

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Education

02/2016 - Ongoing **École Polytechnique Fédérale de Lausanne, Switzerland**,
Ph.D., Doctoral School of Electrical Engineering (EDEE), POWERLab, under guidance of Prof. Elison Matioli.

05/2012 - 05/2015 **Indian Institute of Technology, Bombay**,
Masters (M.Tech.), Microelectronics, Department of Electrical Engineering, under guidance of Prof. Ashwin Tulapurkar, Final grade: 9.57/10 (C.P.I).

05/2005 - 06/2009 **Kerala University**, *Bachelors (B.Tech) Electronics and Communication*,
Final grade: 8.24/10 (C.G.P.A).

04/2003 - 04/2005 **Christ Nagar Higher Secondary School**, *High School*, Final grade: 87.87 %.

Ph.D. Project: "GaN-on-Si vertical power devices"

Employed GaN-on-Si substrates as a cost-effective platform for the realization of vertical p-i-n/Schottky diodes and MOSFETs, which could be adopted for future power applications. Main achievements during this period are:.

- **Developed and optimized** all the process steps involved in the fabrication of vertical power devices on GaN-on-Si from scratch like lithography, ohmic and Schottky contacts, dry and wet etching, p-GaN activation annealing, thin film deposition etc.
- **Reliability measurements** of fabricated devices during ON- and OFF-state repeated operation and avalanche ruggedness (ongoing).
- Investigation of weak points and **failure mechanisms** of the fabricated power devices exhibiting premature breakdown.
- **Highly proficient** in the design of **breakdown improvement structures** like field plates, junction termination extensions (JTE) using Silvaco ATLAS TCAD tool.
- **Highly experienced** in the use of metrology equipments like **SEM, FIB** which were used to investigate device cross-sections, localized fail points, etc.
- **Exhaustive electrical characterization** of devices using high voltage-high current probe stations, pulsed IV measurement tools,high temperature setups, and simultaneous thermal imaging measurements.

Experience

04/2010- 04/2012 **Junior Telecom Officer, Bharat Sanchar Nigam Limited**.

- Was the Junior Engineer of 5000+ subscriber line BSNL Telephone Exchange at Parappanangadi, Kerala.
- Was responsible for the smooth functioning of the day to day activities in the exchange like maintenance of 6000 line capacity telephone switch, mobile BTS station, WiMAX equipment and supervision of 11 line technicians.
- Reduced the number of fault lines from 230 to less than 30 during my tenure.

04/2013- 06/2015 **Research/Teaching Assistant**, *IIT Bombay*.
Assisted Bachelor's degree students with course assignments and trained them on various fabrication tools at the Center for Excellence in Nanoelectronics (CEN) semiconductor fabrication facility.

08/2015 - 02/2016 **Pre-doc Intern at POWERLab** , *EPFL*.
Created a LabVIEW code for simplifying Hall and transmission line measurements, and also worked on optimizing ohmic contact to GaN HEMT. 127

06/2012 - Ongoing **More than 7 years experience in semiconductor fabrication clean rooms at EPFL and IIT Bombay**.

Projects

08/2008 - 06/2009 **B.Tech. Main Project (done at Indian Space Research Organisation - ISRO)**,
Title: Design of FPGA based PWM current loop for 3-phase BLDC motor drive,
Guide: Mr. Sundaramoorthy, Scientist/Engineer SE, ISRO.

- Designed a closed loop control system aimed at positioning the rocket nozzle in the correct trajectory.
- Digital logic blocks used to realize the control system.
- Successfully implemented the digital module using VHDL.

08/ 2013 - 08/2015 **M.Tech Project, IIT Bombay**,
Title: Spin Injection in graphene,
Guide: Prof. Ashwin Tulapurkar.

- Learned Synthesis and transfer of CVD graphene at Tata Institute of Fundamental Research (TIFR).
- Developed and optimized the process steps for fabrication of graphene based electronic devices like ohmic and Schottky metal contact, etching of graphene using O_2 plasma, annealing, etc.
- Fabrication/Characterization of HOPG and CVD graphene 2 terminal devices.
- Investigation of Spin Injection in graphene.

08/2014 - 03/2015 **Analog Devices Design contest, Anveshan-2014, member of winning team**,
Title: Baby Beats,
Guide: Prof. Maryam Shojaei.

- Successfully implemented a wearable health and wellness monitor for babies.
- Implemented and integrated a pulse oximeter, heart rate monitor, fall detection system and diaper wetness sensor into a belt which can be worn by babies.

Skills

Fabrication tools	Electron beam lithography, photo-lithography, Focused ion beam etching, wet and dry etching, e-beam evaporation and sputtering, Argon-ion milling, atomic layer deposition, rapid thermal annealing, PECVD.
Measurement tools	Atomic force microscopy, scanning electron microscopy, profilometer, probe stations.
Programming	LabVIEW, MATLAB, VHDL, Silvaco ATLAS, C/C++.
Languages	Fluent: Malayalam, English, Hindi. Arabic (Read and Write). French (A2). Spanish (A1).
Soft Skills	Team work, strong problem-solving skills, time management, strong work ethic, empathetic.

About me

I have varied interests outside of academics. I am an avid follower of F1 and Kimi Räikkönen. I love reading about history of countries and their culture. I love visiting new places and ever since I moved to Switzerland, I have travelled quite a bit and have visited many countries in southern Europe. I have also successfully completed an expedition to the Himalayas and crossed the 'SAR PASS' at 14,000 ft. Cooking is my therapy and I love experimenting with new dishes.

Publications

Journal publications

IEEE EDL "Quasi-vertical GaN-on-Si Reverse-Blocking (RB) power MOSFETs", R. A. Khadar, A. Floriduz, C. Liu, R. Soleimanzadeh and E. Matioli, *submitted to IEEE EDL*

IEEE EDL "p-NiO/GaN heterostructures for p-i-n diodes and junction termination extensions", R. A. Khadar, A.Floriduz, T. Wang, C. Erine, R. V. Erp, L.Nela, R. Soleimanzadeh, P. Sohi and E. Matioli, *submitted to IEEE EDL*

IEEE EDL "820-V GaN-on-Si Quasi-Vertical p-i-n Diodes With BFOM of 2.0 GW/cm^2", R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, Vol. 39, Is. 3, p. 401 - 404, March 2018.

IEEE EDL "Fully vertical GaN-on-Si power MOSFETs", R. A. Khadar, C. Liu, R. Soleimanzadeh and E. Matioli, Vol. 40, Is. 3, p. 443 - 446, March 2019.

IEEE EDL "GaN-on-Si Quasi-Vertical Power MOSFETs", C. Liu, R. A. Khadar, and E. Matioli, Vol. 39, Is. 1, p. 71 - 74, January 2018.

IEEE EDL "Vertical GaN-on-Si MOSFETs With Monolithically Integrated Freewheeling Schottky Barrier Diodes", C. Liu, R. A. Khadar, and E. Matioli, Vol. 39, Is. 7, p. 1034 - 1037, July 2018.

JAP "Near-junction heat spreaders for hot spot thermal management of high power density electronic devices" R. Soleimanzadeh, R. A. Khadar, M. Naamoun, R. van Erp, and E. Matioli, Vol. 126, Is. 16, p. 165113, October 2019

IEEE EDL "H-Terminated Polycrystalline Diamond p-Channel Transistors on GaN-on-Silicon", R. Soleimanzadeh, M. Naamoun, R. A. Khadar, R. van Erp, and E. Matioli, Vol. 41, Is. 1, p. 119 - 122, November 2019

Conferences

IEEE COMPEL 2020, Aalborg "Output Capacitance Losses in Wide-Band-Gap Transistors: From Packaged Devices to the Epitaxy", M. S. Nikoo, A. Jafari, R. A. Khadar, M. Zhu, N. Perera and E. Matioli.

CSW 2018, Boston "High performance 820 V GaN-on-Si p-i-n diodes", R. A. Khadar, C. Liu, R. Soleimanzadeh, L. Zhang, P. Xiang, K. Cheng, and E. Matioli.

CSW 2019, Nara "High performance GaN-on-Si fully-vertical power MOSFETs", R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli.

ISPSD 2018, Chicago "645 V quasi-vertical GaN power transistors on silicon substrates", C. Liu, R. A. Khadar, and E. Matioli.

CSW 2018, Boston "Vertical GaN-on-Si MOSFET with Monolithically Integrated Freewheeling Schottky Barrier Diode", C. Liu, R. A. Khadar, and E. Matioli.

IWN 2018, Kanazawa "Local heat spreaders for quasi-vertical GaN power devices", R. Soleimanzadeh, R. A. Khadar, and E. Matioli

SBDD 2019, Hasselt "Integrated diamond heat spreaders for GaN power devices", R. Soleimanzadeh, M. Naamoun, R. A. Khadar, R. van Erp, and E. Matioli

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