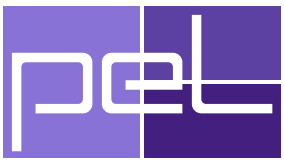

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Solid-State Technology for Shipboard DC Power Distribution Networks

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Solid-State Technology for Shipboard DC Power Distribution Networks

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***Abstract*—The use of DC shipboard power distribution networks has been shown to offer several advantages over their AC counterparts. The reduction of the size and number of system components, the increased simplicity of operation and fuel efficiency of the system and convenient integration of energy storage systems offer significant economical benefits to the ship operator. Solid-state bus tie switches are widely regarded as being an indispensable component in DC shipboard power distribution networks, for their role as first line of defence against faults. Nevertheless, these devices are not limited exclusively to protection, but can provide additional functionality thanks to their design. This paper shows how a solid-state bus tie switch can be employed for soft-starting an unenergised section of a shipboard power distribution network, eliminating the need for additional components aimed specifically at this task. Two techniques are suggested and their performance is experimentally verified in a laboratory scaled-down model of a DC shipboard network. The additional functionality is achieved exclusively on a control basis, without modification of the switch topology initially intended purely for system protection.**

I. Introduction

Today, DC shipboard power distribution networks (PDNs) are already a reality on commercial vessels at the low voltage (LV) level, and they are expected to expand to the medium voltage (MV) voltage level in the coming years [1]–[5]. This will allow DC distribution to be employed in vessels with rated powers of several tens of MW. The incentive for the transition from AC to DC PDNs rests mainly on their widely recognised advantages in terms of efficiency, simplicity of operation and ability to integrate means of electrical energy storage [6]–[9]. An essential component in such DC shipboard systems is the solid state bus tie switch (SSBTS) [10]: this device provides two functions that are key to the operation of DC PDNs. The first of these functions is to provide the ability to connect and disconnect different DC buses in the distribution system, as seen in Fig. 1. This allows a degree of reconfigurability of the PDN that permits the selection of optimal energy flow direction according to the needs of the vessel. The second and more critical function [11]–[14] is to provide a first line of defence in the power system by providing protection through ultrafast electrical separation between buses in the event of a fault. This ultrafast separation, integrated in a larger protection coordination strategy for the vessel, provides reliable protection that allows DC vessels to operate with closed SSBTSs in almost all operating modes, including dynamic positioning (DP), resulting in improved fuel economy and lowered operating costs.

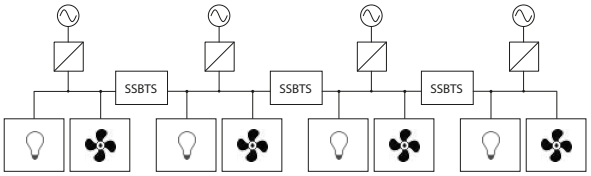

Fig. 1: Shipboard DC PDNs include multiple switchboards clustering generator sets and loads. These clusters are interfaced through SSBTSs providing both protection and reconfigurability to the system.

While these discussed functions of the SSBTS make it a necessary component of DC shipboard PDNs, further opportunities exist in using this device to achieve new functionalities. A significant advantage of modern DC shipboard PDNs lies in the the simplicity of bus-to-bus and generator-to-bus connection. In traditional AC PDNs, the connection of synchronous generators to the network requires careful synchronisation. For this purpose, four factors are to be matched: phase sequence, voltage magnitude, frequency, and phase angle. By contrast, the only factor to be considered in DC PDNs is the voltage magnitude.

Contrary to traditional AC PDNs, in existing DC shipboard PDNs, the interconnection of two DC buses through a SSBTS can only be performed when the voltage difference between the two DC buses is within a well defined range [15]–[17]. Therefore, it is not possible to interconnect the buses in the event that one bus is fully energised (at the rated voltage level) and the other is unenergised (e.g., following fault and its clearance) with no precharge circuits. Without such a circuit, the energisation of the bus without activation of the prime generators cannot be achieved. The soft-start function proposed by this paper and achieved through an existing SSBTS by smoothly transferring energy from one bus to the other eliminates the need for additional circuitry required for bus capacitance charging. Removing the limitations of voltage matching during interconnection processes significantly extends operation sequences and/or modes of DC

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shipboard PDNs: it becomes possible to supply electric power to the bus in which no electric source is available. This can happen for a variety of reasons like system design, operating mode (one generator operating mode), or generator failure. Furthermore, the soft-start function can also be employed in solid-state circuit breakers located both at the supply side and feeder sides, allowing to freely connect and disconnect power supplies and loads without additional inrush current limiting circuitry. This is one of the key advantages of the proposed method as the functionality of the device is extended at no additional cost. Traditional soft-start methods employ precharge resistors between the energised DC source and the unenergised capacitances, with means to bypass the precharge resistor once the precharge is complete. The bypass can be performed by contactors or semiconductors, depending on the system requirements. However, by doing so, additional semiconductor devices or contactors remain in series with the conducting SSBTS when the DC buses are interfaced, reducing efficiency and negating a part of the benefits of a DC PDN. The additional circuitry may also require additional cooling, depending on the employed devices and PDN power level. Compared to these solutions, the adaptation of the funtionality of the SSBTS to include soft-start ability provides a more streamlined option with lower component count, and no decrease in efficiency.

Therefore, the contribution of this paper consists in *i)* the proposal and comparison of two techniques to provide unenergised DC bus soft-start functionality through the SSBTS, without any alterations of its design; *ii)* the experimental demonstration of the proposed techniques through the laboratory scaled-down shipboard PDN model. The model in question is displayed in Fig. 2 and includes two DC buses highlighted as *BUS 1* and *BUS 2*. Each bus includes a DC motor, simulating the Diesel generators employed in shipboard PDNs, externally excited synchronous generator with active voltage regulator (AVR), diode rectifier, capacitor bank and load resistors. The two DC buses are interfaced by an SSBTS equipped with an internal controller, while the whole system is supervised by a central PDN controller.

This paper is organised as follows: Section II provides a short introduction to the employed SSBTS topology, Section III discusses the scenarios in which the soft-start function is expected to be employed, Section IV presents the principles of the operation of the SSBTS in soft-start mode, and finally Section V presents the proposed soft-start method and experimental results in the laboratory installation where the performance of the method is experimentally verified and validated.

II. SSBTS Topology and Operation

A recently developed and demonstrated SSBTS unit is analysed in this paper for the additional soft-start function it can provide to the displayed scaled-down shipboard DC PDN model. Since the primary function of this device is ensuring the protection of the system, no alterations are made to the SSBTS design rules provided in [10], [18]. The additional soft-start functionality is achieved solely through the implementation

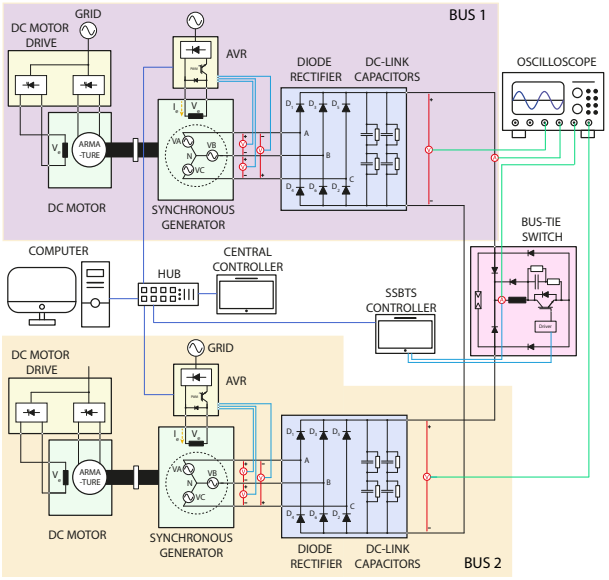

Fig. 2: Block schematic of the laboratory scaled-down DC shipboard PDN.

TABLE I: SSBTS ratings.

I_{nom}	I_{max}	V_{DC}	$t_{reaction}$
100 A	200 A	500 V	10 µs

of additional control schemes. The topology on which the device is based, displayed in Fig. 3a, is built upon a well known four-quadrant switch, expanded upon to cover the role of a protection device by adding a number of components: *1)* a current rate limiting inductor $L_{didt} = 48\,\mu\text{H}$ to control the maximum rate of current increase during a fault; *2)* the associated antiparallel freewheeling diode D_L to enable freewheeling of the current in L_{didt} after interruption; *3)* a metal oxide varistor (MOV) across the terminals of the SSBTS to clamp the voltage at the terminals of the device to a set value; *4)* an RC snubber in parallel to the IGBT switching position to limit the voltage on the semiconductor upon current interruption. The currents and voltages of the components of the SSBTS during a fault and interruption are displayed in Fig. 4. Here, one can see how after a fault the current in the device increases up the time of interruption (t_1), and is then taken over by the MOV dissipating the DC bus magnetic energy (t_2) until the current in the device reached 0 A (t_3). A more detailed description of the device's operation is available in [10]. Based on this topology, a prototype shown in Fig. 3b is built with the ratings listed in Table I. These are are chosen in accordance with the ratings of the installation in Fig. 2, and sufficient for demonstration purposes. where V_{DC} is the blocking voltage of the device, that is to say the voltage of the power system in which it is intended to operate. I_{nom} is the nominal current that the device is thermally sized to conduct indefinitely, and I_{max} is the maximum current the

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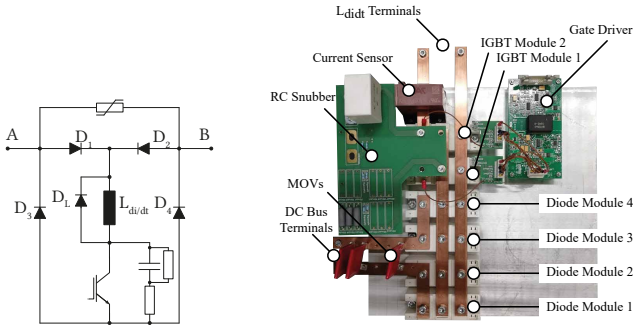

(a) (b)

Fig. 3: (a) SSBTS topology used for validation of soft-start, presented in detail in [10], where A and B are the terminal connected to the positive DC bus bar; (b) SSBTS prototype.

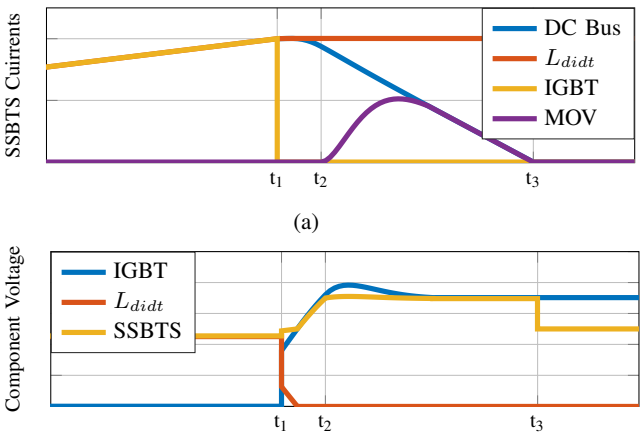

Fig. 4: SSBTS currents (a) and voltages (b) during a fault and current interruption.

device can interrupt safely. Finally, $t_{reaction}$ is the maximum allowed time delay from the time the device is tripped to the time the interruption takes place.

The control of the device is deployed on a *PLEXIM RT-Box* rapid control prototyping platform, that is fitted with a custom interface board for the task. This is shown in Fig. 5. Through the interface board the RT-Box has access to current and voltage sensors on board the SSBTS prototype. Based on the values sampled from these sensors at a frequency of 1 MHz, the RT-Box can identify the presence of a fault and turn the SSBTS off avoiding fault propagation. The controller can use three different criteria to determine the presence of a fault. These can use the sensed current level in the device, the current rate of increase, or the voltage applied to the terminals of the current rate limiting inductor L_{didt}. All of these criteria have been shown to be effective in the identification of a fault in the PDN in laboratory conditions. A block schematic of the employed SSBTS test setup is provided in Fig. 6. The test verified that the device was reliably and safely able to perform a current interruption once the value of the current in the device exceeded the nominal value of 100 A, as this was the

Fig. 5: A *PLEXIM RT-Box* fast control prototyping platform is fitted with a custom interface board to control the SSBTS prototype for the purpose of the laboratory testing.

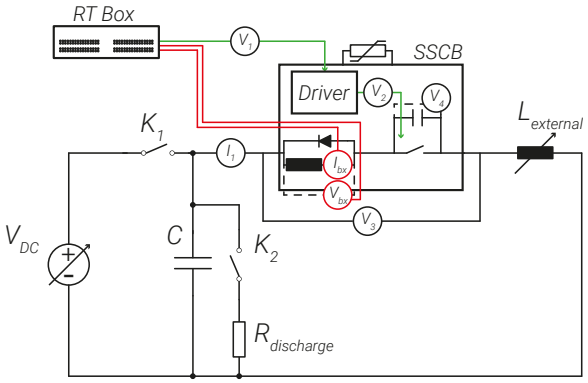

Fig. 6: Block diagram of the SSBTS test setup for the evaluation of the device's interruption performance. [10].

employed criterion to determine the need for an interruption in the presented case.

III. Soft-Start Scenarios

Evaluating different soft-start scenarios that are possible in the context of shipboard DC PDN is essential for the selection of an effective soft-start method. The necessity of a soft-start can emerge in different operating modes and in different conditions of the PDN. Nevertheless, in all considered scenarios the soft-start does not take place under load, as the amount of power that can be transferred through pulsed operation of the SSBTS is limited, as will be shown in the paper. The considered scenarios are as follows:

(a) DC bus soft-start: The first scenario in Fig. 7a is that of the charging of an unenergised DC bus. In the condition that the loads interfaced to an unenergised, healthy DC bus need to be operated, soft-start of the bus through the SSBTS can provide significantly faster loading than what can be achieved by starting generators on the unenergised DC bus side. Once the voltage of the DC bus is brought up to its nominal value, the SSBTS closes definitively to allow the flow of its nominal current toward the loads interfaced to the newly connected bus.
(b) Fault recovery: The second scenario in Fig. 7b considers the event of a fault taking place in one DC bus. In this case, the SSBTS will perform its protection function by providing ultrafast disconnection of the faulty bus from the rest of

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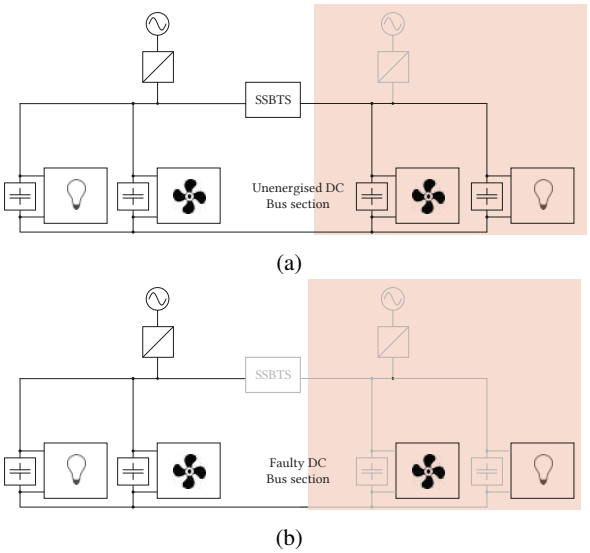

Fig. 7: The SSBTS soft-start function can provide energisation under conditions of (a) an unenergised DC bus; (b) a faulty DC bus.

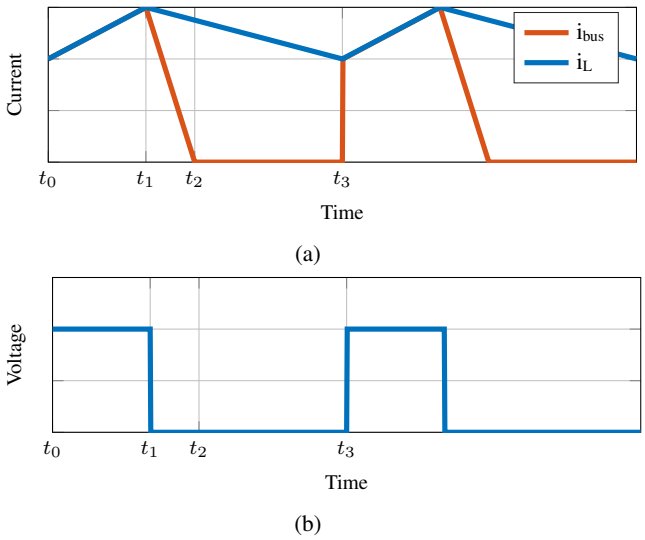

Fig. 8: (a) Upon the SSBTS opening, the current in the DC bus is interrupted, while the current in L_{didt} is permitted to freewheel; (b) Corresponding SSBTS switching pulses.

the power systems. Once this has happened and the fault is isolated, an attempt can be made to quickly restore the loads connected to the unenergised DC bus. Depending on whether the fault is still present or not in the DC bus, its energisation can be successful or not.

Therefore, the soft-start control of the SSBTS must have the following abilities:

- Provide energisation of an unenergised bus in the shortest time possible.
- Determine the presence of a fault during charging and interrupt the process.

With these capabilities, the SSBTS can provide fast and reliable soft-start of the unenergised bus without endangering the condition of the system.

IV. Operating Principle of the Soft-Start

Most loads connected to a shipboard DC bus are interfaced through power converters that present a varying amount of input capacitance toward the bus. When a DC load or bus is not energised, these capacitances are not charged and direct connection to nominal voltage will result in large inrush currents through the load input capacitances. To prevent this, the implementation of the bus soft-start function through the SSBTS employs repeated current pulses to precharge capacitances connected to the unenergized load or DC bus from a fully energised DC bus. This avoids a capacitive inrush current and allows for controlled charging. Figs. 8a and 8b display an idealised current profile and the SSBTS control pulse in such mode of operation. Between times t_0 and t_1, the SSBTS is *ON* and the two DC buses are connected. Current flows through the SSBTS with a rate of increase determined by the current rate limiting inductor and the difference in voltage between the two buses interfaced by the SSBTS. To prevent the current from reaching dangerous levels, the SSBTS

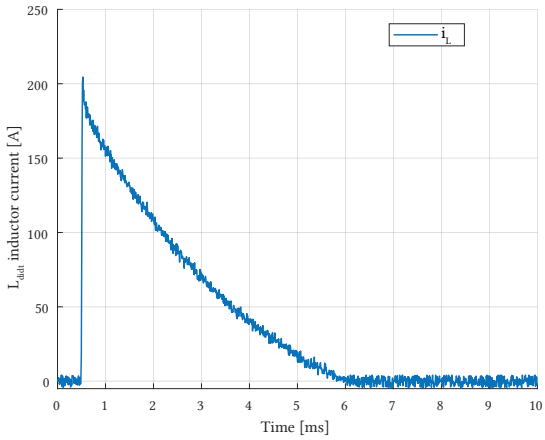

Fig. 9: Gradual decay of current in L_{didt} following interruption, starting from 200 A.

is turned *OFF* at time t_1, separating the two buses. The current drops quickly, reaching 0 A at t_2. As the SSBTS topology allows for freewheeling of the current in L_{didt} (to reduce switching stress on the IGBT modules), the current in the inductor is not interrupted at time t_1, but continues flowing at a decreasing rate determined by the value of L_{didt} and the on-state resistance of D_L. In Fig. 8a this is presented as a linear current decrease according to

$$\frac{di}{dt} = \frac{V_{D_L}}{L_{didt}}, \tag{1}$$

as the forward voltage of D_L varies only marginally as a function of i_L. Fig. 8b shows the corresponding control pulse, while Fig. 9 displays the measured current decay in L_{didt} after interruption starting from a current of 200 A. This is relevant during the soft-start process as the decay time of the inductor current will be shown to be the main factor in determining

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the SSBTS pulsing frequency. At t_3, the current in L_{didt} has decreased to a lower level and it is possible to turn *ON* the device again and the two buses can be reconnected, starting a new charge transfer.

The energy transfer between the two DC buses takes place during a short time period, between the instants the SSBTS is turned on and then off. In Fig. 8a this corresponds to time interval t_0 to t_1 (neglecting the time of bus current decrease). From $t_2 tot_3$, no energy is transferred between the two buses. This is the case every time the inductor current is decreasing, as in this case the energy present in the inductor is being dissipated thermally in D_L. Clearly, this does not result is an energy-efficient charging process. Nevertheless, it must be underlined that the SSBTS is designed for the protection of the shipboard PDN, and that the soft-start functionality presented in this paper is an additional benefit that the use of such a device offers. Due to the relatively infrequent nature of the soft-start process, installing additional equipment such as a charging resistors and contactors represents an increase in complexity compared to which the energy losses in the SSBTS-based soft-start are reasonable. The characteristic of the soft-start process can be analysed as a function of:

- DC bus nominal voltage V_{DC}.
- DC bus capacitance C_{bus}.
- Current rate limiting resistor L_{didt}.
- D_L forward voltage drop V_{D_L}.
- I_{max} maximum allowed current in the SSBTS.

For the analysis presented in the following section, it is assumed that the energised DC bus is a stiff voltage source providing a constant voltage equal to V_{DC}. The considered system is displayed in Fig. 10.

V. Soft-Start Method

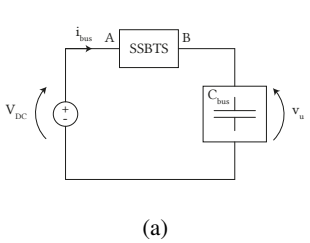
A safe and rapid start of an unenergised DC bus improves the flexibility of the DC shipboard power system by allowing for rapid connection of loads and for timely restart of operation in the event of a fault. To achieve charging of the unenergised DC capacitance, whether of a load or of a full DC bus, in the shortest time possible, the goal is to maximise the average current transferred through the SSBTS while also maintaining it at a controlled level. At the same time, the method must be able to detect the presence of a fault in the system being energised and interrupt the process. To achieve this, a method that provides as-fast-as-possible charging of the capacitance (no matter whether of a DC bus or load) is proposed, employing hysteresis control of the L_{didt} inductor current as shown in Fig. 11. The minimisation of the charging time of the capacitance implies the maximisation of the charge transferred from the energised side of the SSBTS to the unenergised side. To have an analytical estimation of the required charging time as a function of the parameters of the system involved, it is assumed that energy transfer between the two buses only takes place in interval $[t_0, t_1]$ (from Fig. 8), while the SSBTS is *ON*. In reality, this is an approximation, as charge transfer between the two buses takes place as long as a current through the DC bus is sustained, and therefore also during the charging of the SSBTS snubber and the MOV breaking ($[t_1, t_2]$ in the figure). Nevertheless, this approximation still provides interesting insight into the main quantities involved in determining the duration of the charging process and most importantly it provides a conservative estimate of the required charging time t_{charge}. Under this hypotheses, the charge transferred with each pulse can be approximated to

$$Q_{pulse} = \frac{I_{OFF} + I_{ON}}{2} t_{ON}, \tag{2}$$

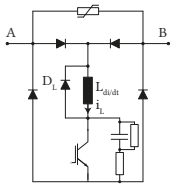
clearly showing that an increase of the hysteresis turn-on and turn-off current levels results in an increased charge transfer per pulse. The time interval t_{ON} is equal to $t_1 - t_0$. The duration of t_{ON} is determined by the value of the current rate limiting inductor and difference in voltage between the two buses, and can be expressed as:

$$t_{ON} = \frac{(I_{OFF} - I_{ON}) L_{didt}}{V_{source} - V_{charge}} \tag{3}$$

where V_{source} is the voltage of the energised DC bus, and V_{charge} is the voltage of the unenergised load. This is because while the SSBTS is *ON*, the difference in voltage between the two buses is applied at its terminals, resulting in a current rate of increase determined by the value of L_{didt}. Once the

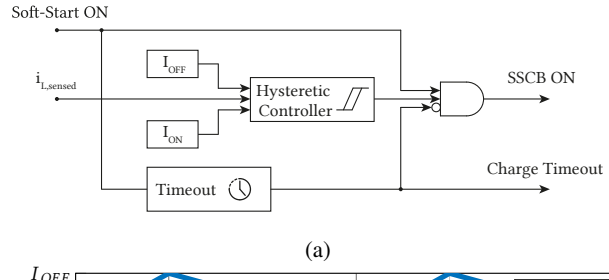


(a)



(b)

Fig. 10: (a) The analysis considers a stiff energised DC bus represented by V_{DC}; (b) The SSBTS topology allows freewheeling of i_L [18].



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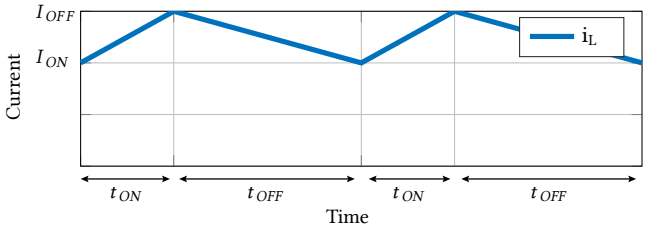

(b)

Fig. 11: (a) Block diagram of the soft-start control logic; (b) Simulated L_{didt} current during fast charging of the DC bus. One can see the two threshold levels I_{OFF} and I_{ON}.

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SSBTS is turned *OFF* the current starts decreasing due to the device's breaking action, and no more charge is transferred to the secondary side as the L_{didt} inductor current decays. The duration of the interval during which the inductor current decreases can be expressed as

$$t_{OFF} = \frac{(I_{OFF} - I_{ON})L_{didt}}{V_{D_L}}, \tag{4}$$

as the rate of decrease of the inductor current is determined by the on-state resistance of the freewheeling diode D_L. The rate of decrease of the inductor current is assumed to be constant for current value included between I_{ON} and I_{OFF} (from Fig. 9). As, due to the low value of V_{D_L}, $t_{OFF} \gg t_{ON}$, it is reasonable to approximate and state that the duration of the whole switching interval $t_{OFF} + t_{ON} \approx t_{OFF}$. This allows to write the average rate of charge transfer during a switching interval as

$$\frac{Q_{pulse}}{t_{OFF}} = \frac{I_{OFF} + I_{ON}}{2(V_{source} - V_{charge})} V_{D_L}, \tag{5}$$

which corresponds to the average current transferred during one switching cycle. The above equation shows how the charge transfer depends on the difference in voltage over the SSBTS, and in particular of the voltage of the unenergised load V_{charge}, as all other quantities are assumed to be constant during the charging process. The equation also shows that increasing the values of I_{OFF} and I_{ON} leads to faster charging. Having determined the average current transferred between the two buses as a function of the voltage of the unenergised bus, the required time to charge the unenergised bus from 0 V can be determined by solving the nonlinear ODE

$$V_{charge}(t) = V_{charge}(0) + \\ + \frac{1}{C_{charge}} \int_0^t \frac{V_{D_L}(I_{OFF} + I_{ON})}{2(V_{source} - V_{charge}(t))} dt \tag{6}$$

which, by setting the initial condition $V_{charge}(t) = 0\,\text{V}$, yields

$$V_{charge}(t) = V_{source} - \sqrt{V_{source}^2 - \frac{I_{OFF} + I_{ON}}{C_{charge}} V_{D_L} t}. \tag{7}$$

Equation 7 provides as the voltage of the unenergised bus as a function of time. This allows to rearrange the terms to provide the charging time as a function of the nominal DC bus voltage V_{source}. The time to reach the voltage value V_{source} can then be expressed by rewriting in the form

$$t_{charge} \propto V_{source}^2 \frac{C_{charge}}{(I_{OFF} + I_{ON})V_{D_L}}. \tag{8}$$

As stated at the beginning of the section, 8 provides a rough estimation of the charging time, overestimating the duration of the process by neglecting charge transfer during interval t_1, t_2. Nevertheless, from the result one can see that:

- In a system with higher nominal voltage, the charging time will be increased.
- Increasing the sum of the current boundaries I_{OFF} and I_{ON} and the forward voltage of the freewheeling diode D_L can be used to decrease the charging time.

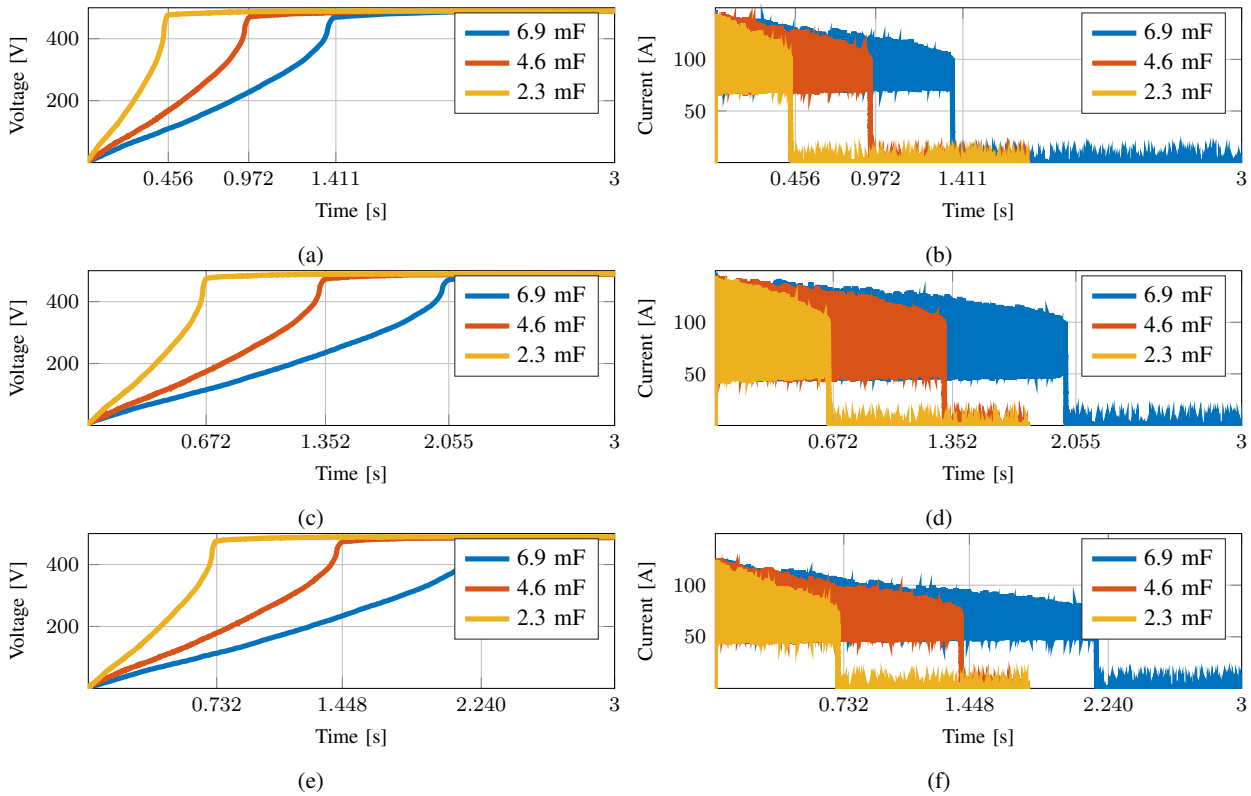

Fig. 12: Voltage and current of the unenergised bus during soft-start process at varying levels of C_{charge} and with I_{OFF} and I_{ON} value of, respectively, (a,b) 100 A and 75 A; (c,d) 100 A and 50 A; (e,f) 75 A and 50 A.

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(a) (b)

Fig. 13: (a) SSBTS rack includes the device, *RT-Box* controller and current rate limiting inductor; (b) Capacitor bank 1 provides energy as capacitor bank 2 is charged.

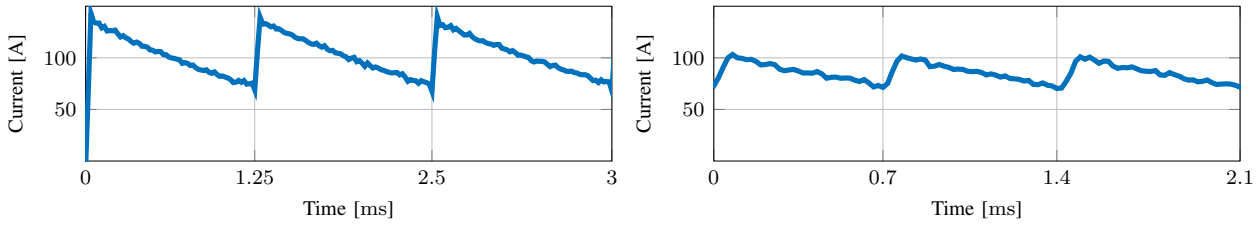
The system voltage is not a parameter that can be altered to result in favourable soft-start condition, and therefore is not considered as a test parameter. The same goes for the freewheeling diode D_L, which is selected based on the primary SSBTS function of current interruption. The parameters that can be truly altered are the values of I_{OFF} and I_{ON}, which can be varied within the limits of the SSBTS maximum interruption current ability. Note also that the value of C_{charge} can vary depending on which load is being charged, or the configuration of the unenergised DC bus. Therefore, charging tests are performed with varying levels of I_{OFF}, I_{ON} and C_{charge}. The capacitance value C_{charge} is also crucial for determining the presence of a fault condition. While the level of the current in the SSBTS and DC bus cannot exceed that of I_{OFF} due to the hysteresis controller, it must still be ensured that the soft-start operation of the SSBTS is not attempting to charge into a short circuit or to charge a loaded DC bus. Charging under load is not possible with this method due to the low power transferred during pulsed operation. For this reason, the soft-start time t_{charge} is precomputed based on 8 that provides, as discussed earlier, an overestimation of the charging time. This computation is performed based on the worst-case-scenario loading conditions, that is to say the largest capacitance connected to the unenergised DC bus. If the charging is not completed after the precomputed time interval t_{charge}, then a charge timeout error signal is raised and the soft-start is interrupted.

Fig. 12 displays the results obtained with this charging method at varying levels of capacitance and with different I_{OFF} and I_{ON} thresholds, as described by the captions. Fig. 13b displays part of the test setup including the SSBTS and DC bus capacitance and load resistors. For each capacitance level, the charging time is displayed on the *x*-axis. The charging time is defined as the time at which the SSBTS turns *ON*, and the threshold of I_{OFF} is not reached by the bus current, ensuring the device can remain in conduction state and definitively connect the two terminals of the SSBTS. In all the figures, one can observe how the capacitance of the unenergised bus results in a linear increase of the charging time as expected from Equation 8. Even at the highest capacitance level tested, of $6.9\,\mathrm{mF}$, the charging process takes less than $1.5\,\mathrm{s}$ with the highest I_{OFF} and I_{ON} values, as presented in Fig. 12a. Decreasing the value of either of these thresholds results in an increase of the charging time, which again is expected from 8. The charging time still does not exceed $2.5\,\mathrm{s}$ even in the worst case of low current threshold and high bus capacitance, as show in Fig. 12e. The tests show that for the purpose of achieving fast charging of the unenergised DC bus with this method, maximising the values of I_{OFF} and I_{ON} is an effective method. In the specific case of the test results presented in this paper, the two thresholds are selected as follows:

- For I_{OFF}, it is selected to be the nominal current of the device. This is because during soft-start operation this level of current is conducted almost constantly by the freewheeling diode D_L. Therefore, it was chosen to not exceed the value of $100\,\mathrm{A}$ to avoid thermal stress on the module containing D_L and the IGBT.
- For I_{ON}, it is selected so that the duration of the ON pulse of the SSBTS, determined by the value of L_{didt} and V_{DC}, would not be shorter than $2.5\,\mu\mathrm{s}$. Below this threshold, the turn on and turn off times of the semiconductor become significant with respect to the *ON* time itself.

As shown in Figs. 12b, 12d and 12f, the upper limit of the measured charging current exceeds the set I_{OFF} threshold. This is due to the reaction time of the SSBTS, that takes between $3\,\mu\mathrm{s}$ and $4\,\mu\mathrm{s}$ to interrupt the bus current after it crosses the tripping threshold of I_{OFF}. The DC bus current rate of increase can be expressed in first approximation by $\frac{V_{SSBTS}}{L_{didt}}$. The reaction time delay results in a further increase of the bus current of $30\,\mathrm{A}$ to $40\,\mathrm{A}$ above I_{OFF} at the beginning of the charging process, when the difference in voltage between the two buses is equal to the nominal DC voltage of $500\,\mathrm{V}$. As the unenergised bus progressively charges, the current increase rate decreases and the same switching delay corresponds to a reduced current increase over I_{OFF}. Fig. 14 highlights this by displaying the L_{didt} current during the initial and final pulses of the charging of a $2.3\,\mathrm{mF}$ capacitance with $I_{OFF} = 100\,\mathrm{A}$ and $I_{ON} = 75\,\mathrm{A}$. This is part of the expected operation of the SSBTS prototype as was shown in [10], [18]. Note also that the exceeding of the current threshold does not take place for I_{ON}, the lower current threshold. This is because the rate of decrease of current, given by Equation 1, is significantly lower during current decrease than during current increase. Therefore, the same reaction delay of $\approx 3.5\,\mu\mathrm{s}$ corresponds to a much smaller decrease of the current below the value of I_{ON}.

Overall, the test demonstrate that the soft-start function can be implemented with minimal additional effort on an existing SSBTS unit. Nevertheless, this kind of operation places additional stress on switching components of the device. Note that the device is not thermally sized for repeated switching actions, but only for always-on operation and conduction losses. For this reason, it was observed during testing that



(a) (b)

Fig. 14: Current in L_{didt} during the soft-start of a $2.3\,\mathrm{mF}$ DC bus capacitance at the beginning (a) and end (b) of the soft-start. For this test, $I_{OFF} = 100\,\mathrm{A}$ and $I_{ON} = 75\,\mathrm{A}$. The variation in the current rate of increase and overshoot is evident and dependant on the difference in voltage between the buses interfaced by the SSBTS.

the $1.8\,\Omega$ snubber resistor in particular reached temperatures of approximately $100\,^{\circ}\mathrm{C}$ during charging of an unenergised $6.9\,\mathrm{mF}$ bus. While the resistors employed in the prototype can operate at temperatures of up to $250\,^{\circ}\mathrm{C}$, it signals that additional increases in capacitance will result in additional losses and temperature increases. The increase in temperature of the snubber resistor constitutes a thermal bottleneck for soft-start operation and is a consequence of the design of the SSBTS being performed exclusively based on its primary protection function. Whether this is acceptable or not depends on the maximum acceptable capacitance C_{charge} that the system will require the SSBTS to soft-start. This may lead to the need to increase the power dissipation ability of the snubber resistors. In the topology discussed in this paper, the total energy dissipated in the snubber resistors per switching cycle allows for the calculation of the snubber resistor average power during a soft-start as:

$$P_{snubber} = \frac{R_s I_{OFF} V_{MOV} C_s + \frac{1}{2} C_s V_{MOV}^2}{L_{didt}(I_{OFF} - I_{ON})} V_{D_L}, \quad (9)$$

where R_s is the snubber resistor and C_s the snubber capacitor. Being aware of the dissipated power in the snubber resistor allows the user to determine the maximum duration of the soft-start operation with an existing SSBTS. Alternatively, this allows for the selection of a new snubber resistor R_s with a suitable nominal power and thermal capacity based on the required duration of the soft-start.

VI. Conclusion

This paper has presented an SSBTS soft-start method and its experimental validation. The method provides additional functions to an SSBTS purely on a control basis and without alterations of its protection-oriented design. A detailed description of the operation of the SSBTS in soft-start mode is given and experimental results and validation are provided. The results demonstrate the ability of the device and proposed method to provide soft-start of a variety of different capacitance values, therefore removing the need of *ad-hoc* precharge components and reducing the size, cost and complexity of the system.

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