



© 2020 IEEE

IEEE Access, pp. 1–1, 2020

Protection Coordination for Reliable Marine DC Power Distribution Networks

S. Kim, G. Ulissi, S.-N. Kim, *et al.*

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of EPFL's products or services. Internal or personal use of this material is permitted. However, permission to reprint / republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2020.DOI

Protection Coordination for Reliable Marine DC Power Distribution Networks

SEONGIL KIM¹, (Member, IEEE), GABRIELE ULISSI¹, (Student, IEEE), SOO-NAM KIM²,
DRAZEN DUJIC¹, (Senior, IEEE)

¹Power Electronics Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne 1015, Switzerland
(e-mail: seongil.kim@epfl.ch, gabriele.ulissi@epfl.ch, and drazen.dujic@epfl.ch)

²Future Power Grid Research Department, Hyundai Electric & Energy Systems Research Centre, Yongin 16891, Republic of Korea
(e-mail: kimsoonam@hyundai-electric.com)

Corresponding author: Seongil Kim (e-mail: seongil.kim@epfl.ch).

This work was supported by Hyundai Electric & Energy Systems, Republic of Korea

ABSTRACT This paper presents demonstration of a protection scheme integrated into marine DC power distribution networks to investigate the coordination between each protection action. The integrated protection scheme is based on three different time-frame protection actions: fast action - bus separation by a solid-state bus-tie switch, medium action - feeder protection by high-speed fuses, and slow action - power supply protection by generator deexcitation. As the backup protection of the power supply protection, AC fuses are installed between generators and rectifiers. To coordinate each protection action, the influences of the inductance in the bus-tie switch and the DC-link capacitance are investigated by DC short-circuit tests with the different inductance and capacitance values. The protection scheme, coordinated by the above investigation, is verified by system-level short-circuit tests for bus and feeder faults. To validate the protection scheme for various fault conditions, low- and high-impedance fault currents are analytically calculated for the bus faults and simulated for the feeder faults. Time-current curve analyses show that the coordinated protection scheme can effectively protect marine two-bus DC power distribution networks with correct operations of the protection measures and enough time margins between the different actions.

INDEX TERMS DC Microgrid, Generator Deexcitation, Marine Power Distribution Networks, Protection Coordination, Shipboard Power Systems, Solid-State Circuit Breaker.

I. INTRODUCTION

THE marine sector has endeavoured to mitigate its impact on global warming, targeting to cut down energy consumption by 30% by 2025 from the level in 2004 [1]. Since 2013, as one of the solutions to achieve the goal, low-voltage DC (LVDC) technologies have been employed into commercial marine power distribution networks (PDNs) with their outstanding benefits: fuel savings with utilisation of variable-speed generation systems, easy integration of energy storage systems, weight and footprint reduction in electrical installations, and optimisation of running engines by closed-bus operation [2]–[6].

Currently, several industrial manufactures are the main players to push the market forward with their DC solutions, as summarised in Table 1. The protection schemes of the DC solutions are commonly composed of three-different time frame protection actions (three-level protection in the paper):

- fast action (the first level) - bus separation by solid-state bus-tie switches (SSBTSs) (up to several tens of microseconds)
- medium action (the second level) - feeder protection by high-speed fuses or solid-state circuit breakers (SSCBs) (up to a few milliseconds)
- slow action (the third level) - power supply protection by generator deexcitation, fold-back protection control, high-speed fuses, or SSCBs (up to several seconds).

When the feeder fault occurs in Fig. 1, the SSBTS rapidly separates the DC buses in a range of several tens of microseconds (fast action). After that, the high-speed fuse on the faulty feeder isolates the fault from the system in a few milliseconds (medium action). As the last action, the power supply protection eliminates the fault contribution of the generator for the feeder protection failure or the DC bus fault (slow action). The power supply protection is strongly linked to the rectifier type. In case of a diode rectifier, deexcita-

TABLE 1. Marine LVDC solutions and their protective devices [7]–[10]. Whereas a synchronous generator (SG) is combined with all rectifiers, a permanent magnet synchronous generator (PMSG) is only coupled with a voltage source converter (VSC) due to the lack of its excitation control.

	Siemens	ABB	Ingeteam	The Switch
Solution	BlueDrive PlusC	Onboard DC Grid	E3-Ship	DC-Hub
Power supply				
Generator	SG	SG	SG/PMSG	SG/PMSG
(AC voltage)	(0.69 kV)	(N/A)	(0.69 kV)	(N/A)
Rectifier	Diode	Thyristor	VSC	VSC
(DC voltage)	(0.93 kV)	(1 kV)	(1.5 kV)*	(1 kV)
Protective device				
Bus separation		SSBTS		
Feeder protection	Fuse	Fuse	Fuse	SSCB
Power supply protection (Backup)	Deexcitation with high X_d''	Fold-back protection (Fuse)	Fuse	SSCB

* Note: The voltage rating of the SSBTS in [7].

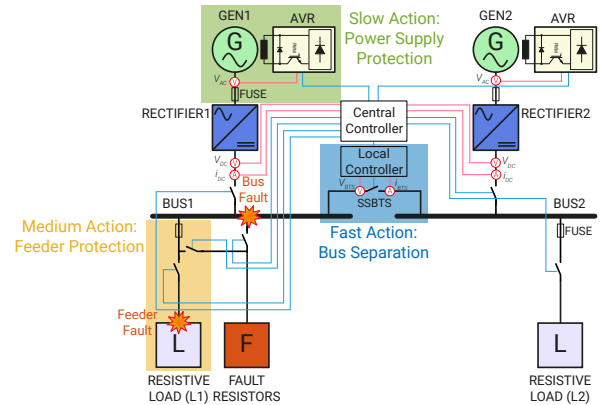


FIGURE 1. Schematic diagram of lab-scaled test setup to replicate marine two-bus DC PDNs with integrated three-level protection.

tion of a synchronous generator, specially designed to have high subtransient reactance (X_d''), is used to limit the fault current from the generator [11]. The amplitude of an initial DC fault current can be mitigated by the high subtransient reactance value. A generator protection unit, on the other hand, removes the excitation for eliminating the fault current generated from the generator when the overload condition is detected. A thyristor rectifier can manage the fault current by forcing the firing delay angle (e.g., around 120° , called fold-back protection control) [12], [13], whereas a high-speed fuse and a SSCB are commercially employed for the VSC protection [9], [10] (see Table 1).

In the three-level protection, the protection actions should be coordinated to ensure the proper operation of the SSBTS, faster than the fuse operation, and the continuous operation of adjacent healthy loads installed in parallel to the faulty feeder. For the first point, the current limiting inductor in the SSBTS (L_{lim} in Fig. 3) should be carefully selected. If the inductance value is not properly selected, it may cause the breaking failure (too low inductance) or the coordination failure (too high inductance). Note that the sizing of the current limiting inductor is presented in Section III. The continuous operation of the adjacent healthy loads is greatly related to the capacitance existed in the faulty bus. In general, the high capacitance helps not only to reduce the fault clearing time by the faster fuse operation, but also to maintain the voltage of the bus at which the fault occurs [14], [15].

To prove the fault ride-through capability, the works of [9], [16], [17] introduced one experimental test result on fault clearing by the three-level protection against the feeder fault. The test result showed that marine LVDC PDNs in [9], [16], [17] were protected by exact operations of an integrated SSBTS and an installed fuse on the faulty feeder (i.e., the

fast action, followed by the medium action). However, the works did not cover technical descriptions and discussions on the protection coordination, the current limiting inductor influence, the DC-link capacitance influence, and their selection as those are crucial for the coordination between the protection actions. Furthermore, the protection method was verified only with one fault resistance case in the works.

For the bus fault in Fig. 1, the two DC bus sections are separated first and then the fault current provided by a synchronous generator is blocked by the power supply protection (i.e., the combination of the fast action and the slow action for the bus fault). If the generator deexcitation is used for the power supply protection, the rectifier should be rigorously sized to sustain relatively high fault energy due to its slow fault blocking ability [18]–[20]. As the diode rectifier is a critical device in power supply systems, the backup protection can be considered to improve the reliability of the protection scheme. Once the backup protection is employed, it is also necessary to coordinate the power supply protection and the backup protection.

There are works to investigate each power supply protection measure in [9], [13], [21]. However, the works focused on each measure and its performance, not dealing with the coordination between the actions and the study on the system-level protection scheme, which are covered in this paper. It should be mentioned that most of the works for marine LVDC PDNs have been conducted by industrial manufacturers. They have published limited information on their solutions to protect their knowledge from being used by others, especially in the technical background of the system protection as it is one of the key technologies.

As described above, the three-level protection has been employed by the industrial manufacturers and the several works introduced its fault management performance. However, with the lack of information regarding the protection coordination, there are technology gaps in system design, protective device setting, and protection coordination verification for various fault resistances. Hence, this paper tackles these gaps by demonstrating the whole process of the system protection along with technical discussions on

the coordination: two-bus DC PDN implementation, device setting, protection scheme integration, and its system-level verification. For this purpose, this paper presents experimental and analytical verifications of the three-level protection in marine DC PDNs, designed and coordinated under in-depth technical assessments. Complete lab-scaled two-bus DC PDNs are implemented with the integrated three-level protection (fast action - bus separation by a SSBTS, medium action - feeder protection by high-speed fuses, slow action - power supply protection by generator deexcitation, and backup protection by AC fuses). Section II describes the hardware test setup, which is to replicate marine two-bus LVDC PDNs, for experimental short-circuit tests and system-level protection scheme study. The influences of the current limiting inductance and the DC-link capacitance are investigated by relevant experimental tests in Section III. In the same section, protective devices and their setting are also introduced. Section IV presents the performance of the implemented protection scheme with experimental and analytical approaches. The last section summarises the findings and the main results.

II. HARDWARE TEST SETUP

The hardware test setup to replicate marine two-bus DC PDNs of 500 V consists of two DC motor-generator sets, two diode rectifier systems, protective devices (a SSBTS and AC/DC fuses), resistive loads, fault resistors, and a central controller, as shown in Fig. 1. Note that the employed fuses are described in the next section.

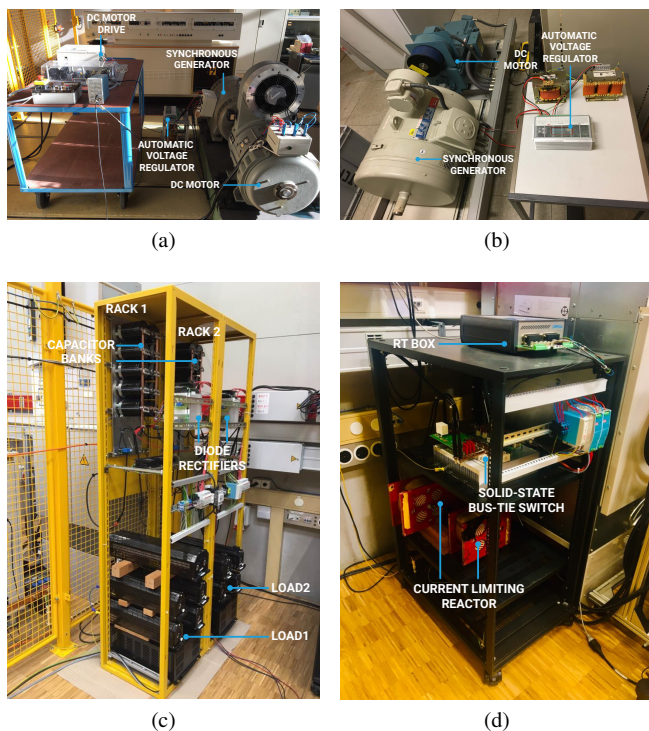


FIGURE 2. Actual implementation of lab-scaled two-bus DC PDNs: (a) GEN1, (b) GEN2, (c) rectifier systems, and (d) SSBTS.

A. POWER SUPPLY SYSTEMS

Two DC motor-generator sets are installed in the test setup: the first set (GEN1) - 10 kW, 380 V; and the second set (GEN2) - 25 kW, 380 V. Each set includes a DC motor drive, a DC motor, and a synchronous generator combined with an automatic voltage regulator (AVR), as shown in Fig. 2a and Fig. 2b. The DC motor driven by the thyristor-based motor drive acts as a prime mover, mimicking a diesel engine typically found in the onboard networks. The generators are based on direct excitation and their terminal voltages are directly regulated by ABB Unitrol 1005 AVRs that utilise a buck converter topology [22].

To establish the diode-based DC solution in Table 1, three-phase six-pulse diode rectifiers (SEMIKRON SKKD 100/16 [23]) are assembled in the rack (see Fig. 2c) and they are coupled with DC-link capacitor banks. The capacitor banks are designed to adjust the DC-link capacitance values from 2.3 mF to 11.5 mF.

B. SOLID-STATE BUS-TIE SWITCH

A SSBTS developed in the works of [24], [25] is installed in the test setup, as shown in Fig. 2d. The SSBTS has the following ratings: nominal voltage - 600 V, rated current - 100 A, and maximum allowed current - 200 A.

The SSBTS uses a four-quadrant switch topology [four

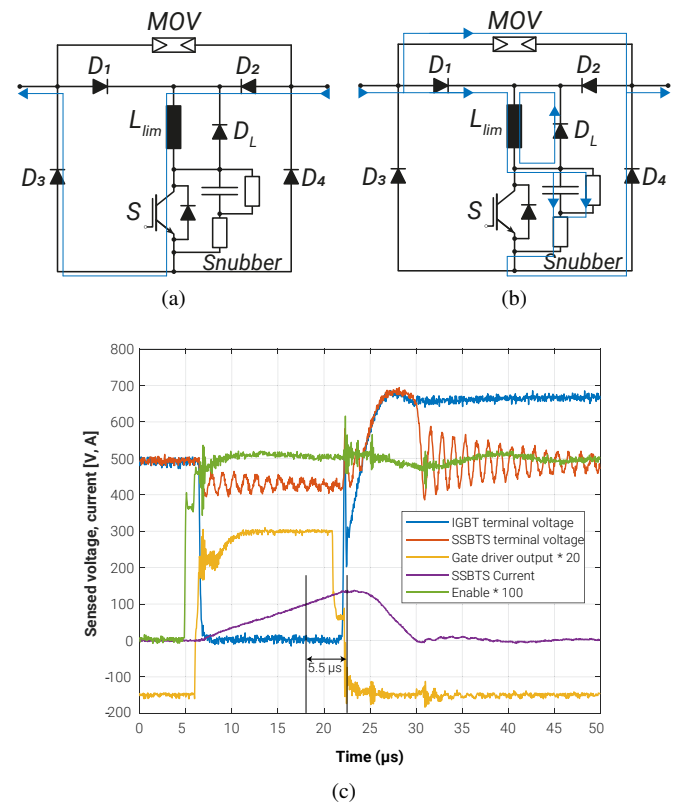


FIGURE 3. Operational principle and breaking performance of the SSBTS: (a) current path in normal operation with right-side supply, (b) current path in right-side fault condition after the IGBT is turned OFF, and (c) breaking test result taken from [24].

diodes (D_1 , D_2 , D_3 , and D_4) and one IGBT module (S) with a current limiting reactor (L_{lim}) and a freewheeling diode (D_L) in series to the IGBT module, as illustrated in Fig. 3. An RC snubber and metal oxide varistors (MOVs) are employed for retaining transient overvoltages during the interruption.

The right-side supply forces to flow the current through D_2 , L_{lim} , S , and D_3 if the IGBT is the *ON*-state (see Fig. 3a). For the left-side supply, the current direction is the opposite, i.e., the current flows through D_1 , L_{lim} , S , and D_4 . The IGBT module is first turned *OFF* in the event of a fault. This forces the overcurrent to flow through the snubber circuit and the MOVs (see Fig. 3b). The energies stored in the current limiting inductor and the system stray inductance are dissipated by the diode of D_L and MOVs, respectively, until the interruption is terminated.

To select the current limiting inductor, it is necessary to check the time to interrupt the fault current after the instant of the threshold level (time delay in the paper). For this purpose, the breaking test result conducted in the work of [24] is provided in Fig. 3c. When the current reaches the threshold value of 100 A, the SSBTS starts to interrupt the current. Total clearing time under the test condition is about 15 μ s. This result shows that the SSBTS can autonomously detect and clear the fault current within several tens of microseconds that is required for achieving the three-level protection, and the time delay between the detection and the interruption is observed as approximately 5.5 μ s. Note that the current limiting inductor shown in Fig. 2d is large because it has a current rating of 1 kA, available in the laboratory. The actual required component can be much smaller.

C. CENTRAL CONTROLLER

A central controller for the system control and protection is realised with Pixsys TD820 that is a human-machine interface panel with an integrated programmable logic controller (PLC) [26]. The central controller controls the AVRs to regulate DC bus voltages under normal conditions as well as to remove the excitation under fault conditions. The controller also handles the SSBTS by talking with its local controller (PLEXIM RT Box in Fig. 2d [27]), as depicted in Fig. 1. Moreover, it manipulates switches to generate feeder and bus fault conditions. Two resistors of 2 Ω in parallel are used and the fault resistance including the stray and line resistances is 1.3 Ω . Note that the bus separation by the SSBTS is done by its local controller (RT Box) with its sampling rate of 1 μ s in case of a fault event.

III. IMPLEMENTATION OF PROTECTION SCHEME

DC faults are highly sensitive on system parameters (equivalent inductance and equivalent capacitance existed in a fault circuit) [28] and thus their impacts on the faults should be examined to design the protection scheme. In this section, the influences of the current limiting inductance in the SSBTS and the DC-link capacitance are investigated with relevant experimental tests. From the investigations, the whole pro-

tection scheme and its setting are established and applied to the lab-scaled two-bus DC PDNs.

A. INFLUENCE OF THE CURRENT LIMITING INDUCTANCE

A DC short-circuit fault in the DC networks results in a voltage drop at the bus at which the fault occurs. This voltage drop generates the potential difference between the healthy bus and the faulty bus. The potential difference finally causes the current flow from the healthy bus to the faulty bus. The current limiting inductor in the SSBTS plays a role to control the rate of rise of this current.

Once the fault current passing through the SSBTS reaches the threshold value, it interrupts the current after the time delay, aforementioned, i.e., an actual breaking current is higher than the threshold current due to the current increase during the time delay. If the inductance is too small, the fault current level at the interruption instant may be higher than the breaking current rating (the maximum allowed current rating) of the SSBTS. On the other hand, if it is too high, the high inductance significantly decreases the rate of the current rise. This may cause the time coordination failure between the fast action and the medium action (an example case of this failure is shown in Fig. 4). Hence, the basic principle for the inductor sizing is to select the minimum inductor value that does not cause the breaking failure under the worst condition. With this principle, the required inductance can be calculated by

$$L_{lim} \geq V_d \frac{\Delta t}{\Delta i} \quad (1)$$

As shown in Fig. 3c, the SSBTS integrated in the test setup takes around 5.5 μ s to interrupt the fault current after the detection. In addition to that, the maximum allowed current of the SSBTS is 200 A. As 40 A (2 pu of the GEN1 current rating) is selected for the threshold current in the paper, Δt and Δi in the test setup are 5.5 μ s and 160 A ($= 200 \text{ A} - 40 \text{ A}$), respectively. With these parameters, the required inductance is 17.2 μ H by the consideration of the worst condition ($V_d = 500 \text{ V}$). However, in practice, there is no zero impedance fault and the voltage decreases with

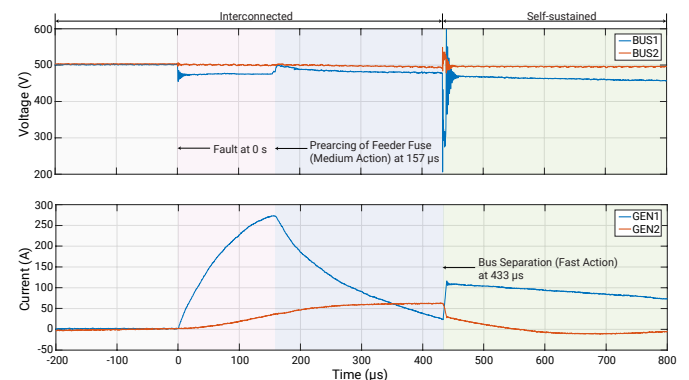


FIGURE 4. Example case of time coordination failure. With 48 μ H of the current limiting inductance, the current rise through the SSBTS is highly decreased. This makes the feeder fuse to be blown before the bus separation.

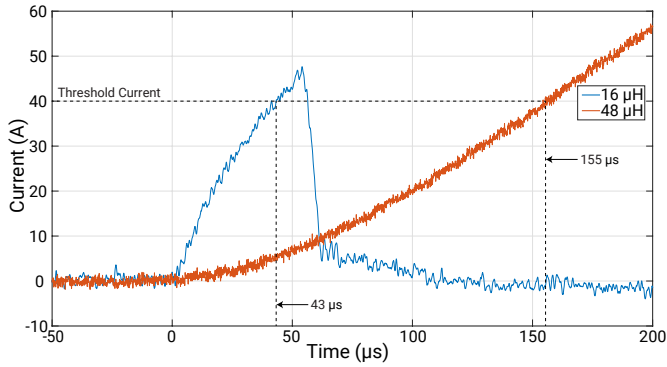


FIGURE 5. Comparison of the rates of the current rise for different current limiting inductance values.

the time constant of the system capacitance and the fault resistance. This allows the networks to employ slightly lower inductance. Based on this technical review, the inductor of 16 μH , which was available in the laboratory, is installed in the SSBTS (see Fig. 2d).

The other reason why this low inductor is employed is related to the fault identification time in the SSBTS controller. The decreased rate of the current rise by the high inductance value makes the local controller needing more time to identify the fault. DC short-circuit tests with the fault resistance of 1.3 Ω are carried out to clearly show the relationship between the current limiting inductor values and the rates of the current rise. The currents passing through the SSBTS for 16 μH and 48 μH are shown in Fig. 5. For 16 μH , the current reaches the threshold current of the SSBTS (40 A in the paper) at 43 μs . On the other hand, it takes 155 μs in the case of 48 μH .

The rate of the current rise also depends on the fault resistance value. As shown in Fig. 9d in Section IV, the lower fault resistance develops the higher current rise rate, i.e., the faster fault identification is possible. This lower fault resistance also decreases the fault clearing time by the high-speed fuse. Hence, to achieve the correct operation between the fast action and the medium action, the two DC bus sections have to be separated as fast as possible. In other words, the high value of the current limiting inductance may cause the time coordination failure between the actions.

B. INFLUENCE OF THE DC-LINK CAPACITANCE

In the three-level protection, the higher DC-link capacitance value can generally help to realise the lower fault clearing time of the feeder fuse as well as the lower bus voltage drop. DC short-circuit tests with the fault resistance of 1.3 Ω are conducted to investigate the described general influence of the DC-link capacitance on the system protection. As presented in Fig. 6, when the fault occurs at BUS1 in Fig. 1, the SSBTS is turned OFF at around 50 μs and then the prearcing of the feeder fuse is started at around 170 μs . These actions are similarly observed for all the test cases. On the other hand, the fault clearing time and the bus voltage are different depending on the included DC-link capacitor values. For 2.3

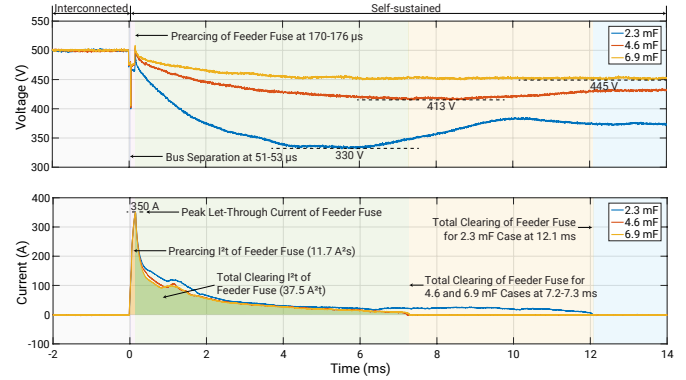


FIGURE 6. Influence of the DC-link capacitance on the bus voltage. Higher DC-link capacitance allows for reducing the voltage drop and the fault clearing time. The IR semiconductor fuse used for the feeder protection is also characterised due to the lack of its datasheet.

mF, the total clearing by the fuse happens at 12.1 ms and the minimum voltage is 330 V. Those become 7.2 ms and 413 V, respectively, in case of the DC-link capacitance with 4.6 mF. By increasing the total capacitance to 6.9 mF, the voltage drop can be reduced around 0.1 pu (445 V) while there is no improvement of the total clearing time.

An inverter installed at every feeder may be disconnected if the bus voltage becomes lower than its undervoltage protection level. It implies that, to maximise the network availability, the adjacent healthy loads connected in parallel to the faulty feeder have to be operated continuously during the feeder fault clearing by the high-speed fuse, i.e., the remaining bus voltage should be higher than the undervoltage trip threshold. Considering this, the DC-link capacitance of 6.9 mF, allowing for around 0.1 pu voltage drop, is selected for the coordination purpose in the paper as the threshold setting value has to be lower than the steady state DC voltage tolerance limit (e.g., 0.1 pu [29]).

C. DEVICE SETTINGS AND PROTECTION SCHEME

The SSBTS including the current limiting inductor of 16 μH is used for the fast action (the bus separation). As the power rating of GEN1 is 10 kW, the threshold current of 40 A (2 pu) is selected to turn OFF the SSBTS.

For the medium action (the feeder protection), IR semiconductor fuses rated for 500 Vdc and 15 A are employed at each feeder. Due to the lack of its datasheet, the characteristics of the fuse is tested, as shown in Fig. 6. From the test, the fuse is characterised with its parameters: I_p (peak let-through current) - 350 A, prearcing I^2t - 11.7 A^2s , and total clearing I^2t - 37.5 A^2s .

The generator deexcitation is implemented in the central controller (the Pixsys PLC), as the slow action (the power supply protection). Once the controller detects the fault current, after a time delay (T_{ON_D}), the deexcitation command is sent to the AVR and then the IGBT in the AVR is turned OFF (see Fig. 7a). The used parameters are $i_{threshold} = 40$ A for GEN1 and 100 A for GEN2, and $T_{ON_D} = 0.1$ s.

As the backup protection of the power supply protection,

TABLE 2. Summary of protection scheme implemented in the test setup.

Fault type	Fast action	Medium action	Slow action
	Bus separation	Feeder protection	Power supply protection [Backup protection]
Feeder fault	SSBTS (pick up: 40 A, inst. operation)	DC fuse	Generator deexcitation (pick up: GEN1/GEN2 - 40/100 A, delay: 0.1 s) [AC fuse]
	SSBTS (pick up: 40 A, inst. operation)		Generator deexcitation (pick up: GEN1/GEN2 - 40/100 A, delay: 0.1 s) [AC fuse]

Mersen AC fuses rated for 690 Vac and 160 A are installed between the generators and the rectifiers. The parameters of the fuse are found from the datasheet [30]: prearcing $I^2t - 2.68 \text{ kA}^2\text{s}$ and total clearing $I^2t - 16 \text{ kA}^2\text{s}$. The overall diagram of the protective devices is depicted in Fig. 7b. The protective devices and scheme, described above, are summarised in Table 2.

In this protection scheme, the fault detection relies on overcurrent criteria in Table 2. On one hand, the SSBTS instantly breaks the overcurrent if the current passing through the SSBTS is higher than the pick up level (40 A in the study) within several tens of microseconds. On the other hand, once 2 pu of the overcurrent through the rectifiers flows for 0.1 s (see Table 2), the generator excitation (the last action) is removed by the block diagram depicted in Fig. 7a. This means that the feeder fault can also be picked up for the last

action. However, there may be no operation of the last action if the fuse on the faulty feeder correctly clears the fault in a time range of a few milliseconds as the turn-on delay applied in the study is 0.1 s.

The implemented protection scheme can autonomously localise DC faults by the three-different time frame actions. For the feeder fault in Fig. 1, the SSBTS disconnects the two bus sections and then the fault is isolated by the high-speed fuse. These bus and feeder disconnections indicate the feeder fault. The bus fault in Fig. 1 causes the bus disconnection, followed by the generator deexcitation. These actions provide the information on the occurrence of the bus fault. As most of marine LVDC PDNs in [7]–[10] are based on the centralised configuration in which all the DC parts are located in the metallic cabinets. Hence, the fault distance in the DC networks is less important in marine LVDC PDNs.

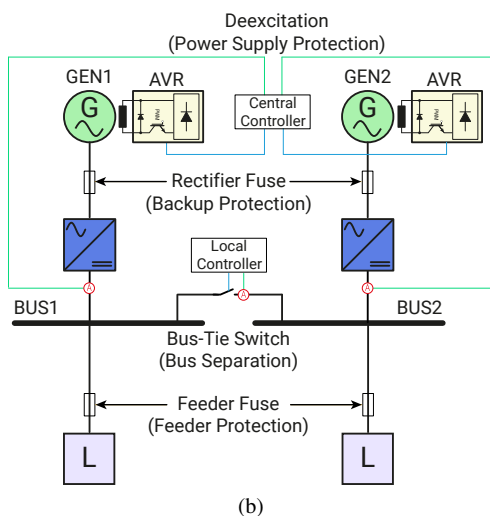
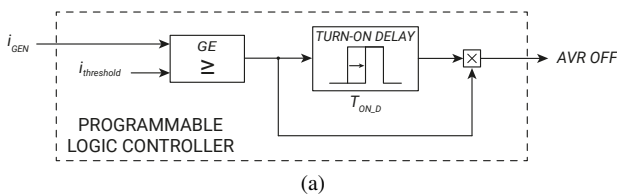


FIGURE 7. (a) Block diagram of deexcitation control and (b) overall protection scheme.

IV. VERIFICATION OF PROTECTION SCHEME

The whole protection scheme is validated by the experimental short-circuit tests with the bus and feeder faults. For further verification for various fault conditions, low- and high-impedance fault currents are calculated by a fault current equation for the bus faults and by a PLECS simulation for the feeder faults.

A. PROTECTION FOR BUS FAULTS

The protection performance for the bus fault is first examined by the DC short-circuit test on BUS1, as shown in Fig. 8a. The fault with its resistance of 1.3Ω develops the voltage drop on BUS1 and it results in the current flows from both power supplies (GEN1 and GEN2) to the fault point (see Fig. 8b). The fast action happens at $61 \mu\text{s}$ and this ultra-fast bus separation allows BUS2 to be operated independently with almost no influence of the fault event. On the other hand, there is the fault current contribution from GEN1 (I_{GEN1}) after the bus separation. In the continuous-time current, the first peak of I_{GEN1} is provided by the DC-link capacitor with a short time constant and then the generator becomes the main source of the fault current with a relatively high time constant. At 0.1 s, the AVR is turned OFF to remove the excitation of the synchronous generator. This deexcitation

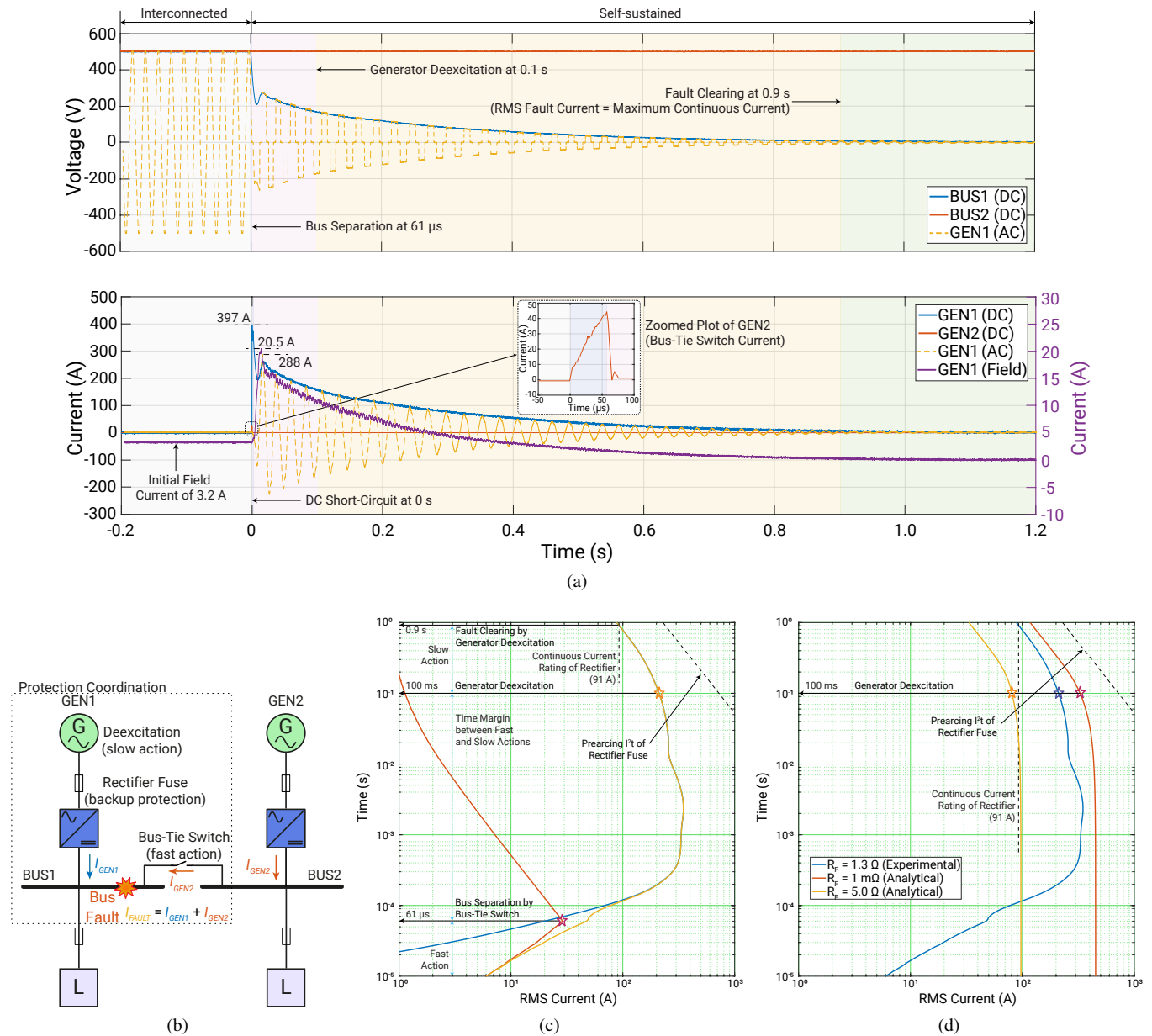


FIGURE 8. Protection for bus faults: (a) continuous-time voltage and current waveforms, (b) protection scheme diagram, (c) time-current curve (TCC) analysis for the tested condition, and (d) TCC analysis for different fault conditions. For the bus fault at BUS1, the SSBTS is disconnected at 61 μ s (the zoomed plot is provided) and the deexcitation of GEN1 is activated at 0.1 s. The TCC analyses show that the coordination is achieved between the bus separation and the deexcitation as well as between the deexcitation and the backup protection.

diminishes the bus voltage and the fault current in time and finally makes them zero.

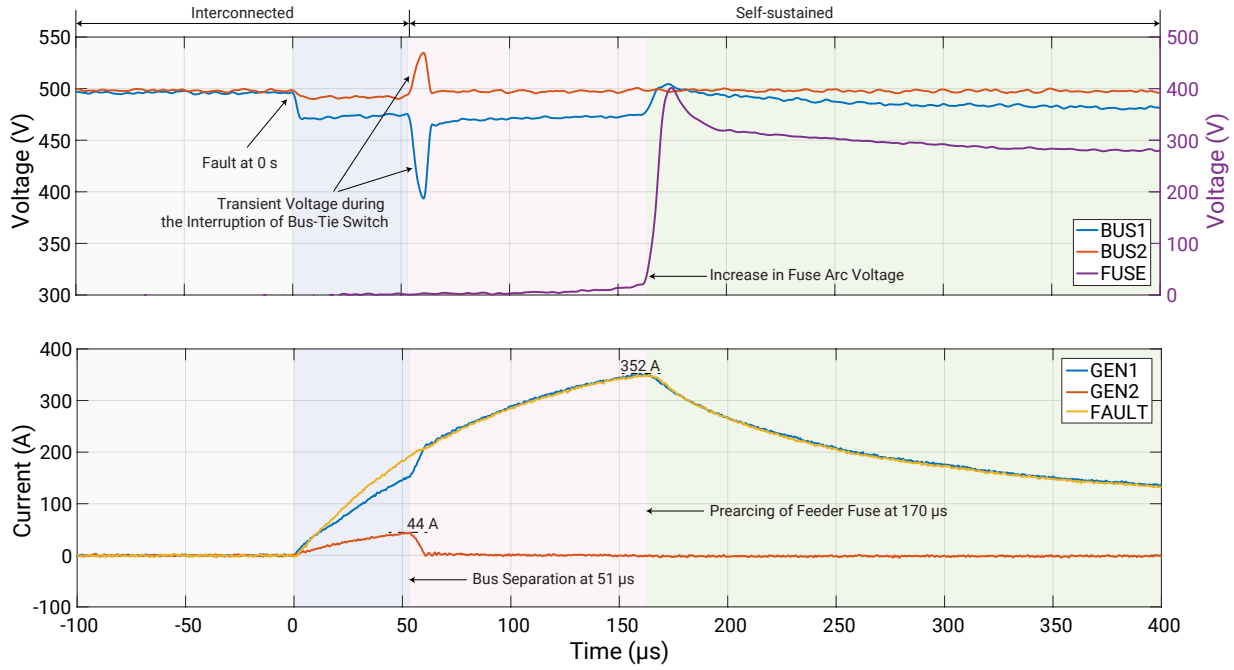
For the analysis by using a time-current curve (TCC), the continuous-time fault current (i_F) is converted to a RMS current (i_{F_RMS}) by

$$i_{F_RMS} = \sqrt{\frac{1}{T} \int_0^T i_F^2 dt} \quad (2)$$

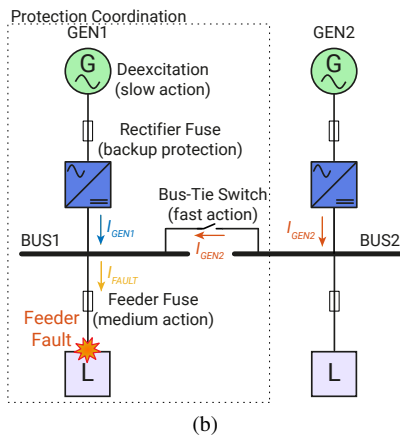
The RMS current is drawn in Fig. 8c and compared to the operating time of the backup protection (the AC fuse). The result shows that the deexcitation effectively mitigates the fault current without the operation of the backup protection and also the time margin between them is enough.

The current limited by the deexcitation is decreased exponentially, i.e., it decreases quickly first and takes a relatively long time to make it completely zero. Hence, the time when the RMS current is the same as the continuous current rating of the rectifier is selected to be a fault clearing time in the paper. At 0.9 s, the RMS current reaches the continuous current rating of 91 A and the continuous-time current is around 6 A.

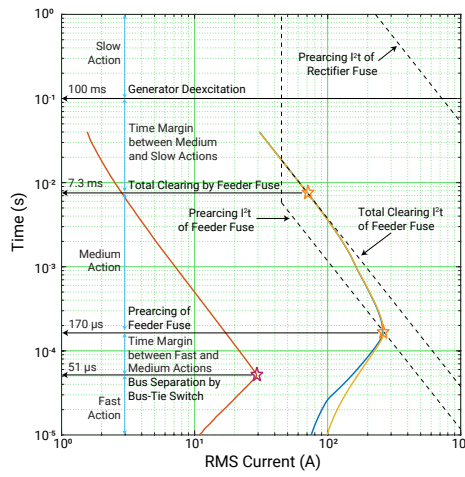
While the protection scheme successfully handles the DC short-circuit fault of 1.3 Ω , it does not guarantee that the DC networks can be protected from other fault conditions. Therefore, its performance should be verified for different fault conditions. For this purpose, fault currents limited by



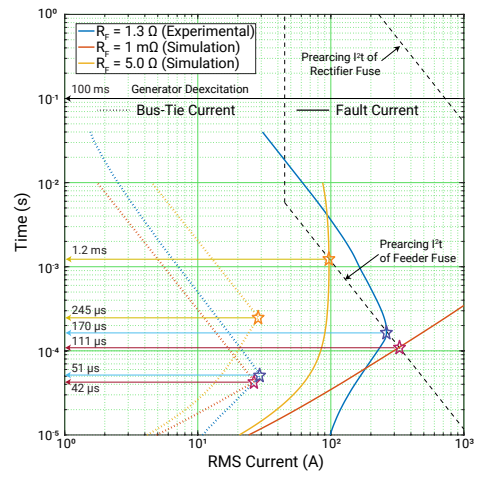
(a)



(b)



(c)



(d)

FIGURE 9. Protection for feeder faults: (a) continuous-time voltage and current waveforms, (b) protection scheme diagram, (c) TCC analysis for the tested condition, and (d) TCC analysis for different fault conditions. For the feeder fault at BUS1, the SSBTS is disconnected at 51 μ s and the pre-arcing of the feeder fuse is started at 170 μ s. The TCC analyses show that the coordination is achieved between the bus separation and the feeder protection.

the generator deexcitation with the fault resistance values of 1 m Ω (assumed as a low-impedance fault condition) and 5 Ω (2.5 times of the power rating of GEN2, as a high-impedance fault condition) are calculated by the equation for the fault current calculation under the deexcitation introduced in [31]:

$$i_F(t) = \sqrt{2}E_0Y(t)F(t) \quad (\text{no damper winding condition}) \quad (3)$$

where, the parameters of $i_F(t)$ are provided in Appendix.

Fig. 8d shows that the DC short-circuit fault with $R_F = 1$ m Ω generates the much higher fault current (red line) than the tested case (blue line). Nevertheless, this low-impedance fault can be managed by the generator deexcitation without the operation of the backup protection. In case of the high-

impedance fault ($R_F = 5$ Ω , yellow line), the continuous-time current at 0.1 s is observed as 70 A and this current is high enough to operate the deexcitation (the threshold level of 40 A). It is expected that the high-impedance fault can be cleared more easily.

B. PROTECTION FOR FEEDER FAULTS

The feeder protection should be more carefully coordinated due to the small time margin between the fast action and the medium action. In the previous section, the influences of the current limiting inductance and the DC-link capacitance were investigated and they were selected as 16 μ H and 6.9 mF, respectively. With these parameters, a DC short-circuit fault of 1.3 Ω at the BUS1 feeder is artificially generated (see

Fig. 9b) and the continuous-time waveforms during this event are presented in Fig. 9a.

In this test, the two DC bus sections are disconnected by the SSBTS (the fast action) and then the feeder fuse isolates the feeder fault (the medium action). The protection scheme based on the three-level protection is correctly operated for the feeder fault without the operation of the generator deexcitation (the slow action). In detail, the two DC bus sections are decoupled at 51 μs after the fault and then the feeder fuse starts its melting at 170 μs . This prearcing (or melting) of the fuse is also observed by the sudden increase in the fuse arc voltage at the same instant (purple voltage line). At 7.3 ms, the fault is completely cleared by the fuse (see Fig. 6). Similarly to the case of the bus fault test, BUS2 can be sustained solely by the ultra-fast bus decoupling. The BUS1 voltage drops below the minimum steady state tolerance limit (i.e., 450 V) at the instant of the SSBTS breaking for around 10 μs . Except this period, the voltage levels are within the limits. Hence, the adjacent inverters (if they are installed) may maintain their operations by filtering out this short period transient in their undervoltage protection.

To confirm the protection scheme for different feeder fault conditions, the DC short-circuit currents under the low- and high-impedance feeder faults are simulated by PLECS that is a software tool for system-level simulations. The system modeling is simplified as the combination of the DC-link capacitances at both buses, the current limiting inductor with a time-controlled ideal switch (disconnected in 5.5 μs after the threshold), and the fault resistance. The equivalent series resistance (38 m Ω /unit) and inductance (20 nH/unit) of the installed DC-link capacitor [32] are applied to the simulation and the result is compared to the test waveform, as shown in Fig. 10. With this simulation model, the fault current from GEN1 and the through SSBTS current (the fault current from GEN2) are calculated for the fault resistance values of 1 m Ω and 5 Ω , assumed as the low- and high-impedance fault conditions. Note that the prearcing of the feeder fuse is not considered in the simulation model and therefore there is no current interruption by the fuse.

The study result on the different fault conditions is presented in Fig. 9d. For the low-impedance fault ($R_F = 1$ m Ω , red line), the SSBTS is disconnected at 42 μs and the

fault energy reaches to the prearcing rating of the feeder fuse at 111 μs . Whereas the time margin between the actions is decreased to 69 μs (the time margin is 119 μs in case of the 1.3 Ω fault case, blue line), the coordination is still achieved. It implies that a low impedance fault develops a high fault current and this increased current reduces the operating time of the SSBTS as well as the feeder fuse. The bus separation is taken place with a relatively high time delay (245 μs) for the high-impedance fault of 5 Ω (yellow line). Along with this delayed operation, the feeder fuse is also melted slowly at 1.2 ms (the prearcing) due to the reduced fault energy.

From these investigations, the performance of the integrated protection scheme is verified for the possible feeder fault conditions. Hence, it could be stated that the protection scheme can provide reliable fault clearing not only with enough time margins between the fast action and the medium action, but also without the maloperation of the slow action.

V. CONCLUSION

This paper has presented coordination and verification of the protection scheme based on the three-level protection. For the study, the protection scheme is integrated into the marine two-bus DC PDNs and it consists of the bus separation by the SSBTS, the feeder protection by the high-speed fuses, and the power supply protection by the generator deexcitation. As the backup protection of the power supply protection, the AC fuses are also installed between the generators and the rectifiers. The coordination of each protection action is investigated by demonstrating the whole process of the system protection, such as, system design and implementation, protective device setting, protection scheme integration under in-depth analyses, and system-level experimental/analytical verifications.

The study results provide the important findings. First, the current limiting inductor in the SSBTS should be rigorously selected to ensure the fault interruption (not too small) and the coordination between the actions (not too high). Secondly, the higher DC-link capacitance helps not only to realise the less fault clearing time by the feeder fuse, but also to allow for the lower voltage drop of the faulty feeder. Lastly, the protection scheme has to be coordinated more thoroughly for the feeder faults as the allowed time margin is in a range of several tens of microseconds.

This paper has covered the protection coordination on the three-level protection composed of the SSBTS, the fuse, and the generator deexcitation. However, considering the various combinations of each protection measure (see Table 1), there are lots of future research perspectives in the protection coordination to be studied.

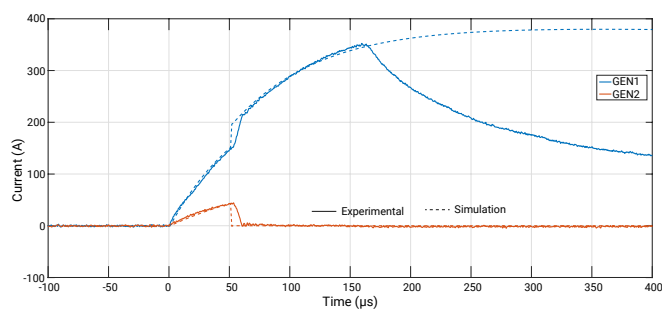


FIGURE 10. Comparison of experimental and simulation currents for the feeder fault of 1.3 Ω in the test setup.

VI. APPENDIX

The parameters of $i_F(t)$ in (3) are

$$Y(t) = \left(\frac{1}{\sqrt{R_{eq}^2 + X_d'^2}} - \frac{1}{\sqrt{R_{eq}^2 + X_d^2}} \right) e^{-\frac{t}{T_d}} + \frac{1}{\sqrt{R_{eq}^2 + X_d^2}} \text{ and}$$

$$F(t) = u(-t + t_d) + u(t - t_d) \frac{T_d' e^{-(t-t_d)/T_d'} - T_e e^{-(t-t_d)/T_e}}{T_d' - T_e}$$

where, $\sqrt{2}E_0 = 500$ V, $R_{eq} = 1.3$ Ω , $X_d = 9.8$ Ω , $X_d' = 1.1$ Ω , $T_d' = 0.12$ s, $T_e = 0.1$ s, and $t_d = 0.1$ s.

REFERENCES

- [1] "International Convention for the Prevention of Pollution from Ships (MARPOL)," *Resolution MEPC.203(62)*, pp. 1–19, Jul. 2011.
- [2] F. D. Kanellos, G. J. Tsekouras, and J. Prousalidis, "Onboard dc grid employing smart grid technology: challenges, state of the art and future prospects," *IET Electrical Systems in Transportation*, vol. 5, no. 1, pp. 1–11, 2015.
- [3] "Edda ferd platform supply vessel (PSV)," accessed 17 September 2020. [Online]. Available: <https://www.ship-technology.com/projects/edda-ferd-platform-supply-vessel/>
- [4] J. F. Hansen, J. O. Lindtjørn, and K. Vanska, "Onboard DC Grid for enhanced DP operation in ships," in *Dynamic Positioning Conference, Houston*, 2011.
- [5] S. O. Settemsdal, E. Haugan, K. Aagesen, and B. Zahedi, "New Enhanced Safety Power Plant Solution for DP Vessels Operated in Closed Ring configuration," in *Dynamic Positioning Conference, Houston*, 2014.
- [6] J. F. Hansen, F. Wendt, and J. O. Lindtjørn, "Fuel efficient power plant featuring variable speed generation system for DP drilling units," in *Dynamic Positioning Conference, Houston*, pp. 1–13, Oct. 2016.
- [7] "High efficiency, integrated compact power system for electric propulsion vessels," accessed 16 December 2019. [Online]. Available: <https://www.ingetteam.com/>
- [8] "Mastering dc distribution for ultimate marine drive efficiency," The Switch, accessed 20 March 2020. [Online]. Available: <https://theswitch.com/marine/>
- [9] S. O. Settemsdal, L. Barstad, and K. Tjong, "Fault ride-through testing of a lv power solution, bluedrive plusc," in *Dynamic Positioning Conference, Houston*, pp. 1–15, Oct. 2016.
- [10] "The Step Forward Onboard DC Grid," accessed 31 August 2018. [Online]. Available: <https://new.abb.com/>
- [11] R. B. Andersen, S. Blystad, I. Haukaas, G. Koenig, D. Radan, and S. O. Settemsdal, "Fault protection system for a power system of dynamically positioned vessel," Apr. 2012, EP Patent 2,654,156. [Online]. Available: <https://patents.google.com/patent/EP2654156A1/en>
- [12] J. Lindtjoern, "A dc-power system with system protection capabilities," Sep. 2015, EP Patent 2,634,885. [Online]. Available: <https://encrypted.google.com/patents/EP2634885B1?cl=zh-TW>
- [13] D. Dong, Y. Pan, R. Lai, X. Wu, and K. Weeber, "Active fault-current foldback control in thyristor rectifier for dc shipboard electrical system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 203–212, Mar. 2017.
- [14] S. D. A. Fletcher, P. J. Norman, S. J. Galloway, and G. M. Burt, "Determination of protection system requirements for dc unmanned aerial vehicle electrical power networks for enhanced capability and survivability," *IET Electrical Systems in Transportation*, vol. 1, no. 4, pp. 137–147, Dec. 2011.
- [15] S. Kim, S. Kim, and D. Dujic, "Extending protection selectivity in dc shipboard power systems by means of additional bus capacitance," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 5, pp. 3673–3683, 2020.
- [16] E. Haugan, H. Rygg, A. Skjellnes, and L. Barstad, "Discrimination in offshore and marine dc distribution systems," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–7, Jun. 2016.
- [17] S. O. Settemsdal and V. Wolfgang, "Dc powergrid for marine and offshore vessel," in *IEEE International Conference on DC Microgrids (ICDCM)*, Jun. 2017.
- [18] C. A. Platero, M. Redondo, F. Blazquez, and P. Frias, "High-speed de-excitation system for brushless synchronous machines," *IET Electric Power Applications*, vol. 6, no. 3, pp. 156–161, Mar. 2012.
- [19] E. Rebollo, F. R. Blazquez, C. A. Platero, F. Blazquez, and M. Redondo, "Improved high-speed de-excitation system for brushless synchronous machines tested on a 20 mva hydro-generator," *IET Electric Power Applications*, vol. 9, no. 6, pp. 405–411, 2015.
- [20] E. Rebollo, C. A. Platero, F. Blazquez, and R. Granizo, "Internal sudden short-circuit response of a new hsbds for brushless synchronous machines tested on a 15 mva generator," *IET Electric Power Applications*, vol. 11, no. 4, pp. 495–503, 2017.
- [21] S. Kim, D. Dujic, and S. Kim, "Protection schemes in low-voltage DC shipboard power systems," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1–7, Jun. 2018.
- [22] *UNITROL 1005 User Manual*, ABB, Aug. 2015.
- [23] *Three phase uncontrolled rectifier SKS 91N B6U 60 V16 SU*, SEMIKRON, Aug. 2015.
- [24] G. Ulissi, S. Y. Lee, and D. Dujic, "Solid-state bus-tie switch for shipboard power distribution networks," *IEEE Transactions on Transportation Electrification*, vol. 6, no. 3, pp. 1253–1264, Sep. 2020.
- [25] G. Ulissi, S. Y. Lee, and D. Dujic, "Scalable solid-state bus-tie switch for flexible shipboard power systems," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 239–247, 2021.
- [26] *HMI series 410-710-810-820 (2300.10.258-RevD)*, Pixsys.
- [27] "Rt box: The hil platform for power electronics," accessed 7 June 2020. [Online]. Available: <https://www.plexim.com>
- [28] K. Satpathi, A. Ukil, and J. Pou, "Short-circuit fault management in dc electric ship propulsion system: Protection requirements, review of existing technologies and future research trends," *IEEE Transactions on Transportation Electrification*, vol. 4, no. 1, pp. 272–291, Mar. 2018.
- [29] "Ieee recommended practice for 1 kv to 35 kv medium-voltage dc power systems on ships," *IEEE Std 1709-2018 (Revision of IEEE Std 1709-2010)*, pp. 1–54, Dec. 2018.
- [30] *Semiconductor protection fuses - square body high-speed fuse-links ac protection*, Mersen.
- [31] S. Kim, S.-N. Kim, and D. Dujic, "Impact of synchronous generator deexcitation dynamics on the protection in marine DC power distribution networks," *IEEE Transactions on Transportation Electrification*, pp. 1–10, 2020.
- [32] "Capacitors with screw terminals (b43564)," EPCOS.



SEONGIL KIM (S'18-M'20) received the B.S. and M.S. degrees from Hanyang University, Ansan and Seoul, Republic of Korea, in 2005 and 2007, respectively, and the Ph.D. degree from École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, in 2020, all in electrical engineering.

From 2007 to 2017, he was a Senior Researcher with Hyundai Heavy Industries Research Centre, Yongin, Republic of Korea, working on high voltage and power system engineering. Since 2017, he has been a Senior Researcher with Hyundai Electric and Energy Systems Research Centre, Yongin, Republic of Korea, working on the protection coordination of dc power systems. In 2017, he joined the Power Electronics Laboratory of École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland as a Full-Time Doctoral Assistant. He has recently received his Ph.D. degree. His current research interests include the areas of design, modeling and protection of dc power systems.

Dr. Kim was a recipient of the IEEE Transportation Electrification Conference and Expo (ITEC) Student Paper Award in 2020.



GABRIELE ULISSI (S'18) received his B.Sc. degree in electrical engineering from the Polytechnic of Turin, Italy, in 2016 and M.Sc. degree in electrical engineering from the École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, in 2018. Since 2018, he is a Doctoral Assistant with the Power Electronics Laboratory at École Polytechnique Fédérale de Lausanne (EPFL), Switzerland. His research focuses on semiconductor-based protection of DC systems.



SOO-NAM KIM received the B.S., M.S., and Ph.D. degrees in electrical engineering from Hanyang University, Ansan and Seoul, Republic of Korea, in 1996, 1998 and 2003, respectively.

From 2003 to 2017, he was a Head Researcher with Hyundai Heavy Industries Research Centre, Yongin, Republic of Korea, working on power system engineering for various areas. Since 2017, he has been a Senior Researcher with Hyundai Electric and Energy Systems Research Centre, Yongin, Republic of Korea, working on switchgear development for ships and smart grids. He is currently leading the Future Power Grid Research Department of Hyundai Electric and Energy Systems Research Centre. His current research interests include the areas of design and control of eco-friendly grids for ships, buildings and cities.

Dr. Kim was a recipient of the Minister's Award for Smart Grid, Republic of Korea, as a Meritorious Person, in 2012.



DRAZEN DUJIC (S'03-M'09-SM'12) received the Dipl. -Ing. and M.Sc. degrees from the University of Novi Sad, Novi Sad, Serbia, in 2002 and 2005, respectively, and the Ph.D. degree from the Liverpool John Moores University, Liverpool, U.K., in 2008, all in electrical engineering.

From 2002 to 2006, he was with the Department of Electrical Engineering, University of Novi Sad as a Research Assistant, and from 2006 to 2009 with Liverpool John Moores University as a Research Associate. From 2009 to 2013, he was with ABB Corporate Research Centre, Switzerland, as a Principal Scientist working on the power electronics projects spanning the range from low-voltage/power switched-mode power supply (SMPS) in below kilowatt range to medium voltage high-power converters in a megawatt range. From 2013 to 2014, he was with ABB Medium Voltage Drives, Turgi, Switzerland, as a R&D Platform Manager, responsible for ABB's largest integrated gate-commutated thyristor (IGCT) based medium voltage drive ACS6000. He is currently with École Polytechnique Fédérale de Lausanne EPFL, Lausanne, Switzerland, as an Assistant Professor in Electrical Engineering and the Director of the Power Electronics Laboratory. He has authored or coauthored more than 150 scientific publications and has filed 14 patents. His current research interests include the areas of design and control of advanced high-power electronics systems and high performance drives.

Dr. Dujic is an Associate Editor for the IEEE Transactions on Industrial Electronics, IEEE Transaction on Power Electronics, and IET Electric Power Applications. He is the recipient of the First Prize Paper Award by the Electric Machines Committee of the IEEE Industrial Electronics Society at IECON, in 2007. He was the recipient of the European power electronics and drives association (EPE) Outstanding Service Award in 2018, and the Isao Takahashi Power Electronics Award in 2014, for outstanding achievement in power electronics.

...