Output-Capacitance Hysteresis Losses of Field-Effect Transistors

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***Abstract*—Resonant-type power converters are supposed to generate zero switching losses during soft-switching operation. In recent research, unexpected switching losses were reported in these converters, which were attributed to a large-signal hysteresis observed in the output-charge versus voltage (*QV*) characteristics of the power device. Since these converters subject the power semiconductor switch to different levels of peak voltages based on design requirements, the dependence of hysteresis losses on the voltage range is important. In this work, planar-Si, Si super-junction, SiC and GaN power device structures are investigated, and categorized based on their *QV* patterns. We report that for different device technologies, the large-signal hysteresis patterns of output charge show diverse dependencies on the excitation voltage amplitude. The frequency dependence of the hysteresis losses is also analysed and discussed. The presented results provide important insights in identifying the root causes for output-charge hysteresis, and may help to improve device *spice* models to properly account for soft-switching losses.**

***Index Terms*—C_{oss}, hysteresis loss, output capacitance, Sawyer–Tower, soft-switching loss, wide-band-gap (WBG) devices.**

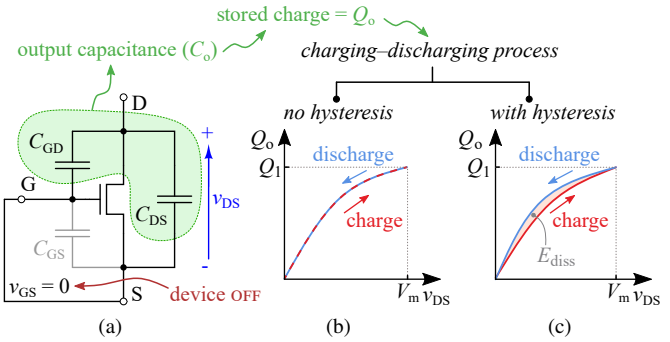

Fig. 1. (a) In resonant-type converters, the charging–discharging process of the output capacitance ($C_o = C_{GD} + C_{DS}$) of a transistor occurs while it is in OFF state, i.e., $v_{GS} = 0$ V. The related variation of the accumulated charge (Q_o) versus device drain–source voltage, v_{DS}, is represented by a *QV* curve. Two cases are possible: (b) without hysteresis; and (c) with hysteresis, where different charging (red line) and discharging (blue line) paths result in a hysteresis energy loss, E_{diss}, which is specified for a given maximum voltage V_m of v_{DS}.

I. Introduction

Resonant-type power converters are an attractive solution to achieving large power densities at high frequencies due to their soft-switching behaviour [1]–[3]. Their applications include, among others, computer power supplies [4], radio-frequency (RF) power amplifiers in communication systems [5]–[7], and wireless power transfer systems [8]. During a single switching cycle in these converters, the output capacitance, C_o, of the switching device is charged and discharged in a resonant manner dictated by the specificities of the topology, as means of achieving soft-switching conditions [1]. Since the device is in OFF state during the charging–discharging process of C_o, this ideally yields zero losses [2], [9]—see Figs. 1(a) and 1(b)—in comparison to hard-switching conditions [10].

However, it has been reported in recent research that, transition losses still exist due to dynamic charging and discharging of the power device's output capacitance under soft-switching conditions [2], [11]–[15]. The corresponding energy loss is attributed to a hysteresis loss [9], which is observed in large-signal charge versus voltage (*QV*) curves as shown in Fig. 1(c). Numerous works have reported such losses pertaining to different device structures: in Si Super-Junction (Si-SJ) transistors [13], [16], [17]; and wide-band-gap (WBG) SiC transistors [15], [18] and GaN high-electron-mobility transistors (HEMTs) [2], [14], [15], [19], [20].

The hysteresis energy loss in C_o is a function of the maximum (or peak) voltage, V_m, across the device's drain–source terminals, and is expressed as

$$E_{diss} = \int_0^{Q_1} v_{DS}\, dQ \; - \int_{Q_1}^{0} v_{DS}\, dQ, \qquad (1)$$

where $Q_1 = Q_o|_{v_{DS}=V_m}$. This energy loss adds an extra constraint on deciding the maximum voltage across a switching device for a given high- or very-high-frequency (HF or VHF) application. This is especially important in resonant converters, for example, in the classical class-E inverter where the device voltage stress could be quite high [5]. Even for converters with low voltage stresses, such as the class-ϕ_2 inverter [6], the circuit components are selected and tuned to achieve a given V_m value. Prior knowledge on the dependence of hysteresis energy losses with V_m, for the available devices, would allow to select the most suitable operational voltage range for the circuit. In light of this, the quantitative variation of the E_{diss} value with V_m has been published for some commercial devices [2], [15], [18]. Although this provides means of selecting a suitable device with lower losses, the

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understanding of how QV patterns vary with V_{m} for different device technologies is important in identifying the root cause for E_{diss}, and thus improving the device performance. This also aids in developing more realistic *spice* models to account for hysteresis losses.

In this work, four prominent field-effect transistor (FET) technologies are examined to observe how their QV patterns change with V_{m}. This allows the identification of voltage ranges upon where the hysteresis patterns emerge. The frequency dependencies are also studied. An overview on the QV hysteresis patterns between different device structures is provided, which is lacking in the literature. The paper is structured as follows. Section II describes the measurement process and introduces the basics of output capacitance hysteresis. Section III and Section IV investigate the dependence of QV patterns on excitation voltage and frequency, respectively. Section V provides a survey on the origin of E_{diss} losses in different device technologies and categorizes QV hysteresis patterns. Section VI concludes the paper.

II. Measurement of Output-Capacitance Hysteresis

This study concerns soft-switching losses in the frequency range of 10 kHz to 1 MHz. The test circuit operates such that the excitation voltage across the device drain–source terminals is of sinusoidal nature, while the gate–source terminals are shorted, i.e., $v_{\mathrm{GS}} = 0$ V. High-voltage Si, Si-SJ, SiC and GaN devices are tested up to a V_{m} of 400 V. To make a comparative study, twelve FETs are selected such that they have a current rating around 30 A. The part numbers, device technologies and other important details from the datasheets of the selected FETs are tabulated in Table I.

A. Experimental Setup and the Measurement Process

QV patterns related to device output capacitances are experimentally obtained using the Sawyer-Tower technique, which relies on only two voltage measurements [9], [21].[1] The circuit consists of a signal generator, a high-voltage amplifier, a fixed linear capacitor known as the reference capacitor, C_{ref}, and the device under test (DUT), as shown in Fig. 2. Since $v_{\mathrm{GS}} = 0$ V, the DUT is essentially a capacitance equal to C_{o} for positive v_{DS} values [9]. The series combination of the DUT and C_{ref} is subjected to a large-signal input voltage v_{IN} created by amplifying a low-voltage signal v_{S}, having an excitation frequency of f. In steady state, a dc bias (V_{REF}) is built across C_{ref}; this renders v_{DS} to vary between 0 V and V_{m} [9]. Since the same current flows through C_{o} and C_{ref} in steady state, the ac voltage ($v_{\mathrm{ref}} = v_{\mathrm{REF}} - V_{\mathrm{REF}}$) across C_{ref} is proportional to the variation of charge in both C_{ref} and C_{o} [9]: i.e.,

$$Q_{\mathrm{o}} \propto C_{\mathrm{ref}} \cdot v_{\mathrm{ref}}. \tag{2}$$

[1]The two voltages v_{REF} and v_{IN} are measured with a Tektronix MDO3104 oscilloscope (1 GHz) accompanied by TPP1000 passive voltage probes (1 GHz). The probe-end uses the MMCX square-pin adapter 131-9717-xx.

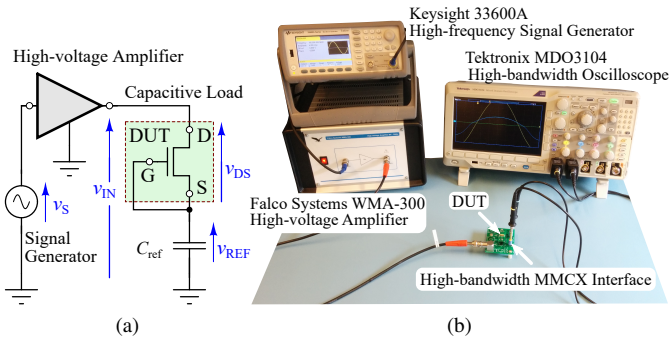

Fig. 2. (a) Schematic and (b) the experimental test setup of the Sawyer-Tower measurement technique used to analyse large-signal output capacitance.

Finally, the QV curves are extracted from the measured v_{REF} and v_{IN} data by using a simple MATLAB® script.[2]

Fig. 3 plots experimental QV curves of the selected devices for = 400 V and 100 kHz. The resulting E_{diss} is calculated by taking the area (shaded in orange in each sub figure) between the charging (solid red line) and discharging (solid blue line) paths. As the peak output voltage of the high-voltage amplifier was limited to $\pm$ 150 V (this limits V_{m} to 300 V), a HF transformer was utilized at the output of the amplifier to boost the voltage, so that V_{m} = 400 V was achievable. A C_{ref} of 1 nF was employed for all the devices, except for the Si devices 2–4, where a C_{ref} of 47 nF was used. This is because the large Q_{o} values ($\geq$ 250 nC) of these three devices cause too large a variation in v_{ref} for $C_{\mathrm{ref}} = 1$ nF, and hence a drop in the available v_{DS} swing. [9].

B. Comparison of QV Patterns at 400 V and 100 kHz

Fig. 3 shows that the DUTs exhibit diverse QV patterns, even within the same semiconductor types. In the Si family, the planar-Si structure shows negligible hysteresis while the SJ counterparts exhibit significant hysteresis with E_{diss} values greater than 1 μJ. The SJ devices show a distinct knee-type behaviour in their discharging paths (indicated by a green circle), around where the region corresponding to E_{diss} is much larger, while the respective charging paths show much smoother transitions. The hysteretic area ceases around 200 V, beyond which the two paths coincide. SJ devices show much larger Q_{o} values ($\geq$ 250 nC), while other devices—with comparable or lower values of on-state resistance, $R_{\mathrm{DS(on)}}$—show much lower Q_{o} values ($\leq$ 100 nC) at 400 V.

The WBG devices SiC-1 and GaN-1 hardly show any hysteresis. The barely visible area between the charge–discharge curves of these two devices and the devices Si-1 and SiC-3, is symmetrically distributed within the whole v_{DS} range (i.e., the widening in the hysteretic area is symmetrical about $\approx V_{\mathrm{m}}/2$). An interesting observation is that the patterns of the cascode structures of the WBG devices (SiC-4 and GaN-4) deviate from their non-cascode counterparts, showing the knee-type behaviour characteristic to SJ structures. Furthermore, the

[2]More details on the Sawyer-Tower measurement technique can be found in the works by Perera et al. [9] and Zulauf et al. [2].

TABLE I
DEVICES EVALUATED IN THE STUDY

Index	Technology	Voltage (V)	Part Number	Manufacturer	Current Rating (A) @ $T_C = 25\ ^\circ$C	$R_{DS(on)}$ (mΩ) typical	Package
Si-1	Si (planar)	500	SiHG32N50D	Vishay Siliconix	30	125	TO-247
Si-2	Si-SJ	650	NTHL110N65S3F	ON Semiconductor	30	98	TO-247
Si-3	Si-SJ	650	IPW65R110CFD	Infineon	31	99	TO-247
Si-4	Si-SJ	650	STW38N65M5	STMicroelectronics	30	73	TO-247
SiC-1	SiC	700	MSC090SMA070S	Microsemi	25	90	D3PAK
SiC-2	SiC	650	SCT3080AL	ROHM Semiconductor	30	80	TO-247
SiC-3	SiC	900	C3M0065090D	Cree	36	65	TO-247
SiC-4	SiC (cascode)	650	UF3C065080K3S	UnitedSiC	31	80	TO-247
GaN-1	GaN	650	GS66508T	GaN Systems	30	50	GaN*PX*
GaN-2	GaN	600	IGOT60R070D1	Infineon	31	55	PG-DSO-20-87
GaN-3	GaN	600	PGA26E07BA	Panasonic	31	56	DFN 8X8
GaN-4	GaN (cascode)	650	TPH3212PS	Transphorm	27	72	TO-220

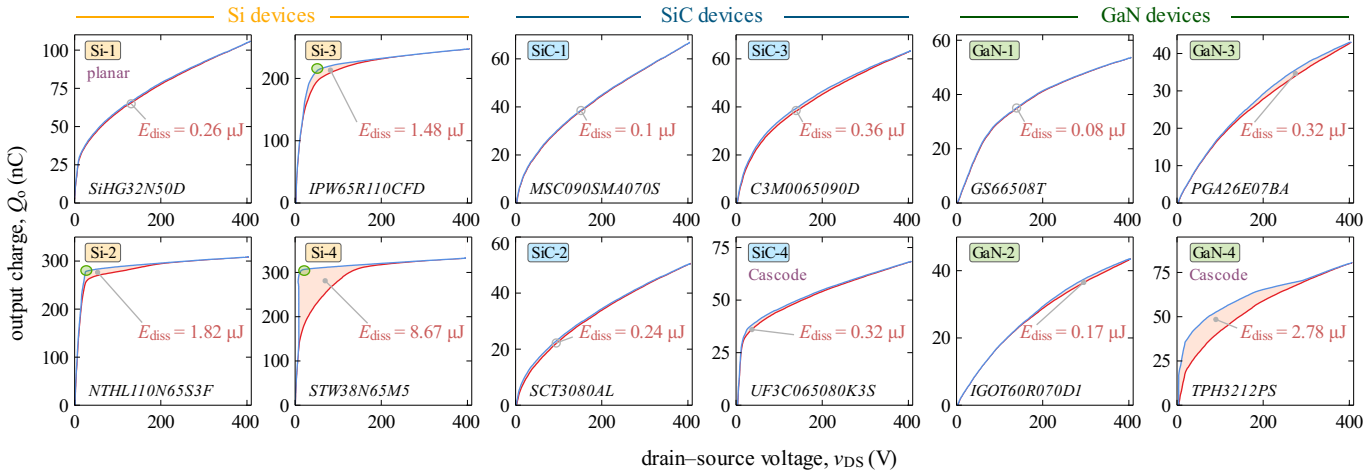

Fig. 3. Experimental QV (Q_o versus v_{DS}) curves of twelve different high-voltage transistors (current rating around 30 A): planar-Si device Si-1, Si-SJ devices Si-2 to Si-4, SiC devices SiC-1 to SiC-4 and GaN devices GaN-1 to GaN-4. The details of the devices are listed in Table I. The solid red and blue lines correspond to charging and discharging paths, respectively; the hysteresis energy loss E_{diss} is indicated by the area between the two curves (shaded in orange colour). The measurements were performed using the Sawyer-Tower technique at $V_m = 400$ V. The excitation signal is a sinusoid of $f = 100$ kHz. A C_{ref} of 1 nF was used for all the measurements, except for the Si devices 2–4, where a C_{ref} of 47 nF was used.

cascode GaN device shows significant hysteresis compared to other GaN devices.

These observations are only indicative of the soft-switching performance of these devices at $V_m = 400$ V and $f = 100$ kHz. A complete understanding requires investigation into their behaviour at different V_m and f values, which is the subject of the next two sections of this paper.

III. VOLTAGE DEPENDENCE OF QV PATTERNS

The dependence of QV patterns on voltage amplitude is investigated in this section. The aim is to identify if the hysteresis patterns emerge only within a certain voltage range, and if so, how they compare with different devices and semiconductor technologies. First, to provide a general view on the selected devices, Fig. 4 compares the variation E_{diss} with V_m for all the devices. Then, the QV patterns of each device is individually presented in Fig. 5 to explain their dependence on V_m. The excitation frequency is kept fixed at 100 kHz.

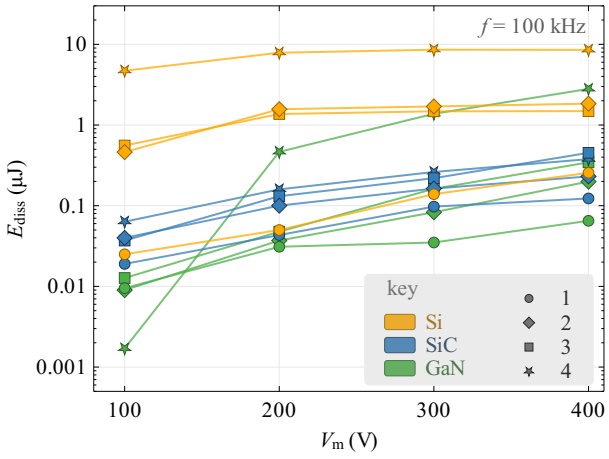

Fig. 4. Variation of E_{diss} with different V_m values for the twelve tested devices. V_m is varied between 100 and 400 V at 100 V steps. The results are obtained with the Sawyer-Tower circuit at 100 kHz.

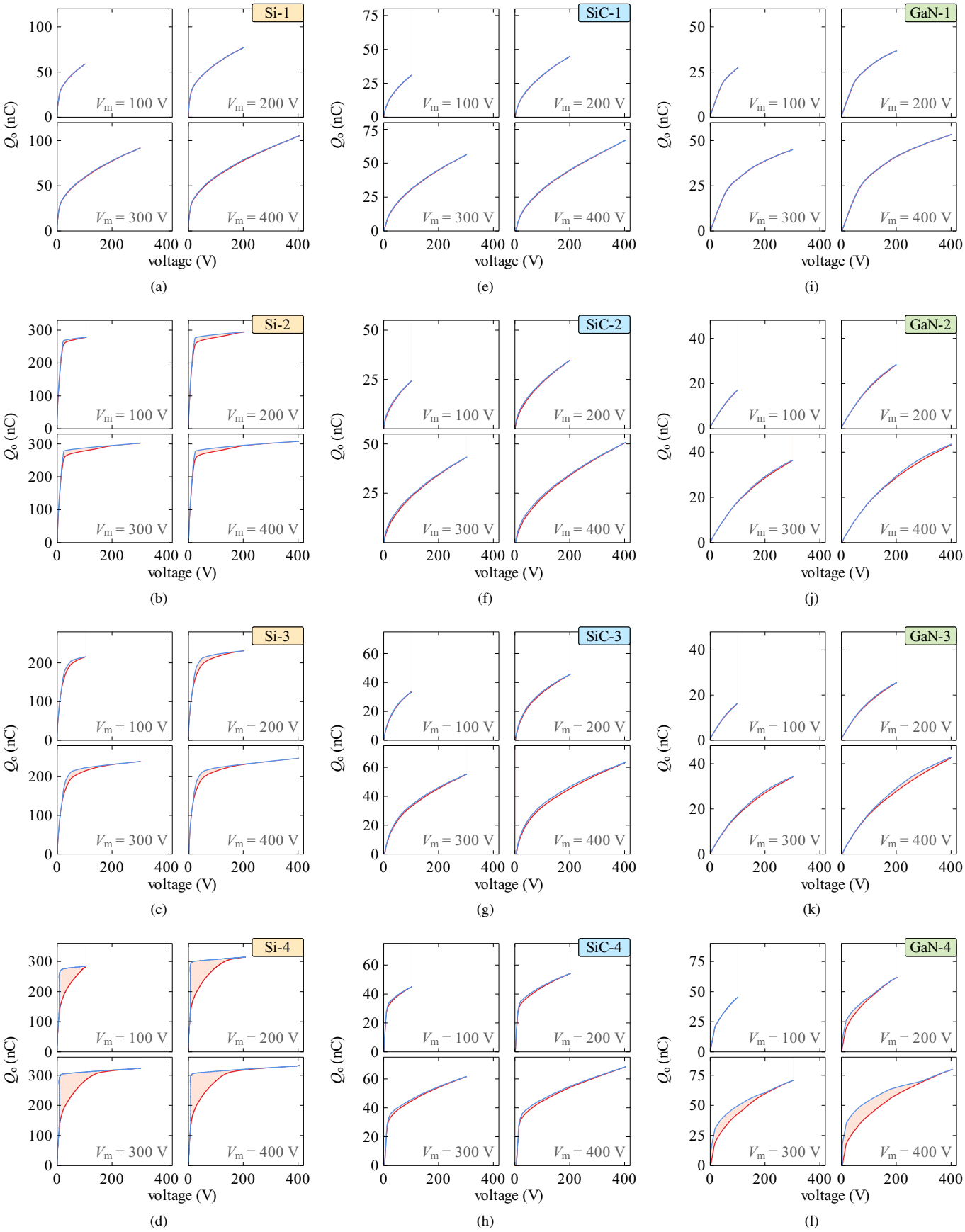

Fig. 5. Experimental results showing the variation of QV hysteresis patterns for various V_m values (at 100 kHz) for all the tested devices. The QV patterns exhibit diverse dependencies on V_m, among different devices and semiconductor technologies.

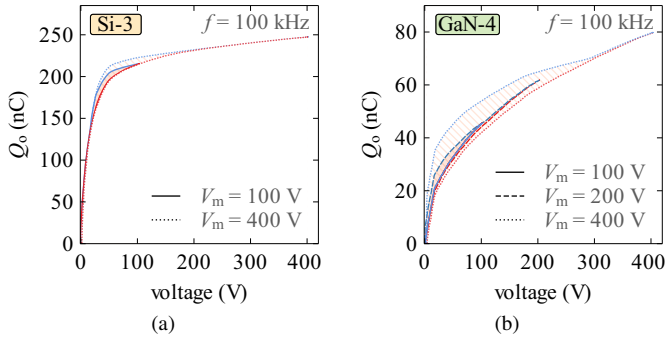

Fig. 6. Superimposition of QV hysteresis patterns of the devices (a) Si-3 and (b) GaN-4. The hysteresis pattern of device Si-3 at 400 V is a clear extension of the pattern at 100 V, with coincidental charging paths at each voltage. Device GaN-4 shows no hysteresis at 100 V; and at 200 and 400 V it shows hysteresis, but unlike device Si-3, it shows non-coincidental charging paths at each voltage.

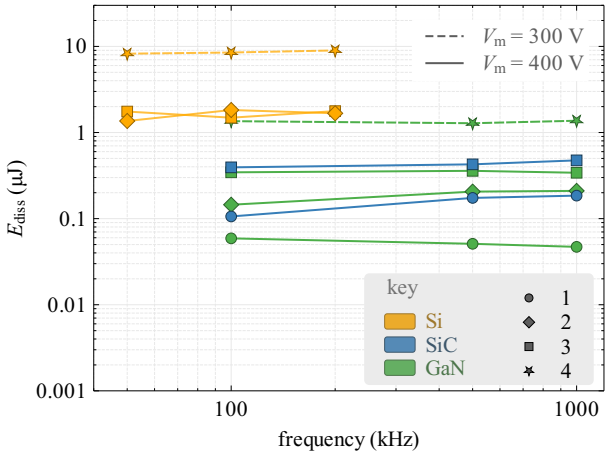

Fig. 7. Variation of E_{diss} versus f for selected devices. The results are obtained using the Sawyer-Tower circuit with a variable frequency sinusoidal excitation signal. As the Si devices have a large output capacitance value at the low v_{DS} range, they could only be tested up to 200 kHz due to increased distortion of v_{IN}, reasons of which are explained in the research article by Perera et al. [9].

A clear observation in Fig. 4 is that the Si-SJ devices show a saturation of their E_{diss} values as V_{m} passes 200 V. This can be explained by observing Figs. 5(b) to 5(d). The hysteresis patterns exist even at 100 V and continue to grow up to 200 V. However, after 200 V, the charging and discharging paths coincide resulting in no hysteretic area. This suggests that the Si-SJ hysteresis is a low-voltage phenomenon, and that operation beyond, for example 200 V in the studied cases, do not result in additional hysteresis energy losses. This could also be related to their significantly large C_{o} values (usually 10–100 nF) in the low v_{DS} range, which can be up to three orders-of-magnitude larger compared to the values at 400 V.

The devices Si-1, SiC-1 and GaN-1, as expected from their 400-V results, exhibit no appreciable hysteresis even at low voltages—see Figs. 5(a), 5(e) and 5(i). Only a barely-visible and symmetrically-spread hysteresis is present. However, Fig. 4 indicates that these devices show, although lower in value, an increasing E_{diss} with V_{m}. A possible reason for this is discussed in Section V-C.

The importance of the graphical observation of hysteresis patterns becomes apparent by looking into the GaN devices 1 to 3, which are from three different manufacturers. According to Fig. 4, the three devices (marked by circle, diamond and square symbols in green) show similar increasing-trends in their E_{diss} values with V_{m}. However, a major anomaly is observed in devices GaN-2 and GaN-3 when their QV patterns are looked into—see Figs. 5(j) and 5(k). The hysteresis area of the two devices widens in the high v_{DS} range (above 200 V), unlike in device GaN-1, which shows no such swelling. The hysteresis appears only for cases with $V_{\text{m}} \gtrsim 100$ V, and the hysteresis pattern widens with increasing V_{m}. On the other hand, there is no visible hysteresis present at voltages below 100 V for these two devices (V_{m} values of 20 and 50 V were also tested and results showed no hysteresis); in this case, they act similar to device GaN-1, but in stark contrast to SJ devices, which clearly show a low-voltage hysteresis. This suggests that for these two GaN structures, C_{o} hysteresis is a phenomenon that occurs only in the high v_{DS} range. In addition, as Fig. 4 shows, device GaN-3 exhibits much larger E_{diss} values compared to device GaN-2, which is also verified by the relatively larger hysteresis patterns of the former.

The superimposition of QV patterns corresponding to different V_{m} values on the same plot yields additional details between technology-specific differences in hysteresis losses. Fig. 6(a) shows that for device Si-3, the charge paths coincide for 100- and 400-V cases. However, for the cascode GaN device, as Fig. 6(b) shows, neither the charging nor the discharging paths show any coincidence for the considered voltages (100, 200 and 400 V), suggesting a non-uniform dependence of the QV patterns with V_{m}. The device also shows a large increase of its E_{diss} value from 100 V to 200 V in Fig. 4. This is explained by its QV hysteresis patterns that appear to take place only if V_{m} is above 100 V, as Fig. 5(l) indicates. Even above 200 V, the shapes of the hysteresis areas are quite different to other GaN devices. The shapes are more similar to that of Si-SJ devices.

IV. Frequency Dependence of QV Patterns

In this section, the frequency dependence of E_{diss} is investigated, while keeping the excitation voltage fixed. Fig. 7 plots experimental results for different device structures up to 1 MHz. None of the devices exhibit significant dependence on frequency in the considered range. This becomes also apparent by looking at the hysteresis patterns of the devices. Fig. 8(a) shows that the QV patterns are almost identical for the SJ device Si-2, when excited at three different frequencies (50, 100 and 200 kHz), explaining the non-existence of any significant frequency dependence. A similar frequency independence can be seen in the QV patterns of the WBG device GaN-1, up to 1 MHz—see Fig. 8(b). However, some works in the literature show that there is a frequency dependence for certain WBG families, whose effects become prominent only above 5-10 MHz; this aspect is discussed in Section V-B.

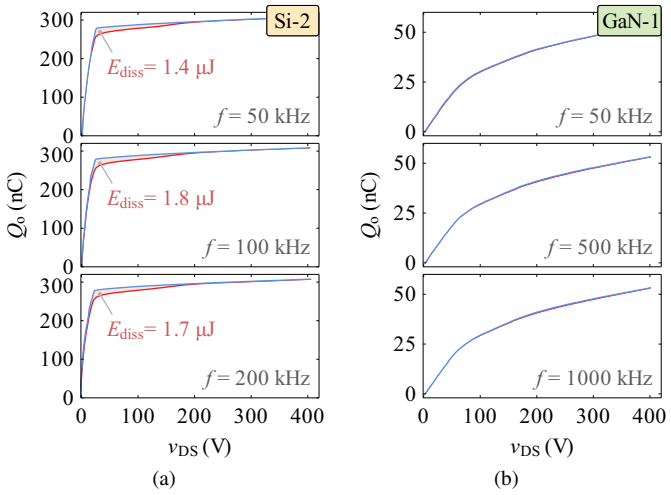

Fig. 8. (a) For different f values, similar QV hysteresis patterns are observed in device Si-2. (b) Device GaN-1 shows no hysteresis and maintains a QV pattern that is independent of f up to 1 MHz.

The impact of hysteresis energy loss is important at high frequencies, as the resulting power loss, P_{diss}, scales with f:

$$P_{\text{diss}} = f \cdot E_{\text{diss}}. \tag{3}$$

For a given P_{diss} value, the maximum operating frequency of a certain device is limited by its E_{diss} value. For instance, at 400 V and 1 MHz, device GaN-4 would result in a power loss greater than 1 W, while device GaN-1 would cause a loss much less than 0.1 W. If a device has a frequency-dependent hysteresis loss, the details of its E_{diss} as a function of f is required up to the test frequency to estimate P_{diss}. For such cases, (3) can be modified to show the frequency dependence of E_{diss} as

$$P_{\text{diss}} = f \cdot E_{\text{diss}}(f). \tag{4}$$

This shows that, if a device has an increasing E_{diss} with f, then it greatly reduces the device's usability, specially at VHF frequencies. However for the considered devices and up to 1 MHz, as Fig. 7 suggests, (3) can be utilized to obtain a good estimate of P_{diss} by using an E_{diss} value measured at a much lower frequency, such as 100 kHz.

V. Discussion

The existing knowledge on the origins of C_{o} hysteresis losses and the behaviour of these losses beyond 1 MHz are discussed in this section. Finally, a general categorization of QV hysteresis patterns are presented.

A. The Origins of Output-Capacitance Hysteresis Losses

Since the report of hysteresis losses observed in Si-SJ FETs [11], several research works have investigated and modelled the origin of these losses with a certain level of experimental validation. A first investigation was presented by Roig et al. for Si-SJ structures [12]. The authors associated the C_{o} hysteresis to trapped stranded charges (Q_{STR}), using mixed-mode simulations. They studied both multi-epitaxy multi-implant (MEMI) and trench-filled epitaxial growth (TFEG) SJ structures, and reported that the former is more prone to E_{diss} losses. The claims were further studied and confirmed by Zulauf et al. [17]. The more recent work by Lin further studied TFEG structures with numerical simulations and reported that the finite velocities of the carriers in the semiconductor are the root cause for C_{o} hysteresis in those devices [22].

Some initial studies on the origin of C_{o} hysteresis losses in GaN-on-Si HEMTs have also been reported [14], [23]. Guacci et al. investigated a 600-V device with a *p*-GaN ohmic gate (device GaN-2 studied in our work) [14]. The study proposed that the cause for the observed hysteresis loss is linked to the non-ideal insulating properties of the GaN carbon-doped buffer, which result in a parasitic resistive behaviour for the drain–substrate capacitance. Such hypothesis was confirmed by the introduction of an improved GaN buffer design, which resulted in a reduced hysteresis loss. Zhuang et al. modelled and analysed a depletion-mode (D-mode) GaN-on-Si device, and consequently, identified additional C_{o} loss mechanisms [23]: 1) resistive losses in the GaN stack; 2) resistive losses in the Si substrate, related to the doping concentration; and 3) losses in the GaN stack due to traps.

The GaN devices studied in this work, to the best of our knowledge, belong to three different device architectures: device GaN-1 is an e-mode device based on a Schottky *p*-GaN gate structure; devices GaN-2 and GaN-3 are e-mode devices featuring an ohmic *p*-GaN gate contact [24]; and GaN-4 is a cascode device. Interestingly, the QV patterns observed in Section III also show three different variations for these devices: device GaN-1 shows no hysteresis, devices GaN-2 and GaN-3 show hysteresis only above 100 V, and the cascode structure shows a significantly large hysteresis loss. These observations suggest that additional investigations from device manufactures are required, as complete knowledge on device structures are proprietary.

As for SiC devices, Bura et al. suspected that the trapping in the dielectric interface states could be the reason for related hysteresis losses [15]. The work by Zulauf et al. confirms this suspicion and states that the loss mechanism should be different to GaN-on-Si HEMTs [18]. To the best of our knowledge, a conclusive analysis on the origin of C_{o} hysteresis in SiC devices is yet to be published. The lower research interest in this could be due to the fact that SiC devices are mainly utilized in the kV range, where the converter switching frequencies are not high, and thus, the limited attention to hysteresis losses.

In summary, the C_{o} hysteresis losses in Si-SJ devices appear to be understood better in comparison to that in WBG devices. On the other hand, it could be argued that, since WBG devices are still emerging, unlike the Si technology, the original reasons of these losses could also vary, as researchers and manufacturers try new, and if not ambitious, device designs. Nevertheless, it is recommended that the manufacturers acknowledge these losses, with the basic information on quantitative values. The knowledge of these losses (with voltage and frequency) is imperative for the design of high-frequency resonant converters, from the circuit engineer's perspective.

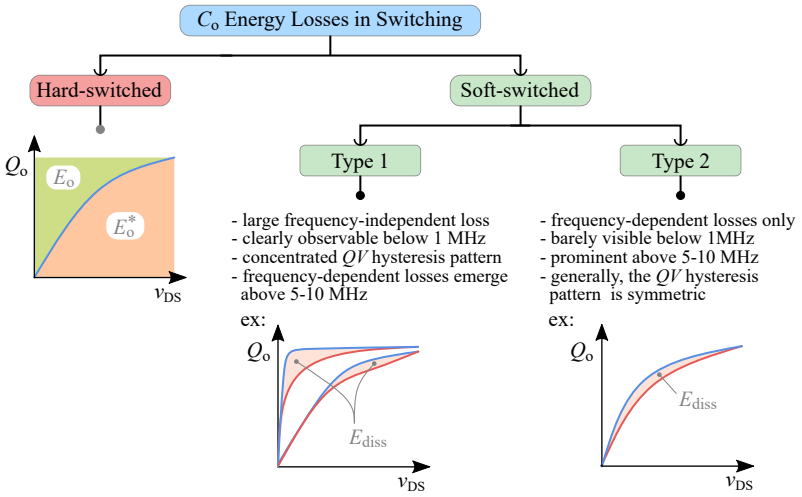

Fig. 9. Categorization of C_o-related energy losses in hard-switching and soft-switching power electronic topologies. Energy losses in a soft-switched device can be further categorized into two types based on the shape of its QV hysteresis pattern. Note: E_o^* is the co-energy component related to hard-switching circuits [10].

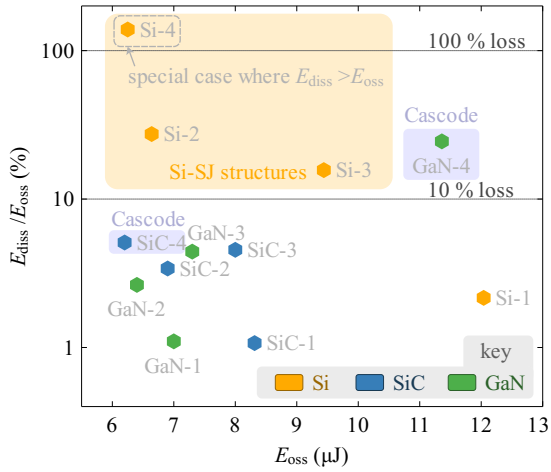

Fig. 10. E_{diss} values of the devices tested in the study plotted as a percentage loss of their E_{oss} values. The E_{diss} values are evaluated at 400 V and 100 kHz, while the E_{oss} values are estimated using datasheet-provided C_{oss} curves for 400 V.

B. Output-Capacitance Hysteresis Losses Beyond 1 MHz

Our observations in this work indicate that E_{diss} show negligible frequency dependence below 1 MHz. However, certain recent research shows that there is indeed a frequency dependence, whose effects become prominent only above 5-10 MHz [18]–[20], [25]: for example, the non-cascode GaN devices [2], [25] and certain SiC families [20], [25].

Moreover, as seen for some SiC devices in the works by Zulauf et al. [18] and Bura et al. [15], the QV patterns exhibit symmetrically distributed hysteresis patterns at high frequencies; for SiC-3 device a glimpse of this can even be seen at 100 kHz in Fig. 3. It should also be noted that the SiC devices tested in the work by Zulauf et al. did not exhibit any appreciable frequency-dependence at high frequencies (up to 35 MHz). However, for some SiC devices, frequency-dependence has been predicted at high frequencies [20], [25].

Certain Si-SJ devices have reported two hysteresis components: a low-frequency hysteresis component with negligible frequency dependence (agreeing with results in Fig. 7), and a high-frequency component with frequency-dependence [18]. The GaN cascode family (used in our study) could be expected to behave similarly; as 1) our work shows a frequency-independent, but large, hysteresis loss at low frequency for device GaN-4; and 2) the work by Zulauf et al. shows frequency-dependent hysteresis losses at high frequencies for a device from the same family.

C. Overview

The output-capacitance-related energy losses in a switching circuit can be broadly categorized into two main components as Fig. 9 shows: 1) hard-switching losses, and 2) soft-switching losses. In hard switching, the energy (E_o) stored in C_o is lost when the device is turned ON, as shown by the area shaded in green.[3]

In relation to soft-switching, two basic scenarios in C_o hysteresis losses can be identified depending on their frequency dependence: 1) a frequency-independent energy loss, i.e., a form of dc energy loss, which is significant at very low frequencies, such as 10-100 kHz; and 2) a frequency-dependent energy loss that becomes prominent above 5-10 MHz, but insignificant at low frequencies. Based on our observations and the discussion in Section V-B, commercial FETs can potentially be classified into two generic categories based on QV hysteresis patterns as shown in Fig. 9.

1) Type 1: devices that show a large frequency-independent energy loss at low frequencies and an additional frequency-dependent energy loss at high frequencies.
   ex: devices Si-2, Si-3, Si-4, GaN-4
2) Type 2: devices that show only frequency-dependent energy losses. They show very small and quite fixed hysteresis losses at frequencies below 1 MHz, but increasing losses above 5-10 MHz.
   ex: devices Si-1, SiC-1, GaN-1

Recent research has also shown that the frequency-dependent energy losses in type 2, specially for WBG devices, exhibit a nearly-quadratic variation with V_m [18], [25]. This could explain why the E_{diss} values of devices Si-1, SiC-1 and GaN-1 in Fig. 4 increased with V_m.

To provide perspective into the levels of energy that correspond to hard-switching and soft-switching loss mechanisms, Fig. 10 plots E_{diss} values (at 100 kHz) normalized by the corresponding small-signal E_o values, E_{oss} (provided in device datasheets),[4] for all the tested devices. As can be observed,

[3]There is another loss component called the *co-energy loss* in hard-switching circuits [10], which is not the focus of this work.

[4]In device datasheets, small-signal output-capacitance-related parameters are given: capacitance, C_{oss}; charge, Q_{oss}; and stored energy, E_{oss}.

E_{diss} values are generally quite small (< 10 %) in comparison to respective E_{oss} values. However, the Si-SJ structures and the GaN cascode show more than 10 % of normalised losses. The SJ device Si-4 shows an anomaly giving an E_{diss} value greater than its E_{oss} value. The devices GaN-1 and and SiC-1 offer the lowest normalised loss for E_{oss} values up to 9 μJ, suggesting the best soft-switching performance up to 1-5 MHz. Beyond this frequency range, frequency dependence of E_{diss} should be taken into account.

As a final remark, it should be mentioned that, a component sampling analysis would provide additional details about the hysteresis loss variations in different units of the same product.

VI. Conclusion

We have investigated all four prominent power FET categories (planar-Si, Si-SJ, SiC and GaN) for their output-capacitance-related QV hysteresis patterns. A categorical overview of hysteresis patterns of different device structures was presented and their frequency dependence was discussed. We have shown that different structures exhibit different dependencies on excitation voltage levels, resulting in diverse hysteresis patterns. For instance, some structures show no hysteresis below 100 V, whereas for another group, hysteresis is a high-voltage (above 150-200 V) phenomenon. These observations are essential in identifying the underlying physical phenomena in output-capacitance-related losses. The modelling of the voltage dependence of QV hysteresis patterns in *spice* simulations is essential for a more realistic analysis of switching transients and losses.

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