Hole-selective front contact stack enabling 24.1%-efficient silicon heterojunction solar cells

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***Abstract*— The window-layer stack limits the efficiency of both-side-contacted silicon heterojunction solar cells. We discuss here the combination of several modifications to this stack to improve its optoelectronic performance. These include the introduction of a nanocrystalline silicon-oxide p-type layer in lieu of the amorphous silicon p-type layer, replacing indium tin oxide with a zirconium-doped indium oxide for the front transparent electrode, capping this layer with a silicon-oxide film, and applying a post-fabrication electrical biasing treatment. The influence of each of these alterations is discussed, as well as their interactions. Combining all of them finally enables the fabrication of a highly transparent and electrically well-performing window-layer stack, leading to a screen-printed silicon heterojunction solar cell with 24.1% efficiency. Paths towards industrialization and for further improvements are finally discussed.**

***Index Terms*—anti-reflection coating, carrier-selective contact, heterojunction, nanocrystalline silicon, p-layer, passivating contact, silicon, silicon oxide, transparent conductive oxide.**

I. Introduction

Crystalline silicon is the main photovoltaic absorber material since many decades, and this domination is set to last for a few more years considering the current evolution of the market [1]. A sunlight-to-electricity conversion efficiency of 25% was demonstrated already at the turn of the century with a finely tuned homojunction architecture [2]. This value was surpassed multiple times in recent years through the advantageous use of full-area passivating contacts [3]. Amongst them, the silicon heterojunction (SHJ) architecture comprising intrinsic amorphous silicon ((i)a-Si:H) layers for passivation dominates the efficiency charts with all-back contacted devices reaching up to 26.7% efficiency [4]. This is 0.6% higher than the best device using a thin silicon oxide passivating layer combined with poly-silicon contacts [5]. However, efficiency in both-side contacted heterojunction devices hovers at 25.1% [6], [7], whereas devices using a homojunction at the front side (and a passivating contact on the rear side) recently reached up to 26.0% efficiency [8]. This difference is principally due to a lower short-circuit current density (J_{SC}) for the SHJ cell, notably due to parasitic absorption of short-wavelength light in the window-layer stack (i.e. layers deposited on the light-incoming side of the wafer) when employing a full-area passivating-contact design [9]. A highest efficiency of 25.1% was interestingly obtained with either a hole-selective [6] or electron-selective [7] contact placed on the light-incoming side.

There are several opto-electrical trade-offs at stake in this window-layer stack: it should be highly transparent and minimize reflection over the spectrum of absorption of Si, yet ensure excellent surface passivation and minimal-resistance charge collection to the metallic grid. (Achieving these two last properties naturally results in near-perfect charge selectivity [10].) These trade-offs typically call for opposite properties. For example, surface passivation requires the use of an (i)a-Si:H layer of at least a few nanometers, which is detrimental both in terms of electrical resistance and parasitic absorption. Then, the carrier density in the transparent

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conductive oxide (TCO) should be high to minimize electrical resistance, yet low to minimize parasitic infrared-light absorption. The same goes for the thickness of the doped a-Si:H layer [9]. In all cases, it is possible to tune specific properties of the involved material to relax the trade-off. This can be the microstructure factor for the (i)a-Si:H layer [11]–[13], the electron mobility for the TCO [14]–[16], or the composition of the thin-film-silicon doped layer [17]–[19].

Using such approach systematically, we applied three alterations to our standard window-layer stack, which enabled to reach a certified solar cell efficiency over 24% starting from a 23.2%-efficient device [20]. These are sketched in Figure 1, and consist of 1) replacing the a-Si:H p-type layer by a nanocrystalline-silicon-oxide (nc-SiO_x:H) layer, 2) replacing the indium tin oxide (ITO) with zirconium-doped indium oxide (IZrO) for the front TCO, and 3) applying a hydrogenating silicon-oxide (SiO_x:H) second anti-reflection coating layer. A final post-fabrication step is to subject the device to an electrical-bias post-treatment. We focus on front-junction configuration which is less documented than the rear-junction one (in particular when involving nc-SiO_x:H layers [21], [22]), to investigate whether high efficiencies can be reached with such films.

Alloying nc-Si:H with oxygen was established as an efficient strategy to obtain a more performant front contact layer in thin-film silicon devices [22]–[26]. A similar approach was then applied to SHJ solar cells, with a clear optical benefit but electrical losses [27]. Concerning the front TCO film, the use of IZrO was shown to enable highly efficient SHJ solar cells [28]. This stems from the high electron mobility reached in this material, similarly to other In-based TCOs [16], [29]–[31], which enables to achieve sufficient conductivity with a free-carrier density below 4×10^{20} cm^{-3}. This ensures simultaneously low resistive losses and low parasitic free-carrier absorption for the solar cell [32]. Another approach to minimize resistive and optical losses in the front TCO layer is to coat it with a SiO_x:H film: such additional coating was shown to both improve the transmittance of light to the silicon wafer and reduce the sheet resistance of the TCO [33], [34]. A similar approach can be economically relevant for high-volume manufacturing [35], and increase the reliability of SHJ solar cells when combined to a tungsten-doped indium-oxide film [13]. The last building block used in the reported results is the application of a forward electrical bias to the finished solar cell. This step was shown to increase the performance of SHJ devices—similarly to the exposure to illumination at open-circuit conditions—due to a passivation improvement stemming from the recombination of charges injected in the silicon wafer [36]. This effect is thus expected to occur in the first few weeks of module operation [37].

All the four elements used in our approach have therefore already been individually implemented but not yet combined in a unique high-efficiency device. Such combination is not straightforward as all layers involved in a SHJ contact stack interact, either by altering the growth of the subsequent layer or by modifying the physical or chemical properties of the underlying ones: This typically prevents the direct growth of doped nc-Si(O_x):H films directly on the passivating (i)a-Si:H layer, requiring the use of intermediate processes to promote nucleation [38], [39]. Similarly, the growth of TCO films is influenced by the nature of the doped silicon layer it grows on, with lower-conductivity films typically obtained on nc-Si:H films than on a-Si:H films for identical growth conditions as exemplified in Figure 1c [20], [40]. Then, although the addition of an SiO_x (or SiN_x) capping layer has been demonstrated as beneficial for multiple TCOs (ITO [33], tungsten-doped indium oxide [13], aluminum-doped zinc oxide [41]), this is still unexplored for IZrO, even less so for an IZrO layer grown on a nc-SiO_x:H film. Lastly, little literature is available on the influence of the device architecture on the effect of a forward bias treatment. Notably, the beneficial effects on the silicon passivation of applying a light soaking treatment (supposedly identical to a forward bias) rely on the presence of the doped layers: samples passivated with a simple (i)a-Si:H film were shown to degrade upon such treatment [36], [42]. In particular, the p-type layer thickness was shown critical for front-junction solar cells, with forward bias yielding improvements even in conditions for which the light soaking led to degradation [43]; the effect of such treatment on devices using (p)nc-SiO_x:H layers has so far not yet been experimentally tested.

II. Experimental Details

Figure 1 shows the schematics of the devices discussed here. These are front-junction silicon heterojunction solar cells processed as follows on 100-mm-diameter, n-type, float-zone silicon wafers with a resistivity of 1.7-2.3 Ω·cm, and a thickness of 195 µm. After the formation of random pyramidal texturing and cleaning using standard chemical baths, the wafers were subjected to a one-minute dip in hydrofluoric acid (HF) followed by loading in a plasma-enhanced-chemical-vapor-deposition (PECVD) reactor to deposit the thin-film silicon layers. A 9-nm-thick (as measured on the flat witness glass) (i)a-Si:H film was then grown on the rear side, followed

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by a phosphorus-doped n-type film with a thickness of 30 nm on glass. After flipping the wafer in air, the same (i)a-Si:H film was grown on the other side, followed by the p-type layer. Reference samples were prepared with a (p)a-Si:H film, yet most devices discussed here include a nanocrystalline-silicon (nc-Si:H) or nanocrystalline-silicon-oxide (nc-SiO_x:H) film. In the case of nc-Si:H or nc-SiO_x:H films, an oxidizing plasma treatment was performed on top of the (i)a-Si:H layer, enabling incubation-free nucleation of the nanocrystallites [39], and the reactor temperature was set to 175 °C (in lieu of the 200 °C used for all other PECVD layers) as this was shown to promote higher-crystallinity layers [44]. A transparent conductive oxide (TCO) was then deposited by reactive sputtering on the front-side using a shadow mask to define five 2 × 2 cm^2 cells per wafer. This front TCO consisted of either ITO deposited using 1000 W direct-current (DC) excitation power or IZrO deposited using 600 W radio-frequency (RF) excitation power, from 378 x 120 mm^2 targets. The scanning speed was adjusted to reach a thickness (on the textured wafer) of either 75 nm or 50 nm, to achieve optimal conditions for single-layer or double-layer anti-reflection coating [41]. On the rear side, a 150-nm-thick ITO film was deposited prior to the silver layer (full area in both cases) to mitigate parasitic absorption [45]. A silver front grid (external busbars, 1.85-mm finger pitch, 40-µm finger width, total shading estimated to 2.3%) was screen-printed on the front side, which was cured at 210 °C for 30 minutes in a belt furnace. This annealing step also cures sputtering-induced damage and improves the conductivity of the TCO film [46]. When applied, a ~100-nm-thick SiO_x film with a refractive index of 1.5 at 600 nm was deposited on top of the TCO film by PECVD at 180 °C. Finally, some devices were subjected to a forward electric bias with a current density of 40 mA/cm^2 for two weeks in the dark, mimicking beneficial light soaking as described in [43].

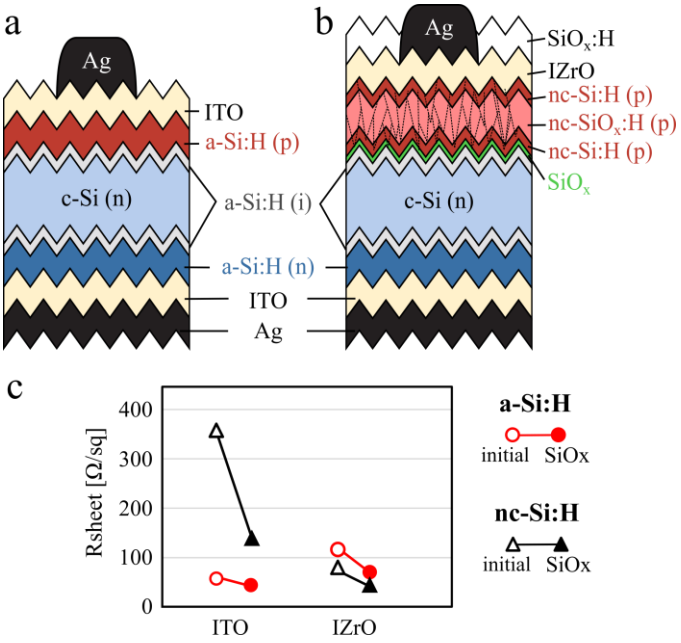

Fig. 1. a,b) Sketch of the standard device (a) and of the improved device (b). c) Sheet resistance of the front TCO measured on a pad directly on the wafer before or after deposition of a SiOx capping layer for a-Si:H or nc-Si:H (p) layers and ITO or IZrO as transparent electrode.

III. Results and Discussion

Figure 2 shows current-voltage (IV) metrics for eight different solar cell structures, consisting of a variation of the hole contact (a-Si:H or nc-Si:H), the TCO layer (ITO or IZrO) and the capping layer (nothing or SiO_x). The addition of the SiO_x capping layer brings a systematic improvement to all devices, irrespective of the nature of their p-type and TCO layers. In the case of the IZrO film, the slight gain originates only from J_{SC} increase due to the lower reflection, without any significant change of open-circuit voltage (V_{OC}) or fill factor (FF). Conversely, both J_{SC} and FF are improved upon SiO_x deposition for the cells using an ITO contact. This FF gain originates from series-resistance reduction, since this layer was relatively resistive prior to the SiO_x deposition as it was grown under conditions optimized for the post-SiO_x state [33]. The ITO film was also slightly thinner than the IZrO one, thus inducing more reflection prior to SiO_x deposition [41].

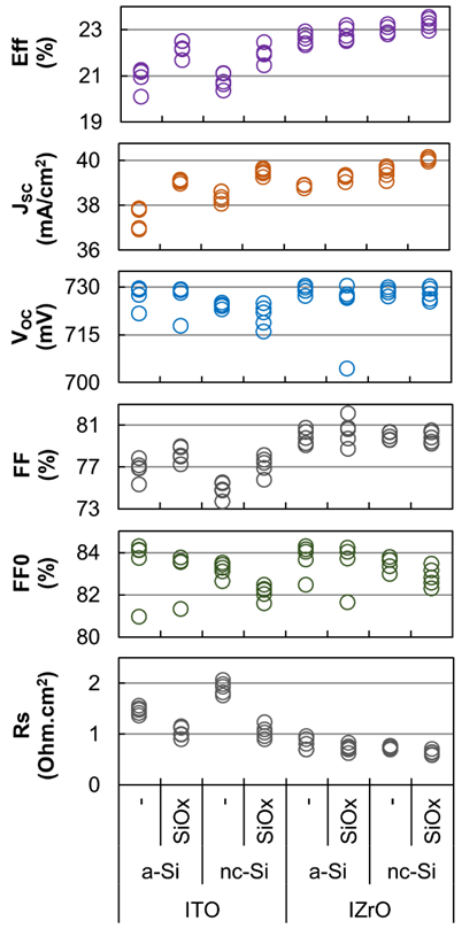

Fig. 2. Solar cell characteristics for devices incorporating either an a-Si:H or a nc-Si:H (p) layer, and an ITO or IZrO front TCO, prior to or after the deposition of the SiO_x:H capping layer.

Then, comparing the performance of solar-cells using either ITO or IZrO, similar V_{OC} are obtained but the use of IZrO enables slightly higher J_{SC} and largely improved FF. The latter partly originates from slightly better passivations (higher FF_0) presumably originating from the 20% lower power used for IZrO sputtering compared to ITO, yet most of the gain comes from reduced series resistance. This stems from improved charge transport on the hole-collecting side due to the use of IZrO thanks to the lower sheet resistance of the IZrO than ITO, even after the SiO_x deposition. Note that although a similar sheet resistance is reachable by decreasing the oxygen content during ITO sputtering in our tool, this comes at the expense of lower transparency, detrimental to Jsc as was previously reported [28]. The higher mobility of IZrO (~60 cm^2/Vs in this experiment compared to ~30 cm^2/Vs for ITO) enables to reach simultaneously high transparency and conductivity [32]. Finally, the use of the (p)nc-Si:H instead of (p)a-Si:H enables higher J_{SC} without affecting the Voc and FF, leading to the highest overall efficiency for the combination of (p)nc-Si:H with IZrO and SiO_x capping layer. A lower Voc is observed when combining (p)nc-Si:H and ITO, which is attributed to poorer passivation for this particular wafer, presumably unrelatedly to the contact choice.

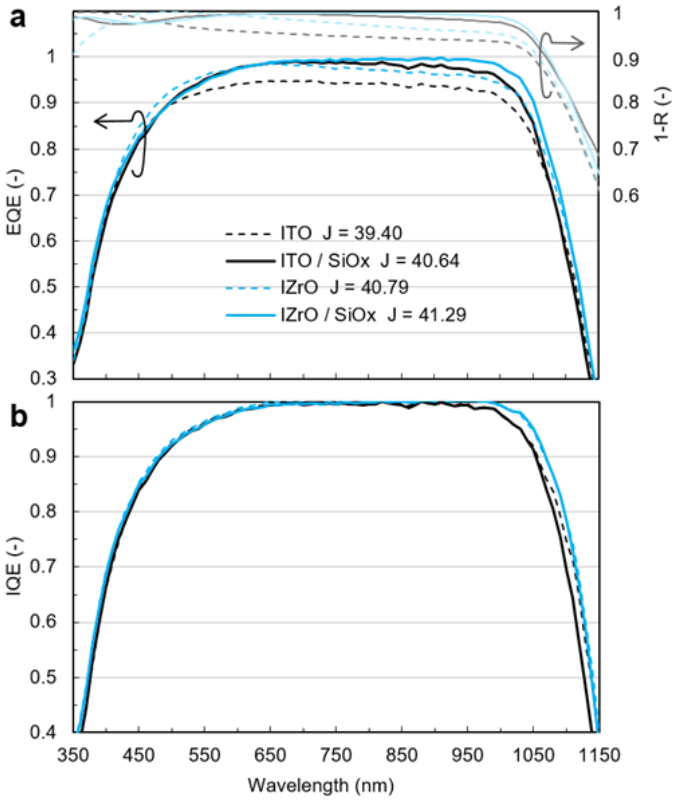

Fig. 3. a) External quantum efficiency (EQE) and one minus reflectance (1-R) for solar cells employing ITO or IZrO front electrodes, uncapped or capped with SiOx. b) Internal quantum efficiency (IQE) of the same samples.

Figure 3a shows external quantum efficiency (EQE) and total absorptance calculated as one minus the reflectance (1-R) both probed on a non-metallized area, for samples using the (p)nc-Si:H layer. ITO and IZrO are compared, and data is shown for both prior to and after the SiOx deposition. Reflection is greatly reduced when adding the SiOx layer in both cases. A larger gain is seen for the ITO film which was slightly thinner, yet after SiOx deposition the IZrO layer yields the lowest total reflectance overall after SiOx deposition thanks to lightly better performance in the near-infrared range. This is ascribed to the higher refractive index (*n*) in the infra-red compared to ITO, due to the lower influence of free carriers on *n*. Figure 3b shows internal quantum efficiency (IQE) for all four conditions. The use of IZrO enables a slight gain in the UV part of the spectrum, and a more substantial one in the infra-red part. The former originates from the

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slightly wider bandgap, whereas the latter is due to lower free-carrier absorption. In this spectral range, the addition of SiO_x on ITO leads to a decrease of IQE accompanying the sheet-resistance drop shown in Figure 1c. Conversely, IQE of the IZrO sample remains remarkably high in spite of the low sheet resistance achieved, thanks to the high electron mobility in this material. IQE of the sample using an SiOx-capped IZrO electrode stays thus above 99% in the 640–1000 nm range.

Figure 4 describes the effect on devices of introducing CO_2 in the gas mix during the (p)nc-Si:H layer growth to push further its transparency by alloying it with oxygen. To investigate an eventual detrimental alteration of the (p)nc-Si:H-layer nucleation or of its interface with the TCO film, either the first or the last minute of the 5.5-minute deposition was performed without CO_2 as also performed in reference [47]. A reference device without CO_2 all along the growth was also produced, as well as a sample without CO_2 during both the first and last minute. As shown in Figure 4a, similar efficiency can be obtained with a (p)nc-SiO_x:H layer as with a (p)nc-Si:H layer providing that both interfaces are kept CO_2-free. V_{OC} is slightly improved when incorporating CO_2 in any part of the film, possibly owing to the increase of the layer resistance or to its wider bandgap [10], [21], [25], [48]. A J_{SC} increase is obtained when adding CO_2, even when only in the bulk part of the layer, at the cost of a FF drop discussed below.

Figure 4b pictures the changes in thermal activation of charge transport when using the different versions of (p)nc-SiO_x:H layers discussed here. Upon heating an ideal solar cell, FF is decreasing, due to the temperature-induced V_{OC} decrease; For silicon heterojunction solar cells, this trend is modified at low temperatures, and FF actually decreases upon cooling below a certain temperature due to thermally-activated transport for hole collection [49]. As can be seen in Figure 4b, this phenomenon is present in all studied devices, and a FF maximum is indeed observed for all device incorporating CO_2. For the no-CO_2 reference, it occurs at a slightly lower temperature than 15 °C, indicating that minimal series resistance is originating from the TCO-Si contact resistance.

Introducing CO_2 in any part of the (p)nc-Si:H layer reduces the maximum FF value and pushes it to higher temperatures. For devices incorporating (p)nc-SiO_x:H films, the temperature at which FF peaks is highest for the layer with CO_2 at the (p)nc-SiO_x:H / TCO interface, and minimal for the layer without CO_2 at both interfaces. For that specific device, FF is only moderately deviating from the theoretical linear trend for 25 °C (which corresponds to standard test conditions, STC).

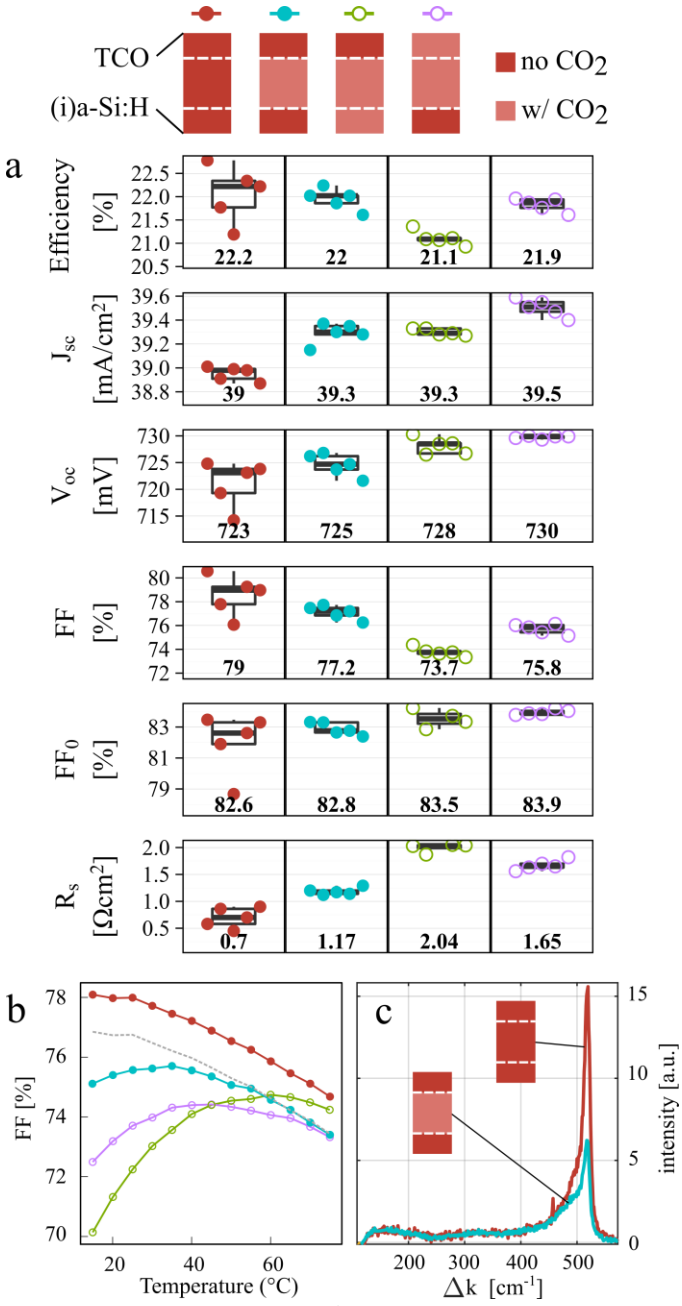

Fig. 4. a) Solar cell characteristics for devices incorporating a (p)nc-Si:H layer or a three-layer stack composed of either (p)nc-Si:H or (p)nc-SiO_x:H for the bottom, middle and top parts as sketched on top of the figure. b) temperature-dependent FF for the same devices as described in a). The dashed gray line corresponds to the no-CO2 curve shifted down by ~1.3%. c) Raman crystallinity of the non-oxyde (p)nc-Si:H layer and of the (p)nc-SiO_x:H stack with both the bottom and top sub-layers grown without CO_2.

Besides, a significant part of the 2.8% FF drop observed at STC compared to the device using a (p)nc-Si:H is also present at 70 °C in the linear part of the curve as evidenced by the dashed gray line corresponding to the FF of the (p)nc-Si:H

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device shifted down by ~1.3%. This indicates that part of the 2.8% FF drop is actually not caused by a thermally activated barrier but by a temperature-independent contribution (e.g. grid resistance or TCO sheet resistance variability), and might therefore not be linked to the use of a (p)nc-SiO_x:H film as will be confirmed later.

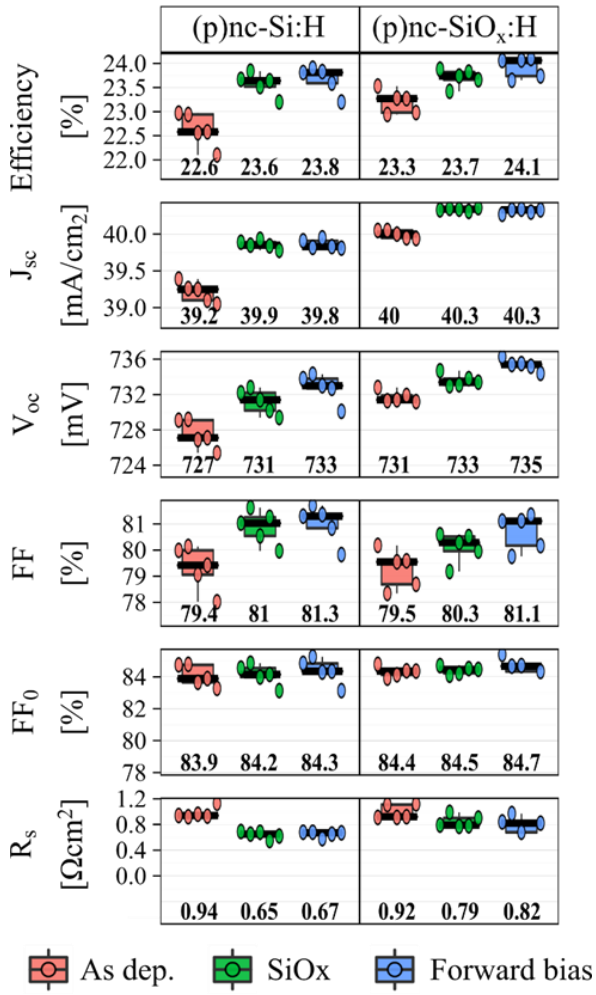

Fig. 5. Solar cell characteristics for devices incorporating a (p)nc-Si:H or three-layer stack with (p)nc-SiO_x :H in between two non-oxyde layers. The as-deposited state is reported, as well as the ones after the SiO_x coating on top of the IZrO and after the forward electrical bias.

Figure 4c shows Raman spectra of the nc-SiO_x:H with both interfaces grown without CO_2, acquired with a 325-nm laser on a complete solar cell device in an area non-coated by the TCO. The strong signal between 510 cm^{-1} and 520 cm^{-1} shifts confirms the nanocrystalline nature of this film. The relative magnitude of this peak compared to the one from the amorphous phase at 480 cm^{-1} is lower than for the nc-Si:H film (also shown in Figure 4c). Note that such lower crystallinity is common for oxide alloys and is not necessarily detrimental to solar cell performance [24].

Figure 5 eventually shows the influence of applying a forward-bias treatment on solar cells incorporating all aforementioned developments. Devices with a (p)nc-Si:H and a (p)nc-SiO_x:H film (the latter having both interfaces grown CO_2-free are compared, and each solar cell was measured firstly after screen-printing, then after the SiO_x deposition, and finally after a 3-week forward-bias treatment. As can be seen, both processes lead to efficiency improvements. The SiO_x deposition improves mostly J_{SC} as previously observed, as well as FF through series-resistance reduction. An unexpected but systematic V_{OC} increase of a few mV is also observed, which could be due to further curing of the sputtering damage, modification of the work-function of the IZrO layer following hydrogenation, or interaction of hydrogen with the passivating (i)a-Si:H layer. Conversely, the forward bias treatment improves mostly FF through FF_0 as well as V_{OC}, thus passivation, without altering J_{SC}. As in the previous section, the series resistance is higher when using a (p)nc-SiO_x:H compared to a (p)nc-Si:H film, leading to a slightly lower FF. There is, however, a smaller difference than in the previous experiment, suggesting that the non-thermally activated difference previously observed is indeed unrelated to the use of the (p)nc-SiO_x:H film. Overall, combining the (p)nc-SiO_x:H hole contact with tailored interfaces, the IZrO layer, the SiO_x coating, and the forward bias treatment enables a remarkable 24.1% efficiency. The best cell of this series was independently certified with the same efficiency value, as shown in Figure 6.

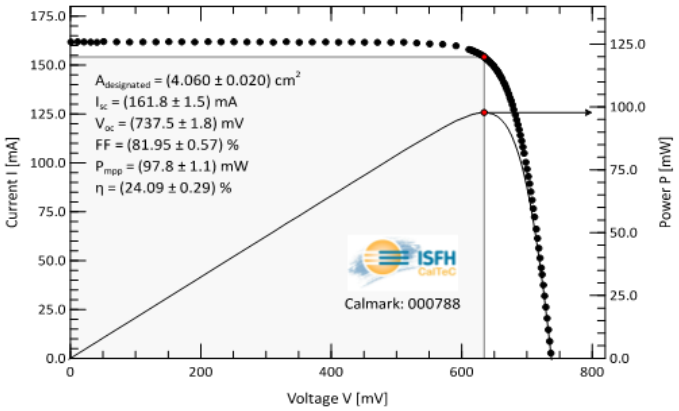

Fig. 6. Certified current-voltage characteristic of a silicon heterojunction solar cell incorporating the developments discussed above.

IV. Outlook

In a further batch of experiments, thinning down the (i)a-Si:H film as well as the oxide part of the (p)nc-SiO_x:H film (from three minutes and a half of deposition to two minutes) was shown beneficial. Indeed, similar electrical performances were maintained, with less than a millivolt of V_{OC} drop and a

$0.1\%_{abs}$ FF improvement(pseudo-FF dropped by half a percent, which was compensated by a series resistance reduction of 0.1 Ω.cm^2). On the other hand, these two thickness reductions decreased parasitic blue-light absorption, as shown in Figure 7, amounting to 0.25 mA/cm^2 J_{SC} gain each. This total J_{SC} increase of 0.5 mA/cm^2 thus enabled a slight efficiency gain compared to the reference sample processed identically to the 24.1% certified device. Going beyond the window-layer, a similar 0.6 mA/cm^2 J_{SC} gain on the infrared part of the spectrum is demonstrated in Figure 7, through the replacement of the thick ITO film by the combination a thin ITO layer with a partial MgF_2 coating prior to the full-area silver layer [50]. The insertion of this low-refractive-index layer reduces plasmonic absorption in the rear silver metallization. However, low V_{OC} and FF were measured for this device, presumably due to improper processing order of this advanced rear reflector. Yet, combining the two approaches gives a path towards further improvements to approach 25% efficiency for silicon heterojunction solar cells in the front-junction configuration using screen-printed contacts. Going further would likely require more advanced metallization such as copper plating or using photolithography, and the production of a higher volume of samples to acquire sufficient statistics for fine-tuning of each layer properties.

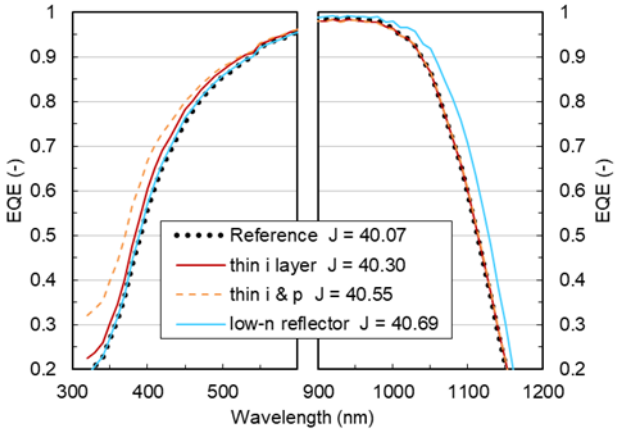

Fig. 7. EQE of solar cells with variations in the front-contact stack or rear reflector focusing on the short- and long-wavelength ranges.

Finally, although all the processes employed here rely on industry-relevant processes, several aspects would need attention towards their implementation in production environment. Firstly, concerning IZrO sputtering, an industrial tool with a 378 x 120 mm^2 linear target was used in this experiment. A slower scanning speed was used compared to our ITO standard recipe, and radio-frequency (RF) excitation was used in lieu direct-current (DC). Investigating the possibility to deposit with a higher throughput with DC excitation—which was not tested here—would therefore be required. Secondly, part of the optical benefits of the SiO_x capping would be lost in an encapsulated module: the surrounding medium of the TCO on the light-incoming side has in that case a refractive index close to 1.5. A similar strategy was however shown industry-relevant by using an SiN_x layer, which is less costly than the ITO layer and yield a 0.2% efficiency increase in industrial laboratory from optical benefit [35]. The electrical gains might be maintained in that case (although no FF improvement is reported in [35] using ITO and industry-optimized a-Si:H layers), and excellent anti-reflective performances could be reached by capping a relatively thin < 50-nm-thick IZrO film with an oxynitride layer (SiN_xO_y) which can provide a transparent layer with an optimal refractive index of 1.7. Then, the (p)nc-SiO_x:H layer used in this study required four minutes of deposition, which is incompatible with cost-effective industrial throughput. Decreasing the deposition time—which again was not tackled in this study—would thus also be required. Finally, although minimal degradation was measured after a few weeks for unencapsulated devices presented here, more attention should be paid to the reliability of modules employing such layers.

V. Conclusion

We applied multiple alterations to the window-layer stack of front-junction silicon heterojunction solar cells to improve their performance. By combining a p-type mixed-phase nanocrystalline silicon oxide hole-collecting layer, a zirconium-doped indium oxide capped with silicon-oxide as an antireflective transparent conductive stack, and a forward bias treatment, we fabricated a silicon heterojunction solar cell with an independently confirmed 24.1% efficiency. The high transparency and conductivity of this stack enable simultaneous reaching of a current density close to 40 mA/cm^2 together with a FF close to 82% while using a single screen-printing metallization step. We could evidence that improvements could be combined together without detrimental interaction. We notably observed a beneficial reduction in series resistance when depositing an SiO_x layer on an IZrO film, and demonstrated that a forward electrical bias can boost performance of finished devices incorporating a (p)nc-SiO_x:H layer. Paths towards further improvements are discussed, notably through fine-tuning of the (i)a-Si:H and (p)nc-SiO_x:H layers for further opto-electrical gains, or alteration of the rear electrode to reduce infrared-light parasitic absorption. The combination of both already evidenced a potential for over 1 mA/cm^2 of J_{SC} improvement.

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