Small-Signal Approach for Precise Evaluation of Gate Losses in Soft-Switched Wide-Band-Gap Transistors

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***Abstract*—High-frequency switching is favorable for fast transient response, small size of passive components and superior power density, especially in soft-switching topologies. At high frequencies, power dissipation due to consecutive charging/discharging of gate capacitance is considerably large. As presented in this work, the *actual* gate charge (Q_G) of a transistor can be very different from the *typical* values reported in manufacturer datasheet, which leads to errors in estimation and modeling of gate loss based on datasheets. Furthermore, the reported Q_G values in datasheets correspond to a hard-switching test condition, and are not a good representative of the losses in soft-switched transistors. Here, we propose a simple method to precisely evaluate gate loss in soft-switched transistors for high-frequency applications. A small-signal input-capacitance measurement is used to derive gate loss in two commercial Gallium-Nitride (GaN) transistors. The estimated losses are then verified by results from accurate thermal modeling based on a matrix of temperatures, when the transistors are driven up to 30 MHz. The results are of great significance to the modeling and accurate measurement of gate losses at high frequencies. It is instrumental to a proper cooling design to avoid device and gate driver thermal runaway and failure. Also, the more accurate gate capacitance measurement enables an accurate dead time adjustment to achieve synchronized turn ON between various transistors in soft-switching topologies.**

***Keywords*—GaN, SiC, gate charge, gate capacitance, gate loss, small-signal measurement, high-frequency circuits, soft switching, thermal measurements, variance in gate charge, hard gating**

I. Introduction

Small gate capacitance (C_{GS}) in wide-band-gap (WBG) transistors enables high-frequency switching with low dissipated energy in charging/discharging of C_{GS}. High-density dc-dc conversion [1]–[7], wire-less power transfer (WPT) and radio-frequency (RF) amplification [8]–[10] operate transistors at very high frequencies in which gate loss (P_G) cannot be neglected and its accurate evaluation becomes crucial for cooling and gate-driver design. Gate loss is among the major sources of losses in high-frequency soft-switched resonant topologies, together with conduction and output capacitance losses [1], [11]–[13]. One can employ a resonant gate driver to recover a part of energy stored in transistor input capacitance (C_{ISS}) using inductors and clamping circuits [3], [4], [14], [15]. Such solutions result in larger driver size, limitations in timing and duty cycle and extra inductor losses. Furthermore, as Fig. 1 shows, C_{ISS} values in Silicon Carbide (SiC) and Gallium Nitride (GaN) devices are highly nonlinear with gate-source voltage (V_{GS}) (unlike Silicon), which makes resonator tuning very challenging for a given frequency. Hence, push-pull gate drivers (hard gating) could still be preferable for many applications based on WBG technology.

The reported gate-charge (Q_G) values in datasheets are measured as the devices are subjected to a hard turn ON, and therefore are not good representatives for a soft-switching operation [11], [16], [17]. Furthermore, reported Q_G refers to a *typical* value, and the *actual* values can vary largely within transistors with a same part number. Fig. 2a presents the measured input capacitance for a sample of twenty GaN transistors with the same part number (GS66508T), when drain was shorted to source and a small-signal voltage at 1-MHz was applied to the gate and source terminal. By extracting the equivalent Q_G for 5-V and 6-V gate-drive voltages, Fig. 2b reveals a variation higher than ±20% in gate charge over the 99% (±3σ) of the samples.

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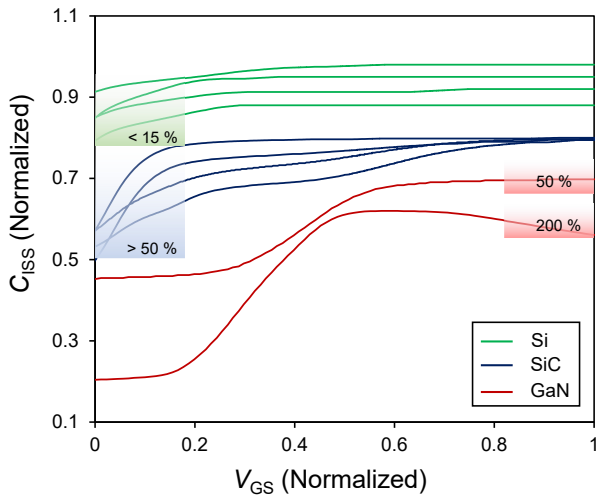

Fig. 1 Normalized C_{ISS} comparison for three semiconductor technologies. Large variation of C_{ISS} with V_{GS} in WBG transistors poses a challenge to resonant gate-drive design at high frequencies. In case of hard gating, Q_G at maximum charging voltage is totally dissipated in gate-drive path.

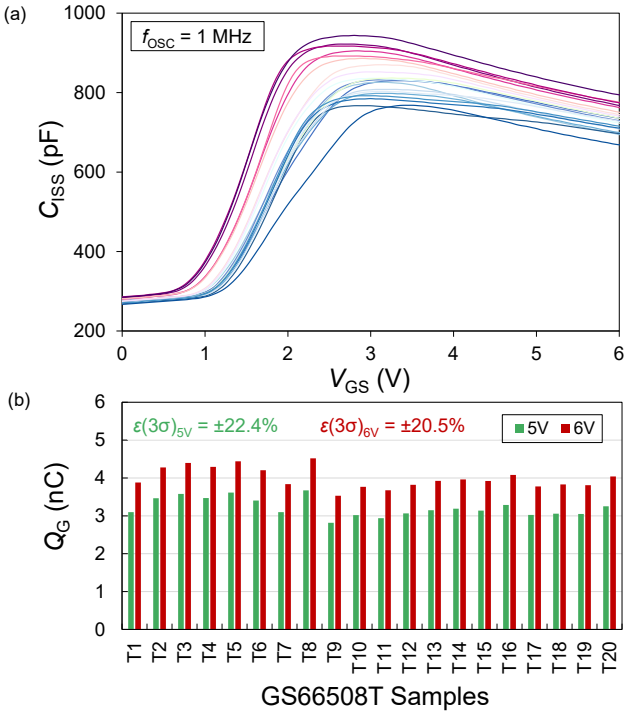

Fig. 2 (a) Variation in C_{ISS} versus V_{GS} in a sample of twenty GS66508T GaN transistors. A variation of more than 20% necessitates a precise measurement method for accurate estimation of gate losses, especially at high frequencies, when the gate losses in WBG devices become considerably large. (b) statistical parameters for the sample, reporting the soft-switching Q_G for a 5-V and a 6-V drive condition. The measurements were performed using a Keysight E4990A impedance analyzer and a 16047E 120-MHz test fixture, when the drain of transistors were shorted to the source.

Thus, a straightforward method for evaluation of individual devices is extremely useful. Here, we propose a simple and accurate method based on small-signal C_{ISS} measurement to evaluate gate loss in soft-switched transistors. The method is then applied to two commercial GaN transistors from two different manufacturers and the evaluated P_G values are verified by results from an accurate thermal modeling based on matrix of temperatures, where the transistors are operated up to 30 MHz at no-load condition, enabling the separation of gate loss from other sources of power dissipation (i.e. conduction loss and output capacitance loss.)

Other than offering accurate P_G evaluations, the extracted C_{ISS} enables more accurate dead time adjustments unique to each transistor in the converter for synchronized turn ON in soft-switching topologies.

Here, the presented thermal modeling not only enables verification of overall P_G for soft-switched transistors based on their small-signal C_{ISS}, but also shows the distribution of temperature over different elements in the gate drive circuit.

Due to several limitations, direct electrical measurements (especially for the gate current) are not feasible [18], [19]; however, one can alternatively measure dc power fed to the gate driver to extract overall P_G.

II. Methodology

By modeling the gate-drive circuit with C_{ISS} of a field-effect transistor (FET) in series with the resistance of the FET and gate driver, gate loss when the voltage varies between V_{OFF} and V_{ON} with a frequency of f_{SW} is

$$P_G = Q_G (V_{ON} - V_{OFF}) f_{SW} \quad (1)$$

where Q_G can be defined as

$$Q_G = \int_{V_{OFF}}^{V_{ON}} C_{ISS}(v)\,dv \quad (2).$$

The reported Q_G in datasheet is measured for a fixed test-current (I_G) forced into the gate of the transistor, as it is submitted to a hard turn ON [16]. To extract soft-switching Q_G for a FET, we propose using impedance analyzer to extract the

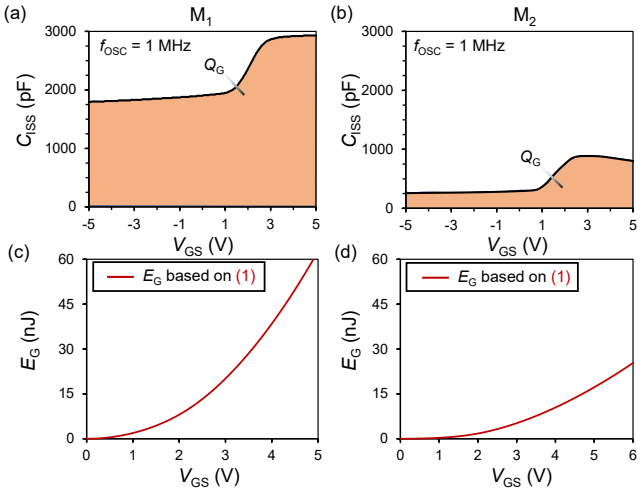

Fig. 3 Small-signal C_{ISS} measurement versus V_{GS} for (a) M_1 and (b) M_2 transistors using E4990A impedance analyzer at 1 MHz. The shaded region represents the soft-switching gate charge (Q_G). Gate energy loss, E_G, extracted from (1) for (c) M_1 and (d) M_2.

small-signal C_{ISS} versus voltage and derive Q_G based on (2), when the drain is shorted to the source, which is similar to zero-voltage switching (ZVS). Small-signal measurements of C_{ISS} at 1 MHz for GaN transistors M_1 (60 V, 48 A, part number EPC2031) and M_2 (650 V, 30 A, part number GS66508T) versus V_{GS} are shown in Figs. 3a, b, respectively. Q_G is indicated by the shaded area under C_{ISS} versus V_{GS} curve. Figs. 3c, d present dependency of gate energy loss (E_G) on V_{GS}.

III. Thermal Verification

To verify the proposed method, we designed a thermal setup to record temperature distribution on device under test (DUT) and its gate driver (Fig. 4a). A Quantum Focus Instruments (QFI) infrared (*IR*) microscope with a 512 by 512 pixels array provided thermographs of the test boards (Fig. 4b shows M_1 test board) under operation, with high spatial resolution and accurate emissivity correction. The surface of each test board was coated with black paint to increase the emissivity. LMG1020 gate driver was employed with a 5-V dc supply and PWM signal was provided by a Keysight 33600A waveform generator. To reduce gate-loop inductance and minimize distortion in V_{GS} signal, the driver was placed extremely close to the transistor. Cutouts surrounded heat sources (i.e. the DUT and its gate driver) in order to minimize heat leakage and increase measurement sensitivity.

The DUT was driven with its drain shorted to source (Fig. 5a) and we chose $R_{ON} = R_{OFF} = 0$ for concentrating the loss in

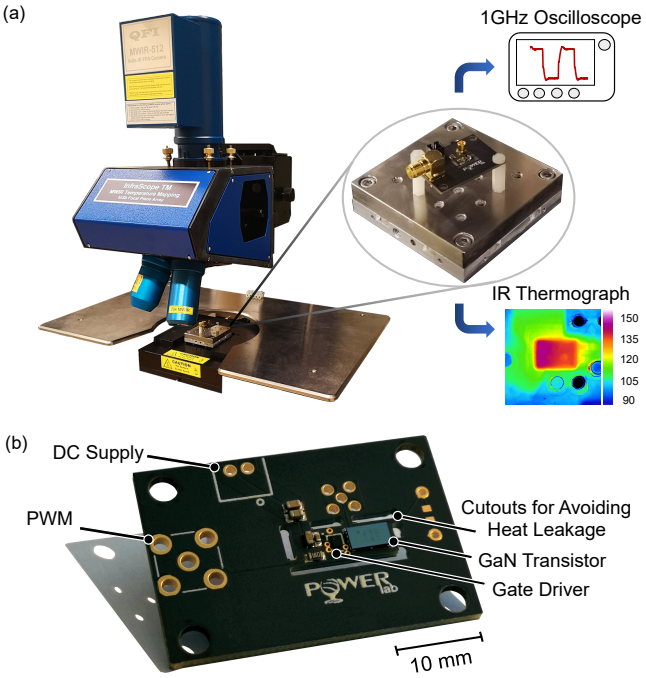

Fig. 4 Experimental setup for temperature mapping between the gate driver and the transistor under test. (a) Setup for experiment consists of DUT (transistor and gate driver), dc supply and PWM signal generator. A high-resolution *IR* camera QFI MWIR-512 extracts the thermograph of the DUT after thermal steady-state is reached. A TPP1000 1-GHz voltage probe measures V_{GS}. (b) The evaluation board for M_1. The inductance between gate driver and the transistor is minimized, with cutouts surrounding gate driver and transistor to avoid heat leakage for higher sensitivity.

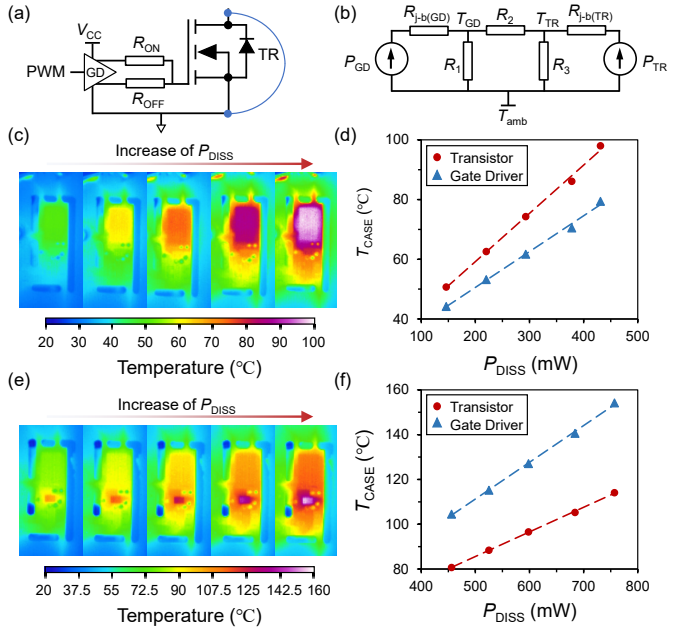

Fig. 5 Thermal calibration and modeling to verify the small-signal method. (a) Electrical schematic of the setup for measuring P_G. For simpler calibration, $R_{ON} = R_{OFF} = 0$. LMG1020 is used to drive M_1 and M_2. (b) Steady-state thermal modeling of the system. (c) DC calibration thermographs of M1 board when only the transistor dissipates power in reverse-conduction mode and (d) corresponding case temperature versus power for the transistor and gate driver. (e) DC calibration thermographs of M_1 board when only the gate driver dissipates power and (f) corresponding case temperature of the transistor and gate driver at each power level. Same method is used for calibration of M_2 board.

DUT and gate driver for simpler calibration. The steady-state thermal model of such circuit is shown in Fig. 5b where P_{GD} and P_{TR} are the portions of gate loss incurred in gate driver and transistor, respectively. Two sets of dc calibrations were performed to obtain thermal resistance values of Fig. 5b. First the transistor was a heat source in reverse conduction (Figs. 5c, d); next, the gate drive was dissipating power by shorting its output (Figs. 5e, f). Thermographs and case temperatures of M_1 and LMG1020 are shown in Figs. 5c-f.

This calibration provided the conductance coefficients (G_{ij}) which were used to extract P_{GD} and P_{TR} values as

$$\begin{bmatrix} P_{GD} \\ P_{TR} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} T_{GD} - T_{amb} \\ T_{TR} - T_{amb} \end{bmatrix} \quad (3).$$

We operated M_1 and M_2 up to 15 MHz and 30 MHz, respectively, and recorded the case temperatures of the gate driver (T_{GD}) and the transistor (T_{TR}) at each frequency, as shown in Figs. 6a, b for M_1 at 15 MHz. By using (3), we extracted the total gate loss as

$$P_G = P_{GD} + P_{TR} \quad (4).$$

A push-pull gate driver is hard switched due to driving a capacitive load (the input capacitance of a FET). Therefore, as

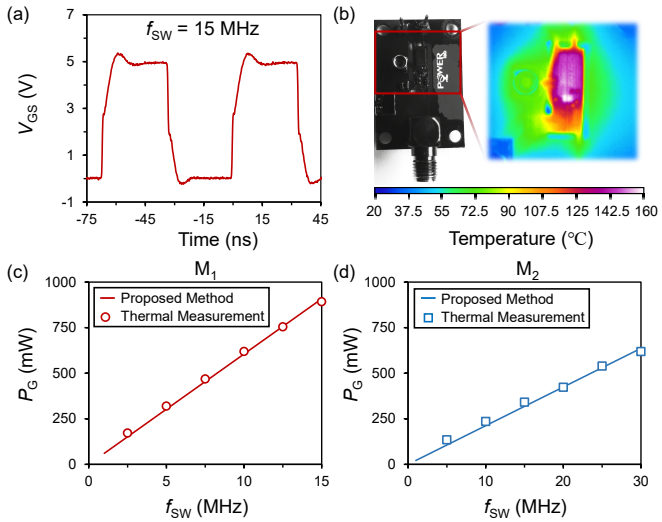

Fig. 6 Validation of electrical method with thermal measurements. (a) V_{GS} waveform applied to M_1 transistor at 15 MHz with turn ON/OFF voltages of 4.9 V/0V and (b) its corresponding thermograph. The PCB is sprayed with black color to increase emissivity. P_G versus f_{SW} for (c) M_1 and (d) M_2 transistors operating between V_{ON} = 5V and V_{OFF} = 0V using LMG1020 gate driver. Thermal results verify the validity of proposed electrical method in evaluation of P_G.

(4) indicates, one needs to sum up the generated heat within the gate driver (due to its hard switching plus conduction loss due to its internal resistance) and that generated inside the transistor due to its inner gate resistance. Adding external gate resistors between the gate driver and the transistor adds more sources of heat on the PCB (which is avoided in this work).

Figs. 6c, d present the agreement between thermal measurement results obtained from (3) and (4) (discrete points) and estimated P_G based on small-signal measurements extracted from (1) and (2) (straight lines).

IV. Discussion

The choice of f_{OSC} in the small-signal measurement becomes important depending on: 1) C_{ISS} value and 2) C_{ISS} variation over frequency. C_{ISS} value typically scales up with the device current rating, and its vatiations depends on the device technology [11]. In [11] various WBG technologies based on GaN and SiC are compared in details.

Fig. 7 presents C_{ISS} versus V_{GS} for transistor M_2 at two different oscillation frequencies (f_{OSC}) of 1 MHz and 10 MHz. The variation of C_{ISS} over f_{OSC} is also shown in the subset of Fig. 7. For all the C_{ISS} measurements in this study, f_{OSC} was set to 1 MHz. At higher frequencies, parasitic elements such as measurement loop inductance induce a resonance, whose frequency (f_R) can be approximated as

$$f_R = 1/2\pi\sqrt{LC_{ISS}} \quad (5)$$

in which L represents the parasitic loop inductance. Therefore, f_R is going to be lower for devices with higher C_{ISS}, making it necessary to choose $f_{OSC} << f_R$.

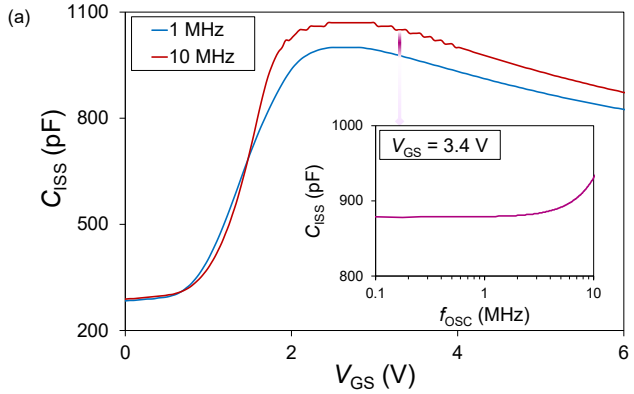

Fig. 7 Variation of C_{ISS} versus V_{GS} with small-signal oscillation frequency in the measurement with impedance analyzer at 1 MHz and 10 MHz for the transistor M_2. The subset shows C_{ISS} versus f_{OSC} at a V_{GS} = 3.4 V. Various WBG technologies exhibit different C_{ISS} versus f_{OSC} behaviors, which needs to be taken into account, for using the proposed method for gate loss evaluation, as described in [11]. Furthermore, f_{OSC} should far enough from f_R, in order to reject the effect of parasitic elements in the small-signal measurement.

V. Conclusion

WBG transistors enable soft-switching converters to achieve high efficiency and large power density at high frequencies, where gate loss becomes an important sources of power dissipation. In this work, we proposed a simple method to evaluate gate loss in soft-switched transistors, based on a small-signal input-capacitance measurement. We developed an accurate thermal model based on *IR* thermographs of transistor and gate driver under calibration, to measure gate loss by sensing the temperature rise of each component under real operation. Thermal measurements validated the small-signal method for evaluation of gate loss in two GaN transistors with different input capacitances. The method is of great significance for high-frequency soft-switched topologies as it precisely evaluates gate loss and can be used for reliable design of drivers and cooling systems, as well as accurate adjustment of dead times for synchronize turn ON in soft-switching topologies. Important considerations for the selection of oscillation frequency were discussed, in order to obtain reliable measurements/evaluations based on the small-signal method. This work highlights the importance of small-signal C_{ISS} versus V_{GS} curve for high-frequency soft-switched designs. At the moment, WBG device datasheets lack such important information; thus, it is recommended that WBG manufacturers include the C_{ISS} versus V_{GS} and C_{ISS} versus f_{OSC} curves in their datasheets.

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