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Protection Coordination in Marine DC Power Distribution Networks

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Dedicated to my family with love

Abstract

The increasing penetration of renewable energy sources, energy storage systems (ESSs), and DC loads (e.g., data center, electric vehicles, and home appliances) has opened the door to DC technology to pave its way into future grids. The shift has been more obvious in the marine domain supported by track records of installed onboard DC solutions since 2013. This new type of power system comes with technical challenges in protection coordination due to no natural current zero-crossing and low fault ride-through capability of power converters. This thesis has focused on the technical challenges tied to protection coordination in DC power distribution networks (PDNs). While marine applications are mainly considered for target DC PDNs, the work is not limited to this area alone.

The thesis starts with the state-of-the-art analysis of marine DC PDN protection. The analysis shows that three-level protection, which consists of three-different time frame protections: fast action - bus separation; medium action - feeder protection; and slow action - power supply protections, has become the dominant trend for marine low-voltage DC PDNs selected for the main research field in the thesis. Along with the analysis, each protection measure is investigated by extensive simulation studies in terms of fault tolerance of equipment against fault energy limited by each measure. In these studies, additional bus capacitance (ABC) and artificial short-circuit methods have been proposed for extending selectivity of feeder protection and protecting voltage source converters (VSCs). The ABC method ensures the fault clearing by a reliable fuse operation that is assisted by the additional energy from the ABC only to the fuse on the faulty feeder. As an alternative to the fuse solution for the VSC protection, the artificial short-circuit method, which blocks the fault current to the rectifier by providing a low impedance path on the AC side, is verified by in-depth simulation studies.

Two-bus DC PDNs rated for 35 kW and 500 V have been implemented for experimental studies. The DC PDNs consist of two DC motor-synchronous generator sets, two diode rectifier systems, a solid-state bus-tie switch, two supercapacitor banks, resistive loads, busbars, and a central controller. In the DC PDNs, the power supply protection method by generator deexcitation is characterized by comprehensive experimental tests for various system parameters. The analytical solution on the fault current during the deexcitation event is newly introduced for rectifier sizing and protection coordination. Apart from the protection topic, a wide range of DC PDN operations have been demonstrated in the implemented DC PDNs, ranging from basic to advanced operations: basic - DC voltage regulation and power sharing control, advanced - soft start (smoothly charging bus potential to the nominal level), seamless transition (transiting islanded and grid-connected modes), load leveling (flattening generator loads by ESSs), transient mitigation (mitigating sudden load changes by ESSs), and zero-emission (powering the marine networks by ESSs near a city or a port).

As the last work in the thesis, a protection scheme based on the three-level protection has been implemented in the DC PDNs. The influences of the system inductance and capacitance are investigated for the bus separation by the bus-tie switch to ensure its proper operation as well as the continuous operation of the adjacent healthy loads after the fault clearing by the fuse. Each protection measure and its settings are thoroughly coordinated from the investigation and the implemented protection scheme is verified by bus and feeder faults artificially generated in the networks. The results prove that the system protection can successfully isolate the faults from the networks with the correct operation of protection measures and enough time margins between the different protections.

Keywords DC microgrids, marine DC power distribution networks, fuse, generator deexcitation, protection coordination, protection scheme, solid-state circuit breaker, three-level protection

Résumé

Le taux croissant des sources d'énergie renouvelables, des systèmes de stockage d'énergie et des charges en courant continu (par exemple, les centres de données, les véhicules électriques et les appareils ménagers) a ouvert la porte aux technologies en courant continu pour ouvrir la voie aux futurs réseaux. Le changement a été plus évident dans le domaine marin, soutenu par les nombreuses applications en courant continu installées à bord depuis 2013. Ce nouveau type de système d'alimentation présente des défis techniques dans la coordination de la protection dûs à l'absence de passage naturel de courant par zéro et à la faible capacité des convertisseurs de puissance à fournir l'alimentation sans panne. Cette thèse se porte sur les défis techniques liés à la coordination de la protection dans les réseaux de distribution d'énergie continue. Bien que les principales applications envisagées pour les réseaux de distribution d'énergie continue en courant continu sont les applications marines, le travail ne se limite pas que à ce domaine.

La thèse commence par l'analyse de l'état de l'art des systèmes de protection des réseaux de distribution d'énergie continue en courant continu. L'analyse montre que la protection à trois niveaux est devenue la tendance dominante pour les réseaux de distribution d'énergie continue en courant continu à basse tension dans les applications marines. Ce type de protection comporte trois protections temporelles différentes: action rapide - séparation de jeux de barres; action moyenne - protection du départ de ligne ; et action lente - les protections d'alimentation électrique. Ainsi la protection à trois niveaux a été sélectionnée comme le principal sujet de recherche de cette thèse. L'analyse de chaque mesure de protection est accompagnée de simulations approfondies qui étudient la tolérance des équipements aux pannes par rapport à l'énergie par défaut limitée par la mesure. Dans ces études, des méthodes de capacité supplémentaire de jeux de barres et de court-circuit artificiel ont été proposées pour étendre la sélectivité de la protection des départs des lignes et protéger les convertisseur à source de tension. La méthode de capacité supplémentaire de jeux de barres garantit l'élimination des défauts par un fonctionnement fiable des fusibles qui est assisté par l'énergie supplémentaire de la capacité supplémentaire de jeux de barres uniquement vers le fusible sur le départ des lignes défectueux. En alternative à la solution fusible pour la protection des convertisseur à source de tension, la méthode des courts-circuits artificiels, qui bloque le courant de défaut vers le redresseur en fournissant un chemin à faible impédance côté courant alternatif, est vérifiée par des études en utilisant des simulations approfondies.

Deux réseaux de distribution d'énergie continue en courant continu à deux bus cotés pour 35 kW et 500 V ont été mis en œuvre pour des études expérimentales. Les réseaux de distribution d'énergie continue en courant continu se consistent en deux groupes électrogènes synchrones à moteur en courant continu, de deux systèmes de redressement à diodes, d'un interrupteur de liaison de départ des lignes à semi-conducteurs, de deux batteries avec des supercondensateurs, de charges résistives, de jeux de barres et d'un contrôleur central. Dans les réseaux de distribution d'énergie continue, la méthode d'alimentation par désexcitation du générateur est caractérisée par des tests expérimentaux complets pour divers paramètres du système. La solution analytique sur le courant de défaut pendant l'événement de désexcitation est nouvellement introduite pour le dimensionnement du redresseur et la coordination de la protection. Outre le sujet de la protection, une large gamme d'opérations des réseaux de distribution d'énergie continue a été démontrée dans les réseaux de distribution d'énergie continue implémentés, allant des opérations basiques aux opérations avancées: de base - régulation de tension en courant continu et le contrôle de partage de puissance, avancé - démarrage progressif (charge en douceur du potentiel du bus au niveau nominal), transition transparente (transit des modes îlotés et connectés au réseau), nivellement de la charge (aplatissement des charges des générateurs

par les systèmes de stockage d'énergie), atténuation des transitoires (atténuation des changements de charge soudains par les systèmes de stockage d'énergie) et zéro émission (alimentation des réseaux marins par les systèmes de stockage d'énergie à proximité d'un ville ou un port).

En tant que dernier travail de la thèse, un schéma de protection basé sur la protection à trois niveaux a été implémenté dans les réseaux de distribution d'énergie continue en courant continu. L'influence de l'inductance et de la capacité du système est étudiée pour la séparation de jeux des barres par le commutateur de couplage de jeux des barres pour assurer son bon fonctionnement ainsi que le fonctionnement continu des charges saines adjacentes après la suppression du défaut par le fusible. Chaque mesure de protection et ses paramètres sont parfaitement coordonnés à partir de l'étude approfondie et le schéma de protection mis en œuvre est vérifié par des défauts de jeux des barres et de départ des lignes générés artificiellement dans les réseaux. Les résultats prouvent que la protection du système peut isoler avec succès les défauts des réseaux avec le bon fonctionnement des mesures de protection et des marges de temps suffisantes entre les mesures de protection.

Keywords réseaux en courant continu, réseaux de distribution d'énergie en courant continu marins, fusible, désexcitation du générateur, coordination de la protection, schéma de protection, disjoncteur à semi-conducteurs, protection à trois niveaux

Acknowledgments

The big bird flies against the wind, the alive fish swims upstream against the current.
Gu Kim

On the day of my turning 40, I am putting an end to my academic journey I have taken since the first day of 2017. As my PhD could be finalized with direct and indirect support from all the people around me, I would like to take this opportunity to express my gratitude and appreciation to them.

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Lausanne, September 26, 2020

List of Abbreviations

ABC	additional bus capacitance
AC	alternating-current
AVR	automatic voltage regulator
DC	direct-current
DP	dynamic positioning
EBL	electronic bus link
EEDI	energy efficiency design index
EMTP-RV	electromagnetic transient program – restructured version
ESL	equivalent series inductance
ESR	equivalent series resistance
ESSs	energy storage systems
HMI	human machine interface
HVDC	high-voltage direct-current
IED	intelligent electronic device
IGBT	insulated-gate bipolar transistor
ILC	intelligent load controller
IMO	International Maritime Organization
KVL	Kirchhoff's voltage law
LVDC	low-voltage direct-current
MMC	modular multilevel converter
MOV	metal oxide varistor
MVDC	medium-voltage direct-current
PCB	printed circuit board

PDNs	power distribution networks
PLC	programmable logic controller
PLL	phase-locked loop
PMSG	permanent magnet synchronous generator
PSV	platform support vessel
pu	per unit
PWM	pulse width modulation
RB-IGCT	reverse blocking-integrated gate-commutated thyristor
RESs	renewable energy sources
RMS	root mean square
SA	surge arrester
SEEMP	ship energy efficiency management plan
SFOC	specific fuel oil consumption
SG	synchronous generator
SSCB	solid-state circuit breaker
TCC	time-current curve
VOC	volatile organic compound
VSC	voltage source converter

List of Symbols

C_{DC}	DC-link capacitance
I^2t_D	limiting load integral
I^2t_F	fault current energy
I_C	collector current
I_{cm}	rated short-circuit making capacity
I_{cs}	rated service short-circuit breaking capacity
$I_{F(AV)M}$	max. average forward current
I_{FSM}	max. surge forward current
I_p	peak let-through current
$I_{T(AV)M}$	max. average forward current
I_{TSM}	max. surge forward current
R_a	stator winding resistance
R_f	fault resistance
T_a	armature short-circuit time constant
t_d	time delay
$T_d^{'}$	direct axis transient time constant
$T_d^{''}$	direct axis subtransient time constant
T_e	exciter time constant
V_{CE}	collector emitter voltage
V_{DRM}	max. repetitive peak forward blocking voltage
V_{RRM}	max. repetitive peak reverse blocking voltage
X_d	direct axis synchronous reactance
$X_d^{'}$	direct axis transient reactance
$X_d^{''}$	direct axis subtransient reactance
$X_q^{''}$	quadrant axis subtransient reactance

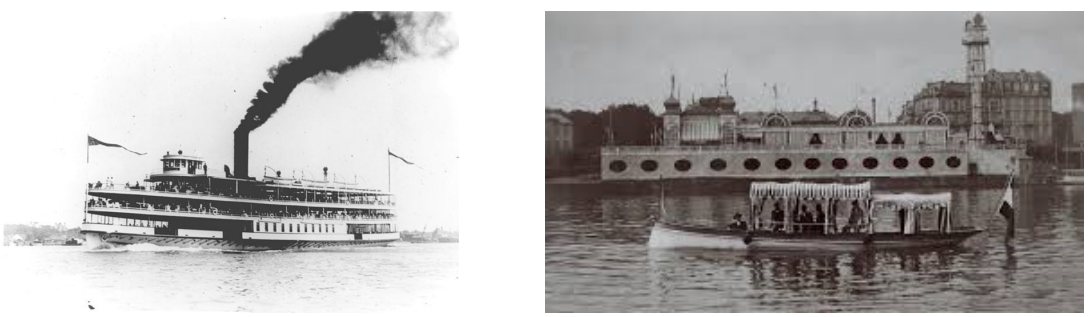
Contents

1 Introduction

On December 31, 1879, the first power distribution networks (PDNs) for incandescent light bulbs were demonstrated by the form of direct-current (DC) [1]. It was followed by the widespread use of the electricity based on the application of DC, which had reached its application in lighting by 1887, powering 103 central stations with 311,400 lamps in the US [2]. This technology was also employed in marine domain. The first electrical installation in marine PDNs was made by DC on the American passenger and freight ship, *SS Columbia*, in 1880 [see **Fig. 1.1(a)**] [3]. Shortly thereafter, this new technology was broadly accepted by both military and commercial vessels, e.g., the German ferry, *Elektra*, in 1886 [see **Fig. 1.1(b)**], the Spanish submarine, *Peral*, in 1888, the American cruiser, *USS Brooklyn*, in 1896, and so forth [3]–[5].

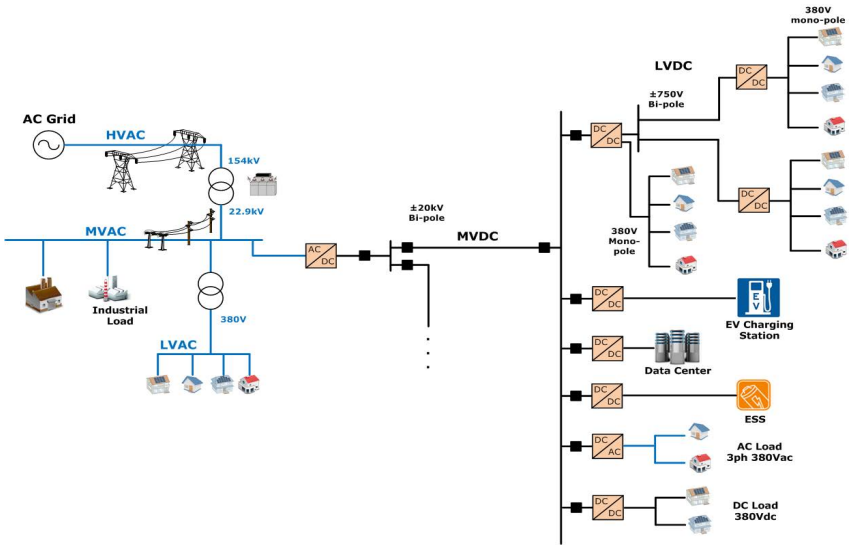
The glory days of the DC power systems were ended with the emergence of the alternating-current (AC) transformer and the AC induction motor in commercial use. With an increase in electrical power demands, the main drawbacks of the DC power system became unequivocally clear in the early 1900s. Compared to AC, it was heavier, larger, and, most importantly, it was difficult to change a voltage level which caused higher power losses and voltage drops for long-distance distribution. Consequently, DC had been gradually losing its dominant position not only in electrical power grids but also in marine PDNs. It is the well-known story of "War of the Currents".

To date, present power systems have been mostly based on the AC technology. The evolution of power electronics technologies, however, allows us to focus on the DC technology again for both power grids and ship networks. Some said this new movement as "Edison's Revenge" or "the Second War of the Currents" [6]. Now, the transition has become reality in modernized electrical grids and marine networks in which power electronics play an important role.

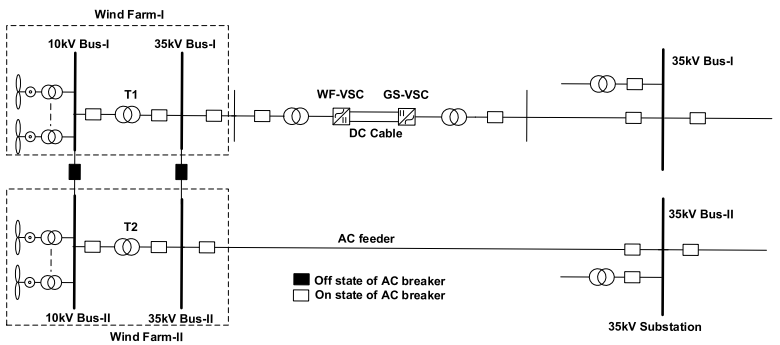


(a) (b)

Fig. 1.1 (a) *SS Columbia*, an excursion steamboat [7] and (b) *Elektra*, an electric boat at the international electrical engineering fair in Frankfurt [8].



(a)



(b)

Fig. 1.2 (a) Example of DC grid configuration in South Korea [9] and (b) network topology of Shanghai Nanhui DC project in China [10].

Conventionally, electricity is transmitted from bulky power plants to consumers through complex electrical networks. During the transmission and the distribution, step-up and step-down voltage conversions are crucially required to minimize power losses. Those have been mostly done by the AC transformers, becoming a key component for voltage coordination. Recently, however, the rapid expansion of renewable energy sources (RESs), energy storage systems (ESSs), and DC loads (e.g., data center, electric vehicles, and home appliances), which are connected through power converters and/or have the DC nature, has opened the door to the DC technology to integrate these new types of power sources and loads more easily or efficiently into the grids, as shown in **Fig. 1.2**. This change has also extended DC PDNs from point-to-point to meshed multi-terminal links [11].

The shift has been observed more obviously in the marine domain. In April 2013, ABB delivered the first platform support vessel (PSV), *Dina Star*, built by its solution 'Onboard DC Grid' [12]. In October of the same year, Siemens also delivered the DC-powered PSV, *Edda Ferd*, equipped with 'BlueDrive Plus C' [13]. The last six years have witnessed outstanding growth of DC-powered dynamic

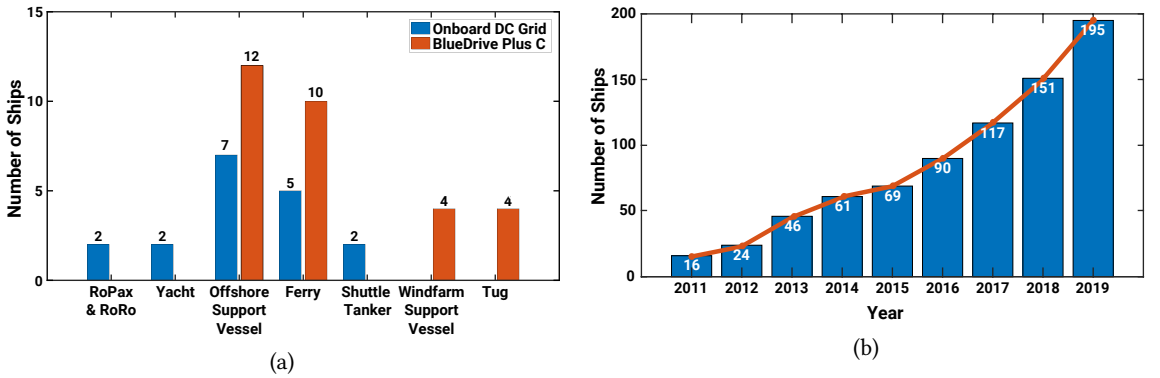


Fig. 1.3 (a) DC ships built by 'Onboard DC Grid' and 'BlueDrive Plus C' since 2013 [15], [16] and (b) ships with installed battery energy storage systems [17].

positioning (DP) and passenger vessels. There are 48 ships and more constructed by the two solutions for this period, as shown in **Fig. 1.3(a)**. Moreover, the increase in the battery integration on a ship [see **Fig. 1.3(b)**] shows that the ship network towards DC PDNs due to its DC nature. The representative ship is the world's first large-size battery-powered Norwegian car ferry, *Ampere*, in 2015 [14]. With these trends, it could be stated that the DC technology has been becoming one of the prominent options for some types of vessels.

1.1 Motivation

According to [18], international shipping emitted more than 2.2% of the total CO_2 emission in 2012. Furthermore, it is expected that the emission level will rise 50% to 250% by 2050 depending on future economic growth and energy consumption. As the global standard-setting authority, in 2011, the International Maritime Organization (IMO) adopted mandatory energy efficiency regulations [e.g., energy efficiency design index (EEDI) and ship energy efficiency management plan (SEEMP)] to control the greenhouse gas emissions from the shipping sector. In accordance with the EEDI as presented in **Tab. 1.1**, newly constructed ships of 400 gross tonnages and above have to increase the energy efficiency to meet the reduction rates, consisting of the three phases. Finally, by 2025, the ships have to be designed to have 30% less energy consumption than those built in 2004.

Tab. 1.1 Reduction factors in percentage for EEDI. Data from [19].

Ship Type	Phase 0	Phase 1	Phase 2	Phase 3
	Jan 2013 - Dec 2014	Jan 2015 - Dec 2019	Jan 2020 - Dec 2024	Jan 2025 and onwards
Bulk carrier	0	10	20	30
Gas carrier	0	10	20	30
Tanker	0	10	20	30
Container ship	0	10	20	30
General cargo ship	0	10	15	30
Refrigerated cargo carrier	0	10	15	30
Combination carrier	0	10	20	30

A ship is an off-grid stand-alone system (or a microgrid) without the need to comply with strict utility grid codes, which allows for the flexibility to utilize a new concept of power systems. This is one of the reasons why the movement toward DC has been proceeding actively in the marine sector. The other reason is more importantly that the DC technology could improve the vessel's fuel efficiency with the following advantages:

Fuel saving with variable-speed generators. Typical marine engines are designed to have the optimum specific fuel oil consumption (SFOC) in the 60-80% load range with the rated rotational speed [20]. On the other hand, reduced rotational speeds are required to minimize the fuel consumption at lower engine loads, as shown in **Fig. 1.4**. While the machine rotational speed in AC PDNs has to be a constant to maintain system frequency at any engine loads, DC permits the use of variable-speed generators because AC of any frequency is converted to DC in DC PDNs. With the variable-speed generator, fuel savings achieved are about 25% at 10% loading and about 10% at 40% loading, respectively, in the calculated case (see **Fig. 1.4**).

Easy integration of ESSs. To integrate ESSs in AC PDNs, at least one AC-DC converter is necessary between the system and the ESSs which have their terminals with DC. Depending on output voltages of ESSs and types of AC-DC converters, a DC-DC converter may be additionally requested. By contrast, ESSs can be connected to DC PDNs through a DC-DC converter or directly (without any converters). The fewer conversion stages help to cut down converter cost and power losses. To conclude, ESSs could be more easily integrated in DC PDNs. The benefits with the ESS installation are: zero-emission operation at harbours, running fewer engines, running engines at optimal loads, avoiding transient engine loads, and facilitating energy harvesting [21].

Weight and footprint reduction in electrical installations. First of all, with the freedom from dependency on a constant AC frequency, high-density high-speed machines, which have smaller weight and volume compared to the fixed systems, can be applied in DC PDNs. Secondly, bulky transformers, which are essential for voltage coordination and harmonics mitigation in AC PDNs, are not needed in DC PDNs. Lastly, the use of AC switchgear can be avoided in DC PDNs with new protection schemes, not relying on conventional mechanical breakers and relays. [23] provides a weight comparison example for a PSV. The weight reduction is about 26% compared to the traditional AC concept.

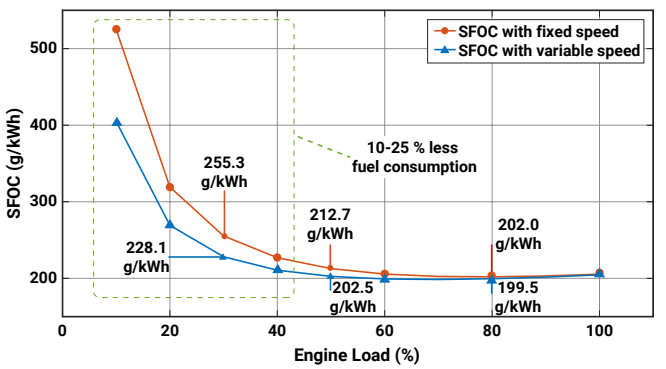


Fig. 1.4 Comparison of SFOC between fixed-speed and variable-speed generators. The SFOC is calculated by the data from [22].

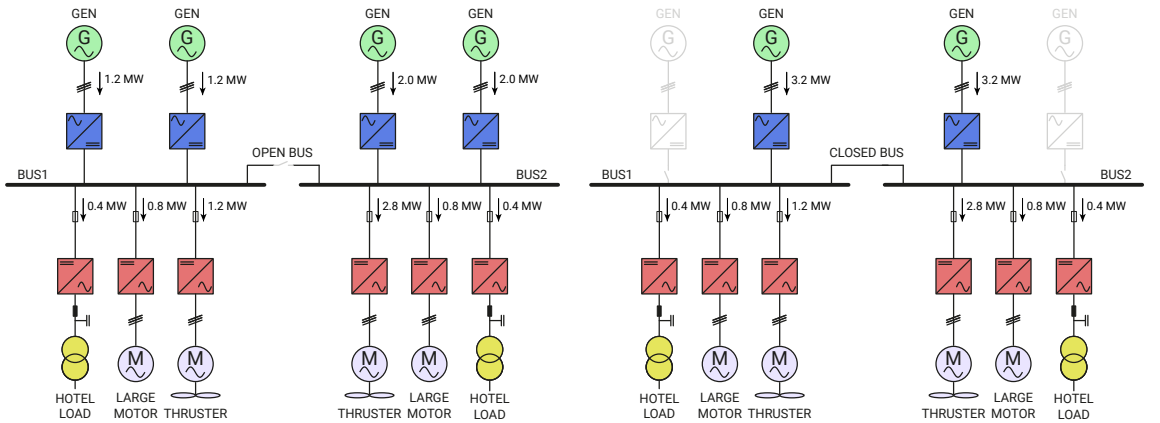


Fig. 1.5 Example of power generation and consumption in DP vessels: (a) open bus and (b) closed bus.

Tab. 1.2 Comparison of fuel consumption between open-bus and closed-bus operations in DP vessels. The SFOC values are taken from **Fig. 1.4** at 30%, 50% and 80% load conditions. For the power generation of 6.4 MWh, the conditions assumed are: open bus - two generators at 30% load and two generators at 50% load [see **Fig. 1.5(a)**] and closed bus - two generators at 80% load [see **Fig. 1.5(b)**].

Generator Type	SFOC (g/kWh)			Fuel Consumption at 6.4 MWh (kg)		Fuel Saving (%)
	at 30%	at 50%	at 80%	Open Bus	Closed Bus	
Fixed speed	255.3	212.7	202.0	1463.6	1292.5	11.7
Variable speed	228.1	202.5	199.5	1357.7	1276.8	6.0

Optimization of running engines by closed-bus operation. During the DP mode, a bus-tie switch, which is a device to connect and disconnect two bus sections (see **Fig. 1.5**), should be normally open due to the safety in AC PDNs [24]. To provide electric power needed in this mode, almost all generators should be in operation for heavy as well as light load conditions and this makes DP ships inefficient [see **Fig. 1.5(a)**] [25]. This limitation can be overcome by using DC PDNs based on solid-state technologies. With solid-state bus-tie switches operated within several tens of microseconds, the closed-bus operation, which allows for reducing the number of running engines, is possible without the safety issue in the DP mode [see **Fig. 1.5(b)**] [26]. An example of the fuel saving with the running engine optimization is provided in **Tab. 1.2**.

The attractive new systems bring with technical challenges in protection coordination, a result of no natural current zero-crossing, very low fault withstand capability of power converters, hybrid AC-DC protection coordination, and no standard for system configurations and protection schemes. The details of the challenges are as follows:

No natural current zero-crossing. When a fault is detected in AC systems, a circuit breaker interrupts the fault current by actuating the moving contact backwards from the fixed contact. Initially, although the two contacts are separated mechanically, they are connected electrically through the arc. In AC, the arc is extinguished at every current zero-crossing. If the dielectric strength between the two contacts is higher than the recovery voltage at the instant of the zero-crossing, the current could be finally interrupted in the time ranges about 3-5 cycles (60 –100 ms at 50 Hz) [28].

Contrarily, there is no polarity change in the DC fault current. To extinguish the current without the zero-crossing, mechanical DC circuit breakers are based on a high volume of arc chutes [29]. When the contacts are open, the arc is established and then the arc moves to the arc chute. The reversal arc voltage, which is proportional to the arc distance, is built up and the current is quenched if the arc voltage is higher than the source voltage. When the solid-state technologies are employed alone or in combination with mechanical elements (a hybrid circuit breaker), the increase in cost cannot be avoided due to the increasing number of components requested. Additionally, these circuit breakers will lead to additional operational cost caused by on-state power losses in semiconductors. To sum up, the DC fault characteristics make the development of DC circuit breakers difficult or costly compared to conventional AC circuit breakers.

Very low overloading capability of power converters. Conventional AC equipment is designed to sustain the maximum fault current over several hundreds of milliseconds [30], [31]. Taking a power transformer as an example, the maximum fault current under the worst condition is calculated during the design phase. Based on this current, the electrical and mechanical design of the transformer is conducted to withstand the current as well as the electromotive force generated by the current for 500 ms [30]. This high overloading capability provides an enough time to proceed all the process of system protection, i.e., fault detection, fault localization, fault isolation, and backup protection.

Differently with the AC protection, such a time frame in order of several hundreds of milliseconds is unavailable for the DC protection. The fault in DC PDNs should be typically cleared within the range of several milliseconds [32]. This is because a power converter based on semiconductors has very low overloading capability (see **Fig. 1.6**). This implies multiple things. First, fast circuit interrupters are indispensable to handle the fault current within a given time. Secondly, the DC protection should be much faster than the AC protection. Lastly, additional devices (e.g., current limiting inductors) or oversized semiconductors are needed if the protection is not operated for the time range of semiconductor overloading capability.

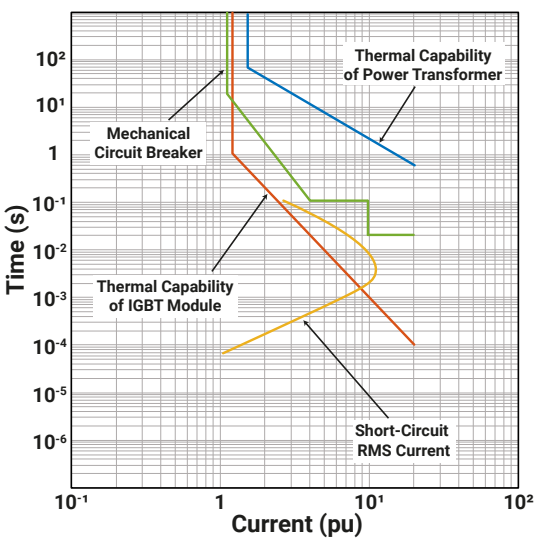


Fig. 1.6 Time-current curve (TCC) comparison of AC and DC devices against root mean square (RMS) short-circuit current [27]. This exemplary TCC shows that the power transformer can be protected by the mechanical circuit breaker, while the failure of the insulated-gate bipolar transistor (IGBT) module cannot be avoided.

Tab. 1.3 Generator-rectifier combination matrix and multi-phase multi-pulse power supply configurations [33]. While a synchronous generator (SG) can be combined with four different rectifiers, a permanent magnet synchronous generator (PMSG) can be only coupled with active rectifiers [e.g., conventional voltage source converter (VSC) and modular multilevel converter (MMC)] due to lack of its excitation control. Note that a recent work of [34] has proposed the combination of a PMSG and a diode rectifier.

Generator-Rectifier Combination					Nx3-Phase Nx6-Pulse Power Supply	
Generator Type	Rectifier Type					
	Diode	Thyristor	VSC	MMC	Configuration	Remarks
SG	✓	✓	✓	✓	Parallel	Constant V & Increasing I
PMSG			✓	✓	Series	Increasing V & Constant I

Hybrid AC-DC protection coordination. While the distribution network is formed with DC, the power generation and consumption have still relied on mature and economic AC technologies. The protection of the conventional AC protection should consequently be coordinated with the newly employed DC protection. For the reliable hybrid AC-DC protection coordination, several differences between both systems have to be taken into account: equipment overloading capabilities, fault characteristics, protection schemes, and protective devices.

No standards for system configurations and protection schemes. At this early stage of DC PDNs, the standard configurations and protections, widely accepted or internationally standardized, are not established. Currently, industrial manufacturers have pushed the market forward with their solutions, having different configurations and protections. On the other hand, the design and protection of DC PDNs are more complicated by the use of solid-state technologies in contrast to AC PDNs. Power supply systems in DC PDNs are a representative example. There are various combinations of generators and rectifiers, as provided in **Tab. 1.3**. Furthermore, multi-phase multi-pulse power supply systems can be configured in series and parallel [33]. This complexity in the combination and the configuration is one of the main barriers to establish the standard configurations and the protection schemes for DC PDNs.

1.2 Objectives and Contributions

In the view of the above discussions, this thesis focuses on the technical challenges tied to protection coordination in DC PDNs, predominantly focusing on marine applications, but not limited to, which could represent DC microgrids (off-grid stand-alone grids) including power supplies, distribution systems, loads, and ESSs, as shown in **Fig. 1.7**. The two-bus DC PDNs considered for all case studies presented in the thesis consist of two supplies, a thruster, a large motor, and a hotel load (connected through AC switchboard) at each bus. Both DC buses are connected through a DC bus-tie switch based on solid-state technology. Also, synchronous generators coupled with diode, thyristor, and active rectifiers are taken into account for the power supply systems.

Based on the two-bus DC PDNs, the thesis aims to extend an up-to-date protection method (three-level protection, as discussed later), commercially adopted, for marine DC PDNs. The objectives selected to achieve the main goal are as follows:

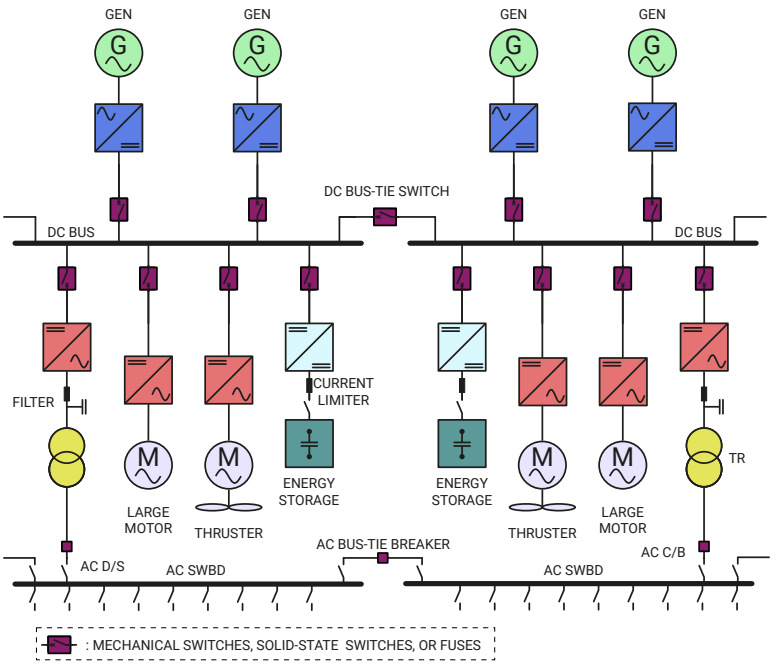


Fig. 1.7 Considered DC microgrids consisting of power supplies, distribution systems, loads, and ESSs.

- Improvement of feeder protection by fuse technology in terms of selectivity and sensitivity.
- Examination of power supply protection concerning overloading capabilities of rectifiers.
- Characterization of the impacts of synchronous generator deexcitation during fault events
- Demonstration of flexible DC grid operations with solid-state technologies and ESSs.
- Verification of integrated three-level protection extended in this work.

Taking the three-level protection as the fundamental protection scheme, the main contribution of this thesis is the extension of the three-level protection for reliable protection coordination. Further detailed contributions of the thesis are summarized hereafter.

- An additional bus capacitance (ABC) method is proposed for the feeder protection based on high-speed fuses, aiming to provide selectivity and sensitivity under any fault conditions. The performance of the ABC method is verified by simulation studies and experimental tests.
- Overloading capabilities of a diode rectifier, a thyristor rectifier, and VSCs are analyzed against DC short-circuit currents limited by each power supply protection. As a new solution, an artificial short-circuit method is proposed for the VSC protection, which currently relies on the fuse technology.
- Dynamic behaviours of the synchronous generator deexcitation are investigated with analytical and experimental approaches. Furthermore, for the deexcitation, comprehensive system studies are provided for different subtransient reactance, fault resistance, DC-link capacitance, fault resistance, exciter response, and time delay.

- Flexible operating modes of DC PDNs are demonstrated with the solid-state DC bus-tie switch, which has a smooth potential charging function, and the supercapacitor-based ESSs. The operating modes demonstrated are: automatic DC voltage regulation, power sharing function, soft start, seamless transition, load leveling, transient mitigation, and zero-emission.
- A protection scheme based on the three-level protection is implemented in the DC PDNs. Each protection measure and its settings are thoroughly coordinated and the implemented protection scheme is verified by bus and feeder faults artificially generated in the networks. The results prove that the system protection can successfully isolate the faults from the networks with the correct operation of protection measures.

1.3 Thesis Outline

This thesis is organized in 9 chapters.

Chapter 2 provides an overview of the general protection technologies in DC power distribution networks as well as the state-of-the-art protection schemes in marine DC power distribution networks. The analysis shows that the three-level protection, which consists of three-different time frame protections: fast action - bus separation; medium action - feeder protection; and slow action - power supply protections, has become the dominant trend for marine low-voltage DC power distribution networks selected for the main research field in the thesis.

Chapter 3 presents the feeder protection by high-speed fuses. The additional bus capacitance method, which can supply the additional energy only to the fuse on the faulty feeder during a fault event, is proposed to ensure the fault interruption by a reliable fuse operation with the consideration of selectivity and sensitivity. The performance of the proposed method is verified by extensive simulation studies under various conditions.

Chapter 4 investigates the performance of power supply protection methods with various case studies. The modeling of three-different low-voltage DC power distribution networks is carried out with the discussions on their configurations, design considerations, and controls. The performance of each protection method is analyzed by comparing the fault energy limited by the protection method and the overloading capability of rectifiers. Moreover, an artificial short-circuit method, which limits the fault current to the rectifier by providing a low impedance path on the AC side, is proposed for the voltage source converter protection.

Chapter 5 presents the impacts of synchronous generator deexcitation dynamics on the diode rectifier protection. The analytical expression of a DC short-circuit current is introduced considering a circuit topology, transient generator dynamics, and generator deexcitation. The DC fault currents under the deexcitation are comprehensively examined for different system factors: subtransient reactance, fault resistance, DC-link capacitance, exciter response, and time delay. Results are collected from a scaled-down experimental test setup.

Chapter 6 demonstrates flexible operating modes of two-bus DC power distribution networks, consisting of two generators operated at different frequencies. First, automatic DC voltage regulation of each power supply is verified by step-load changes. Secondly, power sharing function is implemented and validated with two different tests. Lastly, two operating modes for the DC power distribution

networks are demonstrated with new functions of the solid-state bus-tie switch: soft start - smoothly charging bus potential to the nominal level; and seamless transition - promptly supplying electric power to the bus experienced a power outage during the open-bus operation.

Chapter 7 presents extended DC system operating modes with energy storage systems. For the energy storage systems, two supercapacitor banks (2 × 2 F) are integrated into the lab-scaled test setup through DC-DC converters. The potential benefits of energy storage inside the DC power distribution networks are examined with the demonstration of the following operating modes: transient mitigation - supporting transient demands by energy storage with short time constants; load leveling (peak shaving) - operating generators at optimal loads by storing energy during light load conditions and providing it during too heavy load conditions; and zero-emission operation - turning *OFF* generators and powering the networks by energy storage when a ship is entering or exiting a port.

Chapter 8 validates an integrated protection scheme in two-bus DC power distribution networks. The three-level protection is implemented in the lab-scaled test setup (fast action - bus separation by a solid-state bus-tie switch, medium action - feeder protection by a high-speed fuse, and slow action - generator deexcitation). The protection scheme is evaluated by testing actual operating times of the three actions and the fault energies limited by those. Bus and feeder faults are artificially generated in the networks, and the system protection successfully isolates the faults from the networks with the correct operation of protection measures and enough time margins between the actions.

Chapter 9 summarizes the main findings and the contributions of the thesis. In addition to the summaries, future research perspectives in this topic are outlined.

1.4 List of Outcomes

The scientific outcomes in conjunction with the PhD thesis are:

Journal papers:

J1. **S. Kim**, G. Ulissi, S.-N. Kim, and D. Dujic, "Protection coordination for reliable marine dc power distribution networks," *IET Electric Power Applications*, pp. 1–8, 2020 (Under Review)

J2. G. Ulissi, **S. Kim**, and D. Dujic, "Solid-state technology for shipboard power distribution networks," *IEEE Transactions on Industrial Electronics*, pp. 1–8, 2020 (Under Review)

J3. **S. Kim**, J. Kucka, G. Ulissi, S.-N. Kim, and D. Dujic, "Solid-state technologies for flexible and efficient marine dc microgrids," *IEEE Transactions on Smart Grid*, pp. 1–8, 2020 (Under Review)

J4. **S. Kim**, S.-N. Kim, and D. Dujic, "Impact of synchronous generator deexcitation dynamics on the protection in marine DC power distribution networks," *IEEE Transactions on Transportation Electrification*, pp. 1–10, 2020 (Early Access)

J5. **S. Kim**, S.-N. Kim, and D. Dujic, "Extending protection selectivity in DC shipboard power systems by means of additional bus capacitance," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 5, pp. 3673–3683, May 2020

Conference papers:

C1. **S. Kim**, J. Kucka, S.-N. Kim, and D. Dujic, "Improving energy efficiency in dc microgrids with integrated energy storage," in *The 26th international conference and exhibition on electricity distribution (CIRED 2021)*, Jun. 2021 (Under Review)

C2. **S. Kim**, S.-N. Kim, and D. Dujic, "Deexcitation characterization for power supply protection in DC shipboard power systems," in *2020 IEEE Transportation Electrification Conference and Expo (ITEC)*, Jun. 2020, pp. 1-6 **(**Student Paper Award)

C3. **S. Kim**, S.-N. Kim, and D. Dujic, "Protection coordination in DC shipboard power systems: Challenges, current status and new technologies," in *The 25th international conference and exhibition on electricity distribution (CIRED 2019)*, Jun. 2019, pp. 1–5

C4. **S. Kim**, G. Ulissi, S.-N. Kim, and D. Dujic, "Marine DC power distribution networks," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2019, pp. 1–8

C5. **S. Kim**, D. Dujic, and S.-N. Kim, "Achieving protection selectivity in DC shipboard power systems employing additional bus capacitance," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2018, pp. 3377–3382

C6. **S. Kim**, D. Dujic, and S.-N. Kim, "Review of protection coordination technologies in DC distribution systems," in *24th International Conference on Electrical Engineering (ICEE 2018)*, Jun. 2018, pp. 1–6

C7. **S. Kim**, D. Dujic, and S.-N. Kim, "Protection schemes in low-voltage dc shipboard power systems," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Jun. 2018, pp. 1–7

C8. Y. Park, **S. Kim**, H. Jeong, S.-N. Kim, W. Lee, and D. Won, "Fault current characteristics and protection scheme of LVDC microgrids," in *KIEE Summer Annual Conference Proceedings*, Jul. 2017, pp. 1–6

Patent:

P1. **S. Kim**, Y. Park, D. Lee, S.-N. Kim, and D. Dujic, *DC shipboard power system*, KR Patent 10-2018-0116473, filed Sep. 2018, and issued May 2020

Invited talk:

T1. **S. Kim** and D. Dujic, "Technologies and applications of DC grids in Europe," in *Korea-Europe Collaboration Workshop for Energy Transition - BIXPO 2018*, Nov. 2018

Other outcomes, not directly related to the scope of the thesis:

Conference papers:

C1. Y. Park, **S. Kim**, and S.-N. Kim, "A comparative study on the topology of high power solid state transformer for MVDC to LVDC link," in *24th International Conference on Electrical Engineering (ICEE 2018)*, Jun. 2018, pp. 1–11

C2. J. Heo, **S. Kim**, J. Kim, and S.-N. Kim, "An improved modeling of transformer inrush current for voltage drop analysis," in *24th International Conference on Electrical Engineering (ICEE 2018)*, Jun. 2018, pp. 1–10

C3. D. Lee, Y. Park, **S. Kim**, and S.-N. Kim, "Study on analysis of wye-delta open transition current for motor starting and molded case circuit breaker selection," in *24th International Conference on Electrical Engineering (ICEE 2018)*, Jun. 2018, pp. 1–13

Patents:

P1. Y. Park, S. Ryu, S.-N. Kim, **S. Kim**, S. Milovanovic, and D. Dujic, *Power converting apparatus having scott transformer*, International Patent 2019-005262, filed Nov. 2019 (Pending)

P2. Y. Park, S. Ryu, S.-N. Kim, **S. Kim**, S. Milovanovic, and D. Dujic, *Power converting apparatus having scott transformer*, KR Patent 10-2018-0050472, filed May 2018 (Pending)

Technical brochure:

B1. CIGRE WG A3.38, "Shunt capacitor switching in distribution and transmission systems," *CIGRE Technical Brochure*, 2020 (Main Contribution: Chapter 6. Switching of filter banks) (Will be published soon)

2
State-of-the-art

This chapter provides an overview of the general protection technologies in DC power distribution networks as well as the state-of-the-art protection schemes in marine DC power distribution networks. The analysis shows that the three-level protection, which consists of three-different time frame protections: fast action - bus separation; medium action - feeder protection; and slow action - power supply protections, has become the dominant trend for marine low-voltage DC power distribution networks selected for the main research field in the thesis.

2.1 Introduction

Protection in electrical power systems is to minimize the impact of any system faults. The fundamental concepts of the system protection are [35]:

- reliability - correct operation of system protection
- selectivity - the maximum system availability with the minimum area disconnection
- speed - fast operation to reduce equipment damage and avoid system instability
- simplicity - the minimum number of protective devices and associated components
- economical efficiency - high functionality with the minimum cost

With the consideration of the fundamental protection concepts, the general procedure shown in **Fig. 2.1** is used for DC system protection [36]. First, when a fault occurs in DC PDNs, it has to be identified promptly. One important thing for the detection is that the fault has to be distinguished from any normal transients to avoid an abnormal operation of system protection. For the reliable DC fault detection, signal processing-based methods have been proposed in addition to conventional direct measurement methods [37]–[43].

Secondly, fault localization is necessary to continuously supply electric power to healthy parts by selectively isolating faulty parts. The fault impedance calculated by transient voltage and current provides the information on a fault location. For long-distance point-to-point DC networks, the amplitude of the calculated fault impedance represents the fault location without any communication. Low fault impedance (high current increase and voltage drop) means a near fault, while high fault impedance (low current increase and voltage drop) indicates a far fault, including higher line impedance [44]. However, it is a challenge to determine the fault location only with the fault impedance in short-distance and complex DC networks. It is for this reason that there are approaches to employ communication-based fault locating methods [39], [45].

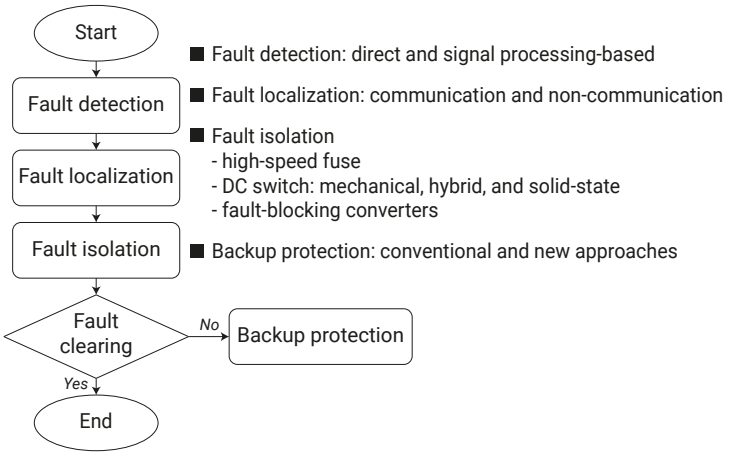


Fig. 2.1 Procedure of DC power system protection.

Thirdly, to prevent damages of any other equipment, the fault should be interrupted rapidly by protective devices: high-speed fuses, DC switches (or circuit breakers), and fault-blocking converters. Although a fuse has notable disadvantages, e.g., manual replacement of the fuse if it blows and low reliability in protection compared to circuit breakers, it is still an attractive solution because of its high breaking capability at low cost. A switch or a circuit breaker is a primary element in the protection with its functions of reliable operation and selective interruption. A wide range of research activities have been performed for three different types of DC switches: mechanical, hybrid, and solid-state [46]–[49]. Otherwise, a few converters, e.g., thyristor converter and full-bridge MMC, can handle the DC fault current [50], [51]. It contributes to open the possibility of breakerless systems.

Lastly, backup protection can be considered for a primary protection failure to increase the reliability of the protection system. The issue of backup protection in the DC networks is how to quickly initiate backup protection without the maloperation and with the minimum impact.

2.2 General Overview of DC Protection

An overview of each protection procedure is provided with the short discussions on benefits and limitations of approaches, currently employed and/or recently proposed for DC protection.

2.2.1 Fault Detection

There are two main categories for the fault protection: direct measurement methods and signal processing-based methods, as given in **Tab. 2.1**. A fault in electrical systems can be characterized by an increase in current and a decrease in voltage. The current flow may also be different from normal conditions depending on fault locations. The first category directly uses the characteristics of measured voltage and current such as their amplitudes, derivatives, and directions. These methods provide fast fault identification with low computational resources. However, they are highly sensitive to noise and it may make these detection methods less reliable. The second is based on signal processing techniques, e.g., wavelet analysis and travelling wave analysis. There are lots of works on

Tab. 2.1 Fault detection techniques.

Category	Fault Detection	Main Benefit	Main Limitation
Direct measurement	Undervoltage (amplitude) [37]	Faster detection	Less reliable
	Voltage & current derivatives [38], [55]		
	Overcurrent (amplitude) [39], [56]		
	Current difference (or direction) [40], [57]		
	Impedance (or distance) [41], [58]		
Signal processing-based	Wavelet analysis [38], [42], [52], [54]	Higher accuracy	Slower detection
	Travelling-wave analysis [43], [52], [53]		

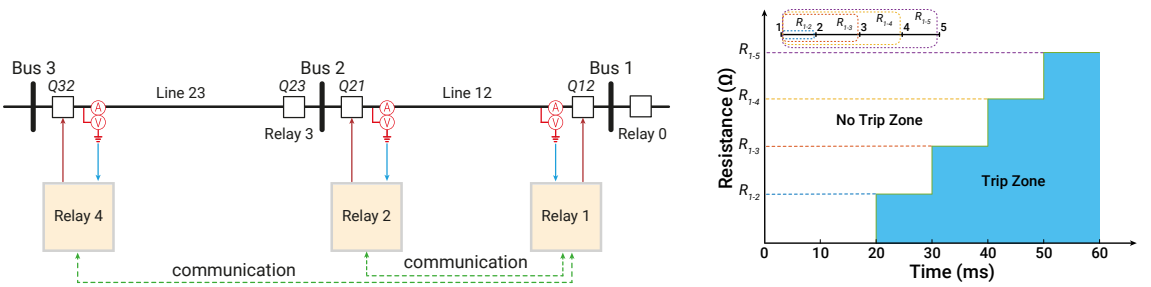
the signal processing approach [38], [42], [43], [52]–[54]. The works report that the signal processing approach is superior than the direct approach in terms of fault detection and localization. However, the signal processing approach also brings negative impacts on detection time and implementation.

2.2.2 Fault Localization

Fault localization is required to minimize the impact of the fault by selectively removing a faulty part. Fault localization based on communication [see **Fig. 2.2(a)**], which has been reported to provide high accuracy in fault locating, is based on the data transferring between several adjacent local relays or the data gathering into a central controller [45], [59]. Therefore, it is not possible to avoid a certain time delay. By contrast, non-communication measures can rapidly operate local circuit breakers when measured signals are higher than preselected thresholds. In this way, fault localization between different protection zones is given by time-inverse methods, selecting different operating times depending on amplitudes of fault current, voltage dip, or impedance [39], [58], [60] [see **Fig. 2.2(b)**]. However, providing selectivity with these time-inverse methods is a challenging issue in DC networks due to low DC cable impedance and fast fault-clearing requirement.

2.2.3 Fault Isolation

Fault isolation methods are classified into four groups: (a) high-speed fuse with DC isolator, (b) fault-blocking converter with DC isolator, (c) conventional converter with AC circuit breaker, and (d)



(a) (b)

Fig. 2.2 Fault localization: (a) communication-based [59] and (b) non-communication [60].

conventional converter with DC circuit breaker.

The fuse is made up of a metallic wire or strip that is melt down by an overcurrent. With this simple configuration, the fuse is an economic solution and convenient to employ. Furthermore, high-rupturing capacity fuses can be applied to high-power systems with their very high-interrupting ratings. Those are the reasons why the fuses are widely accepted into various industrial applications. On the other hand, the blown fuse has to be manually replaced with a new fuse, while circuit breakers are simply resettable after the breaking operation. It is also difficult to achieve the fuse discrimination between upstream and downstream feeders unless the fuses have significant difference in breaking ratings. It means that the use of the fuse installed at the supply side makes the system less reliable.

The fault-blocking converter, e.g., a thyristor rectifier and a full-bridge MMC, can handle the fault current by itself without any circuit breakers. Once the fault is detected, a controller of a thyristor rectifier forces the firing angle to 120° to extinguish the fault current by reversing the DC voltage polarity, using so-called fold-back protection control [50]. With this control, the thyristor rectifier has a competitive advantage in the system protection. The full-bridge MMC can also make the DC voltage to zero as well as to negative during the fault event. The disadvantages of the MMC are its high cost and high conduction losses, and the fact that it is suited for MVDC and HVDC applications.

The approach by means of the conventional converter with AC CB is proposed in [61]. In this way, the protection technology is already mature and there are lots of commercial products to implement this protection scheme with the expected installation cost. However, this method requires to install a very high AC coupling reactor or an oversized converter to sustain the fault current for a long interrupting time of AC circuit breakers (3 –5 cycles).

As the last approach for the isolation, there are three types of DC switches: mechanical, hybrid (a mechanical circuit breaker combined with solid-state technology), purely solid-state circuit breakers (SSCB). SSCBs have been proposed and employed for the marine LVDC PDNs due to the ability of ultra-fast fault clearing compared to mechanical and hybrid circuit breakers. However, the use of

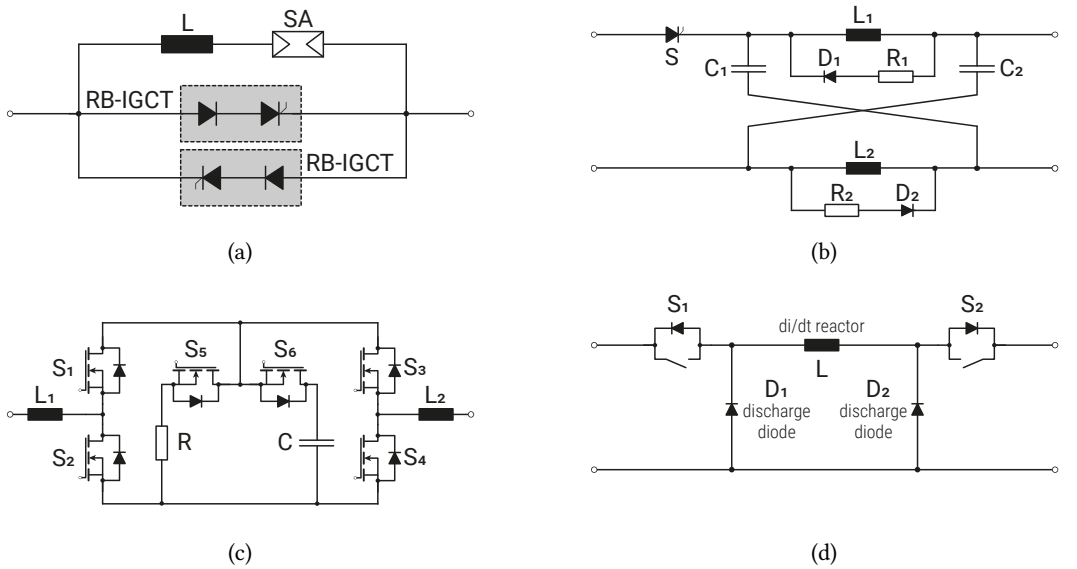


Fig. 2.3 SSCB topologies: (a) interrupting [46], (b) resonant [47], (c) resistive [48], and (d) limiting [49].

SSCBs is generally limited to the bus-tie purpose due to their high cost. In the aspect of a circuit topology, SSCBs commonly include semiconductors to interrupt the overcurrent, inductors to limit the rate of rise of the overcurrent, and protection circuits to dissipate inductive energy and mitigate overvoltage [46]–[49]. These SSCBs can be classified by ways to interrupt the current and dissipate inductive energy stored in the system during the interruption: interrupting, resonant, resistive, and limiting topologies, as illustrated in **Fig. 2.3**. The operational principle of each topology is briefly summarized.

- Interrupting topology [**Fig. 2.3(a)**]: the current in the circuit is interrupted by reverse blocking semiconductors (e.g., RB-IGCT) and the stored energy is dissipated by a surge arrester (*SA*) installed in parallel that can also reduce overvoltage on the semiconductors.
- Resonant topology [**Fig. 2.3(b)**]: when the fault current flows through the SSCB, the resonant circuit creates an artificial current zero without any active circuits. During this current zero, the thyristor (*S*) is turned *OFF* and the energy in inductances (L_1 and L_2) is dissipated in the respective anti-parallel diode and resistor.
- Resistive topology [**Fig. 2.3(c)**]: when the main current path is interrupted by turning *OFF* S_2 and S_3, the current is directed to the capacitor (*C*). If the voltage on the capacitor exceeds a threshold level, the stored fault energy is discharged by the resistor (*R*) with turning *ON* S_5 and S_6. The capacitor charge and discharge actions by the resistor are repeated until the current is driven to zero.
- Limiting topology [**Fig. 2.3(d)**]: the current can be interrupted by S_1 or S_2 depending on current direction. The freewheeling diode (D_1 or D_2) allows the fault current present in the di/dt limiting reactor to freewheel through one of the two discharge diodes, depending on current direction. The inductive energy is therefore dissipated in the circuit and the fault resistance.

2.2.4 Backup Protection

Backup protection has to be considered for the failure of the primary protection. To prevent misoperation of the backup protection, a time margin [Δt_{pb} in **Fig. 2.4(a)**] between the primary and backup protections has been used in AC networks [62]. Such a time margin can, however, make the backup protection slower and it may lead to undesired equipment failures in DC networks. In [63], a detecting algorithm for the primary protection failure is proposed and it can instantly identify the nonoperation of the primary action by observing impedance changes from the fault inception to the breaker opening

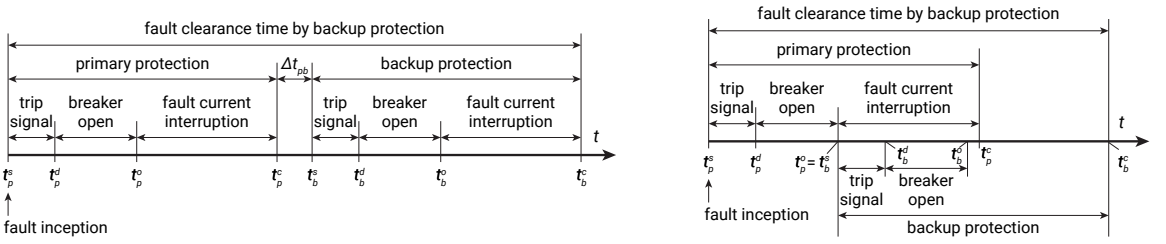


Fig. 2.4 Fault clearance time by backup protection: (a) conventional approach for AC networks [62] and (b) new approach for DC networks [63].

of the primary protection. This new approach can reduce the fault clearance time by the backup protection [**Fig. 2.4(b)**], whereas it is still needed to verify its effectiveness for various types of faults and fault resistances.

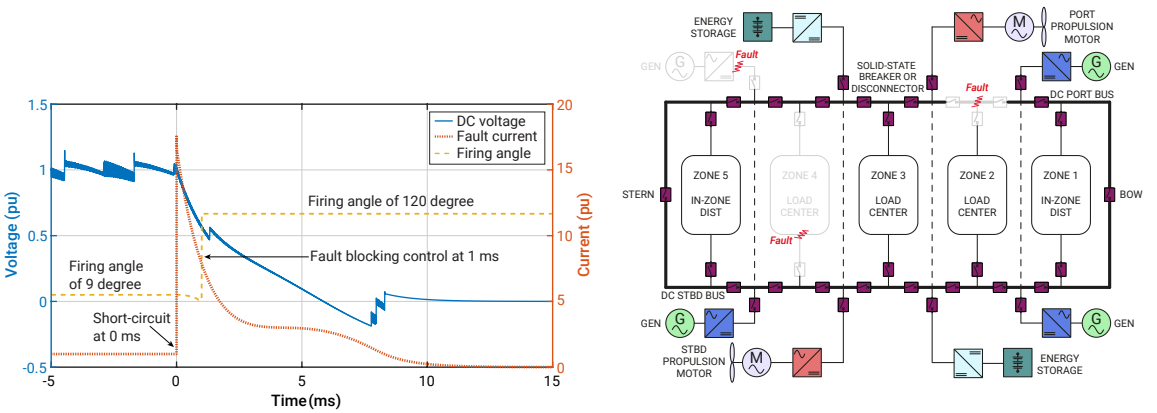
2.3 Protection Schemes

Protection schemes depend on system architectures, desired reliability requirements, system earthing, and so forth. Thus, different protection methods have been proposed and employed for different marine DC PDNs.

2.3.1 Zonal Protection

Zonal protection is a protection scheme for ring-configured military vessels that should be built with the design philosophy of high reconfigurability and survivability. In the zonal protection, there are two approaches: unit-based and breaker-based protections. Rectifiers in the unit-based protection play an important role in the fault control [65], [66]. The current contribution of the source is limited by the rectifiers with their DC fault handling capabilities, e.g., thyristor rectifier or full-bridge MMC [50], [51]. Mechanical bus-tie switches between the port and starboard buses should be normally open for this protection. If a DC fault occurs in one area, the current is blocked by the rectifiers [an example shown in **Fig. 2.5(a)**] and mechanical disconnectors isolate the fault and reconfigure the system [see **Fig. 2.5(b)**]. However, for this operation complex communication is imperative [48] and the system restoration is relatively slow due to the mechanical disconnectors.

On the other hand, the breaker-based protection allows for normally closing bus-tie switches that are based on solid-state technologies. In the breaker-based protection, the fault can be isolated with the minimum power outage [67], [68] [see **Fig. 2.5(b)**]. The main disadvantage of this approach is that it requires the installation of a large number of DC circuit breakers.



(a) (b)

Fig. 2.5 Zonal protection [64]: (a) rectifier fault blocking and (b) system reconfiguration.

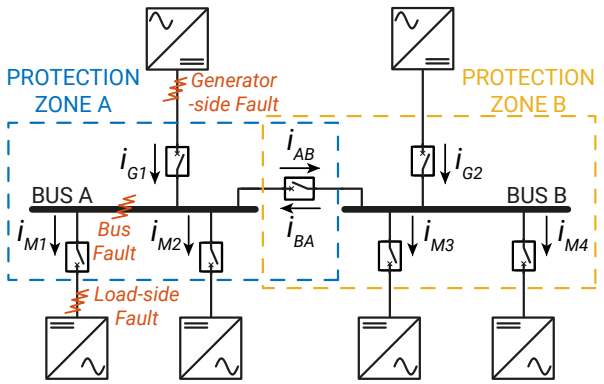


Fig. 2.6 Principle of differential and directional protections.

2.3.2 Differential and Directional Protections

Most commercial ships have been built to perform a limited number of functions as well as to minimize electrical installation and operation cost. The latter is the reason why the radial bus configuration is widely used in commercial ships. It is the simplest bus scheme and requires less installation area with the minimum numbers of circuit breakers.

For radial-configured DC PDNs, differential and directional protections combined with an intelligent electronic device (IED) and an SSCB are possible solutions for bus protection and/or other protections [69], [70]. The principle of the differential protection is based on the difference between the sums of currents flowing into and out from the protection zone. During normal states and external faults (the generator- and load-side faults in **Fig. 2.6**), their current sums are equal theoretically ($i_{G1} = i_{M1} + i_{M2} + i_{AB}$). Otherwise, for the internal fault (the bus fault in **Fig. 2.6**), all currents flow into the zone and the difference between the sums is not zero ($i_{G1} \neq i_{M1} + i_{M2} + i_{AB}$) that may be very high, indicating fault conditions.

The directional protection utilizes the comparison of all the current directions as well as current amplitudes. For the generator-side fault, the current direction of i_{G1} is negative. Assuming that the positive direction is the current flowing from upstream feeders to downstream feeders, the negative direction stands for the fault between the bus and the generator. In case of the bus fault, the current directions of the generator and load sides are positive and negative, respectively. Similar to the differential protection, the current directions and some more information (e.g., current amplitudes and bus voltages) provide enough information to detect the bus fault.

2.3.3 Three-Level Protection

As an economic solution, a three-level protection has been used for marine LVDC PDNs [26], [71], [72]. The three-level protection consists of three different actions with different operating time frames (see **Fig. 2.7**):

- fast action (first) - bus separation by bus-tie switches (up to several tens of microseconds)
- medium action (second) - feeder protection by fuses or SSCBs (up to a few milliseconds)
- slow action (third) - power supply protection (up to several seconds)

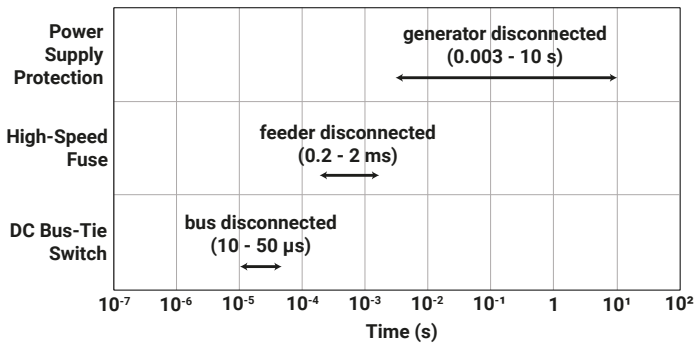


Fig. 2.7 Operating time frames of three-level protection for low impedance faults. Time discrimination in the three-level protection is coordinated with their different operating times and the time margins between the actions.

For the power supply protection, several methods are available depending on the rectifier type. In case of the diode rectifier, deexcitation of a synchronous generator, specially designed to have high subtransient reactance, is used to limit the fault current from the generator [16], [26], [49], [73]. A fold-back protection control is applied to the thyristor rectifier [50], [71], while a high-speed fuse solution is commercially employed for the VSC protection [72].

When the feeder fault occurs in **Fig. 2.8**, the DC bus-tie switch rapidly separates the DC buses. After that, the high-speed fuse on the faulty feeder isolates the fault from the system. As the last action, the power supply protection eliminates the fault contribution of the generator for the feeder protection failure or the DC bus fault. The conventional generator protection can manage AC faults.

The three-level protection does not rely on communication. Moreover, this protection generally uses the costly SSCB only for the bus-tie purpose and the economical fuse solution for the feeder protection to minimize the electrical installation cost. Hence, it can be stated that the three-level protection is simple and cost-effective. Such benefits make the three-level protection to be the dominant trend for marine LVDC PDNs selected for the main research field in the thesis [26], [71], [72].

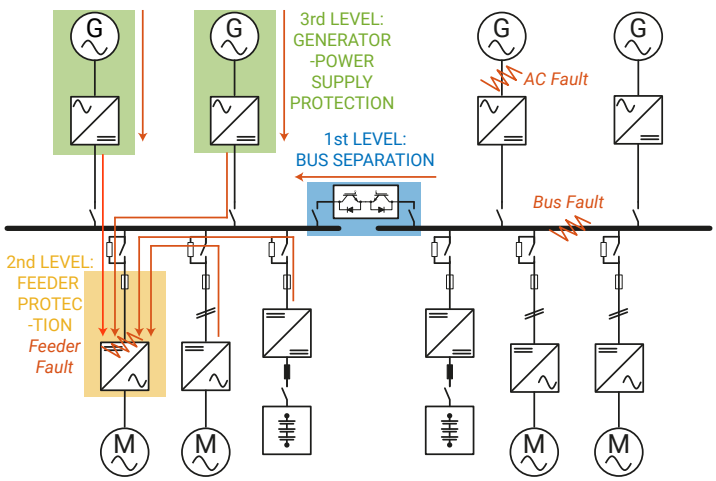


Fig. 2.8 Operational diagram of three-level protection [26].

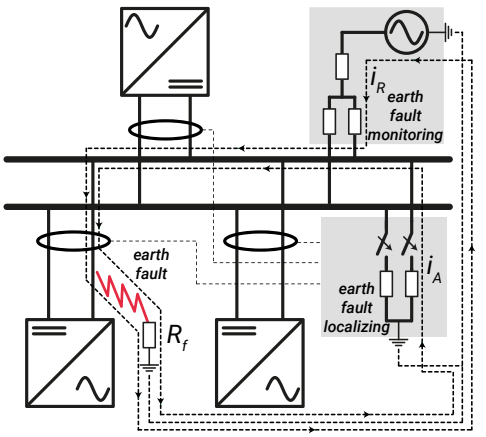


Fig. 2.9 Earth fault detection and localization.

2.3.4 Earth Fault Protection

System earthing is an important factor of system design to ensure equipment protection as well as human safety. In marine DC PDNs, a continuous power supply is a critical issue on the safety. Therefore, among several system earthing methods, the unearthed system (the IT DC system [74]) is mainly recommended for both commercial and military vessels to increase the availability of the system by preventing a power interruption from a single-pole-to-earth fault, which may be the most common type of faults [75]. The unearthed system has no current path for the single-pole-to-earth fault and it can be detected, localized, and cleared with less system impacts.

In the unearthed system, the insulation resistance between pole to earth is a good indicator to detect the earth fault [76]. The insulation resistance is very high under normal conditions ($> 1\,\mathrm{M}\Omega$). If the earth fault occurs, the resistance is decreased below a certain threshold value. The decreased resistance can be measured by analyzing returning current (i_R in **Fig. 2.9**) that is generated by the intentionally applied test voltage.

When the earth fault is detected, the fault should be cleared before the second earth fault that may give a huge impact on the system. A current tracing method can be applied to find a fault location. In this method, a high value of the resistor is connected and it generates an artificial current (i_A in **Fig. 2.9**) from the resistor to the earth fault. The fault can be localized by tracing this current flow.

2.4 Application Cases of the Three-Level Protection

This section presents a brief review of industrial marine LVDC solutions, as summarized in **Tab. 2.2**, which employ the three-level protection. Each solution is also analyzed in terms of protective philosophy, protection devices, and fault clearing time. The solutions are described with the classification of the rectifier type: diode rectifier, thyristor rectifier, and VSC.

Tab. 2.2 Marine LVDC solutions [15], [72], [77]–[79].

	Solution	Siemens BlueDrive PlusC	ABB Onboard DC Grid	Ingeteam E3-Ship	We Tech Hybrid DC Machinery	The Switch DC-Hub
Power supply	**Generator**	SG	SG	SG or PMSG	SG or PMSG	SG or PMSG
	(AC voltage)	(0.69 kV)	(N/A)	(0.69 kV)	(0.45 kV)	(N/A)
	Rectifier	Diode rectifier	Thyristor rectifier	VSC	VSC	VSC
	(DC voltage)	(0.93 kV)	(1 kV)	(1.5 kV)*	(1 kV)	(1 kV)
Protective device	**Bus separation**	Solid-state bus-tie switch				
	Feeder protection	Fuse	Fuse	Fuse	N/A	SSCB
	Power supply protection (Backup)	Deexcitation with high X_d''	Fault-blocking converter (Fuse)	Fuse	N/A	SSCB

* Note: The voltage rating of the solid-state bus-tie switch in [72].

2.4.1 Diode Rectifier-Based PDNs

A protection scheme for diode rectifier-based PDNs (see **Fig. 2.10**) in [26] is a representative three-level protection and relies on the combination of bus-tie switches, high-speed fuses, and deexcitation of a synchronous generator specially designed to have high subtransient reactance. The operating sequence of this protection is illustrated in **Fig. 2.11**. As the first level, the bus-tie switch [intelligent load controller (ILC) in **Fig. 2.11** and **Fig. 2.10**] separates two bus sections within 10 –50 μs [26]. The limiting topology shown in **Fig. 2.3(d)** is used for the ILC, presenting its figure in **Fig. 2.14(a)**.

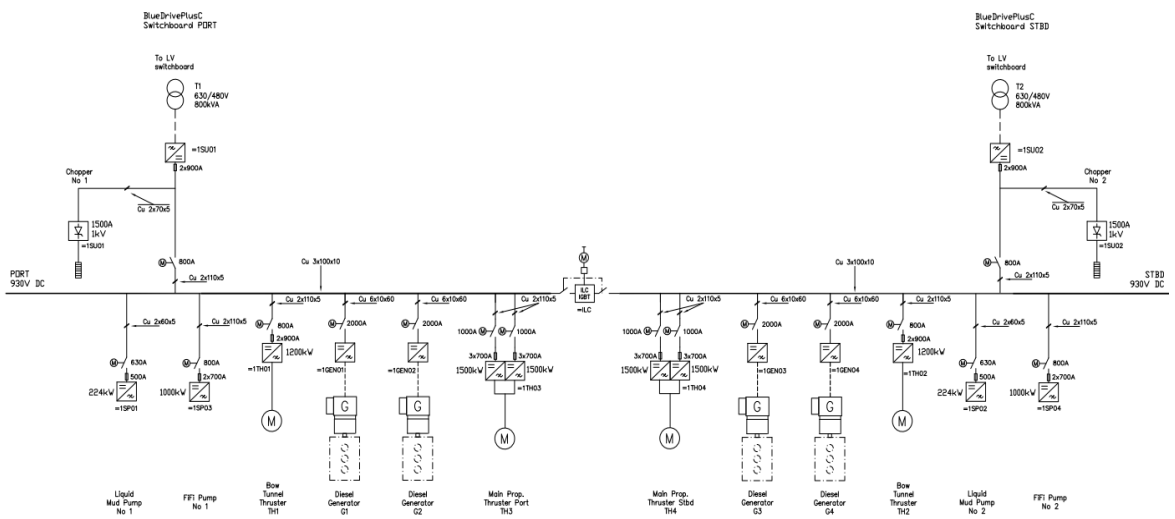


Fig. 2.10 Single line diagram of diode rectifier-based PDNs [77].

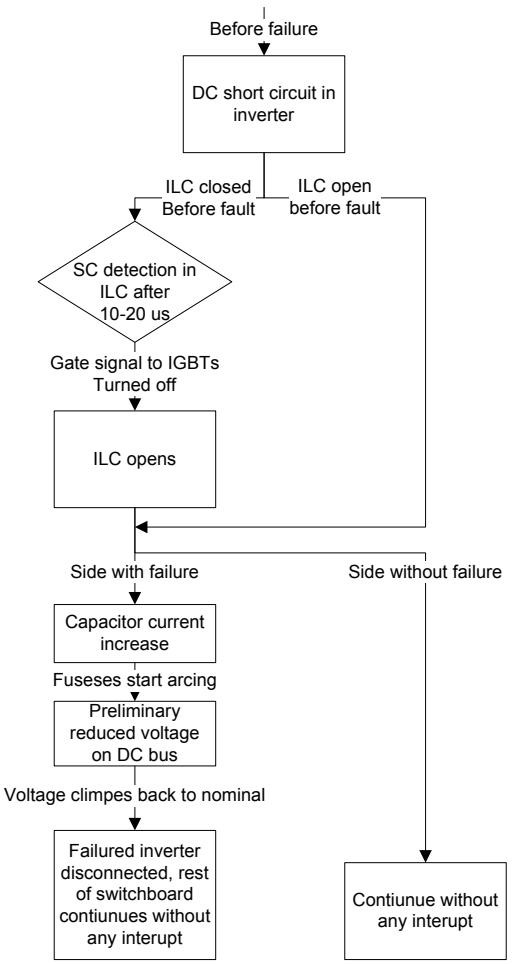


Fig. 2.11 Block diagram of protection sequence for diode rectifier-based PDNs [49].

According to [26], for the feeder protection (the second level), the fuses are dimensioned to clear any faults in its protection zone even with the minimum fault condition (sensitivity). It is also coordinated that the fuse on the faulty feeder has to clear a fault before none of the adjacent fuses starts the prearcing even with the maximum fault condition (selectivity). However, it is difficult to know how to dimension the fuse to achieve sensitivity and selectivity due to limited information.

The key technology of the power supply protection (the last action) is the deexcitation of the synchronous generator having high subtransient reactance. The fault current amplitude and energy can be controlled within the ratings of a diode rectifier by the high subtransient reactance and the deexcitation, respectively. The amplitude of DC fault current provided by the synchronous generator can be mitigated greatly by the high subtransient reactance value. A generator protection unit, on the other hand, removes the excitation with the time delay of 2.5 ms for eliminating the fault current from the generator when the overload condition is detected [16]. In case of a brushless excitation system, the flux linkage in the field winding of the synchronous generator starts to naturally discharge after the deexcitation and it results in the slow decay of the fault current through the rectifier. Contrarily, a direct (or static) excitation system has fast response characteristics.

It takes several seconds to eliminate the fault current by the deexcitation [26]. To avoid any device damages, the overloading capability of the rectifier that is a critical part in DC networks should carefully be designed to sustain the fault energy for such a long time. Additionally, this protection scheme does not consider the backup protection, i.e. the fuses on the supply side are not considered (see **Fig. 2.10**).

2.4.2 Thyristor Rectifier-Based PDNs

Fig. 2.12 shows a simplified diagram of thyristor rectifier-based PDNs [15]. A protection philosophy proposed in [15], [80] divides the PDNs into two parts: grid side (blue-colored bus) - power generation zone; and DC-link side (red-colored bus) - traditional DC-link zone for a multidrive. The rectifiers in the grid side do not equip DC-link capacitors and this makes the fault current of the grid side slow. On the other hand, fault currents in the DC-link side have very short time constants due to the presence of the DC-link capacitors.

In this approach, for the faults in any sides, the solid-state bus-tie switch (the input circuit in **Fig. 2.12**) segregates the DC-link side from the grid side at first. In case of the fault in the grid side, the input circuit disconnects the two sides and the rectifier based on thyristors manages the fault current by forcing the firing angle to around 120° [fold-back protection control [50], [71], as shown in **Fig. 2.5(a)**]. Similarly to the grid side fault, the input circuit also blocks the fault current from the grid side for the fault in the DC-link side. As the medium action, the high-speed fuse clears the fault within a few milliseconds if it is a fault event at the drive unit. For the fuse failure or the bus fault, the fold-back protection control retains the fault current from the generator at last.

While the protection in the grid side consists of the two stages due to no feeders in the zone, the three-different measures are employed to the DC-link side. Therefore, it can be stated that the protection scheme used for the thyristor rectifier-based PDNs is the extended three-level protection. The benefit of this PDNs is that the fault current can be controlled within 10-20 ms, resulting in a significant fault energy reduction [81]. In addition to the fault-blocking rectifier, high-speed fuses are installed to the upstream feeders, as the backup protection.

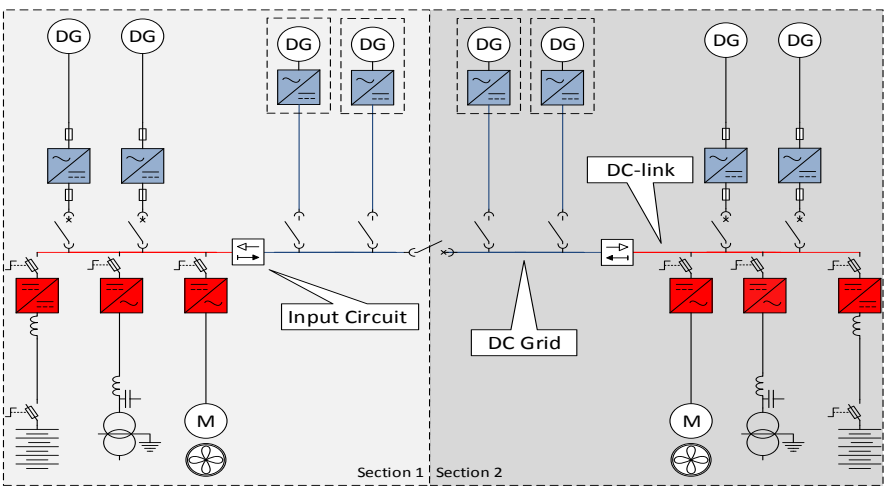


Fig. 2.12 Simplified diagram of thyristor rectifier-based PDNs [15].

2.4.3 VSC-Based PDNs

Three industrial solutions are investigated for VSC-based PDNs: Ingeteam E3-Ship in **Fig. 2.13(a)**, We Tech Hybrid DC Machinery in **Fig. 2.13(b)**, and The Switch DC-Hub in **Fig. 2.13(c)**, all utilizing the solid-state bus-tie switches for the first level protection. Apart from the bus-tie switch, the protection scheme of E3-Ship uses a combination of high-speed fuses and DC isolators. In particular, the fuses are utilized for the feeder protection as well as the power supply protection, as the primary protection.

Unlike all four solutions described in this section, The Switch DC-Hub employs solid-state DC circuit breakers at both supply and feeder sides. Hence, the combination of the bus-tie switch [electronic bus link (EBL) shown in **Fig. 2.14(c)**] and the DC circuit breakers ensures much faster fault clearing compared to the other solutions. Note that the protection scheme of We Tech Hybrid DC Machinery is not presented because of the lack of published information.

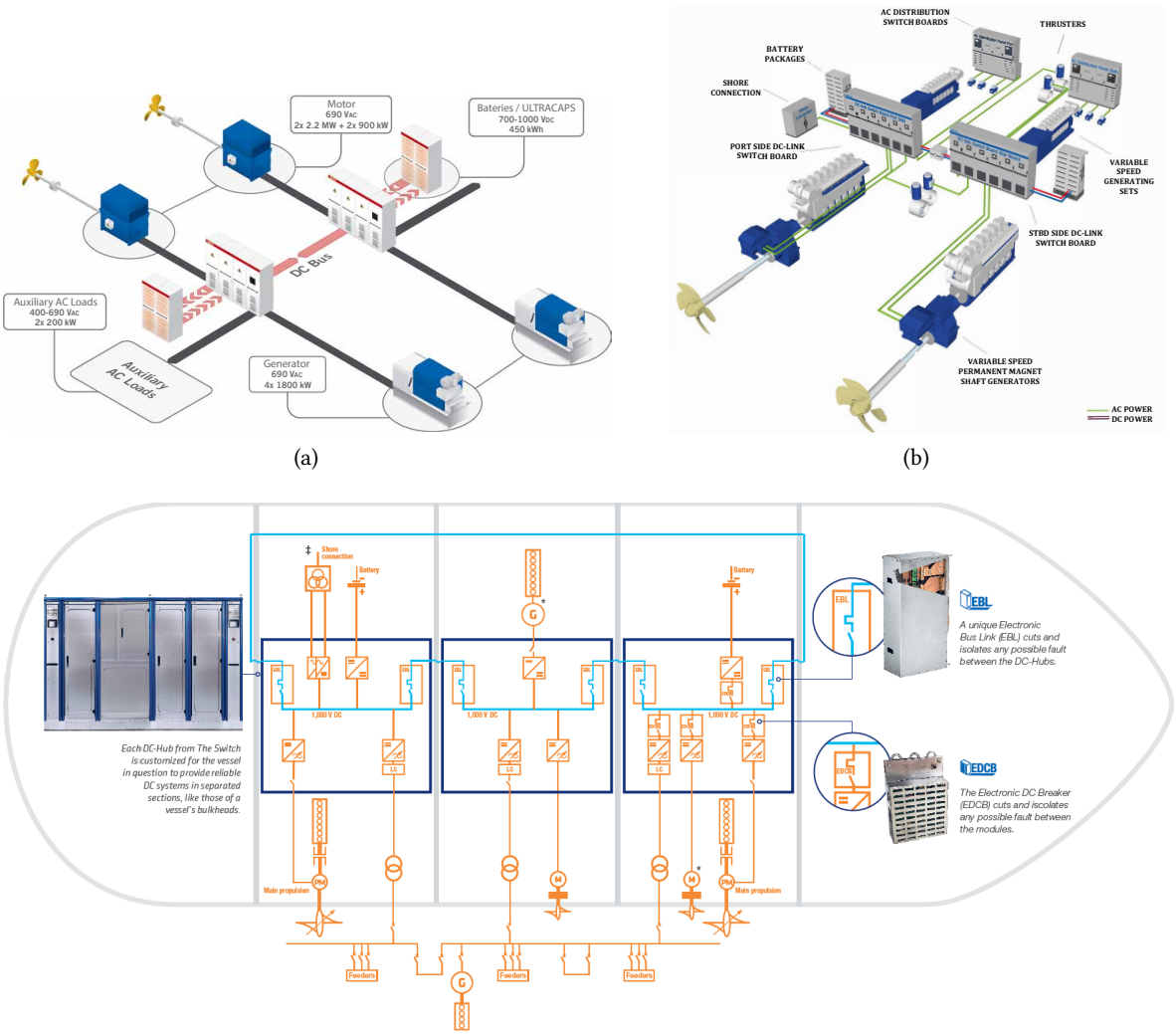


Fig. 2.13 Industrial solutions based on VSC-based PDNs: (a) Ingeteam E3-Ship [72], (b) We Tech Hybrid DC Machinery [78], and (c) The Switch DC-Hub [79].

(a) (b) (c)

Fig. 2.14 Solid-state bus-tie switches: (a) Siemens ILC [26], (b) Astrol DC breaker [82], and (c) The Switch EBL [83].

2.4.4 Summary

This chapter has provided a critical review of general protection technologies in DC PDNs as well as the state-of-the-art protection schemes in marine DC PDNs. Marine LVDC PDNs which are the target systems of the thesis have commonly utilized the solid-state bus-tie switches for the bus separation. The high-speed fuse has generally accepted to be a major protective device to protect inverters, while The Switch solution uses solid-state DC switches at every inverter feeder. The power supply protection has big differences among the analyzed solutions. From these analyses, it could be concluded that the three-level protection is becoming the dominant protection scheme in marine LVDC PDNs.

On the other point, most of the works for marine LVDC PDNs have been conducted by industrial manufacturers. They have published limited information on their solution due to the technology confidentiality. Thus, this thesis focuses on not only integrated technical discussions on different protection methods employed by each solution but also technology gaps that are not covered by previous works for marine LVDC PDNs.

3

Extending Selectivity for Feeder Protection Utilizing Additional Bus Capacitance

This chapter presents the feeder protection by high-speed fuses. The additional bus capacitance method, which can supply the additional energy only to the fuse on the faulty feeder during a fault event, is proposed to ensure the fault interruption by a reliable fuse operation with the consideration of selectivity and sensitivity. The performance of the proposed method is verified by extensive simulation studies under various conditions.

3.1 Introduction

From the practical point of view, a fuse has notable disadvantages: manual replacement of the fuse if it blows and low reliability in protection compared with an AC circuit breaker controlled by a protective relay. In other words, these are the reasons why the combination of the AC circuit breaker and the protective relay is commonly used in marine AC PDNs. Nevertheless, considering that fast DC breaker technology is not yet readily available and various vendors have already offered marine DC solutions on the market, high-speed fuses (semiconductor fuses) have been used for the feeder protection in commercial low-voltage direct-current (LVDC) vessels, as presented in **Chap. 2**.

The other thing that should be considered is the current flow for a feeder fault. In AC PDNs, the fault current is generally provided by the source to the fault, i.e., the current generally flows from the

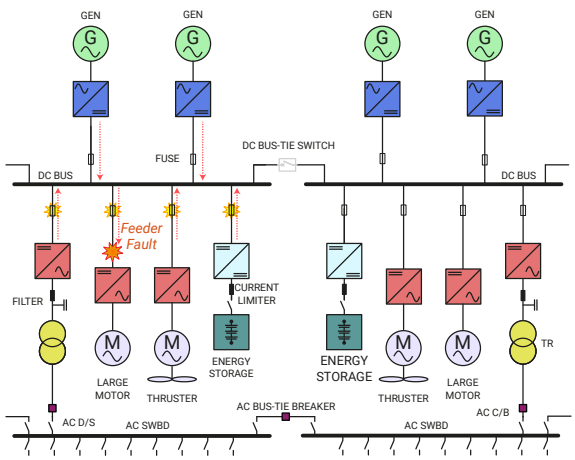


Fig. 3.1 Fault current flows and selectivity issue between feeder fuses in DC PDNs.

upstream side to the downstream side. In this fault condition, the selectivity between the upstream and downstream feeders can be achieved by selecting a higher threshold value for the upstream feeder than that for the downstream feeder. If the capacitor banks are installed at one of the downstream feeders in AC PDNs, resulting in the current flow from the capacitor feeder to the faulty feeder, directional overcurrent protection (ANSI/IEEE Protective Device No. 67) can be applied to the feeder relays [84] or the capacitor banks with a symmetrical double-wye configuration can be used for the unbalanced protection purpose [85].

Unlike AC PDNs, each downstream feeder in DC PDNs normally includes a DC-link capacitor in a converter and it rapidly provides the extra current to the fault (see **Fig. 3.1**). Furthermore, the directional protection is unavailable with the passive fuse solution. Thus, to maintain the maximum continuity of service with the minimum system impact, the protection in DC PDNs should be coordinated to achieve the selectivity between upstream and downstream feeders as well as between adjacent feeders. Note that the term 'selectivity' is used to describe the coordination between adjacent feeders in this chapter. Also, this complies with the definition in [86] as "*coordination between the operating characteristics of two or more overcurrent protection devices, so that when an overcurrent within established limits occurs, the device destined to operate within those limits trips whereas the others do not trip*". Furthermore, the fault has to be properly interrupted not only under the maximum fault condition but also under the minimum fault condition while remaining closed under the maximum load condition. This sensitivity issue is studied in the chapter, as the term of 'sensitivity'.

Works of [16], [26], and [73] present the study results of the selectivity and the sensitivity for the feeder protection by high-speed fuses in marine DC PDNs. However, those do not provide the principle for achieving the selectivity and the sensitivity and there is lack of information on the fuse operation for different system configurations and fault conditions. A work of [87] only mentions the necessity of additional capacitor banks to clear a fault with the extra fault energy if necessary. The work does not cover the technical discussions regarding the additional capacitor banks such as operational principle, physical implementation, sizing, and effects. This chapter, therefore, presents comprehensive system studies on the feeder protection. Furthermore, the additional bus capacitance (ABC) method, which can supply the additional energy only to the fuse on the faulty feeder during a fault event, is proposed to ensure the fault interruption by a reliable fuse operation with thorough technical discussions required to implement. The performance of the ABC method is verified by extensive simulation studies under various conditions.

3.2 Study Considerations

This section describes equivalent circuits for marine LVDC PDNs to perform the study on selectivity and sensitivity. System parameters and conditions used for the study are also presented with the discussion on DC short-circuit faults.

3.2.1 DC PDN Modeling

There are two configurations to implement marine LVDC PDNs: a centralized configuration (or a multidrive approach) and a distributed configuration (or a fully distributed system) [71], [88]. The main difference comes from ways to connect different equipment, e.g., generator-rectifier, rectifier-DC

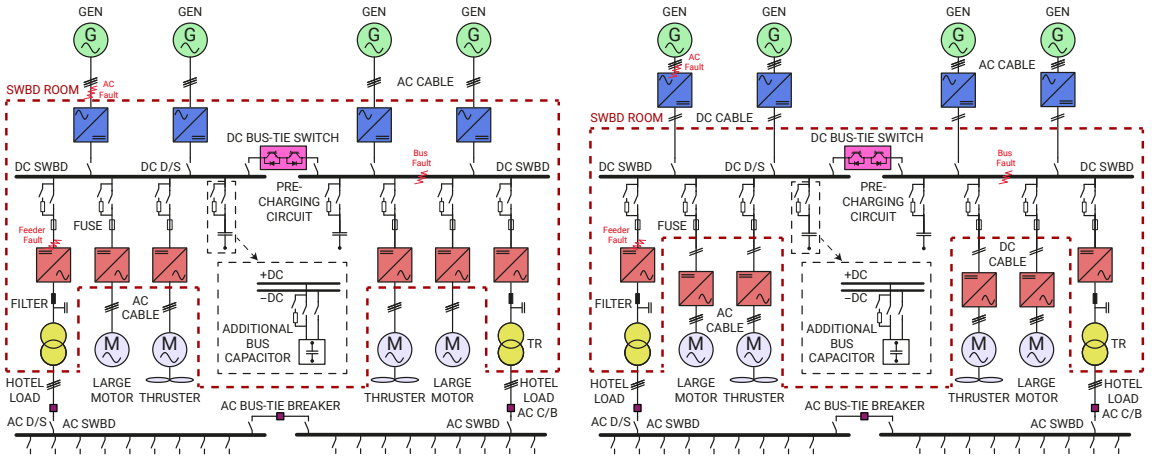


Fig. 3.2 Schematic diagrams of marine LVDC PDNs: (a) centralized configuration and (b) distributed configuration. The proposed ABC is installed between the positive and negative poles of the DC bus.

bus, DC bus-inverter, and inverter-load. The centralized configuration uses AC cables to connect generator-rectifier and inverter-load. All DC parts, e.g., rectifiers, inverters, isolators, and bus-tie switches, are connected to the DC bus through metallic busbars in the cabinet, as illustrated in **Fig. 3.2(a)**. On the other hand, the use of DC cables is necessary to integrate the converters to the DC bus in the distributed configuration. The distributed approach allows for installing power converters next to machines and can achieve high energy efficiency by using DC cables that have lower power losses than AC cables [see **Fig. 3.2(b)**].

Due to the fast discharging characteristics, DC-link capacitors that are applied to power converters mainly contribute to an initial transient current during a DC fault event [89], [90]. In particular, the fault current contribution of the AC generator is much lower than that of the DC-link capacitors and can be neglected in the 1 ms time range for the feeder protection [see **Fig. 3.4(c)**]. By neglecting the

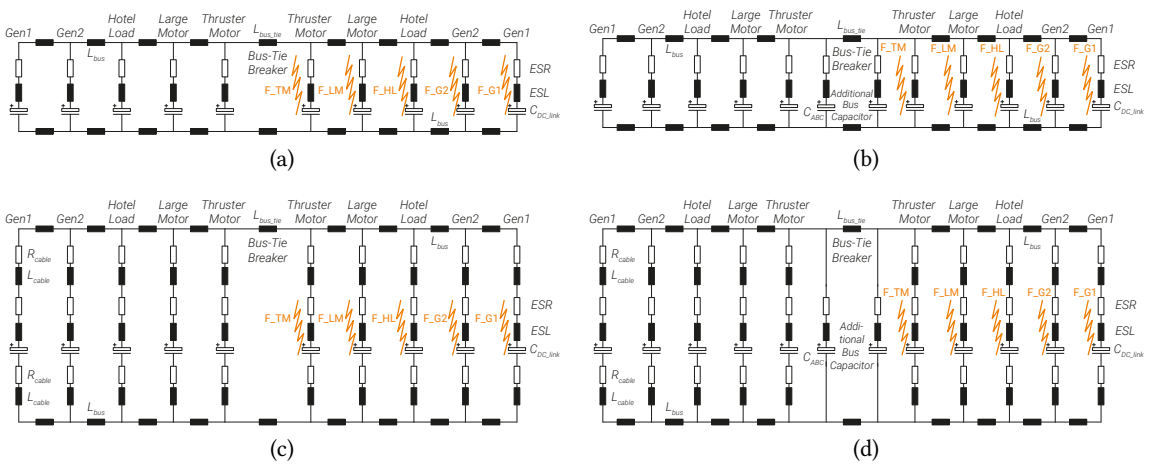


Fig. 3.3 Equivalent circuits for DC PDNs: (a) centralized configuration without ABC (T_1), (b) centralized configuration with ABC (T_2), (c) distributed configuration without ABC (T_3), and (d) distributed configuration with ABC (T_4).

Tab. 3.1 Electric load matrix of ship operating modes.

Electric Load		Operating Mode		
		OM1	***OM2***	***OM3***
Bus1	Gen1 (*G1*)	✓[a]		
	Gen2 (*G2*)	✓	✓	✓
	Hotel Load (*HL*)	✓	✓	✓
	Large Motor (*LM*)[b]	✓		✓
	Thruster Motor (*TM*)	✓	✓	
Bus2	Thruster Motor (*TM*)	✓	✓	
	Large Motor (*LM*)	✓		✓
	Hotel Load (*HL*)	✓	✓	✓
	Gen2 (*G2*)	✓	✓	
	Gen1 (*G1*)	✓		

[a] In service.

[b] Cargo pumps, ballast pumps, and VOC compressors are grouped in a large motor.

current from the generator, the centralized PDNs for the DC short-circuit fault can be modeled as RLC circuits connected via busbar inductance, as depicted in **Fig. 3.3(a)** [without the ABC (*T1*)] and **Fig. 3.3(b)** [with the ABC (*T2*)] [49]. In the case of the distributed PDNs, the resistance (R_{cable}) and inductance (L_{cable}) of the DC cable play an important role in the initial fault current and its rate of change. The equivalent circuits for the distributed PDNs, therefore, include these cable parameters, as illustrated in **Fig. 3.3(c)** [without the ABC (*T3*)] and **Fig. 3.3(d)** [with the ABC (*T4*)]. The capacitance of the DC cable is neglected because its capacitance value is much smaller than that of the DC-link capacitor.

Equivalent series resistance (ESR) and equivalent series inductance (ESL) in **Fig. 3.3** are the equivalent series resistance and inductance of the capacitor, respectively. The four equivalent circuits are implemented by use of electromagnetic transient program – restructured version (EMTP-RV). Note that the DC PDNs considered are classified into four categories: *T1*, *T2*, *T3*, and *T4*.

3.2.2 System Parameters and Conditions

A shuttle tanker, which is a ship to transport oil from an off-shore oil field and is one of the representative dynamic positioning (DP) vessels, is considered for the study. Three considered operating modes of the shuttle tanker are presented with electric load matrix in **Tab. 3.1**. A DP mode (*OM1*, the maximum load condition) is turned *ON* when the shuttle tanker should be manoeuvred accurately. In *OM1*, the maximum number of generators and several high-power motors with hotel loads have to be operated, e.g., thruster motors for the DP operation, cargo pumps for the crude oil transfer, ballast pumps for the ship balance, and volatile organic compound (VOC) compressors for the return of VOC emission gases. During a port in/out mode (*OM2*, the medium load condition), thruster motors with hotel loads are in service to improve the manoeuvrability when the shuttle tanker approaches and leaves a port. For a sailing mode (*OM3*, the minimum load condition), the mechanical power from main engines is used for the propulsion and a small number of large motors (such as ballast pumps) with hotel loads are in service.

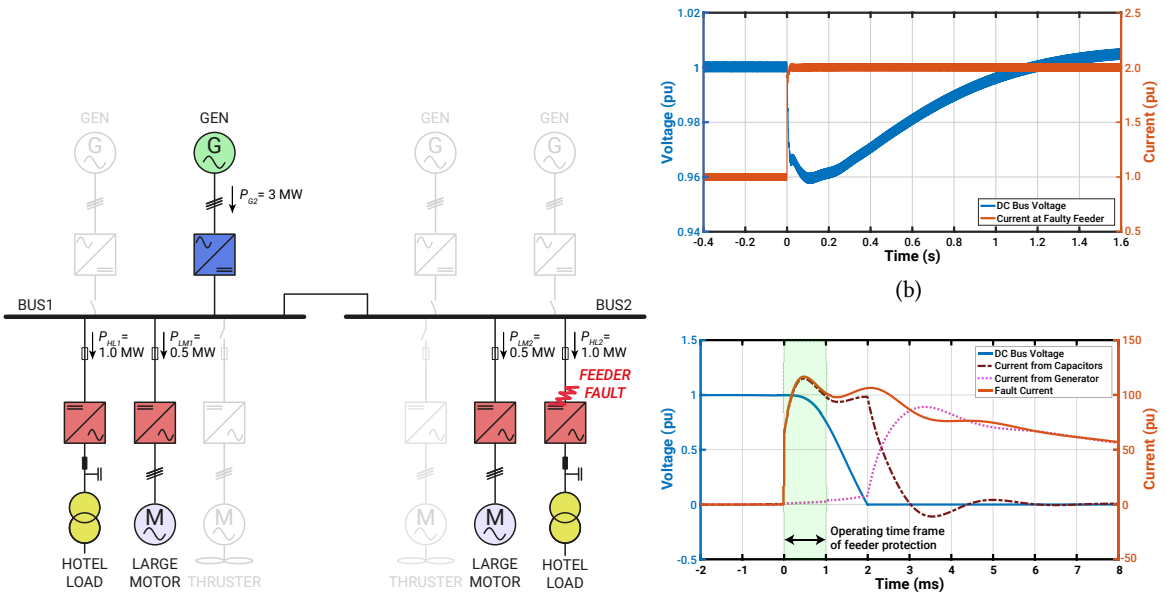


Fig. 3.4 DC short-circuit faults: (a) ship configuration and power flow before the fault under *OM3* in **Tab. 3.1**, (b) high-impedance fault (R_f = **1** Ω), and (c) low-impedance fault (R_f = **1** mΩ). **1 kV = 1.0 pu** and **1 kA = 1.0 pu** are used.

If a high-impedance DC short-circuit fault occurs, it may draw low current and develop low voltage drop, as shown in **Fig. 3.4(b)**. Such a fault gives insignificant system impact and can be removed by the fuse with delayed operation or managed by ship monitoring and supervision systems. On the other hand, a low-impedance DC short-circuit fault causes a high voltage drop and fault current

Tab. 3.2 System parameters used for the study.

Parameters	Values	Parameters	Values	Parameters	Values
V_{DC}	$1kV$	C_{G1}, C_{G2}	$80mF$	I^2t_{pf1} [d]	$1.1 \cdot 10^6 A^2s$
L_{bus} [a]	$1\mu H$	C_{HL}	$20mF$	I^2t_{tf1} [d]	$5.4 \cdot 10^6 A^2s$
L_{bus_tie}	$1\mu H$	C_{LM}, C_{TM}	$60mF$	I^2t_{pf2} [e]	$1.7 \cdot 10^6 A^2s$
R_{cable} [b]	$60.7 m\Omega/km$	ESR [c]	$58m\Omega$	I^2t_{tf2} [e]	$8.5 \cdot 10^6 A^2s$
L_{cable} [b]	$0.284mH/km$	ESL [c]	$20nH$	R_f	$1m\Omega$
l_{cable}	$25m$				

[a] Data for a metallic busbar with **1** μH/**m** [91] and **1 m** length.

[b] Data for a single core cable with **1 kV** and **631** A [92].
Several cables in parallel are used depending on current rating.

[c] Data for two capacitors with **0.5 kV** and **10 mF** [93] in series (capacitance for **1 kV** and **5 mF**).
Several capacitors in parallel are used depending on capacitor rating.

[d] Data for four fuses (170M1833 in [94]) in parallel.

[e] Data for five fuses (170M1833 in [94]) in parallel.

(significant system impact), as provided in **Fig. 3.4(c)**. Therefore, the low-impedance fault has to be cleared as quickly as possible and its management is a challenging issue. For this reason, the low-impedance DC fault (e.g., R_f = 1 mΩ in **Tab. 3.2**) is considered in the study.

The system parameters used in the study are provided in **Tab. 3.2**, where I^2t_{pf1} and I^2t_{tf1} are the prearcing and total clearing I^2t ratings of fuse 1 selected for the protection of the *LM* and *TM* feeders in the distributed PDNs (*T3* and *T4*). I^2t_{pf2} and I^2t_{tf2} are those of fuse 2 selected for the protection of the *LM* and *TM* feeders in the centralized PDNs (*T1* and *T2*). The bus-tie switch inductance (L_{bus_tie}) and the DC cable length (l_{cable}) are assumed to be 1 μH and 25 m, respectively. The fault resistance (R_f) is assumed as 1 mΩ in the study as its exact modeling including nonlinear characteristics is out of the scope. The selection of an ABC value (C_{ABC}) is discussed hereafter.

3.3 Proposed ABC Method

This section discusses the technical issues in the bus separation failure and the feeder protection. As a solution for the issues, the ABC method is introduced and its operational principle is presented. The sizing of the ABC method is additionally carried out for the centralized and distributed PDNs, considering the iterative process addressed in the study.

3.3.1 Effect of ABC Method on Bus Separation Failure

When the feeder fault occurs, the fault current reaches the threshold value of the DC bus-tie switch operation, which is based on solid-state technology to achieve ultra-fast disconnection. The switch rapidly interrupts the fault current within several tens of microseconds [26], [49]. However, if the switch fails to interrupt, all loads in the healthy bus unintentionally suffer a huge voltage drop and may be disconnected due to their own undervoltage protection. Thus, the minimum remaining voltage at the healthy bus has to be higher than any undervoltage trip conditions of the converters during the fault clearing time of the feeder protection (1 ms). With a simple equivalent circuit depicted in **Fig. 3.5**, a sensitivity analysis is carried out to investigate the role of system inductance and capacitance in a voltage drop of the healthy bus.

The DC-link capacitor in **Fig. 3.5** contributes to an initial current of the DC fault. A series RLC circuit, therefore, represents an equivalent circuit of the DC fault in the initial phase of the fault (see **Fig. 3.5**).

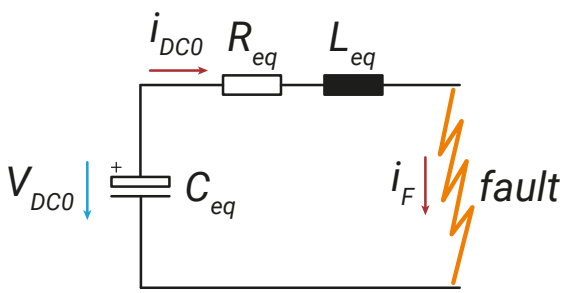


Fig. 3.5 Equivalent circuit for initial DC fault. The voltage of the DC capacitor (V_{DC0}) and the current (i_{DC0}) are the initial conditions for the DC fault current (i_F).

The analytical expression for the DC fault current under the underdamped condition is (see **App. A**)

$$i_F(t) = \underbrace{Ae^{-\alpha t}\sin\omega_d t}_{\text{first term}} + \underbrace{Be^{-\alpha t}\sin\left(\omega_d t + \beta\right)}_{\text{second term}} \tag{3.1}$$

where

$$\alpha = \frac{R_{eq}}{L_{eq}},\ \omega_0 = \frac{1}{\sqrt{L_{eq}C_{eq}}},\ \omega_d = \sqrt{\omega_0^2 - \alpha^2},\ \beta = \arctan\left(\frac{\omega_d}{\alpha}\right),\ A = \frac{\omega_d V_{DC0}}{L_{eq}},\ \text{and}\ B = \frac{\omega_0 i_{DC0}}{\omega_d}.$$

With the assumption of $i_{DC0} = 0$ (the first term is strongly dominant in current amplitude.) and $V_{DC0} = 1kV$ (the rated DC voltage) in (3.1), the remaining voltage of the capacitor can be calculated in per unit (pu) by [95]

$$\frac{\Delta V}{V_{DC0}} \approx e^{-\alpha t}\cos\omega_d t \tag{3.2}$$

Fig. 3.6 shows the sensitivity analysis on the remaining voltage of the DC capacitor depending on the values of the capacitor and the inductor by using (3.2). Note that $R_{eq} = 1m\Omega$ (the equivalent resistance, e.g., line resistance, fault resistance, and parasitic resistance) and $t = 1ms$ (the fault clearing time of the feeder protection) are used for the analysis.

It is seen that the voltage drop can be mitigated with inductance of several tens of μH. On another point of note, capacitance with several tens of mF can also reduce the voltage drop. Therefore, there are two ways to control the voltage drop level: 1) installing additional inductance between the healthy bus and the faulty bus; and 2) installing the additional capacitance between the healthy bus and the faulty bus (the proposed ABC method).

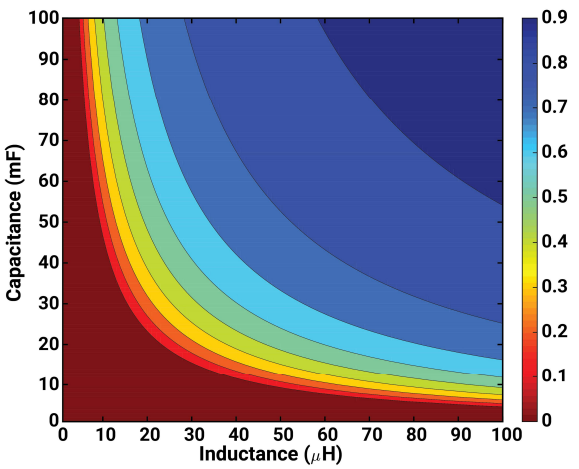


Fig. 3.6 Sensitivity analysis on remaining voltage of DC capacitor. High remaining voltage of the DC capacitor implies its low voltage drop.

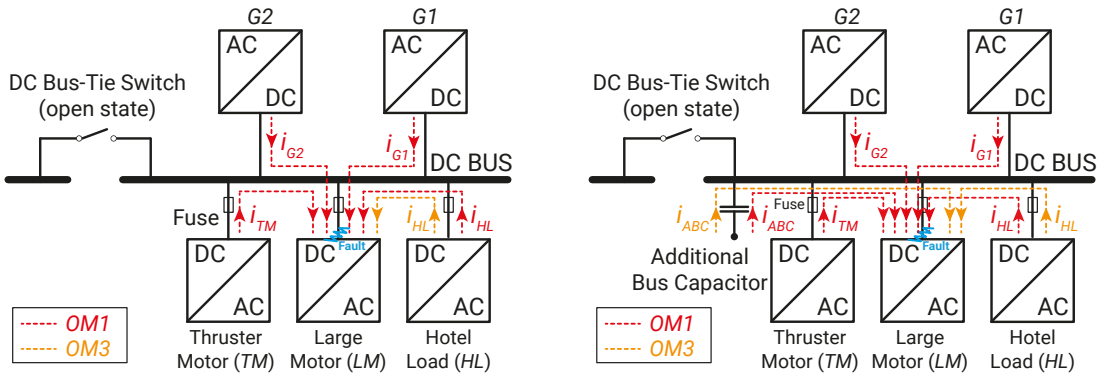


Fig. 3.7 Fault current flows depending on ship operating mode: (a) without the ABC and (b) with the ABC. The two ship operating modes in **Tab. 3.1** are represented: *OM1* (red-dotted line) and *OM3* (orange-dotted line).

With regard to system stability, while high system inductance might cause an instability issue depending on system conditions and converter types, high system capacitance supports the system stability [96]. Therefore, for the bus separation failure, the ABC method is a suitable solution to mitigate the impact on the voltage drop at the healthy bus and to make the system more stable, compared with adding more inductance.

3.3.2 Effect of ABC Method on Feeder Protection

In marine DC PDNs, each DC-link capacitor installed in a converter is the main energy source to blow the fuse for the feeder protection and its value is related to the fault clearing time. Generally, higher capacitance allows for faster fault clearing. Otherwise, the fuse on the faulty feeder is melted by the energy provided by the external capacitance installed at other feeders. In order to achieve the selectivity, the fuse on the faulty feeder has to clear the fault without the prearcing of the fuses on other feeders. For example, the fuse on the *LM* feeder in **Fig. 3.7(a)** (the faulty feeder) has to totally clear the fault without the prearcing of other fuses (the fuses on the thruster motor and the hotel load) [97].

On the other hand, the fuse on the faulty feeder has to clear the faults under the maximum fault condition as well as the minimum fault condition, termed sensitivity in the study. For example, the fuse on the *LM* feeder in **Fig. 3.7(a)** (the faulty feeder) has to be blown by the maximum fault current ($i_{G1} + i_{G2} + i_{TM} + i_{HL}$) under *OM1* and by the minimum fault current (i_{HL}) under *OM3*.

The feeder protection with the high-speed fuse has to comply with these technical aspects, the selectivity and the sensitivity. For the study conditions considered, the selectivity between the fuse on the *LM* feeder (faulty feeder) and the fuse on the *TM* feeder (healthy feeder and having the same fuse and current ratings with the *LM* feeder in **Tab. 3.2**) cannot be guaranteed without the selectivity analysis [see **Fig. 3.7(a)**]. Furthermore, the sensitivity under *OM1* and *OM3* may not be achieved for the *LM* feeder fault since the fault energy from the capacitor at the *HL* feeder may be insufficient to blow the fuse on the *LM* feeder.

To extend the selectivity and the sensitivity, the ABC method is proposed, as illustrated in **Fig. 3.7(b)**. The ABC method directly provides an additional fault current (i_{ABC}) to the fuse on the faulty feeder

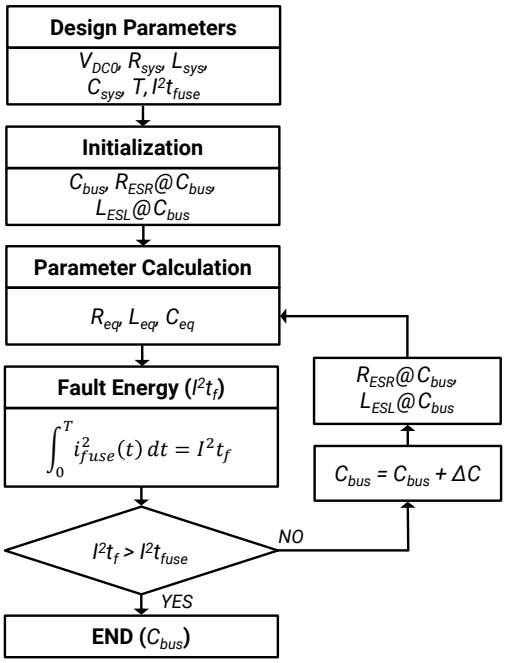


Fig. 3.8 Flowchart representing the iterative process for sizing of ABC value.

for any fault conditions (including *OM1* and *OM3*). The additional energy can significantly assist in melting the fuse in a shorter time than the case without the ABC. With this principle, the proposed method can extend the selectivity and the sensitivity if DC PDNs employ the ABC method that includes high-enough energy to blow the fuse.

3.3.3 Sizing of ABC

As discussed earlier, the voltage drop of the DC bus, which is related to the bus separation failure, is the function of the system capacitance and inductance values. Between these system parameters, the system capacitance is the dominant factor to determine the fault clearing time for the feeder protection. Hence, the sizing of the ABC is based on the consideration of the feeder protection and the selection process addressed is shown in **Fig. 3.8**.

To control the fault clearing time with the ABC method, the fault energy passing through the fuse on a faulty feeder can be calculated by

$$\int_0^T i_{fuse}^2(t)dt = I^2t_f > \text{Total clearing } I^2t \text{ of fuse} \tag{3.3}$$

where i_{fuse} is the fault current passing through the fuse.

Using (3.1), (3.3) can be expressed as

$$I^2t_f = \left[e^{-2\alpha t}\left(\frac{A}{2}\right)^2\left(\frac{\alpha\cos 2\omega_d t - \omega_d \sin 2\omega_d t}{\alpha^2 + \omega_d^2} - \frac{1}{\alpha}\right)\right]_0^T \tag{3.4}$$

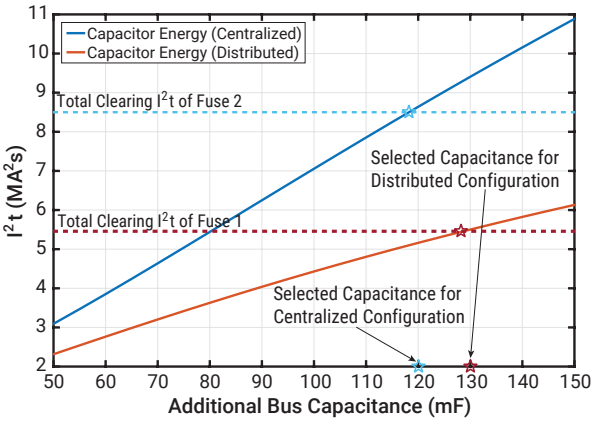


Fig. 3.9 Result of ABC sizing for centralized and distributed configurations.

In (3.4), the expansion of the equation in a variable C_{eq} is impossible since (3.4) is an implicit equation. An iterative method with the process in **Fig. 3.8** is, therefore, used to find the value for the ABC. First, the design parameters are needed to start the calculation such as initial DC voltage (V_{DC0}), system resistance (R_{sys}), system inductance (L_{sys}), system capacitance (C_{sys}), target fault clearing time (T), and total clearing I^2t rating of fuse (I^2t_{fuse}). In the initialization step, equivalent series resistance (R_{ESR}) and inductance (L_{ESL}) are calculated at the base of an initial capacitor value for the ABC method. Higher values of the ABC make lower values of R_{ESR} and L_{ESL} due to the capacitor connection in parallel. With these parameters, the equivalent values (R_{eq}, L_{eq}, and C_{eq}) are calculated to determine the integrated fault energy I^2t_f during T by (3.4). If the fault energy is less than I^2t_{fuse}, the higher ABC value should be considered than that of the previous iteration step and the parameters for the capacitor should be calculated at the base of the updated ABC value. When I^2t_f is greater than I^2t_{fuse}, the process for the ABC sizing is completed with the result of the required ABC value.

With $T = 1ms$ (the operating time of the feeder protection) and the system parameters in **Tab. 3.2** under *OM3* in **Tab. 3.1** (the minimum fault condition considered to ensure the sensitivity), the required ABC values are determined by the process and the results are shown in **Fig. 3.9**. The ABC values with 120 mF and 130 mF, which are slightly higher than the minimum required values, are finally selected to enable the capacitor combination for centralized and distributed PDNs, respectively. Different fuses are used due to the presence of the DC cables in the distributed PDNs. Fuse 2 and fuse 1 are used for the centralized and distributed PDNs, respectively (see **Tab. 3.2**).

3.4 Verification

For the bus separation failure, the voltage drop of the healthy bus is calculated under different configurations, fault conditions, and operating modes. The fault clearing time is also analyzed under the maximum and minimum fault conditions for the feeder protection. The effectiveness of the proposed method is investigated from these studies.

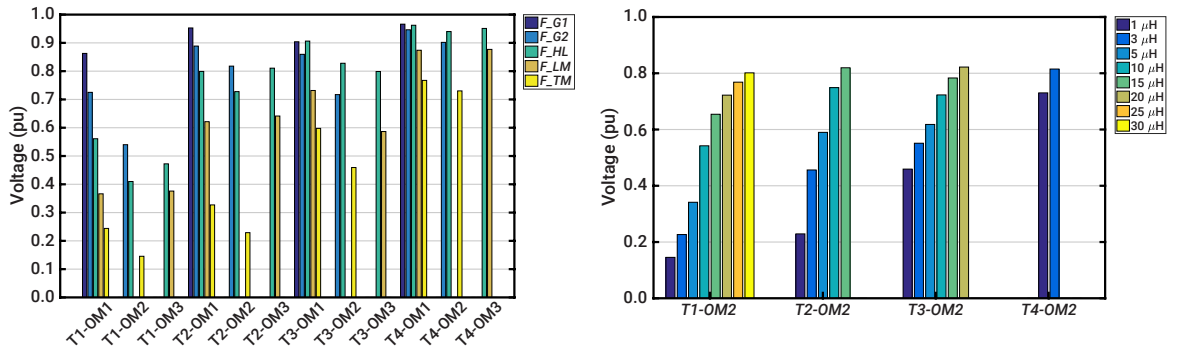


Fig. 3.10 Analysis of voltage drop for bus separation failure: (a) remaining voltage of healthy bus at 1 ms after fault depending on configurations, operating modes, and fault locations and (b) required inductance value to remain healthy bus voltage of 0.8 pu.

3.4.1 Bus Separation Failure

Fig. 3.10 depicts the voltage drop analyses under the five feeder faults (see **Fig. 3.3**) and the three operating modes (see **Tab. 3.1**) for the four configurations. It is observed that, due to absence of the DC cable, the centralized PDNs without the ABC (*T1*) and with the ABC (*T2*) have higher voltage drops than the distributed PDNs without the ABC (*T3*) and with the ABC (*T4*) for all the studied cases. When the ABC method is employed with 120 mF for *T2* and 130 mF for *T4*, the voltage drops for *T2* and *T4* are clearly reduced, compared with those of *T1* and *T3*.

While a certain amount of the system inductance, mostly in the DC busbar for the centralized configuration and in the DC cable and the DC busbar for the distributed configuration, is presented in the system, the extra system inductance is also necessary to control the voltage drop level at the healthy side, as presented in **Fig. 3.6**. Among the study cases in **Fig. 3.10(a)**, the fault at the *TM* feeder (*F_TM*) under *OM2* is chosen to conduct the worst case study in terms of the voltage drop. The result shows that, to remain the voltage of 0.8 pu at 1 ms after the fault, the system inductance values of 30 μH and 20 μH are needed for *T1* and *T3*, respectively. By installing the ABC, the required inductance values can be minimized as 20 μH for *T2* and 3 μH for *T4* [see **Fig. 3.10(b)**]. The study assumes the voltage level of 0.8 pu for the undervoltage trip condition of converters.

For the bus separation failure, the results under the studied condition are summarized:

- The distributed configuration has an advantage considering lower voltage drops.
- The ABC method helps to mitigate the voltage drop for both the configurations (benefit for the bus separation failure).
- The ABC method can reduce the required system inductance value for both the configurations (benefit for the system stability [96]).

3.4.2 Feeder Protection

After the bus separation by the bus-tie switch, each capacitor in a healthy feeder provides the energy to blow the fuse corresponding to the faulty feeder (see **Fig. 3.7**). With this capacitor discharging energy, the fuse on the faulty feeder has to clear the fault not only without the operation of the fuses on other healthy feeders (the selectivity), but also under the maximum and minimum fault conditions (the sensitivity). Selectivity and sensitivity analyses are conducted for the fault at the thruster motor under *OM1* and *OM3* for *T1*, *T2*, *T3*, and *T4* to verify the ABC method (see **Fig. 3.12**). **Fig. 3.11**

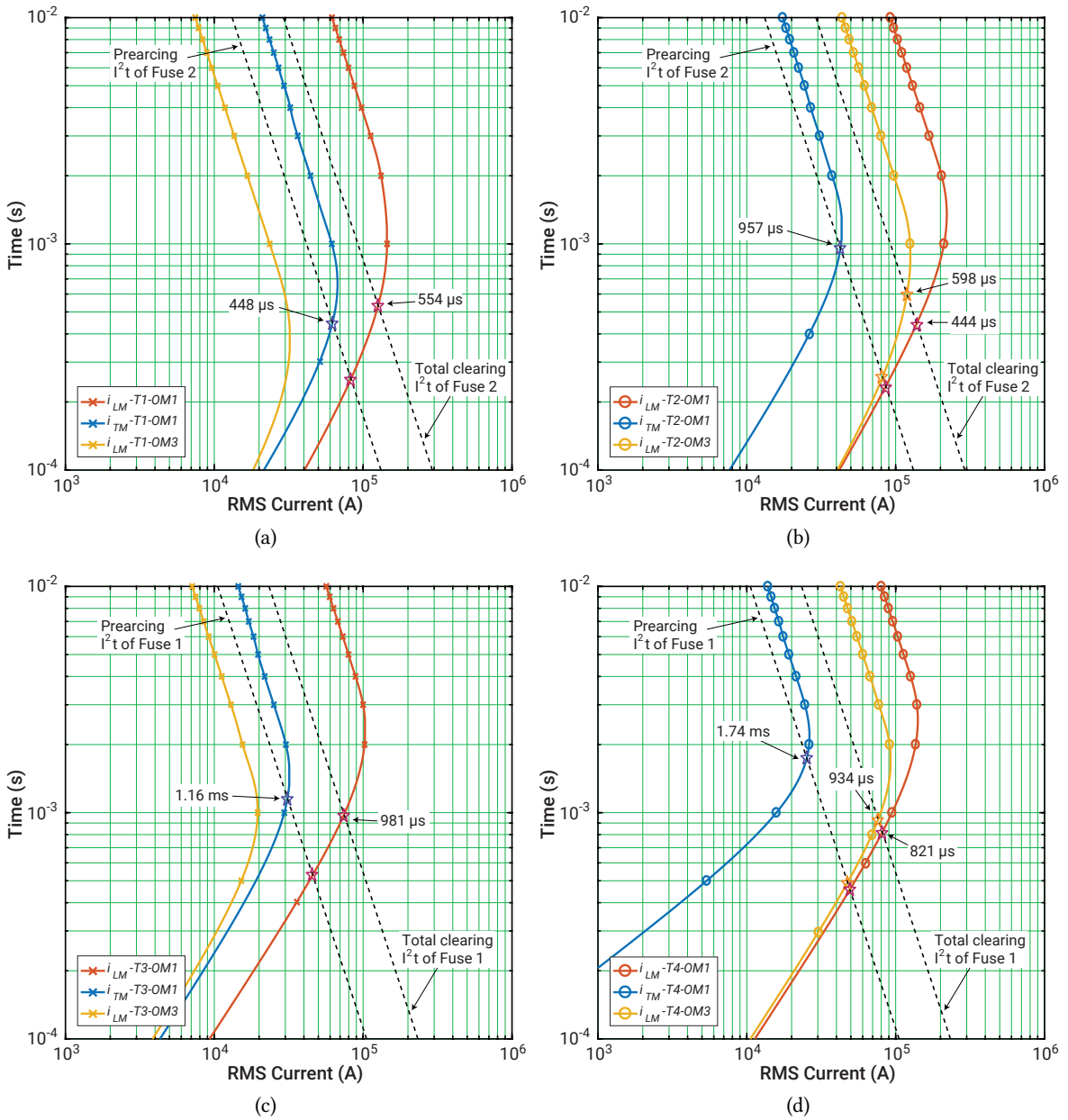


Fig. 3.11 Selectivity and sensitivity analyses for the studied DC PDNs: (a) TCC for *T1*, (b) TCC for *T2*, (c) TCC for *T3*, and (d) TCC for *T4*.

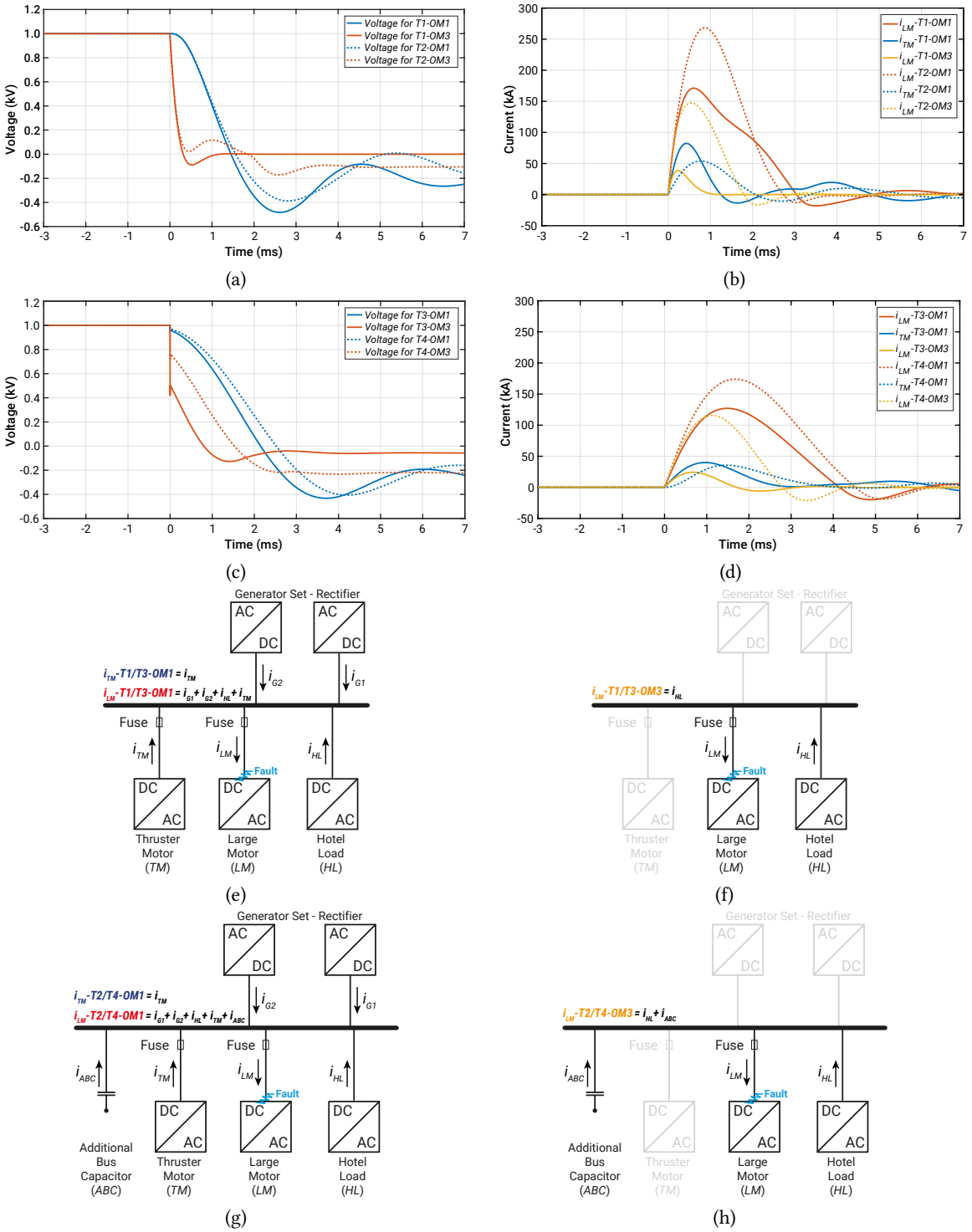


Fig. 3.12 Transient waveforms and current flows under different operating modes and configurations: (a) voltage waveforms for *T1* and *T2*, (b) current waveforms for *T1* and *T2*, (c) voltage waveforms for *T3* and *T4*, (d) current waveforms for *T3* and *T4*, (e) current flows for *T1* and *T3* under *OM1*, (f) current flows for *T1* and *T3* under *OM3*, (g) current flows for *T2* and *T4* under *OM1*, and (h) current flows for *T2* and *T4* under *OM3*.

provides the interrupting times of the fuse 1 and 2 based on calculated overcurrent levels under different operating modes and configurations. The transient waveforms and the current flows under the studied cases are also shown in **Fig. 3.12**. The negative voltages in **Fig. 3.12** are the resonant currents between the DC-link capacitor and the system inductance (the DC busbar inductance, the DC cable inductance only for the distributed configuration, and the inductance in the bus-tie switch). Note that the characteristics of the prearcing and total clearing I^2t ratings of fuse 1 and 2 (black dotted-lines) in **Fig. 3.11** are drawn by the values given in **Tab. 3.2**.

For *T1* in **Fig. 3.11(a)**, it is observed that the current ($I_{TM} - T1 - OM1$) passing through the fuse 2 on the *TM* feeder starts to melt the fuse (prearcing) at 448 μs before the total clearing of the fuse 2 on the *LM* feeder (the total clearing time: 554 μs). It means that the selectivity between the *LM* and *TM* feeders is not achieved for the fault at the *LM* feeder under *OM1*. Moreover, the sensitivity under *OM1* and *OM3* is not available for the fault at the *LM* feeder since the current ($I_{LM} - T1 - OM3$) is not enough to blow the fuse 2.

When the ABC method is employed in the centralized configuration (*T2*) in **Fig. 3.11(b)**, the fault at the *LM* feeder can be cleared at 444 μs under *OM1* by the current ($I_{LM} - T2 - OM1$) and at 598 μs under *OM3* by the current ($I_{LM} - T2 - OM3$). This implies that the sensitivity is available with the ABC method. Otherwise, the prearcing of the fuse 2 on the *TM* feeder is delayed by about 500 μs (from 448 μs to 957 μs). This delayed prearcing time provides enough margin to implement the selectivity between the *LM* and *TM* feeders.

In **Fig. 3.11(c)**, the total clearing time by the current ($I_{LM} - T3 - OM1$) and the prearcing time by the current ($I_{TM} - T3 - OM1$) are 981 μs and 1.16 ms, respectively. Therefore, the selectivity issue is not observed in *T3*. However, there is still the sensitivity issue under *OM1* and *OM3* because the fault energy provided by the capacitor at the *HL* feeder is not enough to blow the fuse 1 under the study condition.

For *T4* in **Fig. 3.11(d)**, the total clearing time of the fuse 1 on the *LM* feeder can be reduced from 981 μs to 821 μs. Otherwise, the ABC method can delay the prearcing time of the fuse 1 on the *TM* feeder from 1.16 ms to 1.74 ms. This increased time margin helps to provide reliable selectivity. In *T4*, the fault clearing is available at 934 μs under *OM3*. Hence, the sensitivity is enabled with the ABC method.

The additional fault energy by the ABC method is only required when the fault energy is not enough to blow the fuse. In other words, the ABC can be disconnected to avoid too much fault energy under ship configurations and operating modes that can provide the enough fault energy to ensure the fuse operation.

For the feeder protection, the results under the studied condition are summarized:

- Depending on ship operating modes and fault locations, there are cases for both the configurations that may have issues on the selectivity and/or the sensitivity.
- The ABC method reduces the fault clearing time of the fuse on the faulty feeder and delays the prearcing time of the fuse on the healthy feeder for both the configurations (achieving or extending the selectivity).
- The ABC method assists the fault clearing under the maximum and minimum fault conditions for both the configurations (enabling the sensitivity).

3.5 Conclusion

This chapter has presented the ABC method, which is based on the additional bus capacitor installed at the DC bus, to extend selectivity for the bus separation failure and the feeder protection. The principle and the selection of the ABC method are addressed and discussed with the modeling of the marine LVDC PDNs. The proposed ABC method is verified with the analyses on the voltage drop and the fault clearing time.

For the bus separation failure, the ABC method can mitigate the voltage drop for both the centralized and distributed PDNs. This improves the selectivity for the bus separation failure by reducing the possibility of the undesired converter trip in the healthy bus.

It is shown that the ABC method can not only reduce the fault clearing time under the maximum fault condition, but also allow for the fault clearing under the minimum fault condition. In other words, the method extends selectivity and sensitivity by directly providing the additional energy to the fuse on the faulty feeder under any system conditions.

4

Investigation on the Power Supply Protection for Different Types of Rectifiers

This chapter investigates the performance of power supply protection methods with various case studies. The modeling of three-different low-voltage DC power distribution networks is carried out with the discussions on their configurations, design considerations, and controls. The performance of each protection method is analyzed by comparing the fault energy limited by the protection method and the overloading capability of rectifiers. Moreover, an artificial short-circuit method, which limits the fault current to the rectifier by providing a low impedance path on the AC side, is proposed for the voltage source converter protection.

4.1 Introduction

At present there are three-dominant power supply systems for commercial marine LVDC PDNs: a diode rectifier, [26], a thyristor rectifier [71], and a voltage source converter (VSC) [72], all fed by a synchronous generator. The main difference among them comes from the rectifier type that gives a big impact on system configurations and controls. Furthermore, the power supply protection, which is the last action of the three-level protection described in **Chap. 2**, is strongly linked to the rectifier type. In case of the diode rectifier, deexcitation of a synchronous generator, specially designed to have high subtransient reactance, is used to limit the fault current from the generator [16], [26], [49], [73]. A fold-back protection control is applied to the thyristor rectifier [50], [71], while a high-speed fuse solution is commercially employed for the VSC protection [72].

The fuse has generally been accepted for converter protection by industrial manufacturers, whereas its notable disadvantage (e.g., low reliability) makes the VSC-based DC PDNs less reliable. Furthermore, the fuse on the generator side can be blown for the feeder fault if the selectivity is not carefully coordinated between upstream and downstream fuses (see **Fig. 4.1**). To tackle these issues this study proposes a new protection method for VSC-based power supply systems, described later on.

On the other hand, most of the works on the power supply protection have been published by industrial manufacturers and focused on their solution with the limited information to keep the technology confidentiality [16], [26], [71], [73]. Hence, it is necessary to provide not only comprehensive descriptions of system modeling (considering configurations, design considerations, and controls) but also integrated technical discussions on different power supply protection methods.

For the above reasons, this chapter thoroughly investigates the performance of power supply protection methods aforementioned with various case studies. The modeling of the three-different LVDC

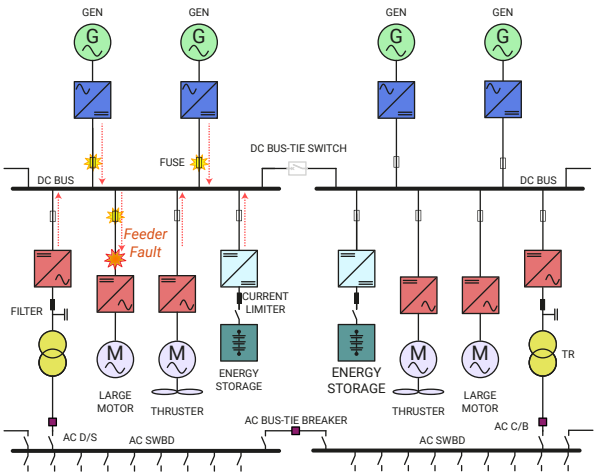


Fig. 4.1 A selectivity issue in DC PDNs with the DC fuse solution for the power supply protection.

PDNs is carried out with the discussions on their configurations, design considerations, and controls. The performance of each protection method is analyzed by comparing the fault energy limited by the protection method and the overloading capability of the three rectifiers. Moreover, an artificial short-circuit method on the AC side, which limits the fault current to the rectifier by providing a low impedance path between a synchronous generator and a rectifier, is newly proposed for the VSC protection.

4.2 System Modeling

This section describes the modeling of DC PDNs based on the three types of rectifiers. The systems selected for the studies on the power supply protection consist of a synchronous generator with a brushless exciter driven by a diesel engine, rectifiers, AC cables, AC and DC filters, DC busbars, a fault impedance, and an inverter-driven induction motor, as shown in **Fig. 4.2**. Note that each rectifier is modeled as one large converter while both paralleling of several small rectifiers and the use of the one large rectifier are possible.

4.2.1 Diesel Engine-Driven Synchronous Generator

A brushless synchronous generator driven by a diesel engine is commonly used for the primary power source on the onboard systems [98]. When a disturbance occurs in the onboard network, the

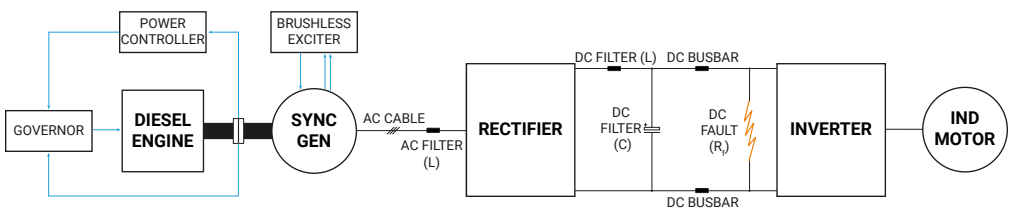


Fig. 4.2 Schematic diagram of the studied DC PDNs.

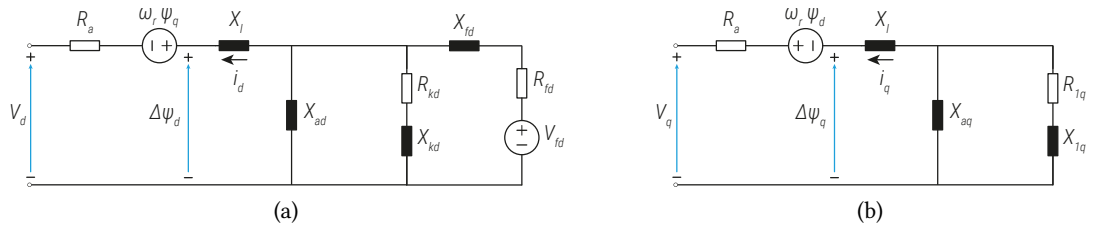


Fig. 4.3 Equivalent circuits for a synchronous generator [100]: (a) direct axis and (b) quadrature axis.

generator should stabilize the PDNs within the given time and the limitation specified in the class regulations. The voltage amplitude and frequency, which are very important factors in the system, can be controlled by the exciter and the governor, respectively.

A. Synchronous Generator

Direct-axis and quadrature-axis equivalent circuits are used for the modeling of a synchronous generator, as illustrated in **Fig. 4.3**. This is because these direct-quadrature circuits have been widely employed and can greatly simplify the generator transient analysis by selecting a reference frame rotating with the rotor [99].

Generally, the parameters of the generator are calculated from the machine design or obtained via open-circuit and short-circuit tests defined by standards [101], [102]. In the latter case, the generator parameters can be calculated from the data given by the tests with (4.1) and (4.2). The generator parameters used for the study are taken from [98] and presented in **Tab. 4.1**. Note that the direct-axis transient time constant ($T_d^{'}$) in [98] of 3.7 s is out of its typical values (0.2 s - 0.5 s [103]). Hence, the time constant is assumed as 0.37 s in the study.

$$
\begin{aligned}
X_d &= X_l + X_{ad} \\
X_d^{'} &= X_l + \left(\frac{1}{X_{ad}} + \frac{1}{X_{fd}} \right)^{-1} \\
X_d^{''} &= X_l + \left(\frac{1}{X_{ad}} + \frac{1}{X_{fd}} + \frac{1}{X_{kd}} \right)^{-1} \\
T_d^{'} &= \frac{1}{\omega R_{fd}} \left(X_{fd} + \left(\frac{1}{X_l} + \frac{1}{X_{ad}} \right)^{-1} \right) \\
T_d^{''} &= \frac{1}{\omega R_{kd}} \left(X_{kd} + \left(\frac{1}{X_l} + \frac{1}{X_{ad}} + \frac{1}{X_{fd}} \right)^{-1} \right)
\end{aligned}
\tag{4.1}
$$

$$
\begin{aligned}
X_q &= X_l + X_{aq} \\
X_q^{''} &= X_l + \left(\frac{1}{X_{aq}} + \frac{1}{X_{1q}} \right)^{-1} \\
T_q^{''} &= \frac{1}{\omega R_{1q}} \left(X_{1q} + \left(\frac{1}{X_l} + \frac{1}{X_{aq}} \right)^{-1} \right)
\end{aligned}
\tag{4.2}
$$

B. Brushless Excitation Systems

The voltage regulation in the study is performed by guidelines given in IEEE AC5A that is a simplified model for brushless excitation systems [104]. **Fig. 4.4** depicts a block digram of the IEEE AC5A exciter model that includes: the first-order main regulator; the second-order damping filter representing the state-derivative feedback; the first-order exciter; and the exciter saturation function. The parameters

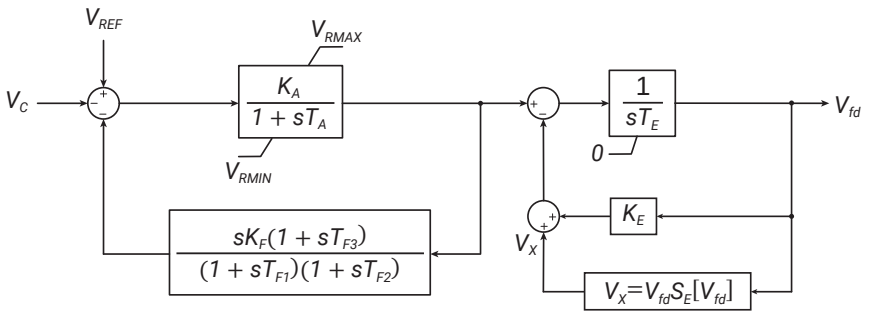


Fig. 4.4 Block diagram of the IEEE AC5A exciter model.

of the AC5A model is taken from [104] and shown in **Tab. 4.1**. Note that it is observed that the exciter time constant (T_E) in [104] of 0.8 s cannot keep the stability for the diode rectifier-based power supply. The time constant is, therefore, assumed as 0.1 s.

C. Diesel Engine Governor

A governor regulates the speed of a synchronous machine by adjusting fuel to the engine to keep the rated frequency in the AC network. On the other hand, the DC network does not have the system frequency and it allows for using variable-speed generators to save fuel consumption under light load

Tab. 4.1 Parameters used for the diesel engine-driven synchronous generator modeling [98], [104], [105].

Components	Parameters	Symbols	Values
Generator	Armature resistance	R_a	0.0036 pu
	Armature leakage reactance	X_l	0.052 pu
	Synchronous reactances	X_d; X_q	1.56 pu; 1.06 pu
	Transient reactance	$X_d^{'}$	0.296 pu
	Subtransient reactances	$X_d^{''}$; $X_q^{''}$	0.177 pu; 0.177 pu
	Transient short-circuit time constant	$T_d^{'}$	0.37 s
	Subtransient short-circuit time constants	$T_d^{''}$; $T_q^{''}$	0.05 s; 0.05 s
Exciter	Voltage regulator gain and time constant	K_A; T_A	400 pu; 0.02 s
	Maximum and minimum regulator output	V_{RMAX}; V_{RMIN}	7.3 pu; −7.3 pu
	Damping filter gain and time constants	K_F; T_{F1}; T_{F2}; T_{F3}	0.03 pu; 1.0 s; 0.0 s; 0.0 s
	Exciter gain and time constant	K_E; T_E	1.0 pu; 0.1 s
	Exciter voltage points	V_{fd1}; V_{fd2}	5.6 pu; 4.2 pu
	Exciter saturation function values	$S_E\left[V_{fd1}\right]$; $S_E\left[V_{fd2}\right]$	0.86 pu; 0.5 pu
Governor	Controller gain and time constants	K_p; T_{1c}; T_{2c}; T_{3c}	12 pu; 0.01 s; 0.02 s; 0.2 s
	Actuator time constants	T_{1a}; T_{2a}; T_{3a}	0.25 s; 0.009 s; 0.0384 s
	Torque limits	T_{MAX}; T_{MIN}	1.1 pu; 0.0 pu
	Machine time delay	T_D	0.024 s

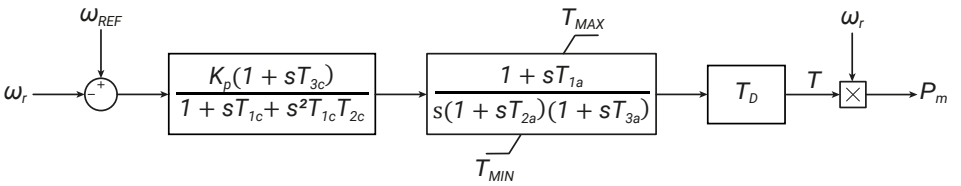


Fig. 4.5 Block diagram of the diesel engine governor model.

conditions. This variable-speed function is implemented in the power controller block in **Fig. 4.2**. Two-different speed levels in the block are assumed to find the severest condition: speed reference of 0.83 pu for light load conditions (< 50 %); and speed reference of 1.0 pu for heavy load conditions (≥ 50 %). Note that the continuous variation of engine speed according to load conditions should be necessary for the energy efficiency study.

Fig. 4.5 shows a block diagram of the diesel engine governor model used for the study [106]. The model is composed of dynamics of the engine and its control. The time delay (T_D) induced from crankshaft dynamics is also applied to the model. The governor parameters are presented in **Tab. 4.1**.

4.2.2 Power Distribution Lines and Filters

The electrical power generated by the generator is delivered via AC cables to the rectifier. The AC cable installation is, therefore, necessary between the generator and the rectifier. The AC cable is modeled by the π model that consists of lumped resistance, lumped inductance, and equally divided capacitance at both ends. Several single core cables in parallel are used depending on current ratings. The parameters of the single core cable with 1 kV and 631 A are: 0.082 Ω/km, 0.284 mH/km, and 0.834 μF/km [92]. The cable of 50 m is used [103].

The DC PDNs studied are based on the centralized configuration (see **Fig. 3.2**). The DC parts are, therefore, assumed to be connected through metallic busbars of 1 m and its inductance is 1 μH [91].

The AC-side inductance (or the phase inductance, L_F) is the inductance between the generator and the rectifier. The inductance plays a role in improving the line current waveform and limiting the short-circuit current. A common size of the inductance is in the range of 0.1 - 0.2 pu [107] and L_F = 0.1 pu is considered.

The DC-link capacitor (C_{DC}) on the DC side reduces a voltage ripple by filtering out harmonic currents. Furthermore, the capacitor decreases the harmonic coupling between converters on an instantaneous basis. The DC-link capacitor can be calculated as a function of the energy to power ratio (E_s) [32]

$$C_{DC} = \frac{2S_cE_s}{V_{DC}^2} \tag{4.3}$$

where S_c is the converter apparent power and E_s is chosen to be in the range of 10 –50 kJ/MVA. With E_s = 10 kJ/MVA and V_{DC} = 1 kV, the DC-link capacitance per power is considered as 20 mF/MVA.

The DC choke (or the DC reactor, L_C) for the harmonic mitigation is placed between the rectifier output and the DC-link capacitor. Among the three rectifiers studied, the DC choke is only considered for the thyristor rectifier due to a higher current ripple compared to the others. The inductance of the

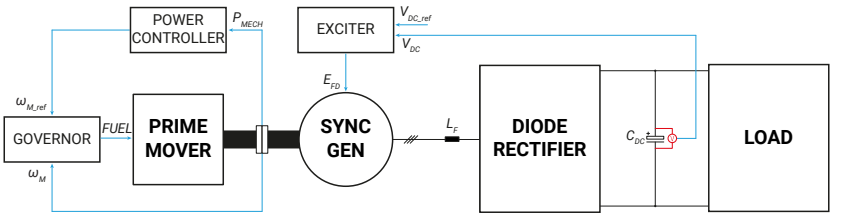


Fig. 4.6 Schematic diagram of power supply systems based on diode rectifier.

DC choke is calculated as [96]

$$L_C = \frac{V_{ripple}}{6\omega I_{DCmin}} \tag{4.4}$$

where V_{ripple} is the ripple voltage and chosen to be 0.05 pu of the rated DC voltage. I_{DCmin} is the minimum DC current which can be chosen to be 0.1 pu of the rated DC current.

4.2.3 Load and Fault

An induction machine driven by a two-level voltage source inverter is implemented to replicate electrical loads with the light (1 MW) and heavy (4 MW) load conditions. In the study, the dynamics of these electric loads is not important because the loads provide the initial fault conditions and will be tripped by the undervoltage protection of the inverter (0.8 pu in the study) if a system fault occurs. Hence, the detailed modeling of the loads is not presented.

The fault comes with the arc and the fault resistance is a function of the arc length and the current [108]. The DC fault can, therefore, occur with different fault resistance values depending on system conditions. The DC fault (R_f) is considered as 10 mΩ by analyzing the DC short-circuit current waveform presented in [73].

4.2.4 Diode Rectifier

The average DC voltage of a six-pulse diode rectifier used for LVDC PDNs is

$$V_{DC} = \frac{3\sqrt{2}}{\pi} V_{LL} - \frac{3}{\pi}\omega L_F I_{DC} \tag{4.5}$$

where V_{LL} is the line-to-line AC voltage, L_F is the AC-side inductance, and I_{DC} is the DC current.

The DC PDNs in [26] are based on the diode rectifier and use a synchronous generator of 690 V that is a common voltage level of commercial generators for marine PDNs. With $L_F = 0$, the average value of V_{DC} is approximately 1.35 V_{LL} and is around 930 V_{DC}. Thus, the rated DC bus voltage of the diode-based PDNs of 930 V_{DC} is considered by using a typical 690 V generator.

The diode rectifier converts AC to DC in an uncontrolled manner. Hence, the dynamics of voltage and current in this system are fully governed by the performances of the exciter and the governor (see **Fig. 4.6**). One distinctive feature in the control systems is that the exciter uses the DC voltage as the voltage input to regulate the DC voltage.

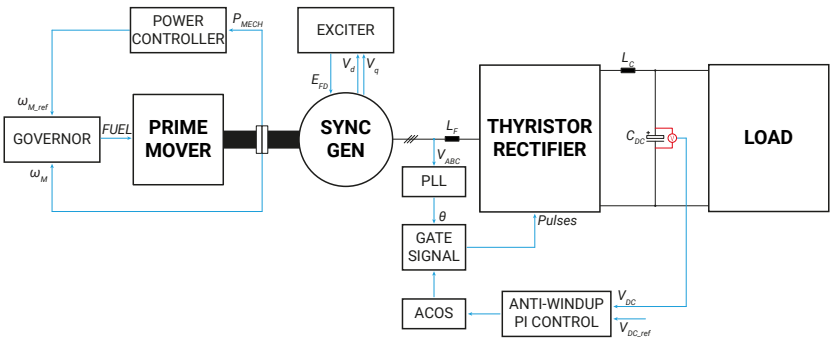


Fig. 4.7 Schematic diagram of power supply systems based on thyristor rectifier.

4.2.5 Thyristor Rectifier

Unlike the diode rectifier, the thyristor rectifier is a controllable rectifier and can adjust the DC output by varying the thyristor firing delay angle (α). By considering the firing angle, the DC voltage of a six-pulse thyristor rectifier is

$$V_{DC} = \frac{3\sqrt{2}}{\pi} V_{LL} \cos\alpha - \frac{3}{\pi}\omega L_F I_{DC} \tag{4.6}$$

Works of [50], [71] introduce the DC PDNs with the thyristor rectifier and provide the rated DC bus voltage of 1 kV without the information on the AC generator voltage. From (4.6), the AC generator voltage can be calculated as around 850 V with the assumptions of L_F = 0.1 pu, I_{DC} = 4 kA, and α = 20°. While the AC voltage of 850 V is not typical for commercial generators, this voltage is considered in the study because the typical 690 V generator cannot develop the DC voltage of 1 kV, without the use of active rectifiers.

In [50], the control scheme for the thyristor rectifier is presented and it consists of voltage and current controls. In this control, the DC bus voltage control provides the current reference and the DC current control regulates the error between the reference current from the DC voltage controller and the measured current. Otherwise, the DC voltage can be controlled only with the voltage control that compensates the DC voltage difference within a preset value by adjusting the firing angle. This study uses this simplified control scheme for the thyristor rectifier, as shown in **Fig. 4.7**. The parameters for the PI control are K_p = 5, K_i = 100, $acos_{MAX}$ = 1, and $acos_{MIN}$ = 0. Note that the fold-back protection control is an extra control function, i.e., it is not a part of the PI control.

4.2.6 Voltage Source Converter

In contrast to the previously presented rectifiers, a VSC in **Fig. 4.8** can boost the DC voltage with the modulation ratio (m_a) as

$$V_{DC} = \frac{2\sqrt{2}}{\sqrt{3}} \frac{1}{m_a} V_{LL} \quad (m_a \leq 1.0) \tag{4.7}$$

In linear modulation, the maximum allowable AC voltage is about 612 V at m_a = 1.0 to obtain the DC voltage level of 1 kV that is considered as the nominal DC voltage for LVDC PDNs in the study. A 480 V

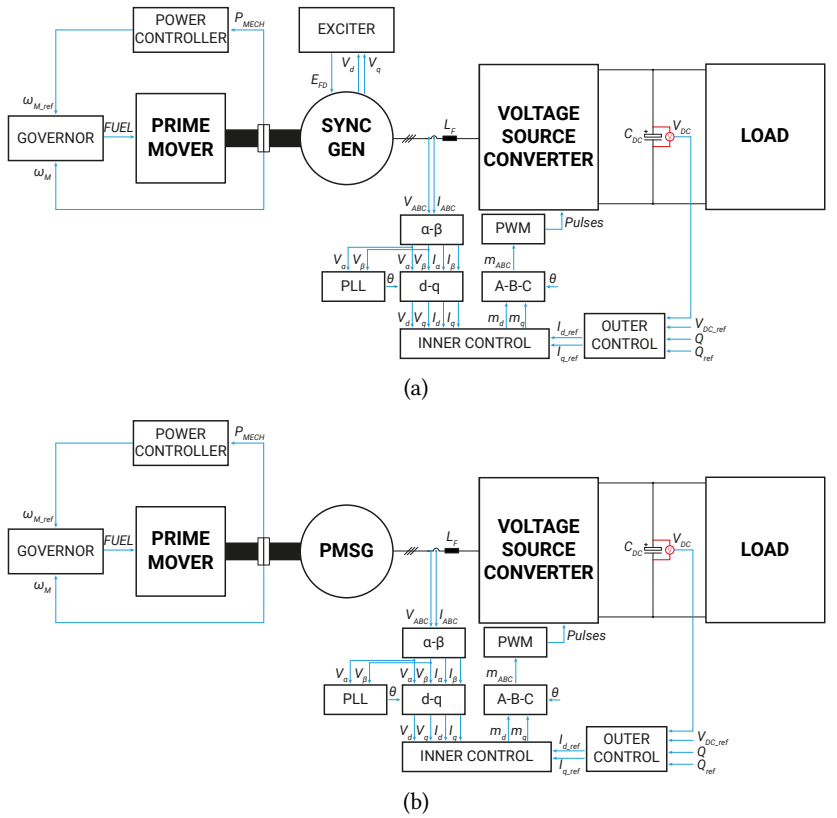


Fig. 4.8 Schematic diagrams of power supply systems based on VSC: (a) SG and (b) PMSG combinations.

generator, which is commercially available, is selected to replicate the VSC-based DC PDNs, presented in **Tab. 2.2**. Note that the use of the 690 V generator is also available with vector modulation.

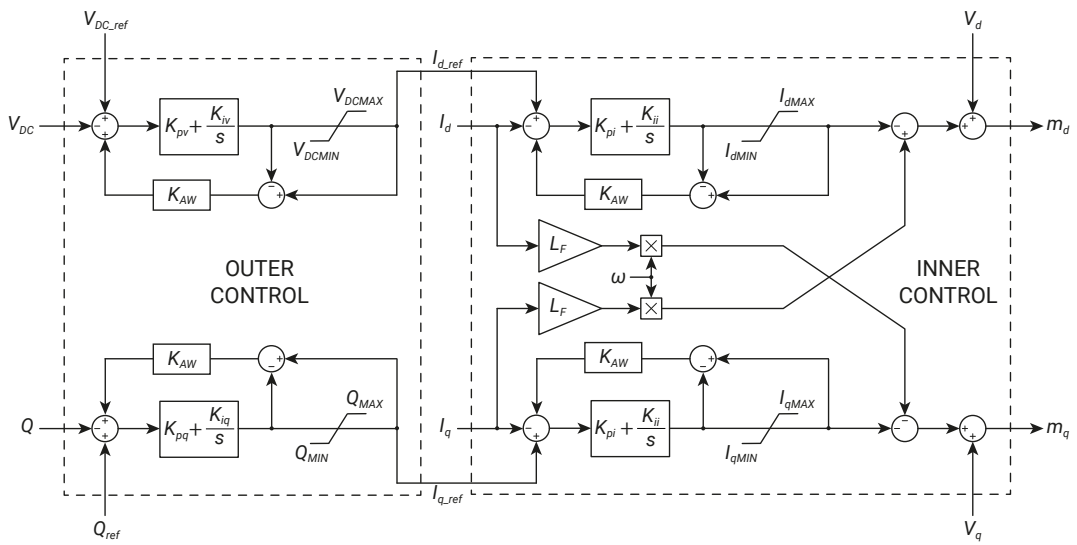


Fig. 4.9 Block diagram of VSC control.

Tab. 4.2 Parameters used for the VSC control.

f_{sw}	K_{pv}	K_{iv}	V_{DCMAX}	V_{DCMIN}	K_{pq}	K_{iq}	Q_{MAX}	Q_{MIN}	K_{pi}	K_{ii}	I_{dMAX}/I_{qMAX}	I_{dMIN}/I_{qMIN}
3000	9.6	293.9	1.2	−1.2	0	30	0.5	−0.5	1.5	4628.5	0.6	−0.6

For the VSC, the amplitude of the DC bus voltage and the reactive power can be adjusted independently by changing the modulation ratio and the phase of the pulse width modulation (PWM) gate pulse, as shown in **Fig. 4.8(a)**. The voltage control provides the current reference and the current control regulates the current to the reference value. Otherwise, the exciter and the governor regulate the generator terminal voltage and the machine speed, respectively. In the VSC, there is no need to precisely regulate the terminal voltage of a synchronous machine by the exciter. It means that a PMSG can be adopted instead of a wound rotor synchronous machine to achieve higher efficiency [see **Fig. 4.8(b)**].

In the study, the synchronous machine combined with a two-level VSC in **Fig. 4.8(a)** is used to keep the three PDNs consistent, except the rectifier type. Otherwise, the control scheme shown in **Fig. 4.9** and its parameters presented in **Tab. 4.2** are taken into account.

4.2.7 Simulation Model Verification

Step-load changes are carried out to verify the simulation models implemented: the first step-load change from 0.25 pu to 1.0 pu at 10 s; and the second step-load change from 1.0 pu to 0.25 pu at 20 s (see **Fig. 4.10**). When the load draws electrical power of 1 MW, the three systems can keep the rated

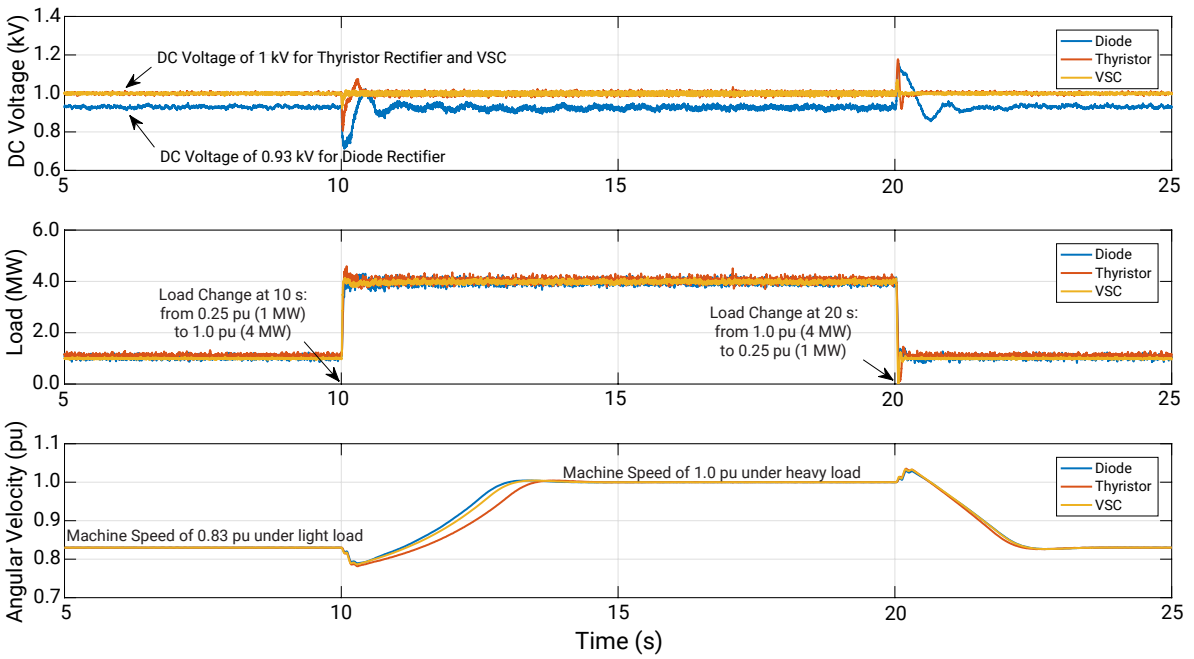


Fig. 4.10 Simulation model verification by step-load changes: (a) DC voltages, (b) electrical loads, and (c) generator speeds.

voltages (i.e., 0.93 kV for the diode rectifier and 1 kV for the thyristor rectifier and the VSC). The machine speeds of all the three systems are also adjusted as 0.83 pu by the variable-speed function implemented in the power controller block.

The step-load change from 0.25 pu to 1.0 pu causes sudden DC voltage drops and then these voltages are recovered by each voltage regulation function with its time constant. The simulation results show that the VSC has the best performance in voltage regulation with less voltage drop and faster recovery time, while the diode-based system demonstrates the worst performance among them, as expected. For the step-load change from 1.0 pu to 0.25 pu, the abrupt voltage increases are also controlled and eventually the voltages go to the rated voltages.

For the generator speed, during the step-load increase, the generators have a decrease in the frequency for a short time and then the speeds approach its rated value (1.0 pu) that is the target speed for the heavy load. **Fig. 4.10** shows that the variable-speed regulation also works for the step-load decrease.

4.3 Proposed Artificial Short-Circuit Method

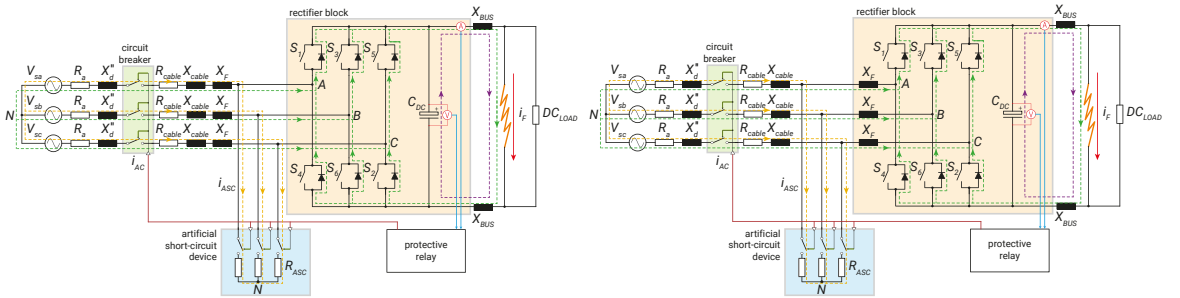
The artificial short-circuit method is proposed as an alternative solution for the VSC protection. The working principle of the method is presented with the technical discussions on a short-circuit making device and a short-circuit resistor intentionally inserted to provide its reliable operation.

4.3.1 Working Principle of the Proposed Method

Aforementioned, the use of the high-speed fuse for the VSC-based power supply has a remarkable drawback in the protection reliability, while it is an economic solution and convenient to employ. There are several ways to address this issue: a fault-blocking converter with a DC isolator; an AC circuit breaker with an increased AC coupling reactor or an oversized VSC; and a solid-state or hybrid DC circuit breaker.

An MMC based on full-bridge cells can block the DC fault current and a DC isolator can provide galvanic isolation (or electrical isolation). This type of the fault-blocking converter is, however, difficult to apply to commercial LVDC PDNs due to its high cost and conduction losses. A larger AC coupling reactor or an oversized VSC is necessary for the relatively slow AC circuit breaker option. The expected issue in this option is that the reactor value and the VSC overloading capability should be very high to withstand the overcurrent for a long fault interrupting time (T_{trip}, 3 –5 cycles). The solid-state or hybrid DC circuit breaker is an attractive solution for the VSC protection. However, the breaker is not yet readily available in the market and its expected cost may make DC PDNs less competitive in the electrical installation cost.

The artificial short-circuit method depicted in **Fig. 4.11** is proposed to overcome the aforementioned drawbacks of the protection methods. When the DC fault is detected, the internal protection of the VSC blocks the operation of the IGBT switches by removing PWM pulses and then the rectifier acts as a diode rectifier. The anti-parallel diodes in the rectifier experience the fault current during this period. The proposed method enables the mitigation of the fault current passing through the diodes by developing the three-phase short circuit between the generator and the rectifier. The artificial short circuit provides a branch current path (orange-colored dot lines in **Fig. 4.11**) with a low impedance



(a) (b)

Fig. 4.11 Schematic diagrams of artificial short-circuit method: (a) short-circuit after the AC reactor (option 1) and (b) short-circuit before the AC reactor (option 2).

within 4 ms if a high-speed earthing switch [109] or a fast arc eliminator [110] is used for the short circuit. Finally, the AC circuit breaker separates the generator from the artificial short-circuit and the DC fault. With this principle, the proposed method can effectively protect the diodes by quickly mitigating the fault energy during this period.

4.3.2 Sizing of Artificial Short-Circuit Resistance

If the fault current is too high, it is a severe fault in the vicinity of the machine and may cause machine damage. Furthermore, the breaking of the AC circuit breaker and the making of the short-circuit device cannot be possible if the overcurrent is higher than the rating of each device. Hence, the overcurrent level should be managed to be lower than the breaking capability of the AC circuit breaker (I_{cs}) and the making capability of the short-circuit device (I_{cm}). The short-circuit resistance (R_{ASC}) is considered for this purpose.

There are two approaches to implement the proposed method. First, the short-circuit device is placed between the AC reactor and the VSC [option 1 in the study, see **Fig. 4.11(a)**]. The second is the installation of the short-circuit device before the AC reactor if the reactor is a part of the rectifier [option 2 in the study, see **Fig. 4.11(b)**]. This approach requests higher short-circuit resistance for the reliable short-circuit making and the AC circuit breaker interruption.

In both configurations, the fault current amplitude is decided by the subtransient reactance, the AC cable impedance (R_{cable} and X_{cable}), the AC reactor (X_F), the short-circuit resistance (R_{ASC}), the DC busbar reactance (X_{BUS}), and the DC fault resistance (R_f). For the reliable breaking, the fault current should be

$$I_{cs} \geq i_{AC} = \frac{V_{ac}}{2Z_S + 2Z_{ASC} // 2Z_{DC}} \tag{4.8}$$

where

$$V_{ac} = V_{sa} - V_{sc}$$
$$Z_{ASC} = R_{ASC}$$
$$Z_S = \sqrt{(R_a + R_{cable})^2 + (X_d'' + X_{cable} + X_F)^2},\ Z_{DC} = \sqrt{(R_f/2)^2 + X_{BUS}^2} \qquad \text{(for option 1)}$$

Tab. 4.3 Parameters and equipment ratings used for the VSC-based PDNs.

V_{ac}	R_a	X_d''	R_{cable}	X_{cable}	X_F	X_{BUS}	R_f	I_{cs}	I_{cm}
480 V	0.0036 pu	0.177 pu	0.0089 pu	0.0116 pu	0.1 pu	0.0082 pu	0.217 pu	50 kA	40 kA

$$Z_S = \sqrt{(R_a + R_{cable})^2 + (X_d'' + X_{cable})^2},\ Z_{DC} = \sqrt{(R_f/2)^2 + (X_F + X_{BUS})^2} \qquad \text{(for option 2)}$$

On the other hand, the making rating based on the peak current (I_{cm}) should be higher than the short-circuit current passing through the short-circuit device as

$$I_{cm} \geq i_{ASC} = \frac{\sqrt{2}V_{ac}}{2Z_S + 2Z_{ASC}//2Z_{DC}} \frac{Z_{DC}}{Z_{ASC} + Z_{DC}} \tag{4.9}$$

Finally, the fault current and its energy passing through the anti-parallel diode in the IGBT module should be

$$I_{FSM} \geq i_F = \frac{\sqrt{2}V_{ac}}{2Z_S + 2Z_{ASC}//2Z_{DC}} \frac{Z_{ASC}}{Z_{ASC} + Z_{DC}} \tag{4.10}$$

and

$$I^2 t_D \geq \frac{1}{3} \int_0^{T_{trip}} {i_F}^2(t) dt \tag{4.11}$$

With the system values in **Tab. 4.3** and the IGBT module ratings in **Tab. 4.4**, the above conditions are applied to the selection of the short-circuit resistance (R_{ASC}) and the values are finally chosen as 5 mΩ for option 1 and 15 mΩ for option 2.

4.4 Protection Method Assessment

The performance of the existing and proposed protection methods is analyzed by comparing the fault energy limited by the protection method and the overloading capability of the rectifiers.

4.4.1 Study Conditions

For the three rectifiers, semiconductor devices in **Tab. 4.4** are chosen to handle the rated DC current (4.3 kA for the diode rectifier and 4.0 kA for the thyristor rectifier and the VSC) and the rated line voltages (690 V for the diode rectifier, 850 V for the thyristor rectifier, and 480 V for the VSC).

Among the three devices in **Tab. 4.4**, the ratings of the peak surge current and the limiting load integral, which provide information on the fault current withstand capability of semiconductors, are the highest for the thyristor, while they are the lowest for the IGBT with anti-parallel diode. It implies that the DC fault in the VSC-based PDNs has to be cleared faster than the other rectifiers.

Tab. 4.4 High-power semiconductor data chosen for the considered rectifiers.

Device	Rated Voltage V_{RRM}, V_{DRM} or V_{CES} (V)	Rated Current $I_{F(AV)M}$, I_C or $I_{T(AV)M}$ (A)	Peak Surge Current I_{FSM} or I_{TSM} (kA)	Limiting Load Integral I^2t (A^2s)
Diode - 5SDD 51L2800 [111]	2800	5380	65.0	$21.13 \cdot 10^6$
Thyristor - 5STP 45Q2800 [112]	2800	5490	77.0	$29.64 \cdot 10^6$
IGBT - 5SNA 3600E170300* [113]	1700	7200	36.0	$12.96 \cdot 10^6$

* Note: Two IGBTs in parallel

A system fault is an unintentional event and can occur under any load conditions. To find more severe condition, the fault simulations for the diode-based PDNs are conducted under the light load condition (1 MW) and the heavy load condition (4 MW), as shown in **Fig. 4.12**. It is observed that the fault current and its energy under the light load are higher than those under the heavy load. This is due to the decreased reactance with the lower machine speed. With this result, the light load condition is considered in the study.

4.4.2 Generator Deexcitation for Diode Rectifier

When a DC fault occurs at the diode-based PDNs, the exciter increases the field voltage to regulate the DC voltage and this regulation supports the fault current until the fault is interrupted (see **Fig. 4.13**) or the system loses its stability. On the contrary, the generator deexcitation can diminish the fault current and finally make it zero. To analyze the deexcitation performance, the study cases consist of two-different subtransient reactances [$X_d^{''}$ = 0.177 pu and $X_d^{''}$ = 0.266 pu (150 % of 0.177 pu)] as well as exciter responses (T_e = 0.1 s and T_e = 1.0 s).

In the studied conditions, the surge current capability of the diode (about 15.1 pu) has enough margin against the fault currents for both reactances. However, the situation is the opposite in the case

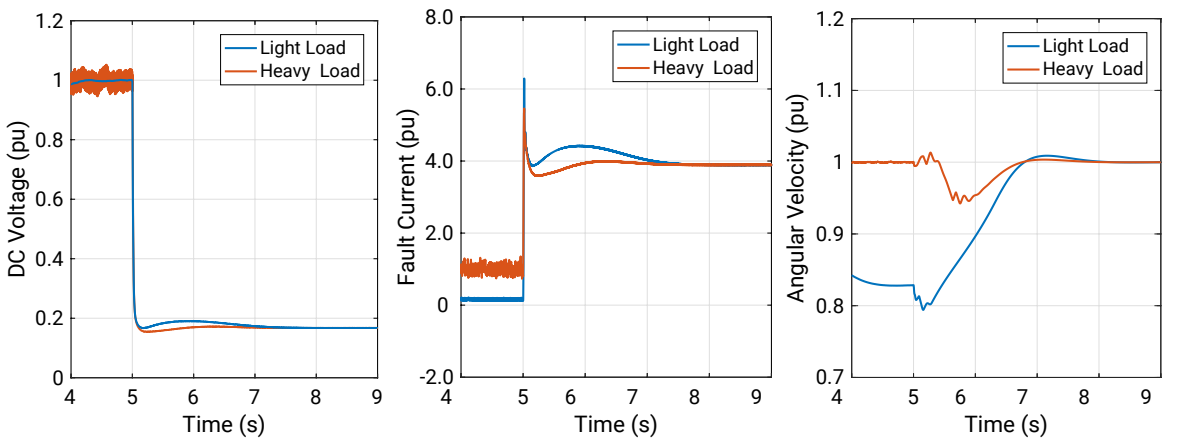


Fig. 4.12 Fault characteristics of variable-speed generation systems: (a) DC voltages, (b) DC currents, and (c) generator speeds.

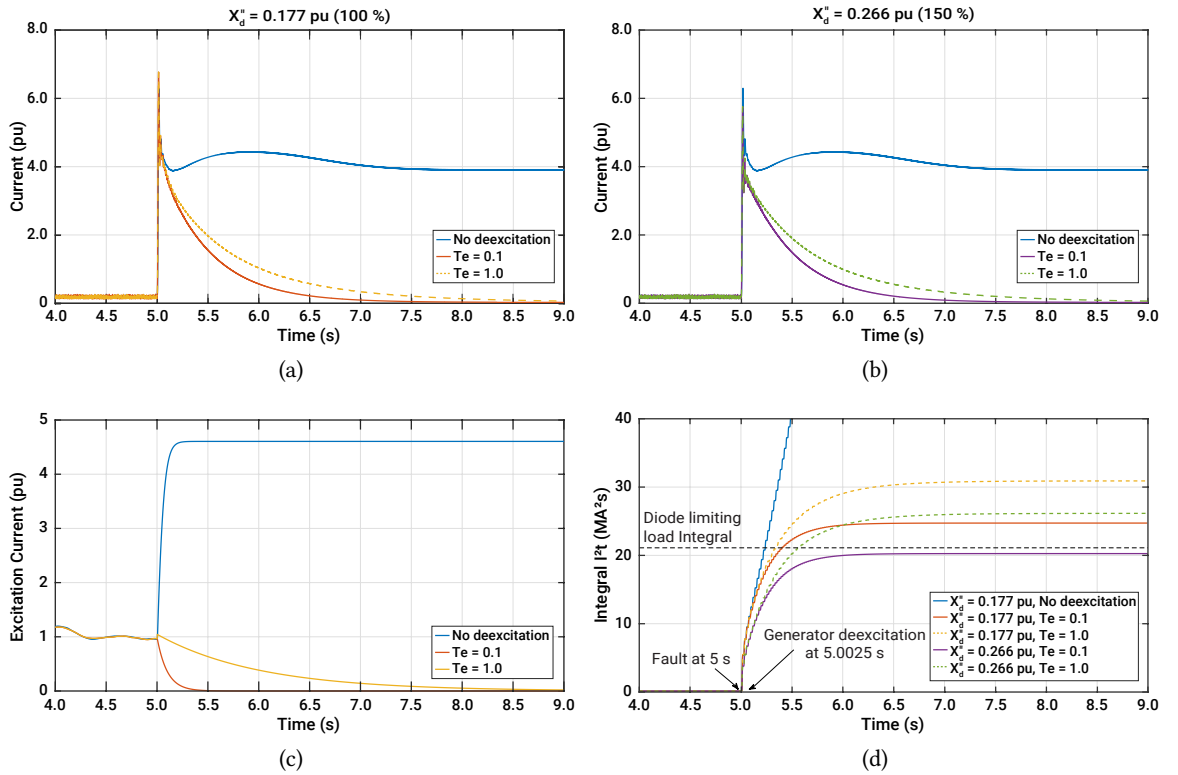


Fig. 4.13 Short-circuit analysis for the diode rectifier-based PDNs: (a) DC currents for normal subtransient reactance, (b) DC currents for high subtransient reactance, (c) exciter currents, and (d) fault energies passing through one of the diodes.

of energy. **Fig. 4.13(d)** shows that the diode cannot be protected for the three cases. Moreover, the diode can sustain the lowest fault energy case (high subtransient reactance with fast exciter response, $X_d^{''}$ = 0.266 pu and T_e = 0.1 s) with very little margin. To conclude, the fault energy limited by the deexcitation should be carefully managed due to its relatively long fault duration. For further investigations, **Chap. 5** presents comprehensive study results on the deexcitation characteristics.

4.4.3 Fold-Back Protection Control for Thyristor Rectifier

The fold-back protection control of the thyristor rectifier can promptly interrupt the fault current by changing the firing angle from 25° to 150°, as shown in **Fig. 4.14**. During the initial stage of the fault, the rectifier attempts to increase the DC voltage by reducing the firing angle to the lowest value. The firing angle of 150° is forced with the considered time delay of 2.5 ms after the fault detection.

Fig. 4.14 shows that the fault current and its energy limited by the fold-back protection control are much less than the ratings of the thyristor surge current (19.2 pu) and overloading capability (29.64 MA^2s). It means that the thyristor rectifier has a competitive advantage in the system protection due to its fault blocking function and high overloading capability.

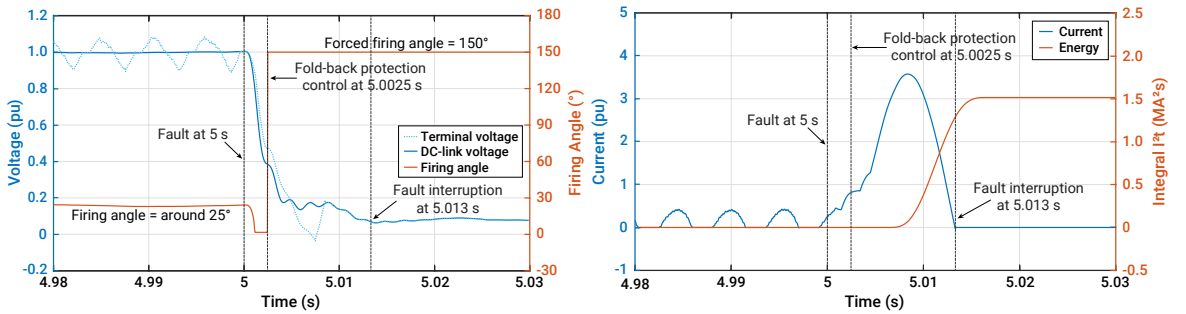


Fig. 4.14 Short-circuit analysis for the thyristor rectifier-based PDNs: (a) DC voltages and firing angle and (b) fault current and energy. Note that the blue-dotted line and the blue solid line represent the rectifier terminal voltage before the DC choke and the DC-link voltage, respectively.

4.4.4 Artificial Short-Circuit for VSC

For the VSC, the DC fuse solution is analyzed in **Fig. 4.15** and the considered prearcing I^2t of the fuse is 4.48 MA^2s [data for eight fuses (179M1833 in [94]) in parallel]. In **Fig. 4.15**, the prearcing of the DC fuse is started in 0.8 ms after the fault under the studied condition. It implies that the total clearing I^2t of the DC fuses on the feeders should be sized to be blown within this time range. This is because the DC short-circuit fault on the feeder side is expected to be a similar fault level due to low impedance in the DC networks, especially in the case of centralized PDNs. As mentioned earlier, unreliable DC fuses may generate the selectivity issue considering this short operating time even though the fuse solution allows for reducing the electrical installation cost.

Once the fault is detected, the short-circuit device is activated within 4 ms and this artificially generated short-circuit mitigates the fault current through the rectifier by providing a low impedance path. The simulation studies for the proposed method are carried out for two conditions: option 1 - short-circuit between the AC reactor and the VSC; option 2 - short-circuit between the generator and the AC reactor. The short-circuit resistances intentionally inserted (R_{ASC}) are 5 mΩ for option 1 and 15 mΩ for option 2, respectively.

For the option 1, the fault current from the generator is effectively controlled to be below the breaking rating of the AC circuit breaker (I_{cs} of 50 kA). The making of the short-circuit device (I_{cm} of 40 kA) is also available in the study. **Fig. 4.16(c)** shows that the DC fault current in the option 1 is rapidly

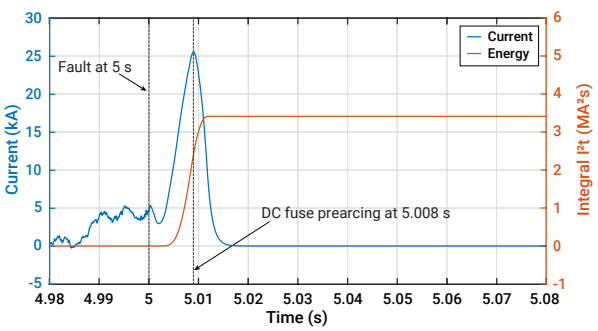


Fig. 4.15 Short-circuit analysis of the DC fuse solution for the VSC-based PDNs.

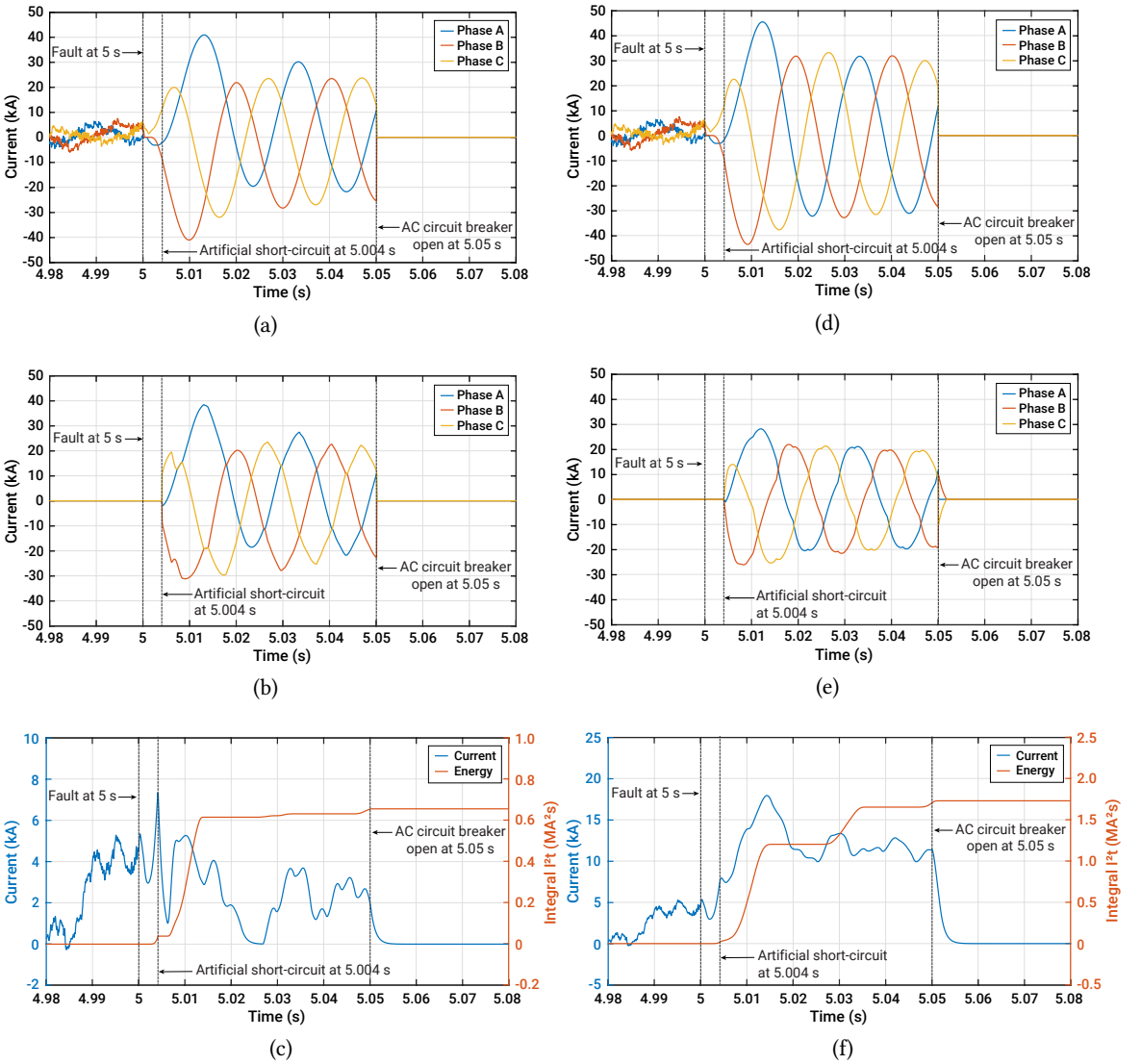


Fig. 4.16 Short-circuit analysis of the artificial short-circuit method for the VSC-based PDNs: (a) currents from the generator (option 1), (b) currents through the short-circuit device (option 1), (c) DC current and fault energy through one of the diodes (option 1), (d) currents from the generator (option 2), (e) currents through the short-circuit device (option 2), and (f) DC current and fault energy through one of the diodes (option 2).

reduced once the short-circuit is generated. The fault energy is not a primary concern of the system protection with this fast operation and the reduced fault current. The fault current and its energy in the option 2 are higher than those in the option 1 due to the location of the AC reactor and the higher short-circuit resistance. Nevertheless, their levels are still under the diode ratings (12.96 MA^2s).

From these study results, it could be stated that the proposed method can control the fault current and its energy below the IGBT module rating with enough margins in which the anti-parallel diode is a critical part after the IGBT blocking. For the proposed method, it is needed to install the AC circuit breaker and the artificial short-circuit device for every single generator. Thus, there may be a cost trade-off issue among various feasible solutions, e.g., the DC fuse solution, the fault-blocking

converter, and the solid-state DC circuit breaker. In spite of the cost increase, the main advantages, fast, reliable, and selective operations, strongly support the proposed method to be a feasible solution for the VSC protection.

4.5 Conclusion

This chapter has investigated the protection schemes for the three-different PDNs with various short-circuit analyses. The overview of the protection schemes for the diode and thyristor rectifiers is briefly provided, and the new protection scheme for the VSC is introduced. With the system modeling, the DC short circuit analyses are carried out for the several protection schemes, and each protection scheme is evaluated by comparing the fault energy limited by the protection operation with the limiting load integral of the semiconductors.

To employ the deexcitation method, the protection scheme has to be thoroughly coordinated to manage the fault energy below the semiconductor overload rating. In the absence of the fast-flux discharging method, it takes a relatively long time (several seconds) to extinguish the fault current in the analysis. The thyristor rectifier has a competitive advantage in the system protection due to its fault blocking function and high overloading capability. For the VSC, the DC fuse is still a feasible solution, while it is necessary to carefully coordinate the operating time frames between the supply-side and feeder-side fuses. The simulation results for the proposed protection method show that the method provides an excellent performance for limiting the fault energy and can be a promising solution for the VSC-based PDNs.

5

Impact of Synchronous Generator Deexcitation Dynamics on Diode Rectifier Protection

This chapter presents the impacts of synchronous generator deexcitation dynamics on the diode rectifier protection. The analytical expression of a DC short-circuit current is introduced considering a circuit topology, transient generator dynamics, and generator deexcitation. The DC fault currents under the deexcitation are comprehensively examined for different system factors: subtransient reactance, fault resistance, DC-link capacitance, exciter response, and time delay. Results are collected from a scaled-down experimental test setup.

5.1 Introduction

As presented in **Chap. 2** and studied in **Chap. 4**, for the diode rectifier protection, the deexcitation of a synchronous generator, specially designed to have high subtransient reactance, has been used to limit the fault current from the generator [16], [26], [49], [73]. While the deexcitation of the generator is activated, the generator produces a very high amplitude of current during the first few cycles. After that, due to the decrease in the excitation current, the fault current is gradually reduced, and finally, it becomes zero. Hence, the diodes in the rectifier should be sized with the consideration of the dynamic characteristics of the generator and the deexcitation under the worst condition.

On one hand, [26] provides the principle of the deexcitation and the effect of the high subtransient reactance with one experimental test result. However, there is lack of information on analytical description, rectifier sizing, and multiple system factor impact, e.g., subtransient reactance, fault resistance, DC-link capacitance, exciter type (or exciter response), and deexcitation time delay (2.5 ms in [16]). These technological gaps are covered in this chapter with the analytical and experimental investigations.

On the other hand, in conventional protection for AC PDNs, the deexcitation of a synchronous machine is considered as the loss of an excitation fault (a field failure) and has to be protected by the generator protection system [62], [114]. As the part of the generator protection, fast field discharging systems have been proposed in [115]–[117] and recommended in [118] to prevent a machine damage from a severe fault in the vicinity of the machine or excitation system. While there are many fast discharge methods, the principal idea is to install the discharge resistor in the rotor circuit and to bypass the current flow through the resistor if the fast field discharge is needed, as shown in **Fig. 5.1**. This can be implemented by the installation of the mechanical field breaker in parallel to the discharge resistor. For the quick operation, the mechanical breaker can be replaced by an IGBT. Note that this fast discharge technique is out of the scope of the work.

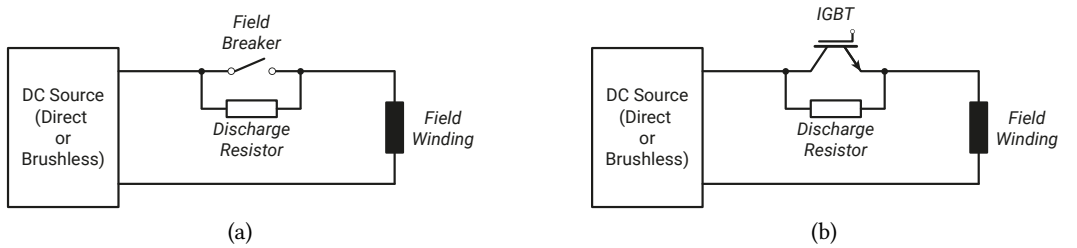


Fig. 5.1 Simplified schematic of fast field discharge circuits: (a) mechanical breaker and (b) IGBT [118].

The new system, which is an off-grid microgrid system based on DC technology, opens the door to use the deexcitation as the power supply protection without any circuit breakers. The fault current and its energy should be carefully managed in case that the deexcitation is used for the rectifier protection purpose in DC PDNs due to very low overloading capability of rectifiers compared with conventional AC equipment. Thus, the comprehensive fault behaviours under the deexcitation, which are not covered by [115]–[117], should be scrutinized for different system factors in DC PDNs, as presented hereafter.

5.2 Theoretical Considerations

The fault current under the deexcitation in DC PDNs, which is weak-grid systems with a low short-circuit ratio, is composed of different system dynamics. To effectively describe its behaviour, the analytical expression is presented in three steps. The analytical expression introduced is verified by comparing it with experimental test results. Lastly, the rectifier sizing is discussed in terms of the peak non-repetitive surge current and the limiting load integral.

5.2.1 DC Short-Circuit in Six-Pulse Diode Rectifier

When a DC short-circuit fault occurs in a six-pulse diode rectifier fed by a three-phase voltage source, the fault current is conducted through one of the diodes in the positive rail (D_1, D_3, and D_5) and one of the diodes in the negative rail (D_2, D_4, and D_6), as shown in **Fig. 5.2(a)**. Each diode conducts the fault current with the interval angle of 120°. For the maximum fault current condition ($R_f = 0$) that allows for neglecting C_{DC}, the system can, therefore, be expressed as a simple RL circuit [see **Fig. 5.2(b)**]. For this circuit, when D_1 is conducting, the current passing through D_1 (i_D) is [32], [99]

$$i_D(t) = \frac{V_m}{Z}\sin(\omega t + \alpha - \phi) - \frac{V_m}{Z}\sin(\alpha - \phi)e^{-\frac{R_{eq}}{L_{eq}}t} \tag{5.1}$$

where

$$V_{g\_ac} = V_m \sin(\omega t + \alpha),\ R_{eq} = 2R_S,\ L_{eq} = 2L_S,\ Z = \sqrt{{R_{eq}}^2 + \left(\omega L_{eq}\right)^2},\ \text{and}\ \phi = \arctan\left(\frac{\omega L_{eq}}{R_{eq}}\right).$$

In (5.1), the fault current consists of the steady-state current and the DC component. Depending on the instant of the short-circuit, the current only consists of the steady-state current (no DC component) when $\alpha = \phi$ or can theoretically reach $2V_m/Z$ with the maximum DC component of V_m/Z when $\alpha = \phi - \pi/2$.

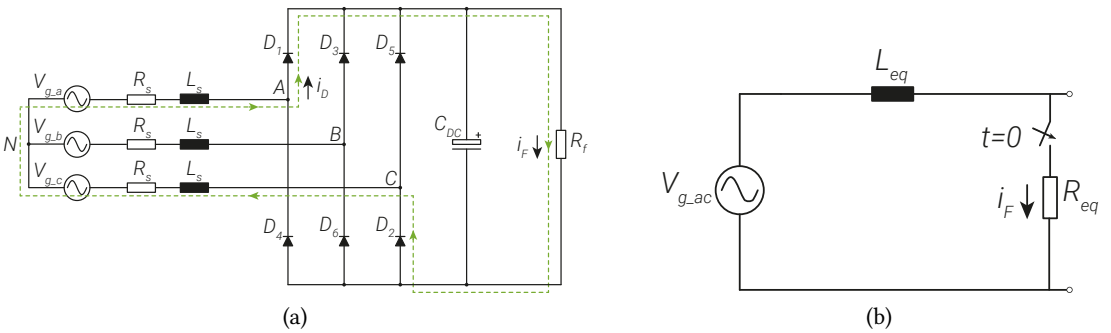


Fig. 5.2 Equivalent circuits of a six-pulse diode rectifier under a DC fault: (a) current flow for one positive half cycle and (b) a simple RL circuit.

5.2.2 Transient Phenomena in Synchronous Generator

However, (5.1) is only valid for a power system with a high short-circuit capacity. In reality, the dynamics of the generator should be considered for transient analyses, especially in the case of an off-grid system directly powered by the generator like marine PDNs. The fault current provided by the synchronous generator consists of three distinct periods: subtransient period, lasting for the first few cycles; transient period, sustaining longer cycles; and finally, steady-state period, remaining constant current (see **Fig. 5.3**). These dynamics of the generator are due to the change of the direct-axis machine parameters depending on the period: subtransient reactance (X_d'') and time constant (T_d''), transient reactance (X_d') and time constant (T_d'), and steady-state reactance (X_d). Additionally, the DC component decays with a time constant (T_a) which is equal to the average value of direct-axis subtransient reactance (X_d'') and quadrant-axis subtransient reactance (X_q'') [119]. The fault current under the consideration of the generator dynamics is

$$i_D(t) = \sqrt{2}E_0\,Y(t)\sin(\omega t + \alpha - \phi) + \frac{\sqrt{2}E_0}{\sqrt{{R_{eq}}^2 + {X_d''}^2}}\sin(\alpha - \phi)e^{-\frac{t}{T_a}} \tag{5.2}$$

where

$$Y(t) = \left(\frac{1}{\sqrt{{R_{eq}}^2 + {X_d''}^2}} - \frac{1}{\sqrt{{R_{eq}}^2 + {X_d'}^2}}\right)e^{-\frac{t}{T_d''}} + \left(\frac{1}{\sqrt{{R_{eq}}^2 + {X_d'}^2}} - \frac{1}{\sqrt{{R_{eq}}^2 + {X_d}^2}}\right)e^{-\frac{t}{T_d'}} + \frac{1}{\sqrt{{R_{eq}}^2 + {X_d}^2}},$$

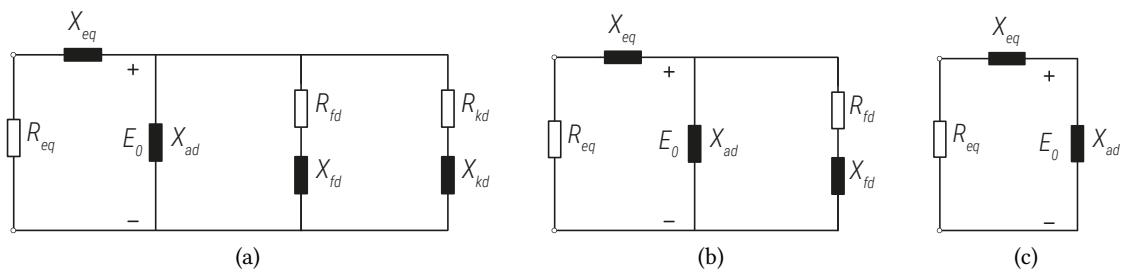


Fig. 5.3 Equivalent circuits of a d-axis synchronous generator: (a) subtransient, (b) transient, and (c) steady-state.

$$
\begin{aligned}
X_d &= X_{eq} + X_{ad}, \\
X_d^{'} &= X_{eq} + \left(\frac{1}{X_{ad}} + \frac{1}{X_{fd}} \right)^{-1}, \\
X_d^{''} &= X_{eq} + \left(\frac{1}{X_{ad}} + \frac{1}{X_{fd}} + \frac{1}{X_{kd}} \right)^{-1}, \\
T_d^{'} &= \frac{1}{\omega R_{fd}} \left(X_{fd} + \left(\frac{1}{X_{eq}} + \frac{1}{X_{ad}} \right)^{-1} \right), \\
T_d^{''} &= \frac{1}{\omega R_{kd}} \left(X_{kd} + \left(\frac{1}{X_{eq}} + \frac{1}{X_{ad}} + \frac{1}{X_{fd}} \right)^{-1} \right), \text{ and} \\
T_a &= \frac{X_d^{''} + X_q^{''}}{2\omega R_{eq}}.
\end{aligned}
$$

Note that (5.2) is the same as the fault current equation in [120] and [121], widely used for the maximum fault current calculation if $R_{eq} = 0$.

5.2.3 Deexcitation of Synchronous Generator

Direct and brushless excitation systems (see **Fig. 5.4**), which provide a magnetizing current to the generator, have been widely used for marine applications. While the direct excitation system has fast dynamic response, the brushless excitation system takes a long time to completely remove the excitation due to its indirect DC voltage generation as well as its inability to reverse the voltage applied to the rotor winding.

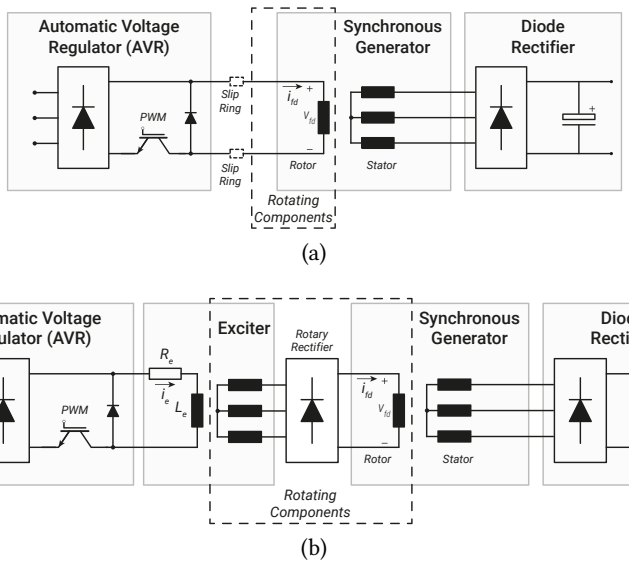


Fig. 5.4 One-quadrant automatic voltage regulator (AVR) combined with synchronous generator and diode rectifier: (a) direct excitation and (b) brushless excitation.

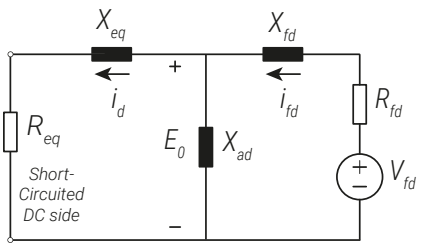


Fig. 5.5 D-axis equivalent circuit with short-circuited stator and field voltage.

Once the deexcitation is started, the internal stator voltage (E_0) is not constant. Thus, in (5.2), the internal voltage decrease in time should be considered to calculate the fault current more accurately. This phenomenon and the full analytical expression are described hereafter.

During the deexcitation of the excitation systems, the main exciter field voltage changes from its initial voltage (V_{fd0}) to zero with the time constant of the exciter (T_e). Thus, the change in the field voltage in s-domain can be expressed as

$$\Delta V_{fd}(s) = \frac{1}{1 + sT_e}\frac{V_{fd0}}{s} \tag{5.3}$$

Ideally, the time constant for the exciter should be zero for the direct excitation system, but it is not allowed to avoid the overvoltage in the circuit, and the AVR has the ramp rate limitation in practice [122]. The time constant should be, therefore, considered for the brushless excitation as well as for the direct excitation.

From the d-axis equivalent circuit shown in **Fig. 5.5**, the incremental field current (Δi_{fd}) during the short-circuit according to the change in the field voltage is

$$\Delta i_{fd}(s) = \frac{\Delta V_{fd}(s)}{R_{fd} + s\left(X_{fd} + \frac{X_{ad}X_{eq}}{X_{ad}+X_{eq}}\right)} = \frac{1}{1 + sT_d^{'}}\frac{\Delta V_{fd}(s)}{R_{fd}} \tag{5.4}$$

As shown in **Fig. 5.5**, the relationship between the field current and the d-axis current is

$$\Delta i_d(s) = \frac{X_{ad}}{\sqrt{{R_{eq}}^2 + \left(X_{eq} + X_{ad}\right)^2}}\Delta i_{fd}(s) = \frac{X_{ad}}{\sqrt{{R_{eq}}^2 + {X_d}^2}}\Delta i_{fd}(s) \tag{5.5}$$

By combining (5.3), (5.4), and (5.5), the change in the d-axis current in the time domain is

$$\Delta i_d(t) = [1 - F(t)]\frac{X_{ad}}{\sqrt{{R_{eq}}^2 + {X_d}^2}}\frac{V_{fd0}}{R_{fd}} = [1 - F(t)]\frac{E_0}{\sqrt{{R_{eq}}^2 + {X_d}^2}} \tag{5.6}$$

where

$$F(t) = u(-t + t_d) + u(t - t_d)\frac{T_d^{'}e^{-(t-t_d)/T_d^{'}} - T_e e^{-(t-t_d)/T_e}}{T_d^{'} - T_e}$$

and t_d is the time delay to activate the deexcitation after the fault instant.

Equation (5.6) shows that the change in the d-axis current during the deexcitation is the function of $F(t)$, and thus, by considering this function to the internal stator voltage, the fault current from the source is

$$i_D(t) = \sqrt{2}E_0\, Y(t)F(t)\sin(\omega t + \alpha - \phi) + \frac{\sqrt{2}E_0}{\sqrt{{R_{eq}}^2 + {X_d''}^2}}\sin(\alpha - \phi)e^{-\frac{t}{T_a}} \tag{5.7}$$

As mentioned earlier, the fault current flows from the positive rail to the negative rail with the one-third phase interval in case of the six-pulse rectifier. Thus, by removing the sinusoidal term in (5.7), the DC fault current (i_F) can be finally expressed as

$$i_F(t) = \sqrt{2}E_0\left(Y(t)F(t) + \frac{\sin(\alpha - \phi)}{\sqrt{{R_{eq}}^2 + {X_d''}^2}}e^{-\frac{t}{T_a}}\right) \tag{5.8}$$

5.2.4 Verification of the Analytical Expression

To verify the analytical expression derived, the DC fault currents and energies are calculated by (5.8) for four study cases, as presented in **Tab. 5.1**. The study cases consist of two different fault resistances (R_f = 1.3 Ω and R_f = 0.9 Ω) as well as exciter responses (T_e = 0.1 s and T_e = 1.0 s). The other parameters are commonly applied to avoid unnecessary or duplicative experimentation. Experimental tests for the same cases are also conducted with the test setup (see **Fig. 5.7**) and the test results are compared with the calculation values, as shown in **Fig. 5.6**.

In the analytical expression introduced, the first peak of the DC current, which is provided by the DC-link capacitor, is not considered and this makes some deviation between them. However, this does not represent a big issue in terms of the energy passing through the rectifier due to its very short duration. Rather than this, it is observed that the current deviation during the transient period develops the bigger energy difference because the deviation is squared and integrated in time.

Tab. 5.1 Parameters for analytical expression verification. The other parameters commonly applied to all the cases are: $\sqrt{2}E_0 = 500V$, $X_d = 9.8\Omega$, $X_d' = 1.1\Omega$, $T_d' = 0.12s$, and $t_d = 1.0s$.

Cases	R_{eq} (Ω)	T_e (s)	$Y(t)$	$F(t)$
Case 1	1.3	0.1	$\left(\frac{1}{\sqrt{1.3^2+1.1^2}} - \frac{1}{\sqrt{1.3^2+9.8^2}}\right)e^{-\frac{t}{0.12}} + \frac{1}{\sqrt{1.3^2+9.8^2}}$	$u(-t+1) + u(t-1)\left(\frac{0.12e^{-\frac{t-1}{0.12}} - 0.1e^{-\frac{t-1}{0.1}}}{0.12-0.1}\right)$
Case 2	1.3	1.0	$\left(\frac{1}{\sqrt{1.3^2+1.1^2}} - \frac{1}{\sqrt{1.3^2+9.8^2}}\right)e^{-\frac{t}{0.12}} + \frac{1}{\sqrt{1.3^2+9.8^2}}$	$u(-t+1) + u(t-1)\left(\frac{0.12e^{-\frac{t-1}{0.12}} - 1.0e^{-\frac{t-1}{1.0}}}{0.12-1.0}\right)$
Case 3	0.9	0.1	$\left(\frac{1}{\sqrt{0.9^2+1.1^2}} - \frac{1}{\sqrt{0.9^2+9.8^2}}\right)e^{-\frac{t}{0.12}} + \frac{1}{\sqrt{0.9^2+9.8^2}}$	$u(-t+1) + u(t-1)\left(\frac{0.12e^{-\frac{t-1}{0.12}} - 0.1e^{-\frac{t-1}{0.1}}}{0.12-0.1}\right)$
Case 4	0.9	1.0	$\left(\frac{1}{\sqrt{0.9^2+1.1^2}} - \frac{1}{\sqrt{0.9^2+9.8^2}}\right)e^{-\frac{t}{0.12}} + \frac{1}{\sqrt{0.9^2+9.8^2}}$	$u(-t+1) + u(t-1)\left(\frac{0.12e^{-\frac{t-1}{0.12}} - 1.0e^{-\frac{t-1}{1.0}}}{0.12-1.0}\right)$

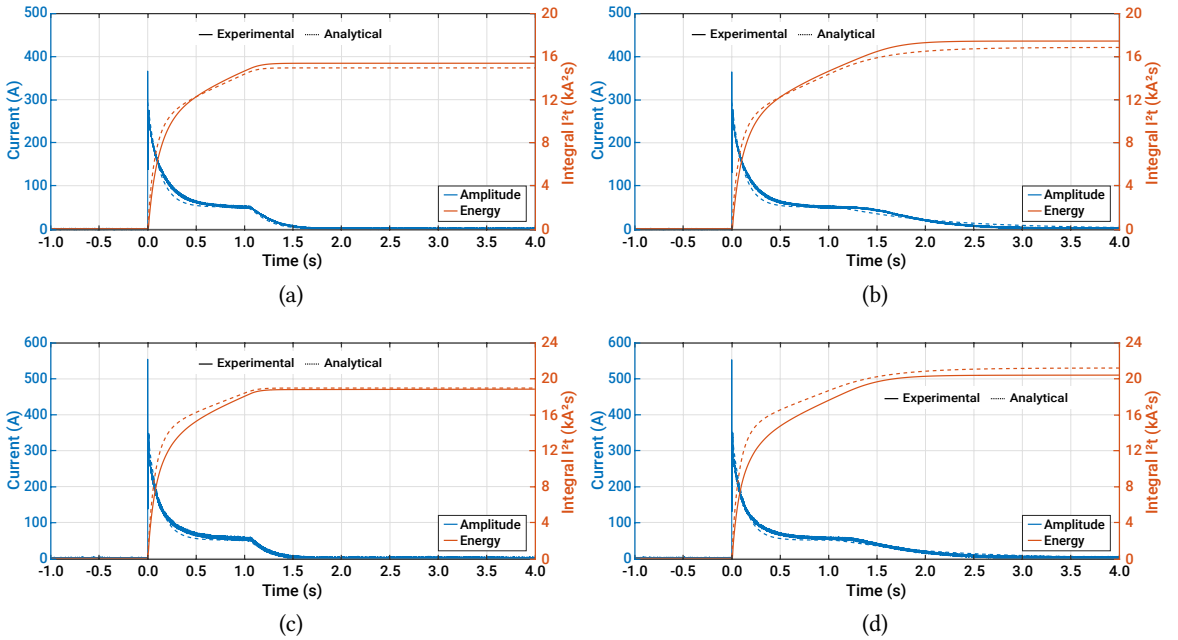


Fig. 5.6 Comparison of fault current and its energy between experimental results and analytical values calculated by (5.8): (a) Case 1, (b) Case 2, (c) Case 3, and (d) Case 4.

The comparison shows that although there are certain differences in the fault current and, more noticeably, in the energy, the equations introduced are reasonably matched with the test results. Hence, the equations could be used for the rectifier sizing and protection purpose.

5.2.5 Discussion on the Rectifier Sizing

During the conduction of one of the diodes, the peak current passing through the diode (i_{Dpeak}), which is the current from the generator, is equal to the peak current (i_{Fpeak}) when $\alpha - \phi = \pi/2$ and $t = 0$ in (5.8). Hence, the peak non-repetitive surge current of diodes (I_{FSM}) should be sized to sustain the peak fault current as

$$I_{FSM} \geq i_{Dpeak} = i_{Fpeak} = \frac{2\sqrt{2}E_0}{\sqrt{{R_{eq}}^2 + {X_d''}^2}} \tag{5.9}$$

By considering the worst condition ($R_{eq} = 0$) in (5.9), the diode should sustain the maximum current $i_{Fpeak-max} = 2\sqrt{2}E_0/X_d''$.

In case of the six-pulse rectifier, the amount of the energy passing through each diode is one-third of the energy of the DC fault current ($I^2 t_F$) due to the conduction interval. In addition, the time delay (t_d) adds the latency of the deexcitation. With these considerations, the diode has to have higher limiting load integral ($I^2 t_D$) than one-third of the maximum fault current energy ($\phi = \pi/2$) with the

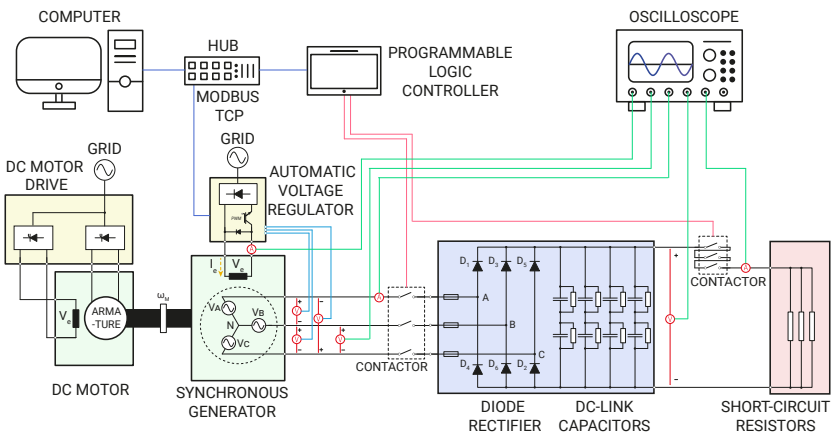
time delay as

$$I^2 t_D \geq \frac{1}{3}\int_0^{\infty} {i_F}^2(t)dt = \frac{2}{3}{E_0}^2 \int_0^{\infty} \left\{ Y(t)F(t) + \frac{1}{\sqrt{{R_{eq}}^2 + {X_d''}^2}} e^{-\frac{t}{T_a}} \right\}^2 dt \tag{5.10}$$

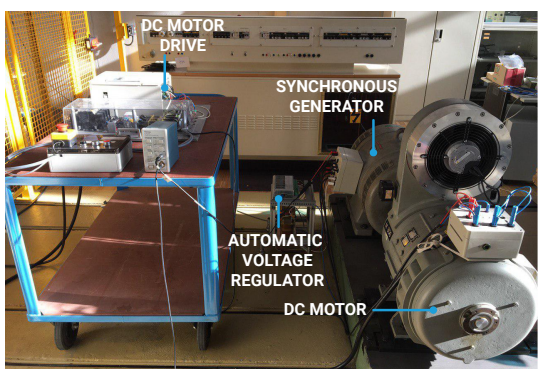
If the fault stresses are kept within the diode ratings specified in the manufacturer's datasheets, the diodes will remain operational after experiencing the fault event. It means that the diodes can endure a large number of the faults if the diodes are properly selected and thermal conditions are favourable, i.e., diodes are cooled down after the fault and before the new fault event [123].

5.3 Deexcitation Characteristics

Analytical calculations and experimental tests are conducted to characterize the DC short-circuit current under the deexcitation conditions. The system factors taken into account are: subtransient reactance (X_d''), fault resistance (R_f), DC-link capacitance (C_{DC}), exciter response (T_e), and time delay



(a)



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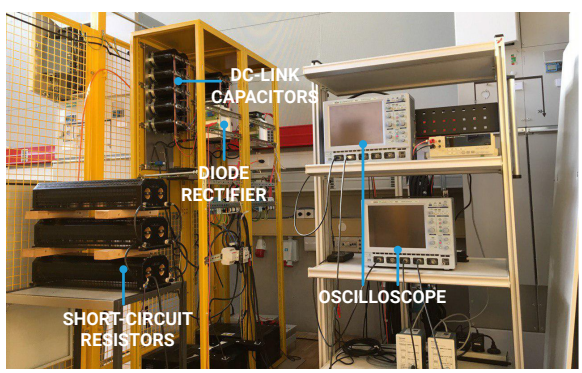


(c)

Fig. 5.7 Experimental test setup: (a) principal schematic, (b) actual implementation - generator side, and (c) actual implementation - rectifier and load side.

Tab. 5.2 Synchronous generator parameters used for DC short-circuit current calculation [124].

Parameters	Values
E_0	1 pu
ω	377 rad/s
T_d''; T_d'; and T_a	0.03 s; 1.5 s; and 0.15 s
X_d''; X_d'; X_d; and X_q''	0.22 pu; 0.28 pu; 1.0 pu; and 0.29 pu

(t_d). Note that per unit (pu) is used for the fault energy calculation because the relative value of the energy provides enough information on the fault characteristics.

5.3.1 Study Parameters and Test Setup

The parameters for the analytical studies are provided in **Tab. 5.2**. With these parameters, the DC fault currents and their energies are calculated for different system factors.

Furthermore, the deexcitation tests with the test setup of 10 kW and 500 V_{DC}, as presented in **Fig. 5.7**, are carried out under the short-circuited DC side with fault resistance. The test setup consists of a DC motor drive, a synchronous generator, a six-pulse diode rectifier with DC link capacitors, and resistors. The generator in the test setup has no damper winding (neglecting the subtransient dynamics) and is based on the direct excitation. Various exciter responses are, therefore, emulated by a programmable logic controller (PLC) [see **Fig. 5.7(a)**]. When the deexcitation is commanded, the PLC controls AVR output voltages with respect to given time constants.

Although the direct excitation system has fast response, it cannot immediately remove the excitation due to the AVR protection. Thus, the fastest excitation removal is tested and the time constant of 0.1 s (T_e = 0.1 s) is observed from the test result (see **Fig. 5.8**). T_e = 1.0 s is taken into account for the brushless excitation system. The excitation responses, which are commanded to turn-off immediately for the direct excitation and to regulate the excitation current with the time constant of 1.0 s for the brushless excitation, are shown in **Fig. 5.8**. There is a time delay associated with activating the

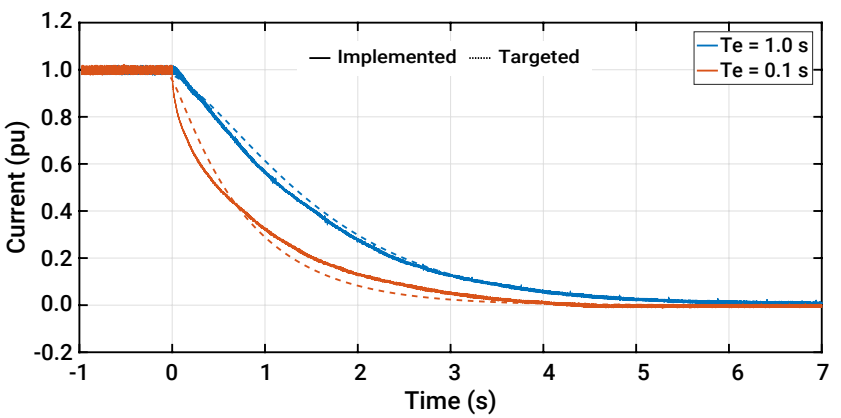


Fig. 5.8 Implemented excitation responses for direct (red, T_e = 0.1 s) and brushless (blue, T_e = 1.0 s) excitation systems.

deexcitation due to fault detection, post-processing, protection coordination, and so on. This time delay (t_d) is also replicated by the PLC.

5.3.2 DC Fault Behaviour

The DC short-circuit tests are performed in the test setup with the condition of C_{DC} = 2.3 mF and R_f = 0.9 Ω. In **Fig. 5.9**, general DC fault behaviours are seen considering that the DC fault current is composed of the current from the DC-link capacitor with the maximum amplitude of V_{DC}/R_{eq}, mainly contributing to the first peak, and the current contribution from the generator, which is important for the rectifier protection and can be recognized from the second peak in the DC fault current. On another point, the AC and DC currents are initially very high due to low transient reactance and turn into the steady-state with the reactance in this stage.

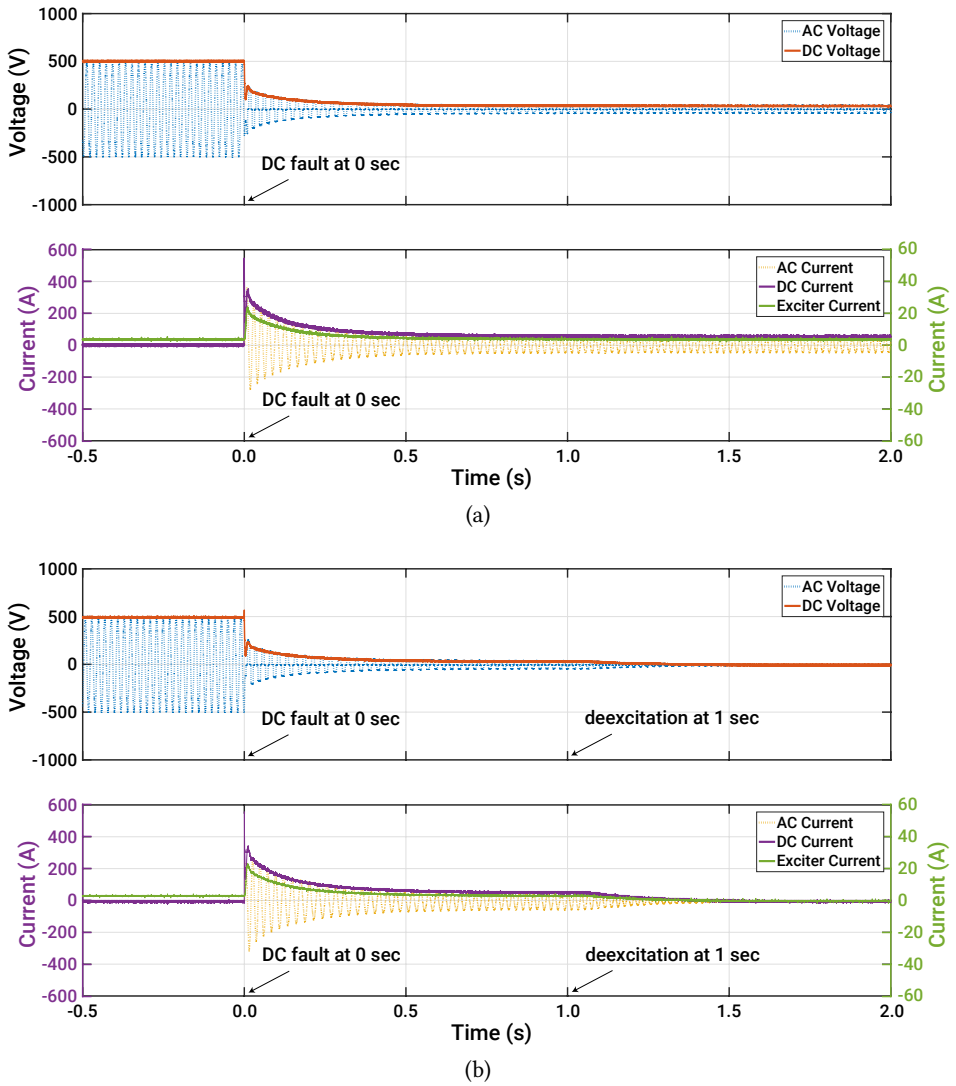


Fig. 5.9 DC short-circuit behaviour: (a) without deexcitation and (b) with deexcitation.

Similar to the current, the DC voltage is first dropped with the function of capacitance and inductance values, and then, the DC voltage is decided by the positive peak AC voltage varied with the generator dynamics. As mentioned earlier, the direct excitation system is used for the test. Hence, in the setup, the field current is the same as the exciter current and its transient behaviour is a linear function of the fault current (the d-axis current), as shown in **Fig. 5.9** and described in (5.5).

Furthermore, the effect of the deexcitation is investigated by conducting the DC short-circuit tests without and with the deexcitation. Although there is a steady-state short-circuit current without the deexcitation protection [see **Fig. 5.9(a)**], the current diminishes in time and then goes to zero with the protection by the deexcitation [see **Fig. 5.9(b)**].

5.3.3 Influence of Subtransient Reactance

In [26], a synchronous generator, specially designed to have high subtransient reactance (X_d''), is used to reduce the initial DC fault current. However, the effect of the subtransient reactance is not discussed concerning the fault energy in [26]. For this reason, the DC fault current and its energy by (5.8) are calculated for three subtransient reactance values: 0.22 pu, 0.11 pu, and 0.33 pu. Note that the experimental tests for the subtransient reactance are not conducted due to no damper winding in the machine.

Fig. 5.10 shows that the initial DC fault current can be minimized by employing the generator having a high value of the subtransient reactance. When the fault current reaches the transient period, there are no differences in the amplitude of the current. With this behaviour, the fault energy gaps among the three cases become larger during the subtransient period and then the gaps are maintained for the other periods. By the consideration of a short subtransient time constant (T_d''), it can be stated that the high subtransient reactance is effective to protect the diode in terms of the peak non-repetitive surge current (I_{FSM}), while its contribution to the diode protection is not high in terms of the limiting load integral (I^2t_D).

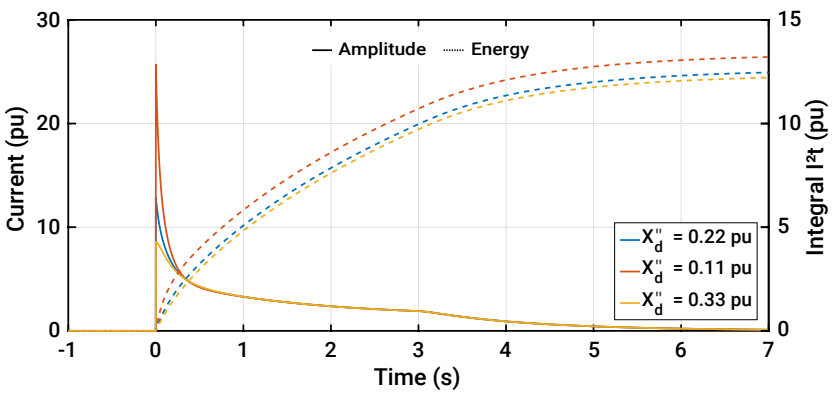


Fig. 5.10 Fault current behaviour under different subtransient reactances. Note that the analytical calculations are only provided due to the limitation of the physical machine.

5.3.4 Influence of Fault Resistance

While the bolted DC line-to-line short-circuit occurs in the system, the fault resistance cannot be zero. The fault comes with the arc and the fault resistance is a function of the arc length and the current [108]. The DC fault can, therefore, occur with different fault resistance values depending on

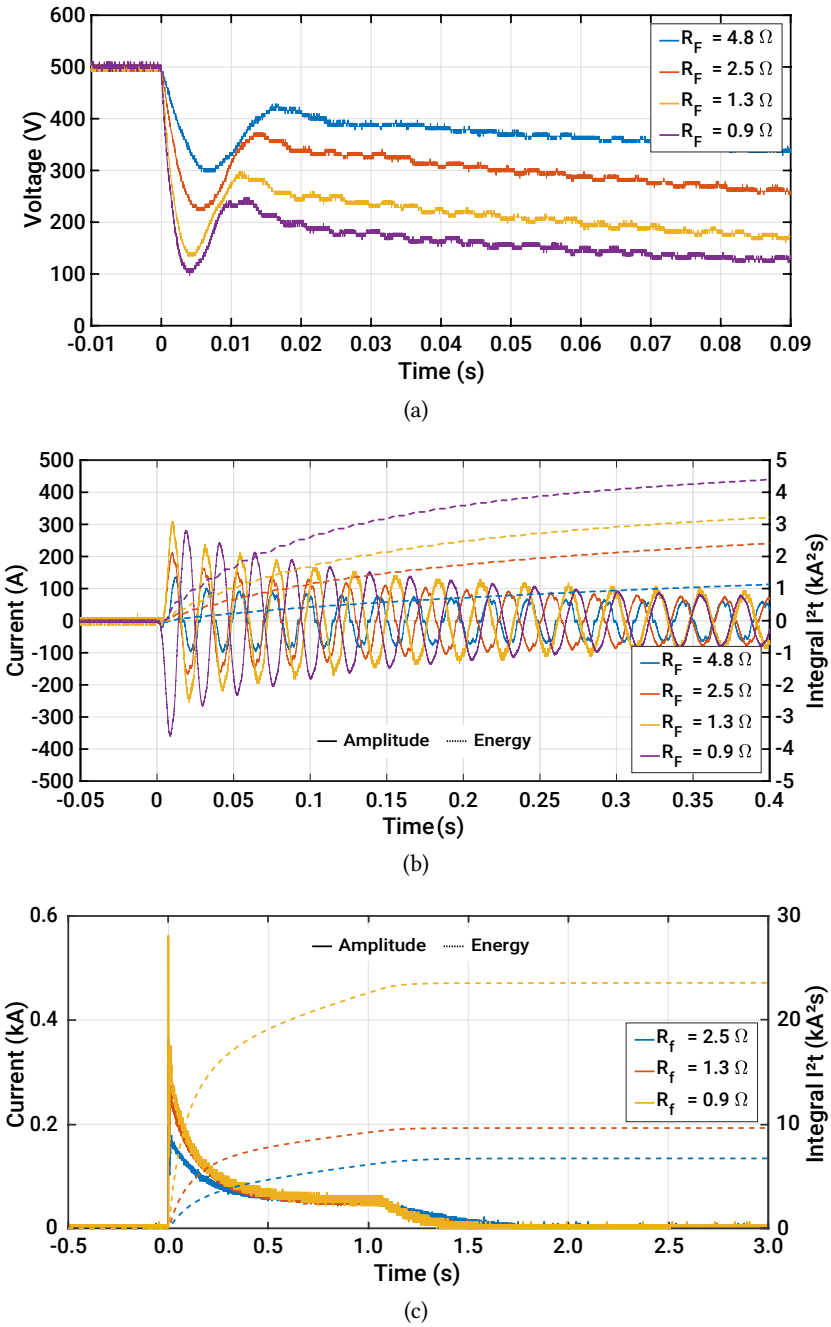
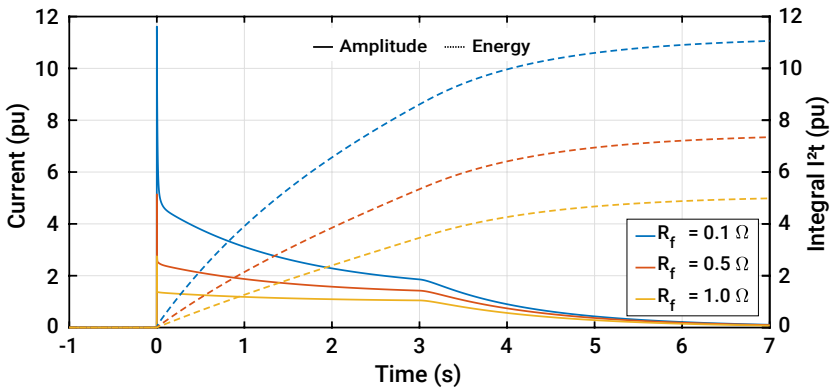


Fig. 5.11 Fault behaviour under different fault resistances: (a) DC voltages tested, (b) AC currents tested, (c) DC currents tested, and (d) DC currents calculated.



(d)

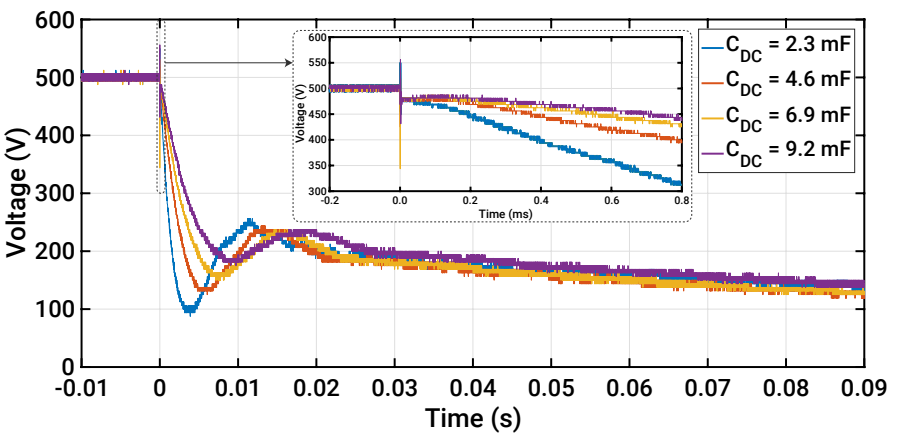
Fig. 5.11 Fault behaviour under different fault resistances: (a) DC voltages tested, (b) AC currents tested, (c) DC currents tested, and (d) DC currents calculated.

system conditions. For the analyses of the fault resistance influence, the DC short-circuit currents are calculated and tested for different fault resistances: analytical approach - 0.1 Ω, 0.5 Ω, and 1.0 Ω; and experimental approach - 0.9 Ω, 1.3 Ω, and 2.5 Ω.

As shown in **Fig. 5.11(c)**, the fault resistance gives the impacts on the fault current for the whole period. Low fault resistance causes high DC fault current and this makes a huge difference in the fault energy, as expected. This trend is also observed in **Fig. 5.11(d)**.

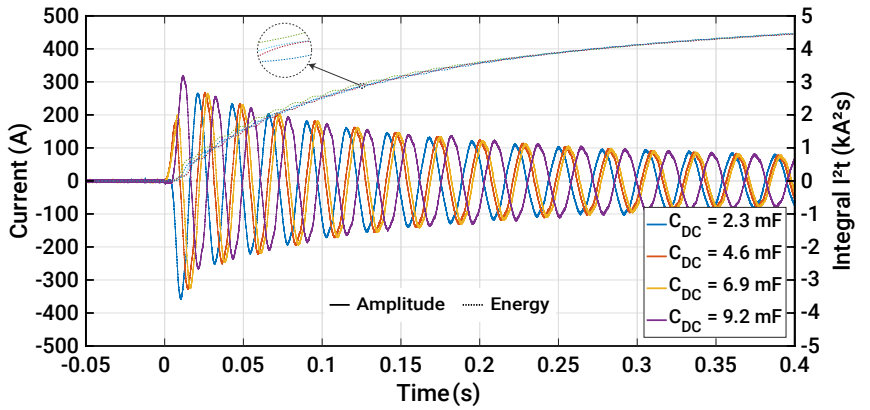
5.3.5 Influence of DC-link Capacitance

The DC-link capacitor, which is a part of the rectifier, not only helps to mitigate the voltage ripple but also plays a role in the inertia in DC PDNs. The capacitor values are different depending on system voltage, power rating, requirement, control, and so on. In order to examine the effect on the capacitor

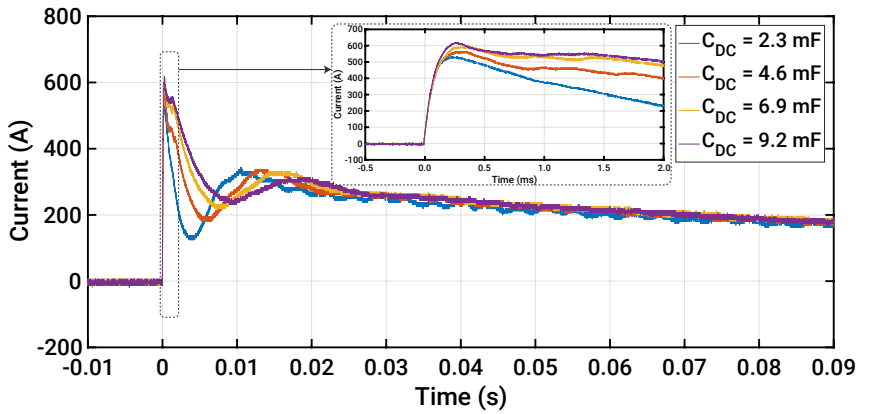


(a)

Fig. 5.12 Fault behaviour under different capacitances: (a) DC voltages, (b) AC currents, and (c) DC currents. Note that the test results are only provided because the effect of the DC-link capacitance is not considered in the analytical expression [see (5.8)].



(b)



(c)

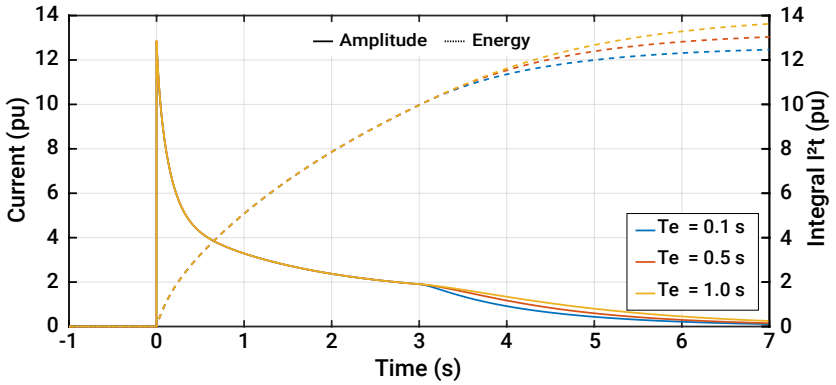
Fig. 5.12 Fault behaviour under different capacitances: (a) DC voltages, (b) AC currents, and (c) DC currents. Note that the test results are only provided because the effect of the DC-link capacitance is not considered in the analytical expression [see (5.8)].

value, DC short-circuit tests are carried out with four capacitor values by connecting or disconnecting the capacitors in **Fig. 5.7(c)**: 2.3 mF, 4.6 mF, 6.9 mF, and 9.2 mF.

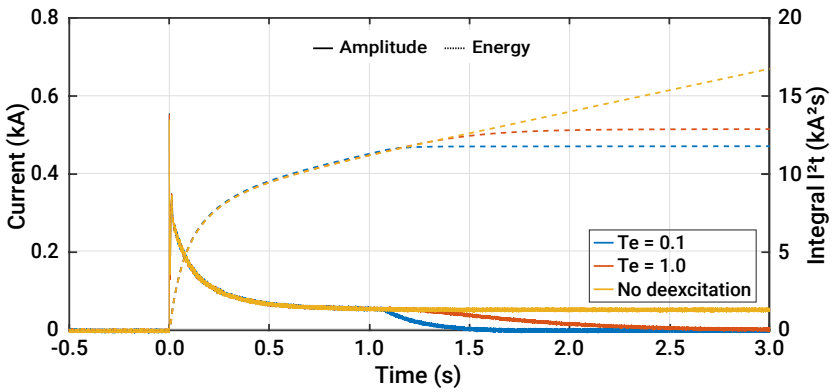
The test results show that the higher capacitor value comes with a lower voltage drop and a higher DC fault current [see **Fig. 5.12(a)** and **Fig. 5.12(c)**], as expected. Otherwise, the amplitude of the AC current is difficult to compare because its first peak is dependent on the instant of the short-circuit making. For further discussion, the energies for the four test conditions are provided and compared in **Fig. 5.12(b)**. This comparison gives important information. The influence of the capacitor value is small enough to be negligible in terms of the fault energy passing through the rectifier. Thus, while capacitor banks installed in DC PDNs have a direct impact on the developed short circuit current peaks, they are not a crucial element for rectifier sizing, e.g., diode selection is the analyzed case.

5.3.6 Influence of Different Exciter Types

Depending on exciter type, the deexcitation characteristics are different. In the study, the direct and brushless excitation systems are analyzed with different exciter time responses: analytical approach -



(a)



(b)

Fig. 5.13 Fault current behaviour under different exciter responses: (a) analytical calculations and (b) experimental tests.

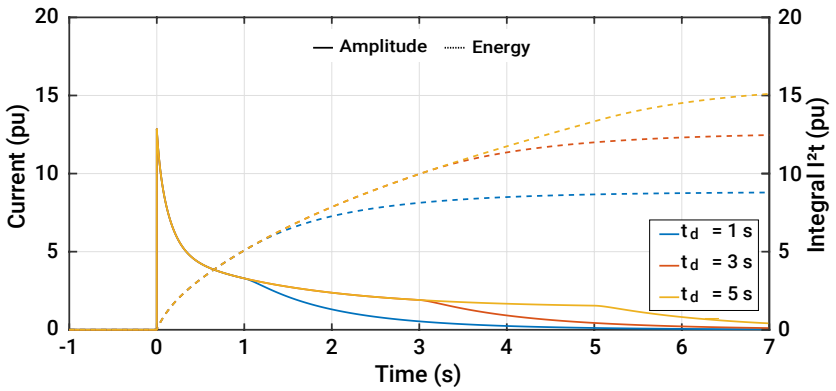
0.1 s, 0.5 s, and 1.0 s; and experimental approach - 0.1 s (the direct excitation case), 1.0 s (the brushless excitation case), and no deexcitation.

When the deexcitation is activated at 3 s in **Fig. 5.13(a)** and at 1 s in Fig. **Fig. 5.13(b)**, the rate of rise of fault energies becomes lower with their time constants. **Fig. 5.13** shows that the lower time constant assists to mitigate the fault energy. In the study cases tested, the fault energies are 11.8 kA^2t and 12.9 kA^2t for the direct and brushless excitation systems, respectively. This implies that the rectifier for the brushless excitation should have around 10 % higher overloading capability than the direct excitation in the study condition.

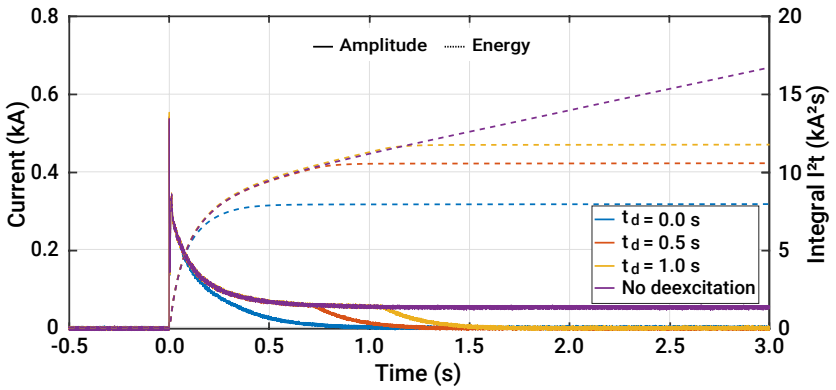
5.3.7 Influence of Time Delay

The deexcitation cannot immediately be activated after the fault. There are certain time delays for fault detection, fault localization, post-processing, protection coordination, and so on. This time delay associated with the deexcitation activation is studied for different time delays: analytical approach - 1 s, 3 s, and 5 s; and experimental approach - 0 s, 0.5 s, 1.0 s, and no deexcitation.

The study results (see **Fig. 5.14**) demonstrate that the time delay is also an important factor to increase



(a)



(b)

Fig. 5.14 Fault current behaviour under different time delays: (a) analytical calculations and (b) experimental tests.

the fault energy. The less time delay mitigates the fault energy. Hence, this time delay should be considered for the rectifier design, as described in (5.10).

5.4 Conclusion

This chapter has presented the comprehensive study results on the protection method by the deexcitation of the generator combined with the diode rectifier. The analytical expressions for the deexcitation are introduced and, from the analytical expression, the rectifier sizing is discussed in terms of the peak fault current and its energy. The experimental tests are carried out and discussed for different subtransient reactances, fault resistances, DC-link capacitances, exciter types, and time delays.

The DC fault characteristics and analytical expressions under the deexcitation, which are described with the consideration of the generator dynamics and the deexcitation, are verified with the test results. This implies that the introduced analytical expressions can be used for developing the protection scheme and dimensioning the rectifier.

The analysis results provide important information: high subtransient reactance is effective to reduce the initial DC fault current, but the effect of the fault energy mitigation is not high due to the short

subtransient period; low fault resistance develops high DC fault current, while the resistance is not controllable in practice; DC-link capacitance only has a direct impact on the first peak DC fault current developed and it is not a crucial element for the rectifier sizing; and faster exciter response and less time delay help to mitigate the fault energy. From these findings, it could be concluded that the system factors studied should be considered for the rectifier sizing and protection.

6
Demonstration of Flexible DC Power Distribution Network Operations

This chapter demonstrates flexible operating modes of two-bus DC power distribution networks, consisting of two generators operated at different frequencies. First, automatic DC voltage regulation of each power supply is verified by step-load changes. Secondly, power sharing function is implemented and validated with two different tests. Lastly, two operating modes for the DC power distribution networks are demonstrated with new functions of the solid-state bus-tie switch: soft start - smoothly charging bus potential to the nominal level; and seamless transition - promptly supplying electric power to the bus experienced a power outage during the open-bus operation.

6.1 Introduction

In AC PDNs, synchronous generators have to be synchronized to the networks when they are interconnected. For the synchronization, four factors to be matched are phase sequence, voltage magnitude, frequency, and phase angle [125]. By contrast, the only factor to be considered is the voltage magnitude in DC PDNs. In other words, the other three factors can be ignored for the interconnection of DC PDNs because they are characteristics of the AC systems. As described in **Chap. 1**, this makes variable-speed generators possible to be employed in DC PDNs. Furthermore, there are a lot of freedom to select generator types: high-speed generators to achieve a higher power-to-volume ratio; and generators with different frequencies to improve the flexibility in system design. While it is fully available in theory, this flexibility in the generator selection should be proven in practice with hardware demonstration.

Bus-tie switches built with solid-state technologies play an important role in system protection of marine LVDC PDNs, as analyzed in **Chap. 2**. The bus-tie switch is used for the bus separation in the range of several tens of microseconds. It allows for promptly clearing DC faults and avoiding converter damages with enough time discrimination margins among the three protection actions. This active device also opens new chances in system operations: soft start - smoothly charging bus potential to the nominal level; and seamless transition - promptly supplying electric power to the bus experienced a power outage during the open-bus operation.

As mentioned above, the voltage levels between DC buses should be matched for the bus interconnection. In a conventional concept, the voltages of the two buses should be at the nominal value and then the bus-tie switch can connect the buses. However, there may be a situation that one bus is fully energized (at the rated voltage level), and the other is deenergized (e.g., following fault and its clearance) and needed to be energized again, without activation of the prime generators. This can

be achieved through the bus-tie switch if its topology allows for smoothly transferring energy from one bus to the other (called soft start in the work). With this bus-tie switch function, PDNs become more flexible, e.g., supplying electric power to the bus in which no electric source is available due to system design, operating mode (one generator operating mode), or machine failure.

On the other hand, the ultra-fast bus-tie switch also allows for the seamless transition of system configuration. An interchange between self-sustained (open bus) and interconnected (closed bus) operations can be achieved with a low system impact if the voltage levels are matched. Furthermore, there may be a case that an electric source in one of the buses is out of service during the open-bus operation, it may cause voltage drop, followed by all load trips with the undervoltage protection of inverters. In this case, the loads experienced the power outage can be powered without the trips by promptly connecting the bus to the other healthy bus (called seamless transition in the work).

With the above reasons, this chapter demonstrates flexible operating modes of two-bus DC PDNs, consisting of two generators operated at different frequencies. First, automatic DC voltage regulation of each power supply is verified by step-load changes. Secondly, power sharing function is implemented and validated with two different tests. Lastly, two operating modes for the DC PDNs are demonstrated with new functions of the solid-state bus-tie switch: soft start and seamless transition.

6.2 Hardware Test Setup

This section describes hardware components of the test setup. The test setup is composed of two DC motor-synchronous generator sets, two rectifier systems, a solid-state bus-tie switch, busbars, and resistors, as shown in **Fig. 6.1**. Each component is described hereafter.

6.2.1 DC Motor-Synchronous Generator Set

In DC PDNs, any frequency of AC is rectified to DC and this gives the flexibility in the selection of generator frequency of a generator voltage, depending on pole pairs of a generator and mechanical

Tab. 6.1 Ratings of DC motor-synchronous generator set.

Components	Ratings	DC Motor-Generator Set 1 (GEN1)	DC Motor-Generator Set 2 (GEN2)
DC motor drive	Output power	10.75 kW	63.05 kW
	Output voltage	430 V	485 V
	Output current	25 A	130 A
DC motor	Output power	15 kW	38.7 kW
	Nominal voltage	380 V	440 V
	Rated current	40 A	98 V
	Rated speed	1500-3000 rpm	1500-3000 rpm
Synchronous generator	Output power	25 kVA	25 kVA
	Nominal voltage	380 V	380 V
	Rated current	38 A	38 A
	Rated speed	1500 rpm	1500-3000 rpm
	Rated frequency	50 Hz	200-400 Hz

shaft speed. To demonstrate the flexibility in the frequency, two different generator sets are utilized in the test setup: GEN1 - 10.75 kW, 380 V, operated at fixed 50 Hz; and GEN2 - 25 kVA, 380 V, operated with variable frequency in the range of 200-400 Hz. The ratings of the components in the test setup are summarized in **Tab. 6.1**.

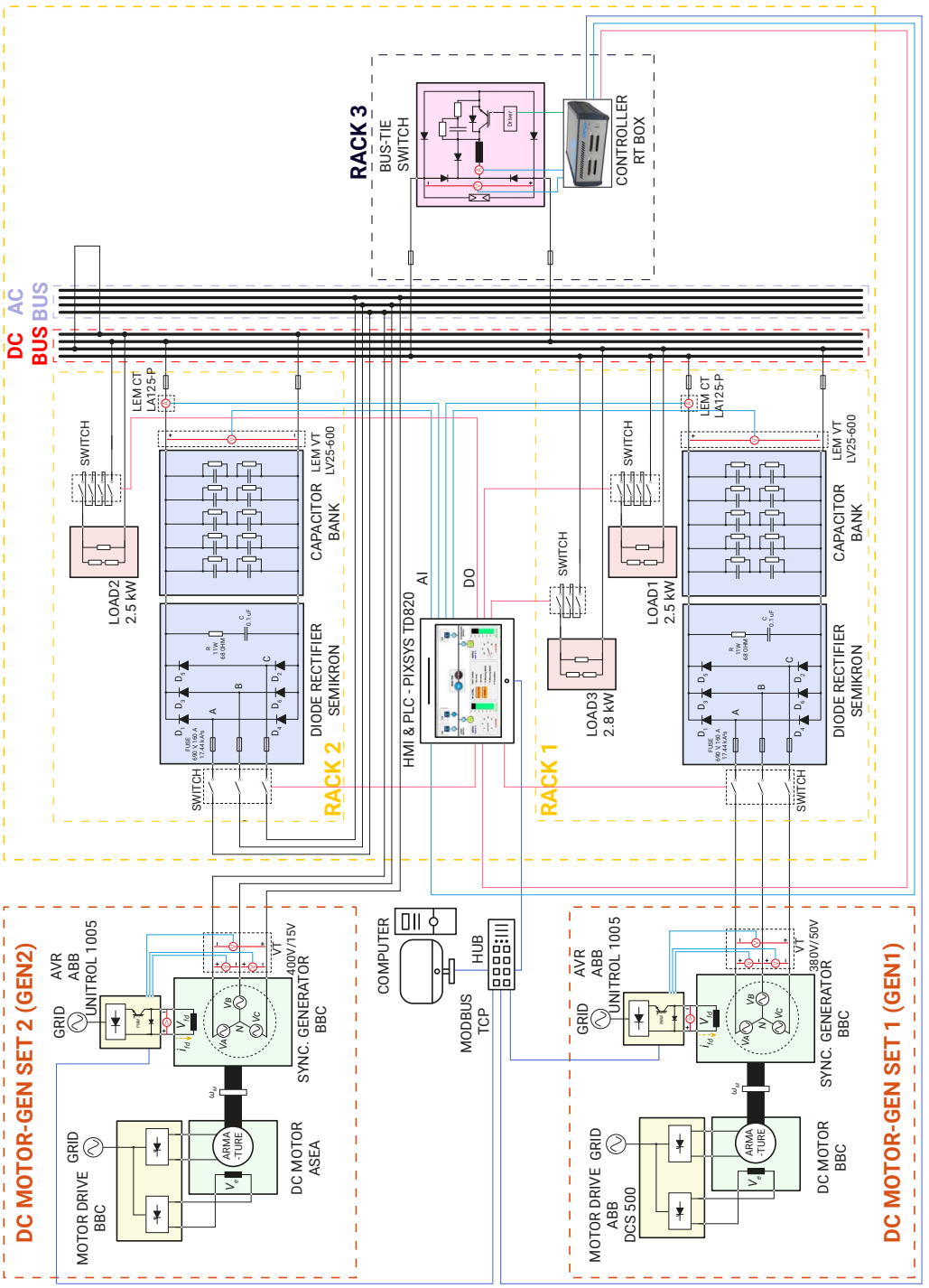
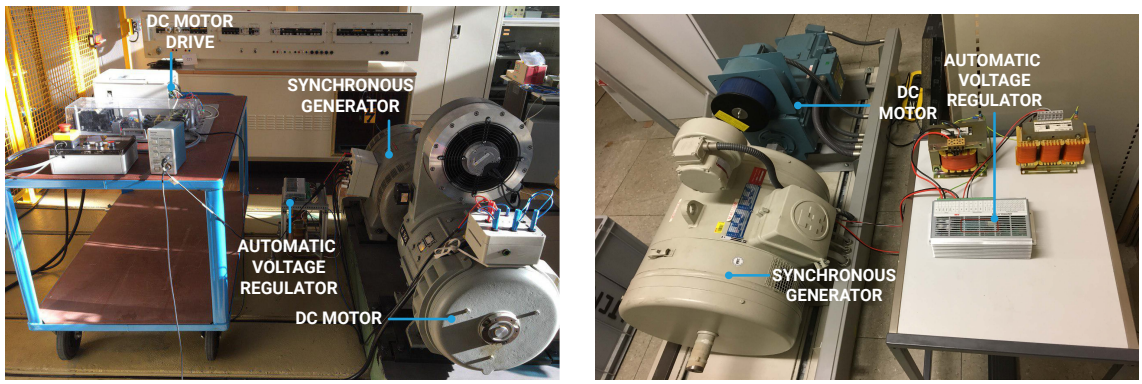


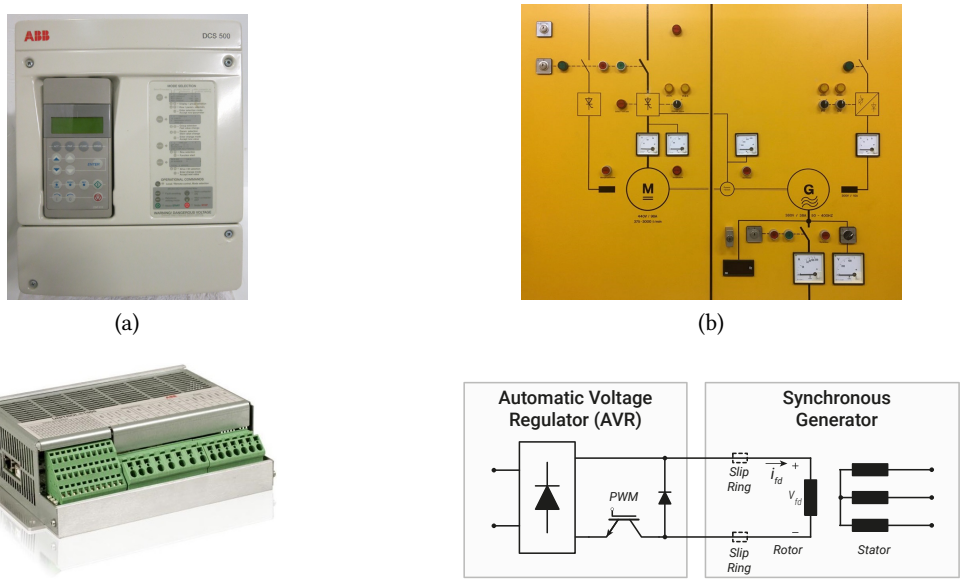
Fig. 6.1 Detailed schematic diagram of test setup.



(a) (b)

Fig. 6.2 DC motor-synchronous generator sets: (a) GEN1 and (b) GEN2.

The first set of the DC motor-synchronous generator (GEN1) consists of a DC motor drive, a DC motor, a synchronous generator, and an AVR, as shown in **Fig. 6.2(a)**. To emulate a prime mover in marine systems, i.e., diesel engine, typically found on a ship, the DC motor is driven by the ABB DCS 500 that is a thyristor power converter and includes a converter module and a field exciter module [see **Fig. 6.3(a)**]. The motor drive regulates the field current and the rotational speed of the DC motor with the functions of constant field control and speed control, respectively. The power rating of GEN1 is the same as the drive power rating of 10.75 kW, available in the laboratory, because it has the lowest power rating in the set. The generator terminal voltage is regulated by the ABB Unitrol 1005 [see **Fig. 6.3(c)**] that is an one-quadrant AVR based on the DC chopper, consisting of a DC input voltage source and a controllable switch. A schematic diagram of the AVR and synchronous generator integration is shown in **Fig. 6.3(d)**.



(a) (b)

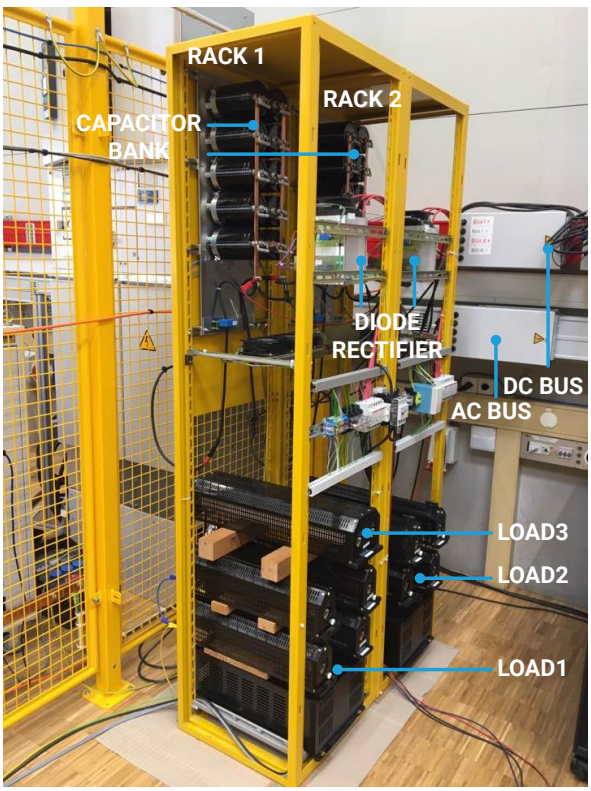
(c) (d)

Fig. 6.3 (a) DCS 500 [126], (b) DC power supply for driving the DC motor of GEN2, (C) Unitrol 1005 [122], and (d) AVR-generator diagram.

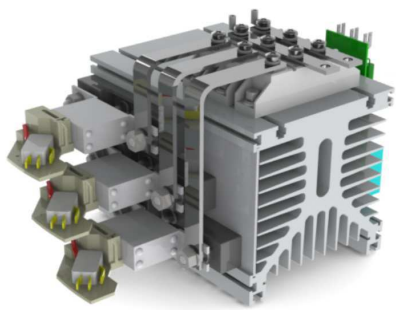
As shown in **Fig. 6.2(b)**, while the configuration of the second set (GEN2) is the same to the first set (GEN1), the power and frequency ratings of GEN2 are different with those of GEN1. In GEN2, a BBC thyristor power converter that is a part of laboratory facilities [see **Fig. 6.3(b)**] drives the DC motor with the rotational speed of 1500-3000 rpm and the synchronous generator of 16 poles produces AC power with output frequency ranges of 200-400 Hz. The Unitrol 1005 is also used to regulate the AC voltage of GEN2.

6.2.2 Rectifier Systems

A three-phase six-pulse diode rectifier [SEMIKRON SKKD 100/16, see **Fig. 6.4(b)**] is employed to each generator set for the rectification. An oversized diode rectifier (670 V and 91 A) is selected to conduct various tests, including short-circuit tests. **Fig. 6.4(c)** shows DC-link capacitors installed at the terminals of the rectifier. Two capacitors are installed in series to handle the DC voltage of 500 V and the capacitance of a pair of the capacitors is 2.3 mF. Five pairs of the capacitors are mounted on the steel plate to change the DC-link capacitance from 2.3 mF to 11.5 mF by manually connecting or disconnecting the cooper bars in the middle of the pairs. The rectifier systems assembled in the racks are presented in **Fig. 6.4(a)**.



(a)



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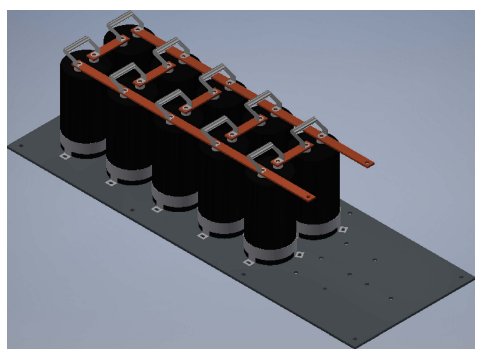


(c)

Fig. 6.4 (a) Rectifier systems assembled in the racks, (b) SEMIKRON diode module [127], and (c) DC-link capacitors.

6.2.3 Solid-State Bus-Tie Switch

As one of the key protection components, a solid-state bus-tie switch developed in the work of [128], available in the laboratory, is integrated into the test setup. The bus-tie switch has the following ratings:

- Nominal voltage: 600 V
- Rated current: 50 A
- Trip current: 100 A
- Maximum allowed current: 200 A

The switch topology is based on a four-quadrant switch configuration [four diodes (D_1, D_2, D_3, and D_4) and one IGBT module (S)] combined with a transient current limiting reactor (L_{lim}) and a freewheeling diode (D_L) in series to the IGBT module, as shown in **Fig. 6.5**. An RC snubber and metal oxide varistors (MOVs) are added to suppress transient overvoltages during the interruption.

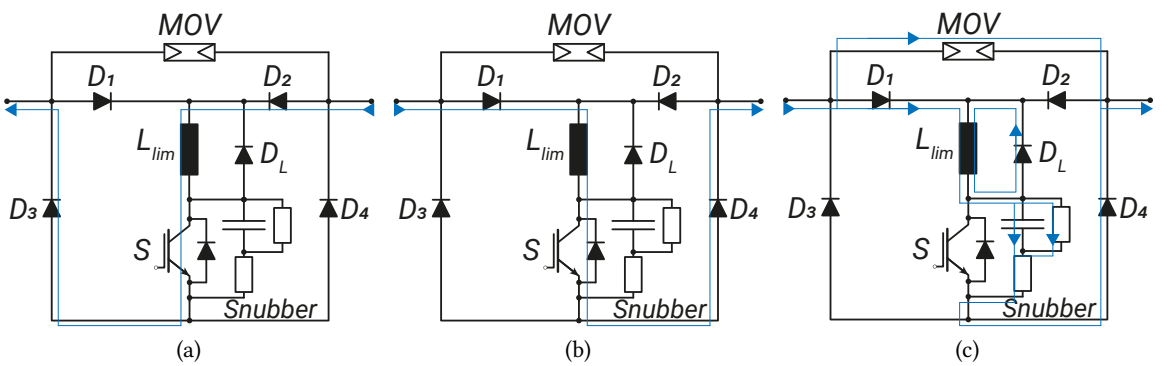


Fig. 6.5 Operational principle of solid-state bus-tie switch: (a) current path in normal operation with right-side supply, (b) current path in normal operation with left-side supply, and (c) current path in right-side fault condition after the IGBT is turned *OFF*.

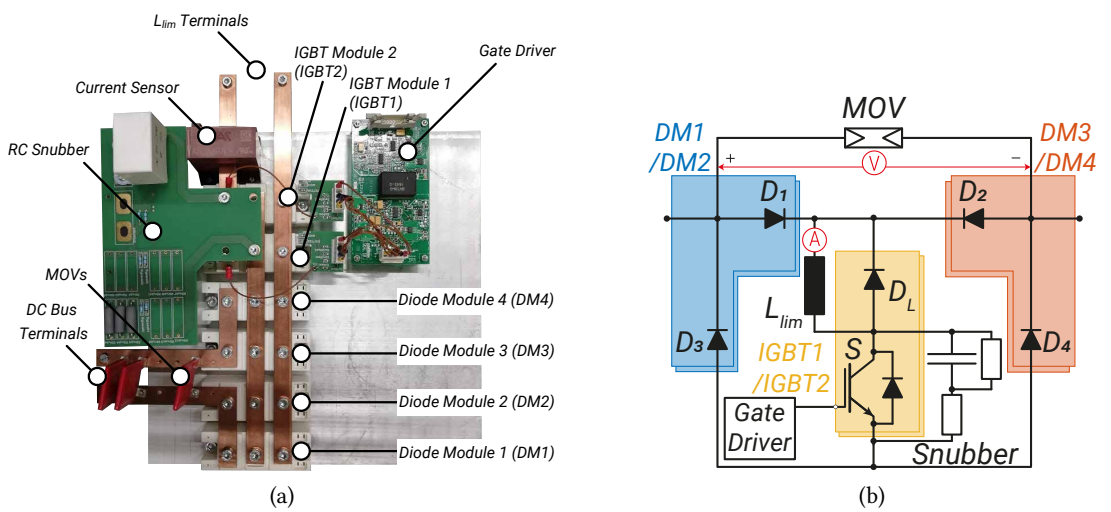


Fig. 6.6 Solid-state bus-tie switch assembly [128]: (a) actual implementation and (b) schematic diagram. A voltage sensor and a current limiting reactor are not shown in **Fig. 6.6(a)** as they are external components.

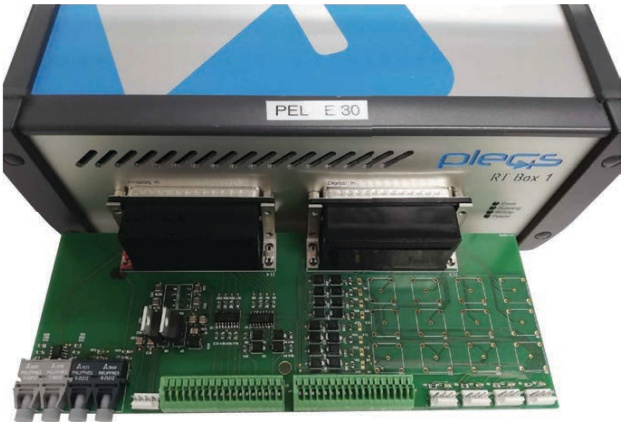
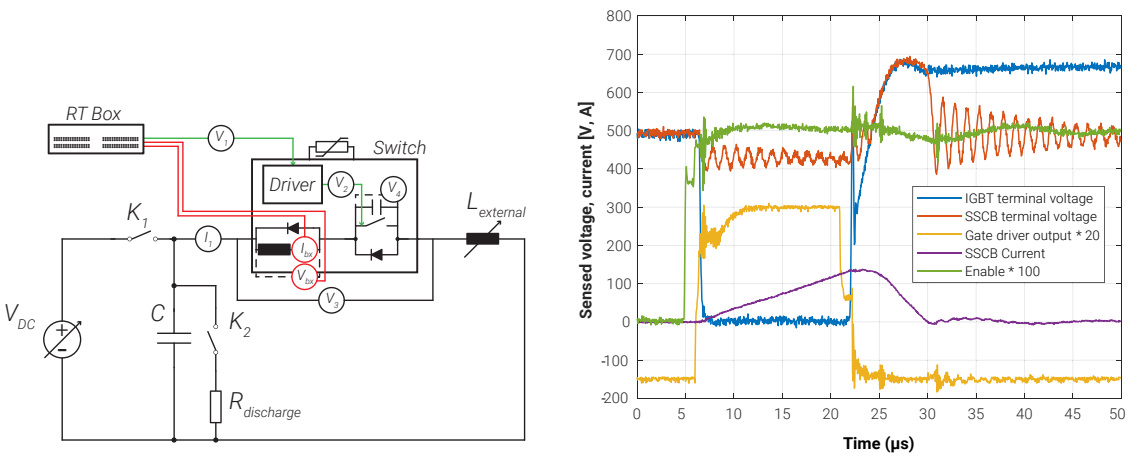


Fig. 6.7 PLEXIM RT Box with an interface board of the bus-tie switch [128].

Fig. 6.5 also provides the operational principle of the bus-tie switch with current paths. The right-side supply forces to flow the current through D_2, L_{lim}, S, and D_3 if the IGBT is the *ON*-state [see **Fig. 6.5(a)**]. For the left-side supply, the current direction is the opposite [see **Fig. 6.5(b)**]. The IGBT module is first turned *OFF* in the event of a fault. This forces the overcurrent to flow through the snubber circuit and the MOVs [see **Fig. 6.5(c)**]. The energies stored in the current limiting reactor and the system stray inductance are dissipated by the diode of D_L and the MOVs, respectively, until the interruption is terminated.

The assembled bus-tie switch is presented in **Fig. 6.6(a)**. On top of the heatsink, the mounted components are four diode modules, two IGBT modules, a gate driver, a PCB-based RC snubber circuit, MOVs, and a current sensor. Note that the current limiting reactor and the voltage sensor are externally connected. To increase overcurrent withstand capability, two modules are installed in parallel for the left-side diodes (D_1-D_3), the right-side diodes (D_2-D_4), and the diode-IGBT modules (D_L-S), as shown in **Fig. 6.6(b)**.



(a) (b)

Fig. 6.8 Performance of the solid-state bus-tie switch [128]: (a) switching test circuit and (b) test result.

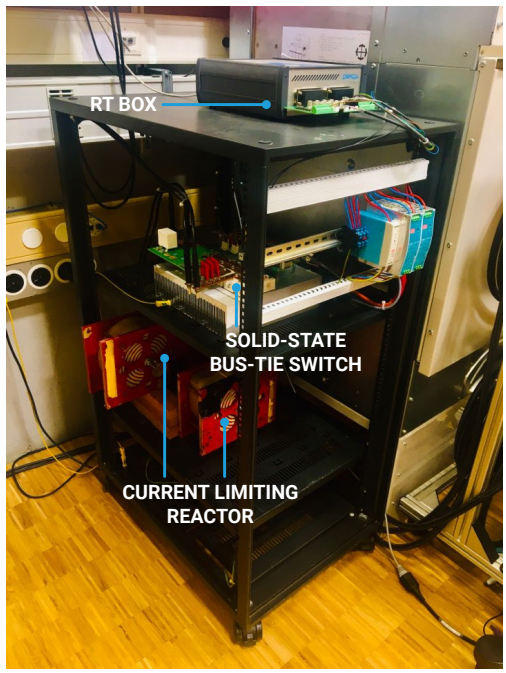


Fig. 6.9 Solid-state bus-tie switch integration.

The control function of the bus-tie switch is implemented in PLEXIM RT Box that can be used either as a real-time simulator or a rapid prototyping controller [129]. The controller uses the voltage and current information provided by the interface board and automatically sends the trip signal to the gate driver if the current magnitude and its rate are higher than preselected threshold values. The PLC that is a central controller in the setup acquires the voltage and current information and controls the bus-tie switch via an analogue/digital input/output module, as illustrated in **Fig. 6.1**.

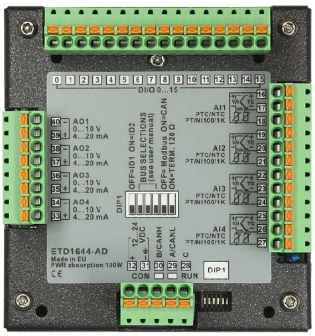
In **Fig. 6.8**, one experimental result is provided to introduce the performance of the bus-tie switch. First, the DC power supply charges the capacitor (C) and it is disconnected if the capacitor voltage becomes the test voltage. At 5 μs in **Fig. 6.8(b)**, the RT Box sends the command to close the switch and this makes the closed loop of the test circuit. When the current reaches the threshold value of 100 A, the switch starts to interrupt the current. Total clearing time under the test conditions is about 15 μs. This result shows that the solid-state bus-tie switch can autonomously detect and clear a fault within several tens of microseconds, and the time delay between the detection and the interruption is observed as approximately 5.5 μs.

As a part of the test setup, the bus-tie switch and the RT Box are installed in the rack with its power supply and control circuit, as shown in **Fig. 6.9**.

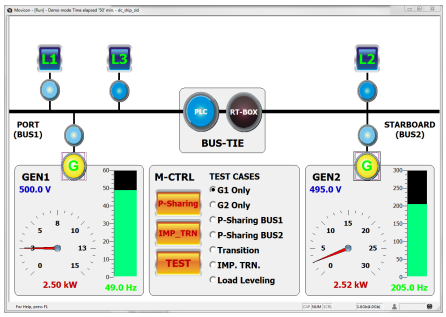
6.2.4 Programmable Logic Controller

A central controller of the test setup is implemented with Pixsys TD820 [a human-machine interface (HMI) panel with an integrated PLC] and two ETD1644 modules (analogue/digital input/output modules), installing at the backside of the HMI panel. As depicted in **Fig. 6.1**, the PLC communicates with the AVRs and the computer via MODBUS TCP communication. Analogue inputs and digital

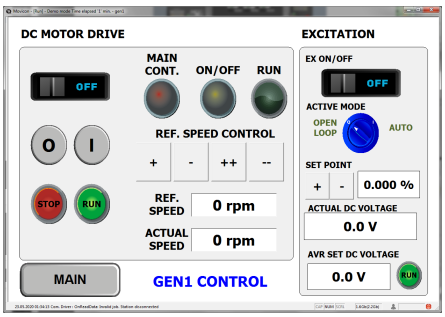
(a)



(b)



(c)



(d)

Fig. 6.10 (a) TD820 HMI panel [130], (b) ETD 1644 module [131], (c) main HMI screen, and (d) HMI screen for voltage control.

outputs of the PLC are used to acquire analogue voltage and current information and to control the switches for the loads, respectively. The implemented HMI screens for the main control and the voltage control of each generator are shown in **Fig. 6.10(c)** and **Fig. 6.10(d)**.

6.3 Two-Bus DC System Control

System control is necessary to demonstrate various operating modes selected in the study. The realized system controls in the test setup are DC voltage regulation, power sharing control, soft start, and seamless transition.

6.3.1 DC Voltage Regulation

A DC voltage regulation is an important function of DC PDN control to maintain a constant DC output voltage against system disturbances and load changes. In the test setup, the regulation function is realized with the combination of the PLC and the AVR. The utilized AVR (Unitrol 1005) is for AC networks, i.e., lack of the DC regulation function, and thus the PLC is combined to provide an AC reference corresponding to the DC voltage error, as shown in **Fig. 6.11**.

The PLC (TD820) acquires the DC voltage information and calculates the voltage error. The new AC voltage reference is sent from the PLC to the AVR via MODBUS TCP communication. The AVR finally

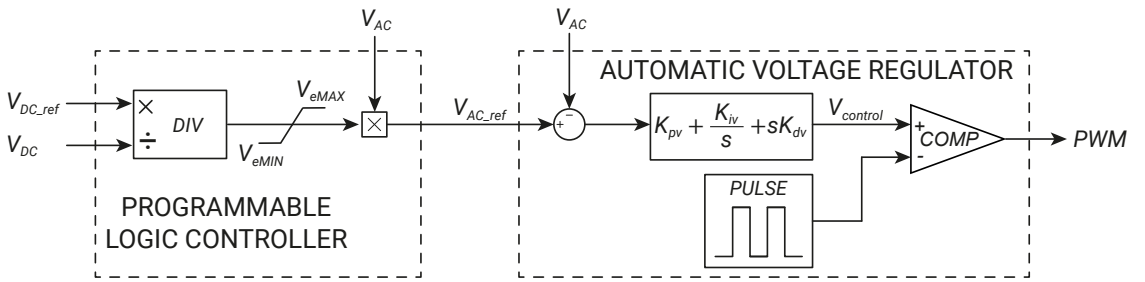


Fig. 6.11 Block diagram of DC voltage control.

Tab. 6.2 Parameters for DC voltage regulation.

Parameters	V_{eMAX}	V_{eMIN}	K_{pv}	K_{iv}	K_{dv}
GEN1	1.05	0.95	20	10	2
GEN2	1.05	0.95	20	5	4

regulates the AC generator terminal voltage with its PID controller. The parameters used for both generator sets are shown in **Tab. 6.2**.

6.3.2 Power Sharing Control

The two generators in the setup have to share loads in proportion to their power rating. Without the power sharing control, the two generators equally take a half of loading power if the two voltage levels are the same, while the power rating of GEN2 is 2.5 times higher than that of GEN1.

In general, current- or power-based DC voltage droop control has been proposed and employed to provide the power sharing function in DC PDNs. In case of the current-based DC voltage droop control, source resistance is virtually added to generate the slope of droop characteristic. It is possible to control the load distribution between multiple generators by selecting different virtual resistances, i.e., higher virtual resistance should be considered for the generator with the lower power rating, and vice versa, as shown in **Fig. 6.12**.

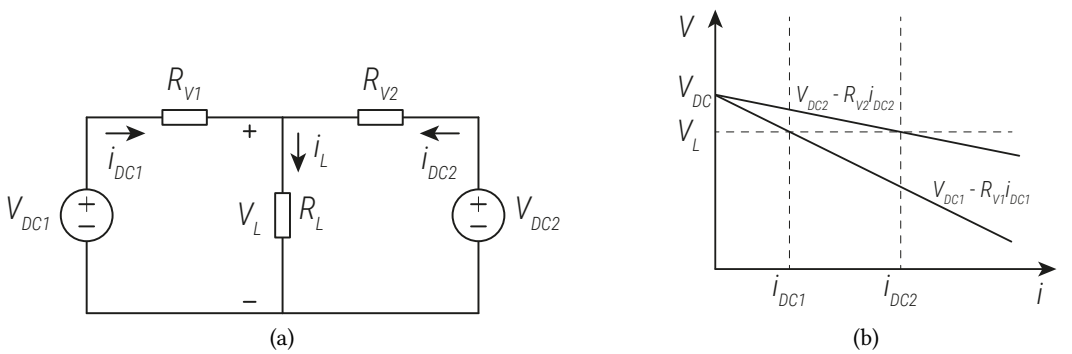


Fig. 6.12 General DC voltage droop control for two parallel voltage sources: (a) circuit diagram and (b) droop characteristics.

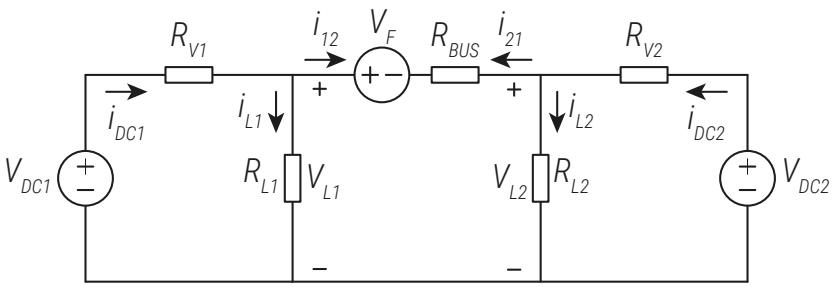


Fig. 6.13 Circuit diagram of two-bus DC PDNs connected through bus-tie switch.

It is found that this general control scheme cannot be applied to the test setup that is the two-bus DC PDNs connected through the bus-tie switch (see **Fig. 6.13**). The first reason is related to the voltage drop (V_F) in the bus-tie switch. The sign of the voltage drop is different depending on power flow due to its bidirectional feature and topology. For the power flow from V_{DC1} to V_{DC2},

$$V_{DC1} - R_{V1} i_{DC1} - V_F - R_{BUS} i_{12} = V_{DC2} - R_{V2} i_{DC2} \tag{6.1}$$

In case of the other flow,

$$V_{DC1} - R_{V1} i_{DC1} + V_F - R_{BUS} i_{12} = V_{DC2} - R_{V2} i_{DC2} \tag{6.2}$$

Because the conventional voltage droop control, as shown in **Fig. 6.12**, does not cover the voltage drop, its magnitude and sign have to be additionally considered in the power sharing control.

The other reason originates from the voltage sensing resolution. If the resolution is not high, it is difficult to precisely regulate the power sharing or it is required to employ the steep droop slope. The former means poor power sharing function, and the latter can generate an issue in voltage regulation, e.g., a large variation of the reference voltage depending on load conditions. The voltage sensing issue is a more dominant cause why the test setup employs a new power sharing scheme. The DC voltage can be measured only with 1 V resolution in the setup, due to combination of used sensors and an analogue/digital converter in the acquisition card of the PLC. After several tests, it became obvious that the 1 V resolution could not guarantee precise power sharing.

The employed power sharing scheme fixes the DC voltage of GEN2 with its DC voltage regulation and manipulates the AC voltage reference of GEN1 to supply electrical power within preselected ranges,

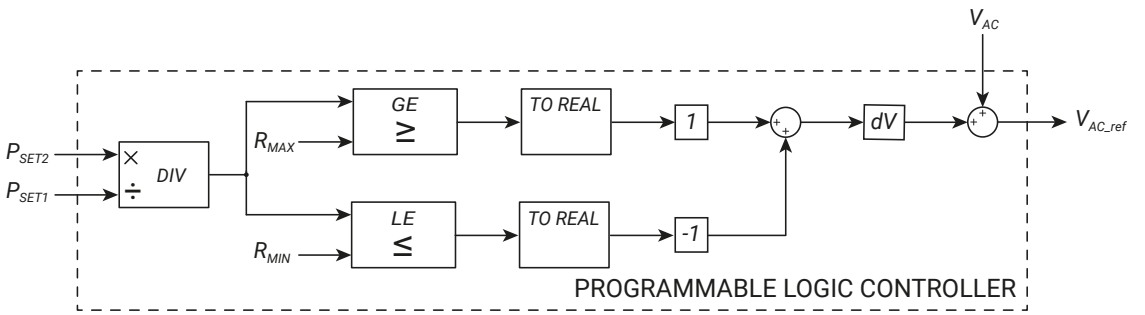


Fig. 6.14 Block diagram of power sharing control.

as illustrated in **Fig. 6.14**. If GEN2 takes more power than the highest threshold, the AC voltage reference of GEN1 is increased with a preselected level (ΔV). For the other case, the AC reference is decreased every 0.1 s (the minimum counter time of the PLC) until the ratio is in the range. The used parameters are: R_{MAX} = 3.3, R_{MIN} = 1.9, and ΔV = 0.05 V.

6.3.3 Soft Start

As explained earlier, the only factor to be matched for the power supply interconnection is the voltage magnitude in DC PDNs. If the bus-tie switch can smoothly charge the potential from one bus to the other bus (called soft start in the work), there is no limitation on the voltage matching requirement during the interconnection process. Furthermore, it allows to extend operation sequences and/or modes of DC PDNs, e.g., supplying electric power to the bus in which no electric source is available due to system design, operating mode (one generator operating mode), or machine failure. The soft start function shown in **Fig. 6.15** is performed by RT Box as the controller of the bus-tie switch.

In addition to the roles of the bus-tie switch (bus connection and disconnection under normal conditions as well as fault interruption), the soft start ability requires only additional control functions for its implementation. The principle of the soft start function is the switch being repeatedly turned *ON* and *OFF*, and the connection of the two buses once the charging is complete. In detail, when the *SOFT START ON* command is transferred from the PLC, the pulse keeps the switch *ON* for a short time. Due to the potential difference between the buses, the charging current (i_{BTS}) flows via the switch, and then the switch is turned *OFF* if the current reaches the threshold level or the pulse becomes *OFF* with its duty cycle (D). This action occurs at every pulse cycle and the potential of the bus being charged is gradually increased. Once the potential difference is within the acceptable range, the switch remains in the *ON* state through the *TURN-ON DELAY* block in **Fig. 6.15**. The used parameters for the soft start control are: f_{BS} = 100 Hz, D = 0.1 pu, T_{ON_D} = 5 s, and $i_{threshold}$ = 100 A. Note that the value of T_{ON_D} is preselected after several charging tests.

6.3.4 Seamless Transition

The used ultra-fast bus-tie switch allows for the seamless transition of system configuration. An interchange between open-bus and closed-bus operations can be achieved with a low system impact. Furthermore, the power source can be transmitted promptly if one bus experiences a power outage

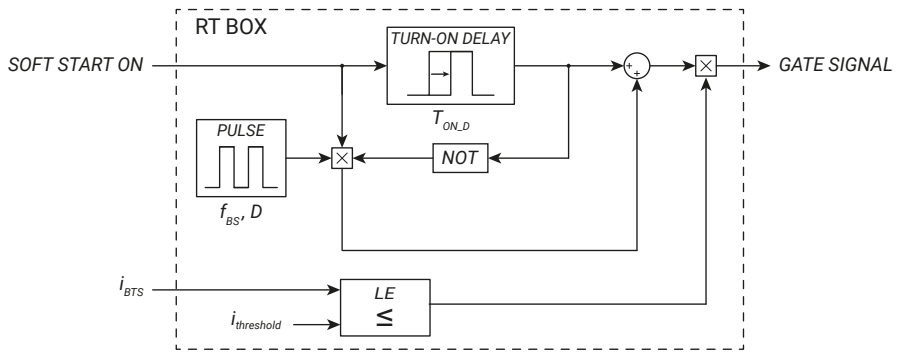


Fig. 6.15 Block diagram of soft start control.

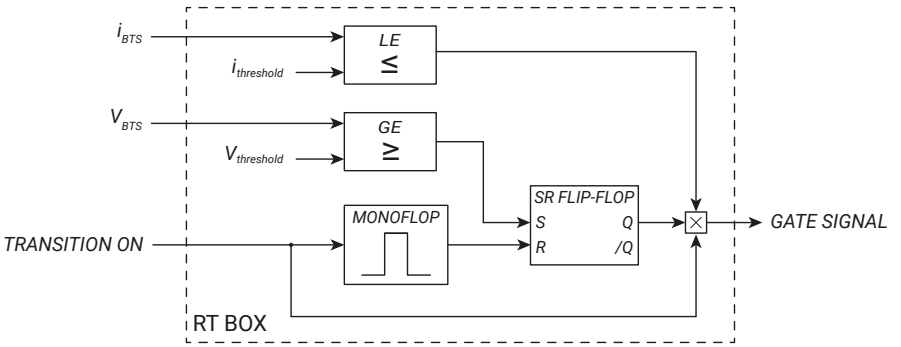


Fig. 6.16 Block diagram of seamless transition control.

during the open-bus operation (called seamless transition in the work). For the latter purpose, the seamless transition function is realized in RT Box.

Fig. 6.16 shows the diagram of seamless transition control implemented. The transition control can be activated during the open-bus operation. While the *ON* signal (*TRANSITION ON* in **Fig. 6.16**) is high, the Q output is reset low. Once the voltage difference between two buses is greater than a threshold value, the gate signal becomes and remains *ON*. If the current passing through the bus-tie switch reaches the fault detection condition (100 A in the work), the bus-tie switch is turned *OFF*. The used value of $V_{threshold}$ is 25 V (5 % of 500 V).

6.4 Experimental Results

Flexible operating modes of two-bus DC PDNs, which consist of two generators with different power ratings and frequencies, are demonstrated in the test setup, as shown in **Tab. 6.3**. The first (*GEN1*

Tab. 6.3 Experimental test cases for DC PDNs demonstration.

Operating Modes	GEN1 (10.7 kW)	GEN2 (25 kVA)	Load1 (L1) (2.5 kW)	Load2 (L2) (2.5 kW)	Load3 (L3) (2.8 kW)	Bus-Tie Switch	Power Sharing
GEN1 only	*ON*	*OFF*	*ON* at **30 s** *OFF* at **40 s**	*ON* at **20 s** *OFF* at **50 s**	*ON* at **10 s** *OFF* at **60 s**	Soft start at **0 s**	*OFF*
GEN2 only	*OFF*	*ON*	*ON* at **30 s** *OFF* at **40 s**	*ON* at **20 s** *OFF* at **50 s**	*ON* at **10 s** *OFF* at **60 s**	Soft start at **0 s**	*OFF*
P-sharing 1	*ON*	*ON*	*ON* at **0 s** *OFF* at **160 s**			Initially closed	*ON* at **40 s** *OFF* at **120 s**
P-sharing 2	*ON*	*ON*		*ON* at **0 s** *OFF* at **160 s**		Initially closed	*ON* at **40 s** *OFF* at **120 s**
Transition	*OFF* at **−2 s** *ON* at **8 s**	*ON*	Initially loaded	Initially loaded		Closed at **0 s** Open at **8 s**	*OFF*
	ON	*OFF* at **58 s** *ON* at **68 s**	Initially loaded	Initially loaded		Closed at **60 s** Open at **68 s**	*OFF*

only) and second (*GEN2 only*) modes are tested not only to verify the DC voltage regulation function, but also to tackle the issue on voltage magnitude matching during the interconnection (the soft start). The power sharing mode is performed in two different test cases (*P-sharing 1* and *P-sharing 2*). Lastly, the seamless transition (*Transition*) is conducted by generating a voltage drop in one bus during self-sustained operation (open-bus operation) and checking the prompt power source transition.

6.4.1 Voltage Regulation and Soft Start

Transient waveforms under the GEN1 only mode is shown in **Fig. 6.17**. The port bus (BUS1) that is supplied by motor-generator set 1 (GEN1) is initially operated with its rated voltage. At 0 s, the soft start command is issued and the bus-tie switch charges the potential of the starboard bus (BUS2) by turning the bus-tie switch *ON* at every 10 ms and *OFF* once the charging current reaches the threshold value or the pulse becomes *OFF* with its duty cycle, repetitively, as shown in **Fig. 6.17(b)**. The potential in BUS2 is fully charged at approximately 3.7 s. Note that the transient current during the soft start is not measured in **Fig. 6.17(a)** due to the sampling rate limitation of a measuring device for a long period time (10 s/div), and thus the current in **Fig. 6.17(b)** is measured by the other device for a short period time (0.5 s/div).

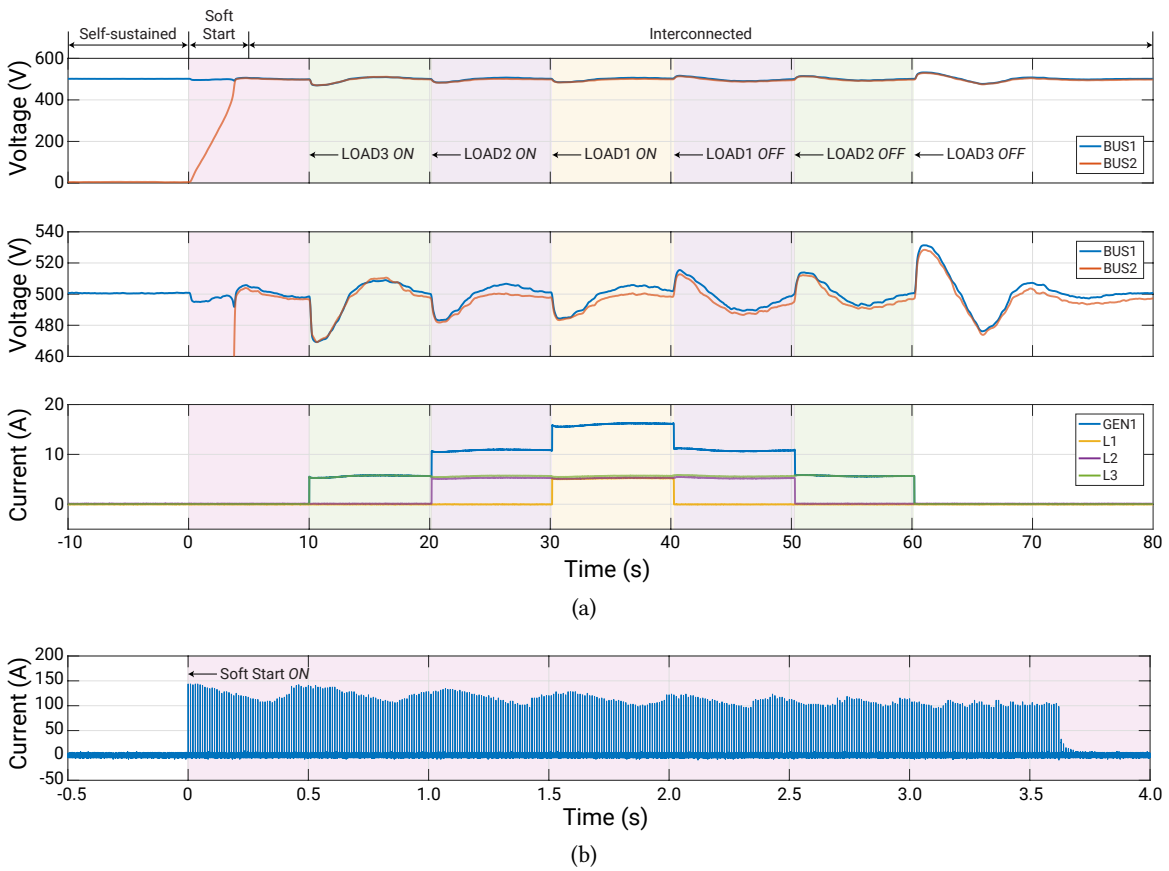
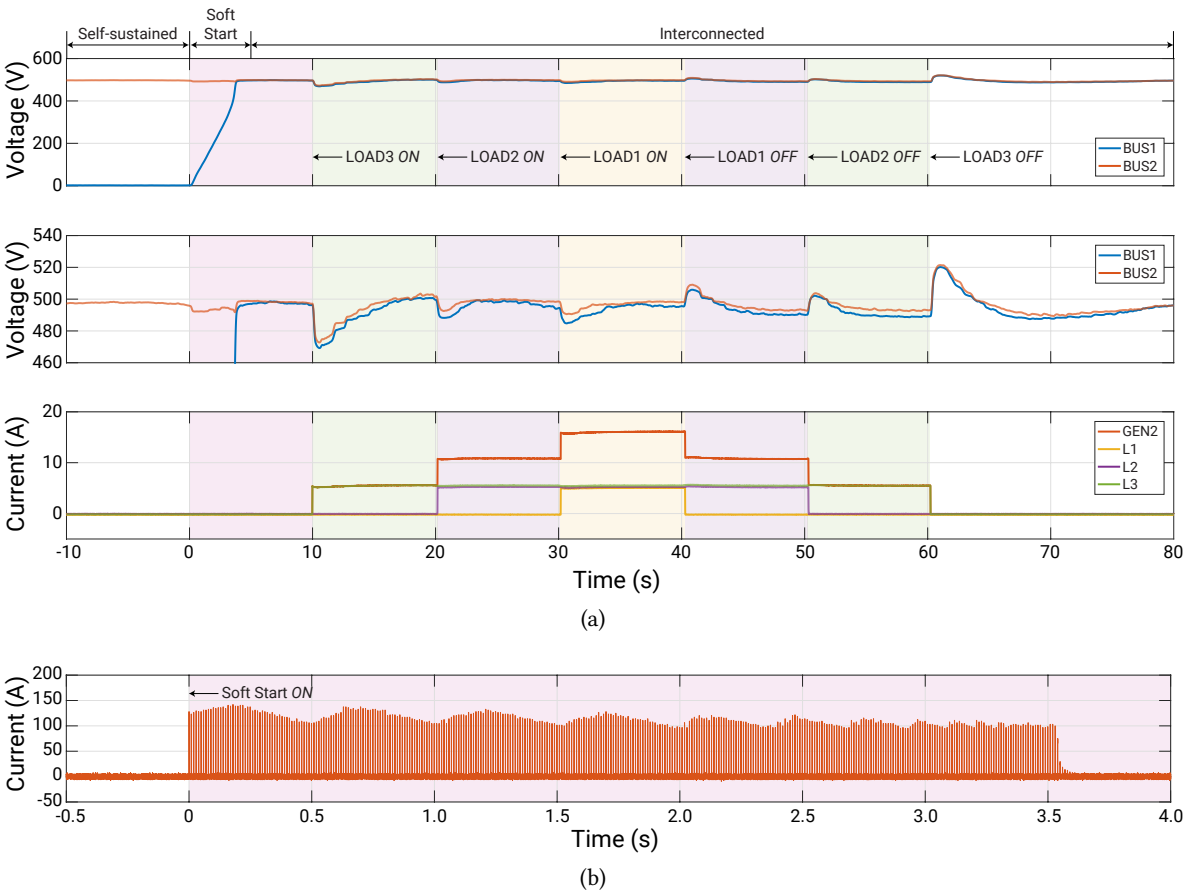


Fig. 6.17 Transient waveforms under GEN1 only mode: (a) bus voltages and generator/load currents (**10 s/div**) and (b) current via the bus-tie switch during the soft start (**0.5 s/div**).



(a)

(b)

Fig. 6.18 Transient waveforms under GEN2 only mode: (a) bus voltages and generator/load currents (**10 s/div**) and (b) current via the bus-tie switch during the soft start (**0.5 s/div**).

It is observed that the voltage of BUS1 is higher than that of BUS2 due to the voltage drop in the bus-tie switch, and the voltage difference becomes higher when higher current flows via the bus-tie switch. After the interconnection, the three loads are sequentially connected and disconnected with 10 s interval. The load changes bring with sudden voltage drops and rises, and the control system successfully regulates its bus voltage at the rated value.

The soft start function and the DC voltage regulation implemented in GEN2 are tested with the GEN2 only mode, as shown in **Fig. 6.18**. Similar to the GEN1 only mode, the starboard bus (BUS2) is operated with its rated voltage and the port bus (BUS1) is charged and interconnected. After the interconnection, the three loads are sequentially connected and disconnected, and the voltage control of GEN2 regulates the DC voltage of BUS2.

Differently with the GEN1 only mode, there is a voltage drop from BUS2 to BUS1 and it causes that the voltage of BUS2 is higher than that of BUS1. The other finding is that the voltage variations due to the load changes are less than those of the GEN1 only mode. This mainly comes from the different generator frequencies: GEN2 operated at approximately 200 Hz and GEN1 operated at 50 Hz. GEN2 is operated with four times higher frequency compared to GEN1 and this increases the system reactance of GEN2. As a result, the increased reactance makes the GEN2 system less sensitive for the sudden load change.

6.4.2 Power Sharing

The power sharing is demonstrated under the conditions of the two generators *ON* and the initially closed bus-tie switch. Load1 (L1) installed at BUS1 is connected at 0 s and the two buses suffer voltage drops. The load is shared between the two generators during the transient period. When each bus is regulated at its rated voltage, GEN1 provides all the load current. It means that GEN2 has no contribution to the load due to the voltage drop in the bus-tie switch, while GEN2 (25 kW) has 2.5 time higher power rating than GEN1 (10 kW).

The power sharing function is activated at 40 s. The function calculates the power sharing ratio between the two generators and gradually decreases the AC voltage reference of BUS1 in the tested case. **Fig. 6.19** shows that power sharing is achieved within each control range for Load1. When the power sharing is deactivated, the voltage regulation control of BUS1 is restarted and GEN1 produces all the power for Load1. When the load is disconnected at 160 s, BUS1 has a higher voltage rise and it generates the current flow from BUS1 to BUS2 for a short time.

In the second case, Load2 (L2) installed at BUS2 is connected at 0 s. As expected, the load is powered only by GEN2 without the power sharing function. When the function is activated, the voltage of BUS1 is gradually increased to share the load within the control range.

Both tests prove that the implemented function can control the power ratio between the two-bus systems connected through the bus-tie switch that has different signs of the voltage drop depending on the current direction. Moreover, by accurately controlling the AC reference voltage, it is possible to overcome the low resolution in the DC voltage sensing, aforementioned.

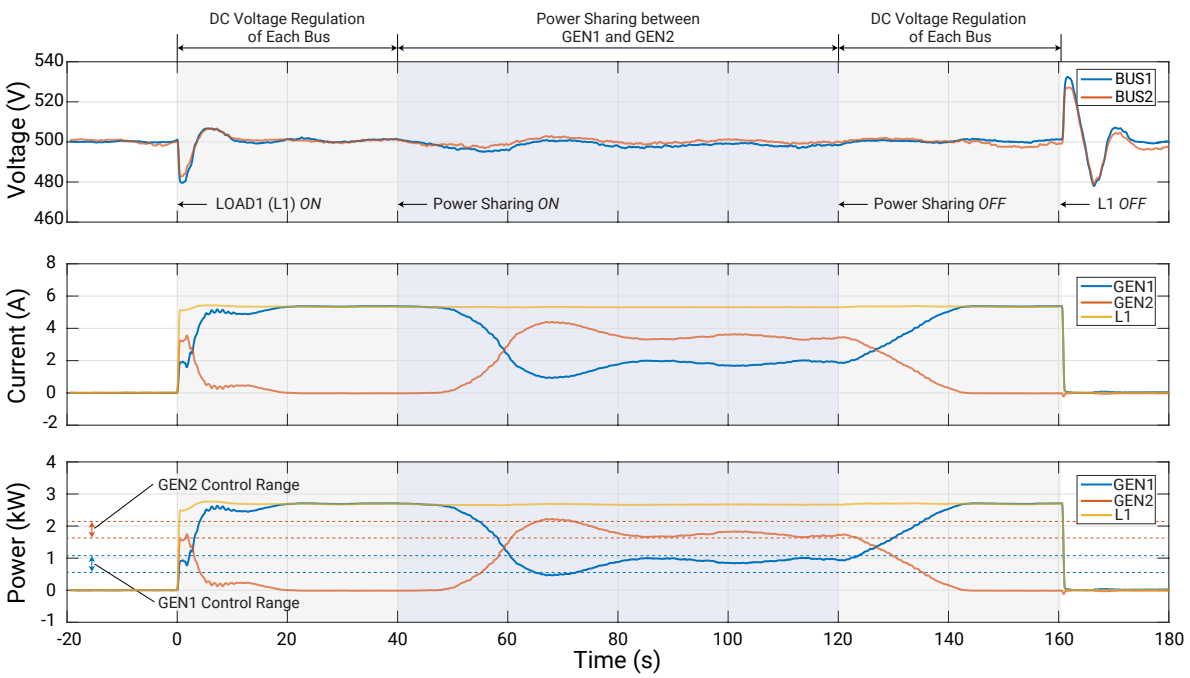


Fig. 6.19 Performance of power sharing function under the loading only at BUS1 (P-sharing 1 mode).

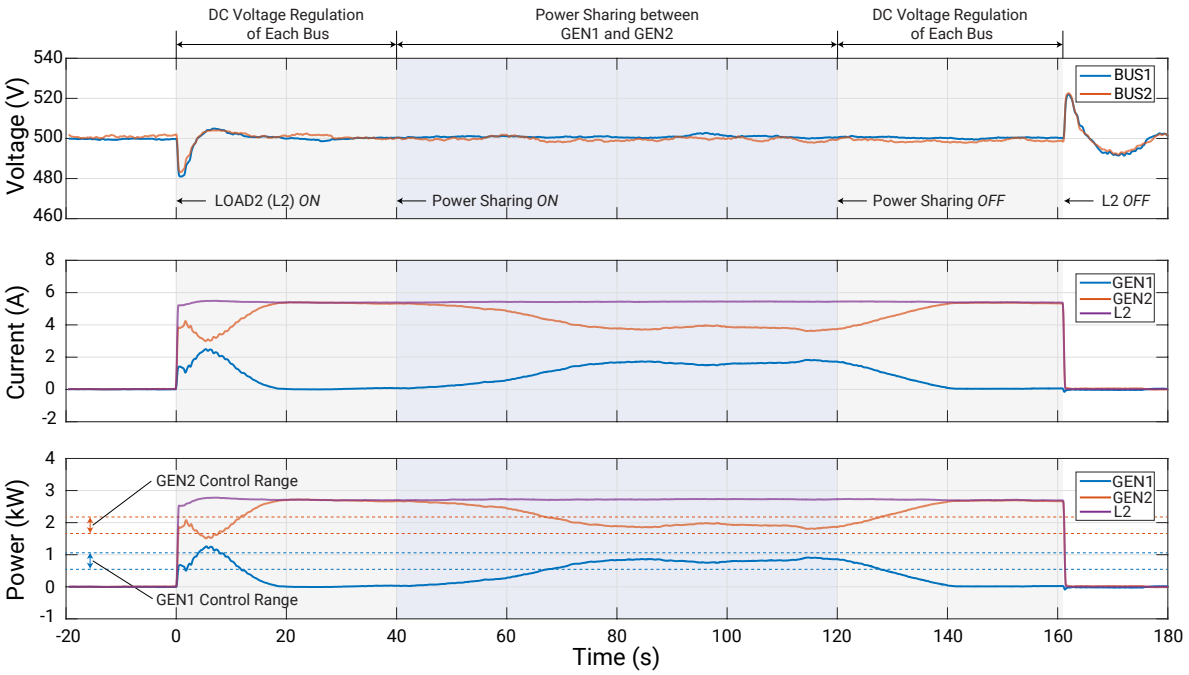


Fig. 6.20 Performance of power sharing function under the loading only at BUS2 (P-sharing 2 mode).

6.4.3 Seamless Transition

A seamless transition test is conducted under the conditions of the two generators *ON* and the two loads at each bus (L1 and L2). Initially, the two buses are operated with the self-sustained mode

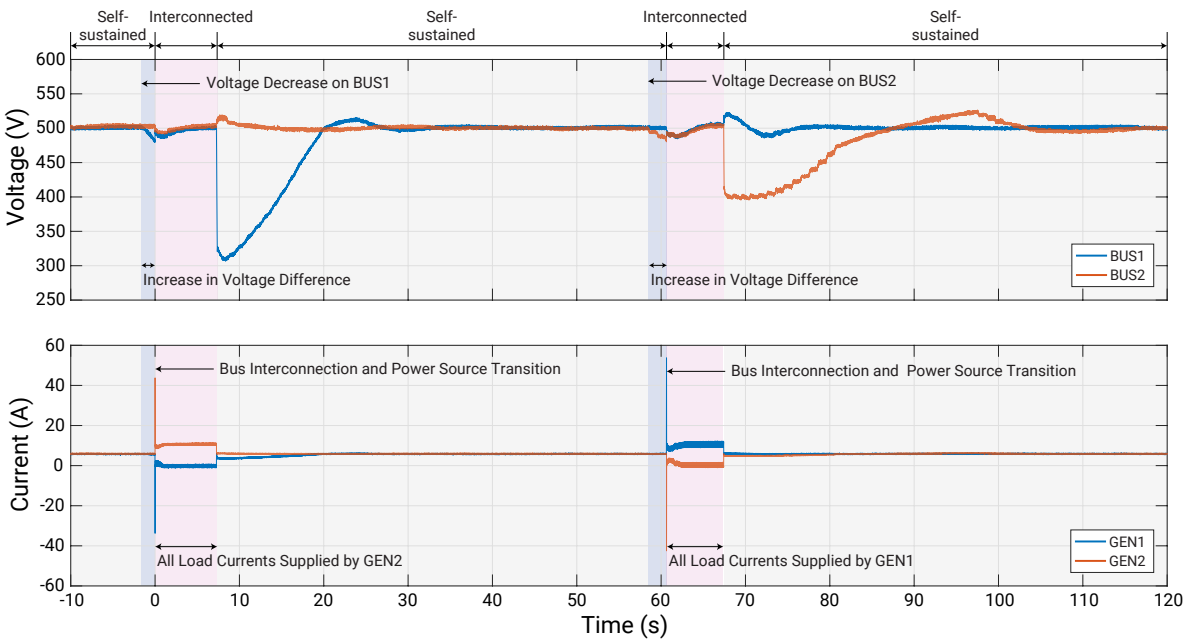


Fig. 6.21 Performance of seamless transition under transition mode.

(open-bus operation), and thus each generator supports the load at its bus. The voltage drop is commanded to BUS1 at −2 s and the two buses are interconnected by the ultra-fast bus-tie switch when the voltage difference becomes the threshold value (25 V) at 0 s (see **Fig. 6.21**). Due to the loss of the source in BUS1, all load currents are supplied by GEN2 under the test condition.

For the other transition test, the bus-tie switch is turned *OFF* at 8 s and the DC voltages of the two buses become the rated value. Same as the initial condition, each bus maintains its bus voltage and each load takes the power from each bus. The second transition is initiated by developing the voltage drop in BUS2 at 58 s and the interconnection occurs at 60 s with the voltage difference of 25 V. The maximum transition current is approximately 55 A under the test conditions. If the bus experienced the voltage drop has a permanent low-impedance fault, the transition current may reach the threshold value and the interconnection cannot be possible with its protection (see **Fig. 6.16**).

The test result verifies that the seamless transition can be achieved in DC PDNs with the solid-state bus-tie switch. It allows for operating the systems more flexible and improving system reliability.

6.5 Conclusion

This chapter has demonstrated flexible operating modes of two-bus DC PDNs with two different power rating and frequency generation systems, which cannot be integrated in AC PDNs. For the hardware demonstration, the test setup of 35 kW consists of the two generator sets (GEN1 - 10 kW / 50 Hz and GEN2 - 25 kW / 200-400 Hz), the three loads of 7.8 kW in total, and the bus-tie switch.

The implemented system controls for the two-bus DC PDNs are DC voltage regulation, power sharing control, soft start, and seamless transition. From the demonstration results, it is summarized: the DC voltage can be regulated by combining the main controller and the AC AVR; power sharing between the two generators is possible with the power sharing function implemented in the work; the bus voltage matching can be ignored with the active bus-tie switch, having the soft start function; and power sources can be flexibly and promptly transited with low system impacts in DC PDNs based on solid-state technologies.

With the above results, it is concluded that DC PDNs offer superior features in term of the flexibility in energy management of the system.

7

DC Power Distribution Networks with Integrated Energy Storage

This chapter presents extended DC system operating modes with energy storage systems. For the energy storage systems, two supercapacitor banks (2 × 2 F) are integrated into the lab-scaled test setup through DC-DC converters. The potential benefits of energy storage inside the DC power distribution networks are examined with the demonstration of the following operating modes: transient mitigation - supporting transient demands by energy storage with short time constants; load leveling (peak shaving) - operating generators at optimal loads by storing energy during light load conditions and providing it during too heavy load conditions; and zero-emission operation - turning OFF generators and powering the networks by energy storage when a ship is entering or exiting a port.

7.1 Introduction

In the past decade, there has been enormous evolution in energy storage systems (ESSs), especially in Li-ion batteries, in terms of energy density, power density, and cost [132], [133]. This progress allows ESSs to be accepted more widely in marine applications, as presented in **Fig. 1.3(b)**. While an ESS is still a costly option, it provides ship owners with several main benefits, mostly related to fuel savings and environmental compliance in a port or during the approach to a port.

As described in **Chap. 1** and **Chap. 2**, two dominant marine LVDC solutions are based on synchronous generators combined with diode and thyristor rectifiers. Dynamic performances of these solutions are governed by an exciter and/or a thyristor control and therefore their dynamic responses are much slower than the LVDC solutions based on VSCs. Once ESSs are integrated into DC PDNs through

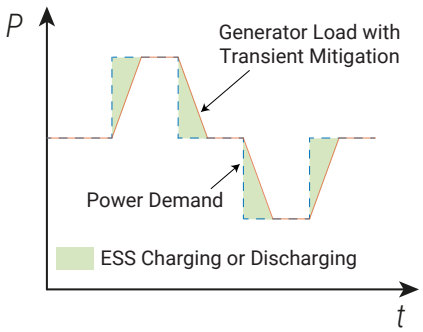


Fig. 7.1 Mitigation of transient generator loads with ESSs.

converters, the transient performance of these solutions can be improved with the fast control action of converters. As shown in **Fig. 7.1**, it is also possible to avoid transient generator loads by rapidly discharging or charging energy during the transient period. This allows for increasing the lifespan of a ship engine-generator set and reducing air pollutants generated during high transient accelerations and decelerations. Furthermore, the regenerative energy from a decelerated induction machine, which is dissipated by braking resistors to prevent a system overvoltage, can be stored in ESSs.

The second main advantage is load leveling (also peak shaving). Engine-generator sets are usually designed to have high efficiency for target operating ranges, e.g., marine engine-generator set: 60-100 % loads [134]. When power demand is highly variable and its peak is slightly higher than the power rating of running generators, the other generator has to be turned *ON* to meet the power demand and they may be operated at non-optimal points. This power redundancy can be achieved by ESSs. ESSs can discharge the energy for the heavy loads and thus this operation enables system operators to reduce the number of running generators and make the generators to be operated in optimal ranges [21]. On the other hand, ESSs can store the energy during light load conditions. These flattened generator loads provide a large potential for fuel savings in marine applications.

Lastly, a port can be free from pollution with ESSs equipped in vessels. Although ships cannot go long-distance cruising only with ESSs due to low energy density of batteries, they can switch their power source from diesel generators to ESSs when they are approaching a port, called zero-emission mode. In a port, shore-to-ship power connection is possible. This means that onshore grids not only supply power to all onboard loads, but also recharge the onboard storage. The zero-emission mode, solely powered by ESSs, can be activated with fully charged ESSs when ships are leaving a port. There are a wide range of activities to meet environmental regulations and to make a cleaner port [135], [136]. This zero-emission operation is crucial to achieve the goal of becoming the zero-emission port.

This chapter presents extended DC PDN operating modes with ESSs. For ESSs, two supercapacitor banks (2 × 2 F) are additionally integrated into the lab-scaled test setup through DC-DC converters. The potential benefits of DC PDNs with ESSs, described above, are examined with the demonstration of following operating modes: **transient mitigation** - supporting transient demands by ESSs with short time constants to improve the transient performance of diode and thyristor-based DC PDNs; **load leveling (peak shaving)** - operating generators at optimal loads by storing energy during light load conditions , discharging it during too heavy load conditions, and reducing the number of running generators; and **zero-emission operation** - turning *OFF* generators and powering the networks by ESSs when a ship is entering or exiting a port to avoid air pollutants from a ship.

7.2 Supercapacitor-Based Energy Storage Systems

Due to lack of access to suitable batteries for the test setup, alternative technology (supercapacitor bank) is used, without major negative effect on the performances that this paper aims to demonstrate. Two pairs of two supercapacitors are connected in series and then these series-connected supercapacitors are wired in parallel (see **Fig. 7.2**). With this configuration each supercapacitor bank is rated for 160 kJ. These supercapacitor banks are coupled in the test setup via DC-DC converters. Two of Imperix half-bridge power modules [137] are used for the converters and the converters are controlled by an Imperix B-Box RCP controller [138]. The central controller (PLC) talks with the ESS controller (B-Box RCP) through CANOpen communication. The actual implementation of the ESSs

is shown in **Fig. 7.3**. The DC-DC converters and the controller are installed under the solid-state bus-tie switch [see **Fig. 7.3(b)**] and the supercapacitor banks (8 supercapacitor units) are mounted in a rack [see **Fig. 7.3(a)**].

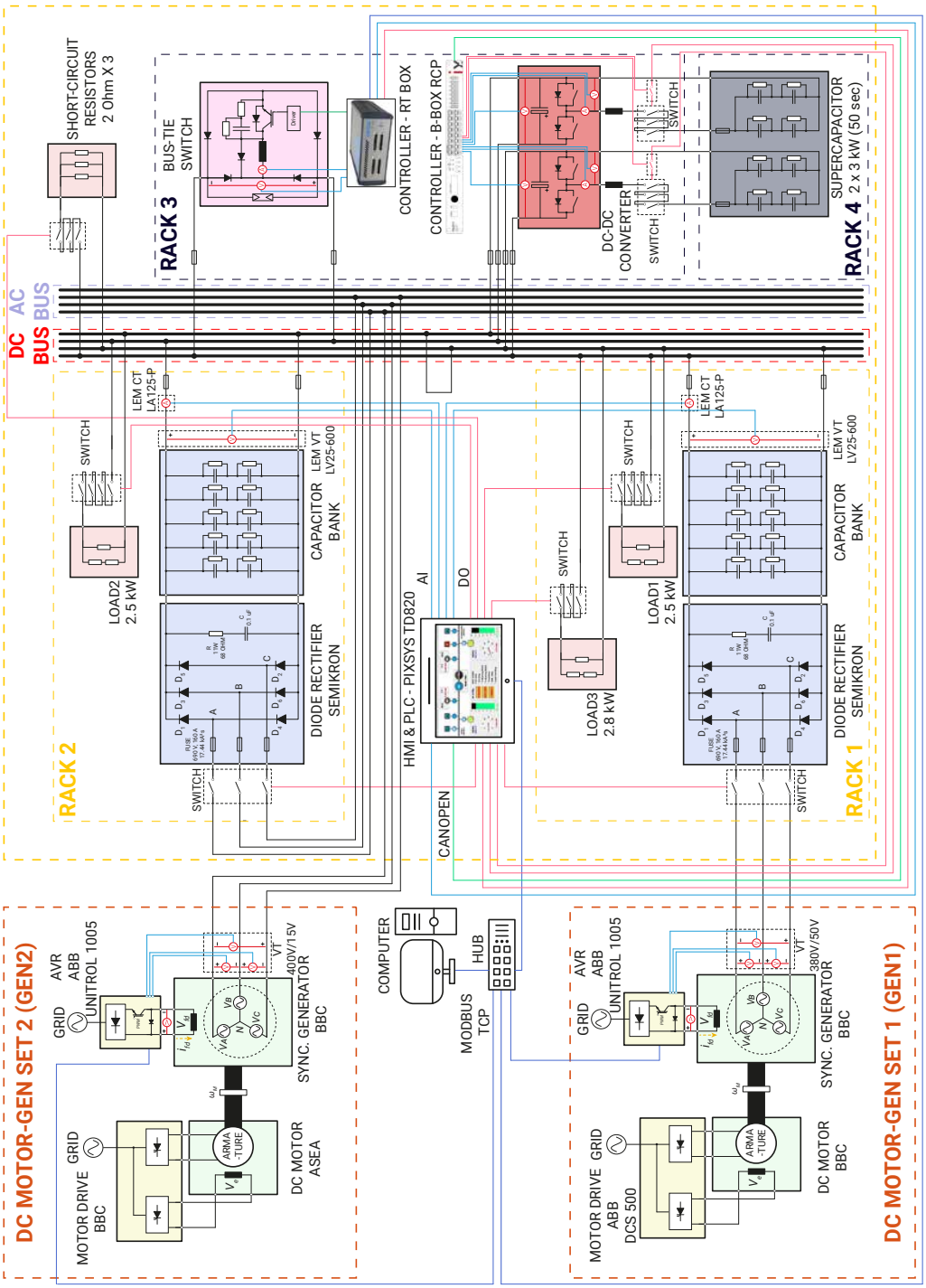
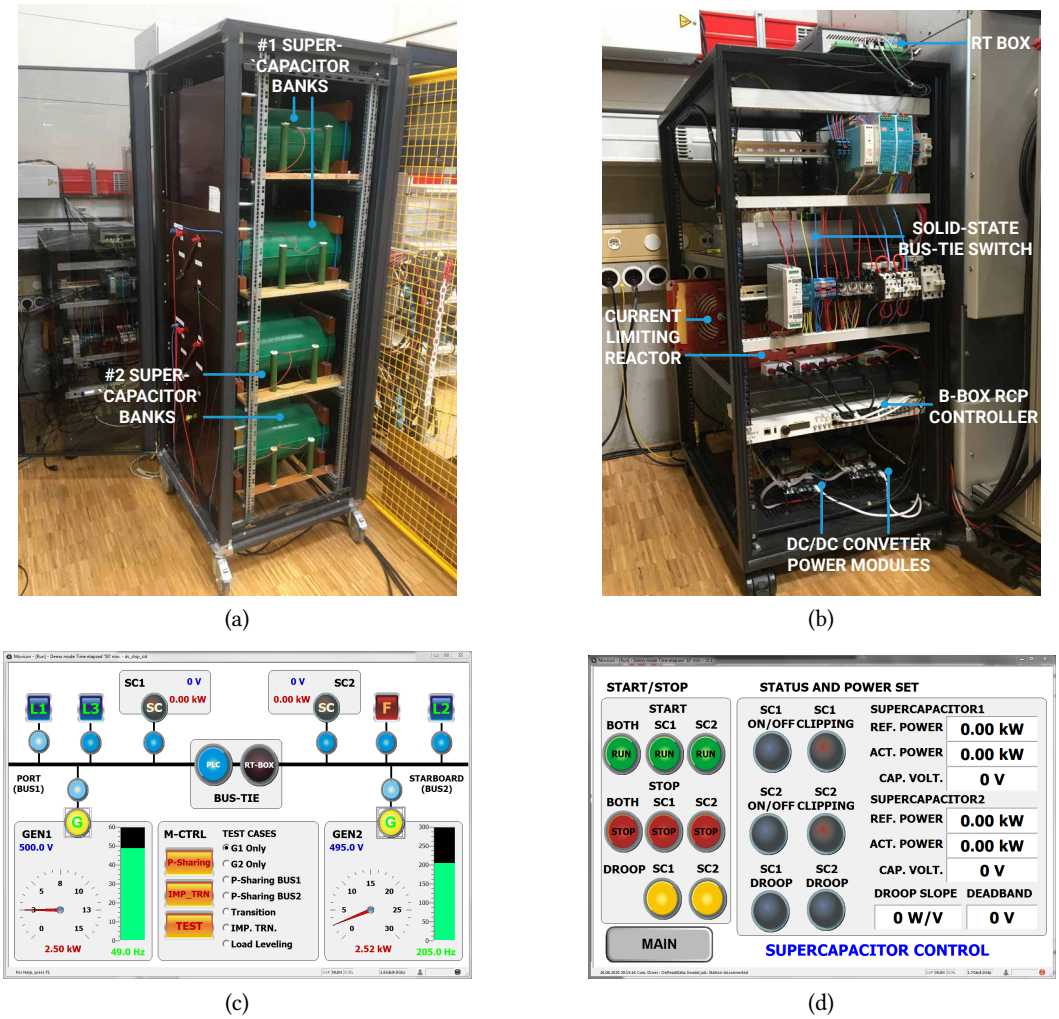


Fig. 7.2 Complete schematic diagram of test setup with ESSs. The ESSs and the short-circuit resistors are additionally installed to the previous test setup, as depicted in **Fig. 6.1**.



(a) (b)

(c) (d)

Fig. 7.3 (a) Supercapacitor banks, (b) DC-DC converters, (c) modified main HMI screen, and (d) HMI screen for supercapacitor control. The converters are additionally installed in the same rack with the solid-state bus-tie switch, as shown in **Fig. 6.9**.

The HMI screen in the PLC is modified to monitor the supercapacitor banks and to generate fault conditions, as shown in **Fig. 7.3(c)**. The supercapacitor banks can be controlled via the screen in **Fig. 7.3(d)**, e.g., switching *ON* and *OFF*, operating mode selection (power reference mode or power droop mode), and setting the power reference or the droop parameters.

7.3 Supercapacitor Bank Control

System control is necessary to demonstrate operating modes extended by the supercapacitor-based ESSs. The controls realized in the supercapacitor banks are DC-DC converter control, load leveling, and power droop. The power droop is to demonstrate transient mitigation and zero-emission modes.

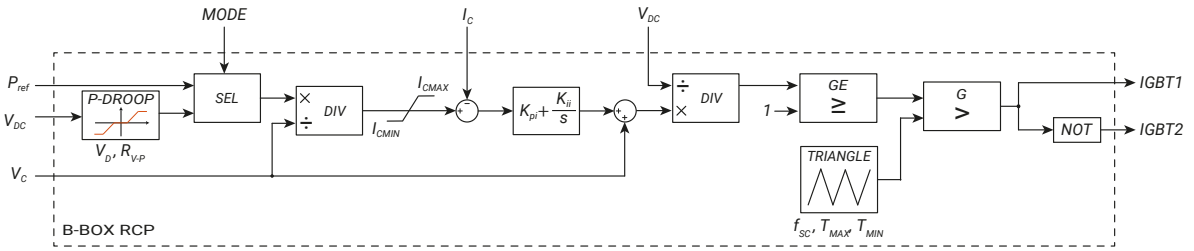


Fig. 7.4 Block diagram of DC-DC converter control.

7.3.1 DC-DC Converter Control

As mentioned, the half-bridge power modules are used for supercapacitor charging and discharging. The supercapacitor banks can be charged by modulating the upper IGBT (*IGBT1*), acting as a buck converter. On the other hand, the DC-DC converters can boost the DC-link voltage with the PWM switching of the lower IGBT (*IGBT2*). The power input of the converters can directly be set in the HMI screen or can be calculated by the DC power droop characteristics. The direct power reference is fed to the converter controller for the load leveling. On the other hand, the transient mitigation and zero-emission modes rely on the droop characteristics.

The block diagram of the converter control is presented in **Fig. 7.4** and the used parameters are: $I_{CMAX} = 8\,\text{A}$, $I_{CMIN} = -8\,\text{A}$, $K_{pi} = 42.4$, $K_{ii} = 3535.5$, $f_{sc} = 10\,\text{kHz}$, $T_{MAX} = 1$, and $T_{MIN} = 0$.

7.3.2 Load Leveling

To maintain the generator load within optimal operating ranges, the difference between power demand and high/low threshold of generator load should be compensated by ESSs. Thus, the central controller collects the total power demand and then sends ESSs the power reference. If there is no margin in the load leveling control, the actual generator load may not be in the control ranges because of the time delay caused by communication, ESS response, and so on. Including the margin (P_{MARGIN}), the block diagram of the load leveling control is presented in **Fig. 7.5** and the used parameters are: $P_{LL\_MAX} = 6.1\,\text{kW}$, $P_{LL\_MIN} = 5.1\,\text{kW}$, and $P_{MARGIN} = 0.3\,\text{kW}$.

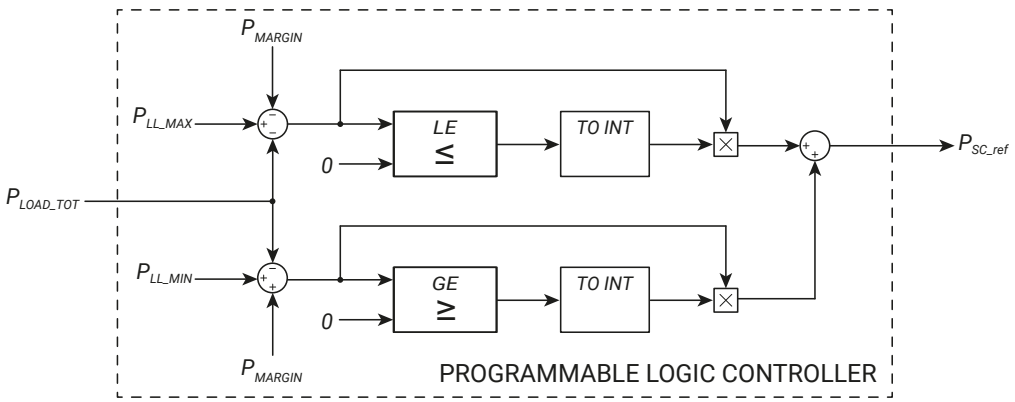


Fig. 7.5 Block diagram of load leveling control.

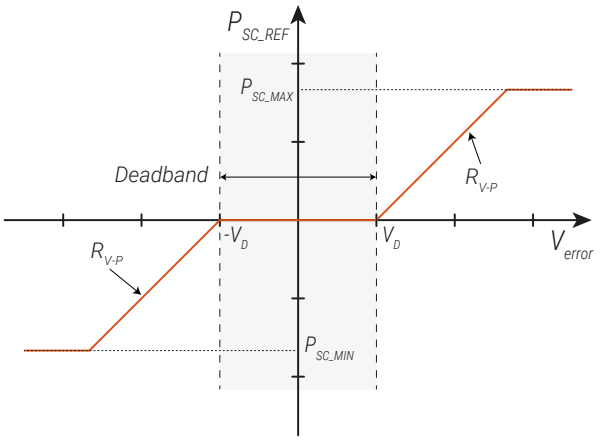


Fig. 7.6 Implemented power droop control.

7.3.3 Power Droop

Transient voltage is a representative indicator to recognize sudden load changes in DC PDNs, i.e., sudden load increases or decreases result in voltage drops or rises, respectively. Furthermore, higher load changes result in higher voltage changes. For these reasons, power droop control depicted in **Fig. 7.6** is applied for the demonstration of transient mitigation. Otherwise, the zero-emission mode is several transitions of power source, e.g., port in - from ship generators to ESSs; in a port - from ESSs to grids; port out - from grids to ESSs; and far from a port - from ESSs to ship generators. These transitions are demonstrated with the power droop in the work.

The droop control is implemented in the B-Box RCP and the PLC can set the parameters. The used parameters are: V_D = 5 V, R_{V-P} = 300 W/V, P_{SC_MAX} = 3 kW, and P_{SC_MIN} = −3 kW.

7.4 Experimental Results

Extended operating modes of two-bus DC PDNs with the supercapacitor banks are demonstrated with experimental test cases, as presented in **Tab. 7.1**. In the load leveling mode, the first supercapacitor

Tab. 7.1 Experimental test cases for DC PDNs with energy storage systems.

Operating Modes	**GEN1** (10.7 kW)	**GEN2** (25 kVA)	**Load1 (L1)** (2.5 kW)	**Load2 (L2)** (2.5 kW)	**Load3 (L3)** (2.8 kW)	**SC1** (3.0 kW)	**SC2** (3.0 kW)
Load Leveling	*ON*	*OFF*	*ON* at **0 s**	*OFF*	Initially loaded	Variable loads from **10** to **80 s**	Load leveling control
Transient Mitigation	*ON*	*OFF*	*ON* at **0 s** *OFF* at **50 s**	*ON* at **10 s** *OFF* at **40 s**	*ON* at **20 s** *OFF* at **30 s**	P droop control	P droop control
Zero-Emission	*OFF* at **0 s** *ON* at **60 s**	*ON* at **20 s** *OFF* at **40 s**	*OFF*	*OFF*	Initially loaded	P droop control	P droop control

bank is used to replicate highly variable loads. On the contrary, the second bank is under the load leveling control to compensate the load variation. The transient mitigation is verified by comparing the performances with and without the transient mitigation function for sudden load changes that are the same condition with the *GEN1 only* in **Tab. 6.3**. For the zero-emission mode, GEN1 and GEN2 are assumed as a generator in a vessel and a grid, respectively. With this assumption, the zero-emission operation near or in a port is demonstrated.

7.4.1 Load Leveling

The load leveling control is demonstrated under the conditions of GEN1, L1, and L3 *ON*. The first supercapacitor bank charges or discharges the energy to replicate highly variable loads from 4.1 kW to 7.1 kW within a minute. Once the power demand reaches 5.8 kW that is the upper threshold power to start the control ($P_{LL\_MAX} - P_{MARGIN}$), the second supercapacitor bank discharges its energy to take the power demand above the threshold. For lower power demand than 5.4 kW ($P_{LL\_MIN} + P_{MARGIN}$), the supercapacitor is operated with the charging mode to maintain the engine-generator operation within the load leveling range from 5.1 kW to 6.1 kW selected in the study.

The experimental test shows that the generator load (blue line) can be flattened within the control ranges while the power demand (blue-dotted line) is highly fluctuated. With the load leveling, it is possible to make the generator set to be operated at optimal operating ranges. Moreover, if the maximum power rating of the generator set is 6.5 kW, two generator sets have to be run for high load conditions (6.5-7.15 kW in the studied case). In this case, the power redundancy can be achieved by one running generator set with ESSs, as demonstrated. To sum up, DC PDNs equipped with ESSs can save large amounts of fuel for highly variable loads (e.g., dynamic positioning) by operating the generator set in optimal operating ranges as well as by reducing the running generator set (its fuel saving is discussed in **Tab. 1.2**).

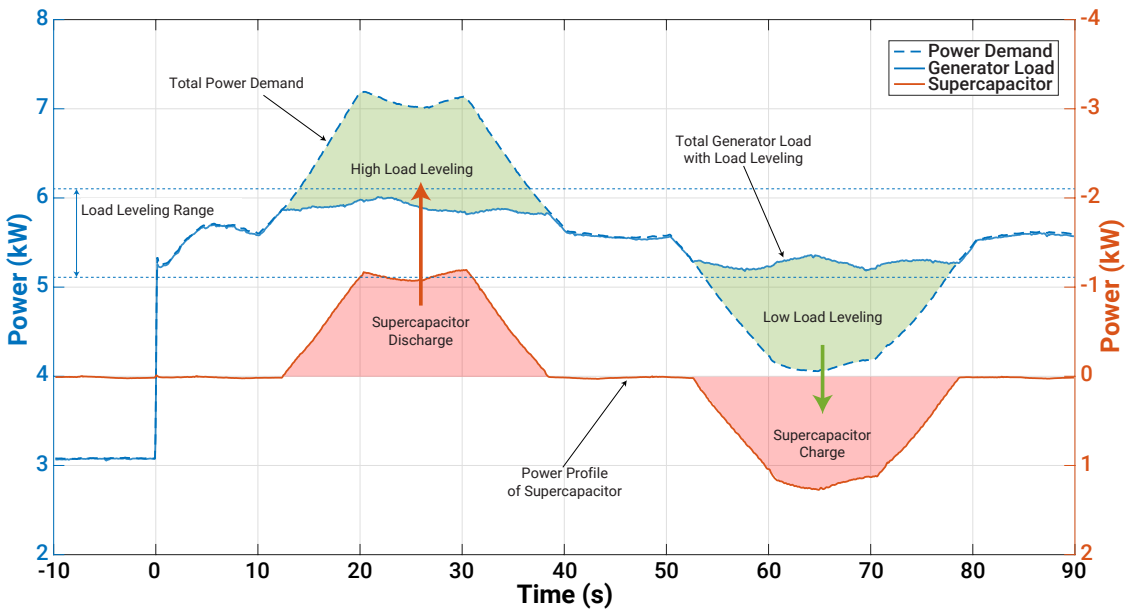
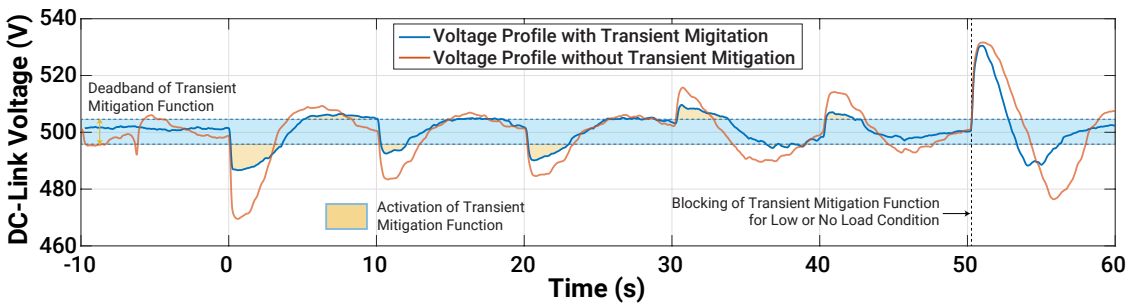


Fig. 7.7 Power profile of load leveling control.

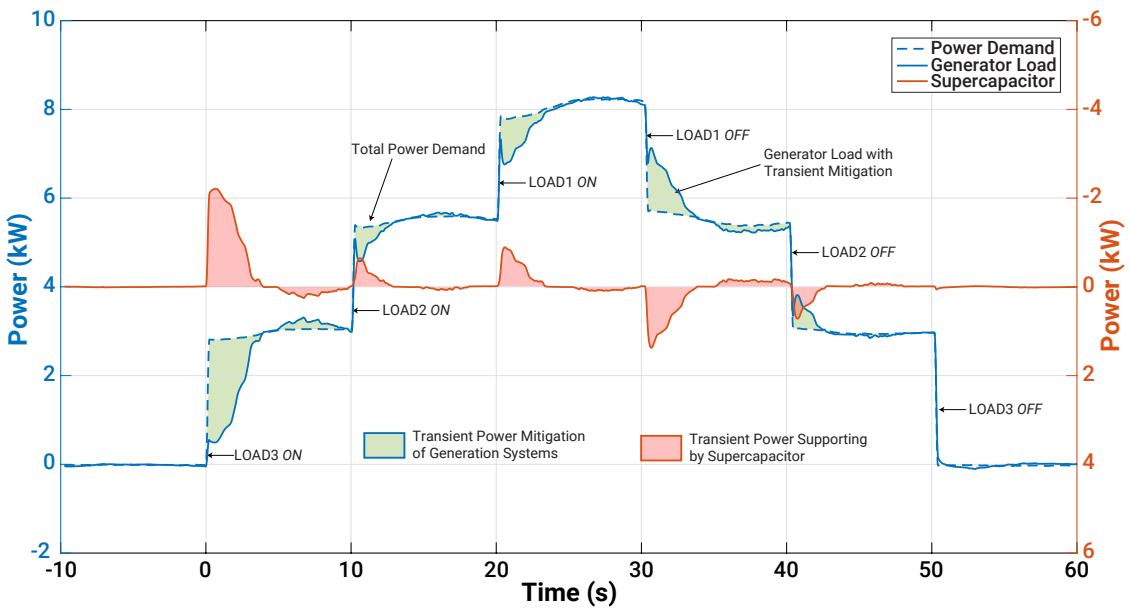
7.4.2 Transient Mitigation

In the test setup, the supercapacitor bank has a much faster response than the main power supply (synchronous generators combined with diode rectifiers). The transient performance of the DC PDNs is improved by using this fast acting device. When sudden load changes occur in the networks, those generate the voltage rises or drops. If the DC-link voltage becomes higher or lower than deadband voltages, the supercapacitor discharges or charges the energy according to the power droop control in **Fig. 7.6**.

Fig. 7.8(a) shows that the DC PDNs with ESSs have remarkably lower voltage drops and rises than those without ESSs. From the result, it could be stated that the system performance is greatly improved. It is also observed that the transients of the engine-generator set are mitigated with ESSs. While the power demand is changed in multi-step forms, the supercapacitor makes the actual generator load softer [see **Fig. 7.8(b)**]. As the last point, the test proves that the regenerative energy can be stored in ESSs. To demonstrate the regenerative energy saving, two resistive loads are disconnected at 30 s and



(a)



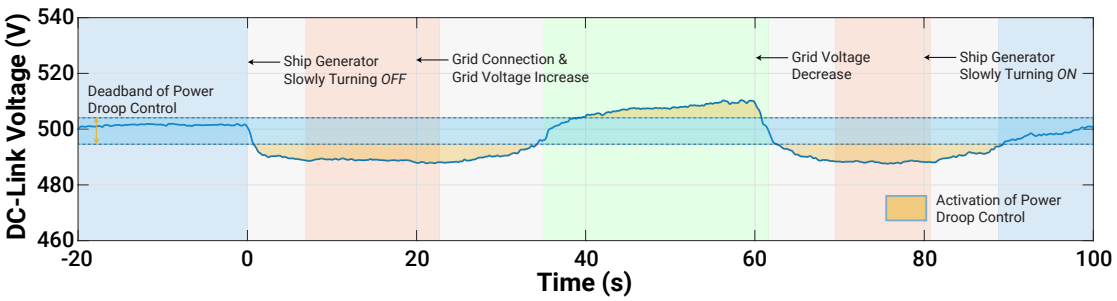
(b)

Fig. 7.8 Transient waveforms under transient mitigation control: (a) voltage profile and (b) power profile.

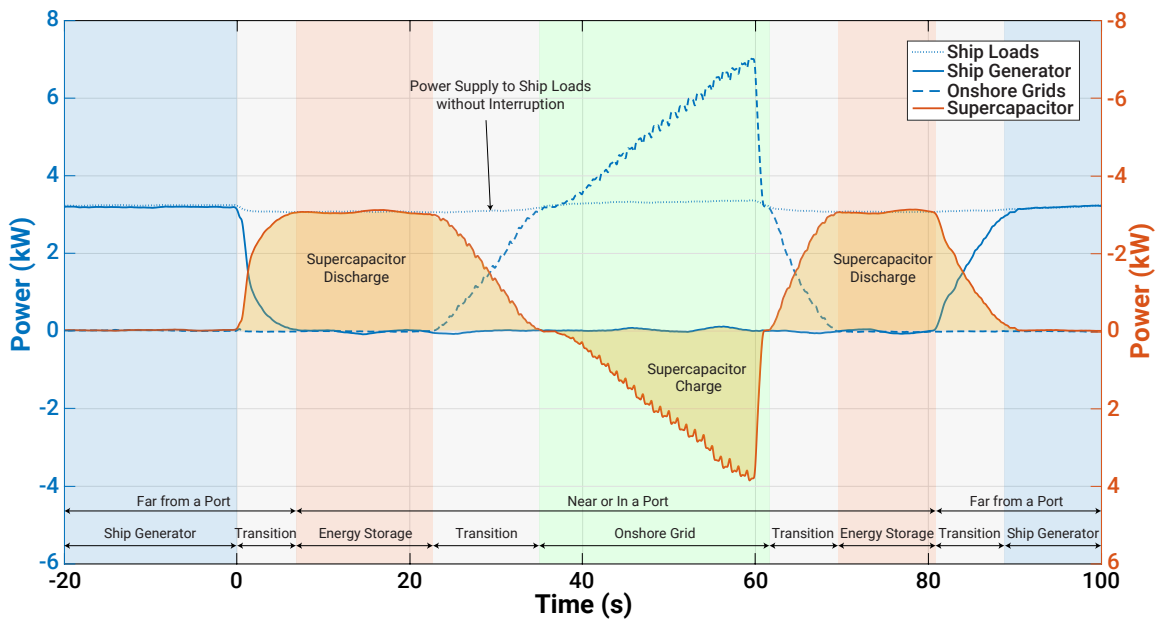
40 s, respectively. These sudden load decreases cause the voltage rises and these energies are stored in the supercapacitor with its power droop control. Note that the droop control to mitigate the transient is deactivated for low or no-load condition to avoid undesired voltage fluctuation.

7.4.3 Zero-Emission

Aforementioned, the zero-emission operation is to avoid air pollutants from ships near a city or a port. Hence, when a ship is approaching a port, the power source should be transited from onboard generators to ESSs. This transient is replicated by slowly turning *OFF* the generators (GEN1 in the work) and then the energy storage systems (the supercapacitor banks) start to supply the power to the system with their power droop control, as shown in **Fig. 7.9**. In a port, grids (GEN2 in the work) can be connected to the ship through a shore-to-ship power supply. After this interconnection, by increasing the grid voltage slightly, the networks can be powered by the grids and this increased network voltage makes the ESSs to be charged according to their droop control. With the fully



(a)



(b)

Fig. 7.9 Transient waveforms under zero-emission operation: (a) voltage profile and (b) power profile.

charged ESSs, the ship can leave the port with the zero-emission operation again.

The experimental test demonstrates that continuous power supply to onboard loads without air pollutant emission can be realized near or in a port with the power droop control of ESSs.

7.5 Conclusion

This chapter has presented extended DC PDN operating modes with ESSs. In addition to the operating modes demonstrated in **Chap. 6**, there are three more operating modes: transient mitigation, load leveling, and zero-emission. The implemented controls for the DC PDNs with ESSs are DC-DC converter control, load leveling, and power droop.

The experimental test results can be summarized as follows: flattening the generator load is possible with the load leveling function controlled by the central controller (the PLC in this work); the transient performance can be improved with the power droop control of ESSs with their low time constant; and the zero-emission mode, which are several transitions of power source, is realized with the power droop control.

With the above results, it is concluded that the DC PDNs with ESSs can provide ship owners with fuel savings and environmental compliance in a port or during the approach to a port.

8

Integrated Protection Scheme for DC Power Distribution Networks

This chapter validates an integrated protection scheme in two-bus DC power distribution networks. The three-level protection is implemented in the lab-scaled test setup (fast action - bus separation by a solid-state bus-tie switch, medium action - feeder protection by a high-speed fuse, and slow action - generator deexcitation). The protection scheme is evaluated by testing actual operating times of the three actions and the fault energies limited by those. Bus and feeder faults are artificially generated in the networks, and the system protection successfully isolates the faults from the networks with the correct operation of protection measures and enough time margins between the actions.

8.1 Introduction

While each protection measure is effective for its protection zone, the measures have to be coordinated to assure the minimum impact on DC PDNs by correct actions through all phases of system faults. This protection coordination is a function of multiple factors: operating times of protection measures, overcurrent withstand capabilities of power equipment, fault locations and impedances, system configurations, operating modes, and so on. Due to the complexity in the coordination, a protection scheme should be simple to use, fast to protect, and effective against all possible conditions. The three-level protection effectively meets these points because it is intuitive and provides robust actions for any DC faults with three-different time frame actions.

As analyzed in **Chap. 2**, in the three-level protection, the feeder fault results in the bus separation by a solid-state bus-tie switch (fast action) and then the fuse on the faulty feeder isolates the fault from the networks (medium action). Through this process, the protection should be coordinated to ensure the proper operation of the bus-tie switch, faster than the fuse operation, and continuing the operation of adjacent healthy loads installed in parallel to the faulty feeder. For the first point, the bus-tie switch has to include current limiting inductance, as presented in **Fig. 6.5**. Once the fault current passing through the bus-tie switch reaches the threshold value, the bus-tie switch interrupts the current after a certain time delay, i.e., an actual breaking current is higher than the threshold current. If the inductance is too small, the fault current level at the interruption instant may be higher than the breaking current rating of the bus-tie switch. On the other hand, if it is too high, the time coordination between the bus-tie switch and the fuse cannot be achieved. The second is greatly related to the capacitance in the faulty bus. This is because the higher capacitance helps not only to reduce the fault clearing time by the fuse, but also to maintain the bus voltage of the faulty feeder (see **Fig. 3.6**). For the above reasons, the influences of the inductance and the capacitance should be

examined.

When a fault occurs in one of the DC buses, the DC buses are separated first (fast action) and then the fault current provided by a generator is blocked by the power supply protection (slow action). As discussed in **Chap. 4** and **Chap. 5**, the power supply protection based on the generator deexcitation, used in this work, has a slow response and thus the rectifier should be carefully sized to sustain the relatively high fault energy limited by this method. As the synchronous generator is a critical power source in the marine networks, backup protection can be considered to improve the reliability of the protection scheme. In this case, the coordination between the deexcitation and the backup protection should be taken into account.

As the last work in the thesis, a protection scheme integrated into two-bus DC PDNs is validated by experimental DC short-circuit tests. The three-level protection is implemented in the lab-scaled test setup (fast action - bus separation by the solid-state bus-tie switch, medium action - feeder protection by the high-speed fuse, and slow action - power supply protection by the generator deexcitation). The influences of the system inductance and capacitance are investigated for the bus separation by the bus-tie switch to ensure its proper operation as well as the continuous operation of the adjacent healthy loads after the fault clearing by the fuse. Along with the investigation, the protection scheme based on the three-level protection is verified for bus and feeder faults. The test results are analyzed by comparing actual operating times of the three actions and the fault energies limited by those.

8.2 Implementation of Protection Scheme

DC faults are highly sensitive on system parameters (equivalent inductance and equivalent capacitance existed in a fault circuit) and thus their impacts on the faults should be examined to design the protection scheme. In the section, the influences of the current limiting inductance in the bus-tie switch and the DC-link capacitance are investigated with relevant experimental tests. From the investigations, the whole protection scheme and its setting are established and applied to the lab-scaled two-bus DC PDNs.

8.2.1 Protective Devices and Scheme

The solid-state bus-tie switch in the test setup (see **Fig. 6.9**) is designed to be operated by an overcurrent magnitude, the rate of overcurrent rise, and a voltage drop. Among them, the overcurrent level of 40 A (2 pu) is selected to turn *OFF* the bus-tie switch as the power rating of GEN1 is 10 kW. The current limiting inductor in the bus-tie switch is discussed in the following subsection.

For the feeder protection, IR semiconductor fuse rated for 500 Vdc and 15 A is employed [see **Fig. 8.1(c)**]. Due to the lack of its datasheet, the characteristics of the fuse is tested, as shown in **Fig. 8.4**. From the test, the fuse is characterized with its parameters: I_p (peak let-through current) - 350 A, prearcing I^2t - 11.7 A^2t, and total clearing I^2t - 37.5 A^2t.

As the power supply protection, the generator deexcitation is implemented in the PLC. Once the PLC detects the fault current, after a certain time (T_{ON_D}), the deexcitation command is sent to the AVR and then the IGBT in the AVR is turned *OFF*, as presented in **Fig. 8.1(d)**. The used parameters are $i_{threshold}$ = 40 A and T_{ON_D} = 0.1 s.

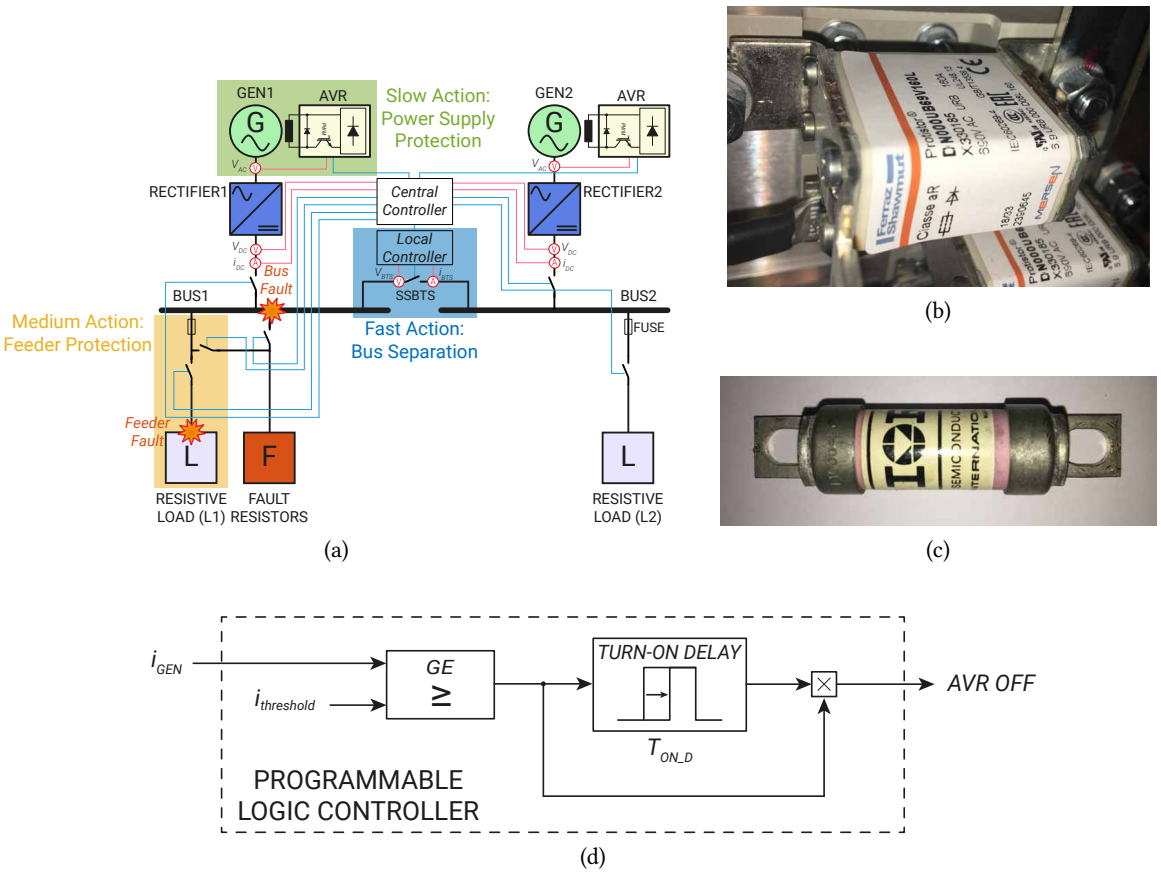


Fig. 8.1 (a) Overall diagram of protective devices, (b) rectifier fuse [139], (c) feeder fuse [140], and (d) block diagram of the deexcitation control.

Backup protection of the power supply protection is also considered in the work. Mersen AC fuses rated for 690 Vac and 160 A are installed between the generator and the rectifier [see **Fig. 8.1(b)**]. The overall diagram of the protective device is depicted in **Fig. 8.1(a)**. The protection devices and scheme, described above, are summarized in **Tab. 8.1**.

Tab. 8.1 Summary of protection scheme implemented in the test setup.

Fault Type	**Fast Action**	**Medium Action**	**Slow Action**
	Bus separation	Feeder protection	Power supply protection
			[Backup protection]
	Bus-tie switch	DC fuse	Generator deexcitation
Feeder fault	(pick up: **40** A, inst. operation)		(pick up: GEN1/GEN2 - **40**/**80** A, delay: **0.1** s)
			[AC fuse]
	Bus-tie switch		Generator deexcitation
Bus fault	(pick up: **40** A, inst. operation)		(pick up: GEN1/GEN2 - **40**/**80** A, delay: **0.1** s)
			[AC fuse]

8.2.2 Influence of the Current Limiting Inductance on the Bus Separation

A system fault in the DC networks results in a voltage drop at the faulty bus. This voltage drop generates the potential difference between the healthy bus and the faulty bus, and it produces the current flow from the healthy bus to the faulty bus. The inductor in the bus-tie switch plays a role to control the rate of the fault current rise. As mentioned, if the inductance value is not properly selected, it may cause the breaking failure (too low inductance) or the coordination failure (too high inductance).

The required inductance can be calculated by

$$L_{lim} = V_d \frac{\Delta t}{\Delta i} \tag{8.1}$$

As mentioned in **Chap. 6**, the maximum allowed current of the bus-tie switch is 200 A and it takes around 5.5 μs to interrupt the fault current after the detection. Hence, Δt and Δi in the test setup are 5.5 μs and 160 A, respectively. With these system parameters, the required inductance is 17.2 μH by the consideration of the worst condition (V_d = 500 V). However, in practice, there is no zero impedance fault and the voltage decreases with the time constant of the system capacitance and the fault resistance. This allows the networks to employ slightly lower inductance. Based on this technical review, the inductor of 16 μH, which is available in the laboratory, is installed in the bus-tie switch.

The other reason why this low inductor is employed is related to the fault detection time. High inductance value decreases the rate of the current rise and it makes the local controller needing more time to identify the fault. DC short-circuit tests with the fault resistance of 1.3 Ω are carried out to clearly show the relationship between the current limiting inductance and the rate of the current rise. The currents passing through the bus-tie switch for 16 μH and 48 μH are shown in **Fig. 8.2**. For 16 μH, the current reaches the threshold current of the bus-tie switch (40 A in the work) at 43 μs. On the other hand, it takes 155 μs in the case of 48 μH. To achieve the selectivity between the fast and medium actions, the bus separation has to be done at least within 100 μs after the fault. In other words, a high value of the current limiting inductance may cause the time coordination issue between the fast and medium actions. An example case of this issue is shown in **Fig. 8.3**.

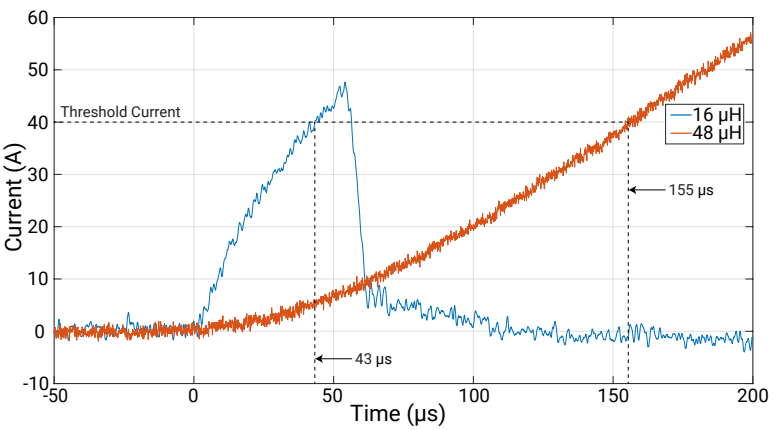


Fig. 8.2 Comparison of the rate of current rise for different current limiting inductances.

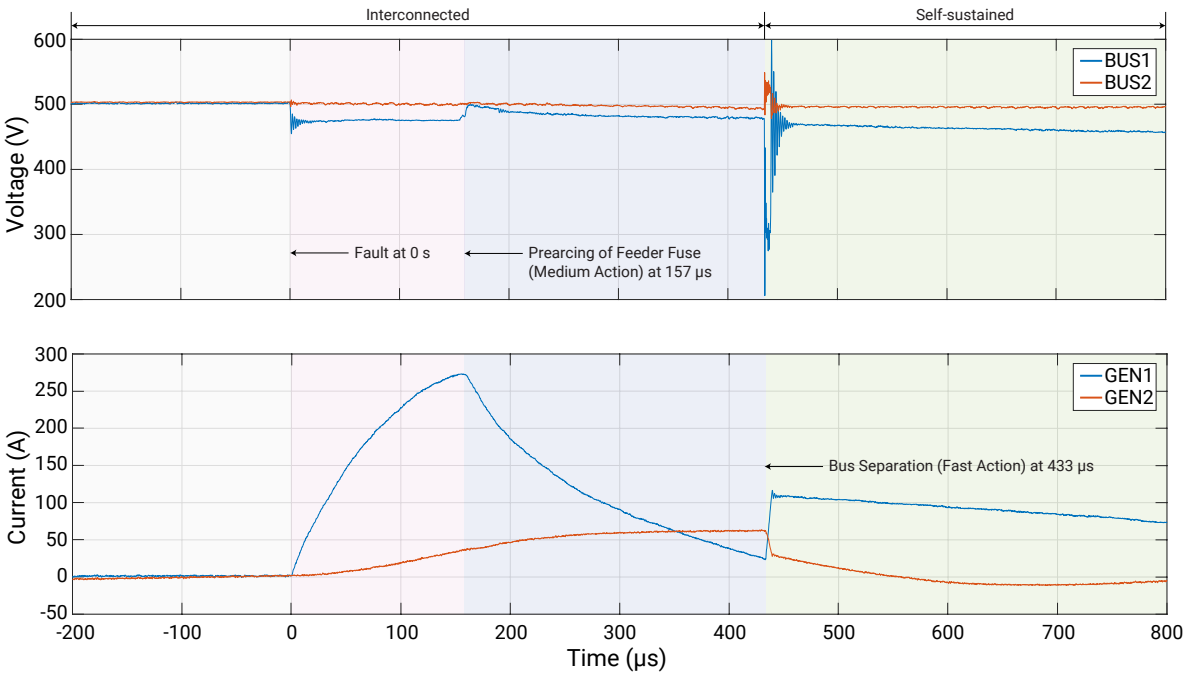


Fig. 8.3 Example case of time coordination failure. With **48** μH of the current limiting inductance, the current rise through the bus-tie switch is highly decreased. This makes the feeder fuse to be blown before the bus separation.

8.2.3 Influence of the DC-Link Capacitance

In the three-level protection, higher DC-link capacitance can help to reduce the fault clearing time of the feeder fuse and to keep the bus voltage after the fault clearance. DC short-circuit tests with the fault resistance of 1.3 Ω are conducted to investigate the influence of the DC-link capacitance. As presented in **Fig. 8.4**, when the fault occurs at BUS1, the bus-tie switch is turned *OFF* at around 50 μs and then the prearcing of the feeder fuse is started at around 170 μs. These actions are similarly observed for all the test cases. On the other hand, the fault clearing time and the bus voltage are different depending on the DC-link capacitance. For 2.3 mF, the total clearing by the fuse happens at 12.1 ms and the minimum voltage is 330 V. Those become 7.2 ms and 413 V, respectively, in case of the DC-link capacitance with 4.6 mF. By adding 2.3 mF more capacitance, the total capacitance of 6.9 mF, the voltage drop can be reduced around 0.1 pu (445 V) while there is no improvement of the total clearing time.

The lower voltage drop is more beneficial to increase the system availability by avoiding load disconnection by its undervoltage protection. Considering this, the DC-link capacitance of 6.9 mF is selected for the protection in the work.

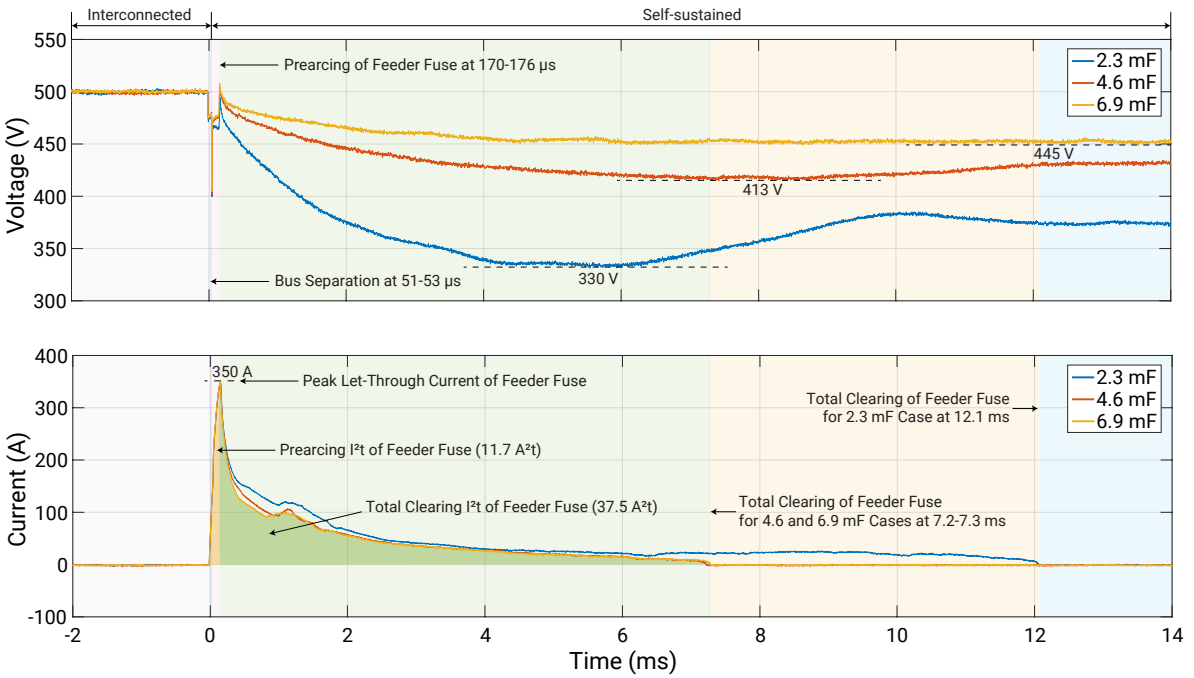


Fig. 8.4 Influence of the DC-link capacitance on the bus voltage. Higher DC-link capacitance allows for reducing the voltage drop and the fault clearing time. The IR semiconductor fuse used for the feeder protection is also characterized due to lack of its datasheet.

8.3 Protection for Bus Faults

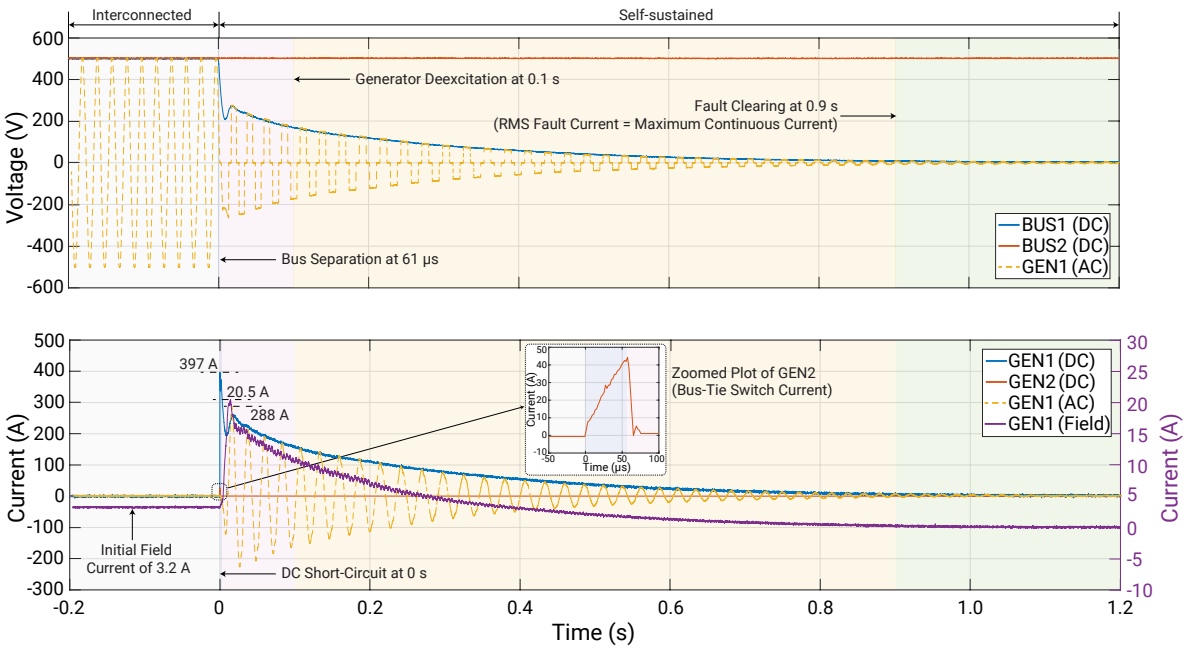
The bus protection in the test setup is verified by the DC short-circuit test on BUS1, as shown in **Fig. 8.5(a)**. The fault with its resistance of 1.3 Ω develops the voltage drop on BUS1 and it results in the current flows from GEN1 and GEN2 to the fault point. The first action happens at 61 μs and this bus separation allows BUS2 to be operated independently [see **Fig. 8.5(b)**]. On the other hand, the current from GEN1 (I_{GEN1}) continues to flow up to several seconds. The first peak of I_{GEN1} is provided by the DC-link capacitor and then the generator is the main source of the fault current. At 0.1 s, the AVR is turned *OFF* and it decreases the system voltage and the fault current.

For the analysis by using a time-current curve (TCC), the continuous-time fault current (i_F) is converted to a RMS current (i_{F_RMS}) by

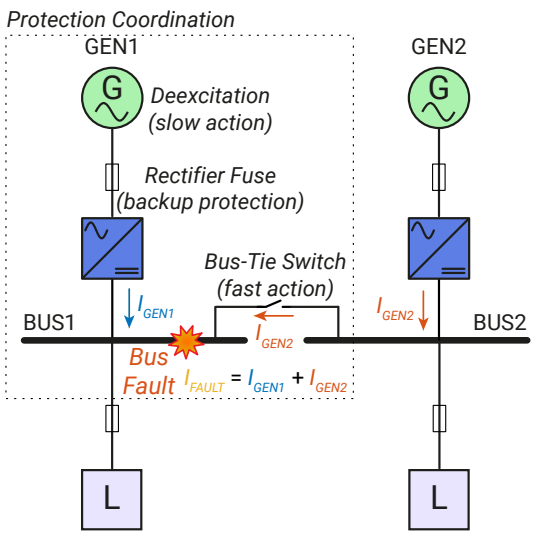
$$i_{F\_RMS} = \sqrt{\frac{1}{T}\int_0^T i_F^2\, dt} \tag{8.2}$$

The RMS current is drawn in **Fig. 8.5(c)** and compared to the operating time of the backup protection (the AC fuse). The result shows that the deexcitation effectively mitigates the fault current without the operation of the backup protection and also the time margin between them is enough.

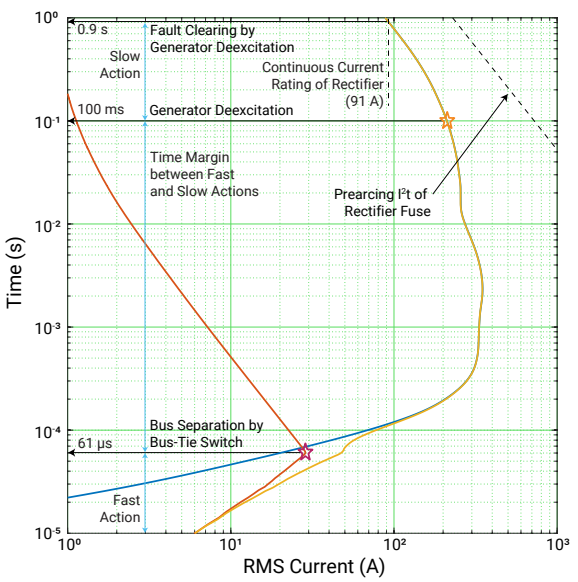
The current limited by the deexcitation is decreased exponentially, i.e., it decreases quickly first and takes a relatively long time to make it completely zero. Hence, the time when the RMS current is the same as the continuous current rating of the rectifier is selected to be a fault clearing time in the work.



(a)



(b)



(c)

Fig. 8.5 Protection for bus fault: (a) continuous-time voltage and current waveforms, (b) protection scheme diagram, and (c) time-current curve analysis. For the bus fault at BUS1, the bus-tie switch is disconnected at **61** μs (the zoomed plot is provided) and the deexcitation of GEN1 is activated at **0.1** s. The TCC analysis shows that the coordination is achieved between the bus separation and the deexcitation as well as between the deexcitation and the backup protection.

At 0.9 s, the RMS current reaches the continuous current rating of 91 A and the continuous-time current is around 6 A.

While the protection scheme is effective for the fault resistance of 1.3 Ω, its performance also has to

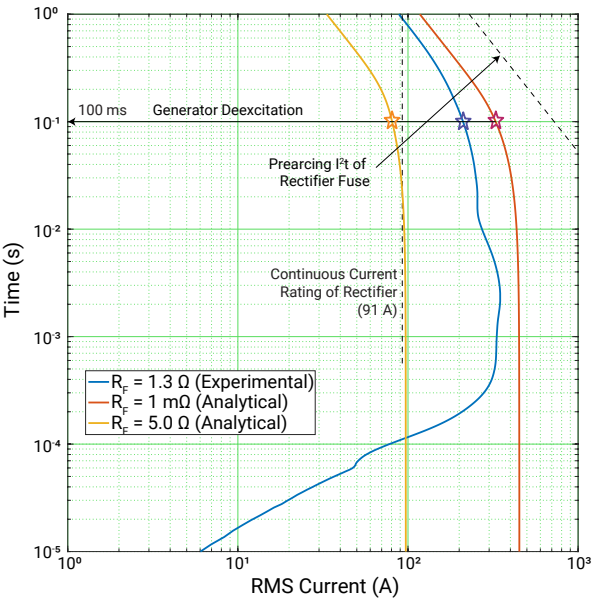


Fig. 8.6 Coordination analysis for different fault currents. All the three currents are limited by the deexcitation and the results show that the deexcitation can mange these fault conditions without the operation of the backup protection.

be proven for the maximum fault condition as well as the minimum fault condition. To check its effectiveness for the different conditions, fault currents under the fault resistances of 1 mΩ and 5 Ω are calculated by the equation introduced in **Chap. 5** [Eq. (5.8)], as the maximum and minimum fault conditions, respectively. Note that the current from the DC-link capacitor is neglected, as discussed in **Chap. 5**.

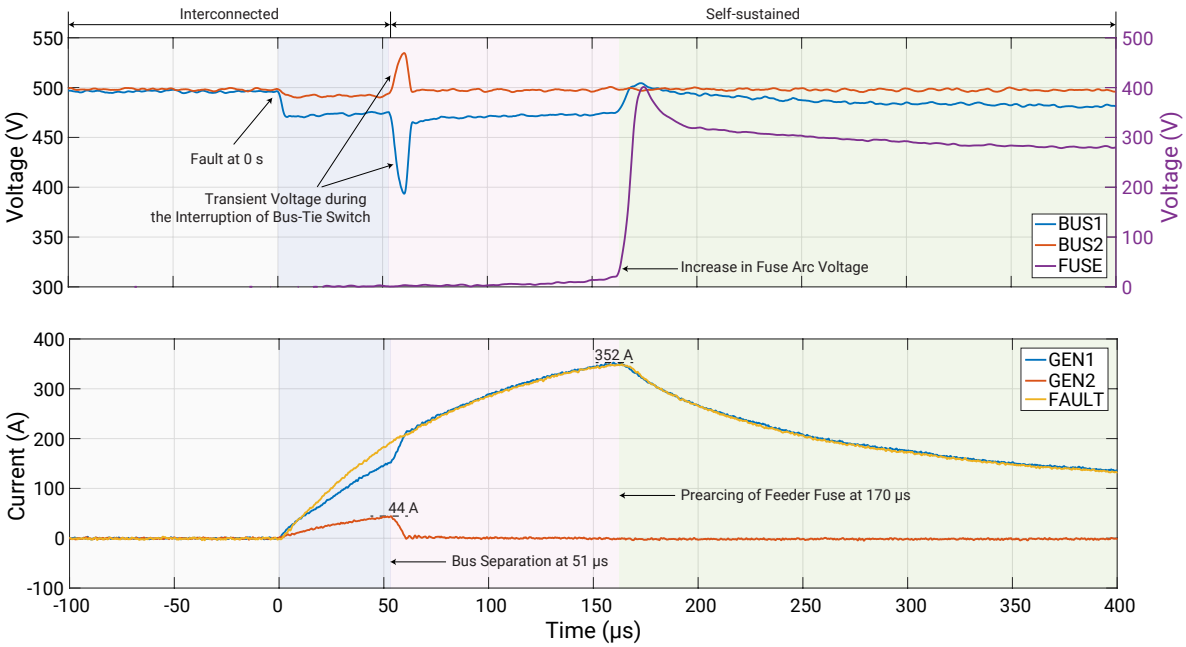
Fig. 8.6 shows that the fault current with R_F = 1 mΩ can be managed by the deexcitation without the operation of the backup protection. In case of the minimum fault (R_F = 5 Ω), the continuous-time current at 0.1 s is observed as 70 A and this current is enough to activate the deexcitation.

8.4 Protection for Feeder Faults

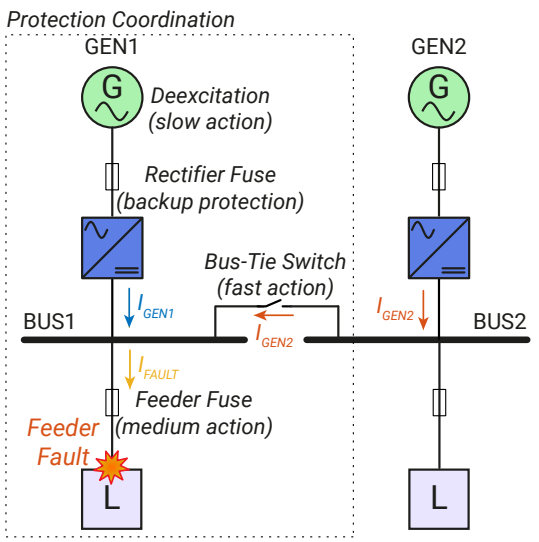
The feeder protection should be carefully coordinated due to the small time margin between the fast and medium actions. In the previous section, the influences of the current limiting inductance and the DC-link capacitance are investigated and they are selected as 16 μH and 6.9 mF, respectively. With these system parameters, a DC short-circuit test with the fault resistance of 1.3 Ω is carried out and its continuous-time waveforms are presented in **Fig. 8.7(a)**.

As presented in **Fig. 8.7(b)**, the first action is done by the bus-tie switch and then the feeder fuse isolates the feeder fault. This protection scheme is correctly operated for the DC short-circuit fault without the operation of the deexcitation. In detail, the two buses are disconnected at 51 μs after the fault and then the feeder fuse is melted at 170 μs. The prearcing (or melting) of the fuse is also observed by the sudden increase in the arc voltage at the same instant. At 7.3 ms, the fault is completely cleared by the fuse (see **Fig. 8.4**).

To verify the feeder protection for different fault conditions, the DC short-circuit currents are simulated by PLECS. The system modeling is simplified as the combination of the DC-link capacitances at both buses, the current limiting reactor with the switch (disconnected in 5.5 μs after the threshold), and the fault resistance. The ESR (38 mΩ/unit) and ESL (20 nH/unit) of the installed DC-link capacitor



(a)



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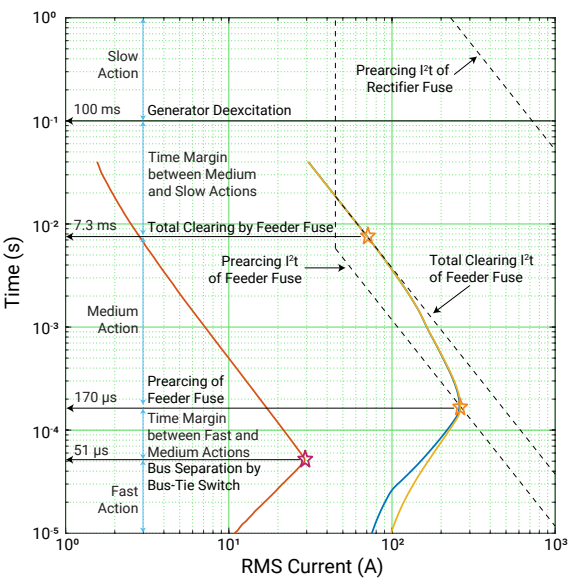

(c)

Fig. 8.7 Protection for feeder fault: (a) continuous-time voltage and current waveforms, (b) protection scheme diagram, and (c) time-current curve analysis. For the feeder fault at BUS1, the bus-tie switch is disconnected at **51** μs and the prearcing of the feeder fuse is started at **170** μs. The TCC analysis shows that the coordination is achieved between the bus separation and the feeder protection.

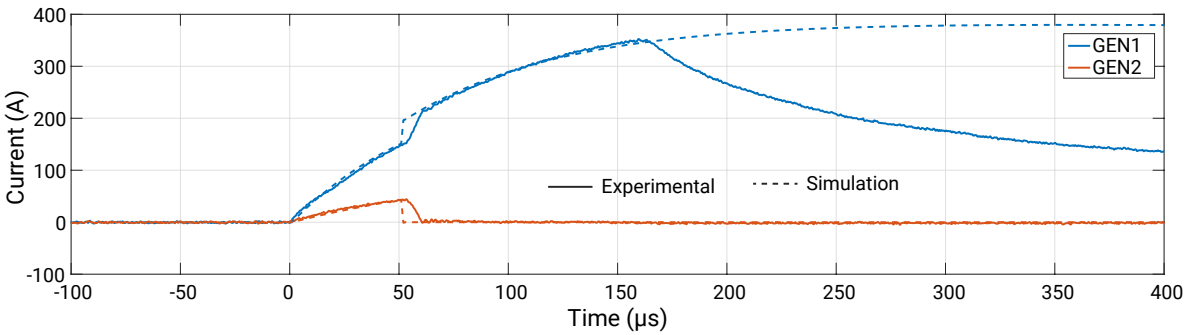

Fig. 8.8 Comparison of experimental and simulation currents.

[141] are applied to the simulation and the result is compared to the test waveforms, as shown in **Fig. 8.8**. With this simulation model, the fault currents and the bus-tie currents are calculated for the fault resistances of 1 mΩ and 5 Ω, as the maximum and minimum fault conditions. Note that the prearcing of the feeder fuse is not considered in the simulation model.

For the low impedance fault (R_F = 1 mΩ), the bus-tie switch is disconnected at 42 μs and the fault energy reaches to the prearcing rating of the feeder fuse at 111 μs. While the time margin between the actions is decreased to 69 μs (the time margin is 119 μs in case of the 1.3 Ω fault case), the coordination is still achieved. It implies that a low impedance fault develops a high fault current and this increased current reduces the operating time of the bus-tie switch as well as the feeder fuse. The bus separation is taken place with a high time delay (245 μs) for the fault of 5 Ω. Along with this delayed operation, the feeder fuse is melted slowly at 1.2 ms due to the lower fault energy. This fuse prearcing can mitigate the fault current and there may be no deexcitation action for the minimum fault condition.

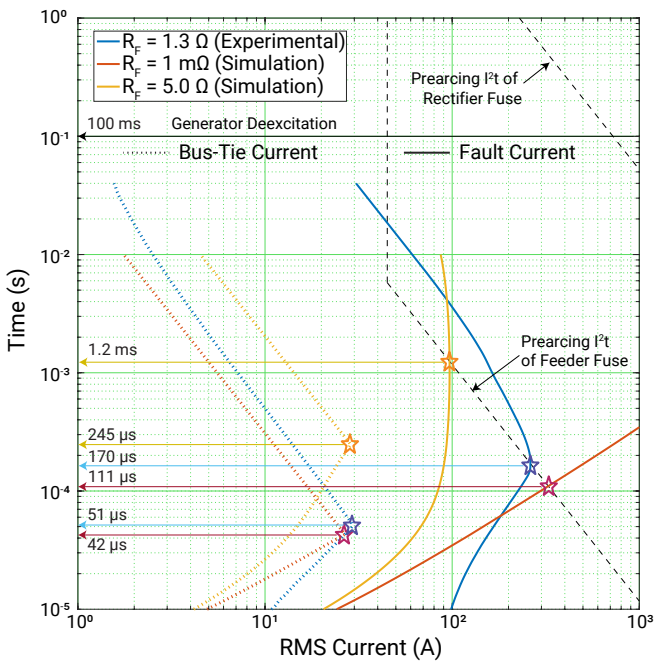

Fig. 8.9 Coordination analysis for different fault currents. As the fuse protection is not considered in the PLECS simulation, the simulated currents are not limited by the fuse unlike the experimental case.

From these investigations, the protection scheme for the feeder protection ensures the fault to be cleared with enough time margins and without the operation of the deexcitation for the possible fault conditions. It could be stated that the protection scheme has to be carefully coordinated for every DC PDNs because the protection is highly sensitive in the system parameters and the protection devices.

8.5 Conclusion

This chapter has validated the protection scheme integrated into the two-bus DC PDNs by experimental DC short-circuit tests. The protection scheme is based on the three-level protection that consists of the bus separation by the bus-tie switch, the feeder protection by the high-speed fuse, and the power supply protection by the generator deexcitation. As the backup protection of the power supply protection, the AC fuse is also installed between the generator and the rectifier.

First, the protection devices are selected with the operating time setting of the active devices (the bus-tie switch and the deexcitation). The characteristics of the feeder and AC fuses are analyzed by the short-circuit tests and from the datasheet. Secondly, the influences of the current limiting inductance in the bus-tie switch and the DC-link capacitance are investigated and their values are selected for the protection coordination. Lastly, the implemented protection scheme is verified by the DC short-circuit tests for the bus and feeder faults. To check its effectiveness for various fault conditions, the fault currents are calculated by the equation introduced in **Chap. 5** and the PLECS simulation. The calculated currents are analyzed by using the time-current curves and the results show that the protection scheme can protect the networks for the various fault conditions studied in the work.

The findings of the work can be summarized as follows. The inductance in the bus-tie switch should be thoroughly selected to ensure the fault interruption (not too small) and the coordination between the actions (not too high). The high DC-link capacitance not only allows for the lower voltage drop of the faulty feeder, but also reduces the fault clearing time by the feeder fuse. The ABC method proposed in **Chap. 3** is also validated with this investigation of the DC-link capacitor. The three-level protection can manage DC short-circuit faults with its distinctive operating times.

9
Conclusions and Future Works

This chapter summarizes the main findings and the contributions of the thesis. In addition to the summaries, future research perspectives in this topic are outlined.

9.1 Summary and Contributions

In the thesis, the technical challenges tied to protection coordination in DC PDNs have been studied. Marine applications are mainly considered for target DC PDNs because of the outstanding growth of DC PDNs-based vessels, but the work is not limited to this area alone. Along with DC PDN operations covered in two chapters (**Chap. 6** and **Chap. 7**), most of the works have been performed to demonstrate, validate, and extend the three-level protection that is the state-of-the-art protection method for marine LVDC PDNs, as analyzed in **Chap. 2**. The main outcomes of the thesis are summarized hereafter.

The additional bus capacitance (ABC) method has been proposed in **Chap. 3** to extend the selectivity and sensitivity for the feeder protection by high-speed fuses. When a fault occurs in a feeder, fault currents flow from the capacitors installed at healthy feeders and rectifiers to the fault location. These currents make the fuse on the faulty feeder to be blown and the fault can be disconnected from the networks. From the system studies, it is found that there may be the cases where the selectivity and/or the sensitivity cannot be achieved. In the proposed ABC method, additional capacitors are directly installed at the DC buses to blow the fuse on the faulty feeder under the minimum fault condition within a specified time. By providing the additional fault energy to the target fuse, the method not only allows for the fault clearing under the minimum fault condition (sensitivity), but also enables to remove the fault without the prearcing of adjacent healthy feeder fuses for the maximum fault condition (selectivity).

As the last action of the three-level protection, the power supply protection methods are examined by simulation studies in **Chap. 4**. Three available measures are characterized with DC short-circuit analyses under various conditions: diode rectifier - the high subtransient reactance combined with the generator deexcitation, thyristor rectifier - the fold-back protection control, and VSC - the high-speed fuses. Furthermore, the artificial short-circuit method has been proposed to overcome a low reliability issue of the fuse solution for VSCs. The study results have proven that the method effectively limits the fault energy through VSCs by providing a low impedance path between the generator and the rectifier. Further investigations on the deexcitation have been conducted in **Chap. 5**. The analytical expression is introduced for the deexcitation and it is verified by experimental tests. In **Chap. 5**, the deexcitation is characterized by analytical calculation as well as experimental tests for different

system factors: subtransient reactances, fault resistances, DC-link capacitances, exciter types, and time delays. The analysis results are summarized. High subtransient reactance is effective to reduce the initial DC fault current, but the effect of the fault energy mitigation is not high due to the short subtransient period. Low fault resistance develops high DC fault current, while the resistance is not controllable in practice. DC-link capacitance only has a direct impact on the first peak DC fault current developed and it is not a crucial element for the rectifier sizing. Faster exciter response and less time delay aid to mitigate the fault energy.

The protection scheme is implemented and integrated into the two-bus DC PDNs in **Chap. 8**. The scheme is based on the three-level protection and consists of the bus separation by the solid-state bus-tie switch, the feeder protection by the high-speed fuse, and the power supply protection by the generator deexcitation. As the backup protection of the power supply protection, the AC fuses are installed between the generator and the rectifier. To coordinate each protection action, the influences of the inductance in the bus-tie switch and the DC-link capacitance are investigated by the DC short-circuit tests with the different inductances and capacitances. It is observed that the operation of the bus-tie switch is sensitive in the inductance value and it has to be selected with thorough system studies to interrupt the fault current within its breaking capability and to quickly identify the fault. The ABC method proposed in **Chap. 3** is validated with the investigation of the DC-link capacitance. The high DC-link capacitance helps to clear the fault quickly and allows for the lower voltage drop of the faulty feeder. The whole protection scheme is verified by the experimental tests with the bus and feeder faults. To verify the scheme for various fault conditions, the maximum and minimum fault currents are calculated by the equation introduced in **Chap. 5** for the bus faults and by the PLECS simulation for the feeder faults. The time-current curve analyses show that the integrated protection scheme can protect the two-bus DC PDNs for various fault conditions with the correct operation of protection measures and enough time margins between the different protections.

The operating modes of the two-bus DC PDNs have been demonstrated without ESSs in **Chap. 6** and with ESSs in **Chap. 7**. In **Chap. 6**, the DC voltage regulation and the power sharing function are implemented by combining the main controller and the AC AVR to maintain the bus voltage within tolerance and to share loads in proportion to the generator power ratings, respectively. The soft start function of the bus-tie switch, which is to smoothly charge the potential from one bus to the other bus, makes DC PDNs to be synchronized without any limitations and this allows to extend operation sequence and modes of DC PDNs. The seamless transition between open-bus and closed-bus operations is demonstrated by using the ultra-fast bus-tie switch. To provide electric power to the microgrid in case of the generator failure in the microgrid, the seamless transition is implemented in the two-bus DC PDNs. The experimental tests show that the power source can be transmitted promptly if one bus experiences a power outage during the open-bus operation.

Supercapacitor-based energy storage systems are integrated into the DC PDNs through DC-DC converters in **Chap. 7**. The main benefits of the ESS integration, which are mostly related to fuel savings and environmental compliance in a port or during the approach to a port, are demonstrated with three operating modes. First, the ESSs are used for flattening the generator load to maintain the generator load within optimal operating ranges and reduce the number of running generators (load leveling). Secondly, the performance of the DC PDNs is greatly improved by the droop control of the ESSs (transient mitigation). With this control, the ESSs mitigate the sudden load changes with their short time constants and make the actual generator load softer. Furthermore, the test proves that regenerative energy in the networks can be stored in the ESSs. Lastly, the zero-emission mode is

fully demonstrated in the test setup with the power droop control of the ESSs. The demonstrated zero-emission mode is characterized by several power source transitions from onboard generators to ESSs during the approach to a port, from ESSs to grids in a port, from grids to ESSs during leaving a port, and from ESSs to onboard generators.

9.2 Overall Conclusion

The transition from AC to DC is ongoing in PDNs, more obviously in the marine domain. One of the main bottlenecks in DC technologies is the protection coordination due to no natural current zero-crossing and low overloading capability of power converters. In the thesis, the protection scheme based on the three-level protection has been verified for the two-bus DC PDNs and extended with the proposed methods. Furthermore, each protection measure has been investigated with system studies and experimental tests. The outcomes of the thesis provide system design engineers with the information on the protection coordination. Furthermore, the proposed methods (the ABC method and the artificial short-circuit method) and the introduced equation on the deexcitation can be applied to improve the system protection in practice.

9.3 Future Works

This work has covered the individual protection measures and the integrated protection scheme with the scrutinized technical discussions on the protection coordination. Nevertheless, considering the complexity in the protection coordination and the move towards MVDC, there are lots of technical gaps to be studied in future. Future research perspectives in this topic are outlined hereafter.

9.3.1 Protection Scheme for MVDC PDNs

The success story of LVDC PDNs in marine applications may motivate to take MVDC technologies in this domain. This is because LVDC solutions are limited in system voltage of around 1 kV and power ratings up to 20 MW. For the bigger-size higher-powered ships, MVDC solutions are necessary to reduce power losses and to minimize the size and installation number of power cables. Same as the LVDC PDNs, the protection scheme is a crucial point to support this cutting-edge technology to be a commercial solution.

9.3.2 Hybrid AC-DC Protection Coordination

While the distribution network is formed with DC, the power generation and consumption have still relied on mature and economic AC technologies. The protection of conventional AC protection should consequently be coordinated with the newly employed DC protection. For the reliable hybrid AC-DC protection coordination, several differences between both systems have to be taken into account: equipment overloading capabilities, fault characteristics, protection schemes, and protective devices.

9.3.3 Development of Cost-Effective DC Circuit Breakers

As analyzed in **Chap. 2**, every solution has its solid-state bus-tie switch. However, except The Switch solution, the use of the solid-state switch is limited only for the bus-tie purpose due to its high cost. On the other hand, while the high-speed fuse is an economic solution to interrupt a fault current, its uncertain and passive operation makes the protection coordination difficult. Hence, cost-effective DC circuit breakers should be studied and developed for incoming and outgoing feeder protection.

Appendices

A

DC Short-Circuit Current Equation

A current of the initial DC fault is mainly contributed by capacitors installed in converters because a capacitor has a much faster response time than AC generators. Hence, an equivalent circuit for the initial peak current can be assumed as a series RLC circuit in **Fig. A.1**.

By using Kirchhoff's voltage law (KVL) the differential equation for the circuit is

$$L_{eq}\frac{di_F}{dt} + R_{eq}i_F + \frac{1}{C_{eq}}\int_{t_0}^{t} i_F \mathrm{d}t - V_{DC0} = 0 \tag{A.1}$$

By differentiating (A.1) with respect to time and dividing L_{eq}

$$\frac{d^2 i_F}{dt^2} + \frac{R_{eq}}{L_{eq}}\frac{di_F}{dt} + \frac{1}{L_{eq}C_{eq}}i_F = 0 \tag{A.2}$$

and its characteristics equation is

$$\lambda^2 + \frac{R_{eq}}{L_{eq}}\lambda + \frac{1}{L_{eq}C_{eq}} = 0 \tag{A.3}$$

and thus

$$\lambda_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \tag{A.4}$$

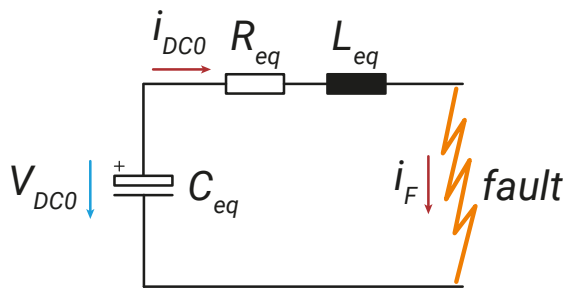

Fig. A.1 Equivalent circuit for initial DC fault.

where

$$\alpha = \frac{R_{eq}}{L_{eq}} \text{ and } \omega_0 = \frac{1}{\sqrt{L_{eq}C_{eq}}}$$

Due to low resistance and inductance in the circuit the equation has typically the underdamped response ($\alpha < \omega_0$) and it is

$$i_F(t) = e^{-\alpha t}(A_1 \cos \omega_d t + A_2 \sin \omega_d t) \tag{A.5}$$

where

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \tag{A.6}$$

With the two initial conditions ($v(0) = V_{DC0}$ and $i_F(0) = i_{DC0}$), we can obtain

$$i_F(0) = i_{DC0} = A_1 \tag{A.7}$$

and

$$\frac{\mathrm{d}i_F(0)}{\mathrm{d}t} = \frac{V_{DC0}}{L_{eq}} = -\alpha i_{DC0} + \omega_d A_2 \tag{A.8}$$

$$A_2 = \frac{\alpha i_{DC0}}{\omega_d} + \frac{V_{DC0}}{\omega_d L_{eq}} \tag{A.9}$$

Therefore, the current is

$$\begin{aligned} i_F(t) &= \frac{V_{DC0}}{\omega_d L_{eq}} e^{-\alpha t} \sin \omega_d t + \frac{\omega_0}{\omega_d} i_{DC0} e^{-\alpha t}\left(\frac{\omega_d}{\omega_0} \cos \omega_d t + \frac{\alpha}{\omega_0} \sin \omega_d t\right) \\ &= \frac{V_{DC0}}{\omega_d L_{eq}} e^{-\alpha t} \sin \omega_d t + \frac{\omega_0}{\omega_d} i_{DC0} e^{-\alpha t}\left(\frac{\omega_d}{\sqrt{\omega_d^2 + \alpha^2}} \cos \omega_d t + \frac{\alpha}{\sqrt{\omega_d^2 + \alpha^2}} \sin \omega_d t\right) \\ &= \frac{V_{DC0}}{\omega_d L_{eq}} e^{-\alpha t} \sin \omega_d t + \frac{\omega_0}{\omega_d} i_{DC0} e^{-\alpha t}\left(\sin\left(\arctan \frac{\omega_d}{\alpha}\right) \cos \omega_d t + \cos\left(\arctan \frac{\omega_d}{\alpha}\right) \sin \omega_d t\right) \end{aligned} \tag{A.10}$$

By using the fact that $\sin(\alpha + \beta) = \sin\alpha\cos\beta + \cos\alpha\sin\beta$ and substituting $\beta = \arctan\frac{\omega_d}{\alpha}$, the final current is

$$i_F(t) = \frac{V_{DC0}}{\omega_d L_{eq}} e^{-\alpha t} \sin\omega_d t + \frac{\omega_0}{\omega_d} i_{DC0} e^{-\alpha t} \sin(\omega_d t + \beta) \tag{A.11}$$

B

Time Domain Simulation Models

This appendix presents the time domain simulation models for the three-rectifier systems. The models by the EMTP-RV software are used for the analyses in **Chap. 4**.

B.1 Diode Rectifier-Based PDNs

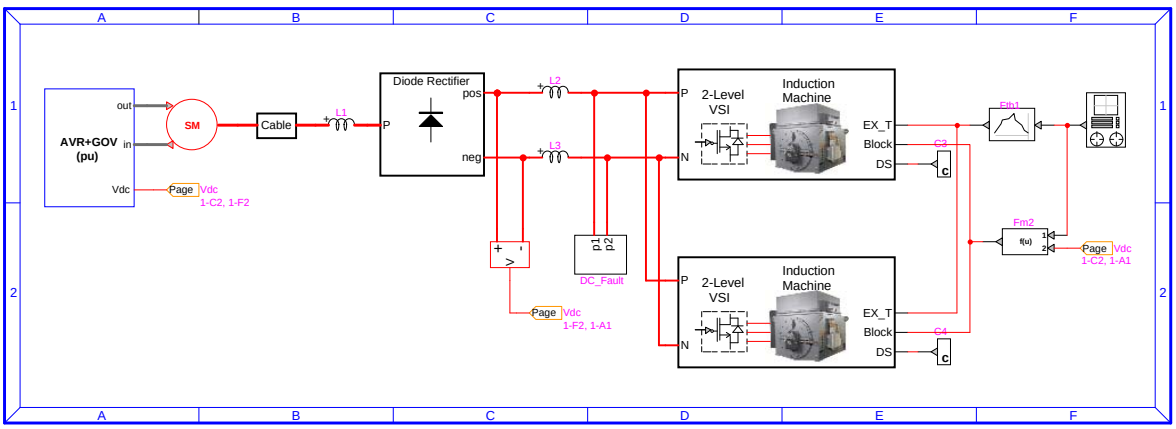

Fig. B.1 Time domain simulation model for the diode rectifier-based PDNs.

B.2 Thyristor Rectifier-Based PDNs

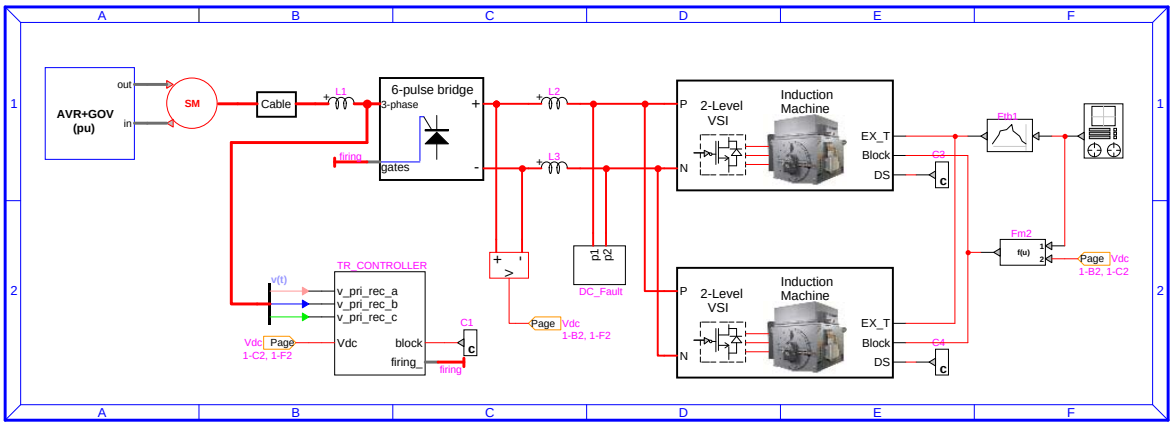

Fig. B.2 Time domain simulation model for the thyristor rectifier-based PDNs.

B.3 VSC-Based PDNs

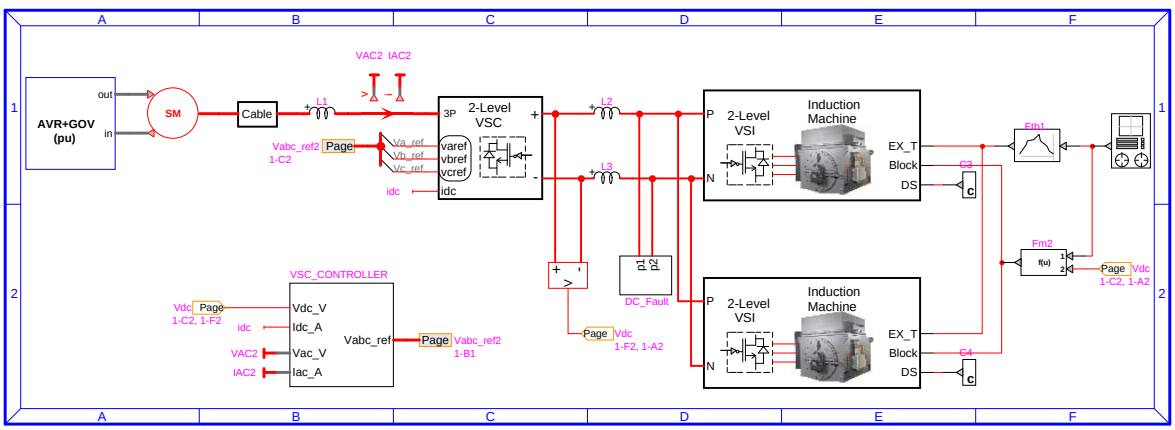

Fig. B.3 Time domain simulation model for the VSC-based PDNs.

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